Design Example Report

Title	***High Efficiency 12 V, 30 W Standby Power Supply Using TOPSwitch®-JX TOP265EG***
Specification	110 VDC – 400 VDC Input; 12 V, 2.5 A, Output
Application	PC Standby Supply
Author	Applications Engineering Department
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Revision	1.4

Summary and Features

- Highly energy efficient
    - Full load efficiency >90%
    - Efficiency >87% above 10% load
    - Average efficiency >90% (25%, 50%, 75%, 100% load points)
    - No-load input power <100 mW
    - Simplifies meeting ENERGY STAR 2.0, 80 Plus and EuP requirements
    - 725 V MOSFET rating allowed high turns ratio (VOR) and use of 60 V Schottky output diode
- Low cost, low component count and small PCB footprint solution
    - Performance met without synchronous output rectification
    - 132 kHz operation optimized core size and efficiency performance
    - Low-profile eSIP package
- Integrated Protection and Reliability Features
    - Line under-voltage lock out (UVLO)
    - Primary sensed latching output overvoltage shutdown (OVP) with fast AC reset
    - Auto recovery output over current (OCP)
    - Meets limited power source (LPS) <100 VA requirement with a single point of failure
    - Accurate thermal shutdown with large hysteresis
- 5 V version of design available - see DER-247

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing standby power supply utilizing a TOPSwitch-JX TOP265EG. This power supply is intended as a general purpose evaluation platform that operates from 110 VDC to 400 VDC input and provides a 12 V, continuous 30 W output.

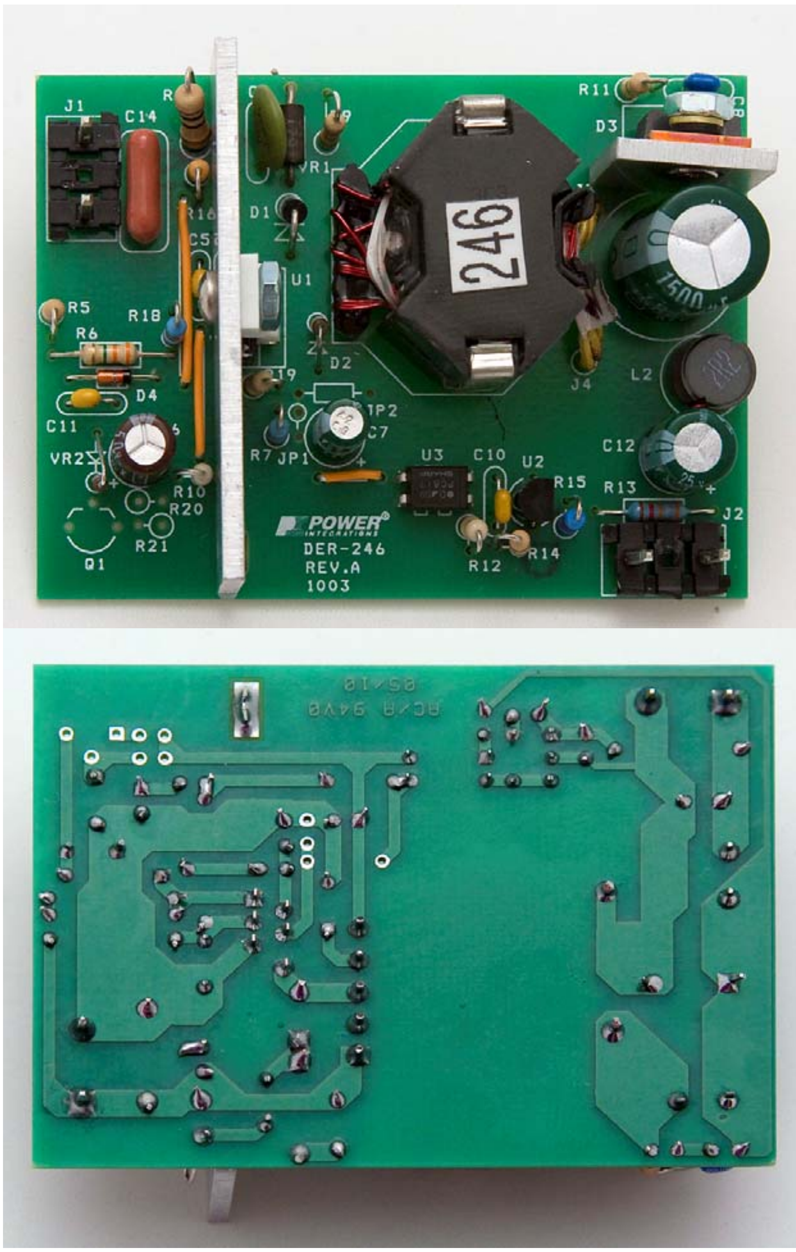

Figure 1 – Populated Circuit Board Photograph (2.97 x 2.14 inches).

This standby supply was designed to meet 80 Plus Standard and Energy star 2.0 >87% average-efficiency, no-load <100 mW at 400 VDC.

This power supply offers these various protection features for few component counts:

- Overvoltage protection (OVP) with latching shutdown and optional fast AC reset
- Primary-side sensed output overload protection, even with a single fault
- Latching open-loop protection
- Auto-restart overload protection
- Accurate thermal overload protection with auto-recovery using a large hysteresis

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	110		400	VDC	
No-load Input Power (400 VDC)				0.1	W	
Output						
Output Voltage	V_{OUT1}		12		V	± 5%
Output Ripple Voltage	$V_{RIPPLE1}$			120	mV	20 MHz bandwidth
Output Current	I_{OUT1}	0		2.5	A	
Total Output Power						
Continuous Output Power	P_{OUT}		30		W	
Efficiency						
Full Load	η	89			%	Measured at P_{OUT} 25 °C
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	$\eta_{ES2.0}$	87			%	Per ENERGY STAR V2.0
Protection						
Over Power				60	W	Auto-recovery
Over-Voltage				22	VDC	Latching
Environmental						
Safety		Designed to meet IEC950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0	25	40	°C	Free convection, sea level

3 Schematic

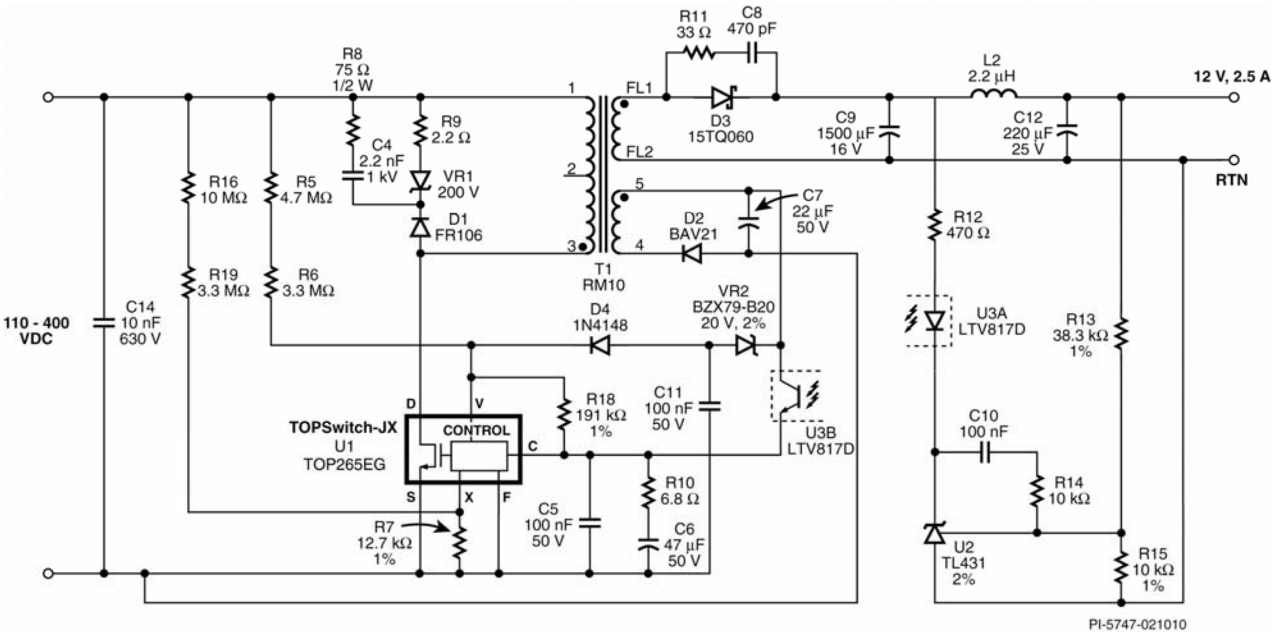

Figure 2 – Schematic.

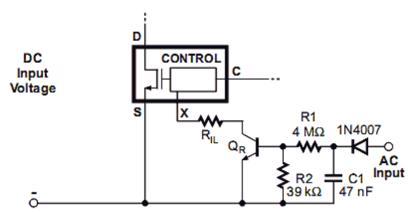

Figure 3 – Fast AC Reset Circuit.

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4 Circuit Description

This flyback converter configuration, built around the TOP265EG (U1), provides a 12 V output, and delivers a load current of 2.5 A. This power supply operates over an input range of 110 VDC to 400 VDC. The output is regulated using voltage reference U3.

4.1 TOPSwitch Primary

Resistors R5 and R6 provide a current into the V pin of U1 proportional to the DC voltage across high voltage bypass capacitor C14. Resistor R18 provides a bias current into the V pin to reduce the current drawn from the DC bus via R5 and R6. The value shown set the undervoltage threshold to 80 V DC, the point at which current into the V pin exceeds 25 µA. At this point switching is enabled and the power supply starts up.

An RCDZ clamp network (D1, R8, R9, C4 and VR1) limits the drain voltage of U1 to below 725 V after the MOSFET inside U1 turns OFF. This configuration was selected as it maximizes efficiency across the load range.

Diode D2 rectifies the bias winding output of transformer T1, and C7 filters it. This provides the necessary bias supply for the optocoupler U3B. The voltage across C7 was adjusted via the bias winding turns to be ~9 V at no-load and 400 VDC input. This both minimizes no-load consumption and ensures the output remains in regulation.

The secondary-side feedback circuitry maintains output voltage regulation via U3A. A change in current through the optocoupler diode causes a change in the current out of the optocoupler transistor (which is proportional to the CTR of the optocoupler) and into U1's C pin. Current into the C pin changes the duty cycle of the internal MOSFET thereby regulating the output voltage.

Zener diode VR2 provides output over-voltage protection. Any fault condition which causes the power supply output to exceed regulation limits also causes the voltage across the bias winding to increase. Consequently, Zener diode VR2 breaks down and sufficient current flows into the V pin of U1 via D4 to initiate OVP. A resistor can be added in series with VR2 that limits the current into the V pin and changes the latching to self-recovering shutdown.

Resistors R7, R16 and R19 provide output power limiting, maintaining relatively constant overload power with input voltage.

4.2 Output Rectification

Diode D3 provides rectification for the 12 V output, and low-ESR capacitor C9 provides filtering. To eliminate high frequency switching noise, a post filter was added (L2 and C12).

The snubber network comprised of R11 and C8 damp oscillations on D3 caused by the transformer winding leakage inductance, reducing radiated EMI and diode voltage stress.

The high turns ratio (VOR of 120 V) allowed selection of a 60 V Schottky to reduce diode loss due to lower V_F vs. a higher voltage rating diode. This was possible while still maintaining adequate margin to the BV_{DSS} rating of the primary MOSFET due to its 725 V rating vs. the typical 600 V / 650 V rating of the MOSFET in other solutions.

4.3 Output Feedback

The output voltage is controlled using shunt regulator U2. Resistors R13 and R15 sense the output voltage, forming a resistor divider connected to the reference input of U2. Changes in the output voltage and hence the voltage at the reference input of U2 results in changes in the anode and therefore optocoupler LED current. This changes the current into the CONTROL pin of U1 and acts to maintain output regulation.

Resistor R14 and capacitor C10 adjust the frequency response of the feedback circuit to achieve stable power supply operation.

Resistor R12 sets the overall loop gain and limits current through U3A during transient conditions.

To reduce feedback dissipation (and lower no-load consumption) a D rank optocoupler was selected with the value of R12 increased to offset the increase in loop gain.

4.4 Fast AC Reset

The TOPSwitch-JX family has a fast AC reset function which can be configured on the X pin (as shown in Figure 3). Should the device stop switching due to a latching OVP fault condition, the circuit connected to the X pin will force I_X to exceed $I_{X(TH)}$ = -27 μA (typ) and reset the latch when the AC input is disconnected or falls below a set threshold value.

In Figure 3, R1, R2 and C1 set the time after AC is removed before the latch is reset. A higher gain BJT Q_R is desirable to allow a higher resistance value for R1 and lower capacitance value for C1, and thus minimize the circuit dissipation.

Consult Application Note AN-47 TOPSwitch-JX Family Design Guide for further information.

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5 PCB Layout

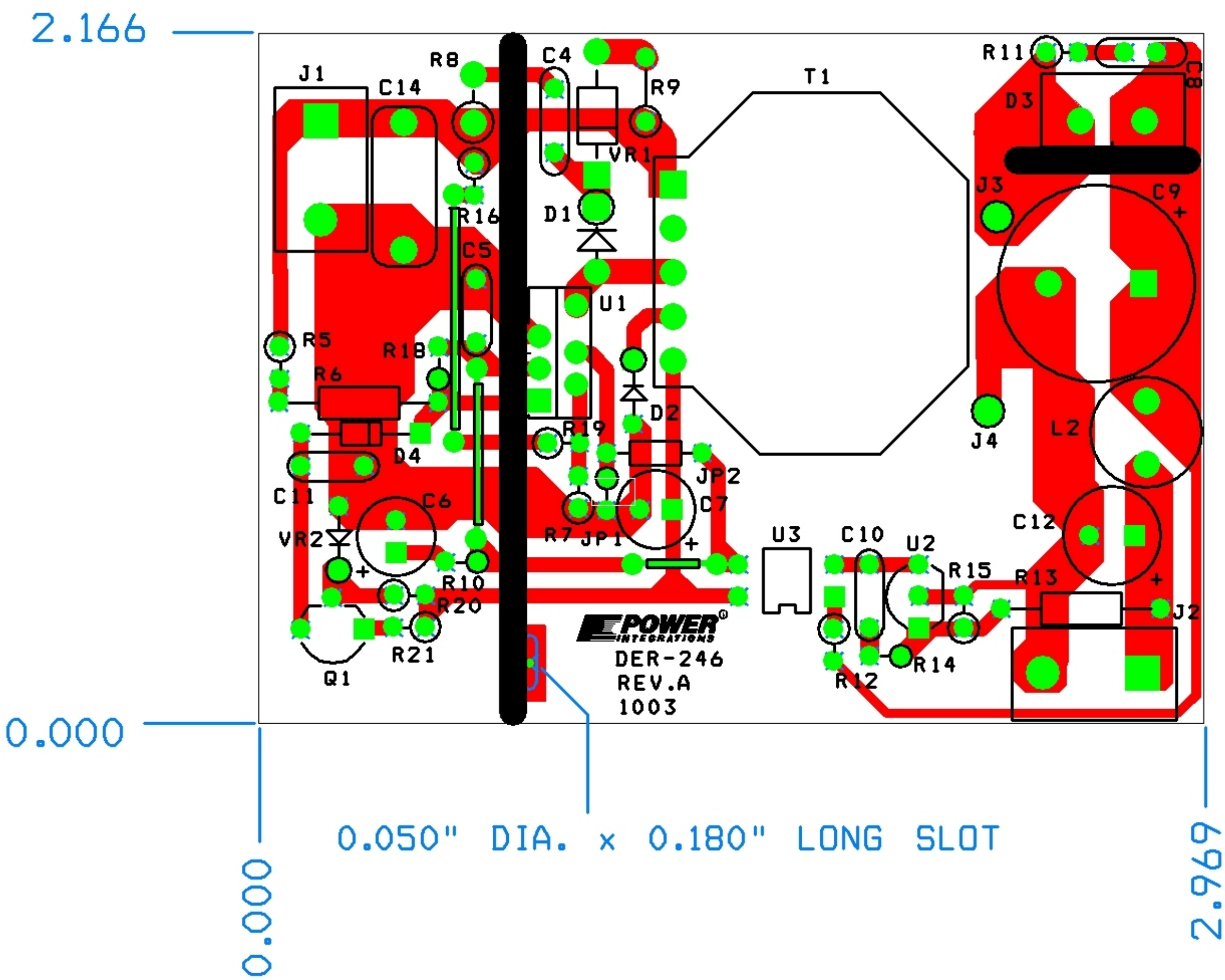

Figure 4 – Printed Circuit Layout

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C4	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC Components
2	3	C5 C10 C11	100 nF, 50 V, Ceramic, X7R	RPER71H104K2K1A03B	Murata
3	1	C6	47 μF, 50 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG500ELL470MF11D	Nippon Chemi-Con
4	1	C7	22 μF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
5	1	C8	470 pF, 100 V, Ceramic, X7R	B37981M1471M000	Epcos
6	1	C9	1500 μF, 16 V, Electrolytic, Very Low ESR, 21 mΩ, (12.5 x 20)	EKZE160ELL152MK20S	Nippon Chemi-Con
7	1	C12	220 μF, 25 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE250ELL221MHB5D	Nippon Chemi-Con
8	1	C14	10 nF, 630 V, Film	ECQ-E6103KF	Panasonic
9	1	D1	800 V, 1 A, Fast Recovery Diode, 500 ns, DO-41	FR106	Diodes Inc.
10	1	D2	250 V, 250 mA, Fast Switching, DO-35	BAV21	Vishay
11	1	D3	60 V, 15 A, Schottky, TO-220AC	15TQ060	Internation Rectifier
12	1	D4	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
13	1	L2	2.2 μH, 6.0 A	RFB0807-2R2L	Coilcraft
14	1	R5	4.7 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-4M7	Yageo
15	2	R6 R19	3.3 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-3M3	Yageo
16	1	R7	12.7 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-12K7	Yageo
17	1	R8	75 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-75R	Yageo
18	1	R9	2.2 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-2R2	Yageo
19	1	R10	6.8 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-6R8	Yageo
20	1	R11	33 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-33R	Yageo
21	1	R12	470 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-470R	Yageo
22	1	R13	38.3 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-38K3	Yageo
23	1	R14	10 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-10K	Yageo
24	1	R15	10 kΩ, 1%, 1/4 W, Metal Film	ERO-S2PHF1002	Panasonic
25	1	R16	10 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-10M	Yageo
26	1	R18	191 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-191K	Yageo
27	1	T1	Bobbin, RM10, Vertical, 5 pins	P-1031	Pin Shine
28	1	U1	TOPSwitch-JX, TOP265EG, eSIP-7C	TOP265EG	Power Integrations
29	1	U2	2.495 V Shunt Regulator IC, 2%, 0 to 70C, TO-92	TL431CLPG	On Semiconductor
30	1	U3	Optocoupler, 35 V, CTR 300-600%, 4-DIP	LTV-817D	Liteon
31	1	VR1	200 V, 1.5 W, DO-41	BZY97C200	FAGOR
32	1	VR2	20 V, 500 mW, 2%, DO-35	BZX79-B20	Vishay

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7 Transformer Specification

7.1 Electrical Diagram

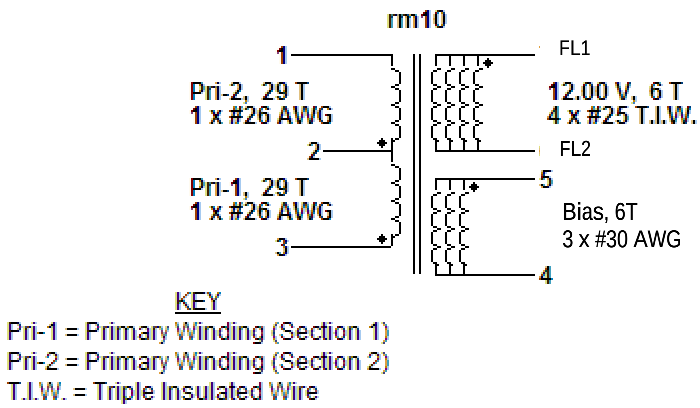

Figure 5 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Specification
Electrical Strength, VAC	60 Hz 1 second, from pins 1, 2, 3, 4, 5 to pins FL1, FL2.	3000
Nominal Primary Inductance,	Measured at 1 V pk-pk, typical switching frequency, between pin 1 to pin 3, with all other Windings open.	2140 μH ±7%
Maximum Primary Leakage,	Measured between pin 1 to pin 3, with all other Windings shorted.	25.0 μH

7.3 Materials

Item	Description
[1]	Core: rm10, 3F3 or Equivalent, gapped for ALG of 645 nH/t²
[2]	Bobbin: Generic, 5 pri. + 0 sec.
[3]	Barrier Tape: Polyester film (1 mil base thickness), 9.60 mm wide
[4]	Separation Tape: Polyester film (1 mil base thickness), 9.6 mm wide
[5]	Varnish
[6]	Magnet Wire: #26 AWG, Solderable Double Coated
[7]	Triple Insulated Wire: #25 AWG
[8]	Magnet Wire: #30 AWG, Solderable Double Coated

7.4 Comments

1.	Use of a grounded flux-band around the core may improve the EMI performance.
2.	For non margin wound transformers use triple insulated wire for all secondary windings.

7.5 Mechanical Diagram

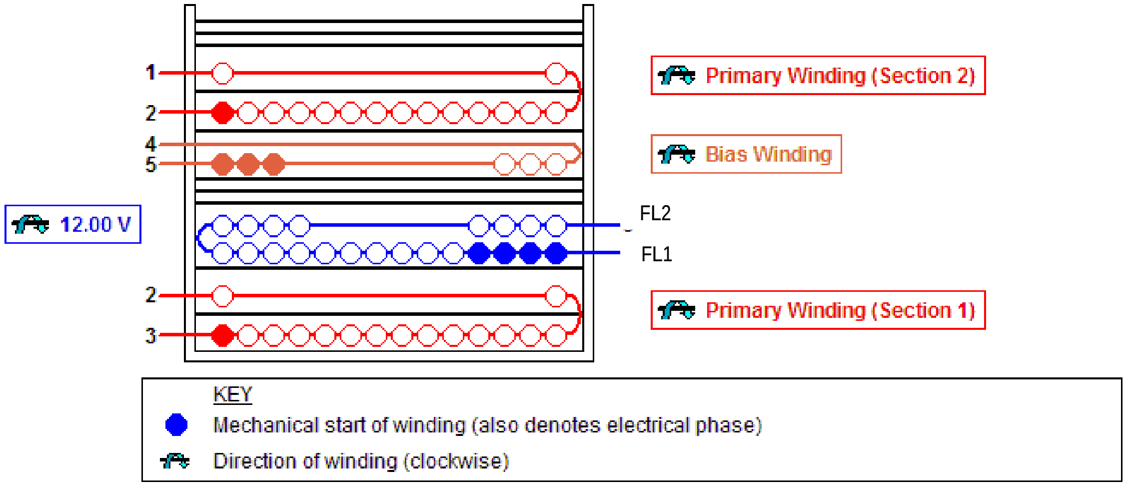

Figure 6 – Transformer Build Diagram.

7.6 Winding Instructions

Primary Winding (Section 1)	Start on pin(s) 3 and wind 29 turns (x 1 filar) of item [6] in 2 layer(s) from left to right. Add 1 layer of tape, item [4], in between each primary winding layer. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 2. Add 1 layer of tape, item [3], for insulation.
Secondary Winding	Start on pin(s) FL1* and wind 6 turns (x 4 filar) of item [7]. Spread the winding evenly across entire bobbin. Wind in same rotational direction as primary winding. Finish this winding on pin(s) FL2*. Add 3 layers of tape, item [3], for insulation.
Bias Winding	Start on pin(s) 5 and wind 6 turns (x 3 filar) of item [8]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 4. Add 1 layer of tape, item [3], for insulation.
Primary Winding (Section 2)	Start on pin(s) 2 and wind 29 turns (x 1 filar) of item [6] in 2 layer(s) from left to right. Add 1 layer of tape, item [4], in between each primary winding layer. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1. Add 3 layers of tape, item [3], for insulation.
Core Assembly	Assemble and secure core halves. Item [1].
Varnish	Dip varnish uniformly in item [5]. Do not vacuum impregnate.

* Flying lead. Flying leads were required for this design to meet safety spacing requirements, The RM10 bobbin spacing from core to secondary pins is less than the required >6 mm.

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8 Transformer Design Spreadsheet

ACDC_TOPSwitchJX_091609; Rev.1.11; Copyright Power Integrations 2009	INPUT	INFO	OUTPUT	UNIT	TOP_JX_091609: TOPSwitch-JJX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (main)
PO_AVG	30.00			Watts	Average Output Power
PO_PEAK			30.00	Watts	Peak Output Power
N	0.89			%/100	Efficiency Estimate
Z	0.50				Loss Allocation Factor
VB	12	*Info*		Volts	Ensure proper operation at no load.
tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	220.0		220	uFarads	Input Filter Capacitor
ENTER TOPSWITCH-JX VARIABLES					
TOPSwitch-JX	**TOP265EG**			Universal / Peak	115 Doubled/230V
Chosen Device		*TOP265EG*	Power Out	57 W / 57 W	81W
KI	0.46				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			0.727	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			0.837	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	**f**		f		Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
fS			132000	Hertz	TOPSwitch-JX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			119000	Hertz	TOPSwitch-JX Minimum Switching Frequency
fSmax			145000	Hertz	TOPSwitch-JX Maximum Switching Frequency
High Line Operating Mode			FF		Full Frequency, Jitter enabled
VOR	120.00			Volts	Reflected Output Voltage
VDS			10	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.35	*Info*			A minimum KP of 0.4 is recommended for Low Line or Universal input supplies.
PROTECTION FEATURES					
LINE SENSING					
VUV_STARTUP			94	Volts	Minimum DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			445	Volts	Typical DC Bus Voltage at which power supply will shut-down (Max)
RLS			4.0	M-ohms	Use two standard, 2 M-Ohm, 5% resistors in series for line sense functionality.
OUTPUT OVERVOLTAGE					
VZ			22	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					
Overload Current Ratio at			1.2		Enter the desired margin to current

VMAX					limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN			1.07		Margin to current limit at low line.
ILIMIT_EXT_VMIN			0.68	A	Peak primary Current at VMIN
ILIMIT_EXT_VMAX			0.49	A	Peak Primary Current at VMAX
RIL			13.16	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**rm10**		rm10		Core Type
Core		*#N/A*		*P/N:*	#N/A
Bobbin		*#N/A*		*P/N:*	#N/A
AE	0.8900		0.89	cm^2	Core Effective Cross Sectional Area
LE	3.3900		3.39	cm	Core Effective Path Length
AL	5200.0		5200	nH/T^2	Ungapped Core Effective Inductance
BW	9.6		9.6	mm	Bobbin Physical Winding Width
M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00				Number of Primary Layers
NS	6		6		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN	110		110	Volts	Minimum DC Input Voltage
VMAX	380		380	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.55		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.31	Amps	Average Primary Current (calculated at average output power)
IP			0.68	Amps	Peak Primary Current (calculated at Peak output power)
IR			0.24	Amps	Primary Ripple Current (calculated at average output power)
IRMS			0.42	Amps	Primary RMS Current (calculated at average output power)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2139	uHenries	Primary Inductance
LP Tolerance	7		7		Tolerance of Primary Inductance
NP			58		Primary Winding Number of Turns
NB			6		Bias Winding Number of Turns
ALG			645	nH/T^2	Gapped Core Effective Inductance
BM			2841	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			3736	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			497	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1576		Relative Permeability of Ungapped Core
LG			0.15	mm	Gap Length (Lg > 0.1 mm)
BWE			28.8	mm	Effective Bobbin Width
OD			0.50	mm	Maximum Primary Wire Diameter including insulation
INS			0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.43	mm	Bare conductor diameter
AWG			26	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			256	Cmils	Bare conductor effective area in circular mils
CMA		*Warning*	612	Cmils/Amp	!!! DECREASE CMA> (decrease L(primary layers),increase NS,smaller

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					Core)
Primary Current Density (J)			3.26	Amps/mm^2	!!! Info. Primary current density is low. Can increase Primary current density. Reduce primary layers, or use smaller core
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			6.54	Amps	Peak Secondary Current
ISRMS			3.66	Amps	Secondary RMS Current
IO_PEAK			2.50	Amps	Secondary Peak Output Current
IO			2.50	Amps	Average Power Supply Output Current
IRIPPLE			2.68	Amps	Output Capacitor RMS Ripple Current
CMS			733	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.73	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.60	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.44	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			616	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			52	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			52	Volts	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12	Volts	Output Voltage
IO1_AVG			2.50	Amps	Average DC Output Current
PO1_AVG			30.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			6.00		Output Winding Number of Turns
ISRMS1			3.663	Amps	Output Winding RMS Current
IRIPPLE1			2.68	Amps	Output Capacitor RMS Ripple Current
PIVS1			52	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			733	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			1.60	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2_AVG				Amps	Average DC Output Current
PO2_AVG			0.00	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.34		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					

VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.34		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			30	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Note - The warning about high CMA indicates that this may be an overdesign. This indicates that it may be possible to use thinner gauge wire.

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9 Heatsink (U1)

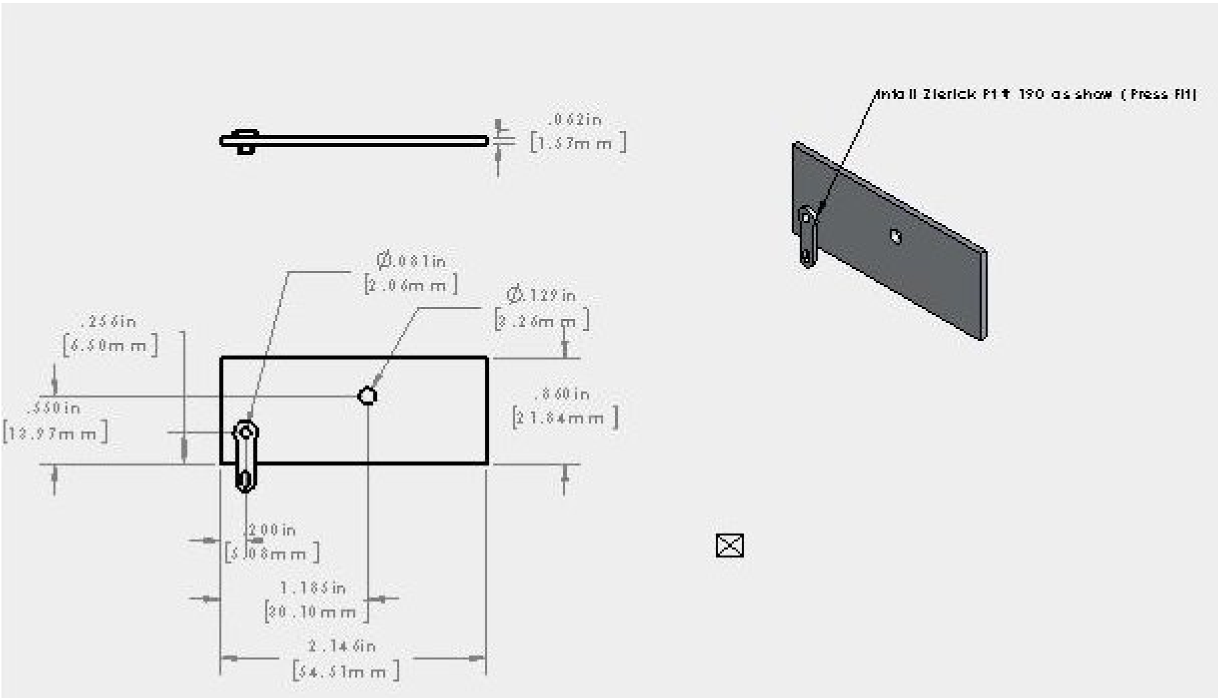

Figure 7 – Heatsink for U1.

10 Performance Data

All measurements performed at room temperature, and DC input supply

10.1 Full load Efficiency

Efficiency data points were recorded after 30 minutes soak time at 25 ºC ambient.

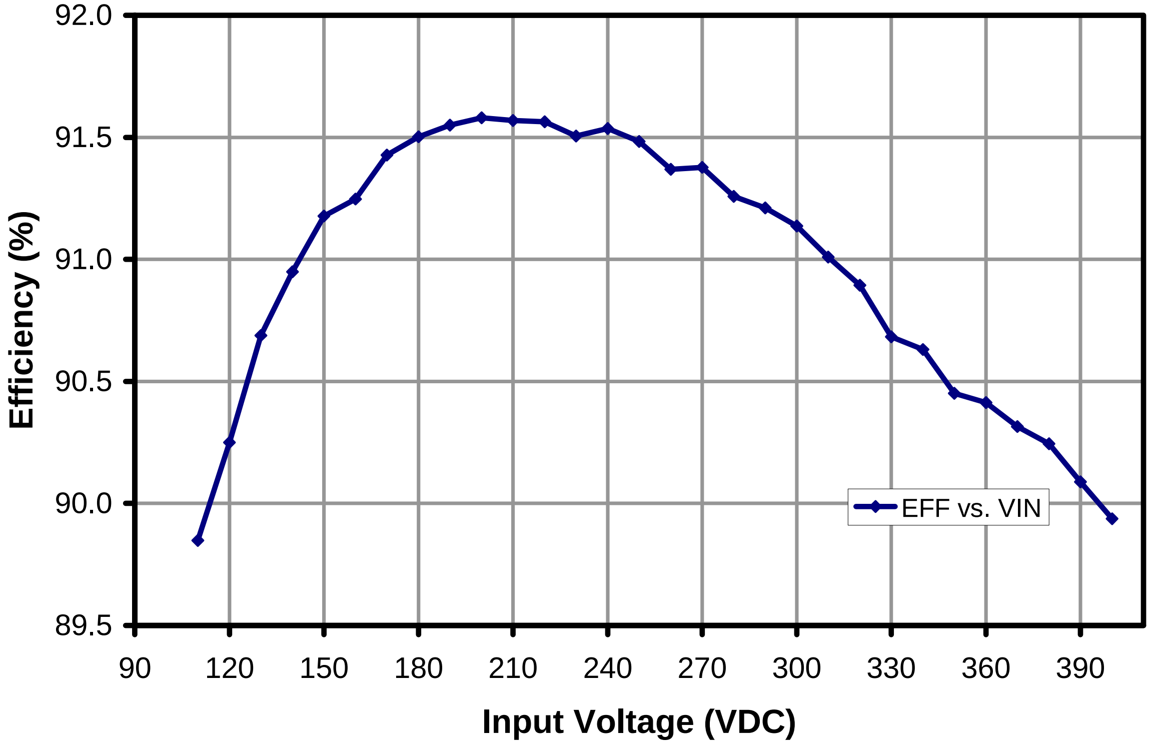

Figure 8 – Efficiency vs. Input Voltage, Room Temperature.

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V_{IN} (VDC)	I_{IN} (A)	V_O (VDC)	I_O (A)	Efficiency (%)
400	0.0836	12.03	2.5	89.937
390	0.0856	12.03	2.5	90.088
380	0.0877	12.03	2.5	90.245
370	0.09	12.03	2.5	90.315
360	0.0924	12.03	2.5	90.413
350	0.095	12.03	2.5	90.451
340	0.0976	12.03	2.5	90.631
330	0.1005	12.03	2.5	90.683
320	0.1034	12.03	2.5	90.894
310	0.1066	12.03	2.5	91.010
300	0.11	12.03	2.5	91.136
290	0.1137	12.03	2.5	91.211
280	0.1177	12.03	2.5	91.258
270	0.1219	12.03	2.5	91.377
260	0.1266	12.03	2.5	91.369
250	0.1315	12.03	2.5	91.483
240	0.1369	12.03	2.5	91.536
230	0.1429	12.03	2.5	91.505
220	0.1493	12.03	2.5	91.564
210	0.1564	12.03	2.5	91.569
200	0.1642	12.03	2.5	91.580
190	0.1729	12.03	2.5	91.550
180	0.1826	12.03	2.5	91.502
170	0.1935	12.03	2.5	91.427
160	0.206	12.03	2.5	91.247
150	0.2199	12.03	2.5	91.178
140	0.2362	12.03	2.5	90.949
130	0.2551	12.03	2.5	90.688
120	0.2777	12.03	2.5	90.250
110	0.3043	12.03	2.5	89.849

Table 1 – Data for Efficiency in Figure 8.

10.2 Active Mode Efficiency

Data are gathered at the following load points 0, 1, 2, 3, 4, 5, 10, 15, 20, 25, 30, 40, 50, 60, 70, 75, 80, 90 and 100 % load with 380 VDC input voltage.

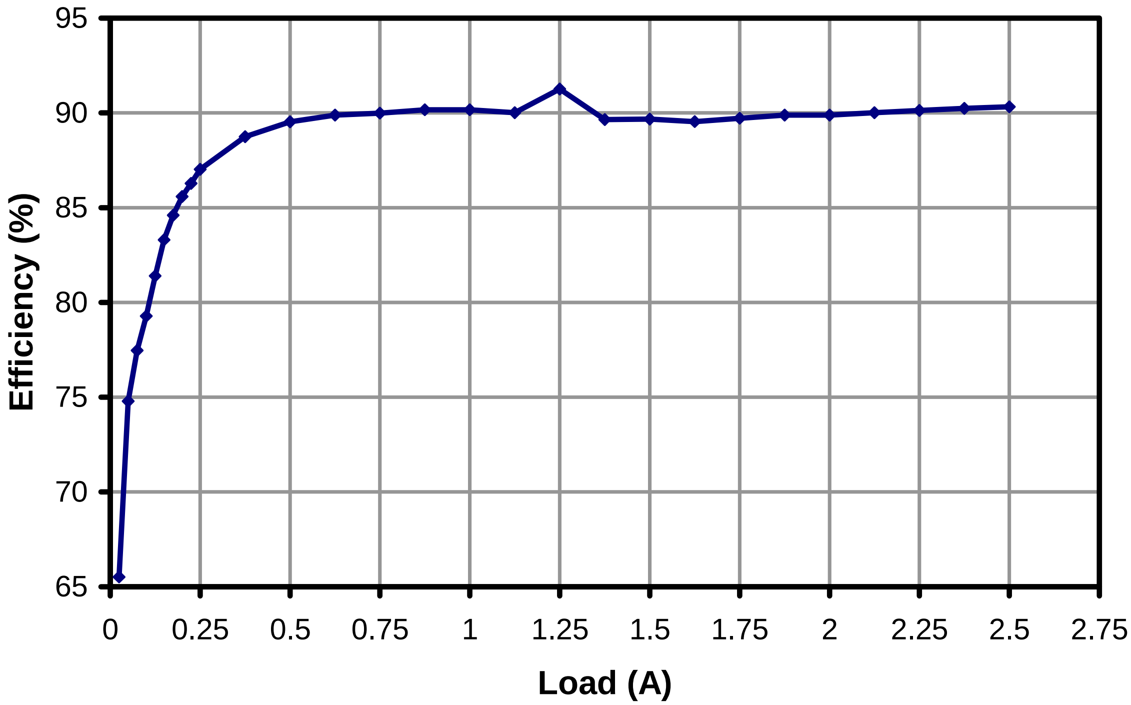

Figure 9 – Efficiency vs. Load (10 – 100%), Room Temperature.

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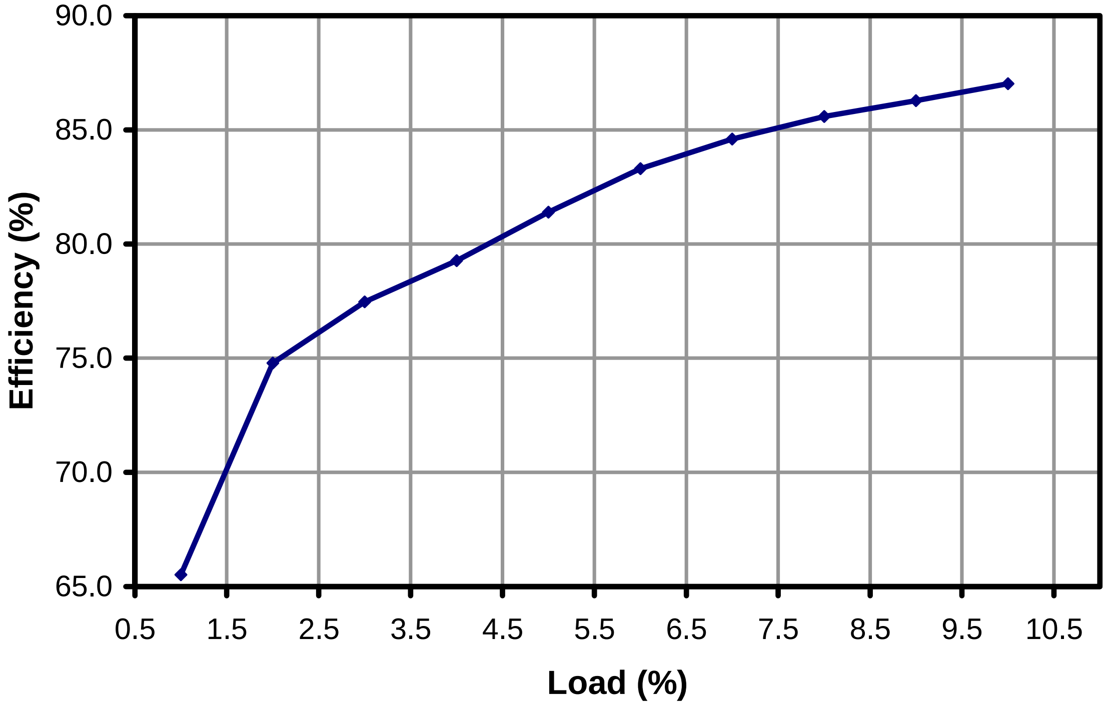

Figure 10 – Efficiency vs. Load (1 – 10%), Room Temperature.

Percent of Load (%)	Efficiency (%)
	230 VAC
100	90.32
50	91.26
20	89.53
10	87.02

Table 2 – Active Efficiency Data at 380 VDC Input.

V_{IN} (VDC)	I_{IN} (A)	V_O (VDC)	I_O (A)	Efficiency (%)	Load (%)
380	0.0877	12.04	2.5	90.320	100
380	0.0834	12.04	2.375	90.228	95
380	0.0791	12.04	2.25	90.126	90
380	0.0748	12.04	2.125	90.012	85
380	0.0705	12.04	2	89.884	80
380	0.0661	12.04	1.875	89.876	75
380	0.0618	12.04	1.75	89.721	70
380	0.0575	12.04	1.625	89.542	65
380	0.053	12.04	1.5	89.672	60
380	0.0486	12.04	1.375	89.642	55
380	0.0434	12.04	1.25	91.256	50
380	0.0396	12.04	1.125	90.012	45
380	0.03514	12.04	1	90.166	40
380	0.03075	12.04	0.875	90.158	35
380	0.02643	12.05	0.75	89.984	30
380	0.02205	12.05	0.625	89.882	25
380	0.01771	12.05	0.5	89.527	20
380	0.0134	12.05	0.375	88.742	15
380	0.00911	12.05	0.25	87.021	10
380	0.00827	12.05	0.225	86.274	9
380	0.00741	12.05	0.2	85.588	8
380	0.00656	12.05	0.175	84.594	7
380	0.00571	12.05	0.15	83.303	6
380	0.00487	12.05	0.125	81.393	5
380	0.004	12.05	0.1	79.276	4
380	0.00307	12.05	0.075	77.469	3
380	0.00212	12.05	0.05	74.789	2
380	0.0012	12.05	0.025	65.518	1

Table 3 – 380 VDC Active Mode Efficiency Data**.**

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10.3 Energy Efficiency Requirements

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

10.3.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

10.3.2 ENERGY STAR EPS Version 2.0
This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq$ 550 mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

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10.4 No-load Input Power

DC input supply without EMI filter.

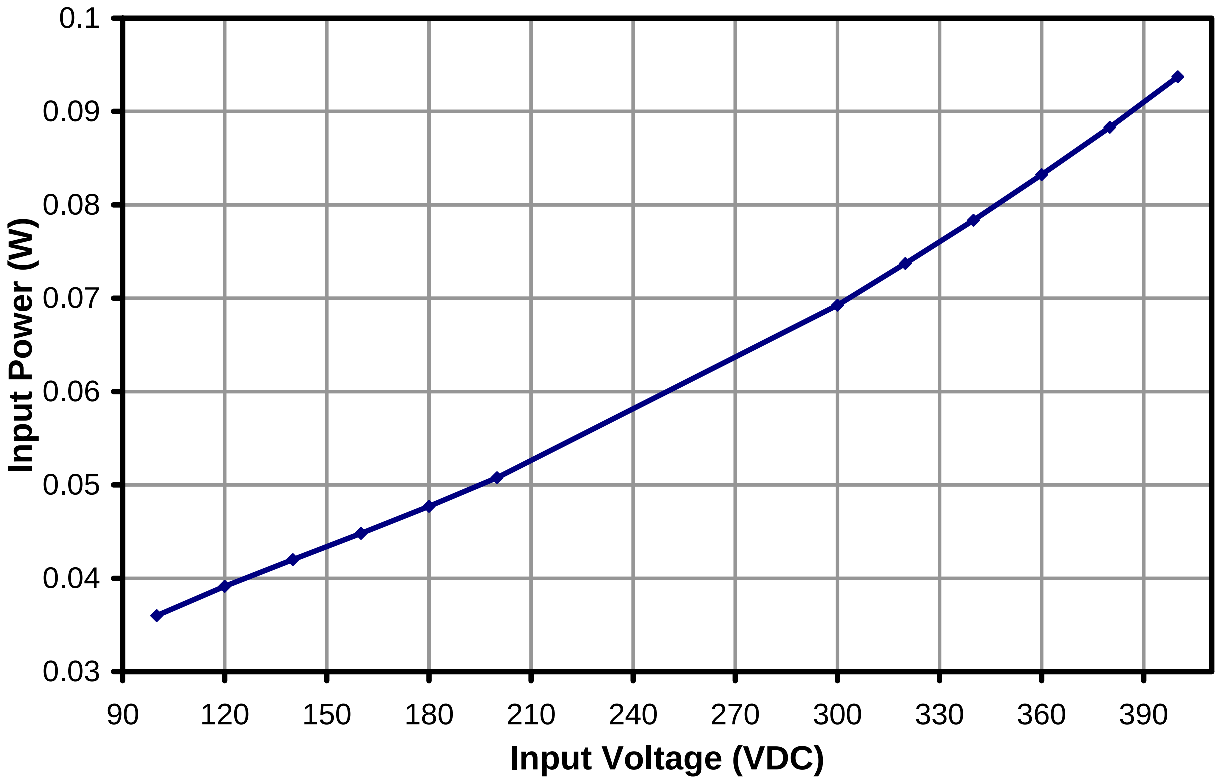

Figure 11 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

V_{IN} (VDC)	I_{IN} (A)	P_{IN} (W)
400	0.000234	0.094
380	0.000232	0.088
360	0.000231	0.083
340	0.00023	0.078
320	0.00023	0.074
300	0.000231	0.069
200	0.000254	0.051
180	0.000265	0.048
160	0.00028	0.045
140	0.0003	0.042
120	0.000326	0.039
100	0.00036	0.036

Table 4 – No-load Input Power Data in Figure 11.

10.5 Regulation

10.5.1 Load Regulation

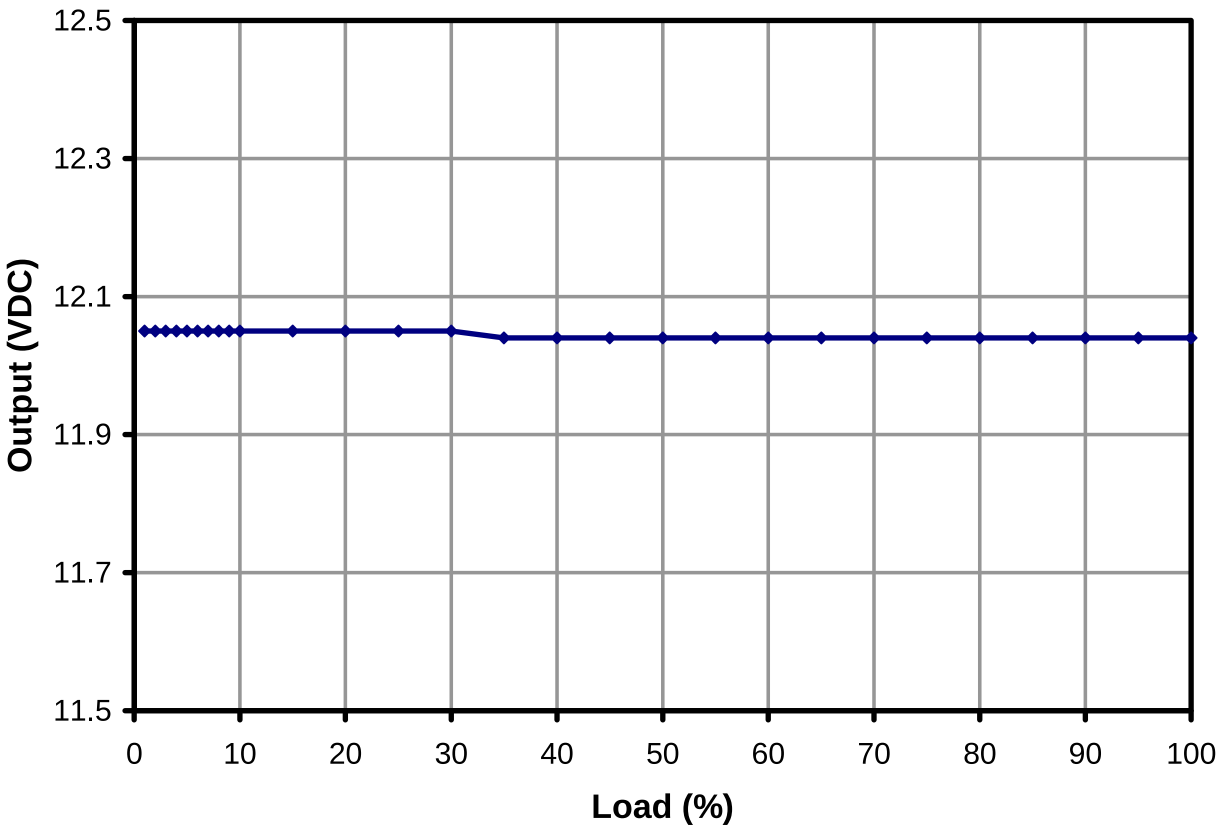

Figure 12 – Load Regulation, Room Temperature.

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10.5.2 Line Regulation

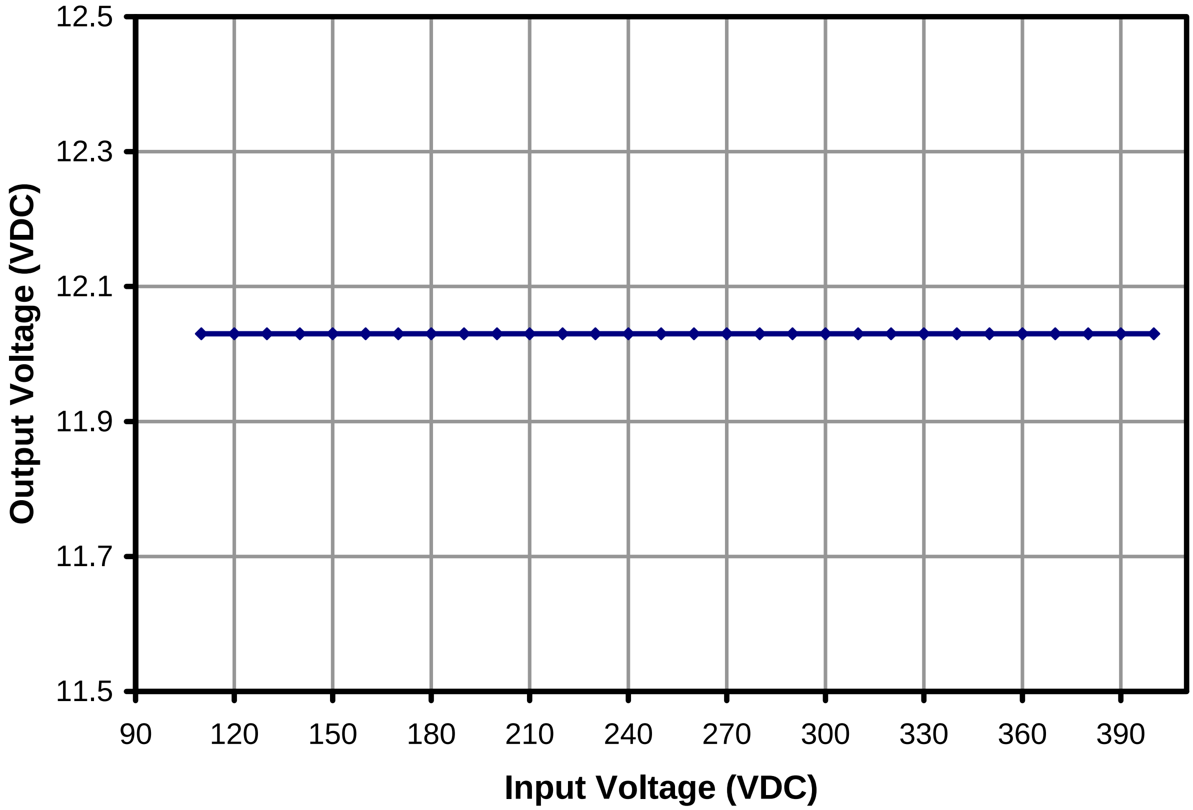

Figure 13 – Line Regulation, Room Temperature, Full Load.

11 Thermal Performance

Test result after 2 hours running continuously at full-load at 110 VDC open frame on bench

Item	Temperature (°C)
	110 VDC
Ambient	25
Transformer core (T1)	48.5
Output diode (D3)	85.3
TOP265(U1)	63.1

Figure 14 – Temperature Data.

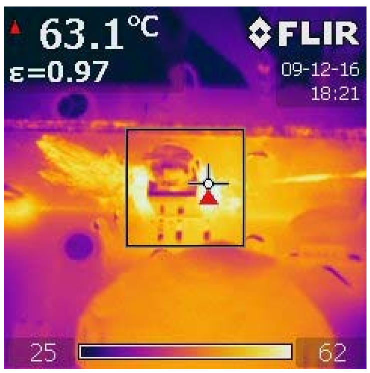

Figure 15 – U1 Thermal Scan.

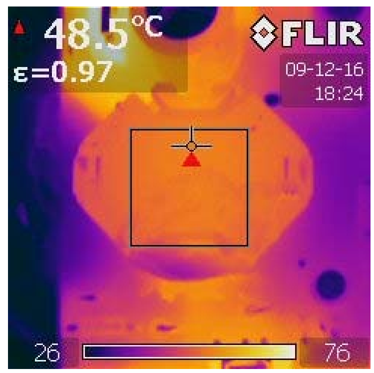

Figure 16 – T1 Thermal Scan.

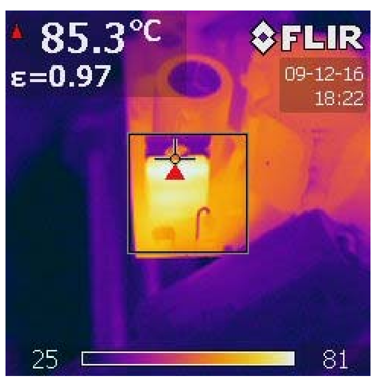

Figure 17 – D3 Thermal Scan.

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12 Waveforms

12.1 Drain Voltage and Current, Normal Operation

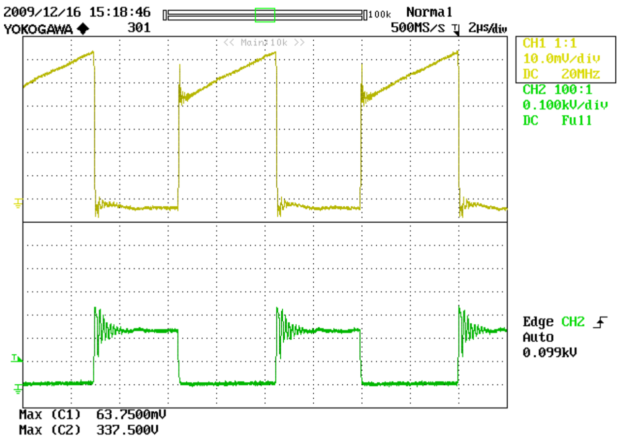

Figure 18 – 110 VDC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div., 2 μs / div.

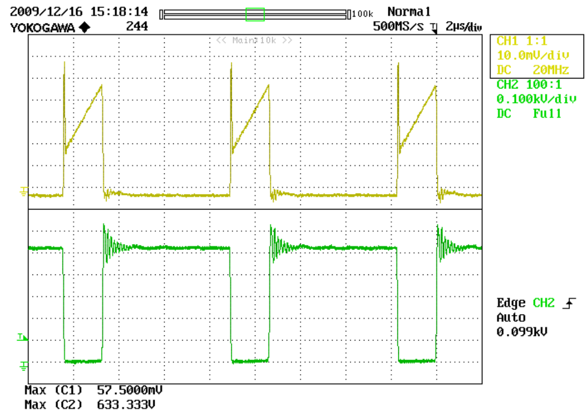

Figure 19 – 400 VDC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div., 2 μs / div.

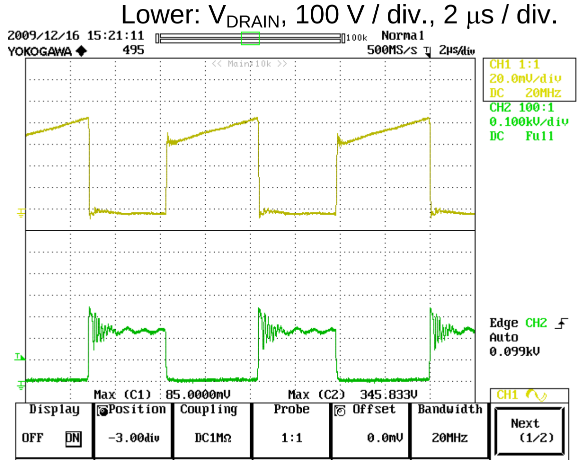

Figure 20 – 100 VDC, Over Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V / div., 2 μs / div.

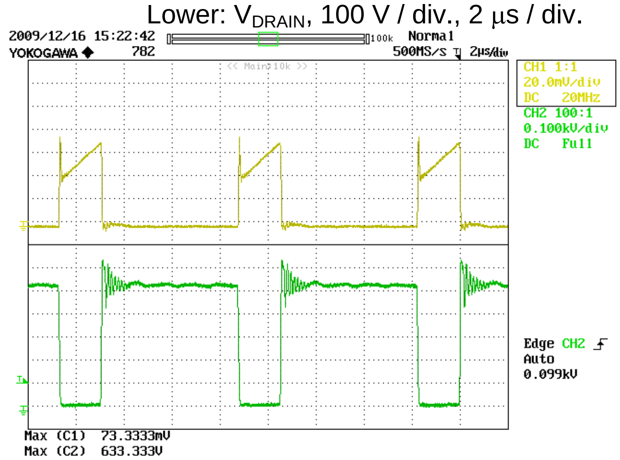

Figure 21 – 400 VDC, Over Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V / div., 2 μs / div.

12.2 Output Rectifier Peak Inverse Voltage (PIV)

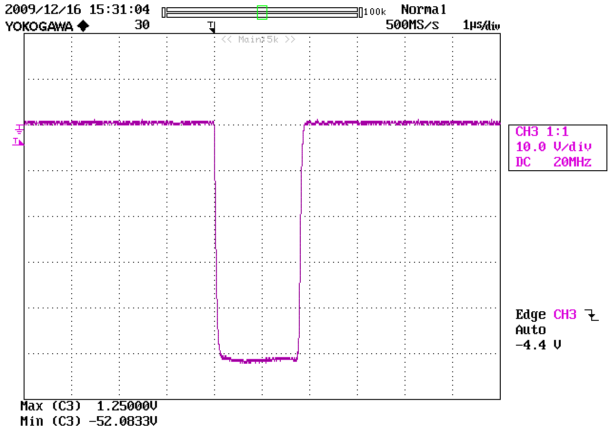

Figure 22 – 380 VAC 100% Load.
10 V / div. & 12 µs / div.

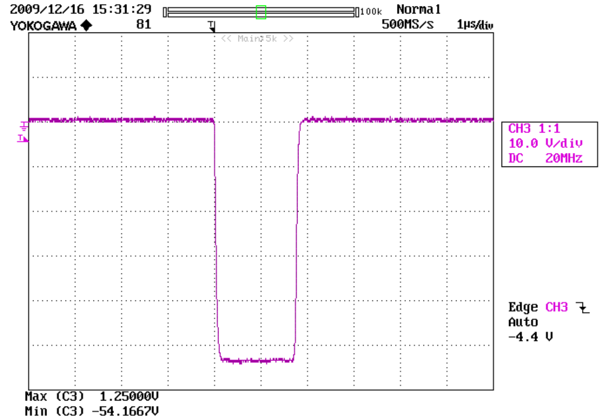

Figure 23 – 400 VDC; 100% Load.
10 V / div. & 12 µs / div.

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12.3 OVP Profile (Latched)

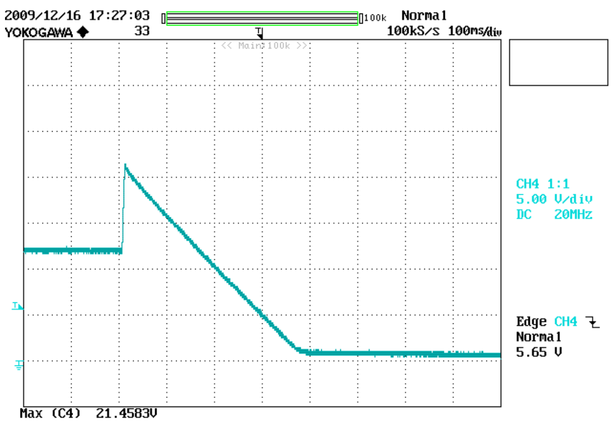

Figure 24 – OVP Profile, 110 VDC, 100 mA Load.
5 V / div. & 100 ms / div.

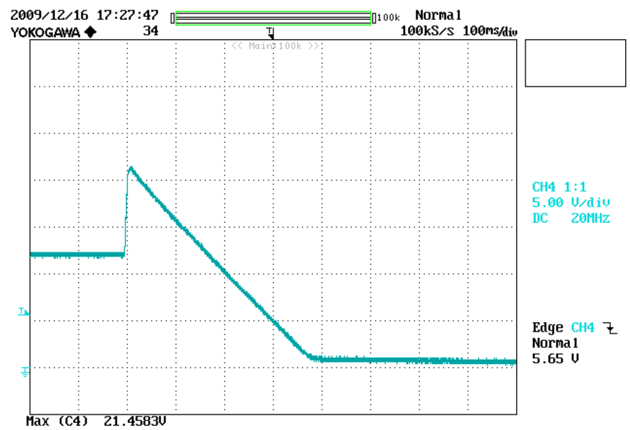

Figure 25 – OVP-up Profile, 380 VDC, 100 mA Load.
5 V / div. & 100 ms / div.

12.4 OCP Profile (Auto-recovery)

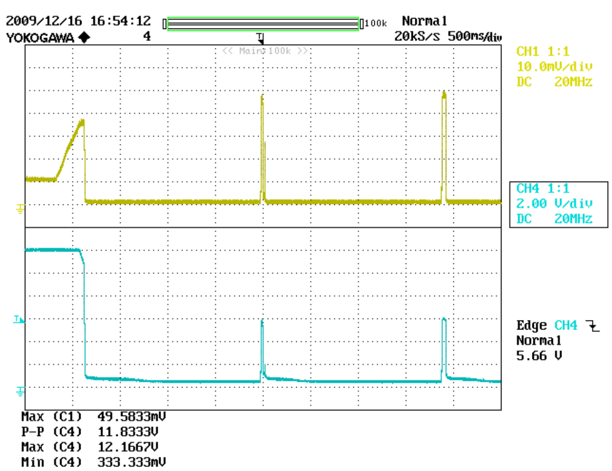

Figure 26 – OCP Profile, 110 VDC.
Ch1: I_{OUTPUT},1 A / div.
Ch4: V_{OUTPUT}, 2 V / div. & 500 ms / div.

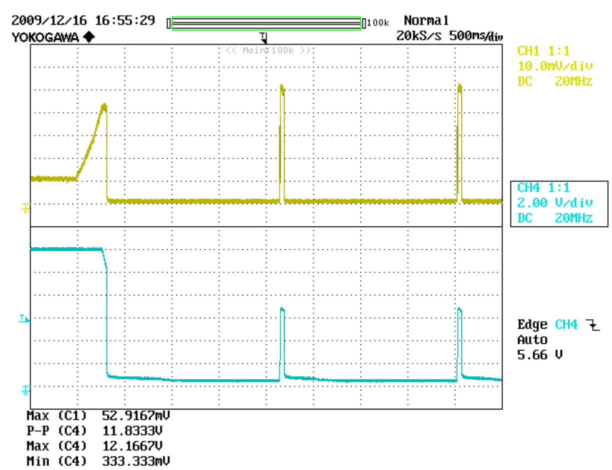

Figure 27 – OCP Profile, 400 VDC.
Ch1: I_{OUTPUT},1 A / div.
Ch4: V_{OUTPUT}, 2 V / div. & 500 ms / div.

12.5 Load Transient Response (50% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

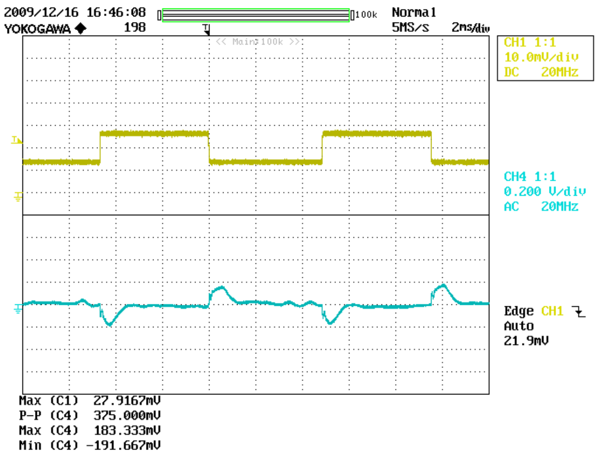

Figure 28 – Transient Response, 110 VDC, 50-100-50% Load Step.
Upper: Load Current, 1 A / div.
Lower: Output Voltage
0.2 V / div., 2 ms / div.

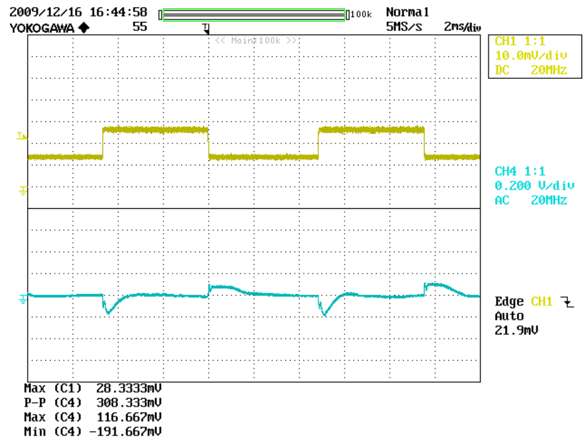

Figure 29 – Transient Response, 380 VDC, 50-100-50% Load Step.
Upper: Load Current, 1 A / div.
Lower: Output Voltage
0.2 V / div., 2 ms / div.

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12.6 Output Ripple Measurements

12.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (next page).

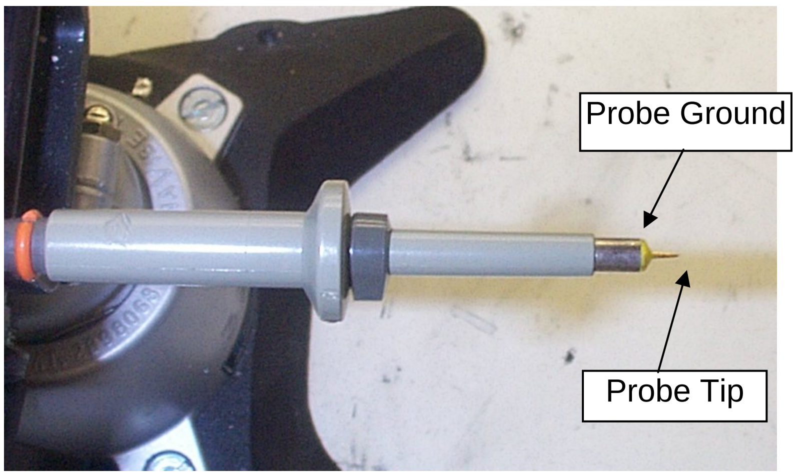

Figure 30 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 31 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.6.2 Measurement Results

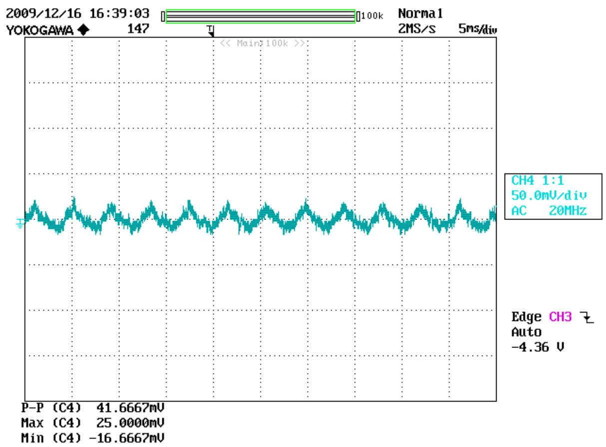

Figure 32 – Ripple 110 VDC, Full Load.
5 ms / div., 50 mV / div.

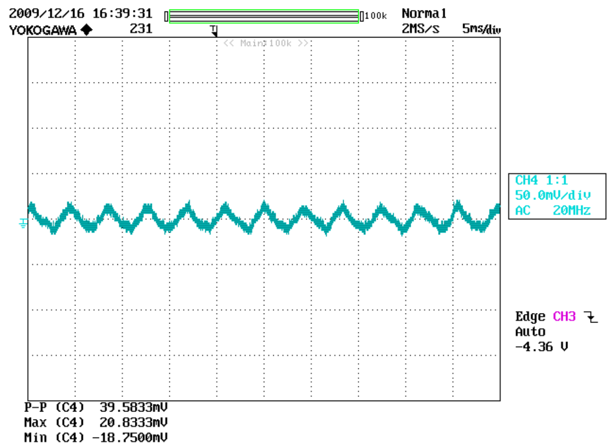

Figure 33 – Ripple 380 VDC, Full Load.
5 ms / div., 50 mV / div.

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13 Control Loop Measurements

EQUIPMENT: Frequency Response Analyzer
Model 4194A
HP

13.1 110 VDC Maximum Load

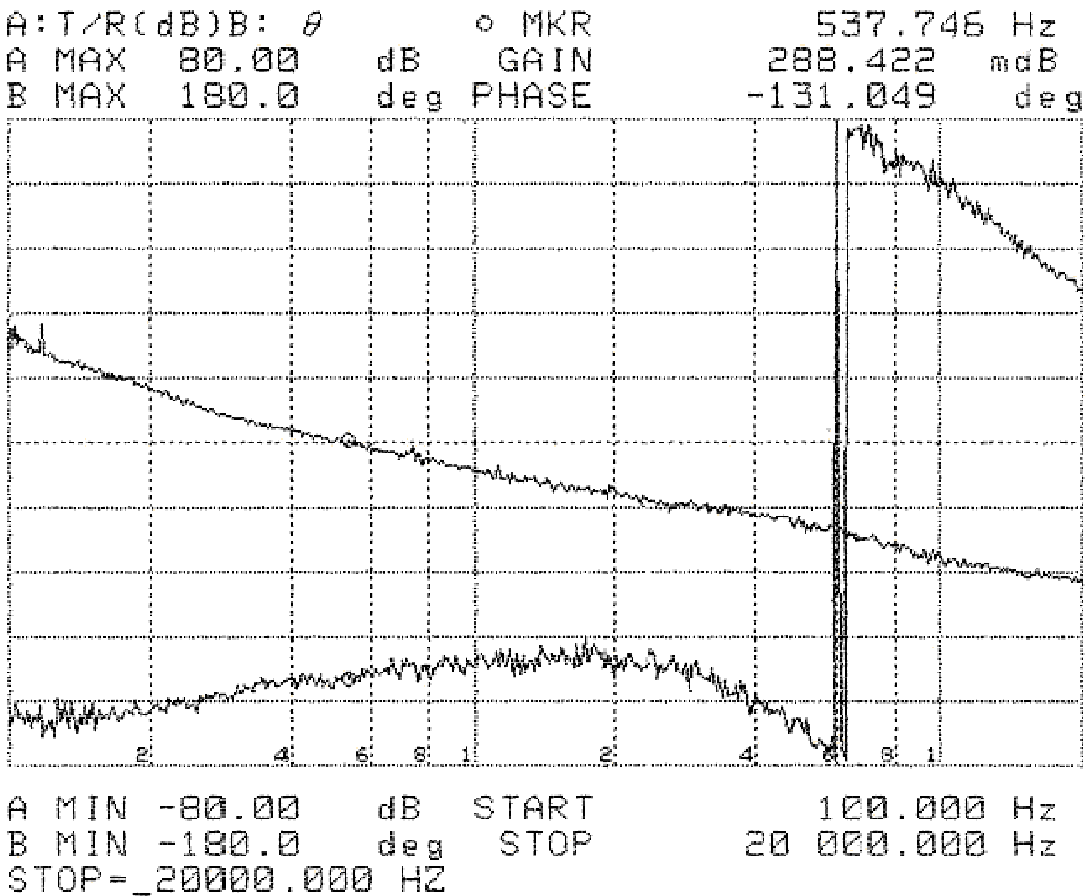

Figure 34 – Gain-Phase Plot, 110 VDC, Maximum Steady State Load.
Vertical Scale: Gain = 16 dB / div., Phase = 36° / div.
Crossover Frequency = 537 Hz Phase Margin = 49°.

13.2 380 VDC Maximum Load

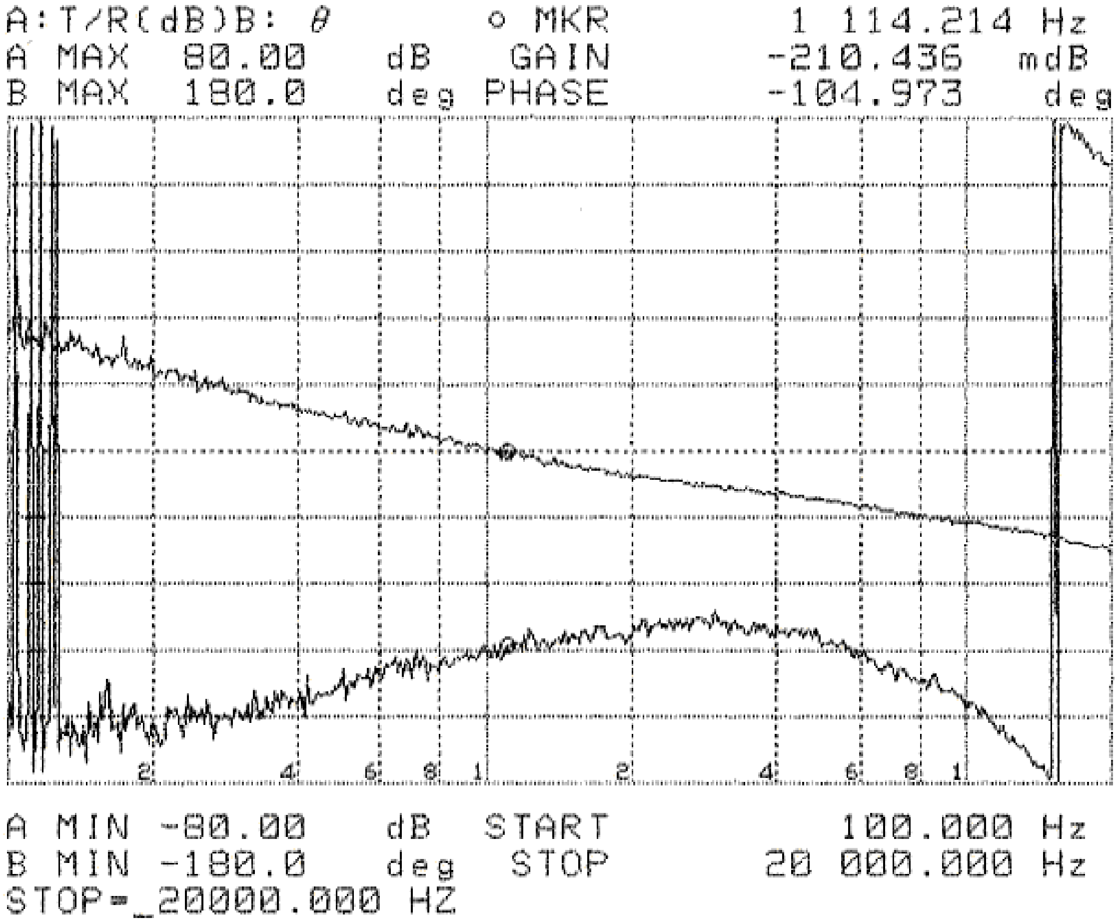

Figure 35 – Gain-Phase Plot, 380 VDC, Maximum Steady State Load
Vertical Scale: Gain = 16 dB / div., Phase = 36° / div.
Crossover Frequency = 1.1 kHz Phase Margin = 75°.

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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
05-Feb-10	ME	1.4	Initial Release	Apps & Mktg

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