Design Example Report

Title	***3.25 W CV/CC Charger Using LinkSwitch™-II That Meets New 2011 European Standards***
Specification	85 – 265 VAC Input; 5 V, 650 mA Output
Application	Low Cost European Charger or Adapter
Author	Applications Engineering Department
Document Number	DER-279
Date	July 8, 2011
Revision	1.0

Summary and Features

- Revolutionary control concept provides very low cost, low part-count solution
  - Primary-side control eliminates secondary-side control and optocoupler
  - 700 V MOSFET rating allows Clampless™ design - eliminates primary clamp components
  - Provides ±5% constant voltage (CV) and ±18% constant current (CC) accuracy including output cable voltage drop compensation.
  - Over-temperature protection – tight tolerance (±5%) with hysteretic recovery for safe PCB temperatures under all conditions
  - Auto-restart output short circuit and open-loop protection
- EcoSmart™ – Easily meets all current international energy efficiency standards – China (CECP) / CEC / ENERGY STAR 2 / EU CoC
  - No-load input energy consumption: <30 mW at 230 VAC
  - Ultra-low leakage current: <5 μA at 265 VAC input (no Y capacitor required)
- Design easily meets EN550022 and CISPR-22 Class B EMI with >8 dB margin
- Meets IEC 61000-4-5 Class 3 AC line surge
- Meets IEC 62684 common mode voltage of DC output
- Meet new European Standard EN 301 489-34 specification
- Meets <5 μA battery discharge requirement
- Output always higher than 4 V with load transient from no-load to 0.5 A.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 2.5 W (minimum), 3.25 W (typical) constant voltage/ constant current (CV/CC) universal input charger power supply for a cell phone. The power supply utilizes the LinkSwitch-II.

The LinkSwitch-II family was developed to cost effectively replace all existing solutions in low-power charger and adapter applications. Its controller is optimized for CV/CC charging applications, for minimal external part count, and for very tight control of the output voltage and moderate current regulation without the use of an optocoupler. The integrated 700 V switching MOSFET and ON/OFF control function achieve both high efficiency under all load conditions, and low no-load energy consumption. No-load performance and operating efficiency exceed all current and proposed international energy efficiency standards.

This circuit takes advantage of Power Integration's Clampless transformer construction techniques. This makes use of the primary winding capacitance to clamp the voltage across the LinkSwitch-II

A unique ON/OFF control scheme provides voltage regulation, as well as support for cable voltage-drop compensation, and tight regulation over a wide temperature range. The output current is regulated by modulating the switching frequency to provide moderately tight CC characteristic.

The LinkSwitch-II controller consists of an oscillator, feedback (sense and logic) circuitry, a 5.8 V regulator, BYPASS (BP) pin programming functions, over-temperature protection, frequency jittering, current-limit circuitry, leading-edge blanking, a frequency controller for CC regulation, and an ON/OFF state machine for CV control.

The LinkSwitch-II also provides a sophisticated range of protection features including auto-restart for control loop component open/short circuit faults and output short-circuit conditions. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

The IC package provides extended creepage distance between high and low voltage pins (both at the package and the PCB), which is required in very humid conditions to prevent arcing and to further improve reliability.

The LinkSwitch-II can be configured as either self-biased from the high voltage drain pin or supplied via an optional bias supply. When configured as self-biased, the very low IC current consumption provides a worst-case no-load power consumption of approximately 200 mW at 265 VAC, well within the 300 mW European Union CoC requirement. When fed from an optional bias supply (as in this design), the no-load power consumption reduces to <30 mW.

The EE16 transformer bobbin in this design provides extended creepage to meet safety spacing requirements.
This document contains the power supply specifications, schematic, bill of materials, transformer specifications, and typical performance characteristics for this reference design using the LinkSwitch-II.

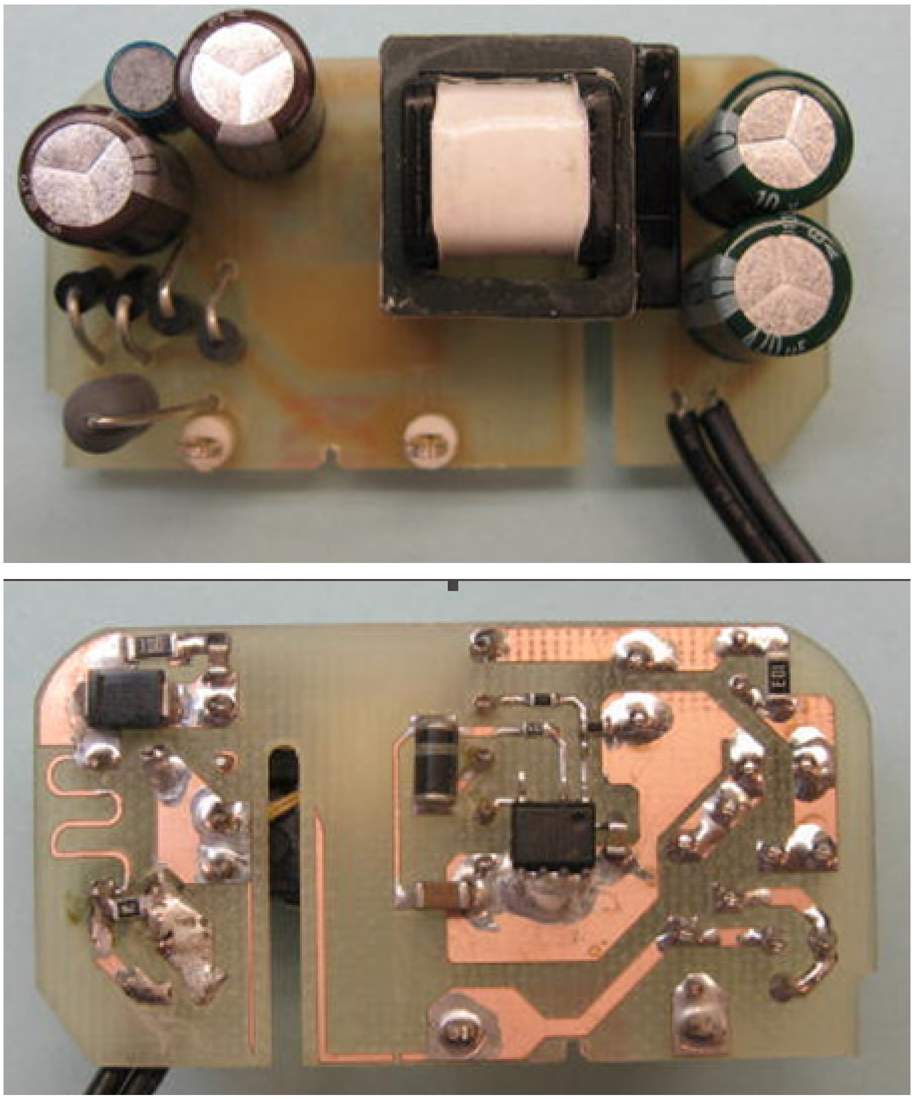

Figure 1 – Populated Circuit Board Photograph.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.03	W	
Output						
Output Voltage	V_{OUT}	4.75	5.0	5.25	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			80	mV	20 MHz bandwidth
Output Current	I_{OUT}	0.5	0.65	0.8	A	
Output Power	P_{OUT}		3.25		W	
Output Cable Resistance	R_{CBL}		0.4		Ω	#26 AWG, 1.2 M long
Name plate output rating						
Nameplate Voltage	V_{NP}		5		V	
Nameplate Current	I_{NP}		0.5		A	
Nameplate Power	P_{NP}		2.5		W	
Efficiency						
Full Load	η	70			%	Measured at P_{OUT} 25 °C
Required average efficiency per EU Code of Conduct V4	$\eta_{EU(CoC)}$	68	Measured Measured per Energy Star "Test Method for Calculating the Energy Efficiency of Single-Voltage External AC-DC and AC-AC Power Supplies (August 11, 2004)".			
Required average efficiency per ENERGY STAR V2	$\eta_{ES2.0}$	68				
Environmental						
Conducted EMI	Meets CISPR22B / EN55022B					> 6 dB margin
Safety	Designed to meet IEC950 / UL1950 Class II					
Surge		1 2			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
ESD		-15		15	kV	Contact and air discharge onto output connector
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level. Assembly is installed in a standard plastic enclosure.

3 Schematic

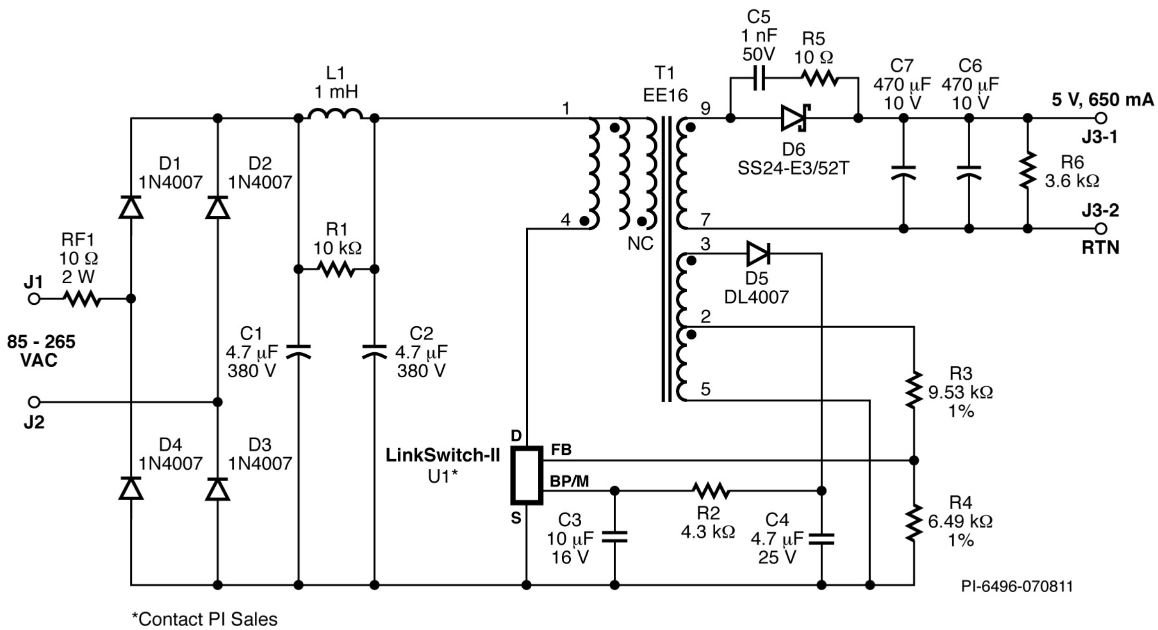

Figure 2 – Schematic.

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4 Circuit Description

This circuit uses the LinkSwitch-II in a primary-side regulated flyback power supply configuration.

4.1 Input Filter

The AC input power is rectified by diodes D1 through D4. Bulk storage capacitors C1 and C2 filter the rectified AC. Inductor L1 forms a pi (π) filter with C1 and C2 to attenuate conducted differential-mode EMI noise. This configuration, and the use of Power Integrations' transformer E-Shield® technology, allows this supply to comply with EMI standard EN55022 class B, with good margin, and without a Y capacitor. Fusible resistor RF1 provides protection against catastrophic failure. It should be rated to withstand the instantaneous dissipation when the supply is first connected to AC input (while the input capacitors charge) at VAC_{MAX}. This means choosing either an over-sized metal-film or a wire-wound resistor. This design uses a wire-wound resistor for RF1.

4.2 LinkSwitch-II Primary

The LinkSwitch-II device (U1) incorporates the power switching device, an oscillator, a CC/CV control engine, startup circuitry, and protection functions into one IC. The integrated 700 V MOSFET allows sufficient voltage margin for universal input AC applications. The device is completely self-powered from the BYPASS pin (BP) and decoupling capacitor C3. Capacitor C3 also selects the output voltage cable-drop compensation amount. For this design enhanced cable voltage drop compensation was selected by choosing a 10 μF value. The optional bias circuit consisting of D5, C4, and R2 increases efficiency and reduces the no-load input power to less than 30 mW at 230 VAC.

The rectified and filtered input voltage is applied to one side of transformer T1's primary winding. The integrated MOSFET in U1 drives the other side of T1's primary winding. This design does not require a primary side clamp circuit.

4.3 Output Rectification and Filtering

Transformer T1's secondary is rectified by D6 and filtered by C6 and C7. A Schottky barrier-type diode was selected for higher efficiency. Capacitor C6 and C7 was selected to have a sufficiently low ESR to meet the load transient requirement and output voltage ripple requirement without using an external LC post-filter. For lower cost design with lower requirement for load transient and ripple, only one capacitor is necessary or smaller value capacitor can be used for C6 and C7.

In designs where lower (3% to 4%) average efficiency is acceptable, diode D6 may be replaced by a PN-junction diode to lower cost. Note that R3 and R4 must be re-adjusted to ensure the output voltage stays centered.

Capacitor C5 and R5 form a snubber network to both limit the magnitude of the transient voltage spikes that appear across D6 and reduce radiated EMI.

Resistor R6 form the output pre-load, necessary to prevent the output voltage rising at no-load.

4.4 Output Regulation

The LinkSwitch-II eliminates the optocoupler by using a primary side AC winding sense on T1. The IC regulates by using ON/OFF control for CV regulation and frequency control for CC regulation. The feedback resistors (R3 and R4) were selected using standard 1% resistor values to center both the nominal output voltage and constant current regulation thresholds.

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5 PCB Layout

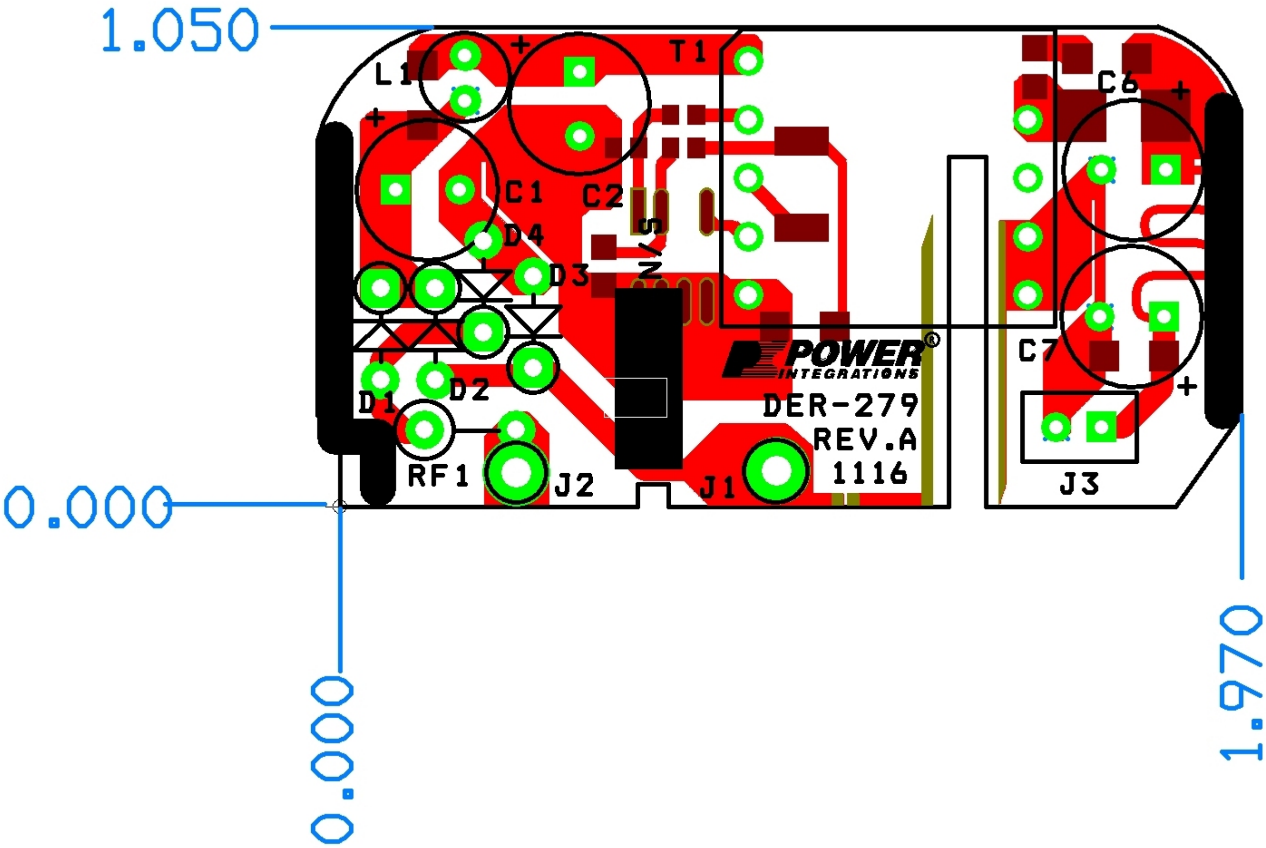

Figure 3 – Printed Circuit Layout (1.050" x 1.970").

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg	Mfg Part Number
1	2	C1 C2	4.7 μF, 380 V, Electrolytic, (8 x 11.5)	XX380VB4R7M8X11LL	Nippon Chemi-Con
2	1	C3	10 μF, 16 V, Ceramic, X5R, 0805	GRM21BR61C106KE15L	Murata
3	1	C4	4.7 μF, 25 V, Ceramic, X7R, 1206	ECJ-3YB1E475M	Panasonic
4	1	C5	1 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H102K	Panasonic
5	2	C6,C7	470 μF, 10 V, Electrolytic, Very Low ESR, 72 m Ω, (8 x 11.5)	EKZE100ELL471MHB5D	Nippon Chemi-Con
6	4	D1 D2 D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
7	1	D5	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
8	1	D6	40 V, 2 A, Schottky, SMD, DO-214AA	SS24-E3/52T	Vishay
9	2	J1 J2	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
10	1	J3	1.2 M, #26 AWG, 2.1 mm connector (custom)	3PH323A0	Anam Instruments
11	1	L1	1000 μH, 0.21 A, 5.5 x 10.5 mm	SBC1-102-211	Tokin
12	1	R1	10 kΩ 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
13	1	R2	4.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ432V	Panasonic
14	1	R3	9.53 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9531V	Panasonic
15	1	R4	6.49 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF6491V	Panasonic
16	1	R5	10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
17	1	R6	3.6 k Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ362V	Panasonic
18	1	RF1	10 Ω, 2 W, Fusible/Flame Proof Wire Wound	CRF253-4 10R	Vitrohm
19	1	T1	Bobbin, EE16 Extended Creepage, Horizontal, 10 pins	TF-1613	Shulin Enterprise
20	1	U1	LinkSwitch-II, SO-8-C	LinkSwitch-II	Power Integrations

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7 Transformer Specification

7.1 *Electrical Diagram*

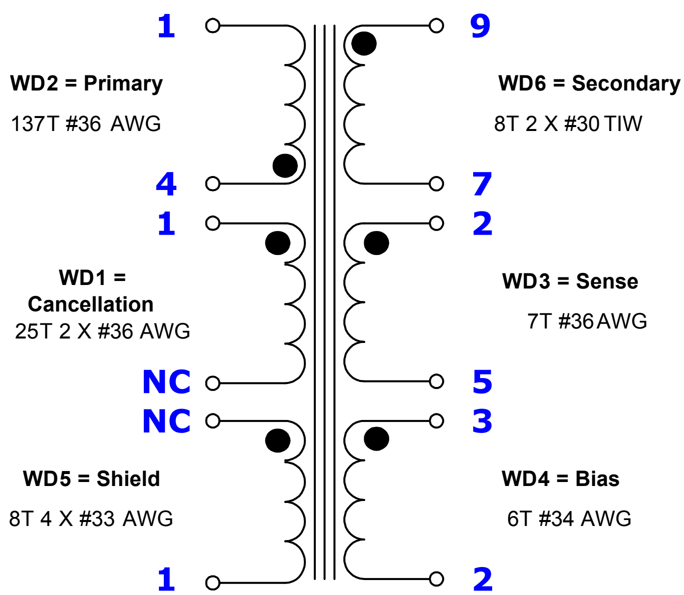

Figure 4 – Transformer Electrical Diagram.

Note: Windings WD3 and WD4 are wound to spread across the entire winding window. These windings interleave each other and there is no tape between these windings.

7.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pin 10.	3000 VAC
Primary Inductance	Pins 1 and 4 all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	4036 μH, ±10%
Resonant Frequency	Pins 1 and 4, all other windings open.	600 kHz min.
Primary Leakage Inductance	Pins 1 and 4 with pins 7 and 10 shorted, measured at 100 kHz, 0.4 V_{RMS}.	110 μH max.

7.3 *Materials*

Item	Description
[1]	Core: EE16, NC-2H or equivalent, gapped for ALG = 215 nH/T^2
[2]	Bobbin: EE16, Horizontal, 10 pins (5/5)
[3]	Magnet Wire: #36 AWG
[4]	Magnet Wire: #34 AWG
[5]	Magnet Wire: #33 AWG
[6]	Triple Insulated Wire: #30 AWG
[7]	Tape: 3M 1298 Polyester film, 2.0 mils thick, 8.0 mm wide
[8]	Varnish

7.4 Transformer Build Diagram

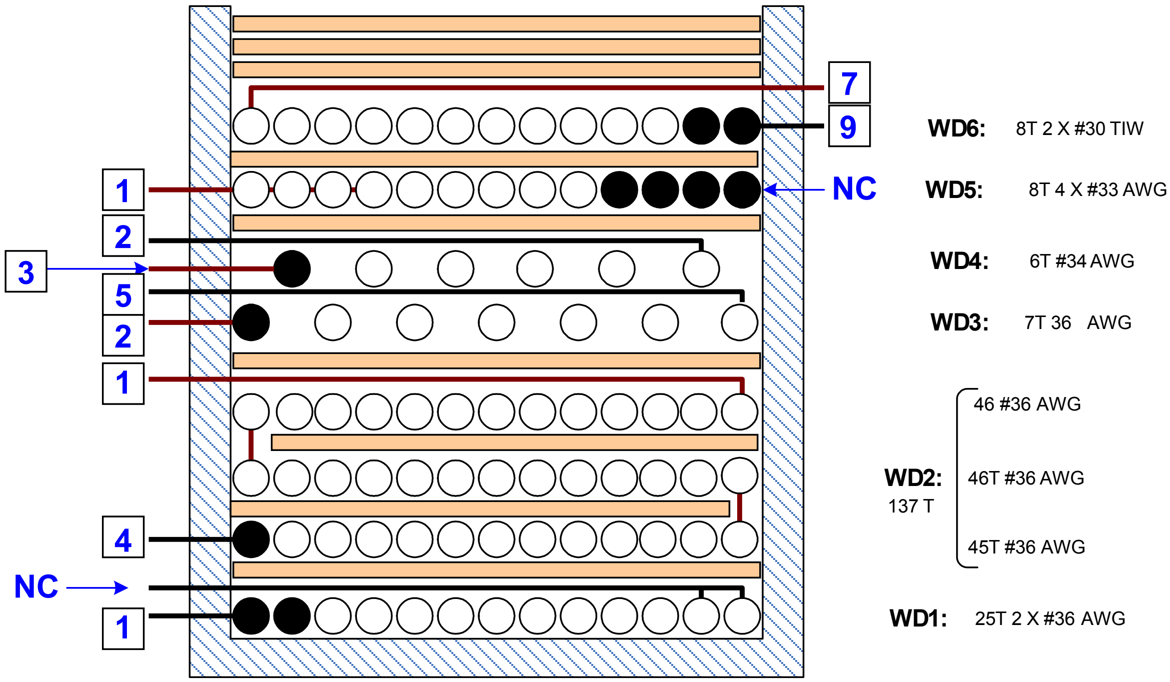

Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

Core Cancelation	Start at pin 1. Wind 25 bifilar turns of item [3] in 1 full layer. Cut finish. Apply one layer of tape [7].
Primary	Start at Pin 4. Wind 45 turns of item [3] in approximately 1 layer. Apply one layer of tape [7]. Wind 46 turns on next layer. Apply 1 layer of tape [7]. Wind 46 turns and finish on pin 1.
Basic Insulation	Use one layer of item [7] for basic insulation.
Sense Winding	Starting at pin 2, wind 7 turns of item [3]. Spread turns evenly across bobbin. Finish at pin 5.
Bias winding	Start at pin 3, wind 6 turns of item [4]. Spread turns evenly across bobbin interleaving with sense winding. Terminate on pin 2.
Basic Insulation	Use one layer of item [7] for basic insulation.
Shield Winding	Temporally start at pin 6. Wind 8 quadfilar turns of item [5] across entire width of bobbin. Terminate on pin 1. Remove start from pin 6 and cut wire such that it fills bobbin width (no gaps).
Basic Insulation	Use one layer of item [7] for basic insulation.
Secondary Winding	Start at pin 10. Wind 8 bifilar turns of item [6] to fill bobbin layer. Finish on pin 7.
Outer Wrap	Wrap windings with 3 layers of tape item [7].
Final Assembly	Assemble and secure gapped core halves. Cut pin 10 and varnish impregnate with item [8].

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8 Transformer Design Spreadsheet

ACDC_LNK63X_022509; Rev.1.0; Copyright Power Integrations 2009	INPUT	INFO	OUTPUT	UNIT	ACDC_LNK63X_022509_Rev1-0.xls; Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.10			Volts	Output Voltage
PO	2.95			Watts	Output Power
n	0.75				Efficiency Estimate
Z			0.5		Loss Allocation Factor
tC			3	ms	Bridge Rectifier Conduction Time Estimate
Clampless Design	YES				Choose 'YES' from the 'clampless Design' drop down box at the top of this spreadsheet for a clampless design. Choose 'NO' to add an external clamp circuit. Clampless design lowers the total cost of the power supply
CIN	9.40			uFarads	Input Filter Capacitor
ENTER LinkSwitch-II (LNK63X) VARIABLES					
LinkSwitch-II Device	**LNK632DG**		**LNK632DG**		LinkSwitch-II (LNK63X) device
ILIMITMIN			0.135	Amps	LinkSwitch-II (LNK63X) Minimum Current Limit
ILIMITMAX			0.155	Amps	LinkSwitch-II (LNK63X) Maximum Current Limit
fS			100000	Hertz	LinkSwitch-II (LNK63X) Switching Frequency
I2FMIN			1987	A^2Hz	LinkSwitch-II (LNK63X) Min I2F (Power Coefficient)
I2FMAX			2582	A^2Hz	LinkSwitch-II (LNK63X) Max I2F (Power Coefficient)
VOR	96.00		96	Volts	Reflected Output Voltage
VDS			10	Volts	LinkSwitch-II (LNK63X) on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
DCON			5.16	us	Output Diode conduction time
KP_TRANSIENT			0.79		Worst case ripple to peak current ratio. Maintain KP_TRANSIENT above 0.25
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EE16**		**EE16**		Transformer Core size
Core		*EE16*		*P/N:*	PC40EE16-Z
Bobbin		*EE16_BOBBIN*		*P/N:*	BE-16-118CPH
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
BW			8.5	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00		3		Number of Primary Layers
NS			8		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			93	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
FEEDBACK VARIABLES					
NFB			7.00		Feedback winding number of turns
VFLY			4.90	Volts	Voltage on the Feedback winding when LinkSwitch-II (LNK63X) turns off
RUPPER			9.53	k-ohms	Upper resistor of feedback network
RLOWER			6.81	k-ohms	Lower resistor of feedback network
Fine Tuning Section					
Measured Output Voltage	5.40		5.40	k-ohms	Actual (Measured) Voltage at the output of power supply

RLOWER_FINE			6.49	k-ohms	Adjusted (Fine tuned) value of lower resistor (RLOWER). Do not change value of RUPPER
Bias Winding Parameters					
Add Bias winding			YES		External Bias winding needed. AC stack bias winding on top of Feedback winding
VB	11		11	Volts	Bias Winding Voltage
NB			8		Number of Bias winding turns. Bias winding is assumed to be AC stacked on top of the Feedback winding
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.54		Maximum Duty Cycle
IAVG			0.04	Amps	Average Primary Current
IP			0.14	Amps	Minimum Peak Primary Current
IR			0.11	Amps	Primary Ripple Current
IRMS			0.06	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			3669	uHenries	Minimum Primary Inductance
LP_TYP			4036	uHenries	Typical (Nominal) Primary Inductance
LP_TOL			10		Tolerance of Primary inductance
NP			137		Primary Winding Number of Turns
ALG			215	nH/T^2	Gapped Core Effective Inductance
BM			2223	Gauss	Maximum Flux Density, (BM<2500) Calculated at typical current limit and typical primary inductance
BP			2592	Gauss	Peak Flux Density, (BP<3100) Calculated at maximum current limit and maximum primary inductance
BAC			803	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1654		Relative Permeability of Ungapped Core
LG			0.10	mm	Gap Length (Lg > 0.1 mm)
BWE			25.5	mm	Effective Bobbin Width
OD			0.19	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.15	mm	Bare conductor diameter
AWG			35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			32	Cmils	Bare conductor effective area in circular mils
CMA		*Info*	512	Cmils/Amp	CAN DECREASE CMA < 500 (decrease L(primary layers),increase NS,smaller Core)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			2.31	Amps	Peak Secondary Current
ISRMS			1.00	Amps	Secondary RMS Current
IO			0.58	Amps	Power Supply Output Current
IRIPPLE			0.81	Amps	Output Capacitor RMS Ripple Current
CMS			199	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			27	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.36	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.06	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.35	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			-	Volts	Peak Drain Voltage is highly dependent on Transformer capacitance and leakage inductance. Please verify this on the bench and ensure that it is below 650 V to allow 50 V margin for transformer variation.
PIVB			46	Volts	Bias Diode Maximum Peak Inverse Voltage
PIVS			27	Volts	Output Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					

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1st output					
VO1			5.1	Volts	Output Voltage (if unused, defaults to single output design)
IO1			0.578	Amps	Output DC Current
PO1			2.95	Watts	Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			8.00		Output Winding Number of Turns
ISRMS1			1.00	Amps	Output Winding RMS Current
IRIPPLE1			0.81	Amps	Output Capacitor RMS Ripple Current
PIVS1			27	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			199	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			27	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.36	mm	Minimum Bare Conductor Diameter
ODS1			1.06	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			1.00		Output Winding Number of Turns
ISRMS2			0.00	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			1.00		Output Winding Number of Turns
ISRMS3			0.00	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			2.95	Watts	Total Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Active Mode Efficiency

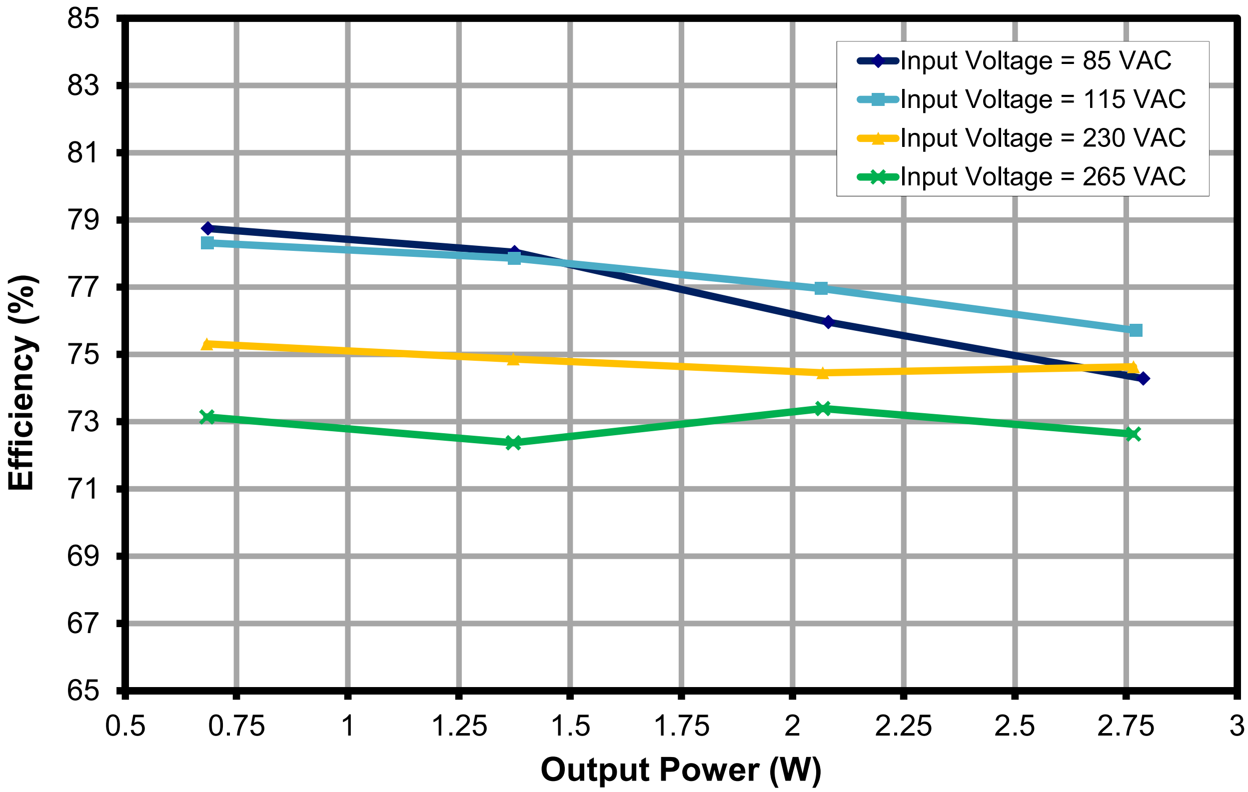

Figure 6 – Efficiency vs. Input Voltage, Room Temperature, 60 Hz.

Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	68.5	75.3
50	77.9	74.5
75	77.0	74.5
100	75.7	74.6
Average	77.2	74.8
EC Code of Conduct (V4) requirement	68	
ENERGY STAR 2.0 requirement	68	

Note: Measurements were taken at the end of a 1.2M long #26 AWG 0.4 Ω cable.

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9.2 Energy Efficiency Requirements

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

9.2.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

9.2.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and I_O ≥ 550 mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

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9.2.3 EC Code of Conduct Version 3

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.44 \times P_O + 0.145$
> 1 W to ≤ 36 W	$0.08 \times \ln(P_O) + 0.585$
> 36 W	0.87

ln = natural logarithm

Mobile handheld battery applications

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.5 \times P_O + 0.029$
> 1 W to ≤ 8 W	$0.095 \times \ln(P_O) + 0.529$

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
≥ 0.3 W to < 50 W	≤ 0.25 W
≥ 50 W to < 250 W	≤ 0.5 W

No-load Energy Consumption (mobile handheld battery applications)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
≥ 0.3 W to ≤ 8 W	≤ 0.25 W (current)
≥ 0.3 W to ≤ 8 W	≤ 0.15 W (from 1/1/2011)

9.3 No-load Input Power

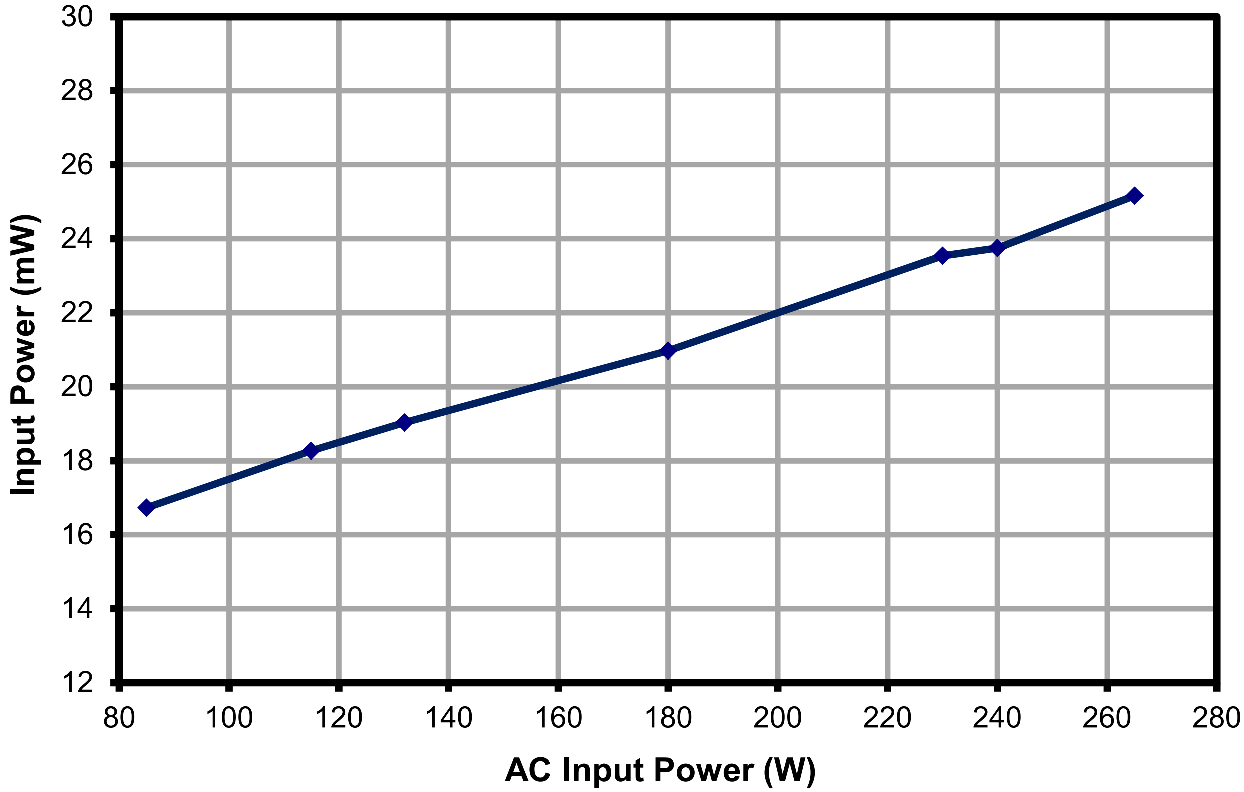

Figure 7 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

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9.4 Regulation

9.4.1 Line and Load

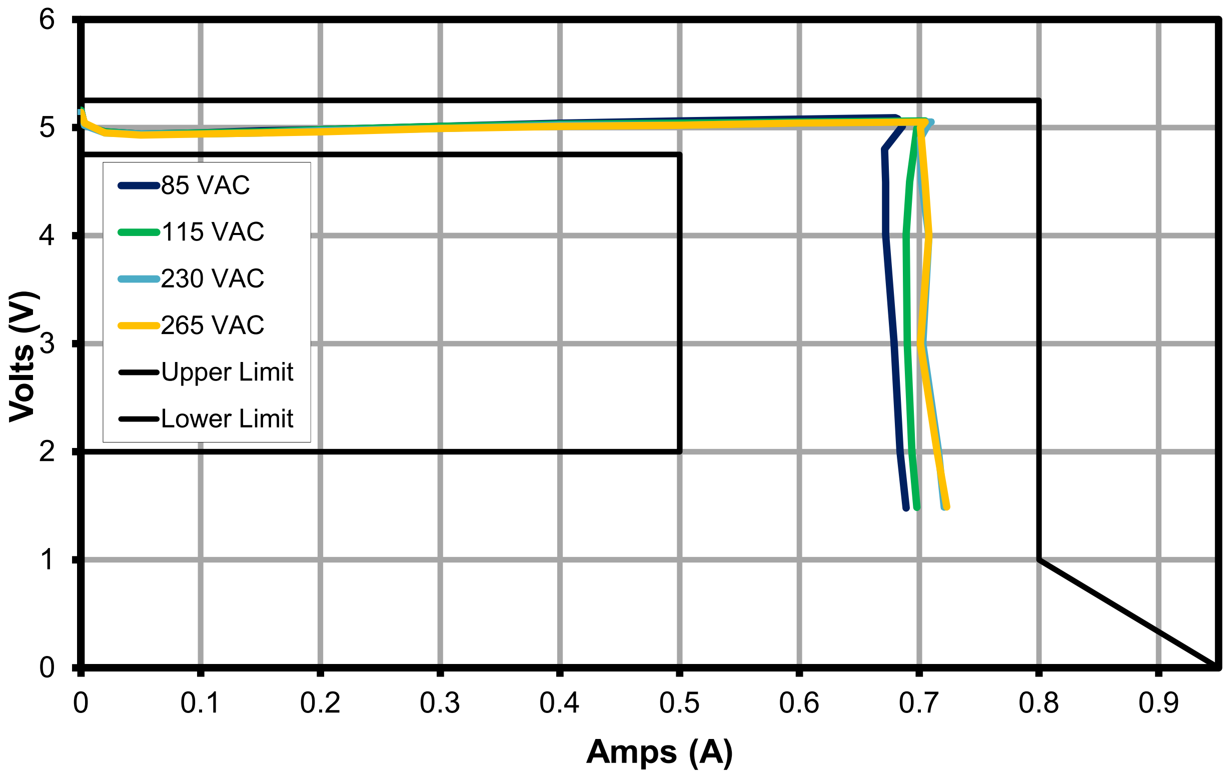

Figure 8 – Line and Load Regulation with 10 µF Bypass Capacitor and #26 AWG Output Cable, Room Temperature.

10 Thermal Performance

The temperature of the LinkSwitch-II was measured by soldering a thermocouple to the source pin of the device. A thermocouple was soldered to Drain of output diode to measure the temperature of D6. For the 40 °C ambient test, the power supply was placed into a small box which was enclosed into a bigger box.

Item	Temperature (°C)			
	85 VAC	115 VAC	230 VAC	265 VAC
Ambient	40	40	40	40
LinkSwitch-II (U1)	76	72	73	77
Output Diode (D6)	70	69	70	71

Figure 9 – Thermal Image of Assembly (Bottom) $V_{IN:}$ 85 VAC, Full Load, LinkSwitch-II is Highest Recorded Temperature at 49.3 °C.

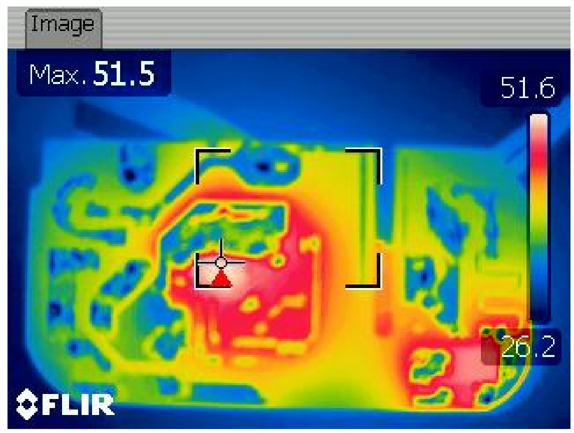

Figure 10 – Thermal Image of Assembly (Bottom) $V_{IN:}$ 265 VAC, Full Load, LinkSwitch-II is Highest Recorded Temperature at 51.5 °C.

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

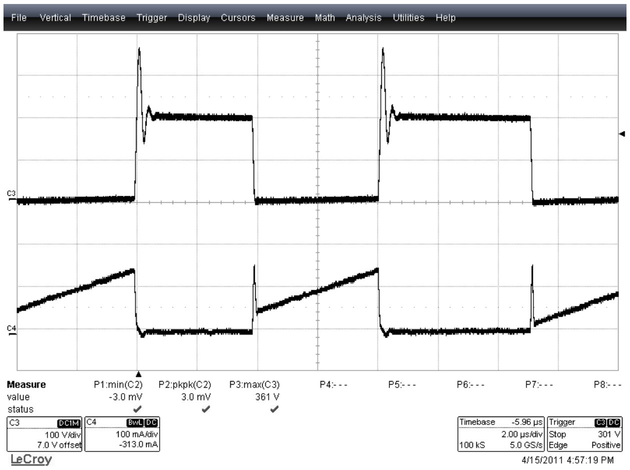

Figure 11 – 85 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA / div, 2 μs / div.

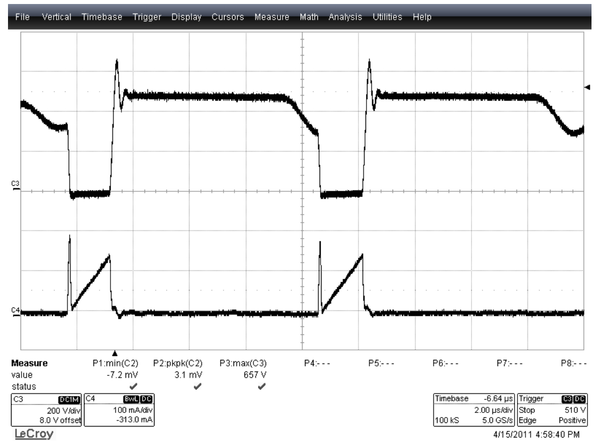

Figure 12 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 100 mA / div, 2 μs / div.

11.2 Output Voltage Start-up Profile

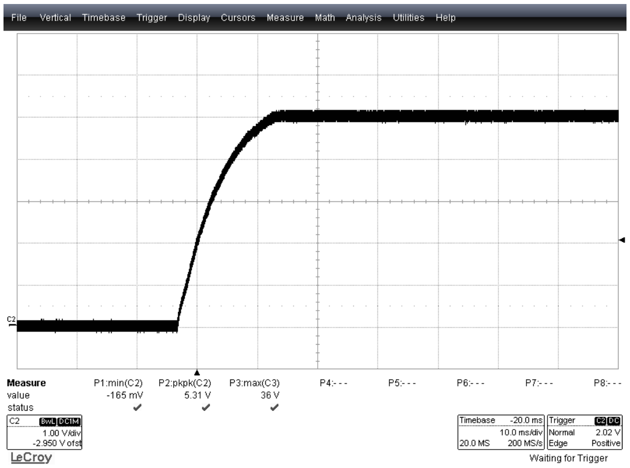

Figure 13 – 115 VAC, Full load. 1 V, 10 ms / div.

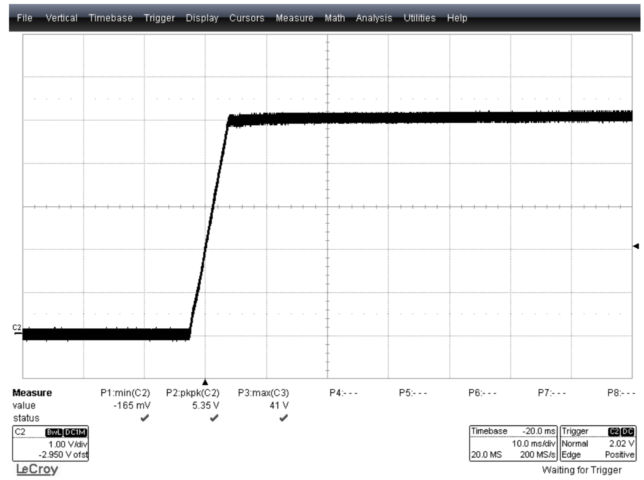

Figure 14 – 115 VAC, No-Load. 1 V, 10 ms / div.

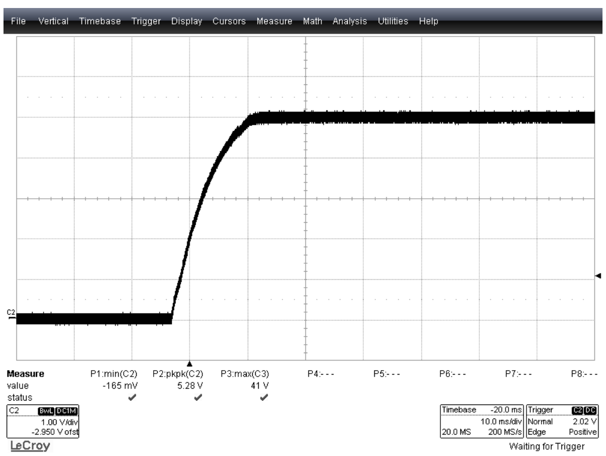

Figure 15 – 230 VAC, Full load. 1 V, 10 ms / div.

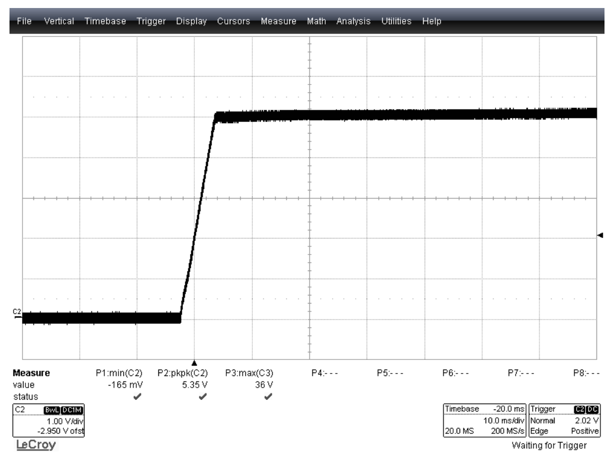

Figure 16 – 230 VAC, No-Load.1 V, 10 ms / div.

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11.3 Drain Voltage and Current Start-up Profile

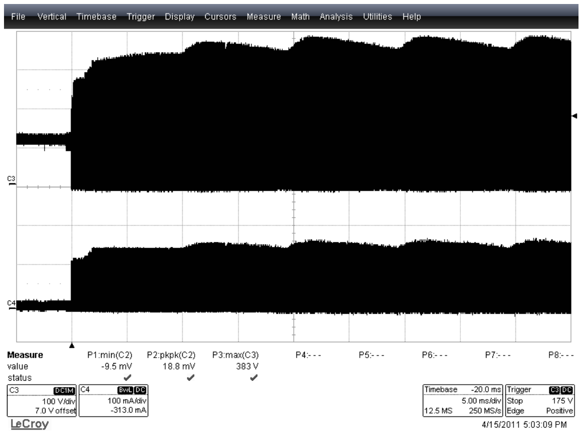

Figure 17 – 85 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA / div, 5 ms / div.

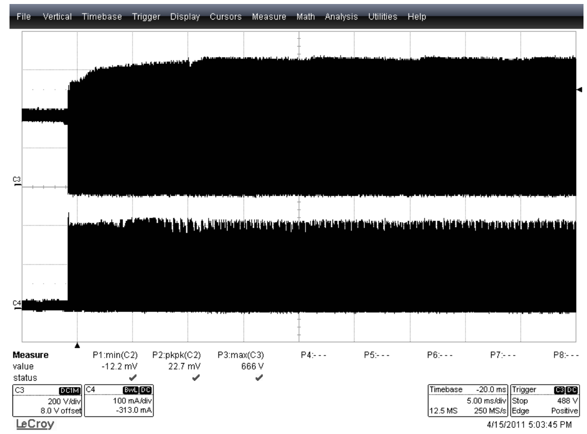

Figure 18 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 100 mA / div, 5 ms / div.

11.4 Load Transient Response

In the figures shown below, the oscilloscope was triggered using the load current step as a trigger source. Load transient from 50% load to full load and load transient from no load to full load are shown in the following pictures. As can be seen from the following picture, the V_{OUT} is always higher than 4 V even with load transient from no-load to full load 0.5 A.

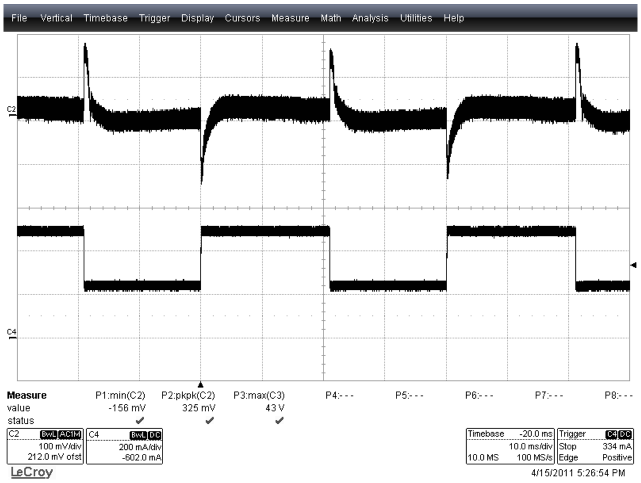

Figure 19 – 115 VAC, 50-100-50% Load Step.
Upper: V_{RIPPLE}, 100 mV, 10 ms / div.
Lower: I_{LOAD}, 0.2 A / div.

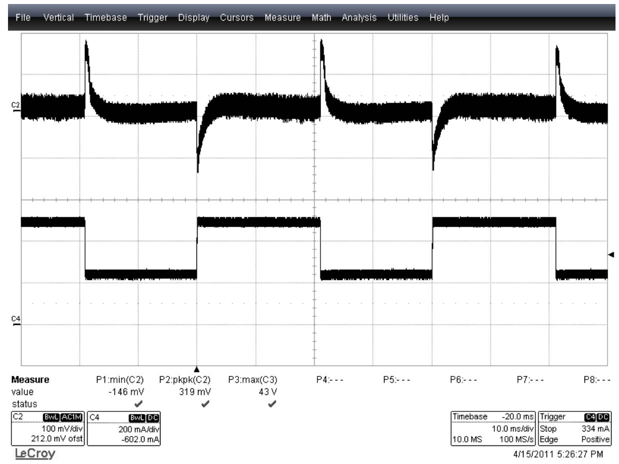

Figure 20 – 230 VAC, 50-100-50% Load Step.
Upper: V_{RIPPLE}, 100 mV, 10 ms / div.
Lower: I_{LOAD}, 0.2 A / div.

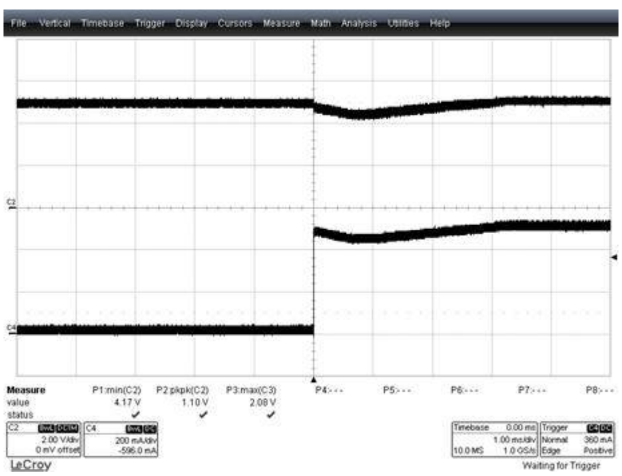

Figure 21 – 115 VAC, No-load to Full Load.
Minimum V_{OUT} 4.13 V
Upper: V_{OUT}, 2 V, 1 ms / div.
Lower: I_{LOAD}, 0.2 A / div.

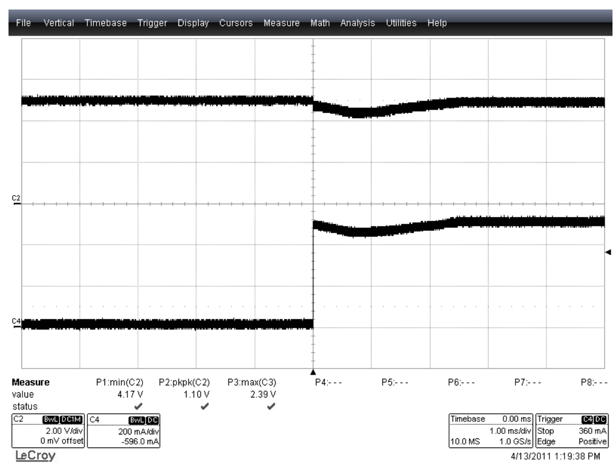

Figure 22 – 230 VAC, No-load to Full Load.
Minimum V_{OUT} 4.17 V
Upper: V_{RIPPLE}, 100 mV, 10 ms / div.
Lower: I_{LOAD}, 0.2 A / div.

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11.5 Short-Circuit Output Current

The photos below show the output current during auto-restart with the output shorted at the end of the #26 AWG cable.

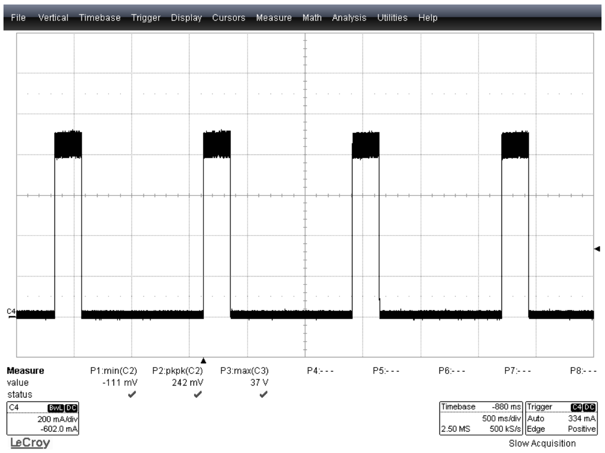

Figure 23 – 115 VAC. I_{OUT} 0.2 A / div, 500 ms / div.

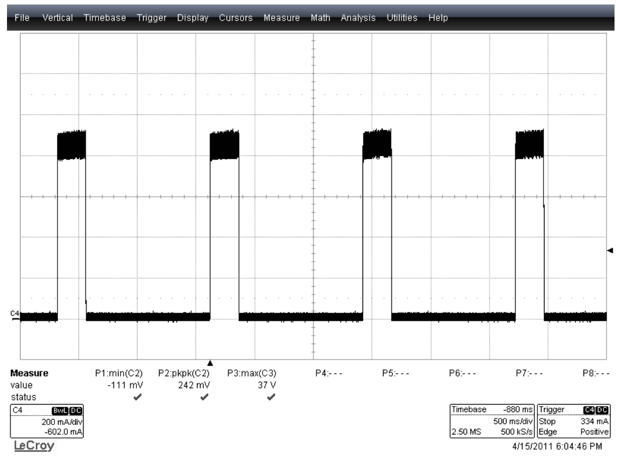

Figure 24 – 230 VAC. I_{OUT} 0.2 A / div, 500 ms / div.

11.6 Output Ripple Measurements

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

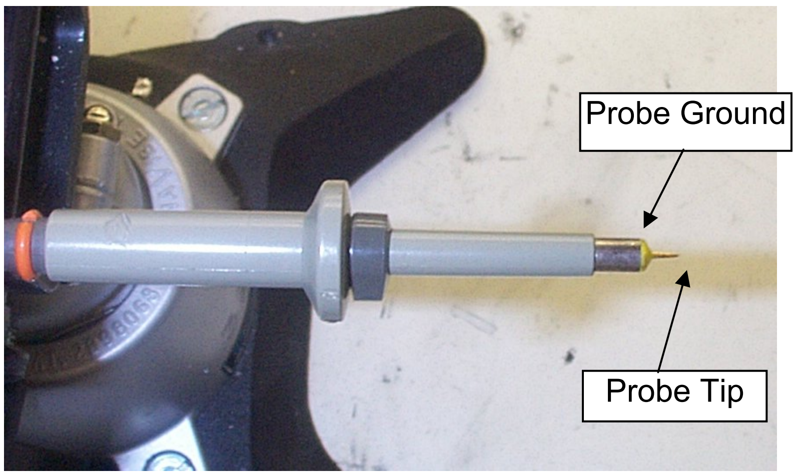

Figure 25 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

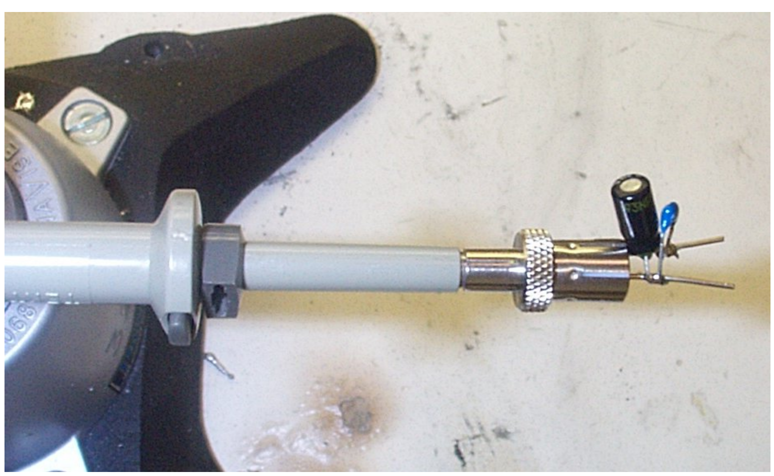

Figure 26 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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11.6.2 Output Ripple Measurement Results

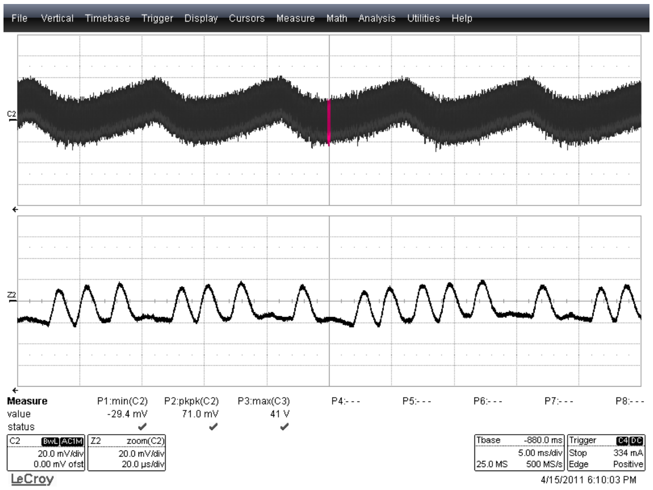

Figure 27 – 85 VAC, Full Load.
71 mV pk-pk
5 ms and 20 µs, 50 mV / div.

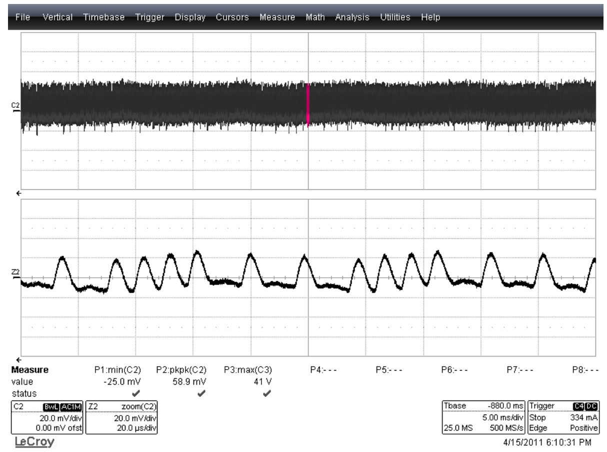

Figure 28 – 5 V Ripple, 115 VAC, Full Load.
60 mV pk-pk
5 ms and 20 µs, 50 mV / div.

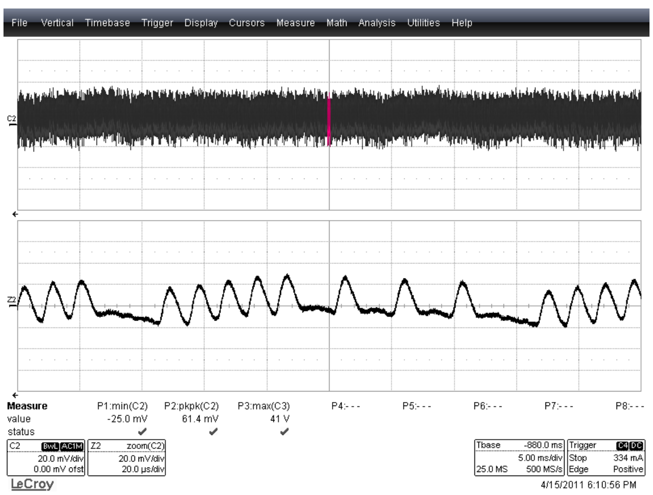

Figure 29 – 230 VAC, Full Load.
61.4 mV pk-pk
5 ms and 20 µs, 50 mV /div.

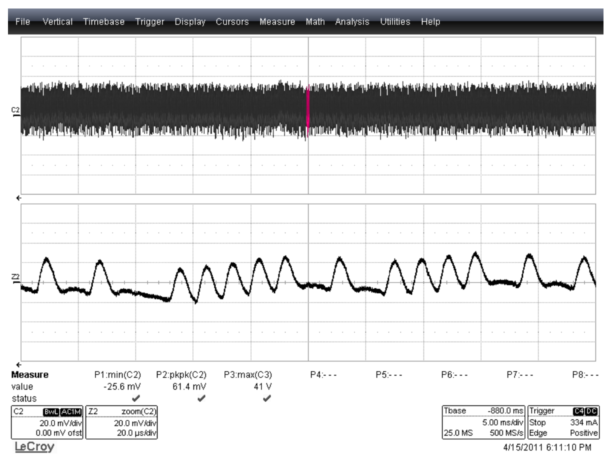

Figure 30 – 265 VAC, Full Load.
61.4 mV pk-pk
5 ms and 20 µs, 50 mV /div.

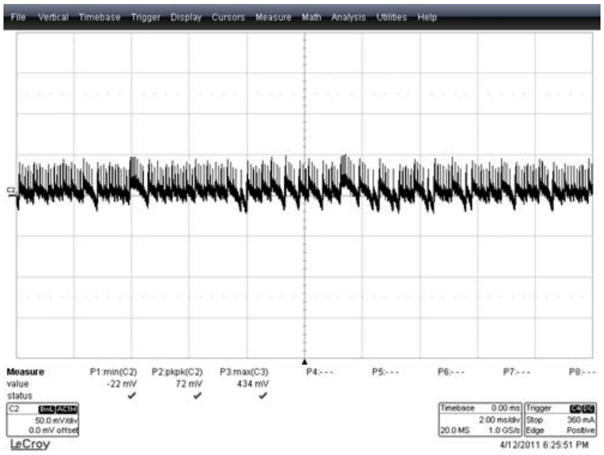

Figure 31 – 230 VAC, 0.088 A Load
72 mV pk-pk
5 ms, 50 mV /div.

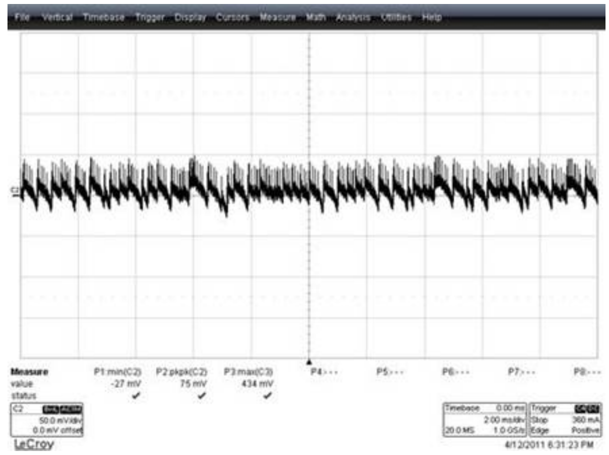

Figure 32 – 265 VAC, 89 mA Load.
75 mV pk-pk
5 ms, 50 mV /div.

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11.7 Common Mode Noise Voltage of the DC Output and Measure Set-up

The design passed requirements of EN 301 489-34 V1.1.1 (V_{CM}< 95 V_{P-P}).

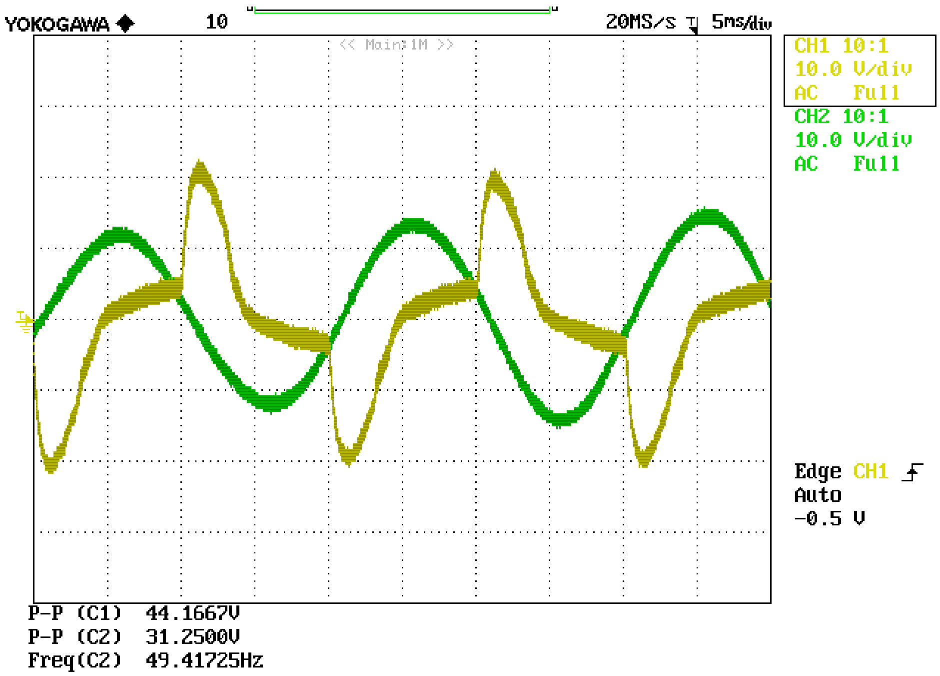

Figure 33 – 253 VAC 50 Hz, 10 Ω Load.
CH1: Common Mode Voltage; 10 V / div., 5 ms / div.
CH2: Reference Voltage; 10 V / div., 5 ms / div.

11.8 Common Mode Noise Voltage Measurement Set-up Diagram

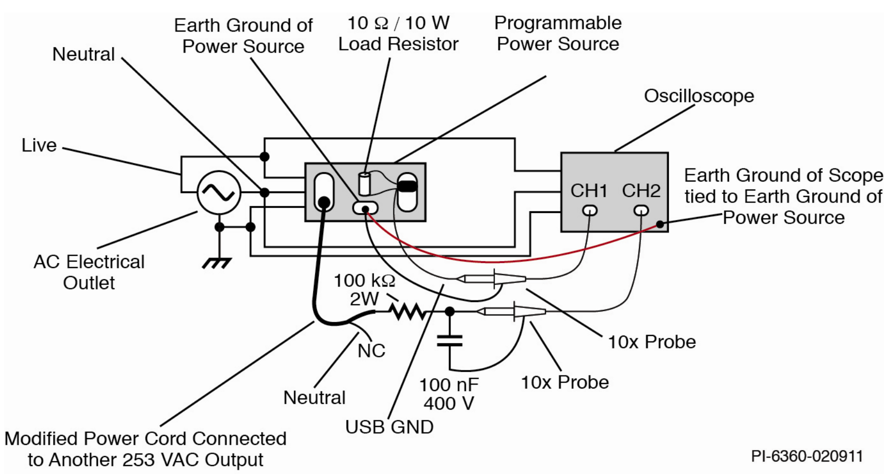

Figure 34 – Set-up Diagram.

11.8.1 Common Mode Noise Voltage Verification Set-up

AC Source: KIKUSUI PCR1000M set at V_{OUT}: 253 VAC / 50 Hz
Oscilloscope: LecRoya 104MXi-A
CH1: TEST VOLTAGE; 10x PROBE; 10 V / div.; 5 ms / div.; Full BW
CH2: REFERENCE VOLTAGE; 10x PROBE; 10 V / div.; 5 ms / div.; Full BW

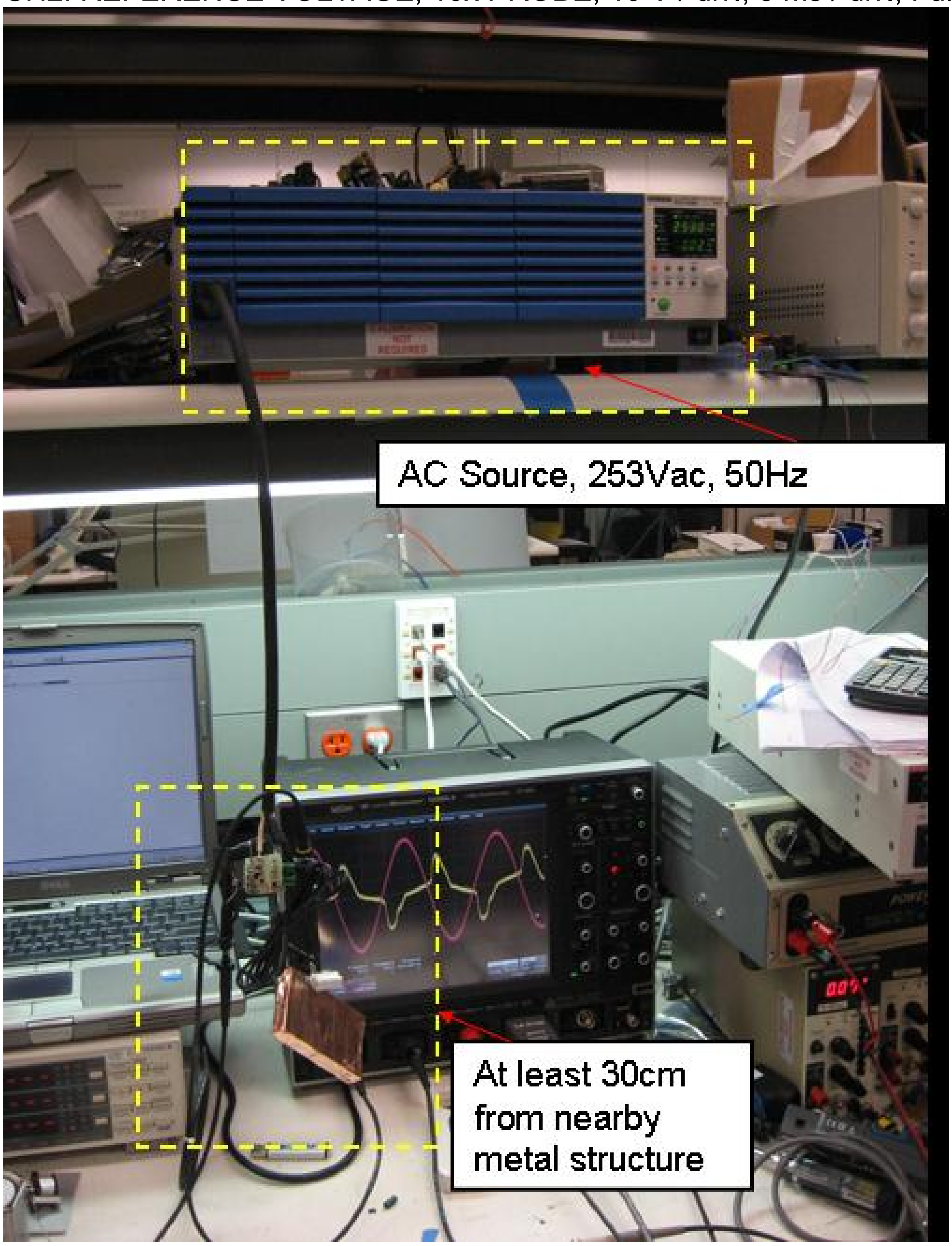

Figure 35 – Common Mode Noise Voltage Verification Test Set-up.

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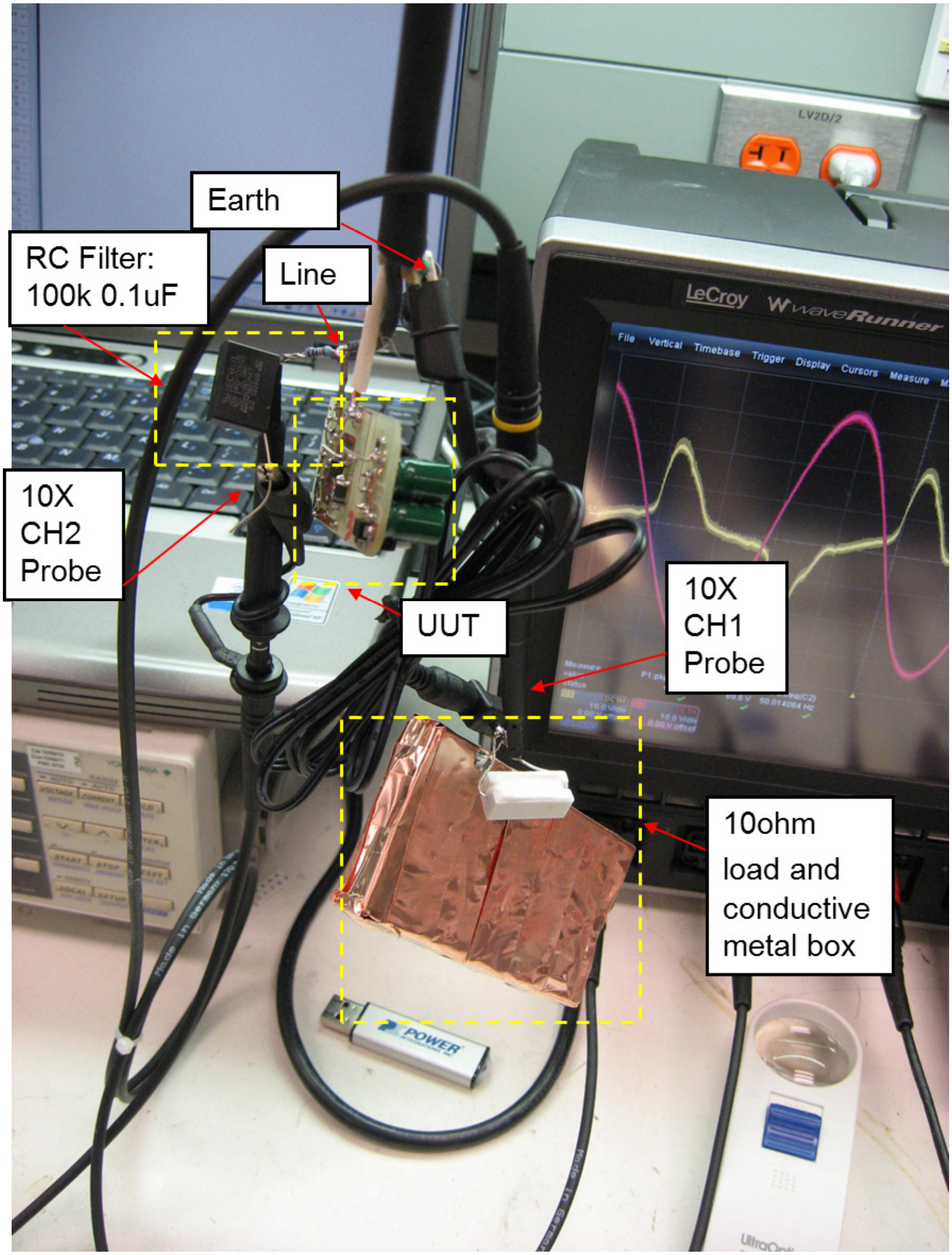

Figure 36 – Common Mode Noise Voltage Verification Test Set-up.

12 Line Surge

Differential and common mode input line 1.2 / 50 μs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+2000	230	L, N to Output	90	Pass
-2000	230	L, N to Output	90	Pass

100 kHz ring wave, 500 A short circuit current, differential and common mode.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
1000	230	L to N	90	Pass
1000	230	L, N to Output	90	Pass

Unit passes under all test conditions.

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13 Conducted EMI

EMI of line and neutral were scanned into the same picture, with output return connected at artificial hand. Margin of 9 dB was measured at both high line and low line.

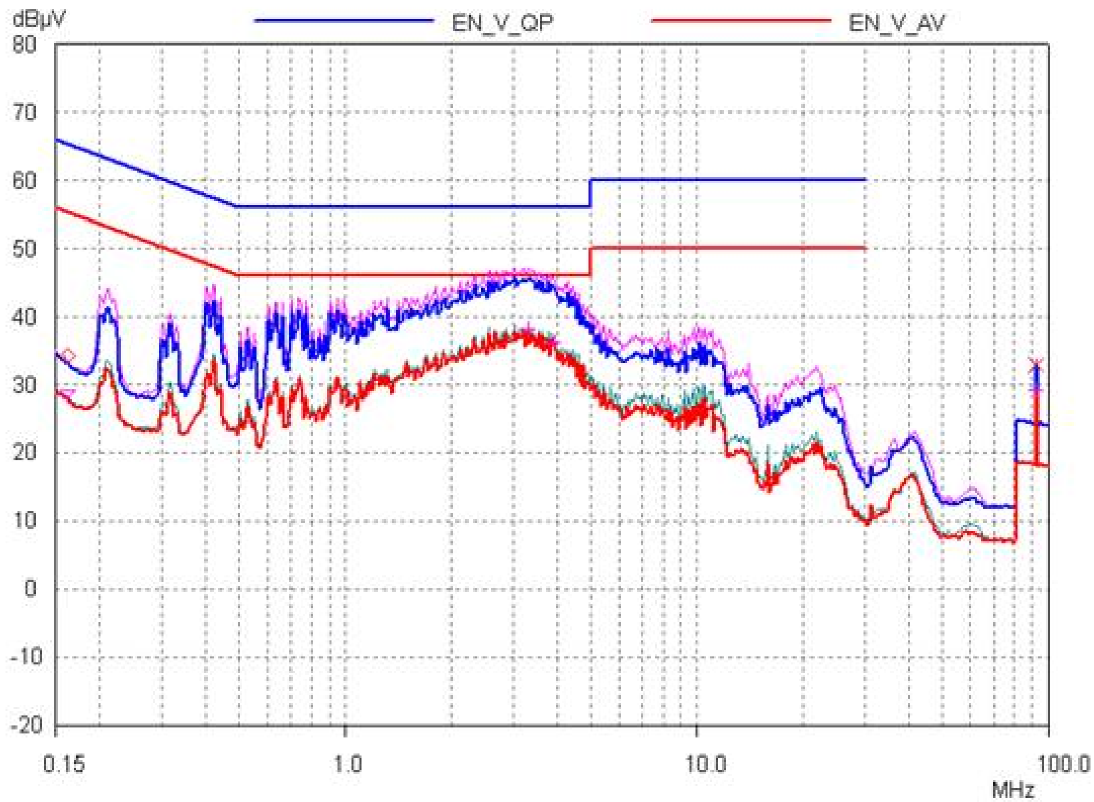

Figure 37 – Conducted EMI, Maximum Steady-State Load with Artificial Hand 115 VAC, 60 Hz, and EN55022 B Limits.

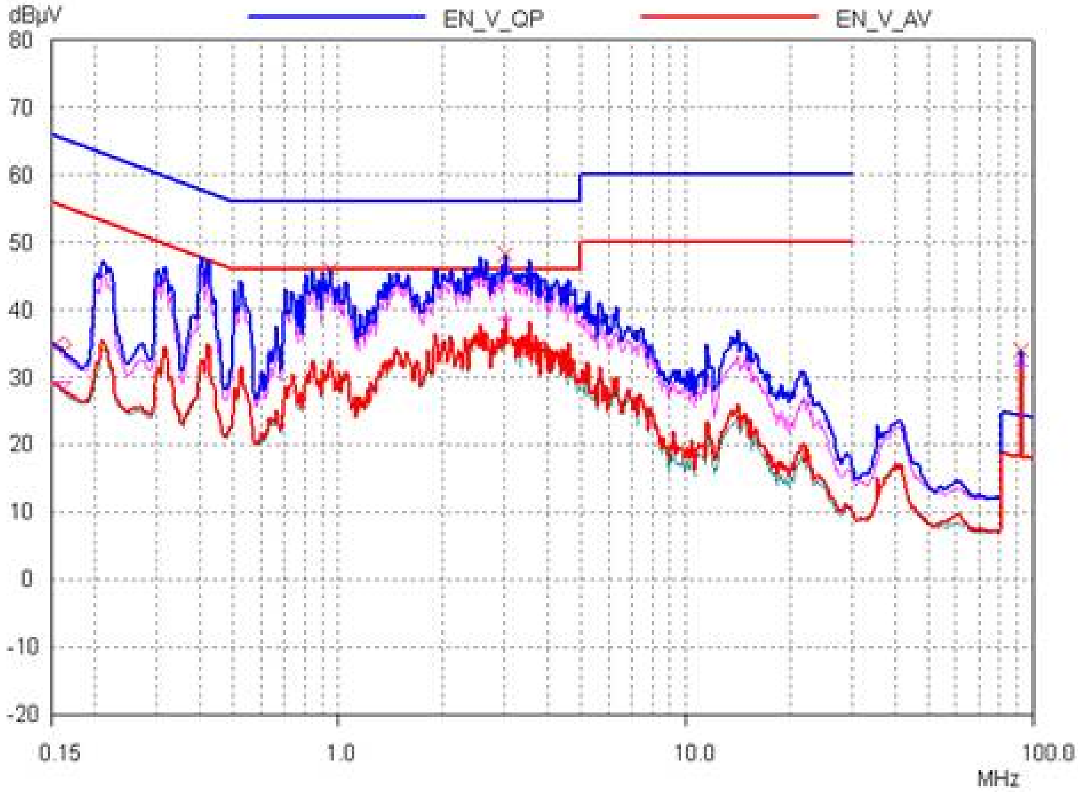

Figure 38 – Conducted EMI, Maximum Steady-State Load With Artificial Hand, 230 VAC, 60 Hz, and EN55022 B Limits.

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14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
08-Jul-11	PL	1.0	Initial Release	Apps and Mktg

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