Design Example Report

Title	***4.5 W Power Factor Corrected LED Driver (Non-Isolated Buck Boost) Using LinkSwitch™-PL LNK458KG***
Specification	85 VAC – 132 VAC Input; 48 V, 93 mA Output 48 V, 60 mA Output 96 V, 45 mA Output
Application	LED Driver for B10 Lamp Replacement
Author	Applications Engineering Department
Document Number	DER-297
Date	February 17, 2012
Revision	1.7

Summary and Features

- Single-stage power factor corrected and accurate constant current (CC) output
- Low cost, low component count and small PCB footprint solution
- Highly energy efficient, >87% at 115 VAC input for 48 V and >87% for 96 V output
- Superior performance and end user experience
  - Fast start-up time (<300 ms) – no perceptible delay
- Integrated protection and reliability features
  - Single shot no-load protection / output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis protects both components and PCB
  - No damage during brown-out conditions
- PF >0.95 at 115 VAC
- %A THD <20% at 115 VAC
- Meets IEC ring wave, differential line surge and EN55015 conducted EMI

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Important Note:
Although this board is designed to satisfy safety requirements for non-isolated LED drivers, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a non-isolated LED driver (power supply) utilizing a LNK458KG from the LinkSwitch-PL family of devices.

The DER-297 provides a single constant current output with an output power of 4.5 W. The board can be easily configured for output voltages from 35 V to 100 V as shown in the example table below.

The key design goals were high efficiency and small size, enabling the driver to fit into candelabra and B10 sized lamps and maximize efficacy.

Output / Part	35 V_{NOM} / 130 mA η≥85%	48 V_{NOM} / 93 mA η≥87%	48 V_{NOM} / 60 mA η≥86%	96 V_{NOM} / 45 mA η≥87%
L3 (DC-DC Inductor)	330 μH	500 μH	725 μH	725 μH
R3 (Sense Resistor)	2.2 Ω	3.09 Ω	4.87 Ω	6.49 Ω
C7 (Output Capacitor)	22 μF / 50 V	22 μF / 63 V	22 μF / 63 V	10 μF / 200 V
VR1 (Open Load Zener Clamp)	47 V	56 V	56 V	110 V
Reference Document	RDR-271	DER-297	DER-297	DER-297

The board was optimized to operate over the low AC input voltage range (85 VAC to 132 VAC, 47 Hz to 63 Hz). LinkSwitch-PL based designs provide a high power factor (>0.95) meeting current international requirements.

The form factor of the board was chosen to meet the requirements for standard B10 LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate the output of the supply and the LED load from the user.

The design was not optimized for operation with phase controlled (TRIAC) dimmers but this is possible with some modification and a resultant reduction in efficiency.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, design spreadsheet and performance data.

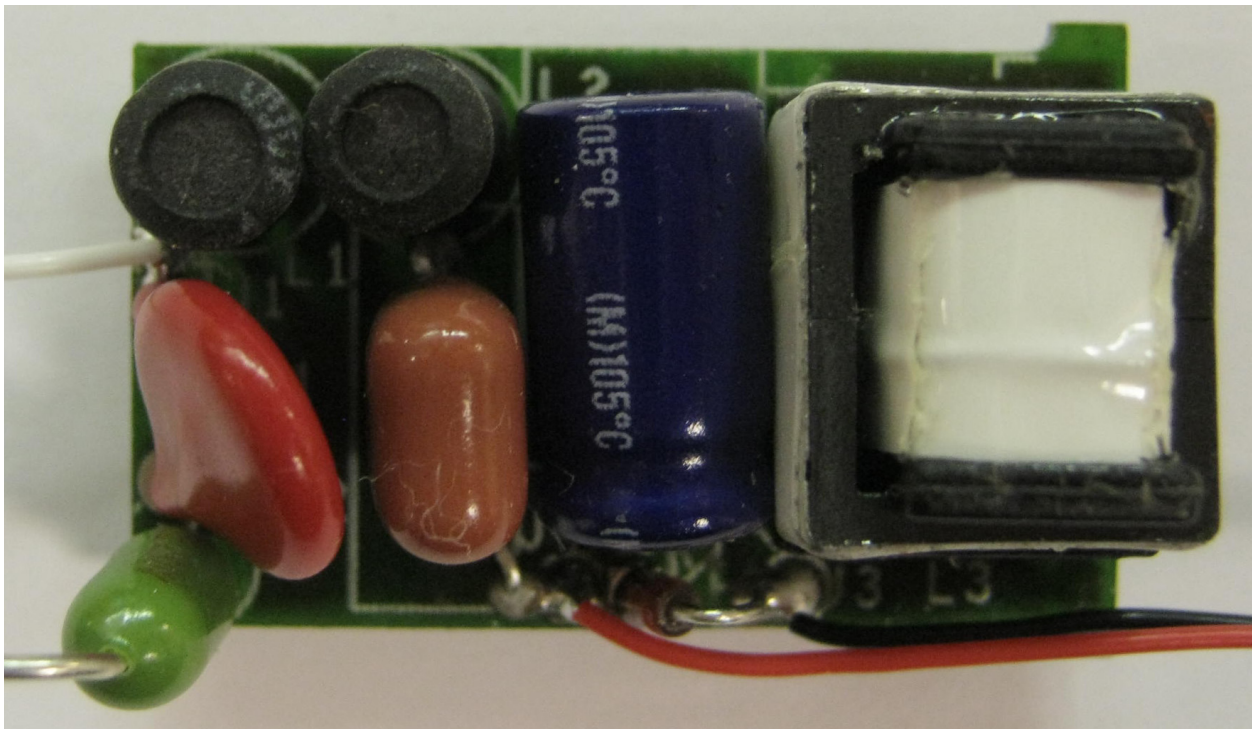

Figure 1 – Size of a Populated Circuit Board. Top Side

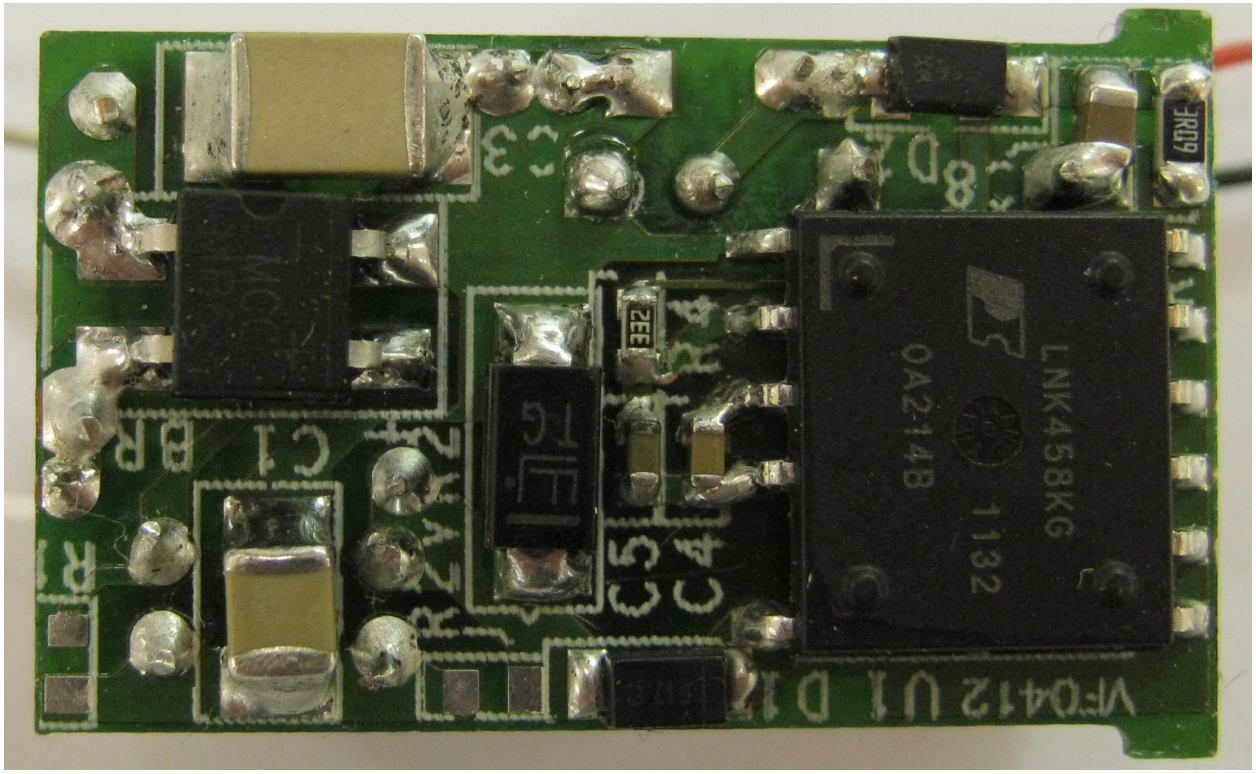

Figure 2 – Size of a Populated Circuit Board. Bottom Side

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2 Power Supply Specifications

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 48 V, 93 mA Version

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115	132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Power Factor		0.9				At any line input voltage
%ATHD				20		
Output						
Output Voltage	V_{OUT}		48		V	
Output Current	I_{OUT}	87	93	97	mA	
Total Output Power						
Continuous Output Power	P_{OUT}		4.5		W	
Efficiency						
Nominal	η		87		%	Measured at P_{OUT} 25°C at 115 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				
Line Surge Differential Mode (L1-L2)			1		kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	2 Ω short-circuit Series Impedance

2.2 48 V, 60 mA Version

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115	132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Power Factor		0.9				At any line input voltage
%ATHD				25		
Output						
Output Voltage	V_{OUT}		48		V	
Output Current	I_{OUT}	56	60	64	mA	
Total Output Power						
Continuous Output Power	P_{OUT}		2.9		W	
Efficiency						
Nominal	η		86		%	Measured at P_{OUT} 25°C at 115 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				
Line Surge Differential Mode (L1-L2)			1		kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	2 Ω short-circuit Series Impedance

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2.3 96 V, 45 mA Version

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115	132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Power Factor		0.9				At any line input voltage
%ATHD				20		
Output						
Output Voltage	V_{OUT}		96		V	
Output Current	I_{OUT}	42	45	48	mA	
Total Output Power						
Continuous Output Power	P_{OUT}		4.3		W	
Efficiency						
Nominal	η		87		%	Measured at P_{OUT} 25°C at 115 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				
Line Surge Differential Mode (L1-L2)			1		kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	2 Ω short-circuit Series Impedance

3 Schematic

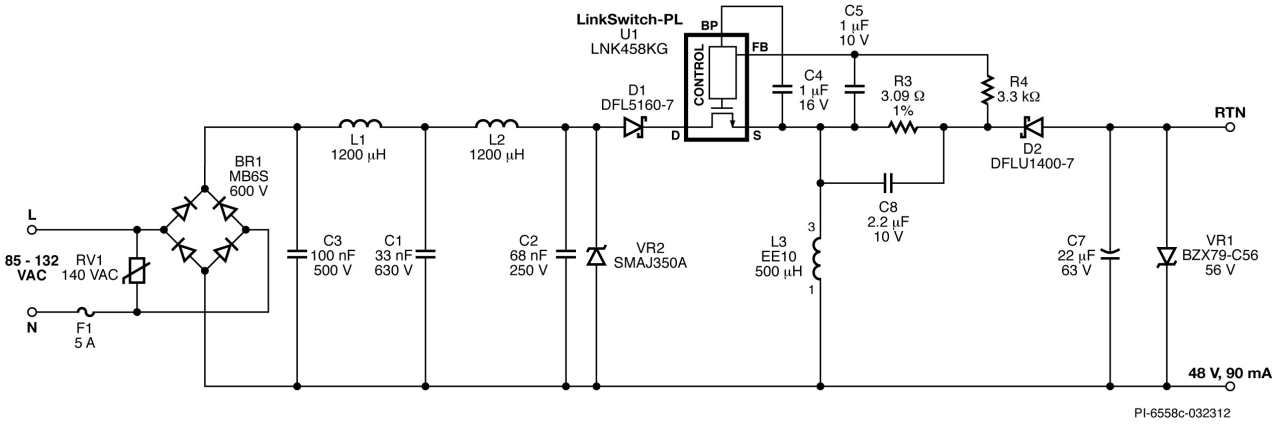

Figure 3a – 48 V, 93 mA Schematic.

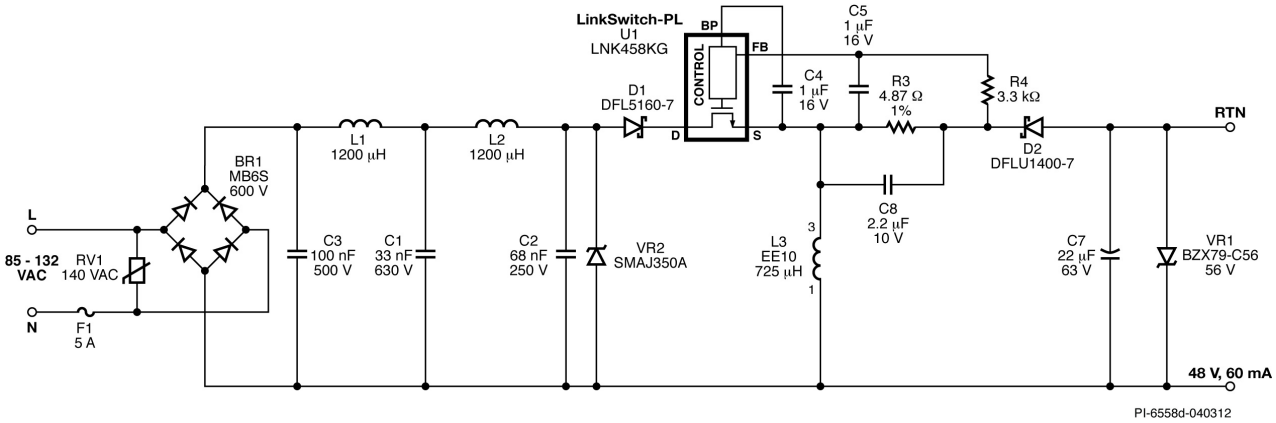

Figure 3b – 48 V, 60 mA Schematic.

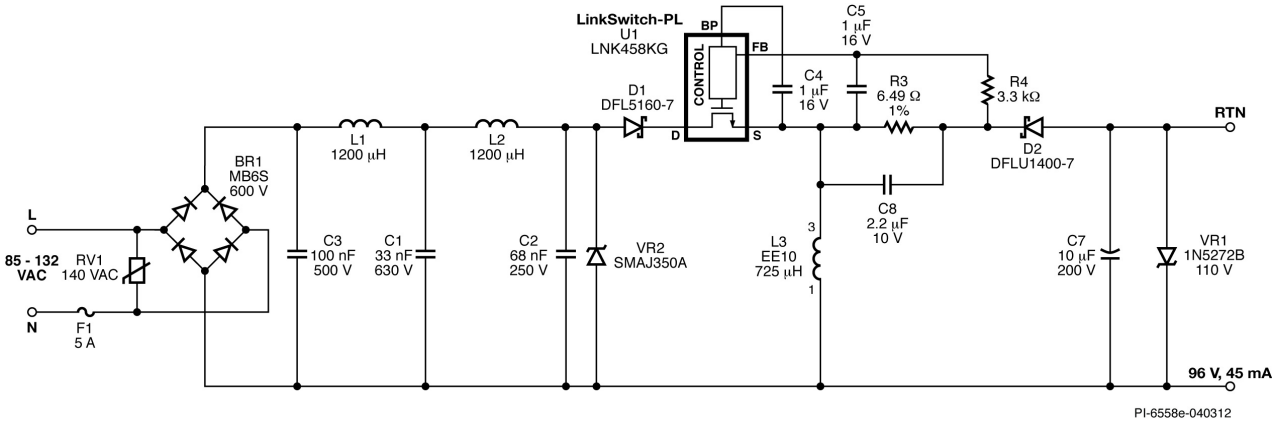

Figure 3c – 96 V, 45 mA Schematic.

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4 Circuit Description

The LinkSwitch-PL (U1) is a highly integrated primary side controller intended for use in LED driver applications. The LinkSwitch-PL provides high power factor in a single-stage conversion topology while regulating the output current across a range of input (85 VAC - 132 VAC) and output voltage variations typically encountered in LED driver applications. All of the control circuitry responsible for these functions plus a high-voltage power MOSFET are incorporated into the IC.

Important Note: The driver must always be connected to a load. Operating unloaded will cause the output overvoltage (OV) Zener diode VR1 to fail shorted (as designed). Once VR1 is shorted, the LinkSwitch-PL operates in auto-restart limiting the circuit dissipation to very low levels. This simple 0 V approach was taken to reduce component count, important due to space constraints of the design. An auto-recovering OV circuit can be implemented if desired, by replacing VR1 with and SCR, configured to a trigger above the normal output voltage range.

4.1 Input EMI Filtering

Fuse F1 provides protection against component failure. A fast 5 A rating (this being relatively high) was needed to prevent false opening during line surges. The maximum input voltage is clamped by RV1 and by VR2 (TVS) during differential line surges. Zener diode VR2 can be removed for a differential line surge requirement of ≤500 V.

The AC input is full wave rectified by BR1 (vs. half wave) to achieve good power factor and THD.

Capacitor C1, C2, C3 and differential choke L1 and L2 perform EMI filtering while the limited total capacitance maintains high power factor. This input 2-π filter network plus the frequency jittering feature of LinkSwitch-PL allows compliance with Class B emission limits. Provisional resistors R1 and R2 can be used to damp the resonance of the EMI filter if needed, preventing peaks in the EMI spectrum when measured in a system (driver plus enclosure).

- Inductor L1 and L2 are positioned after the bridge to avoid an imbalance in the EMI scan between line and neutral. This also gives leeway to use small high-voltage ceramic capacitors in the input filter.
- Film capacitor C2 can be increased from 68 nF to 100 nF to achieve more than 10 dBμV margin.

4.2 Buck Boost using LinkSwitch-PL

The buck boost power train is composed of U1 (power switch + control), D2 (free-wheeling diode), C7 (output capacitor), and L3 (inductor). Diode D1 was used to prevent negative voltage appearing across the drain-source of U1 especially near the zero-crossing of the input voltage. Capacitor C8 reduces the RMS current through R3,

improving efficiency. The bypass capacitor C4 provides the internal supply for the device when the power MOSFET is on.

- Diode D1 is a low drop diode (Schottky) type to maximize efficiency.
- Inductor L3 winding construction and wire gauge are optimized to minimize inter-winding capacitance and reduces AC losses.

4.3 Output Feedback

The output current feedback is sensed on the voltage drop across R3 and then filtered by a low pass filter (R4 and C5) to keep the LinkSwitch-PL operating point such that the average FEEDBACK (FB) pin voltage is 290 mV in steady-state operation.

4.4 Disconnected Load Protection

In order to avoid catastrophic failure of the output capacitor (C7) if the load is not connected, the output is protected by VR1. Zener diode VR1 will short the output if the load is not connected; this protection is not auto-recovering. Zener diode VR1 must be replaced in order to reuse the LED driver. Note that at the system level the LED load is always connected. If the system will be potted or enclosed tightly, VR1 might not be required.

Another option shown in Figure 6 is an auto-restart overvoltage protection. Zener VR1 is connected to V_{OUT+} and in series with blocking diode D3. If a no-load condition is present on the output of the supply, the output overvoltage Zener diode (VR1 in Figure 6) will conduct once its threshold is reached. A voltage VOV in excess of $V_{FB(AR)}$ = 2 V will appear across the FB pin and the IC will enter auto-restart.

This was not implemented due to PCB space constraint.

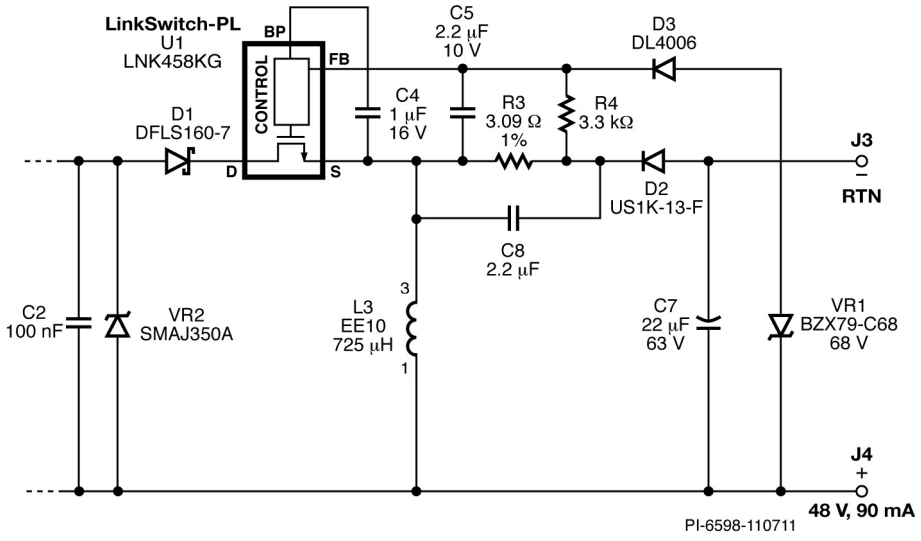

Figure 4 – Auto-Restart Overvoltage Protection with Buck-Boost Configuration.

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5 PCB Layout

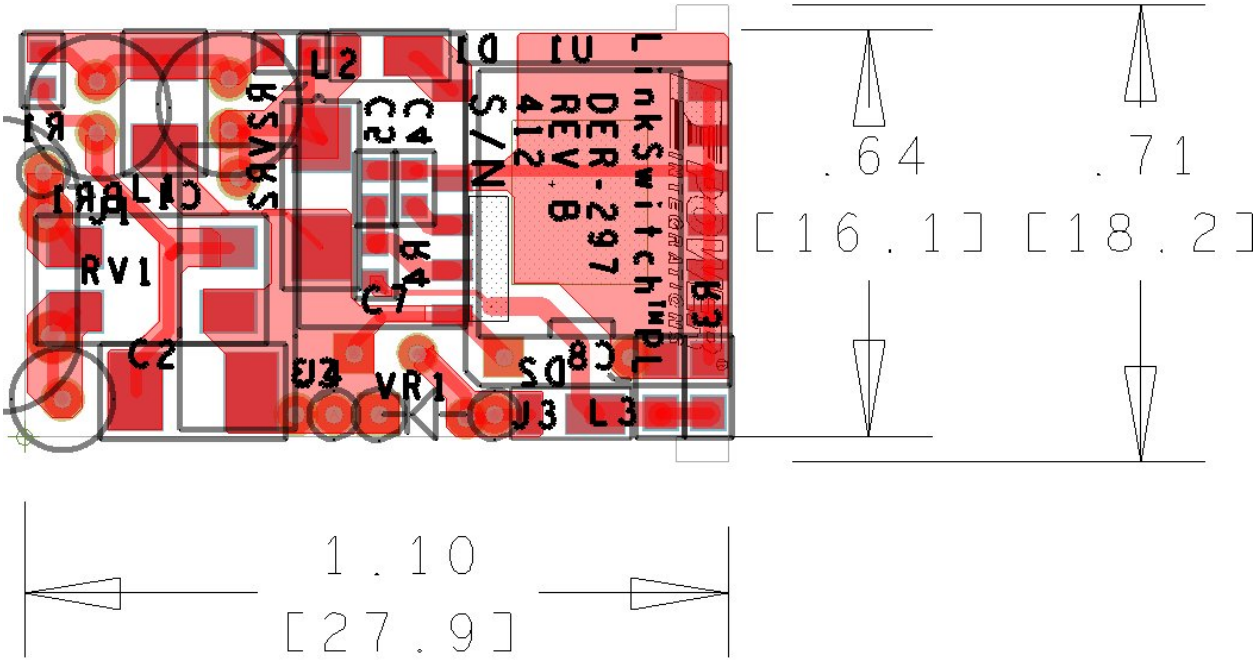

Figure 5 –Printed Circuit Layout, Dimensions (in. /[mm])

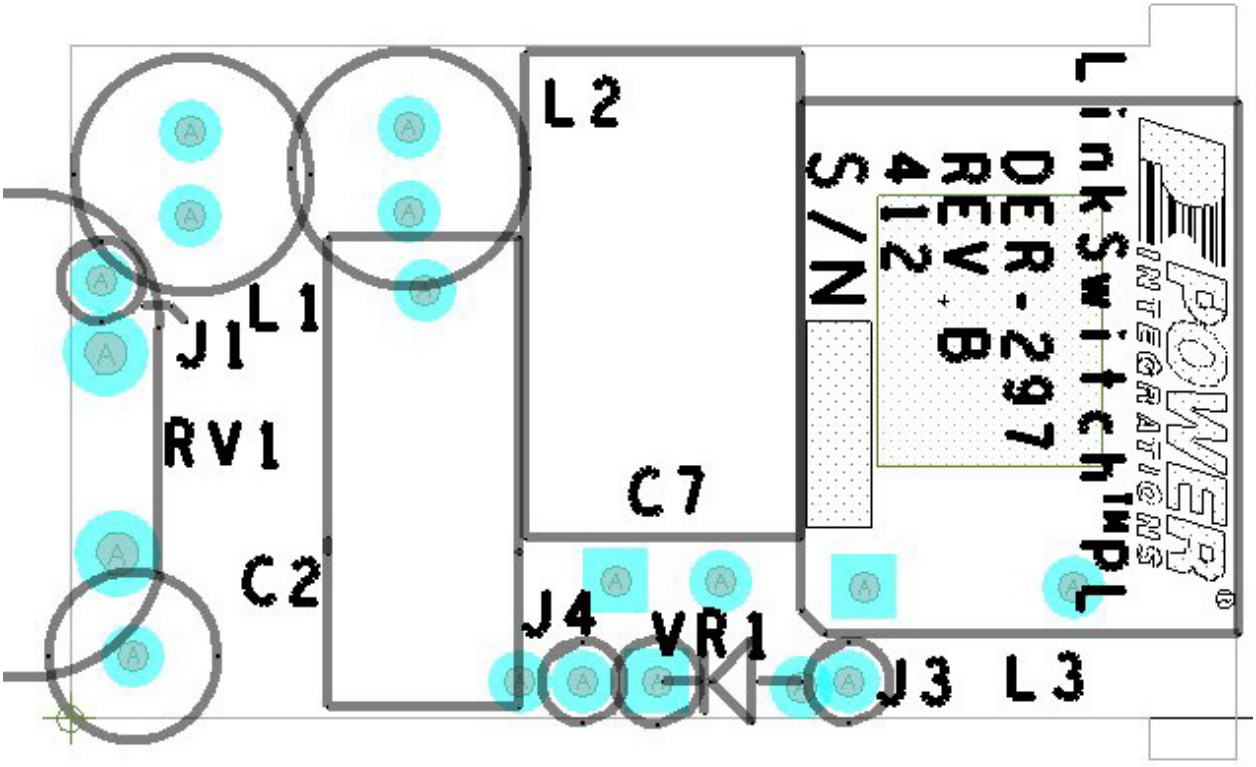

Figure 6 – Top Printed Circuit Layout.

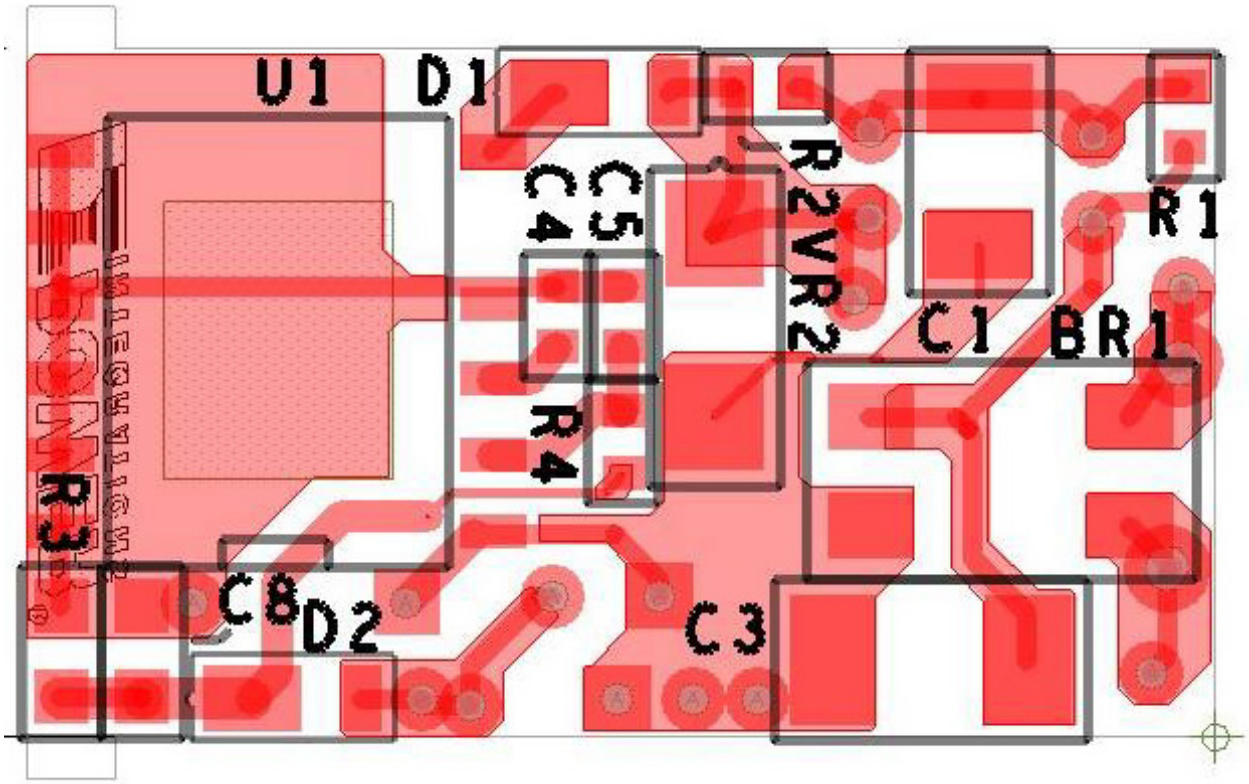

Figure 7 – Bottom Printed Circuit Layout.

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6 Bill of Materials

The table below is the reference design BOM.

6.1 48 V, 93 mA Version

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	33 nF, 630 V, Ceramic, X7R, 1210	GRM32DR72J333KW01L	Murata
3	1	C2	68 nF, 250 V, Polyester Film	ECQ-E2683KB	Panasonic
4	1	C3	100 nF, 500 V, Ceramic, X7R, 1812	VJ1812Y104KXEAT	Vishay
5	2	C4 C5	1 μF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
6	1	C7	22 μF, 63, Electrolytic, Low ESR, 1000 mΩ, (6.3 x 11.5)	ELXZ630ELL220MFB5D	Nippon Chemi-Con
7	1	C8	2.2 uF, 10 V, Ceramic, X7R, 0805	GRM21BR71A225MA01L	Murata
8	1	D1	60 V, 1 A, DIODE SCHOTTKY, PWRDI 123	DFLS160-7	Diodes, Inc.
9	1	D2	400 V, 1 A, DIODE SUP FAST 1A PWRDI 123	DFLU1400-7	Diodes, Inc.
10	1	F1	5 A, 250 V, Fast, Microfuse, Axial	0263005.MXL	LittleFuse
11	2	L1 L2	1200 μH, 0.060 A	RL-5480-1-1200	Renco
12	1	L3	Custom made EE10 Inductor, 500uH	TF-1003	Taiwan Shulin
13	1	R3	3.09 Ω, 1%, 1/8 W, Thick Film, 0805	RC0805FR-073R09L	Yageo
14	1	R4	3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
15	1	RV1	140 V, 12 J, 7 mm, RADIAL	V140LA2P	Littlefuse
16	1	U1	LinkSwitch-PL, eSOP-12P	LNK458KG	Power Integrations
17	1	VR1	56 V, 500 mW, 5%, DO-35	BZX79-C56	Taiwan Semi
18	1	VR2	350 V, 400 W, 5%, DO214AC (SMA)	SMAJ350A	LittleFuse

6.2 48 V, 60 mA Version

Make the following changes to modify the design from 48 V, 93 mA to 48 V, 60 mA.

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	L3	Custom made EE10 Inductor, 725 μH	TF-1003	Taiwan Shulin
2	1	R3	4.87 Ω, 1%, 1/8 W, Thick Film, 0805	RC0805FR-074R87L	Yageo

6.3 96 V, 45 mA Version

Make the following changes to modify design from 48 V, 93 mA to 96 V, 45 mA.

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C7	10 μF, 200 V, Electrolytic, (8 x 11)	SMQ200VB10RM8X11LL	Nippon Chemi-Con
2	1	L3	Custom made EE10 Inductor, 725 μH	TF-1003	Taiwan Shulin
3	1	R3	6.49 Ω, 1%, 1/8 W, Thick Film, 0805	RC0805FR-076R49L	Yageo
4	1	VR1	110 V, 5%, 500 mW, DO-35	1N5272B-TP	Micro Commercial

7 Inductor Specification

7.1 Electrical Diagram

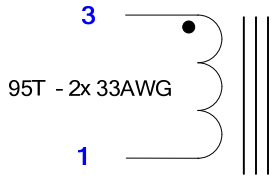

Figure 8 – 48 V Inductor Electrical Diagram.

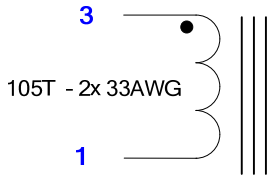

Figure 9 – 96 V Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}
48 V, 93 mA Version	500 µH ±5%
96 V, 45 mA / 48 V, 60 mA Versions	725 µH ±5%

7.3 Materials

Item	Description
[1]	Core: EE10/PC40
[2]	Bobbin: EE10, Horizontal, 8 pins, (4/4), Taiwan Shulin Enterprise Co., Ltd. or Kunshan Fengshunhe Electronics Co., Ltd Equivalent
[3]	Magnet Wire: 2 x #33 AWG
[4]	Loctite Super Glue Control Gel

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7.4 Inductor Build Diagram

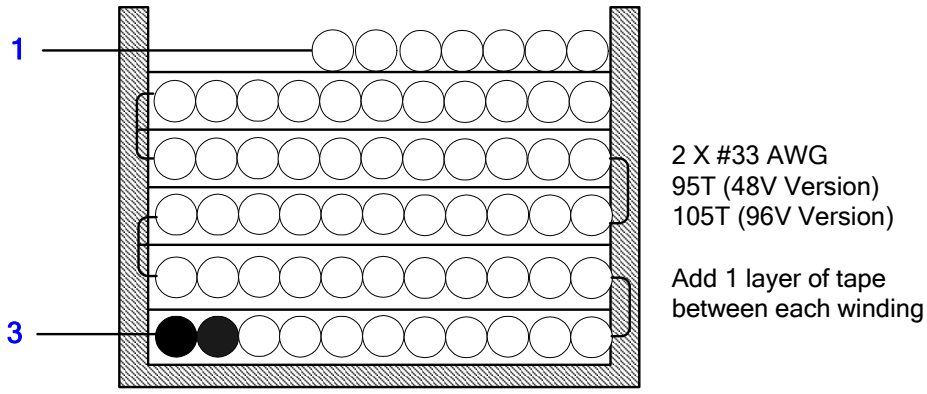

Figure 10 – Inductor Build Diagram.

7.5 Inductor Construction

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left (Figure 10). Winding direction is counter-clockwise.
WD1	Start at pin 3. Wind enough turns of item [3] as shown in Figure 10 with 1 layer of tape between the windings. Continue winding and terminate at pin 1. Note: eliminating the tape between layers will increase capacitance and reduce driver efficiency
Finish	Grind the core to get the specified inductance. Apply tape to secure both cores. Cut pins 2, 4, 5, 6, 7 and 8. Apply adhesive item [4] to core and bobbin to prevent core movement.

8 Inductor Design Spreadsheet

8.1 48 V Inductor Design Spreadsheet

Power Supply	INFO	OUTPUT	UNIT	LinkSwitch-PL Buck-boost Inductor Design Spreadsheet
VACMIN	85	85	V	Minimum AC input voltage
VACNOM	115	115	V	Nominal AC input voltage
VACMAX	132	132	V	Maximum AC input voltage
FL	60	60	Hz	Minimum line frequency
VO_MIN	40.00	40.0	V	Minimum output voltage tolerance
VO_NOM	48.00	48.00	V	Nominal Output Voltage
VO_MAX	54.00	54.00	V	Maximum output voltage tolerance
IO	0.093	0.093	A	Average output current specification
n	0.85	0.850	%/100	Total power supply efficiency
Z		0.5		Loss allocation factor
Enclosure	Retrofit Lamp	Retrofit Lamp		Enclosure selections determines thermal conditions and maximum power
PO		4.46	W	Total output power
VD	0.40	0.4	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES				
Device	LNK458	LNK458		Chosen LinkSwitch-PL Device
TON		1.85	us	Expected on-time of MOSFET at low line and PO
FSW		106.6	kHz	Expected switching frequency at low line and PO
Duty Cycle		19.8	%	Expected operating duty cycle at low line and PO
VDRAIN		262	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS		0.108	A	Nominal RMS current through the switch
IPK		0.691	A	Worst Case Peak current
ILIM_MIN		1.012	A	Minimum device current limit
KDP	1.22	1.21		Ratio between off-time of switch and reset time of core at VACNOM
Device	LNK458	LNK458		Chosen LinkSwitch-PL Device
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS				
RSENSE		3.118	Ohms	Output current sense resistor
Standard RSENSE		3.09	Ohms	Closest 1% value for RSENSE
PSENSE		27.0	mW	Power dissipated by RSENSE
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	EE10	EE10		Core Type
Core Part Number		Custom		Core Part Number (if Available)
Bobbin Part Number		Custom		Bobbin Part Number (if available)
AE	12.10	12.10	mm^2	Core Effective Cross Sectional Area
LE	26.10	26.10	mm	Core Effective Path Length
AL	850	850	nH/T^2	Ungapped Core Effective Inductance
BW	6.00	6	mm	Bobbin Physical Winding Width
L	5	5		Number of winding layers
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP		497.9	uH	Primary Inductance
LP Tolerance		5	%	Tolerance of Primary Inductance

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N	5.00	95	Turns	Number of Turns
ALG	95	55	nH/T^2	Gapped Core Effective Inductance
BM		2992	Gauss	Reduce BM < 3000 G. Decrease BP (increase NP) or increase core size.
BAC		1496	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
BP	*Warning*	5858	Gauss	!!! Reduce peak flux density (BP < 3600 G) by increasing NP, selecting a bigger core or decreasing KDP; See note below
LG		0.276	mm	Gap Length (Lg > 0.1 mm)
BWE		30	mm	Effective Bobbin Width
L_IRMS		0.257	A	RMS Curren through the inductor
OD		0.32	mm	Maximum Primary Wire Diameter including insulation
INS		0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.26	mm	Bare conductor diameter
AWG		30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		102	Cmils	Bare conductor effective area in circular mils
CMA		396	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Current Density (J)		5.04	A/mm^2	Inductor Winding Current density (3.8 < J < 9.75 A/mm^2)
Output Parameters				
IO		0.093	A	Expected Output Current
PIVS		59.8	V	Peak Inverse Voltage at VO_MAX on output diode

Note: Peak flux density is limited by slowly increasing the duty cycle of LinkSwitch-PL family during start-up.

8.2 96 V Inductor Design Spreadsheet

Power Supply	**INFO**	**OUTPUT**	**UNIT**	**LinkSwitch-PL Buck-boost Inductor Design Spreadsheet**
VACMIN	85	85	V	Minimum AC input voltage
VACNOM	115	115	V	Nominal AC input voltage
VACMAX	132	132	V	Maximum AC input voltage
FL	60	60	Hz	Minimum line frequency
VO_MIN	90.00	90.0	V	Minimum output voltage tolerance
VO_NOM	96.00	96.00	V	Nominal Output Voltage
VO_MAX	105.00	105.00	V	Maximum output voltage tolerance
IO	0.045	0.045	A	Average output current specification
n	0.85	0.850	%/100	Total power supply efficiency
Z		0.5		Loss allocation factor
Enclosure	Retrofit Lamp	Retrofit Lamp		Enclosure selections determines thermal conditions and maximum power
PO		4.32	W	Total output power
VD	0.40	0.4	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES				
Device	LNK458	LNK458		Chosen LinkSwitch-PL Device
TON		2.06	us	Expected on-time of MOSFET at low line and PO
FSW		122.1	kHz	Expected switching frequency at low line and PO
Duty Cycle		25.2	%	Expected operating duty cycle at low line and PO
VDRAIN		312	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS		0.094	A	Nominal RMS current through the switch
IPK		0.517	A	Worst Case Peak current

ILIM_MIN		1.012	A	Minimum device current limit
KDP	1.25	1.76		Ratio between off-time of switch and reset time of core at VACNOM
Device	LNK458	LNK458		Chosen LinkSwitch-PL Device
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS				
RSENSE		6.444	Ohms	Output current sense resistor
Standard RSENSE		6.49	Ohms	Closest 1% value for RSENSE
PSENSE		13.1	mW	Power dissipated by RSENSE
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	EE10	EE10		Core Type
Core Part Number		Custom		Core Part Number (if Available)
Bobbin Part Number		Custom		Bobbin Part Number (if available)
AE	12.10	12.10	mm^2	Core Effective Cross Sectional Area
LE	26.10	26.10	mm	Core Effective Path Length
AL	850	850	nH/T^2	Ungapped Core Effective Inductance
BW	6.00	6	mm	Bobbin Physical Winding Width
L	5	5		Number of winding layers
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP		728.7	uH	Primary Inductance
LP Tolerance	5.00	5	%	Tolerance of Primary Inductance
N	105	105	Turns	Number of Turns
ALG		66	nH/T^2	Gapped Core Effective Inductance
BM	*Info*	2964	Gauss	Reduce BM < 3000 G. Decrease BP (increase NP) or increase core size.
BAC		1482	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
BP	*Warning*	7756	Gauss	!!! Reduce peak flux density (BP < 3600 G) by increasing NP, selecting a bigger core or decreasing KDP; See note below
LG		0.230	mm	Gap Length (Lg > 0.1 mm)
BWE		30	mm	Effective Bobbin Width
L_IRMS		0.166	A	RMS Curren through the inductor
OD		0.29	mm	Maximum Primary Wire Diameter including insulation
INS		0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.23	mm	Bare conductor diameter
AWG		31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		81	Cmils	Bare conductor effective area in circular mils
CMA		486	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Current Density (J)		4.11	A/mm^2	Inductor Winding Current density (3.8 < J < 9.75 A/mm^2)
Output Parameters				
IO		0.045	A	Expected Output Current
PIVS		115.9	V	Peak Inverse Voltage at VO_MAX on output diode

Note: The peak flux density warning (BP) can be ignored for this design. The spreadsheet BP calculation assumes that the LNK458KG will operate at $I_{LIM(MAX)}$ during start-up. In practice, due to the internal soft-start function this current level is not reached and therefore no core saturation occurs. This was confirmed in both Figures 31 and 32 for normal start-up and Figures 45 and 46 for start-up with a shorted output (fault condition). In all cases, the peak drain current is below the absolute maximum data sheet specification.

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9 Performance Data

All measurements performed at 25 ºC room temperature, 60 Hz input frequency unless otherwise specified.

9.1 Active Mode Efficiency

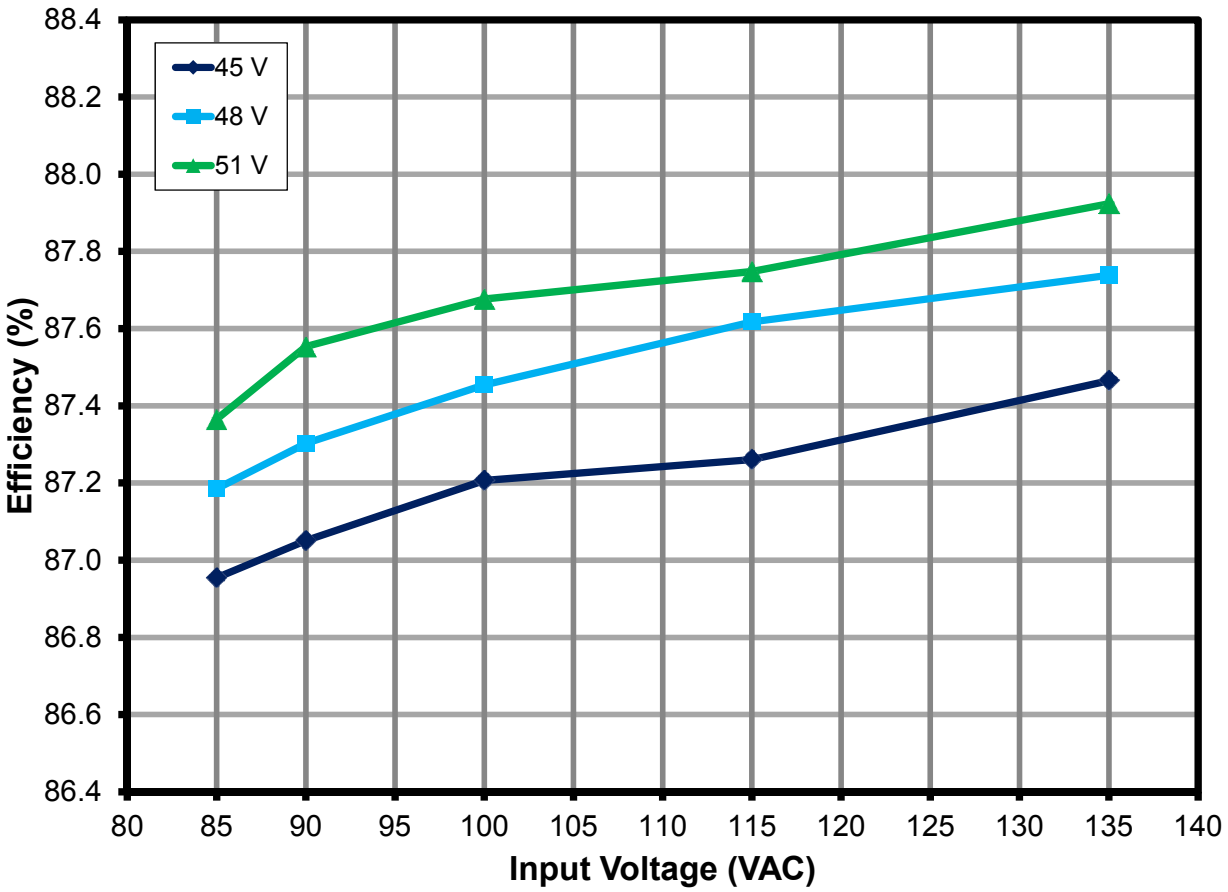

Figure 11 – Efficiency with Respect to AC Input Voltage for 48 V, 93 mA Version.

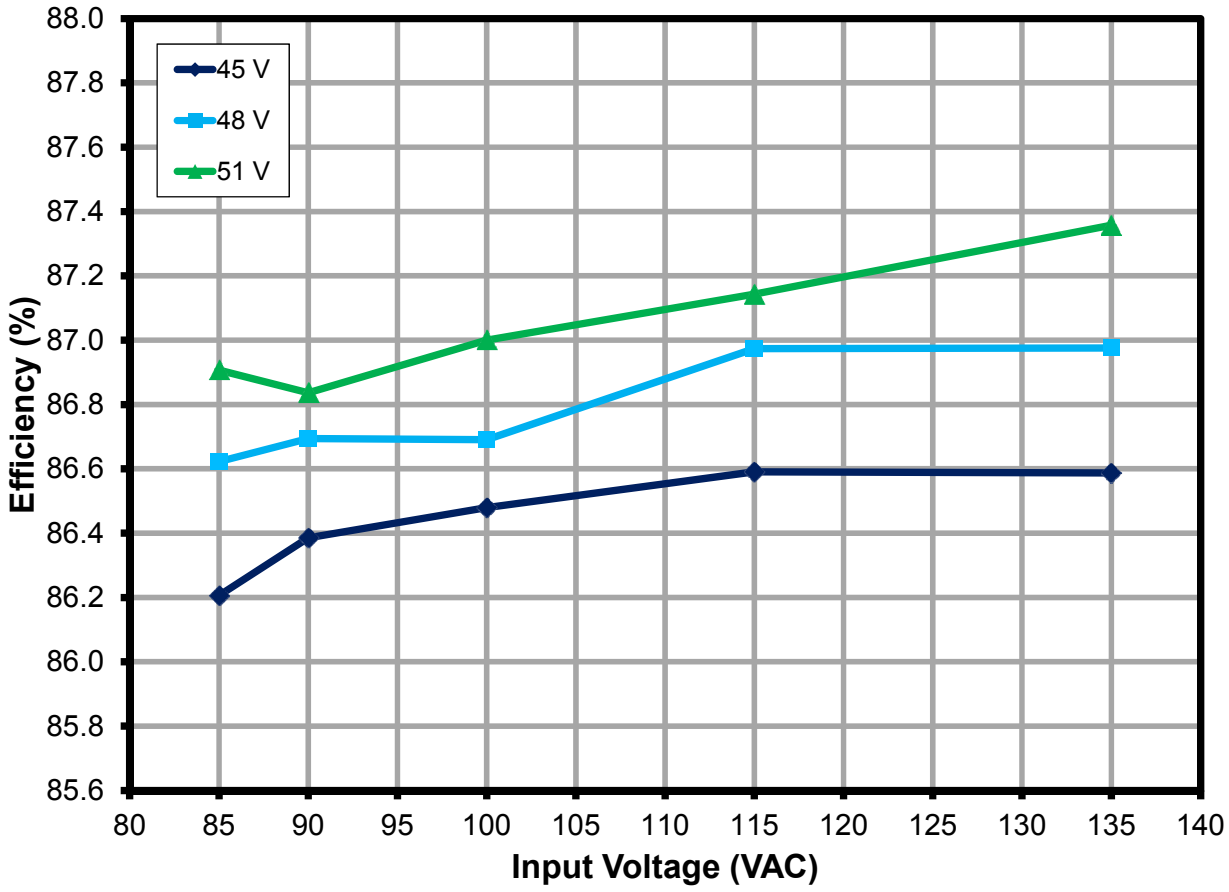

Figure 12 – Efficiency with Respect to AC Input Voltage for 48 V, 60 mA Version.

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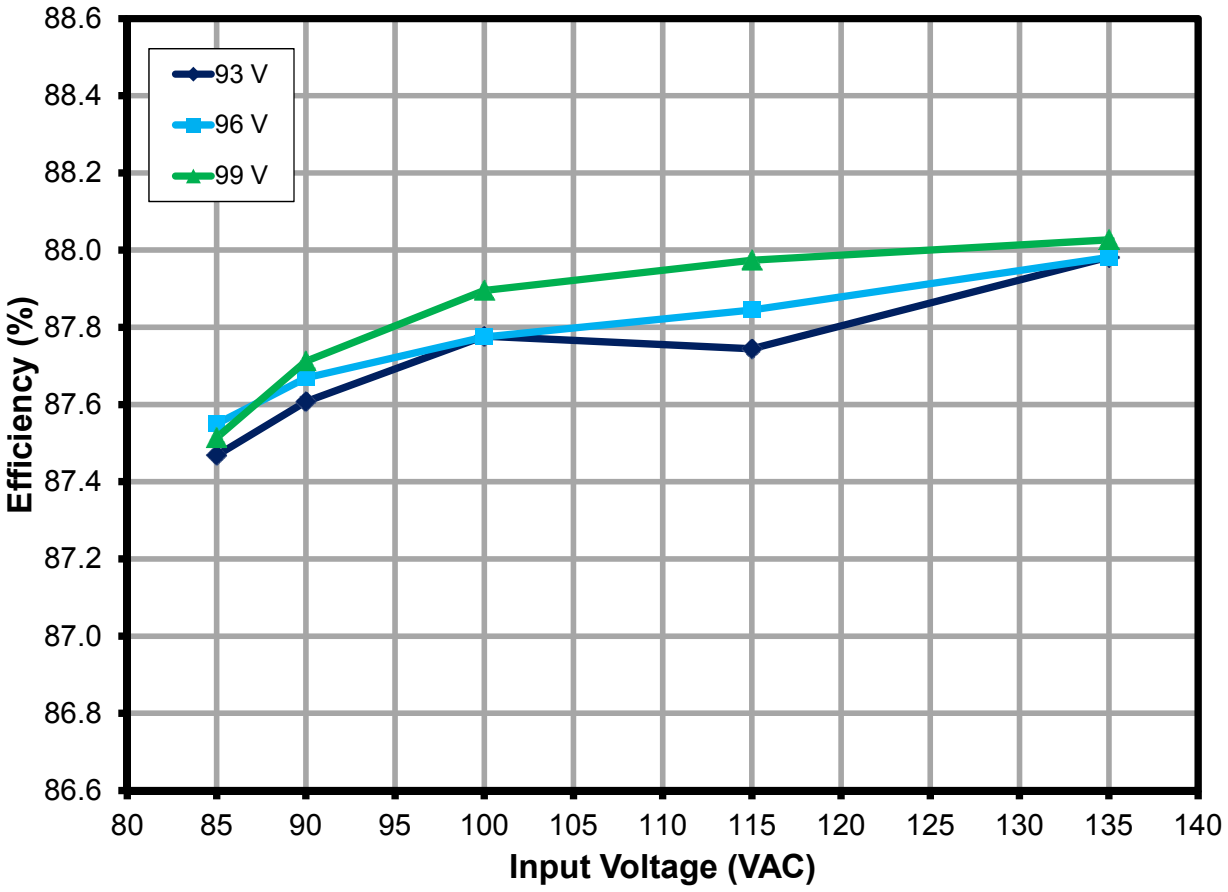

Figure 13 – Efficiency with Respect to AC Input Voltage for 96 V Version.

9.2 Line Regulation

The LinkSwitch-PL device regulates the output by controlling the MOSFET on-time and switching frequency to maintain the average FB pin at its 0.29 V threshold. Slight changes in output current may be observed when input or output conditions are changed or after AC cycling due to the device selecting a slightly different operating state (selection of on-time and frequency).

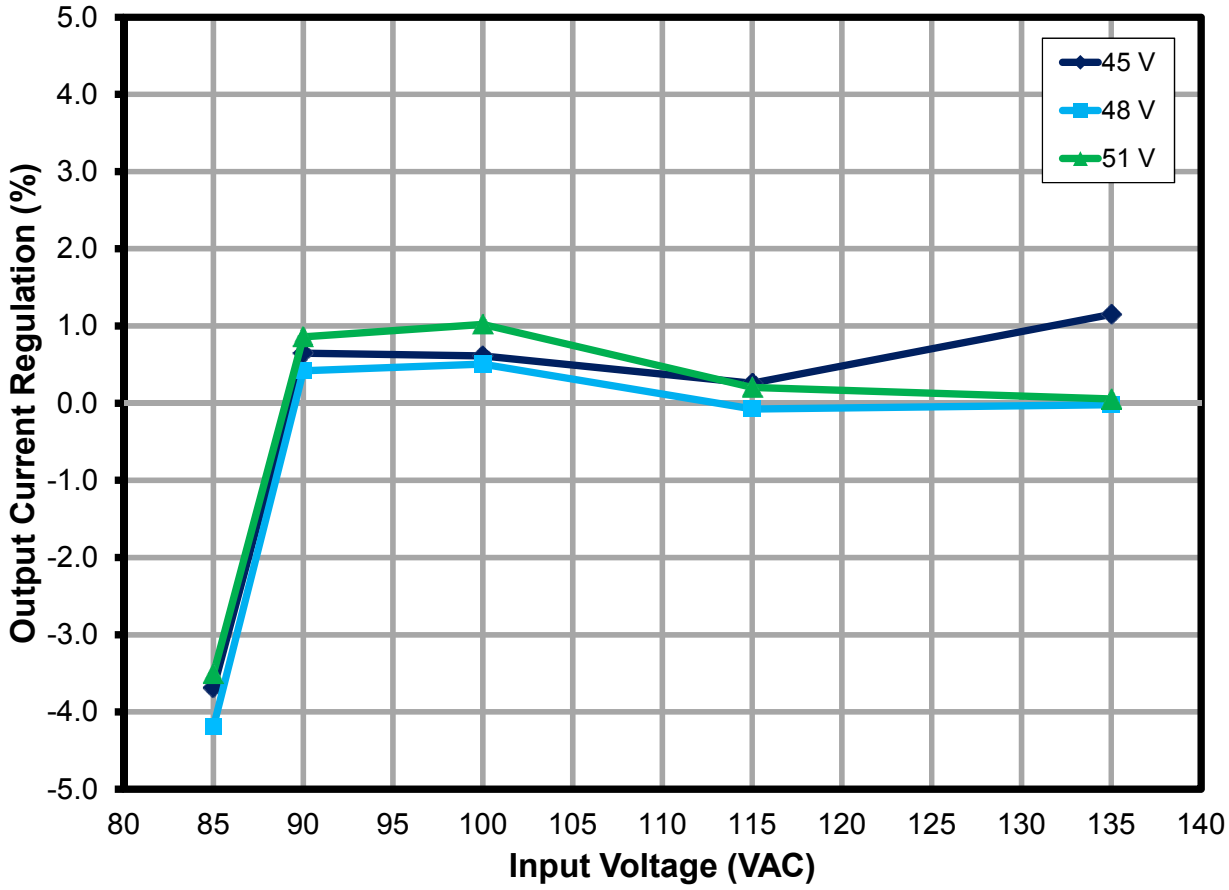

Figure 14 – Line Regulation, Room Temperature for 48 V, 93 mA Version.

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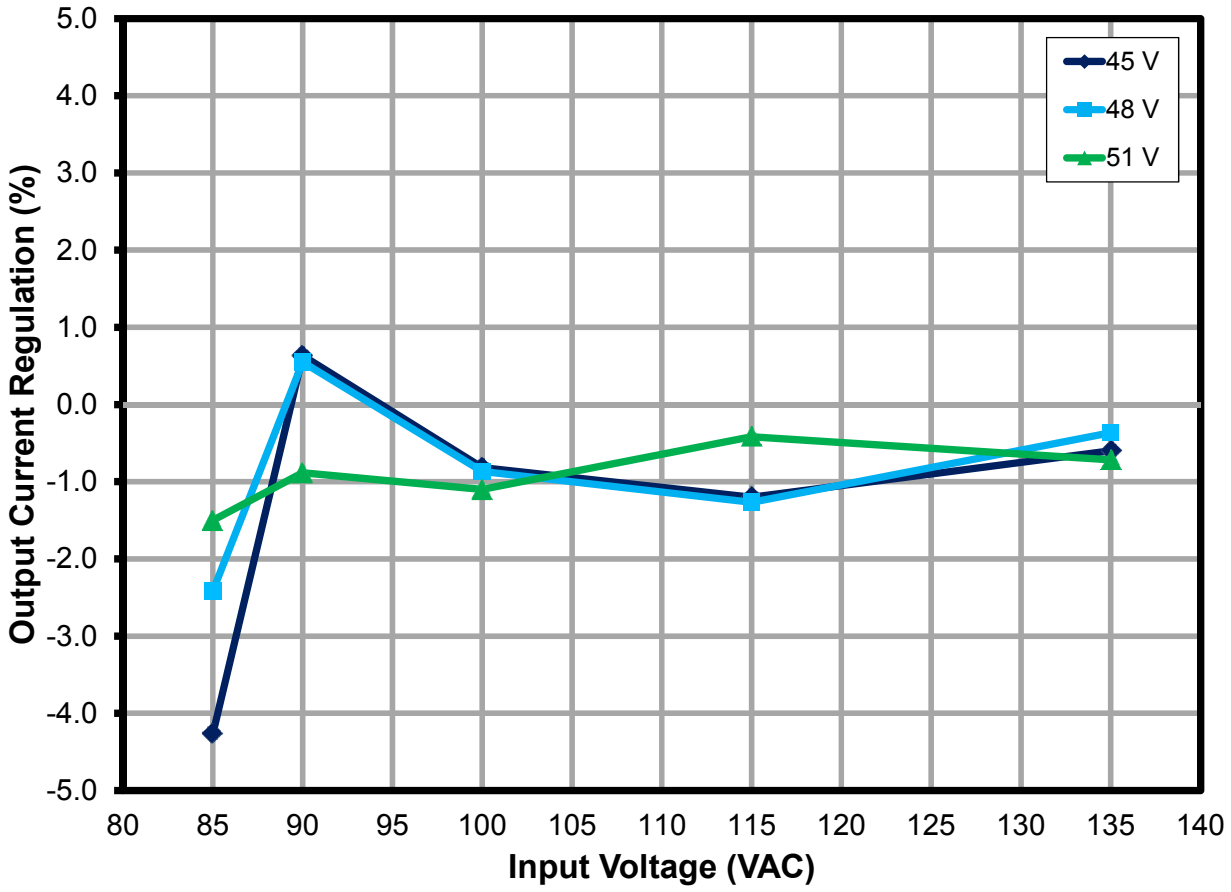

Figure 15 – Line Regulation, Room Temperature for 48 V, 60 mA Version.

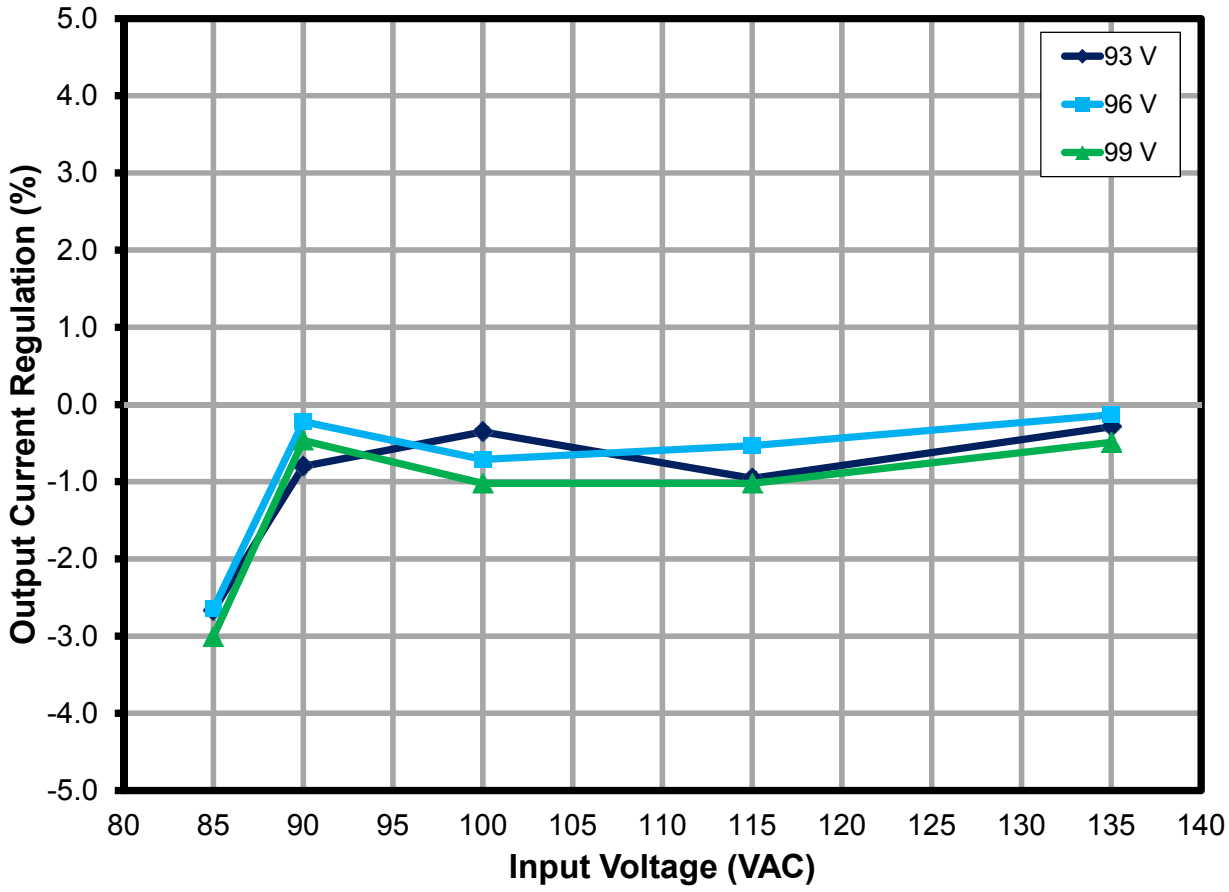

Figure 16 – Line Regulation, Room Temperature for 96 V Version.

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9.3 Power Factor

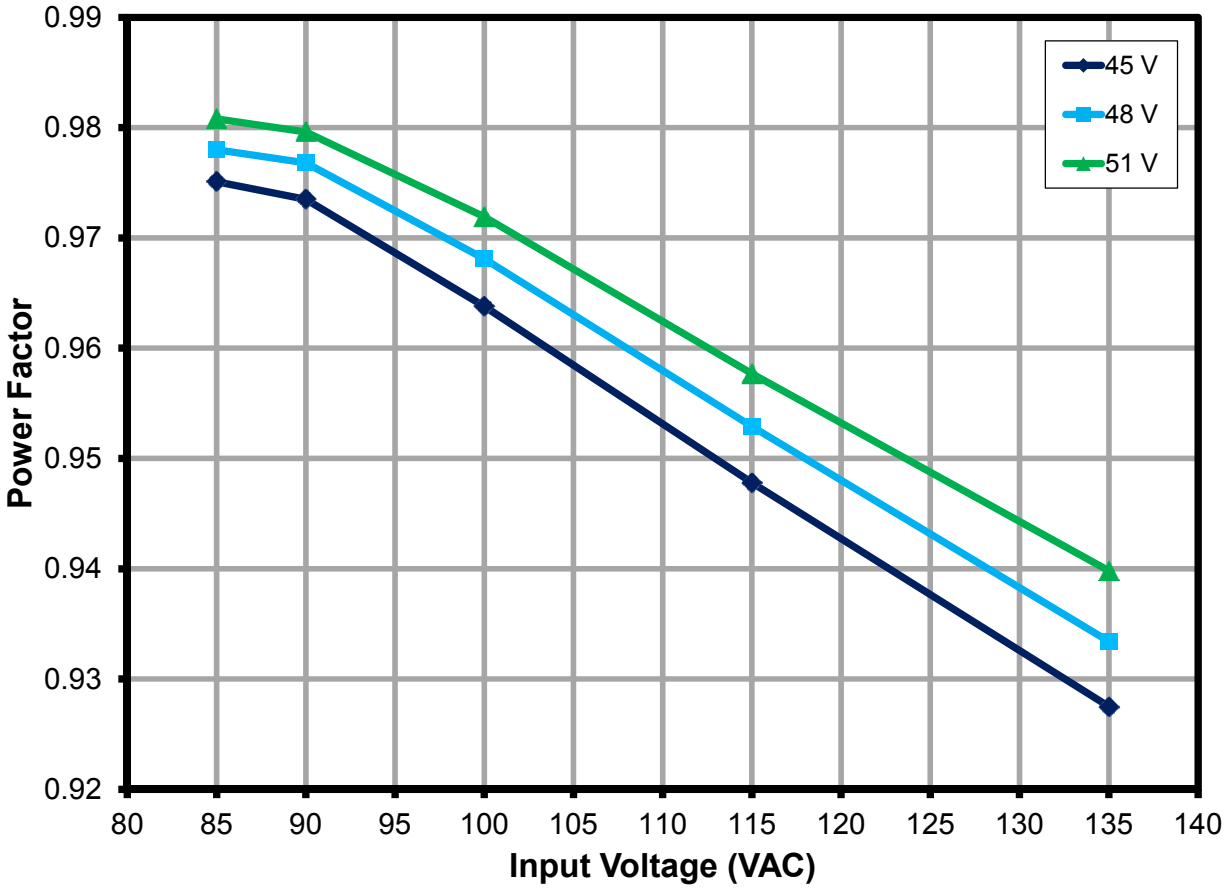

Figure 17 – High Power Factor within the Operating Range for 48 V, 93 mA Version.

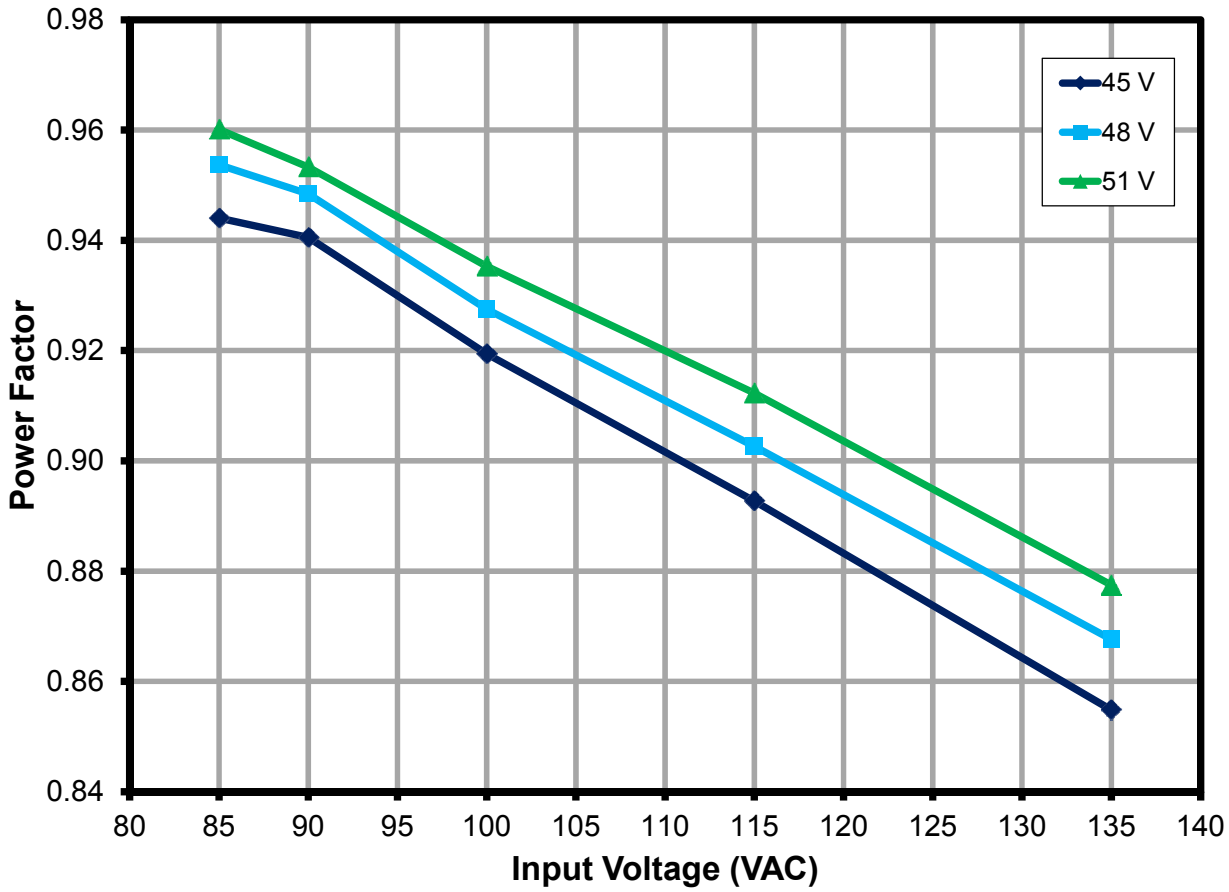

Figure 18 – High Power Factor within the Operating Range for 48 V, 60 mA Version.

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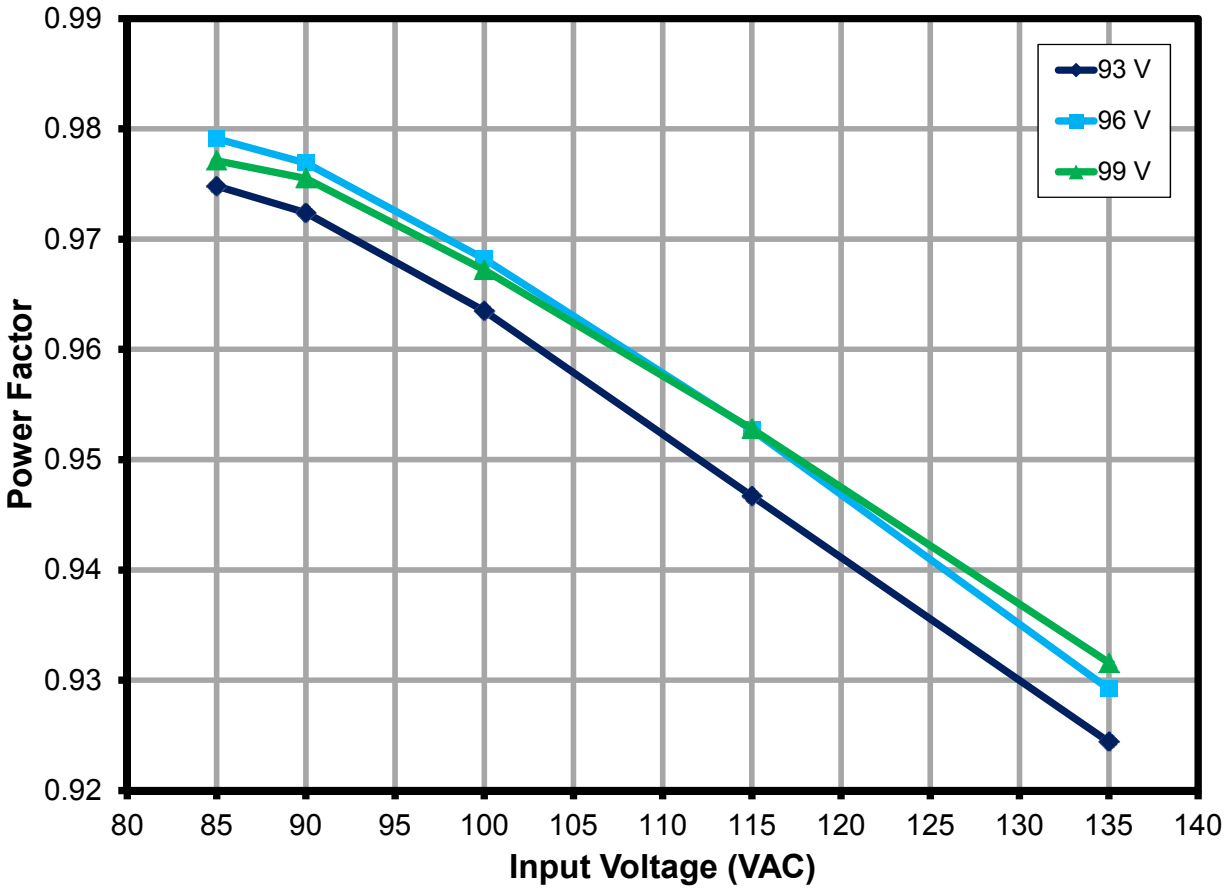

Figure 19 – High Power Factor within the Operating Range for 96 V Version.

9.4 %THD

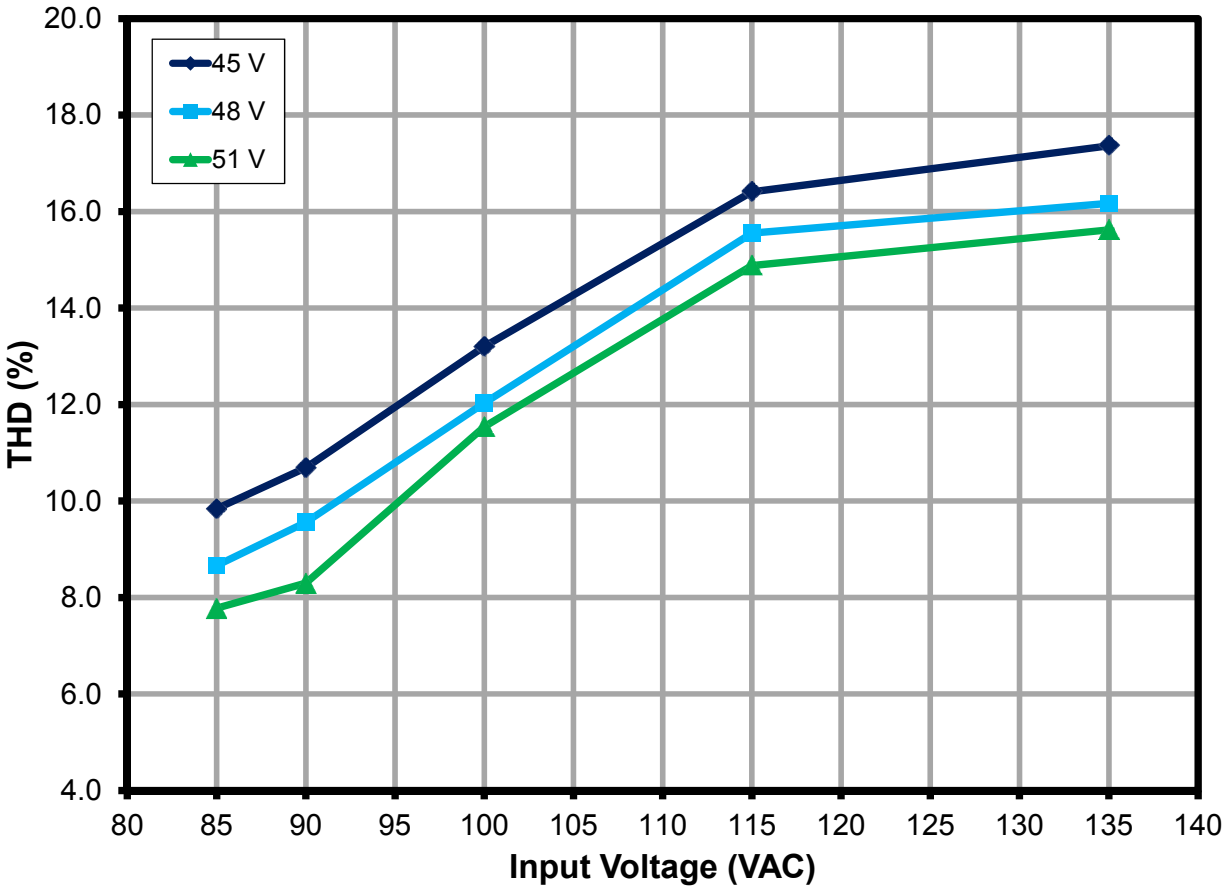

Figure 20 – Very Low %ATHD within the Operating Range for 48 V, 93 mA Version.

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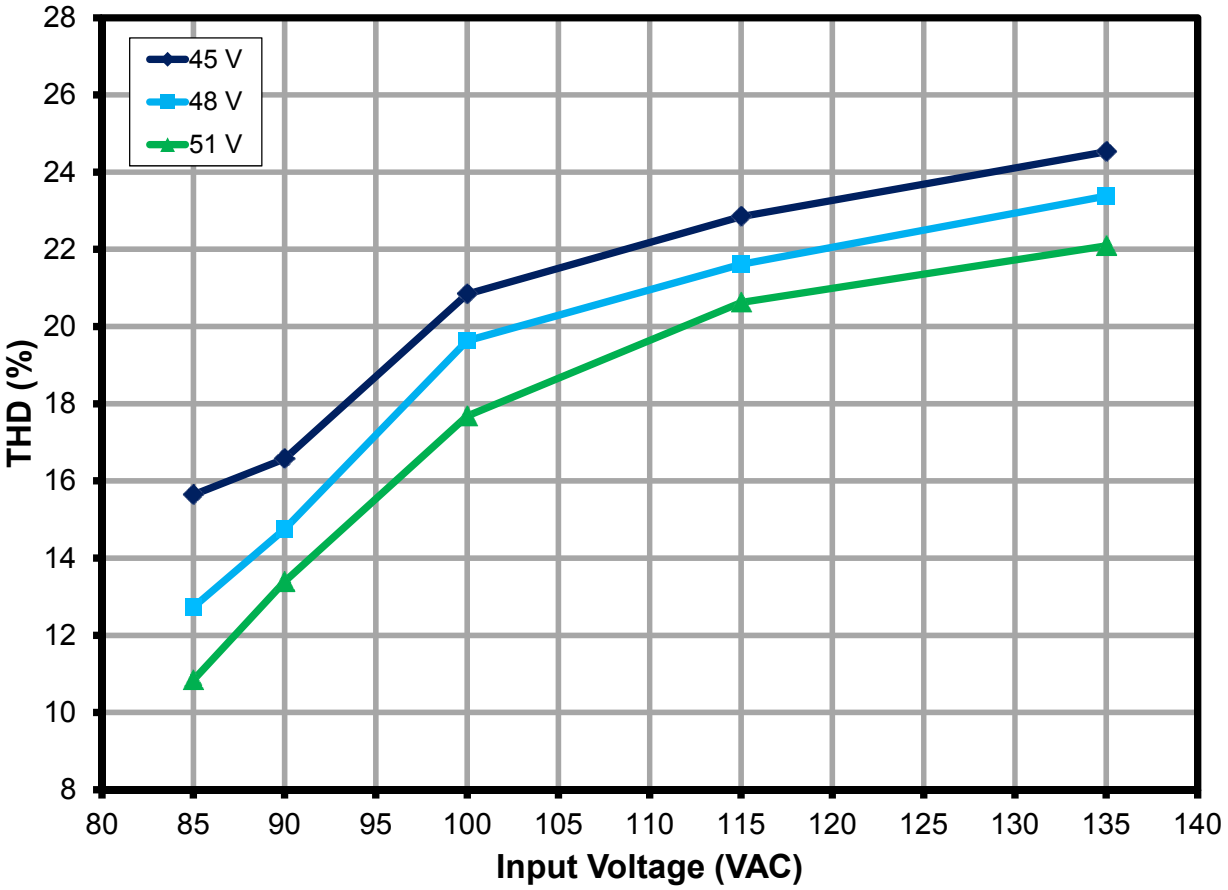

Figure 21 – Very Low %ATHD within the Operating Range for 48 V, 60 mA Version.

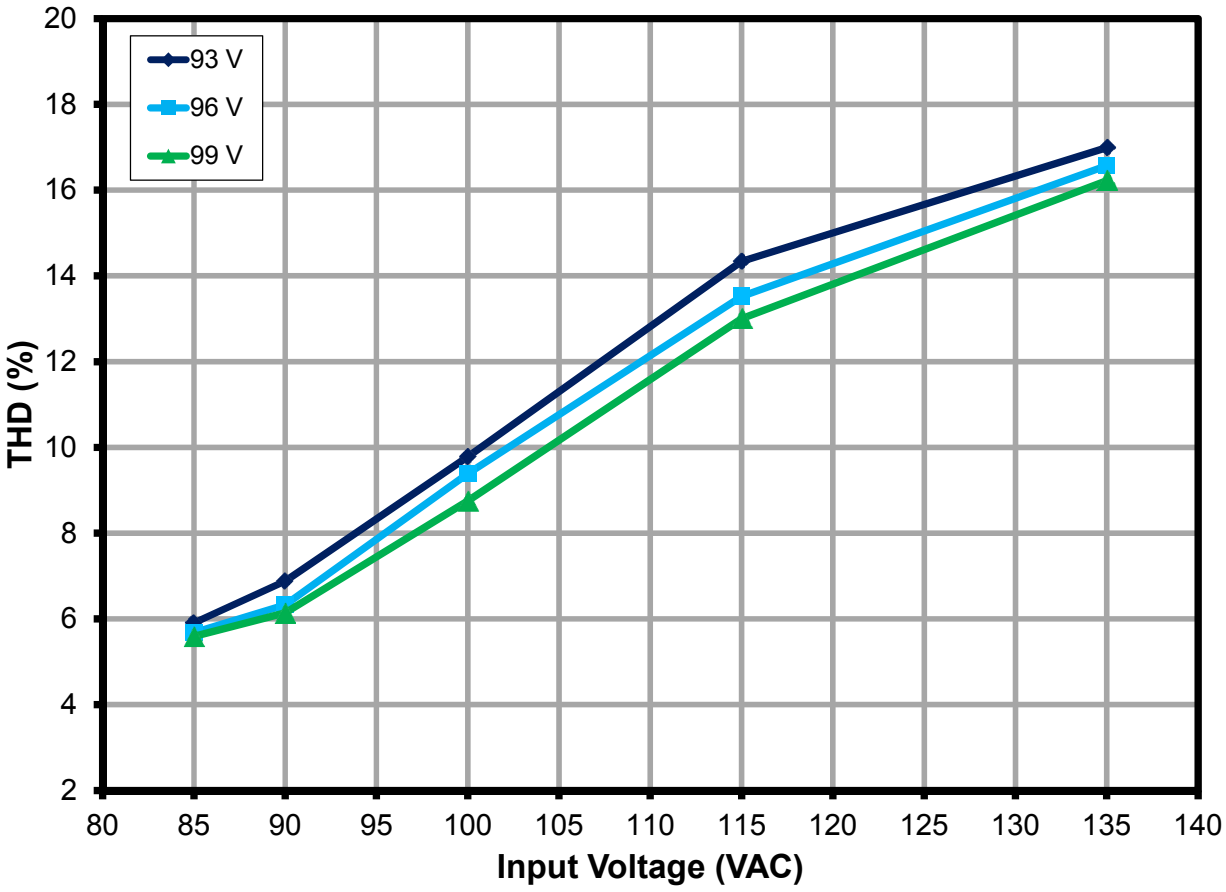

Figure 22 – Very Low %ATHD within the Operating Range for 96 V Version.

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9.5 Harmonic Measurements

9.5.1 48 V, 93 mA Version

V	Freq	I (mA)	P	PF
115	60.00	46.11	5.2537	0.9504
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Remarks**
1	44.16			
2	0.05	0.10%		
3	1.85	4.20%	35.7252	**Pass**
5	2.30	5.20%	19.9641	**Pass**
7	2.32	5.24%	10.5074	**Pass**
9	2.70	6.10%	5.2537	**Pass**
11	2.04	4.62%	3.6776	**Pass**
13	1.75	3.96%	3.1118	**Pass**
15	0.96	2.17%	2.6969	**Pass**
17	0.48	1.09%	2.3796	**Pass**
19	0.25	0.57%	2.1291	**Pass**
21	0.46	1.04%	1.9264	**Pass**
23	0.64	1.46%	1.7588	**Pass**
25	0.42	0.95%	1.6181	**Pass**
27	0.26	0.60%	1.4983	**Pass**
29	0.09	0.20%	1.3949	**Pass**
31	0.35	0.79%	1.3050	**Pass**
33	0.35	0.79%	1.2259	**Pass**
35	0.36	0.81%	1.1558	**Pass**
37	0.43	0.98%	1.0933	**Pass**
39	0.36	0.81%	1.0373	**Pass**

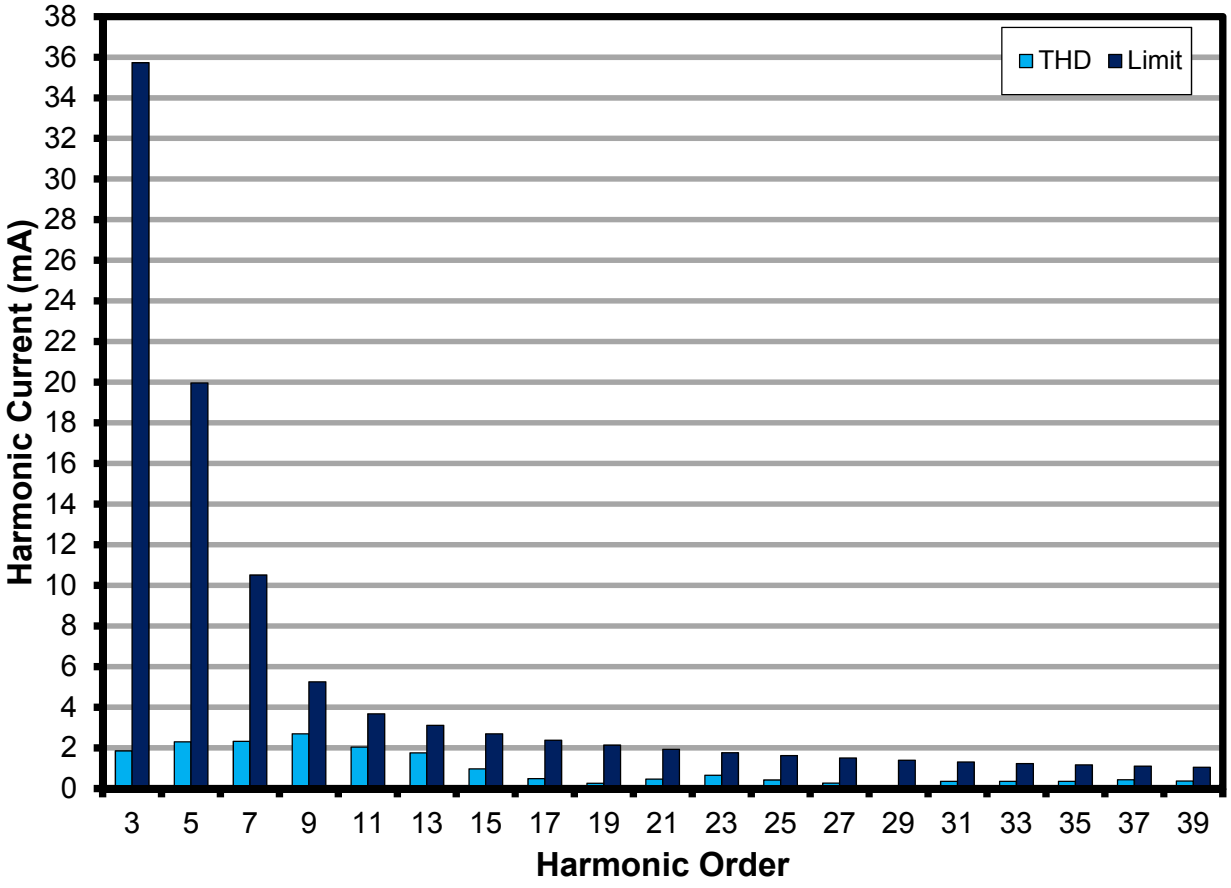

Figure 23 – Meets EN61000-3-2 Harmonics Contents Standards for <25 W Rating for 48 V, 93 mA version.

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9.5.2 48 V, 60 mA Version

V	Freq	I (mA)	P	PF
115	60.00	30.61	3.2615	0.8888
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Remarks**
1	28.46			
2	0.03	0.10%		
3	3.09	10.84%	22.1782	Pass
5	3.67	12.89%	12.3937	Pass
7	3.01	10.56%	6.5230	Pass
9	2.24	7.86%	3.2615	Pass
11	0.84	2.93%	2.2831	Pass
13	0.19	0.67%	1.9318	Pass
15	0.38	1.32%	1.6742	Pass
17	0.56	1.96%	1.4773	Pass
19	0.23	0.81%	1.3218	Pass
21	0.29	1.01%	1.1959	Pass
23	0.51	1.77%	1.0919	Pass
25	0.71	2.48%	1.0045	Pass
27	0.65	2.28%	0.9301	Pass
29	0.55	1.92%	0.8660	Pass
31	0.62	2.17%	0.8101	Pass
33	0.49	1.71%	0.7610	Pass
35	0.33	1.16%	0.7175	Pass
37	0.27	0.93%	0.6787	Pass
39	0.21	0.72%	0.6439	Pass

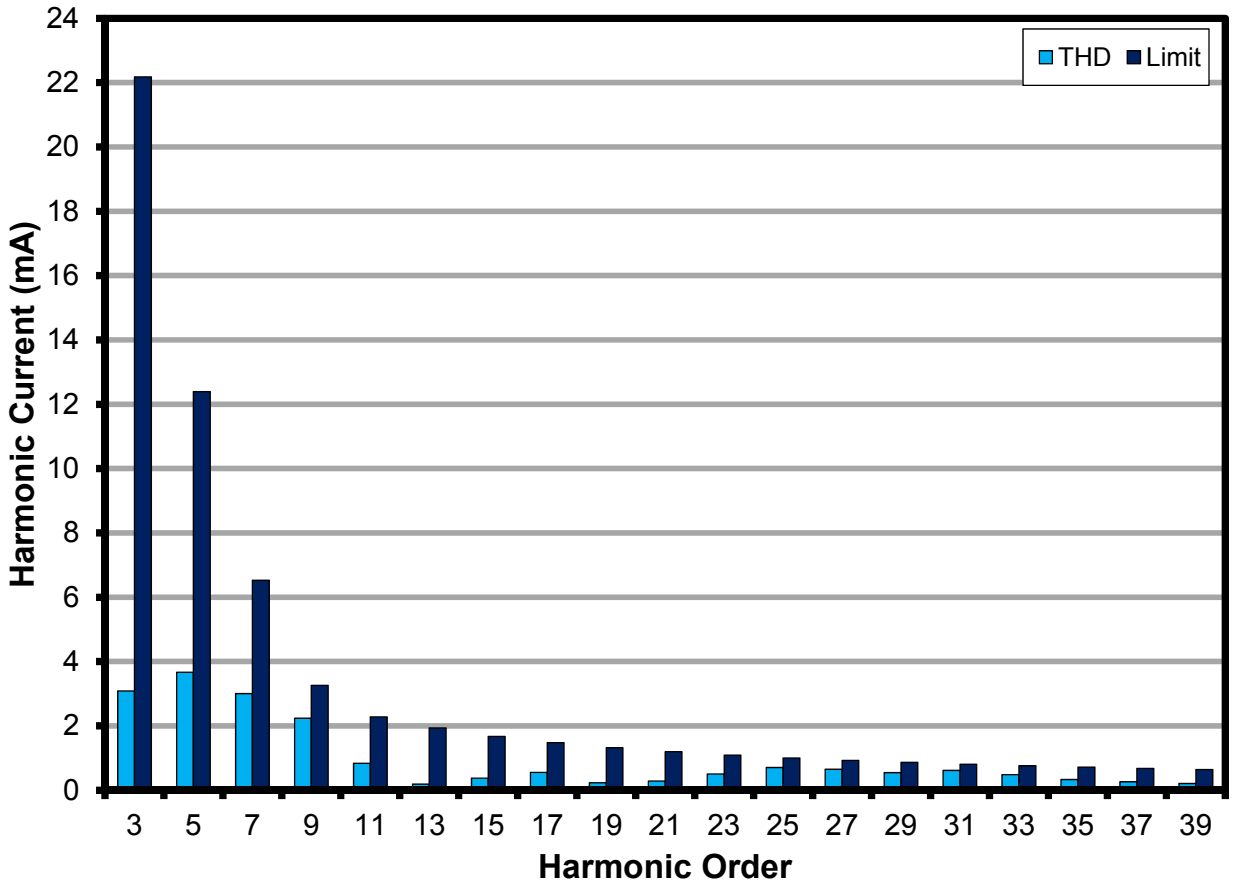

Figure 24 – Meets EN61000-3-2 Harmonics Contents Standards for <25 W Rating for 48 V, 60 mA version.

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9.5.3 96 V, 45 mA Version

V	Freq	I (mA)	P	PF
115	60.00	43.68	4.9460	0.9446
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Remarks**
1	42.07			
2	0.05	0.12%		
3	2.19	5.21%	33.6328	**Pass**
5	3.63	8.63%	18.7948	**Pass**
7	2.63	6.26%	9.8920	**Pass**
9	2.53	6.01%	4.9460	**Pass**
11	1.83	4.34%	3.4622	**Pass**
13	0.23	0.55%	2.9296	**Pass**
15	0.64	1.51%	2.5389	**Pass**
17	0.75	1.79%	2.2402	**Pass**
19	0.63	1.51%	2.0044	**Pass**
21	0.18	0.43%	1.8135	**Pass**
23	0.59	1.39%	1.6558	**Pass**
25	0.52	1.24%	1.5234	**Pass**
27	0.60	1.43%	1.4105	**Pass**
29	0.67	1.59%	1.3132	**Pass**
31	0.66	1.57%	1.2285	**Pass**
33	0.57	1.36%	1.1541	**Pass**
35	0.38	0.91%	1.0881	**Pass**
37	0.43	1.01%	1.0293	**Pass**
39	0.24	0.58%	0.9765	**Pass**

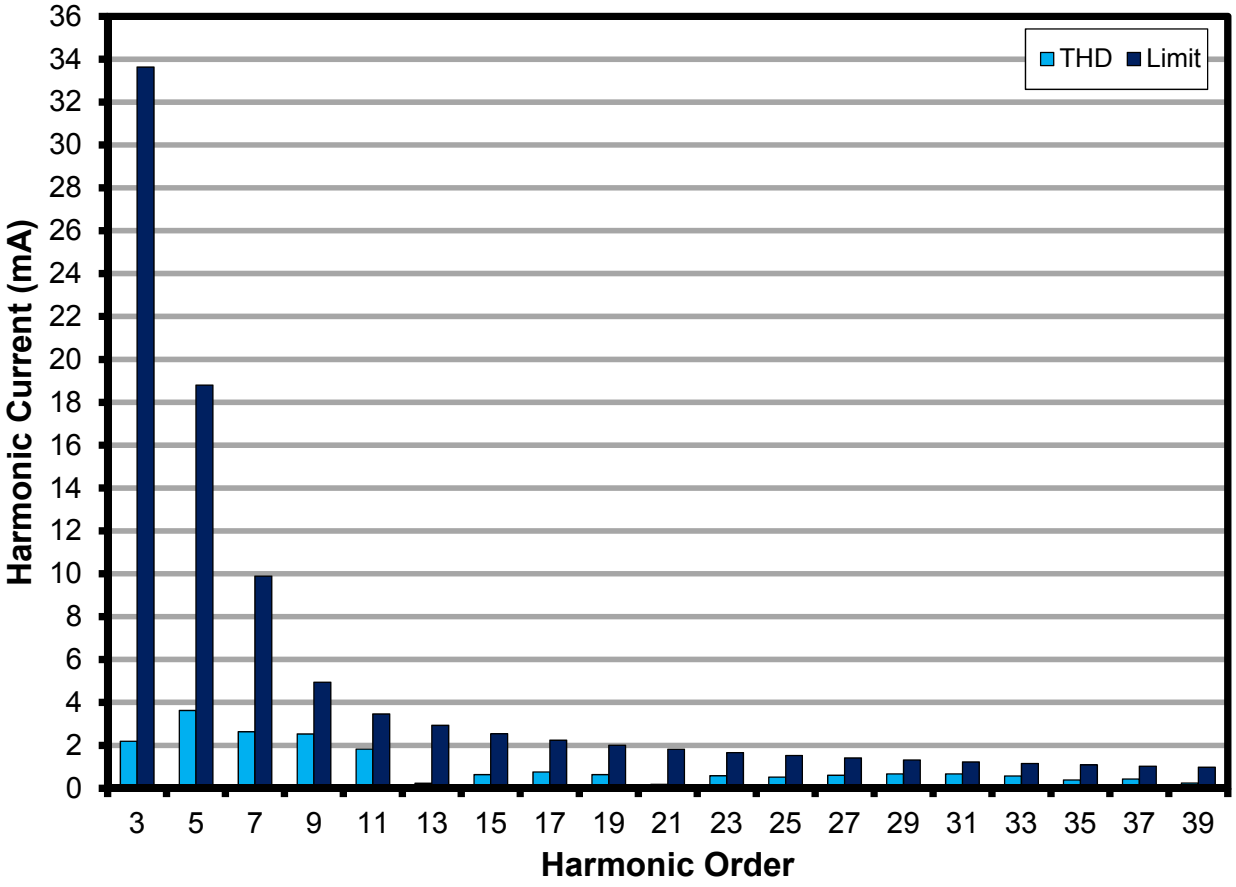

Figure 25 – Meets EN61000-3-2 Harmonics Contents Standards for <25 W Rating for 96 V, 45 mA Version.

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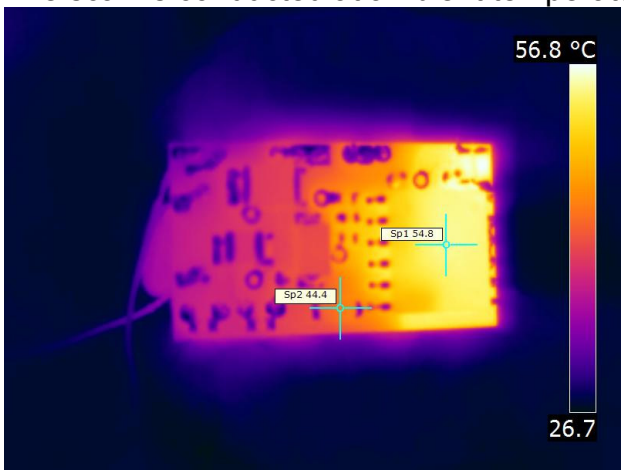
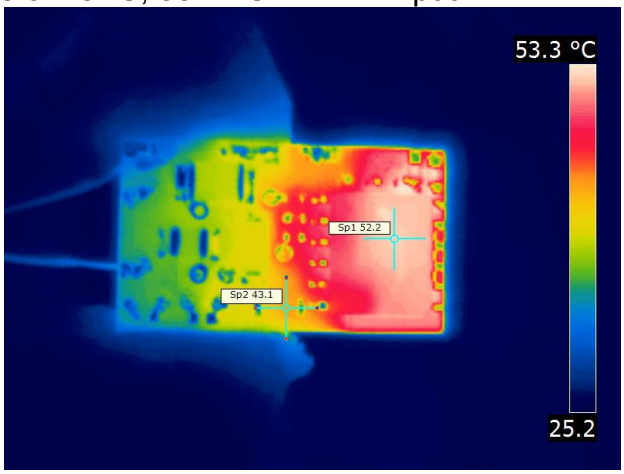
9.6 Thermal Scans

The scan is conducted at ambient temperature of 25 ºC, 85 VAC / 47 Hz input.



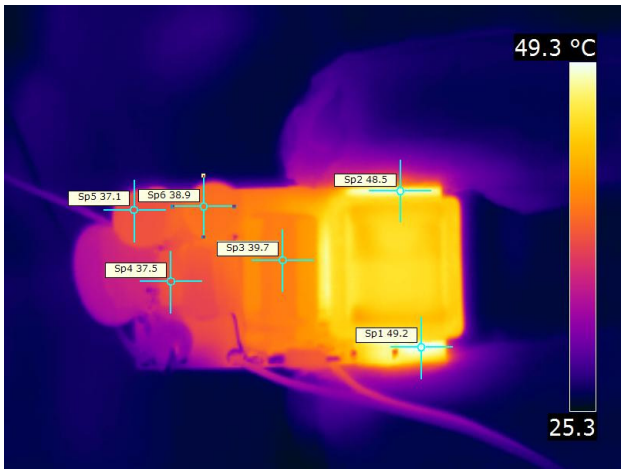
48 V Design Configuration

Figure 26 – U1 Case Temperature (Sp1).
D1 Case Temperature (Sp2).



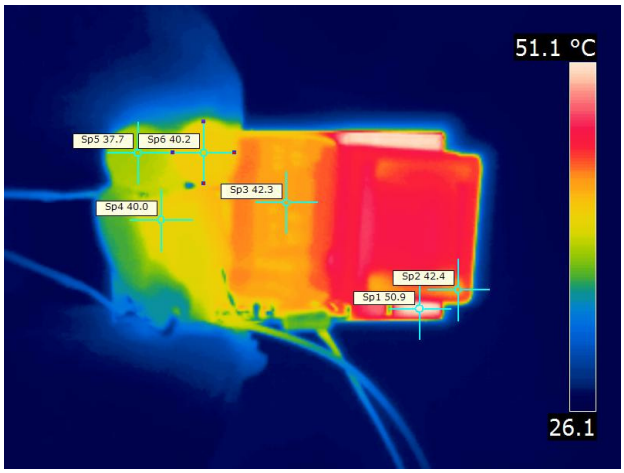
96 V Design Configuration

Figure 27 – U1 Case Temperature (Sp1).
D1 Case Temperature (Sp2).



48 V Design Configuration

Figure 28 – D2 Case Temperature (Sp1).
L3 Core Temperature (Sp2).
C7 Output Capacitor (Sp3).
BR1 Bridge Rectifier (Sp4).
L1 Differential Choke (Sp5).
L2 Differential Choke (Sp6).

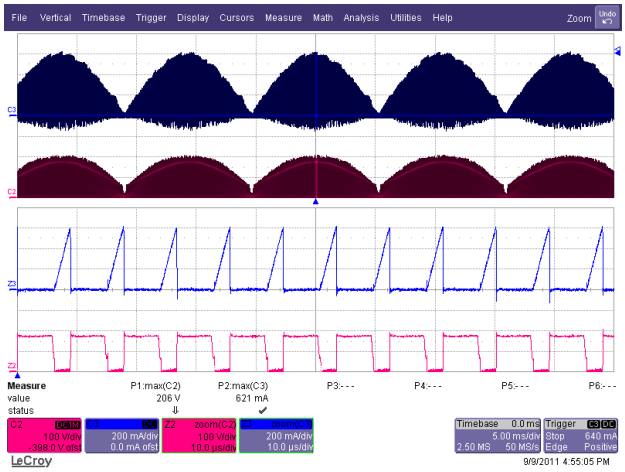


96 V Design Configuration

Figure 29 – D2 Case Temperature (Sp1).
L3 Core Temperature (Sp2).
C7 Output Capacitor (Sp3).
BR1 Bridge Rectifier (Sp4).
L1 Differential Choke (Sp5).
L2 Differential Choke (Sp6).

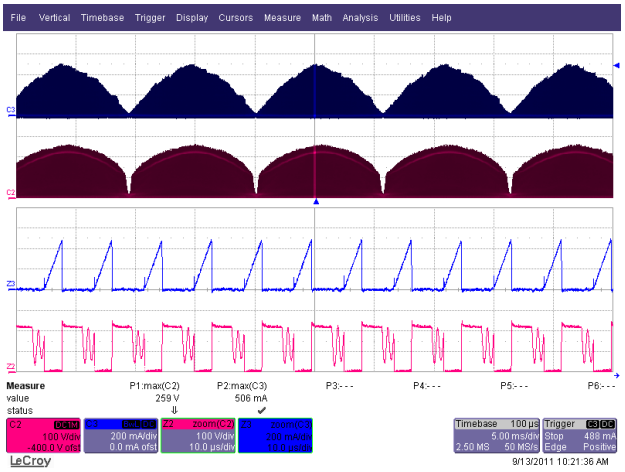
10 Waveforms

10.1 Drain Voltage and Current, Normal Operation



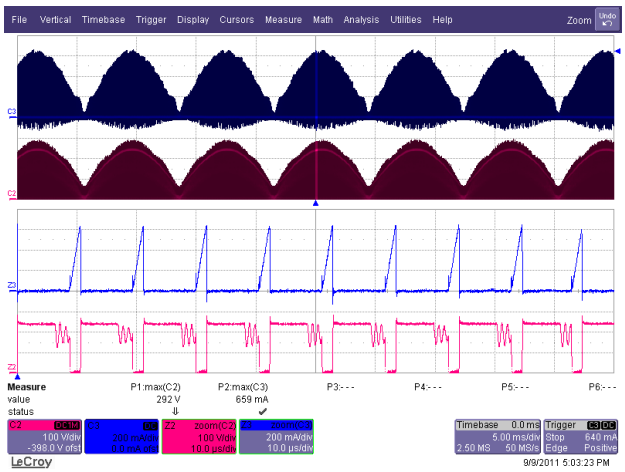
48 V Design Configuration

Figure 30 – 85 VAC / 47 Hz, 48 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 µs / div.



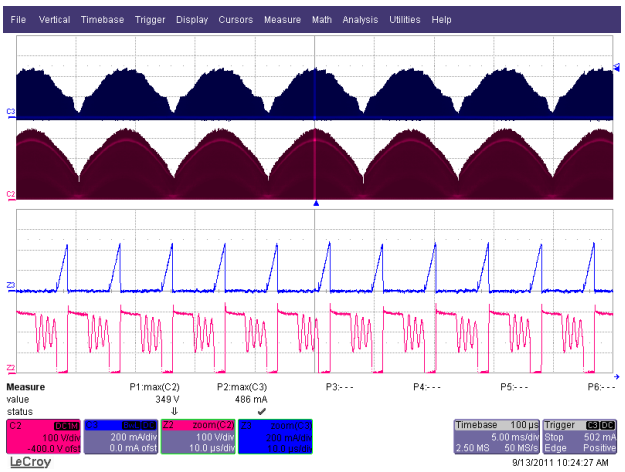
96 V Design Configuration

Figure 31 – 85 VAC / 47 Hz, 96 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale:5 ms / div.
Zoom Time Scale: 10 µs / div.



48 V Design Configuration

Figure 32 – 132 VAC / 63 Hz, 48 V LED String.
Ch2: V_{DRAIN}, 100 V / div..
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 µs / div.



96 V Design Configuration

Figure 33 – 132 VAC / 63 Hz, 96 V LED String.
Ch2: V_{DRAIN}, 100 V / div..
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 µs / div.

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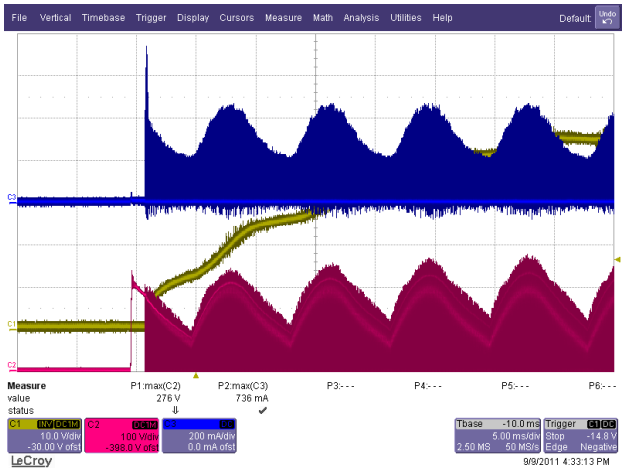
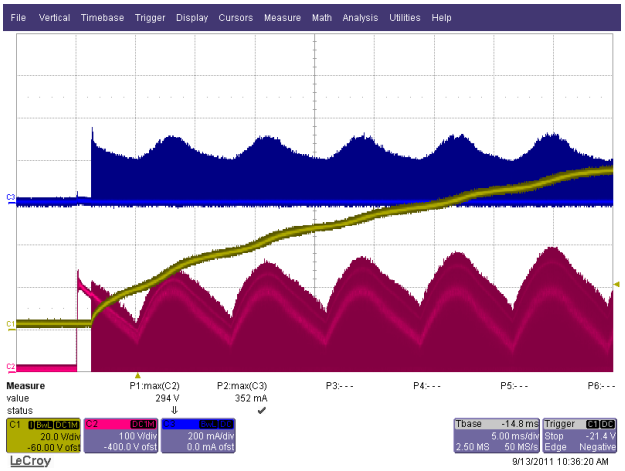
10.2 Drain Voltage and Current Start-up Profile



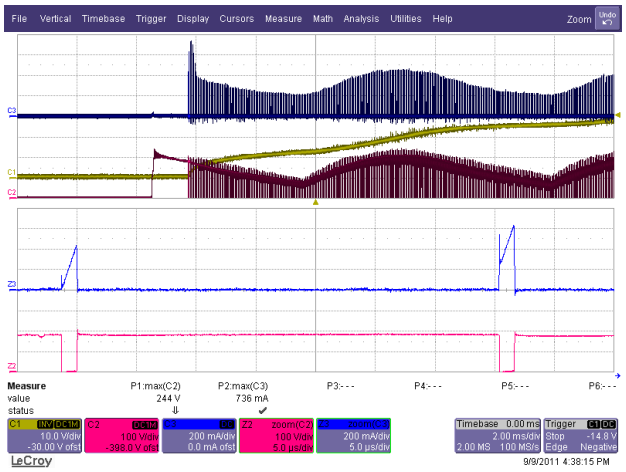
48 V Design Configuration

Figure 34 – 132 VAC / 60 Hz, 48 V LED String.
Ch1: V_{OUT}, 10 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div., 5 ms / div.



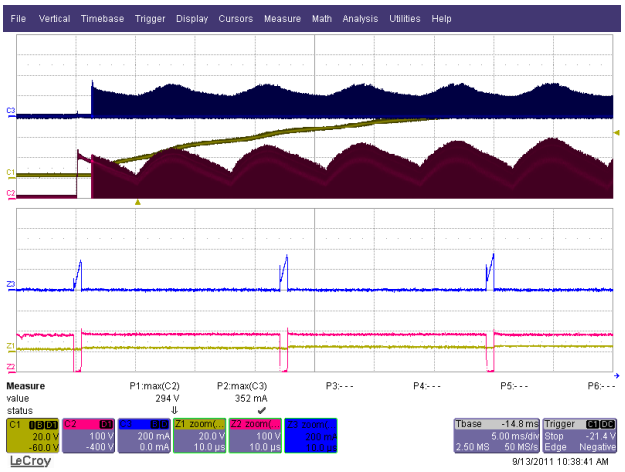
96 V Design Configuration

Figure 35 – 132 VAC / 60 Hz, 96 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div., 5 ms / div.



48 V Design Configuration

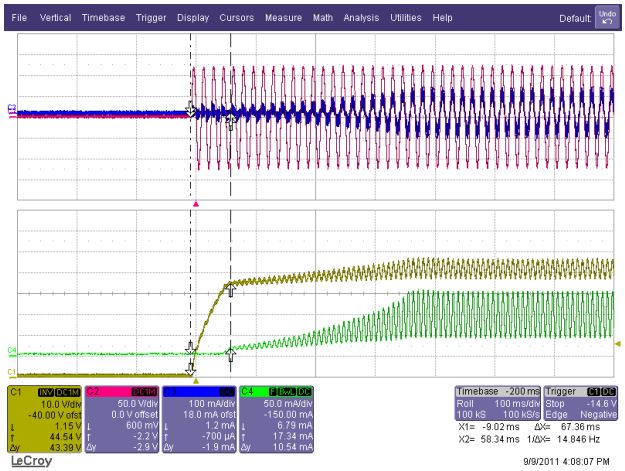
Figure 36 – 132 VAC / 60 Hz, 48 V LED String.
Ch1: V_{OUT}, 10 V / div.
Ch2, Z2: V_{DS}, 100 V / div.
Ch3, Z4: I_{DRAIN}, 200 mA / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 5 μs / div.



96 V Design Configuration

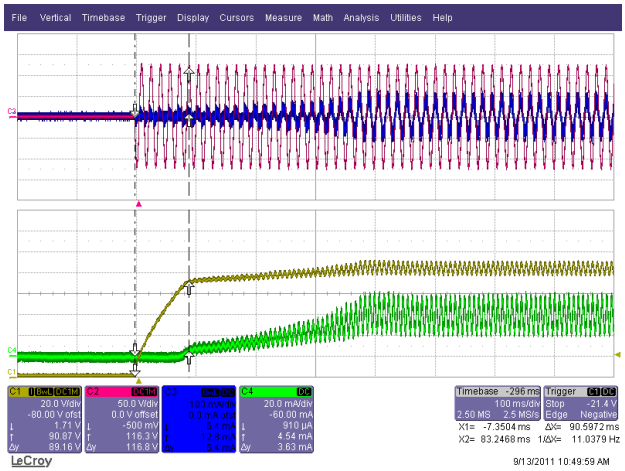
Figure 37 – 132 VAC / 60 Hz, 96 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2, Z2: V_{DS}, 100 V / div.
Ch3, Z4: I_{DRAIN}, 200 mA / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

10.3 Output Voltage Start-up Profile



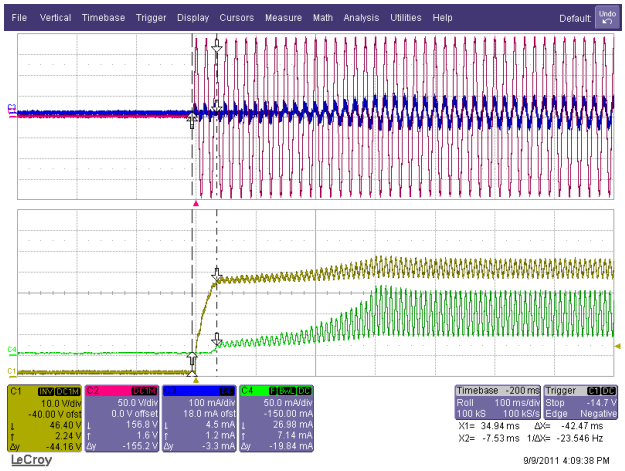
48 V Design Configuration

Figure 38 – 85 VAC / 60 Hz, 48 V LED
Ch1: V_{OUT}, 10 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.



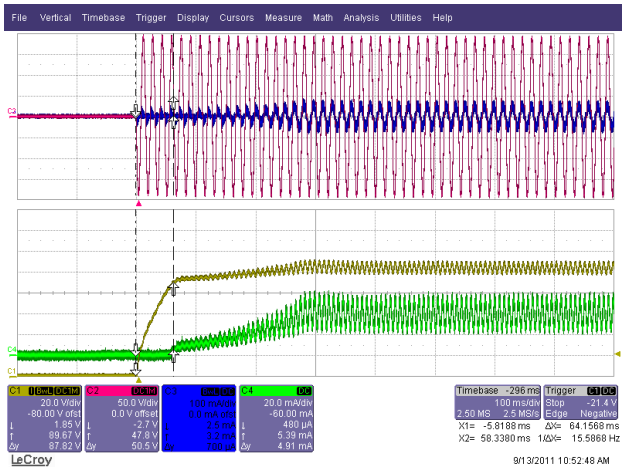
96 V Design Configuration

Figure 39 – 85 VAC / 60 Hz, 96 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.



48 V Design Configuration

Figure 40 – 132 VAC / 63 Hz, 48 V LED String.
Ch1: V_{OUT}, 10 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.



96 V Design Configuration

Figure 41 – 132 VAC / 63 Hz, 96 V LED String.
Ch1: V_{IN}, 20 V / div.
Ch2: V_{OUT}, 50 V / div.
Ch3: I_{IN}, 100 m A / div.
Ch4: I_{OUT}, 20 mA / div., 100 ms / div.

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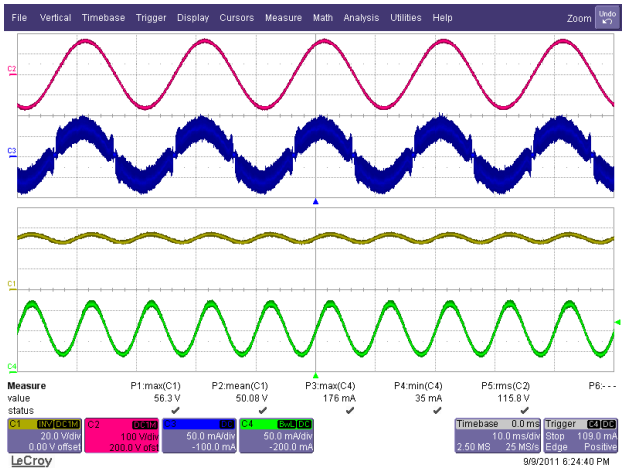
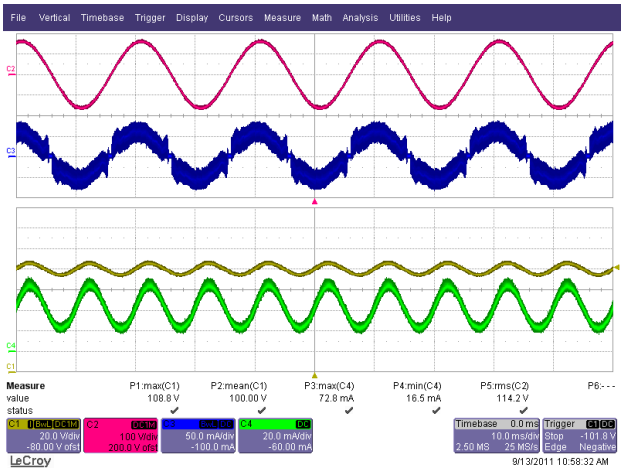
10.4 Input and Output Voltage and Current Profiles



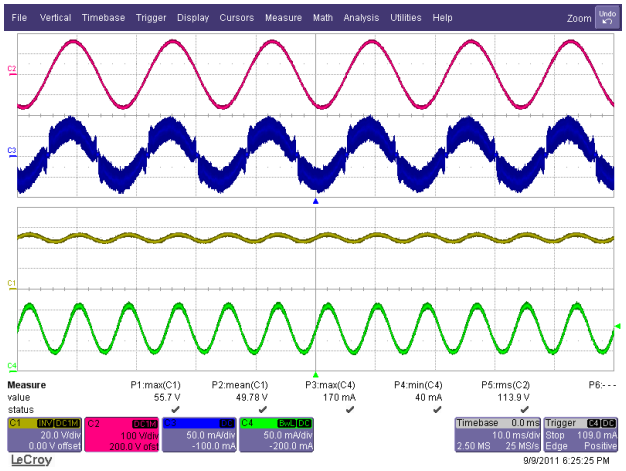
48 V Design Configuration

Figure 42 – 115 VAC / 50 Hz, 48 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 100 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 50 mA / div., 10 ms / div.



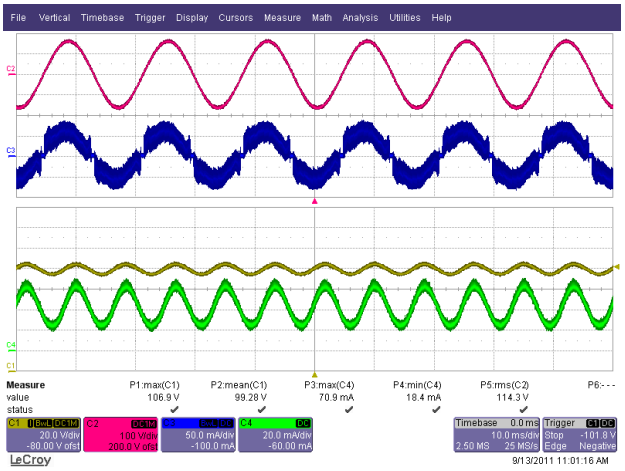
96 V Design Configuration

Figure 43 – 115 VAC / 50 Hz, 96 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 100 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 20 mA / div., 10 ms / div.



48 V Design Configuration

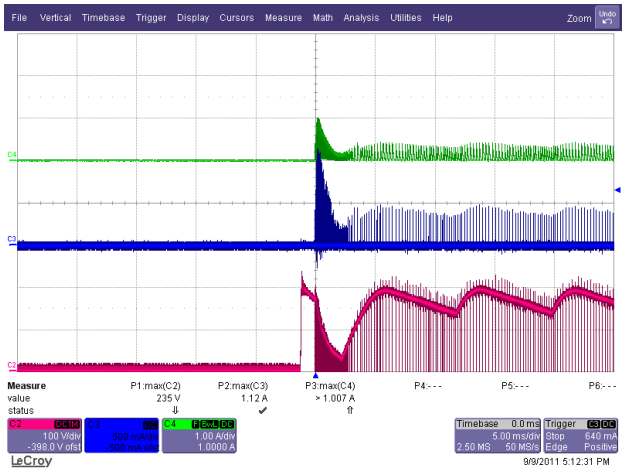
Figure 44 – 115 VAC / 60 Hz, 48 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 100 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 50 mA / div., 10 ms / div



96 V Design Configuration

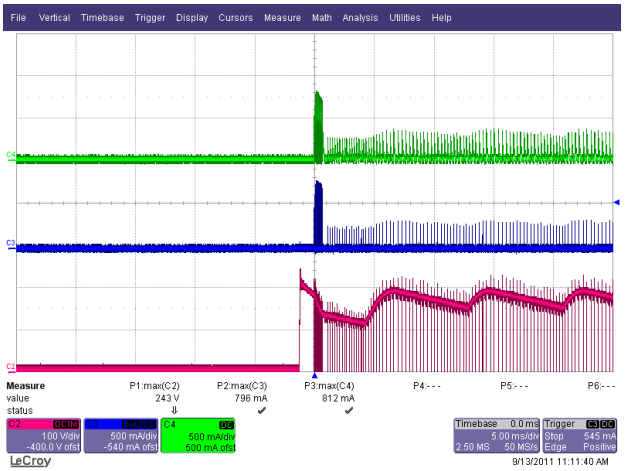
Figure 45 – 132 VAC / 63 Hz, 96 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch2: V_{OUT}, 10 V / div.
Ch3: I_{IN}, 50 m A / div.
Ch4: I_{OUT}, 50 mA / div., 50 ms / div.

10.5 Drain Voltage and Current Profile with Output Shorted



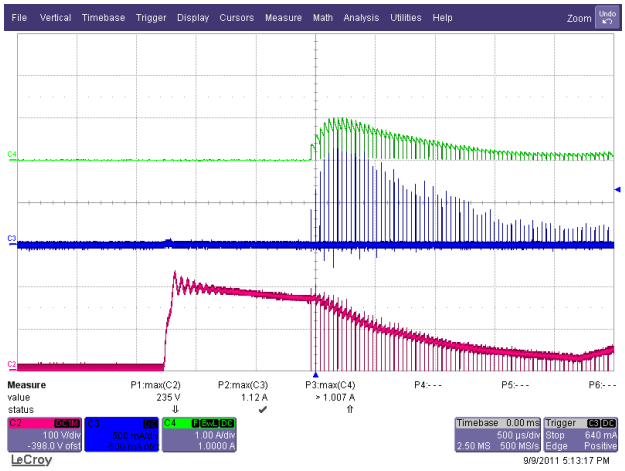
48 V Design Configuration

Figure 46 – 132 VAC / 63 Hz, Output Shorted.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{SOURCE} , 1 A / div., 5 ms / div.



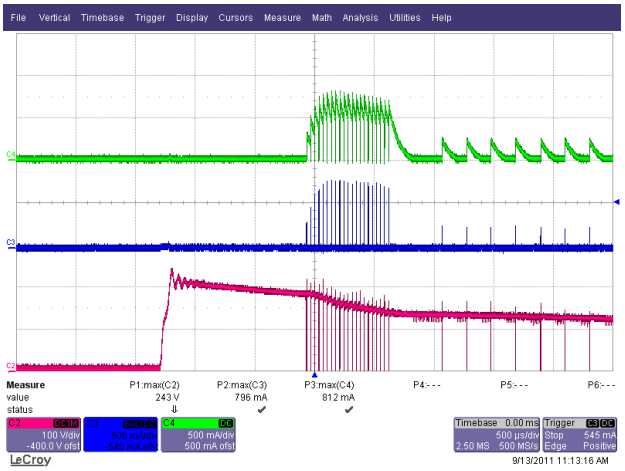
96 V Design Configuration

Figure 47 – 132 VAC / 63 Hz, Output Shorted.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{SOURCE} , 0.5 A / div., 5 ms / div.



48 V Design Configuration

Figure 48 – 132 VAC / 63 Hz, Output Shorted.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{SOURCE} , 1 A / div., 500 µs / div.



96 V Design Configuration

Figure 49 – 132 VAC / 63 Hz, Output Shorted.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{SOURCE} , 0.5 A / div., 500 µs / div.

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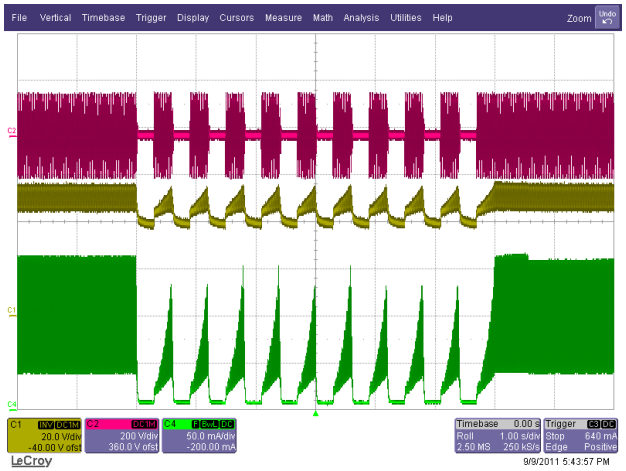
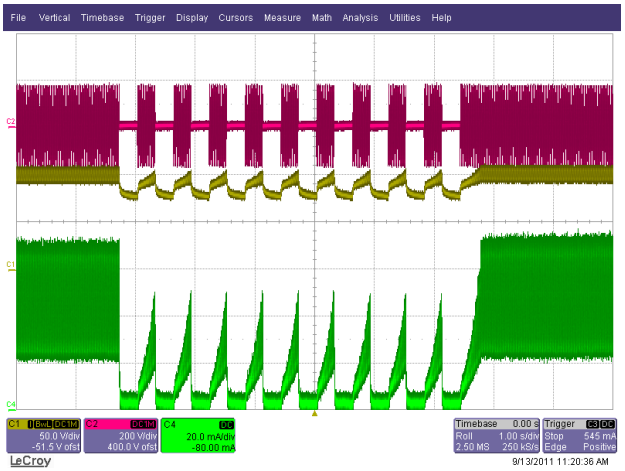
10.6 Line Transient Response



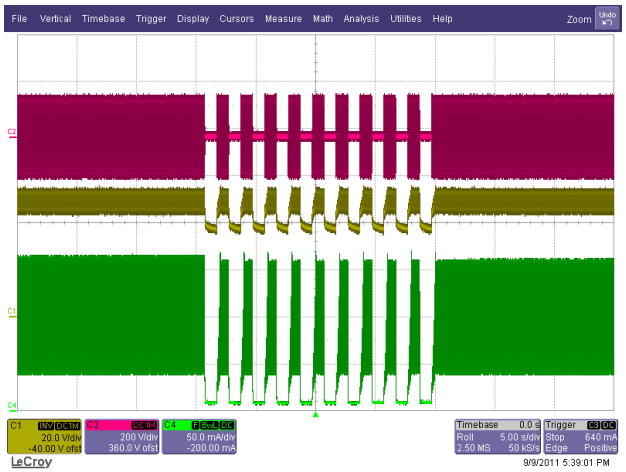
48 V Design Configuration

Figure 50 – 115 VAC / 50 Hz,
300 ms On – 300 ms Off.
Load: 48 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 200 V / div.
Ch4: I_{OUT}, 50 mA / div., 1 s / div.



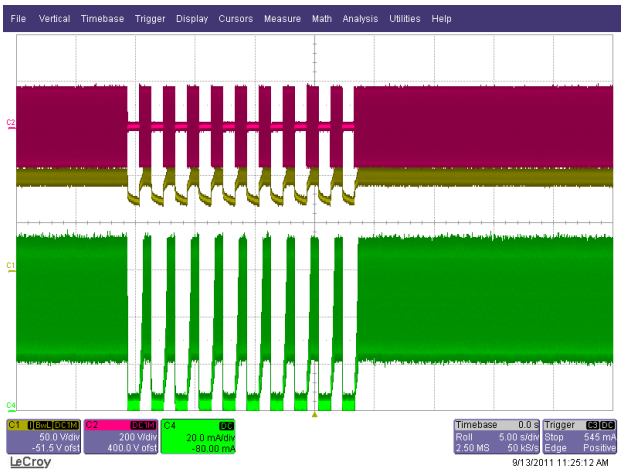
96 V Design Configuration

Figure 51 – 115 VAC / 50 Hz,
300 ms On – 300 ms Off.
Load: 96 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{IN}, 200 V / div.
Ch4: I_{OUT}, 20 mA / div., 1 s / div.



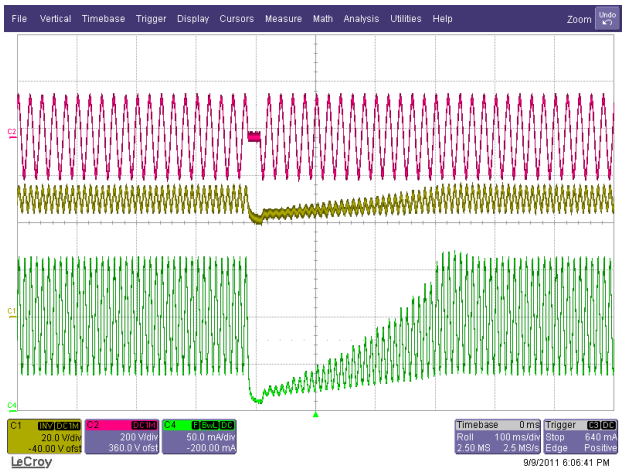
48 V Design Configuration

Figure 52 – 115 VAC / 50 Hz,
1 s On – 1 s Off.
Load: 48 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 200 V / div.
Ch4: I_{OUT}, 50 mA / div., 5 s / div.



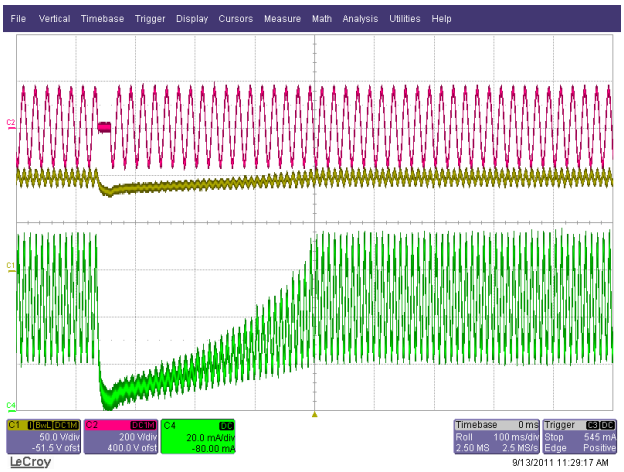
96 V Design Configuration

Figure 53 – 115 VAC / 50 Hz,
1 s On – 1 s Off.
Load: 96 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{IN}, 200 V / div.
Ch4: I_{OUT}, 20 mA / div., 5 s / div.



48 V Design Configuration

Figure 54 – 115 VAC / 50 Hz, 1 Cycle Drop-out.
Load: 48 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 200 V / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.



96 V Design Configuration

Figure 55 – 115 VAC / 50 Hz, 1 Cycle Drop-out.
Load: 96 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{IN}, 200 V / div.
Ch4: I_{OUT}, 20 mA / div., 100 ms / div.

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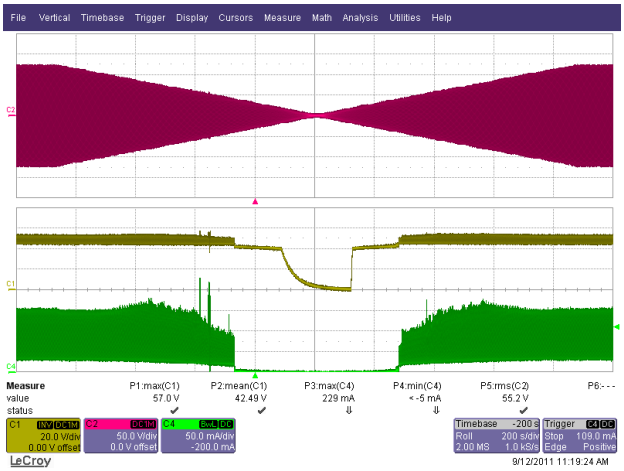
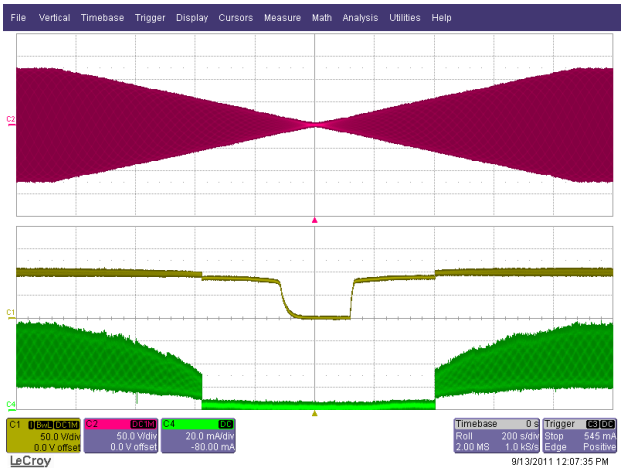
10.7 Brown-out

Input voltage slew rate of 0.1 V / s from 85-0-85 VAC / 50 Hz line input variation; no failure observed.



48 V Design Configuration

Figure 56 – 85 VAC / 50 Hz, 48 V LED String.
Below 50 VAC the peak current of the load is higher than normal steady current but the average current is regulated.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 50 V / div.
Ch4: I_{OUT}, 50 mA / div., 200 s / div.

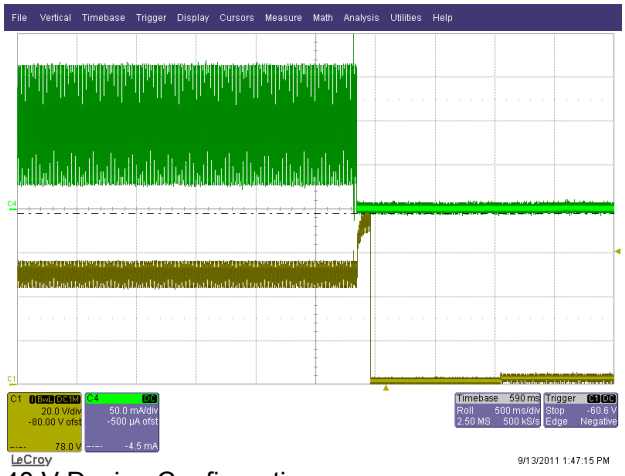


96 V Design Configuration

Figure 57 – 85 VAC / 50 Hz, 96 V LED String.
Ch1: V_{OUT}, 20 V / div.
Ch2: V_{IN}, 50 V / div.
Ch4: I_{OUT}, 50 mA / div., 200 s / div.

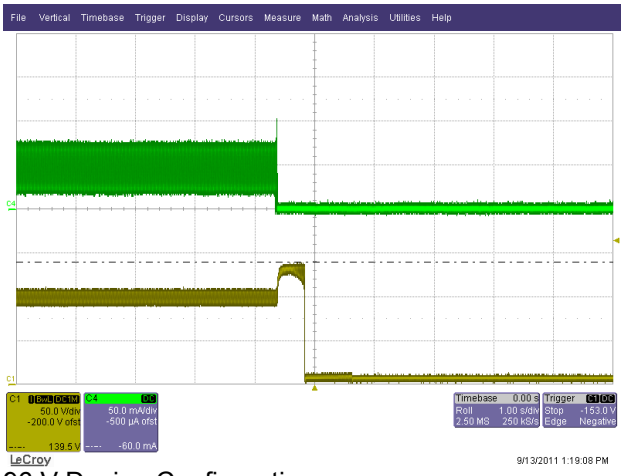
10.8 Start-up No-load

This LED driver is protected by VR1 in case of no-load condition occurs in order to avoid leakage from the output capacitor. This protection is not auto-recovering; replace VR1 in case this condition occurs.



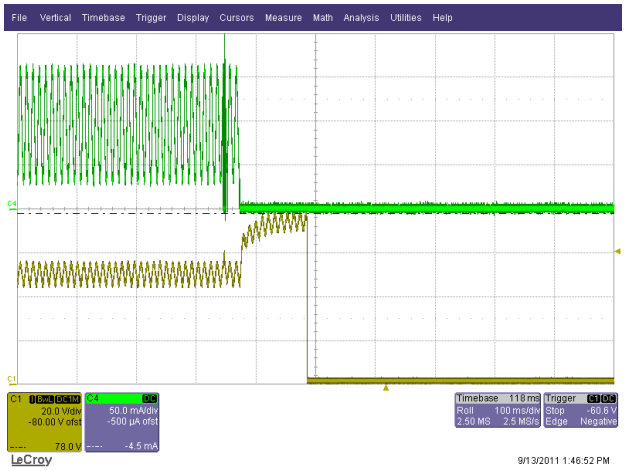
48 V Design Configuration

Figure 58 – 85 VAC / 63 Hz, Start-up No-load.
Ch1: V_{OUT}, 20 V / div.
Ch4: I_{OUT}, 50 mA / div., 0.5 s / div.



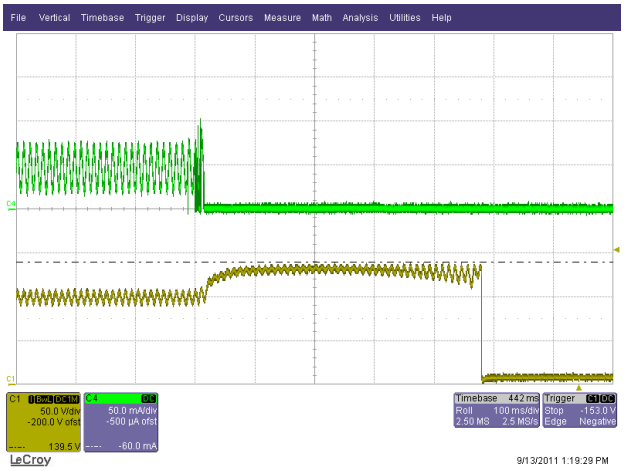
96 V Design Configuration

Figure 59 – 85 VAC / 63 Hz, Start-up No-load.
Ch1: V_{OUT}, 50 V / div.
Ch4: I_{OUT}, 50 mA / div., 1s / div.



48 V Design Configuration

Figure 60 – 855 VAC / 63 Hz, Start-up No-load.
Ch1: V_{OUT}, 20 V / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.



96 V Design Configuration

Figure 61 – 85 VAC / 63 Hz, Start-up No-load.
Ch1: V_{OUT}, 50 V / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div..

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10.9 Line Surge Waveform

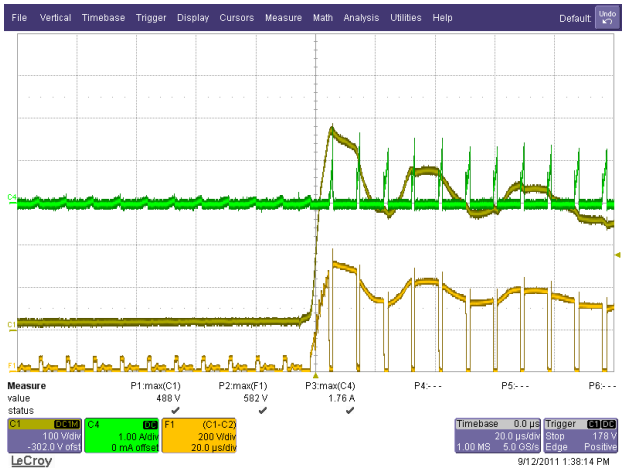

Figure 62 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=582 V_{PK}
(+)2.5 kV Differential Ring Surge at 0º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 20 µs / div.

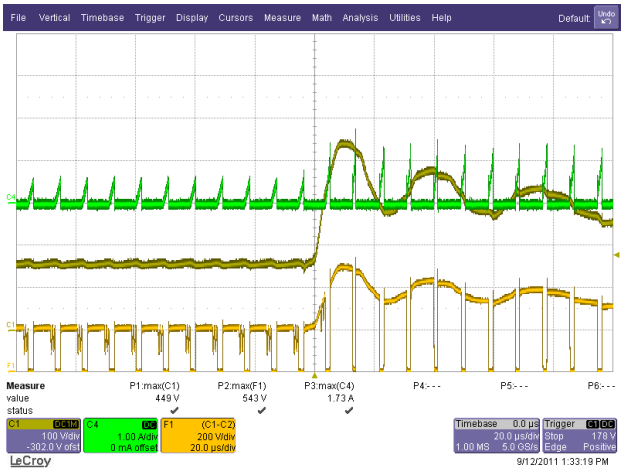

Figure 63 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=543 V_{PK}
(+)2.5 kV Differential Ring Surge at 90º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 20 µs / div.

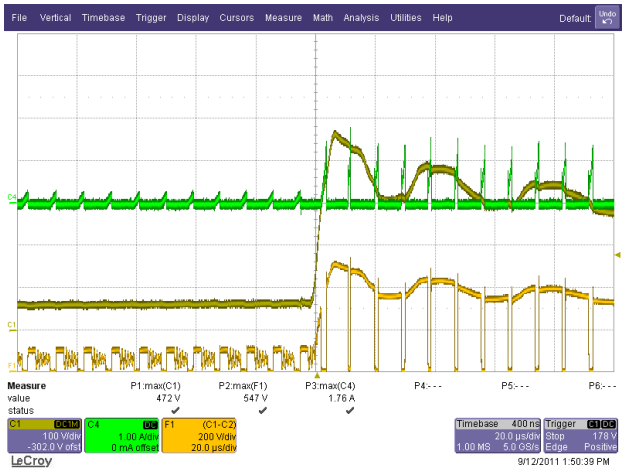

Figure 64 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=547 V_{PK}
(-)2.5 kV Differential Ring Surge at 0º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 20 µs / div.

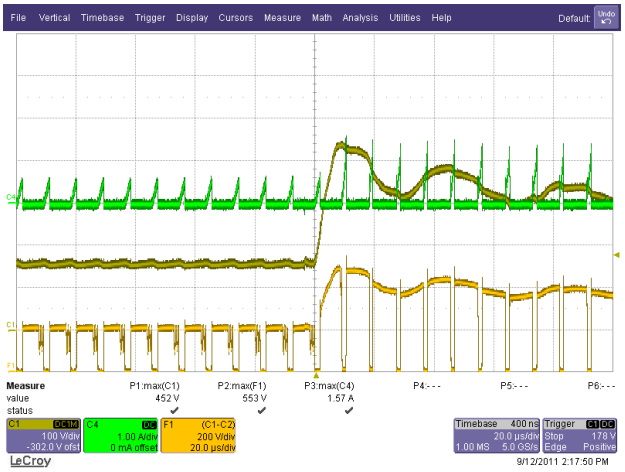

Figure 65 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=553 V_{PK}
(-)2.5 kV Differential Ring Surge at 90º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 20 µs / div.

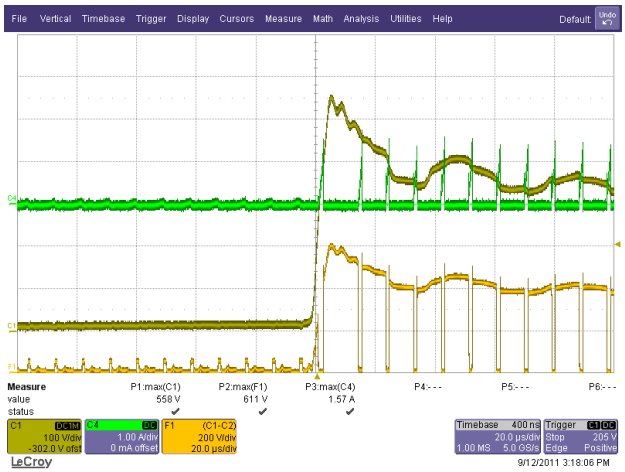

Figure 66 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=611 V_{PK}
(+)1 kV Differential Surge at 0º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 20 µs / div.

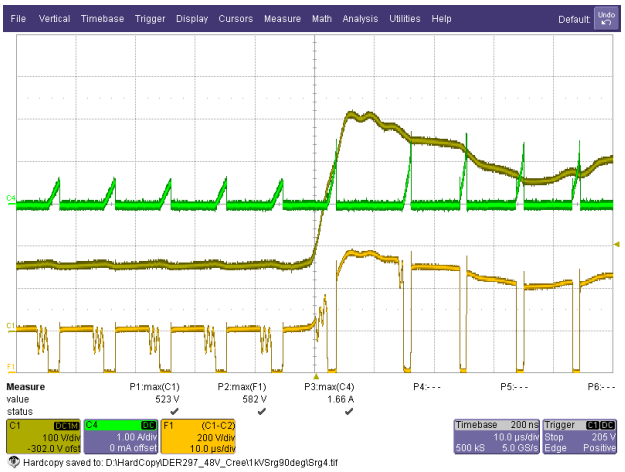

Figure 67 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=582 V_{PK}
(+)1kV Differential Surge at 90º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 10 µs / div.

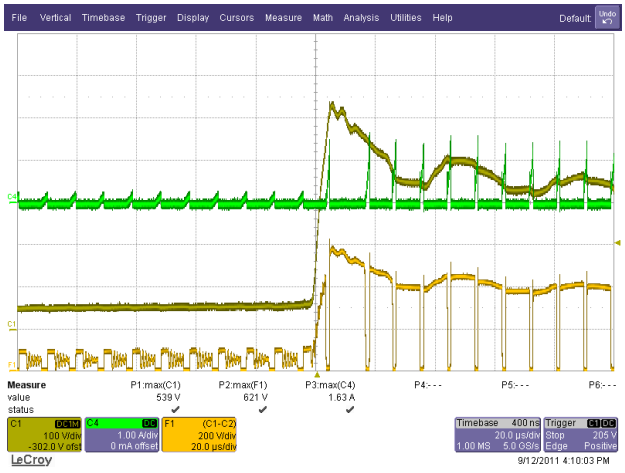

Figure 68 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=621 V_{PK}
(-)1 kV Differential Surge at 0º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 20 µs / div.

Figure 69 – 115 VAC / 60 Hz, 48 V Load,
V_{DS}=608 V_{PK}
(-)1 kV Differential Surge at 90º.
Ch1: V_{IN}, 100 V / div.
Ch4: I_{DRAIN}, 1 A / div.
F1: V_{DS}, 200 V / div., 20 µs / div.

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11 Line Surge

Input voltage was set at 115 VAC / 60 Hz. Output was loaded with 48 V LED string and operation was verified following each surge event.

Differential input line 1.2 / 50 μs surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	115	L to N	0	Pass
-1000	115	L to N	0	Pass
+1000	115	L to N	90	Pass
-1000	115	L to N	90	Pass

Differential input line ring surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	115	L to N	0	Pass
-2500	115	L to N	0	Pass
+2500	115	L to N	90	Pass
-2500	115	L to N	90	Pass

Unit passes under all test conditions.

12 Conducted EMI

12.1 Equipment:

Receiver:

Rohde & Schwartz
ESPI - Test Receiver (9 kHz – 3 GHz)
Model No: ESPI3

LISN:

Rohde & Schwartz
Two-Line-V-Network
Model No: ENV216

12.2 EMI Test Set-up

LED driver is placed in a conical metal housing (for self-ballasted lamps; CISPR15 Edition 7.2).

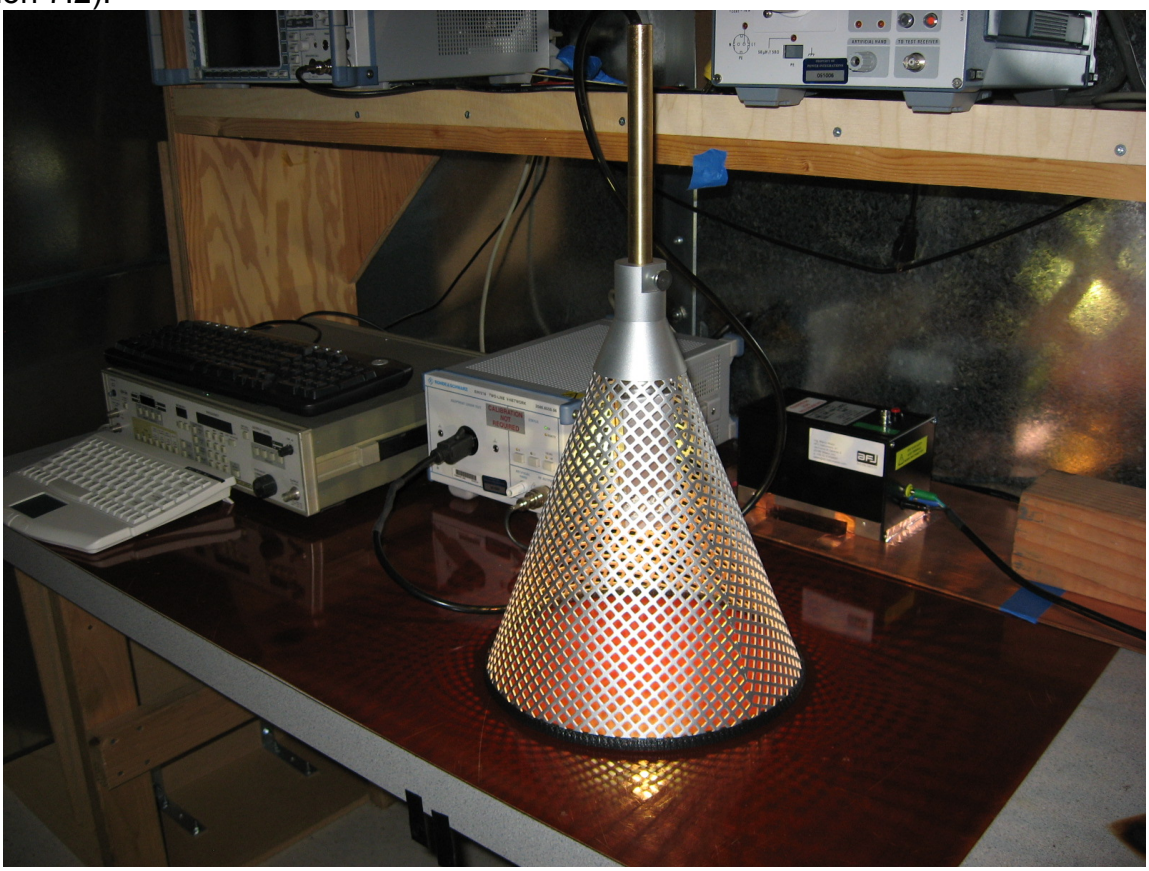

Figure 70 – Conducted Emissions Measurement Set-up
Showing Conical Ground Plane Inside which UUT was Mounted.

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12.3 EMI Test Result

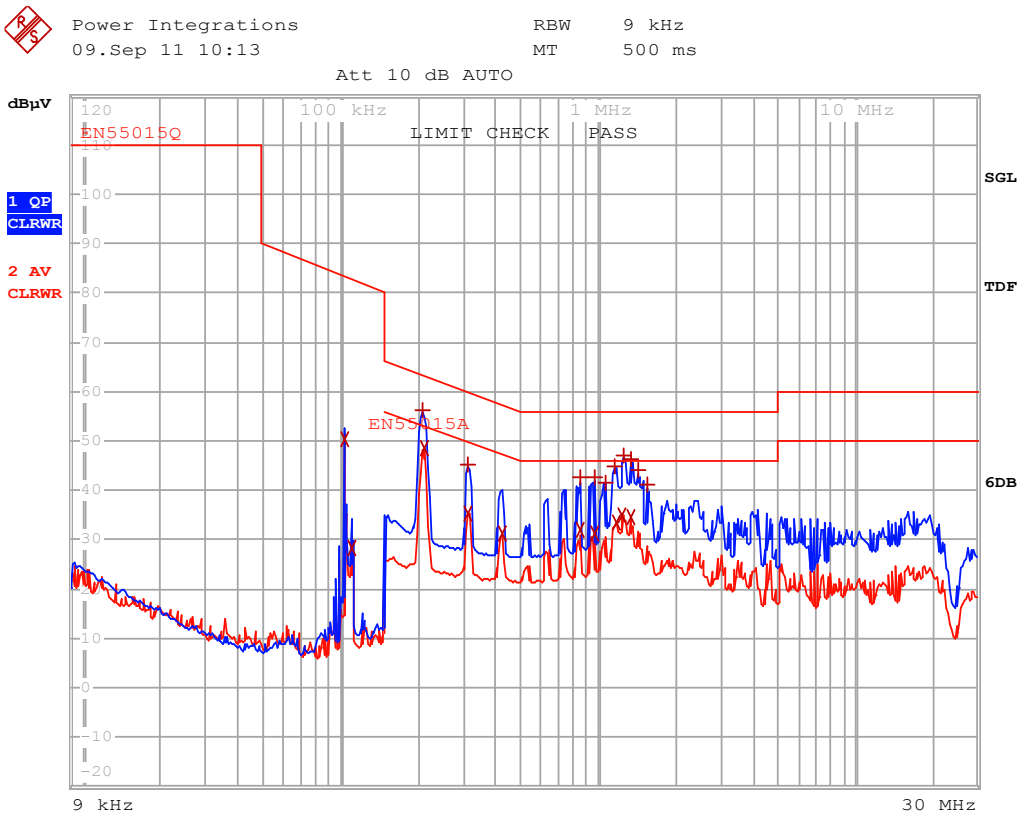

Figure 71 – Conducted EMI, 48 V / 93 mA Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV			DELTA LIMIT dB
2	Average	104.063986756 kHz	50.25	L1	gnd	
2	Average	110.466018893 kHz	28.22	L1	gnd	
1	Quasi Peak	206.24110178 kHz	56.10	L1	gnd	-7.24
2	Average	210.386547925 kHz	48.63	L1	gnd	-4.55
1	Quasi Peak	310.135545783 kHz	45.19	N	gnd	-14.77
2	Average	313.236901241 kHz	35.44	N	gnd	-14.44
2	Average	426.417977756 kHz	31.29	N	gnd	-16.03
1	Quasi Peak	855.719977385 kHz	42.75	N	gnd	-13.24
2	Average	855.719977385 kHz	31.90	N	gnd	-14.09
1	Quasi Peak	964.246689302 kHz	42.80	N	gnd	-13.20
2	Average	964.246689302 kHz	31.24	N	gnd	-14.75
1	Quasi Peak	1.07577950963 MHz	41.61	N	gnd	-14.38
1	Quasi Peak	1.16491505578 MHz	45.03	N	gnd	-10.96
2	Average	1.17656420634 MHz	33.56	N	gnd	-12.43
2	Average	1.23658080545 MHz	35.11	N	gnd	-10.88
1	Quasi Peak	1.2489466135 MHz	47.03	N	gnd	-8.96
1	Quasi Peak	1.33903981723 MHz	46.48	N	gnd	-9.51
2	Average	1.33903981723 MHz	34.42	N	gnd	-11.57
1	Quasi Peak	1.43563192593 MHz	44.07	N	gnd	-11.92
1	Quasi Peak	1.53919174041 MHz	41.15	N	gnd	-14.84

Figure 72 – Conducted EMI, 48 V / 93 mA Steady-State Load Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits. Line and Neutral Scan Design Margin Measurement.

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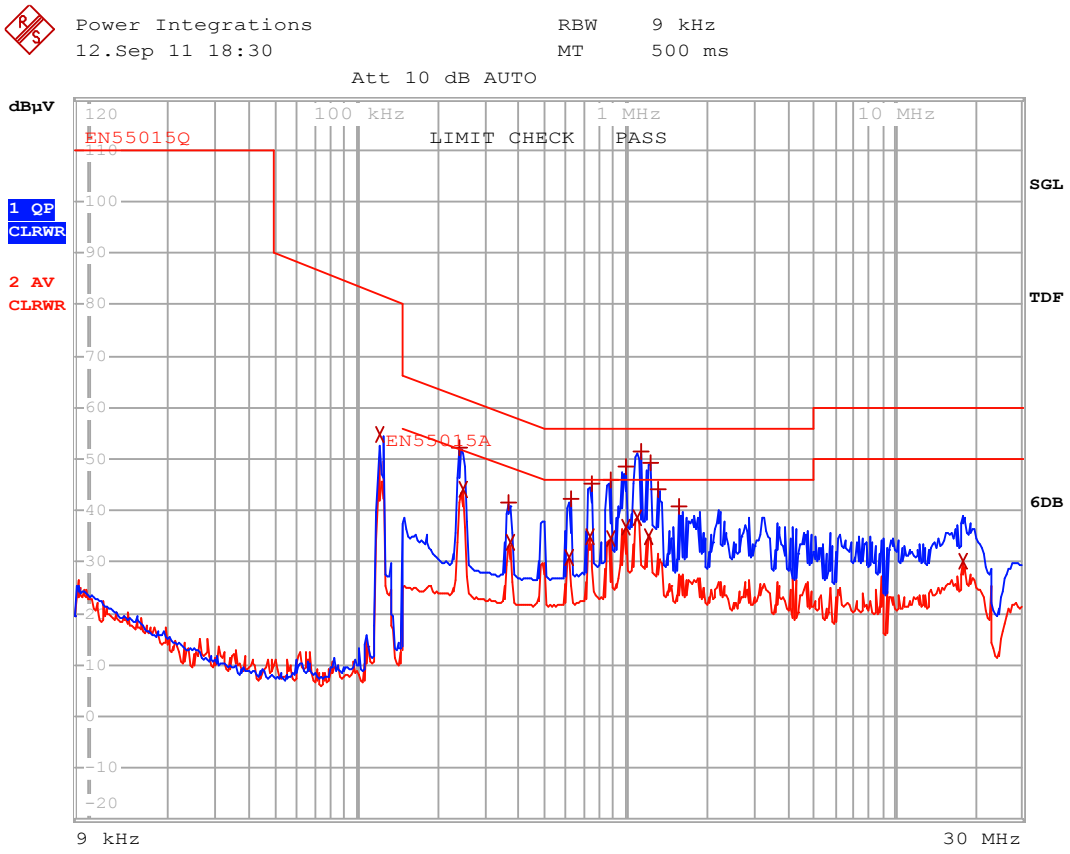

Figure 73 – Conducted EMI, 96 V / 45 mA Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	122.023208575 kHz	54.88	N gnd	
1	Quasi Peak	241.833911652 kHz	52.34	N gnd	-9.68
2	Average	246.694773277 kHz	44.07	L1 gnd	-7.79
1	Quasi Peak	363.658318017 kHz	41.72	L1 gnd	-16.92
2	Average	370.967850209 kHz	33.67	L1 gnd	-14.80
2	Average	610.105531335 kHz	30.92	L1 gnd	-15.07
1	Quasi Peak	628.59233904 kHz	42.21	L1 gnd	-13.78
2	Average	729.776191209 kHz	34.87	L1 gnd	-11.12
1	Quasi Peak	751.889139579 kHz	45.07	L1 gnd	-10.92
2	Average	872.919948931 kHz	34.49	L1 gnd	-11.51
1	Quasi Peak	881.64914842 kHz	45.82	L1 gnd	-10.17
1	Quasi Peak	1.00339897152 MHz	48.37	L1 gnd	-7.62
2	Average	1.00339897152 MHz	36.77	L1 gnd	-9.22
2	Average	1.09740267777 MHz	38.76	L1 gnd	-7.23
1	Quasi Peak	1.13065507631 MHz	51.29	L1 gnd	-4.70
2	Average	1.22433743114 MHz	35.01	N gnd	-10.98
1	Quasi Peak	1.23658080545 MHz	49.20	L1 gnd	-6.79
1	Quasi Peak	1.32578199726 MHz	44.12	N gnd	-11.87
1	Quasi Peak	1.58583078933 MHz	40.87	L1 gnd	-15.12
2	Average	17.975130353 MHz	29.98	L1 gnd	-20.01

Figure 74 – Conducted EMI, 96 V / 45 mA Steady-State Load Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits. Line and Neutral Scan Design Margin Measurement.

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13 Revision History

Date	Author	Revision	Description and Changes	Reviewed
13-Sep-11	JDC	1.1	Initial Release	Apps & Mktg
06-Oct-11	AS	1.2	Minor Corrections	Apps & Mktg
27-Oct-11	PV	1.3	Corrected bridge diode schematic symbol. Added 48 V, 45 mA version.	
07-Nov-11	ME	1.4	Added Figure 6 Auto-restart overvoltage protection	
10-Nov-11	PV	1.5	Added 48 V, 60 mA Specification Table	
09-Feb-12	KM	1.6	Updated Introduction Text	
17-Feb-12	DS	1.7	Updated to Single-Sided PCB Design.	

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