

# Designing AC to DC Forward Converters using ***TOPSwitch-GX***

# Agenda

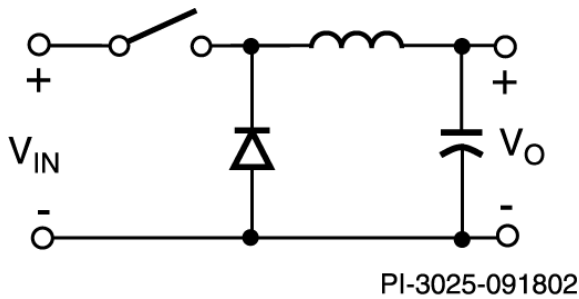
- ***TOPSwitch-GX* Advantages in Forward**
- **Forward Basics**
- **Transformer Reset and  $DC_{MAX}$  reduction**
- ***TOPSwitch-GX* Forward Converter Design Methodology**
  - Selecting *TOPSwitch-GX*
  - Magnetics design
  - Loop compensation
- **Application Examples**
  - 145 W PC Main/10 W standby - meets 1 W spec
  - 180 W PC Main/10 W standby - meets 1 W spec
- **Hints & Tips**

## ***TOPSwitch-GX* Advantages in Forward**

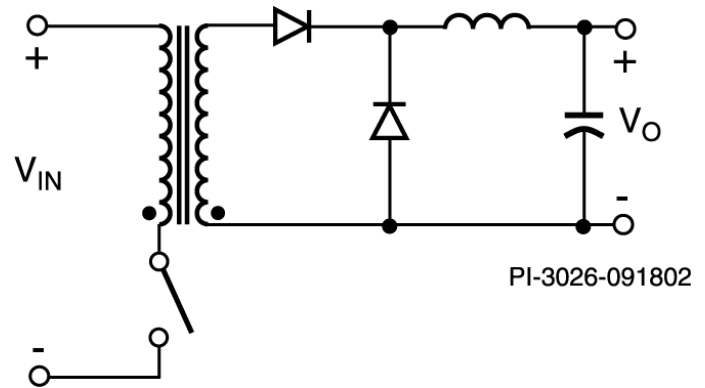
- **Small form factor, fewer components and high efficiency**
- **Allows for a simple robust design with high reliability**
- **Fully protected under fault conditions**
  - Max duty cycle reduction with line voltage
  - Line OV/UV, autorestart and thermal shutdown
- **Tight tolerances for high volume manufacturing**
- **Wide creepage for forced-air cooled environments**
- **Integrated soft-start for lower component stress**
- **Meets 1 W standby spec (using remote OFF)**

***TOPSwitch-GX* is a cost effective solution for Forward converter applications**

## Forward Basics



**Buck Converter**

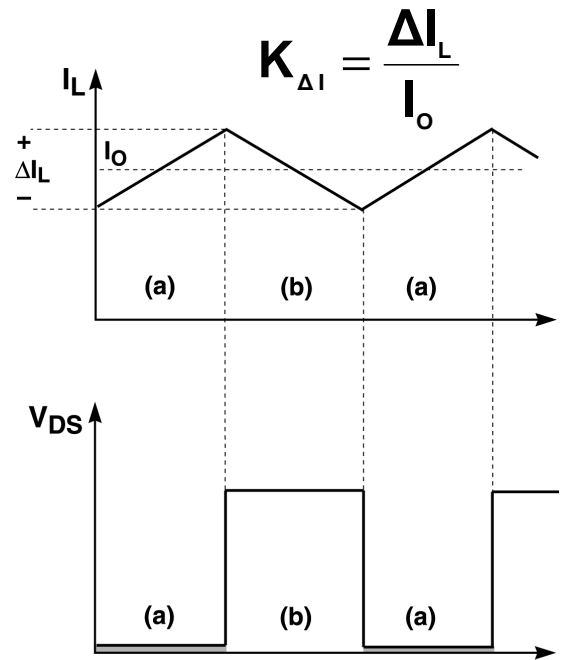
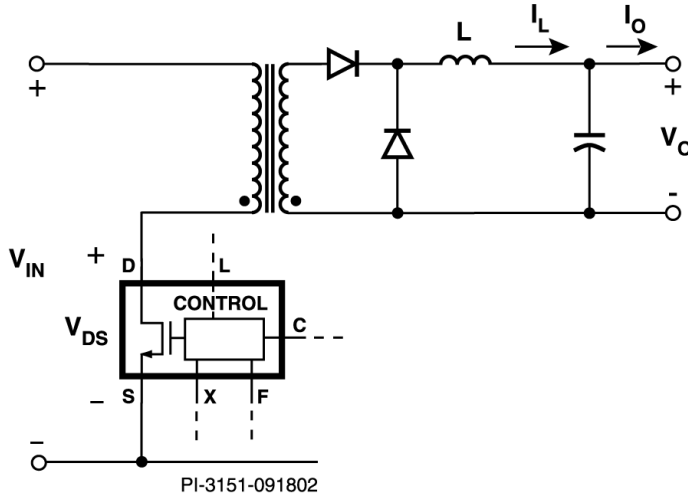


**Forward Converter**

- **Forward converter is a buck converter with a transformer**
  - Reduces primary current, provides isolation and multiple outputs
- **More cost effective than Flyback for  $\geq 6$  A output currents**

- **The Forward converter is the topology of choice for the Desktop PC industry in the 50 to 300 W range**
- **Forward topology is generally more effective than Flyback for low-voltage and high-current outputs**

# Forward Basics

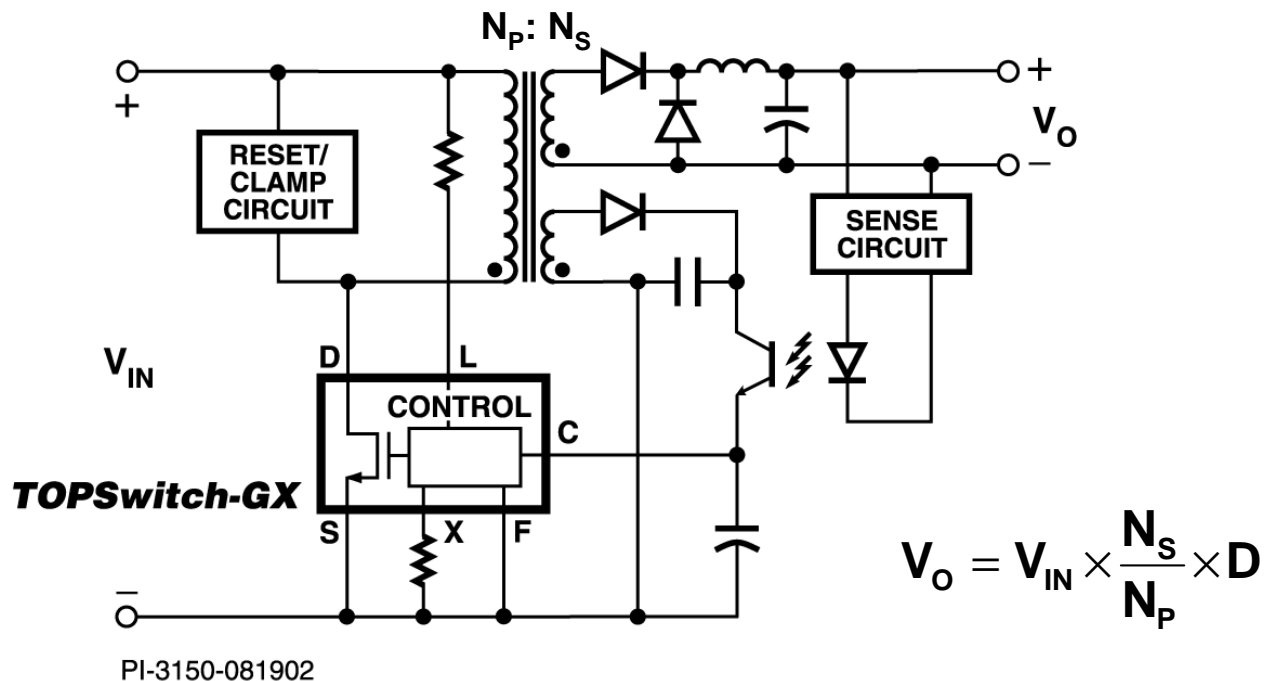


(a) Switch ON:  $I_L$  ramps up, delivering energy to inductor L and output

(b) Switch OFF:  $I_L$  ramps down in inductor L continuing delivery of energy to output

- In a Forward converter, the current in the output inductor supplies the load both when the primary switch is on and off. This means a small ripple current  $K_{\Delta I}$  in the output capacitor, smaller secondary RMS currents and output capacitors.
- Conversely, in a Flyback converter the transformer only delivers energy to the output during the off-time of the primary switch. The remainder of the time the energy comes from the output capacitors. This causes the ripple current in the capacitors and output diodes to be 2 to 3 times larger.
- The high switching current in Flybacks is the main reason why they become less cost effective at output currents greater than approximately 6 A, due to the higher cost of low ESR capacitors.

# Forward Transfer Function



$D = \text{TOPSwitch-GX duty cycle}$



- The Forward converter has a linear transfer function whereby duty cycle varies linearly with input voltage. This can limit the practical input voltage range over which a Forward converter is effective to typically 2:1 (>3:1 internally from DC rail).
- In contrast, a Flyback converter has a non-linear duty cycle with input voltage, allowing Flybacks to be effective over a much larger voltage range of typically 4:1
- (the transfer function shown on this slide is for continuous conduction mode only)

# Transformer Reset and $DC_{MAX}$ Reduction Circuits

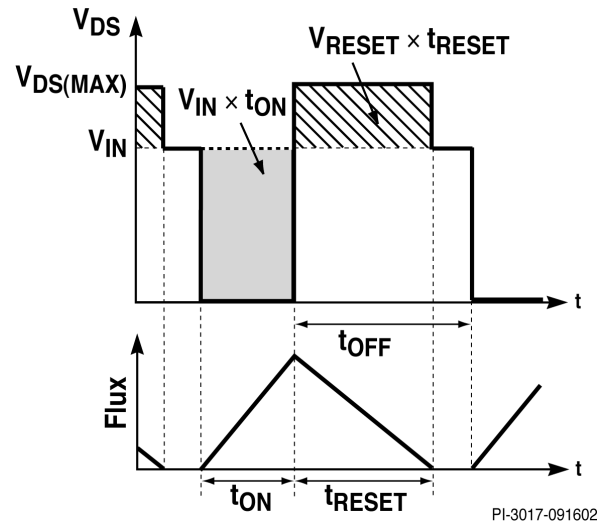
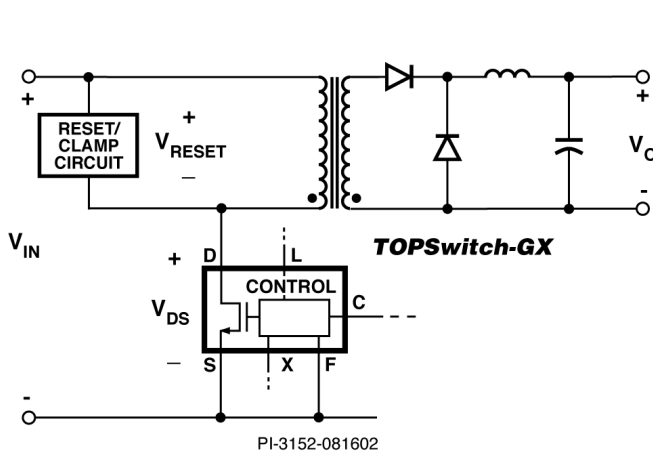
147

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- The *TOPSwitch-GX* Maximum Duty Cycle ( $DC_{MAX}$ ) reduction feature and other features allow the use of improved transformer reset techniques
- The transformer core reset technique that works best with the *TOPSwitch-GX* will be explained first. Then the more commonly used transformer reset techniques will be examined, and explanations given for why they should not be used with the *TOPSwitch-GX*.

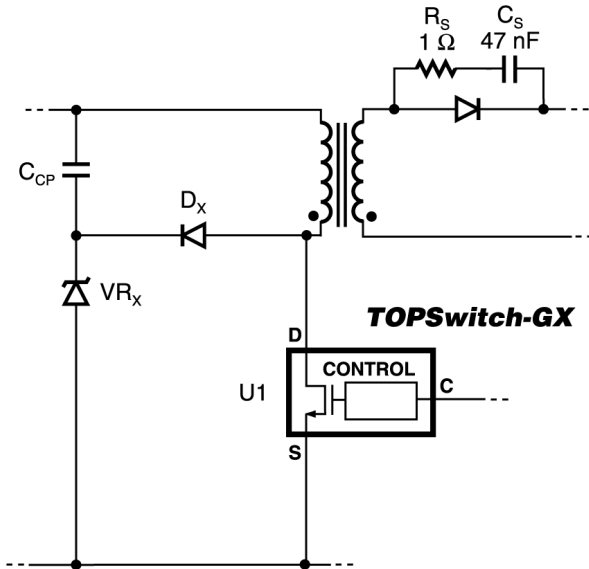
# Transformer Reset



- **Non ideal transformer has finite magnetizing inductance**
  - Flux builds up in magnetizing inductance when switch is on
  - Flux is reset each cycle by the reset circuit to prevent core saturation
- **$(V_{\text{RESET}} \times t_{\text{RESET}})$  must be  $\geq (V_{\text{IN}} \times t_{\text{ON}})$  to prevent transformer saturation**

- Flux built up in one direction by  $(V_{\text{IN}} \times t_{\text{ON}})$  is reset by an equal and opposite Volt-second area of  $(V_{\text{RESET}} \times t_{\text{RESET}})$
- Transformer should also be designed to prevent excessive peak flux within the on-time ( $t_{\text{ON}}$ ) of each switch-cycle. Excessive peak flux may cause transformer saturation.

# Zener Capacitor Reset Circuit



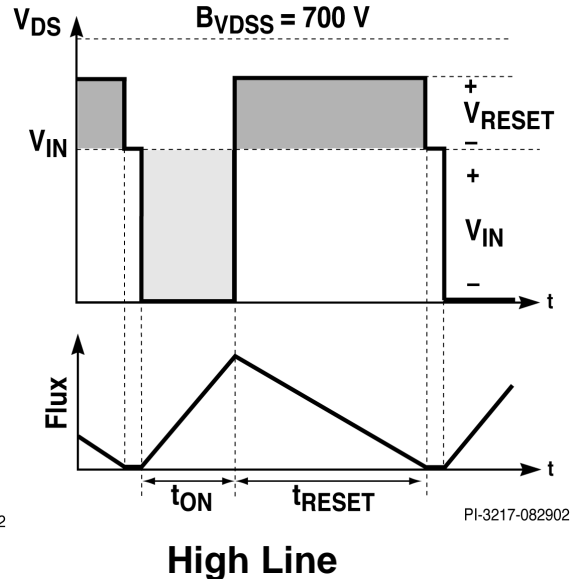
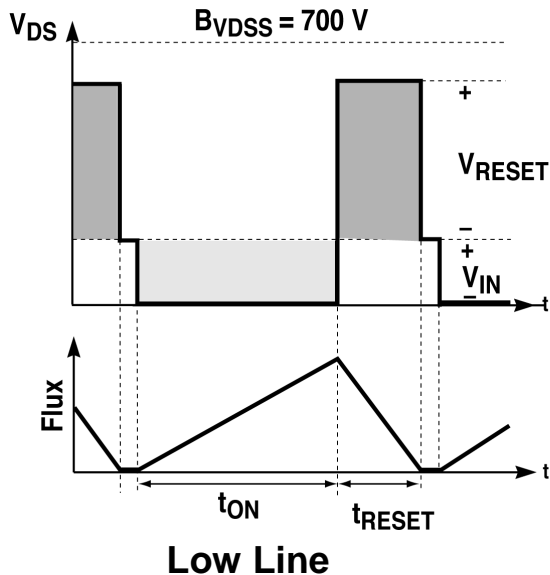
**Zener Capacitor Reset**  
Recommended for  $P_o < 200$  W

- **Maximizes reset voltage for all line conditions**
  - High reset voltage at low-line
  - Allows wide low-line duty cycle
  - Low reset voltage at high-line
  - Minimizes  $BV_{DSS}$  requirements
- **High efficiency**
  - Allows recovery of reset energy
- **Optimal use of MOSFET  $BV_{DSS}$  and  $R_{DS(ON)}$**
- **Requires *TOPSwitch-GX*  $DC_{MAX}$  reduction feature**

- **Allows wide low-line duty cycle and lowers peak  $V_{DS}$**
- **Variable reset voltage  $V_{RESET}$  adapts with input voltage allowing lower  $BV_{DSS}$  MOSFET to be used**
- **Maximum Duty Cycle ( $DC_{MAX}$ ) reduction must be used with this reset technique**

## Zener Capacitor Reset Advantages

- Limits peak drain voltages to  $\leq 600$  V
- Allows widest low-line duty cycle, reducing primary RMS currents



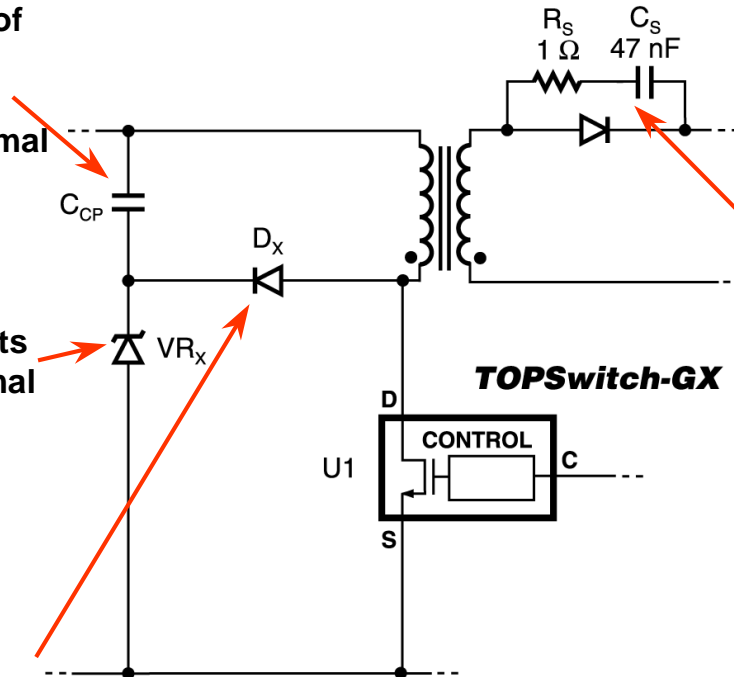
- This shows the voltage waveforms for Zener Capacitor Reset. Using the *TOPSwitch-GX* duty cycle reduction feature, Zener Capacitor Reset can be implemented with a 700 V MOSFET.
- The maximum duty cycle reduction feature prevents transformer saturation under transient load and overvoltage conditions
- As the line voltage reduces and the duty cycle increases, the reset voltage dynamically increases to ensure complete reset. Wide low-line duty cycle will minimize peak and RMS MOSFET currents and increase power supply efficiency.

# Zener Capacitor Reset Operation

A minimum value of  $C_{CP}$  - used only to absorb leakage energy during normal operation.

Zener only conducts briefly during normal operation, limiting  $V_{DS}$

Most energy in  $C_{CP}$  is recovered through slow-diode  $D_X$



$C_S$  is the main reset capacitor, which stores and recovers the magnetizing energy while the switch is off.  $R_S$  damps oscillations.

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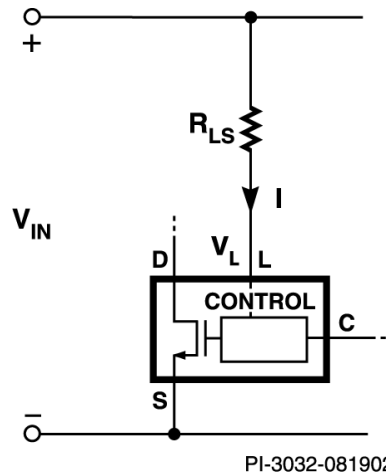
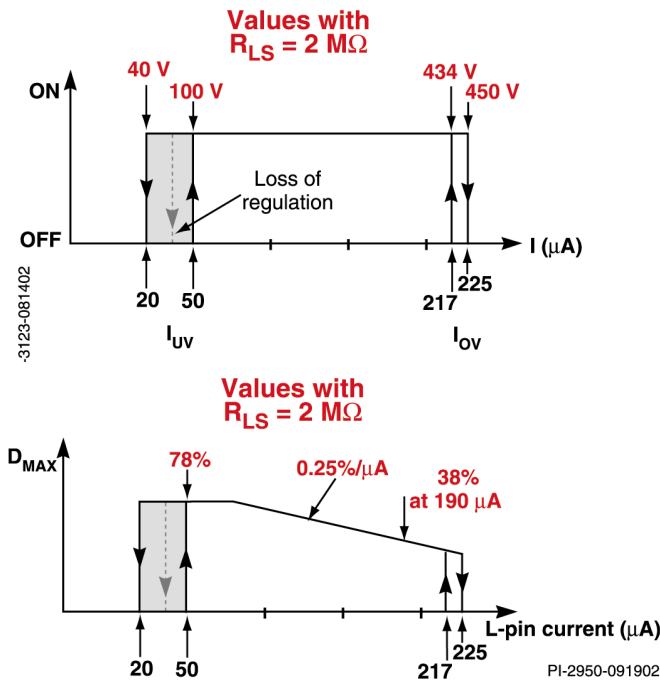
Typical values shown



- $C_S$  should be minimized to ensure successful worst case reset
- Transformer magnetizing energy is transferred to  $C_S$  when the switch is off, and then transferred to the output during the next switch on cycle, increasing efficiency
- Leakage energy is stored in  $C_{CP}$  during turn-off. This energy is partially recovered by slow diode  $D_X$ , helping to drive transformer flux negative. This is then cycled to the output through the transformer on the successive switch cycle.
- Zener  $VR_X$  sets the maximum drain voltage at turn off
- Allows wide duty cycle during power down, increasing hold-up time for a given input capacitance
- $DC_{MAX}$  reduction must be used with this reset technique.  $DC_{MAX}$  reduction is explained in the following slides.

# Linear DC<sub>MAX</sub> Reduction using Single Resistor

- L pin current sets UV/OV thresholds and activated DC<sub>MAX</sub> function



152

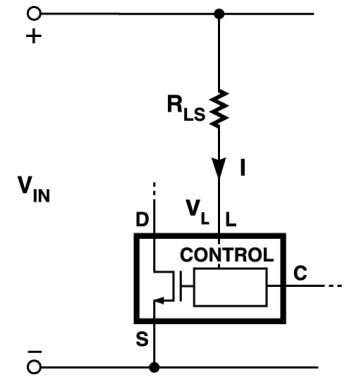
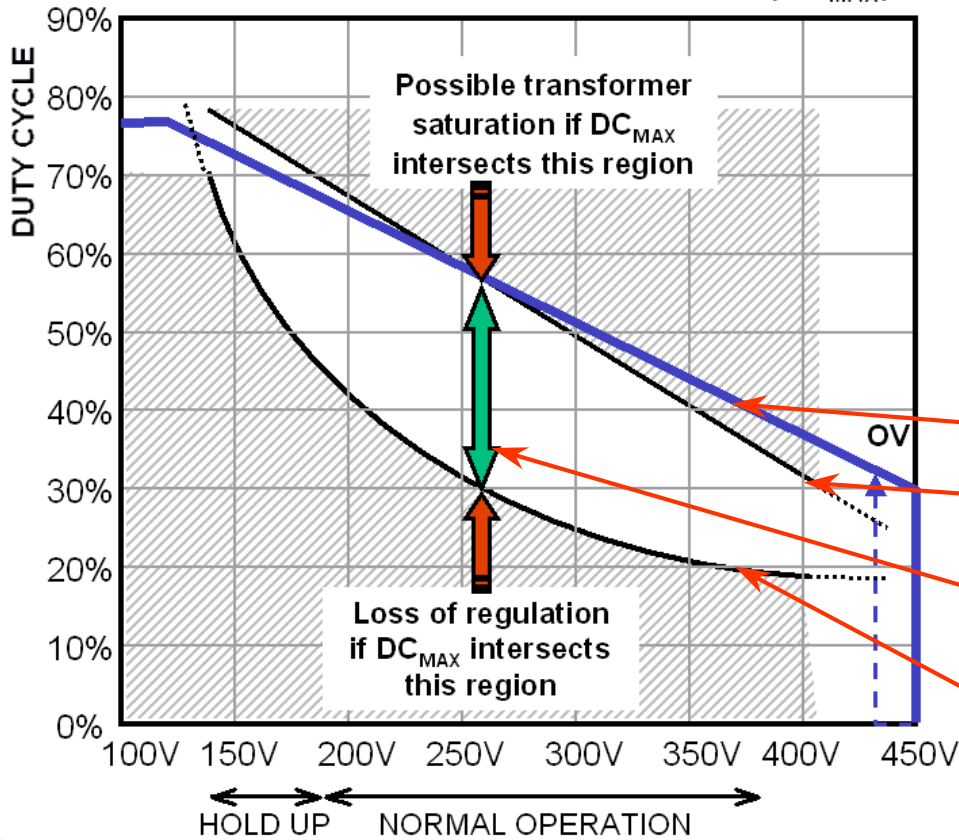
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- The built-in DC<sub>MAX</sub> function needs modification for Forward converter operation due to the strict limits on duty cycle required for transformer reset
- Also, in applications using input voltage doublers, the ratio of UV:OV requires modification from the TOPSwitch-GX internal default (set for universal)
- For example, using  $R_{LS} = 2\text{ M}\Omega$ , as in the diagram above:
  - Sets the UV turn on threshold at 100 V. This is too low - 230 V is required for PC Main (requiring a higher value for  $R_{LS}$ )
  - Sets the DC<sub>MAX</sub> limit too high for effective transformer saturation protection (requiring a lower value for  $R_L$ )
- Linear DC<sub>MAX</sub> reduction using a single resistor is not sufficient in most Forward converter designs, as shown in the following slides

# Linear $DC_{MAX}$ Reduction using $R_{LS} = 2\text{ M}\Omega$

LIMITS OF MAXIMUM DUTY CYCLE ( $DC_{MAX}$ )



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$DC_{MAX}$  with  $R_{LS} = 2\text{ M}\Omega$

Transformer reset limit  
(set by  $V_{RX}$ )

$DC_{MAX}$  must fall within this range

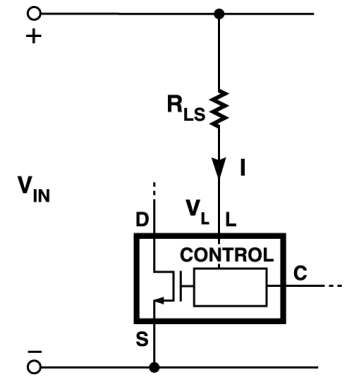
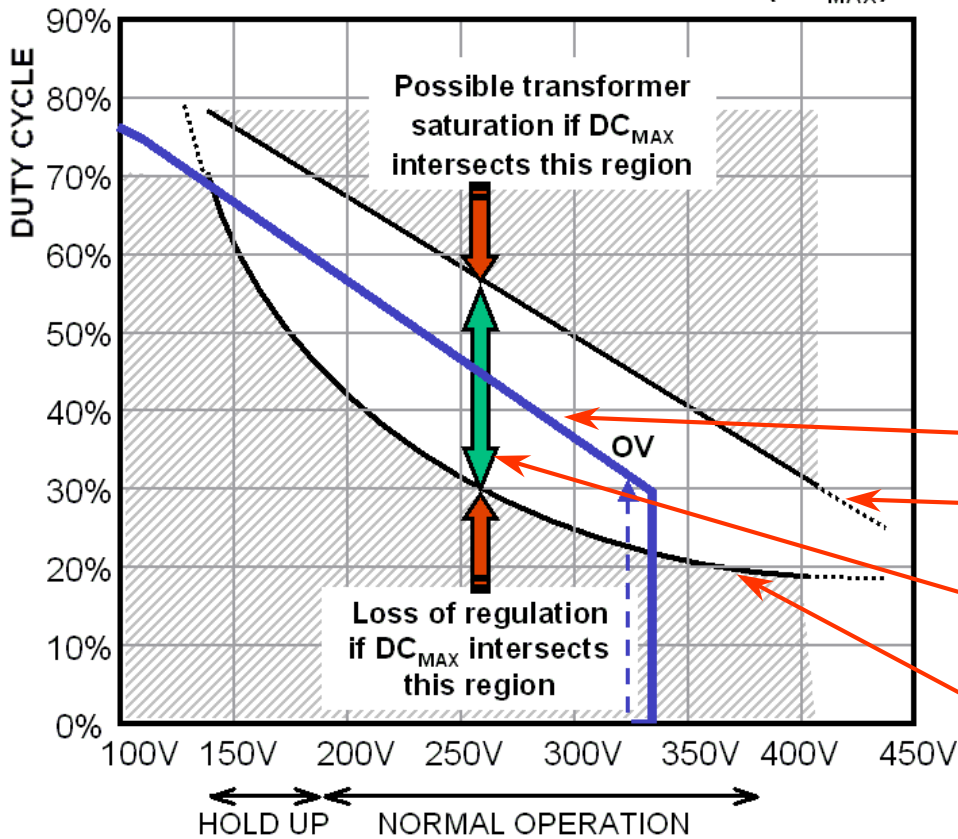
Operating duty cycle



- The Maximum Duty Cycle limit ( $DC_{MAX}$ ) must fall between the transformer reset limit and the operating duty cycle limit, allowing adequate margin for tolerance and transient operation:
  - If  $DC_{MAX}$  intersects the operating duty cycle area, loss of regulation will occur
  - If  $DC_{MAX}$  intersects the transformer reset area, saturation may occur under transient conditions
- With  $R_{LS} = 2\text{ M}\Omega$ , the  $DC_{MAX}$  limit line intersects the transformer reset limit region above approx. 250 VDC, causing possible transformer saturation during transients, overload etc.
- HOLD UP and NORMAL OPERATION ranges typical for a PC Main power supply application

# Linear $DC_{MAX}$ Reduction using $R_{LS} = 1.5 M\Omega$

LIMITS OF MAXIMUM DUTY CYCLE ( $DC_{MAX}$ )



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$DC_{MAX}$  with  $R_{LS} = 1.5 M\Omega$

Transformer reset limit

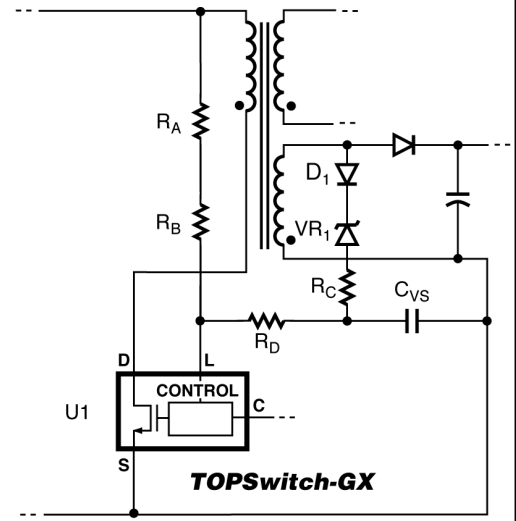
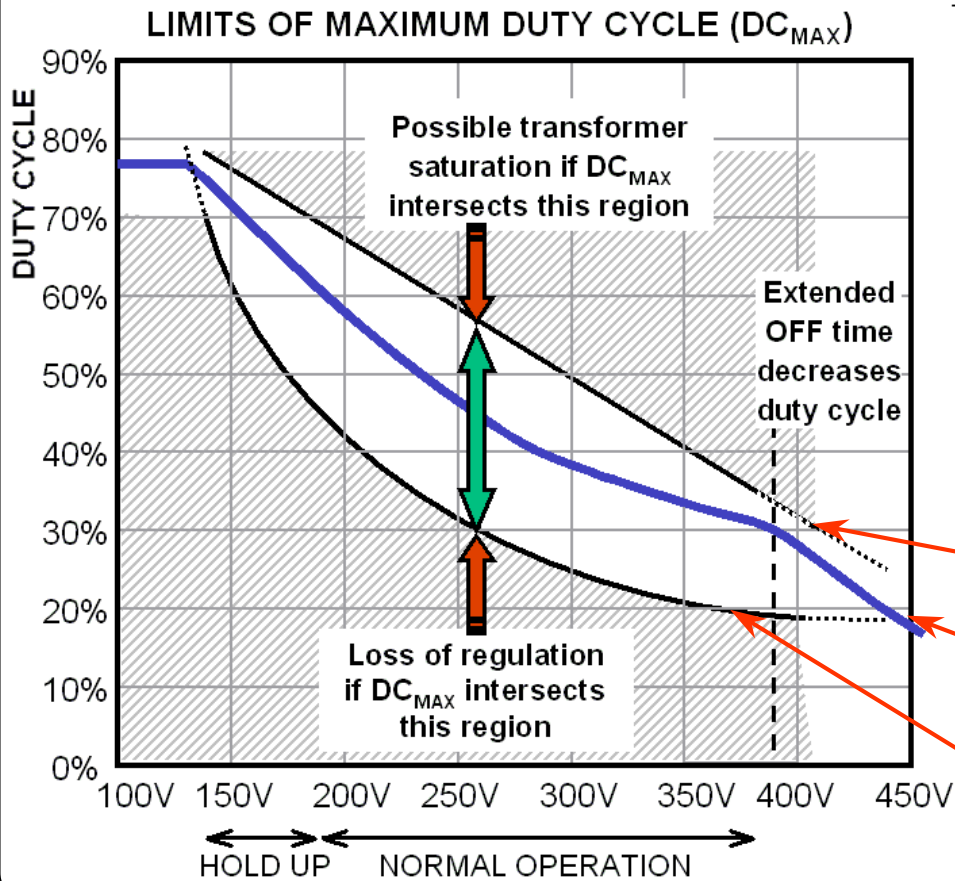
$DC_{MAX}$  must fall within this range

Operating duty cycle



- It is possible to change the slope and intercept of the  $DC_{MAX}$  limit line by changing the resistor value
- However, increasing the slope will also lower the OV shutdown threshold
- With  $R_{LS} = 1.5 M\Omega$ , the  $DC_{MAX}$  limit line is centered at lower voltages, but the OV threshold is set too low, causing OV shutdown above 335 VDC
- Additional external components are required to modify the  $DC_{MAX}$  reduction and still achieve acceptable OV shutdown thresholds

# Modified DC<sub>MAX</sub> Reduction



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Transformer reset limit  
Modified DC<sub>MAX</sub>  
Operating duty cycle



155

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- The modified DC<sub>MAX</sub> circuit centers DC<sub>MAX</sub> between the transformer saturation and operating limit boundaries as follows:
  - The startup threshold (230 V) is set by  $R_A + R_B$
  - After startup, components  $R_C$ ,  $C_{VS}$ ,  $D_1$  and  $VR_1$  provide a control signal that is dependant upon the line voltage and duty cycle. Resistor  $R_D$  feeds this signal to the L pin modifying the DC<sub>MAX</sub> characteristic in a non-linear manner

**Note:** when the L pin current exceeds the OV threshold (typically 225  $\mu$ A), the OFF time is extended until the current drops back below the lower OV threshold (typically 215  $\mu$ A). This lowers the switching frequency during OV, effectively decreasing the duty cycle below the preset minimum DC<sub>MAX</sub>, allowing full transformer reset and limiting  $V_{DS}$  at high line.

- An independent X pin UV shutdown is used (set at 130 V)
  - OV protection is achieved at high voltage when the modified DC<sub>MAX</sub> limit intersects the operating duty cycle limit, causing the power supply to lose regulation and latch off
- (Note: DI-20 and DI-30 both have a latching shutdown for fault conditions, such as loss of regulation)

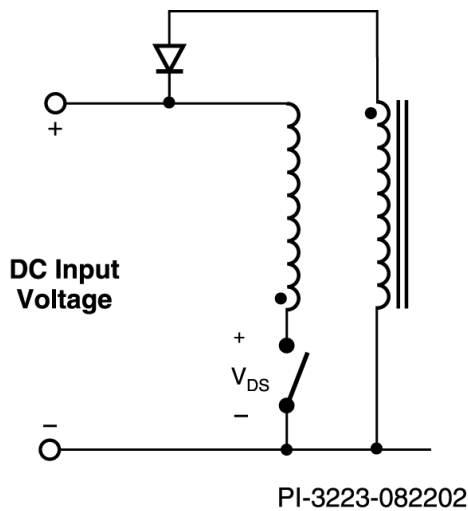
## Advantages of $DC_{MAX}$ Reduction

- **Prevents transformer saturation:**
  - On a cycle by cycle basis during output transient, power down and input overvoltage
  - Through transformer magnetizing energy build up
- **Allows sufficient off-time to recover clamp energy, using a slow diode**
- **Enables use of Zener Capacitor Reset circuit**
- **Enables use of 700 V MOSFET with good margin**
- **In conjunction with Zener/Capacitor reset, enables use of wide duty cycles at low input voltage**
  - Minimizes peak and RMS primary current

**The next few slides explain why other well known clamping techniques are not recommended**

- **Components values and duty cycle curves for  $DC_{MAX}$  reduction are covered by the design spreadsheet within PI Expert**

# 1:1 Reset Winding Not Recommended

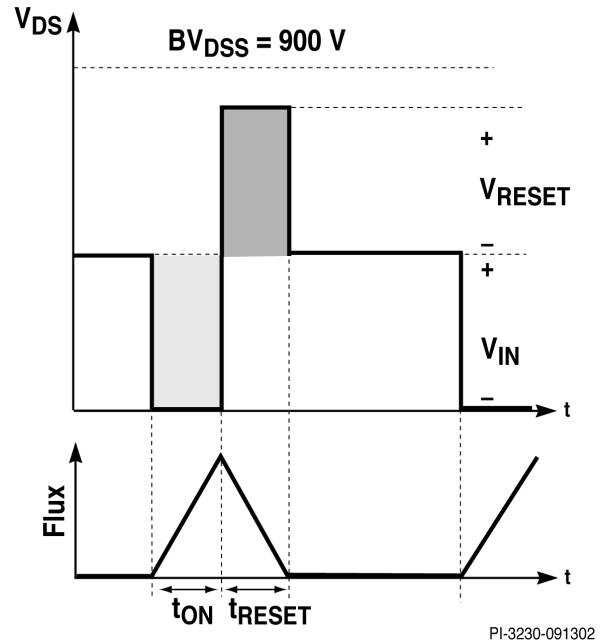
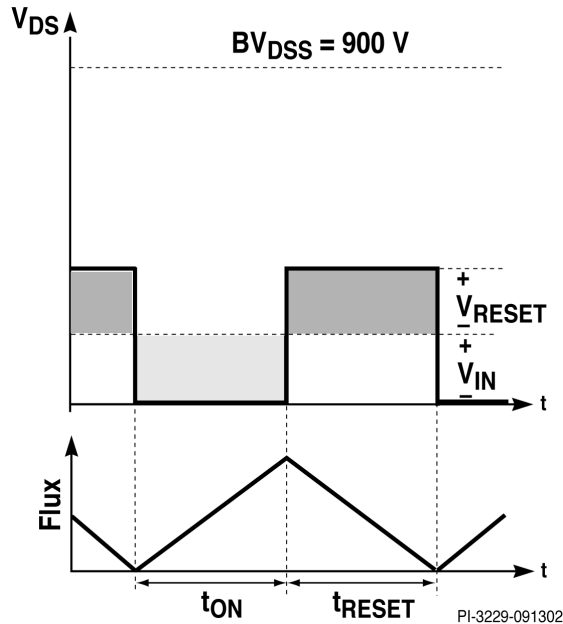


- Requires additional winding on transformer
- For 1:1 Reset Winding, duty cycle is limited to <50%
  - Lower primary to secondary turns ratio, increases RMS currents requiring lower  $R_{DS(ON)}$
  - Requires high breakdown voltage (900 V for 230 VAC applications)
- Does not efficiently use MOSFET  $BV_{DSS}$  and  $R_{DS(ON)}$

- Reset Winding is a commonly used technique to reset the transformer. It is shown for reference only.
- (Reset Winding is not recommended: this slide is for background information only)

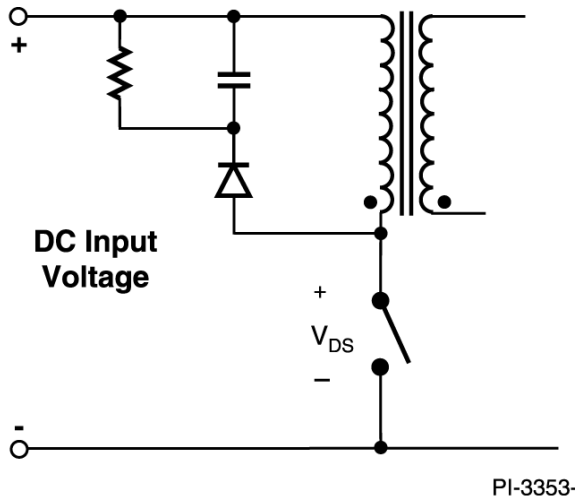
# 1:1 Reset Winding Waveforms

1:1 Reset Winding limits duty cycle to 50%, increasing conduction losses



- This shows the voltage waveform for a Reset Winding technique. For a typical power supply, use of Reset Winding would require a 900 V MOSFET to handle 265 VAC.
- At low-line the duty cycle is limited to  $\leq 50\%$  due to the 1:1 ratio of transformer reset voltage vs input voltage. Limited low-line duty cycle will increase peak and RMS MOSFET currents and reduce power supply efficiency.
- At high-line the duty cycle is limited by the  $BV_{DSS}$  of the MOSFET.
- (Reset Winding is not recommended: this slide is for background information only)

## RCD Reset Not Recommended

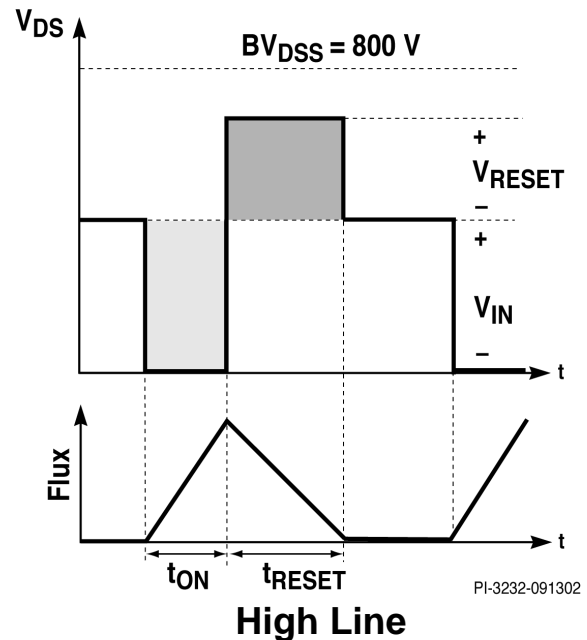
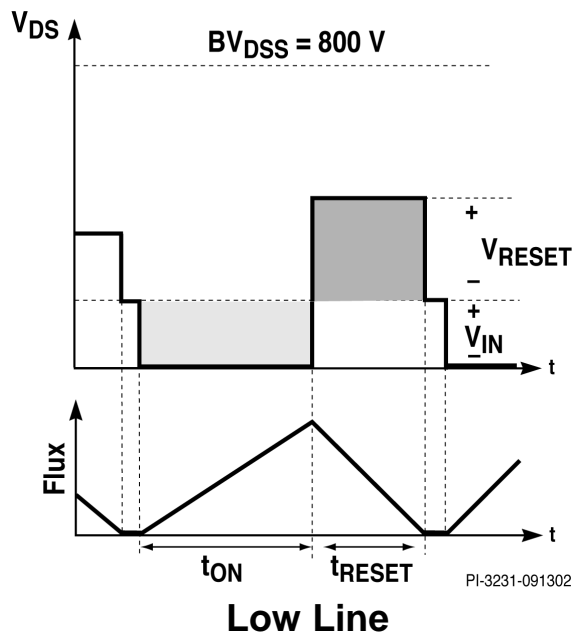


- **Reset clamp voltage varies with load conditions**
  - Worst case clamp voltage occurs for overload/fault at high line
  - Potential for drain overvoltage and transformer saturation during overload/fault and low to high step loads
- **Low efficiency dissipative reset scheme**
- **RCD Reset trades off low-line duty cycle vs  $BV_{DSS}$** 
  - Wide low-line duty cycle requires higher  $BV_{DSS}$  (800 V) device

- **Limited low-line duty cycle causes increased RMS currents hence higher conduction losses, making RCD not cost effective with TOPSwitch-GX**
- **(RCD Reset is not recommended: this slide is for background information only)**

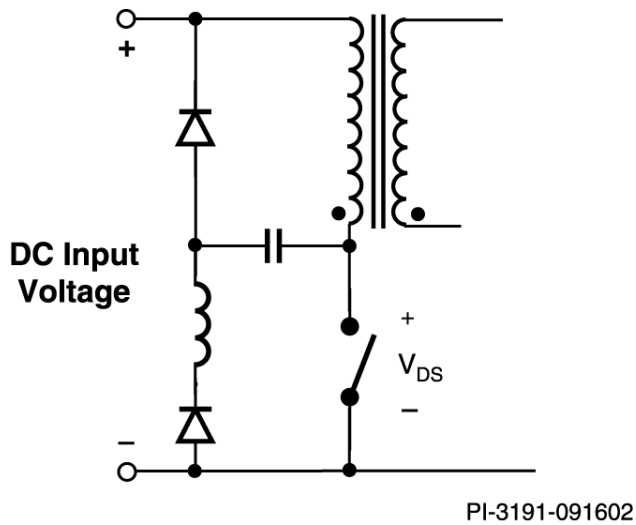
# RCD Reset Waveforms

Even with 800 V  $BV_{DSS}$  low-line duty cycle is limited, causing higher primary RMS currents



- This shows the voltage waveform for RCD Reset. For a typical power supply, use of RCD Reset would require an 800 V MOSFET. Without duty cycle reduction techniques, RCD Reset scheme may not prevent transformer saturation under certain conditions (power down, overvoltage and transient load).
- At low-line the duty cycle is constrained by the limited reset voltage available
- Wide low-line duty cycle increases the reset voltage required to guarantee reset, and thereby increases  $BV_{DSS}$  requirements for high line
- Limited low-line duty cycle will increase peak and RMS MOSFET currents and reduce power supply efficiency
- (RCD Reset is not recommended: this slide is for background information only)

## Resonant LC Clamp Not Recommended

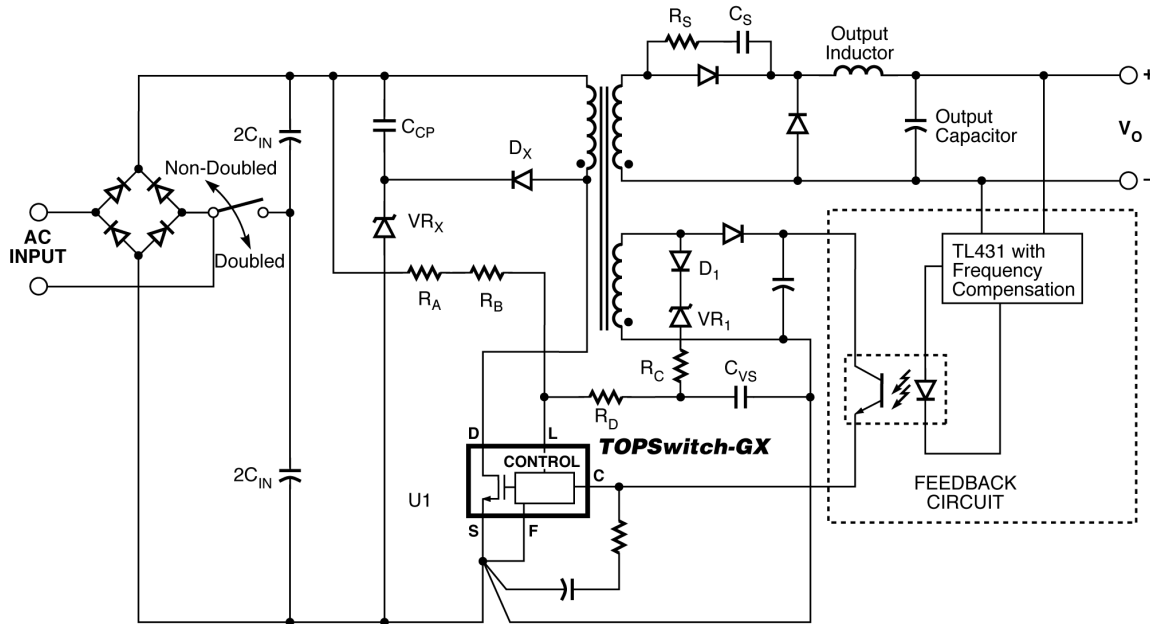


- $V_{DS}$  uncontrolled during overload
- Reset currents can interfere with *TOPSwitch-GX* current limit (clamp current sums with primary current)
- Higher cost than Zener Capacitor Reset

- (Resonant Reset is not recommended: this slide is for background information only)

# ***TOPSwitch-GX* Forward Design Methodology**

# TOPSwitch-GX Forward Design



PI-2817-082302

- **TOPSwitch-GX** provides many features and functions that enable a very cost effective, low component count Forward converter design

# AN-30 *TOPSwitch-GX* Forward Design Methodology

## TOPSwitch-GX Forward Design Methodology


Application Note AN-30

**Introduction**

The single-ended forward converter topology is often the best solution for AC-DC applications that require higher powers and higher output currents than are practical from flyback converters. The forward converter extends the power capability of TOPSwitch-GX to greater than 200W for high current outputs.

The feature set of TOPSwitch-GX offers the following advantages in single-ended forward designs:

- Built-in soft-start
- Built-in under-voltage lockout
- Built-in adjustable current limit
- Programmable duty cycle reduction to limit duty cycle excursion at high line and transient load conditions
- Higher efficiency (typically >70%)
- Very good light load efficiency
- Voltagemode control for simpler loop design with magnetic amplifier post-regulators
- Built-in remote on-off
- Low component count
- Improved EMI



**Scope**

This application note is for engineers designing an AC-DC power supply using TOPSwitch-GX in a single-ended forward converter. It addresses single input voltage 200VAC, and output 115 VAC input, but does not address universal input (85 V to 265 V) designs. The document highlights design parameters that are fundamental to the use of TOPSwitch-GX in a single-ended forward converter. It offers a procedure to compute transformer turns, output inductance and other design parameters. This procedure enables designers to build an operational prototype in the shortest possible time. Refinement of the prototype hardware after bench evaluation will lead to a final design.

The design methodology presented here is sufficiently general to cover a variety of single-ended forward designs, including power supplies for personal computers. It provides formulas for multiple outputs with coupled inductors, independent multiple outputs, and outputs with both linear or magnetic amplifier post regulators.

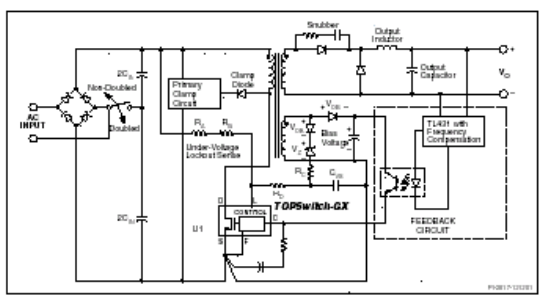
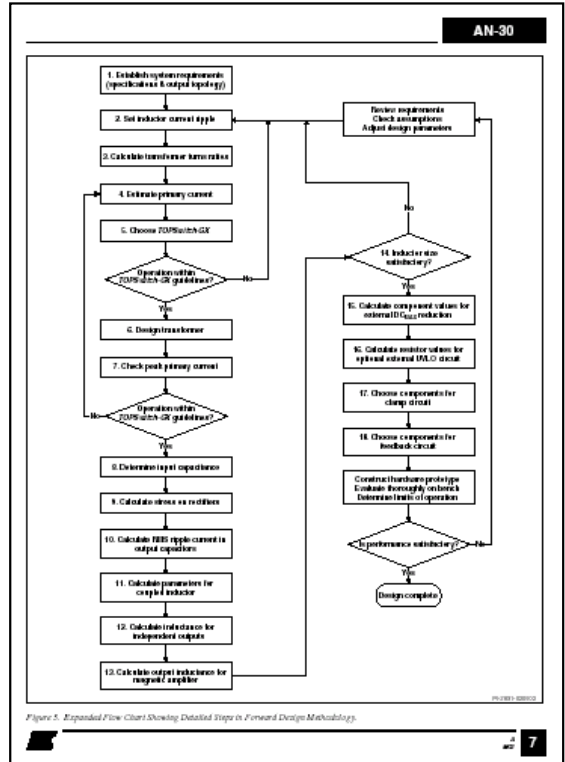


Figure 1. Typical Configuration of TOPSwitch-GX in a Single-Ended Forward Converter.

August 2000



**Note: The following slides will highlight steps in the design process. See AN-30 for full details**



An AN-XX document is an Application Note:

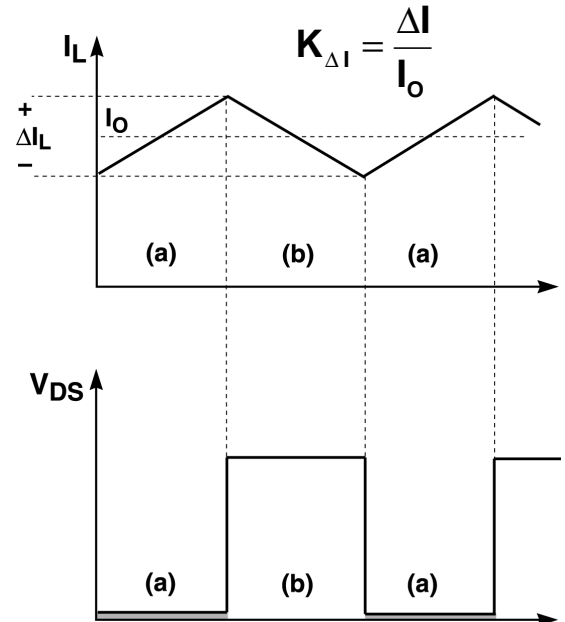
- AN-30 describes the step-by-step design process for designing Forward converters with the *TOPSwitch-GX* family of devices
- AN-30 includes all of the equations needed to create a design manually
- The step numbers in the following slides refer to the steps in AN-30
- The *PIXI*s spreadsheet performs most of the complex design calculations required by AN-30, greatly reducing the design time

## Step 1: Design Requirements

- Enter power supply specifications into *PIXI's* spreadsheet
- Consider the following points when designing PC Main Forward converter
  - PC Main with doubler input typically has a minimum bus voltage of 200 VDC at full load, based on commonly used capacitor values
  - Passive PFC reduces the minimum bus voltage from 200 VDC to 180 VDC
  - To meet holdup time requirements, full power delivery is usually required during power-down to a bus voltage of 140 VDC
  - Therefore, a PC Main has to deliver:
    - Continuous full power from 180 VDC to 375 VDC (thermally limited)
    - Full power during power down to 140 VDC (not thermally limited)
  - This puts the input voltage range for PC Main in between 230 VAC $\pm$ 15%, and Universal (85-265 VAC) in the *TOPSwitch-GX* power table

## Step 2-4: Estimate Inductor Ripple Current

- **Step 2** : Ripple current is estimated at highest input voltage
- User provides the value of  $K_{\Delta I}$  which for most designs is in the range  $0.15 < K_{\Delta I} < 0.3$ , based on inductor and capacitor ripple current
- **Step 3**: Transformer turns ratio is then estimated at  $V_{\text{DROPOUT}}$  max duty and full load
- **Step 4**: Peak current is estimated once  $K_{\Delta I}$  and turns ratio are known



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- In PC main applications  $V_{\text{DROPOUT}}$  is typically 140 VDC
- In the EP12 PC Main example,  $K_{\Delta I}$  is 0.15

## Step 5: Select **TOPSwitch-GX** for Peak Current and Continuous Power

OUTPUT POWER TABLE – Y or F PACKAGE (TO-220)				
PRODUCT	230 VAC $\pm$ 15%		85-265 VAC	
	Adapter	Open Frame	Adapter	Open Frame
TOP242 Y or F	10 W	22 W	7 W	14 W
TOP243 Y or F	20 W	45 W	15 W	30 W
TOP244 Y or F	30 W	65 W	20 W	45 W
TOP245 Y or F	40 W	85 W	26 W	60 W
TOP246 Y or F	60 W	125 W	40 W	90 W
TOP247 Y or F	85 W	165 W	55 W	125 W
TOP248 Y or F	105 W	205 W	70 W	155 W
TOP249 Y or F	120 W	250 W	80 W	180 W
TOP250 Y or F	135 W	290 W	90 W	210 W

- **Open frame power is based on peak current and input voltage**
  - larger device may be required depending on thermal environment
- **For a PC Main the input range is in between 230 VAC $\pm$ 15% and 85-265 VAC**
  - Example 1: TOP249Y can deliver approx. 180 W with passive PFC
  - Example 2: TOP247Y can deliver approx. 145 W



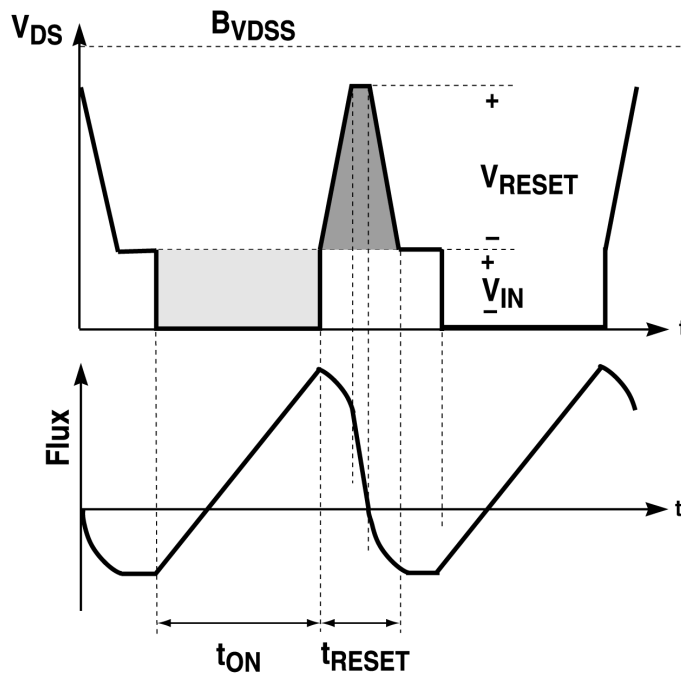
- **Power capability depends on the thermal environment, the minimum input voltage, and the input capacitance**
- **In PC Main applications the input voltage range falls between the two input voltage ranges shown in the power table (i.e. 230 VAC  $\pm$ 15% and 85-265 VAC)**
- **As a result, the device power capability will also fall between the two voltage ranges shown in the table, as demonstrated later in the two examples (see applications section)**
- **With passive PFC, the input voltage range is almost equivalent to 85-265 VAC**
- **PIXIs will automatically select the smallest TOPSwitch-GX for the required power, but a larger device may be chosen for higher efficiency**

## Step 6-7: Transformer Design

- **(Step 6) Select from industry standard cores in the spreadsheet**
  - The spreadsheet will design the transformer with no gap as recommended for the Zener Capacitor Reset circuit
- **Spreadsheet calculates the minimum secondary turns (limited by max flux density)**
  - Can be manually overridden for output voltage centering
  - Spreadsheet designs for a Max flux density  $B_M < 2000$  gauss (0.2 T)
- **Spreadsheet calculates the maximum primary to secondary turns ratio for lowest RMS currents**
  - Consider DC stacking for multiple output designs
- **(Step 7) Check peak and RMS primary current, using transformer parameters as calculated above to replace estimated values (from step 4)**

- Use the *PIXIs* spreadsheet for transformer design. AN-30 provides sufficient information to design manually.
- *PIXIs* does not provide transformer construction details

## Zero Gap Transformer Recommended



PI-3291-083002

- Zero gap transformer maximizes magnetizing inductance and minimizes magnetizing current thus minimizing reset energy, improving efficiency
- Zener Capacitor Reset circuit causes negative residual flux at end of reset cycle
- Negative flux completely resets transformer allowing use of a zero gap transformer
- Zero gap recommended with Zener Capacitor Reset scheme

- The Zener Capacitor Reset technique allows use of zero gap transformer. Zero gapping is often avoided in the industry due to the limited available AC-flux range.
- With Zener Capacitor Reset, transformer flux actually resets slightly below zero on each cycle, expanding the available AC-flux range for the same final peak flux
- Zero gap transformers improve power supply efficiency and are recommended for use with *TOPSwitch-GX* and Zener Capacitor Reset

## Step 7-16: *PIXIs* Spreadsheet

- **Spreadsheet**
  - Calculates RMS and peak currents and voltages for primary and all outputs
  - Output inductor value
- **Calculates component values for *TOPSwitch-GX* programming**
  - $R_X$  for X pin  $I_{LIMIT}$
  - $R_{UVA}$ ,  $R_{UVB}$  and  $R_{UVC}$  resistors for independent (X pin) undervoltage lockout
  - $R_A$ ,  $R_B$ ,  $R_C$ ,  $R_D$  and  $C_{VS}$  for  $DC_{MAX}$  reduction
  - Includes graph of  $DC_{MAX}$  reduction vs input voltage

	A	B	D	F	G	
1	ACDC_TOPGXForward_Rev_1.04_082302 Copyright Power Integrations Inc. 2002	INPUT	INFO	OUTPUT	UNIT	ACDC_TOPGXFwd_082302_r104.xls Transformer Design Spreadsheet
2	OUTPUT VOLTAGE AND CURRENT					<b>EP12 PC Main power supply</b>
3	VMAIN	5			Volts	Main output voltage
4	IMAIN	12			Amps	Main output current
5	VMAINMA	3.3			Volts	Magamp output voltage
6	IMAINMA	12			Amps	Magamp output current
7	VALX1	12			Volts	Auxiliary output voltage
8	IALX1	4			Amps	Auxiliary output current
9	VIND1				Volts	Independent output voltage
10	IIND1				Amps	Independent output current
11	PO			147.6	Watts	Total output power
12						
13	ENTER APPLICATION VARIABLES					
14	VACMIN	90			AC volts	Minimum AC input voltage. Input voltage dc
15	VACMAX	132			AC volts	Maximum AC input voltage. Input voltage d
16	VMIN			188	Volts	Minimum DC Bus voltage at low line input
17	VMAX			373	Volts	Maximum DC Bus voltage at high line input
18	CIN	165			uFarads	Equivalent bulk input capacitance. Input vc
19	fL	50			Hz	Input AC line frequency
20	tc	3.0			mSeconds	Estimate input bridge diode conduction time
21	th	16.0			mSeconds	Minimum required hold-up time from VDRDP
22	EFF	0.75				Efficiency estimate to determine minimum DC
23	VHOLDUP			188	Volts	DC Bus voltage at start of hold-up time (defe
24	VDRDPOUT			132.518313	Volts	DC Bus Voltage at end of hold-up time
25	DMAX GOAL			0.69		Maximum duty cycle at DC dropout voltage
26	VDSOP			580	Volts	Maximum operating drain voltage

ACDC\_TOPGXForward\_Rev\_1.04\_082302

- The *PI Expert* program provides a design spreadsheet tool called *PIXIs*. This spreadsheet calculates all key power supply parameters. *PI Expert* and *PIXIs* are both freely available and periodically updated - check Power Integrations' web site for latest version.
- ( $R_{UVA}$ ,  $R_{UVB}$  and  $R_{UVC}$  are resistors for independent (X pin) undervoltage lockout circuit )
- ( $R_A$ ,  $R_B$ ,  $R_C$ ,  $R_D$  and  $C_{VS}$  used for  $DC_{MAX}$  mentioned in earlier slides)
- The *PIXIs* spreadsheet tool covers steps 7 through 16

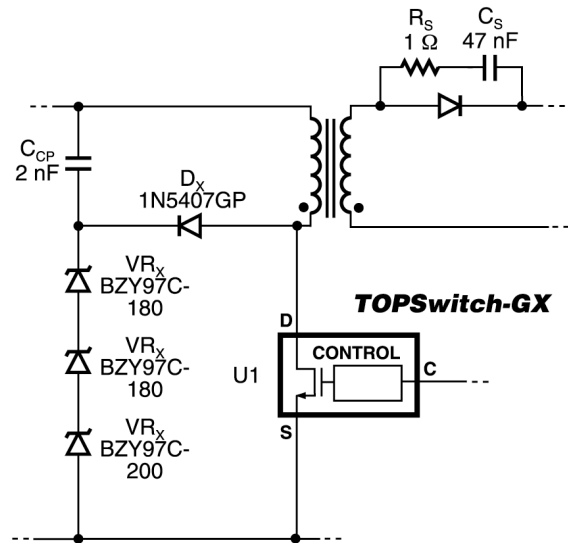
## Step 8-16: Calculate Component Values

- AN-30 provides equations and guidance for calculation of the main primary and secondary components:
- Input capacitors (step 8)
- Input rectifiers (step 9)
- Output capacitors and ripple current (step 10)
- Output coupled inductor (step 11-14)
- Component values for  $DC_{MAX}$  reduction circuit (step 15)
- Optional UV lockout circuit (step 16)

- *PI Expert* provides automated calculation of these components

## Step 17: Reset Circuit Component Selection

- Select Zener  $V_{R_X}$  voltage to provide required clamp level. A number of Zeners can be used in a series chain to reduce individual Zener dissipation (series sum of Zener voltages gives desired clamp voltage).
- $C_{CP}$  must be chosen empirically to accommodate parasitics. Too small will increase Zener dissipation. Too large may cause saturation during step loads
- Diode  $D_X$  is a slow recovery diode
- Use recommended values for  $R_S$  and  $C_S$

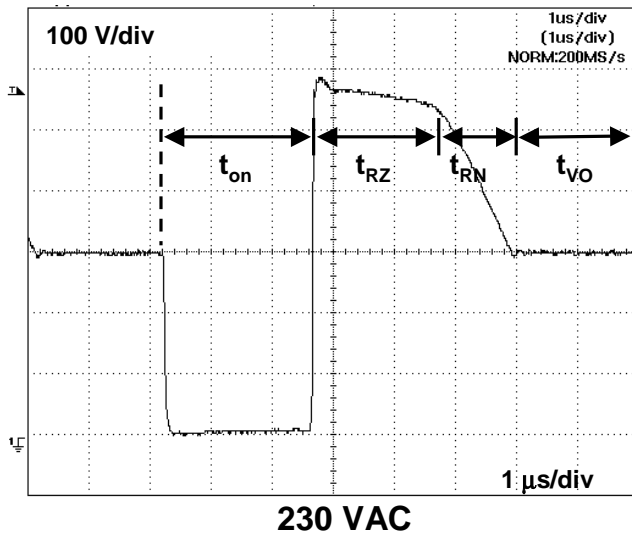


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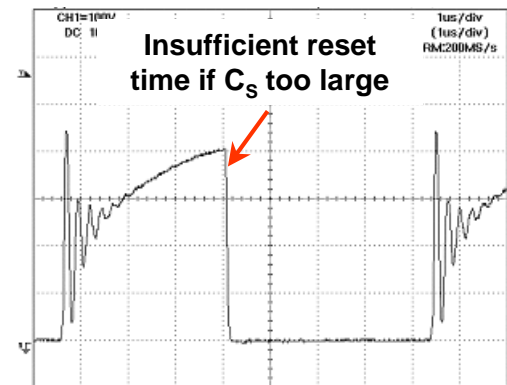
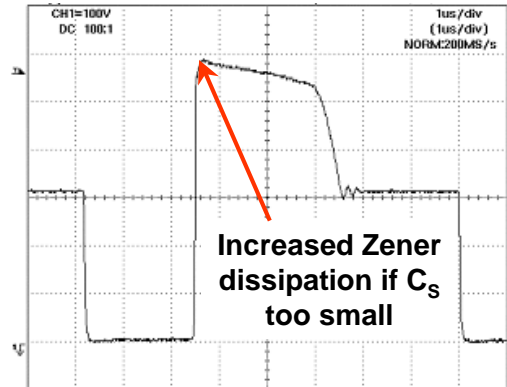
Zener Capacitor <200 W

- Typical value for  $C_{CP}$  is approximately 2 nF
- $D_X$  is a slow recovery type, such as 1N5407 but should be a glass passivated type
- $V_{RX}$  is typically made up of three Zeners in series:  
BZY97C-200, 2 x BZY97C-180

# Optimizing $C_S$ Value using Drain Waveforms

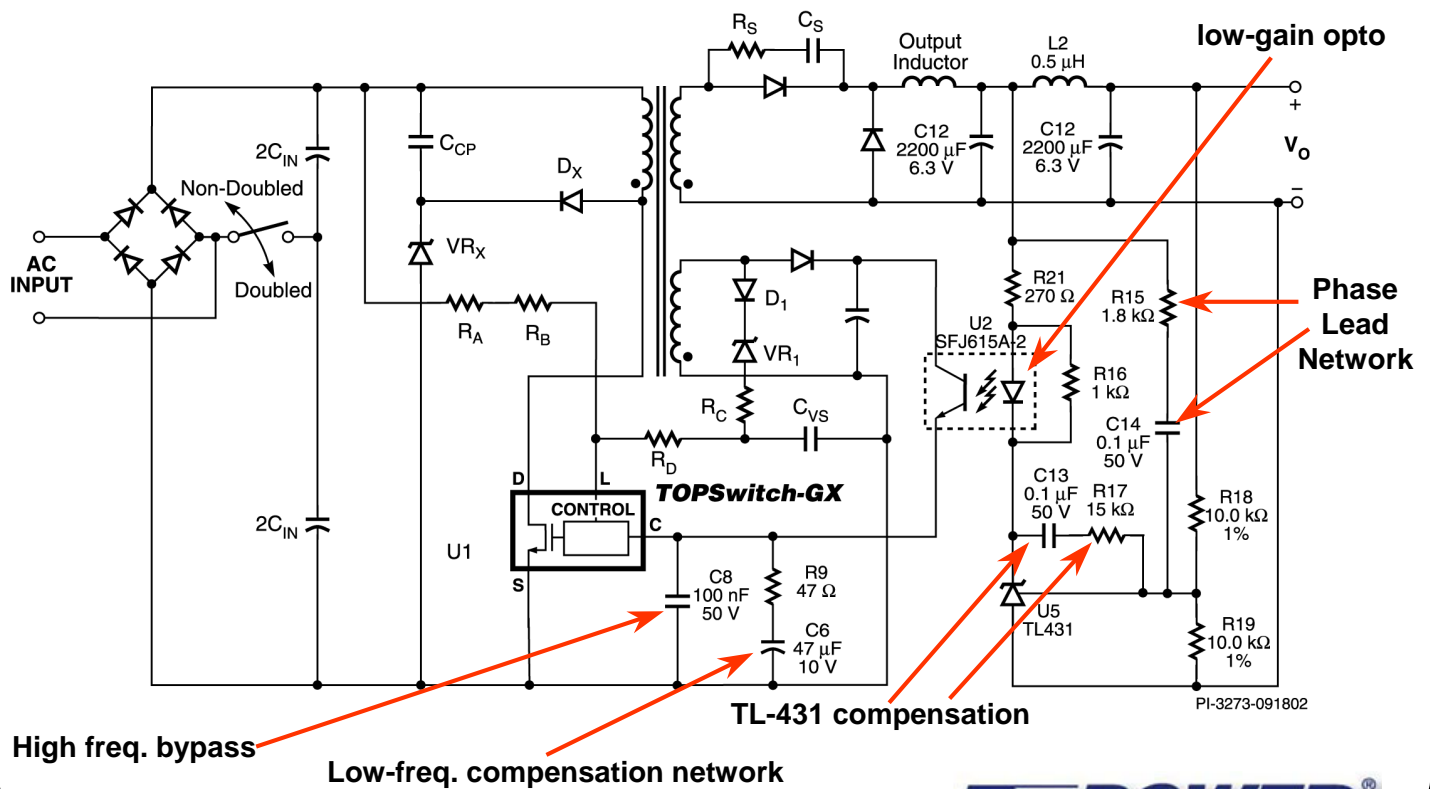


- $t_{on}$  - MOSFET on time
- $t_{RZ}$  - reset of magnetizing flux to zero
- $t_{RN}$  - relaxation ring (below zero flux)
- $t_{VO}$  - clamped by forward output diode



- An optimized value of  $C_S$  ensures the best efficiency and adequate reset time
- Note: In the upper right hand scope plot  $C_S = 0$ . In the lower right hand scope plot  $C_S = 470$  nF (10 x the ideal value)

## Step 18: Typical Feedback Components



174

Filename: GX Forward 10062004.ppt



### • Optocoupler

- Use low gain low cost opto (example:  $0.5 < \text{CTR} < 2.0$ ) and set high frequency gain using optodiode series resistor (see Applications section for typical values)

### • TL431

- An RC network across TL-431 determines low to mid-frequency gain – use  $0.1 \mu\text{F}$  compensation capacitor
- DC feedback may be shared for multi-output designs
- An RC Lead network is connected before post-filter inductor for good gain crossover phase margin – start design with values shown and adjust if necessary

### • CONTROL pin cap sets low frequency pole & defines low freq gain characteristics

- **100 nF decoupling capacitor between CONTROL and SOURCE pins of TOPSwitch-GX device is for bypassing high frequency switching noise**

### • See AN-30 for details

## Refine the Design

- **Build a prototype of the design**
- **Verify that output characteristics meet system requirements**
- **Check that device current, voltage, and power measurements are sufficiently within specification limits for all components**
- **If necessary, modify design parameters and recalculate key design values**
- **Build the next iteration of the design, test it, and verify the results**

- **A quick design checklist of the critical parameters is provided on the next slide**

## Quick Design Checklist

- **Maximum drain voltage**
  - Verify that the peak drain voltage is  $< 675$  V at highest line voltage and maximum overload output power.
  - Maximum overload output power occurs when output is loaded to a level just before auto-restart occurs
- **Maximum drain current at maximum input voltage, output load and ambient temperature**
  - Verify sufficient time for complete transformer reset at start-up, overload and step load conditions
  - Leading edge current should be below current limit envelope after leading edge blanking (see *TOPSwitch-GX* data sheet - Fig. 52)
- **Verify temperature of key components (maximum load, ambient temperature and minimum input voltage)**
  - Input diodes, *TOPSwitch-GX*, clamp components, transformer, output diodes and output capacitors
  - Recommended maximum *TOPSwitch-GX* source pin/tab temperature is  $100$  °C at full  $I_{LIMIT}$  and  $110$  °C with reduced  $I_{LIMIT}$
  - Leave enough thermal margin for part-to-part variation of the  $R_{DS(ON)}$

- **See AN-30 Appendix B, for details on how to verify that the maximum duty cycle reduction function is working properly**

# Application Examples

- **145 W (160 W pk) ATX PC Main without PFC** (EPR-12/DI-20)
  - +3.3V, +5V and +12V
- **180 W (200 W pk) SFX12 PC Main with Passive PFC** (EPR-31/DI-30)
  - +3.3V, +5V, +12V and –12V

DI: Design Idea  
EPR: Engineering Prototype Report



- **Additional Design Ideas, Engineering Prototype Reports and Design Example Reports are available on the *PI* web site, at [www.powerint.com/appcircuits.htm](http://www.powerint.com/appcircuits.htm)**

## 145 W PC Main Performance Table (DI-20)

DESCRIPTION	MAIN SUPPLY	STANDBY SUPPLY
Input Voltage (doubled)	185 to 265 VAC 90 to 132 VAC	185 to 265 VAC 90 to 132 VAC
Output Voltage/Current	3.3 V / 0.5 to 12 A 5.0 V / 0.4 to 15 A 12.0 V / 0.05 to 3 A	5 V / 0 to 2 A (2.5 A pk)
Output Power	145 W (160 W pk)	10 W (12.5 W pk)
Efficiency	71%	75%
No-Load Input Power (Output Power)	5 W Blue Angel 1 W Standby 30 W Energy Star	– 4.2 W (2.5 W out) – 0.91 W (0.5 W out) – 23.5 W (15.1 W out)

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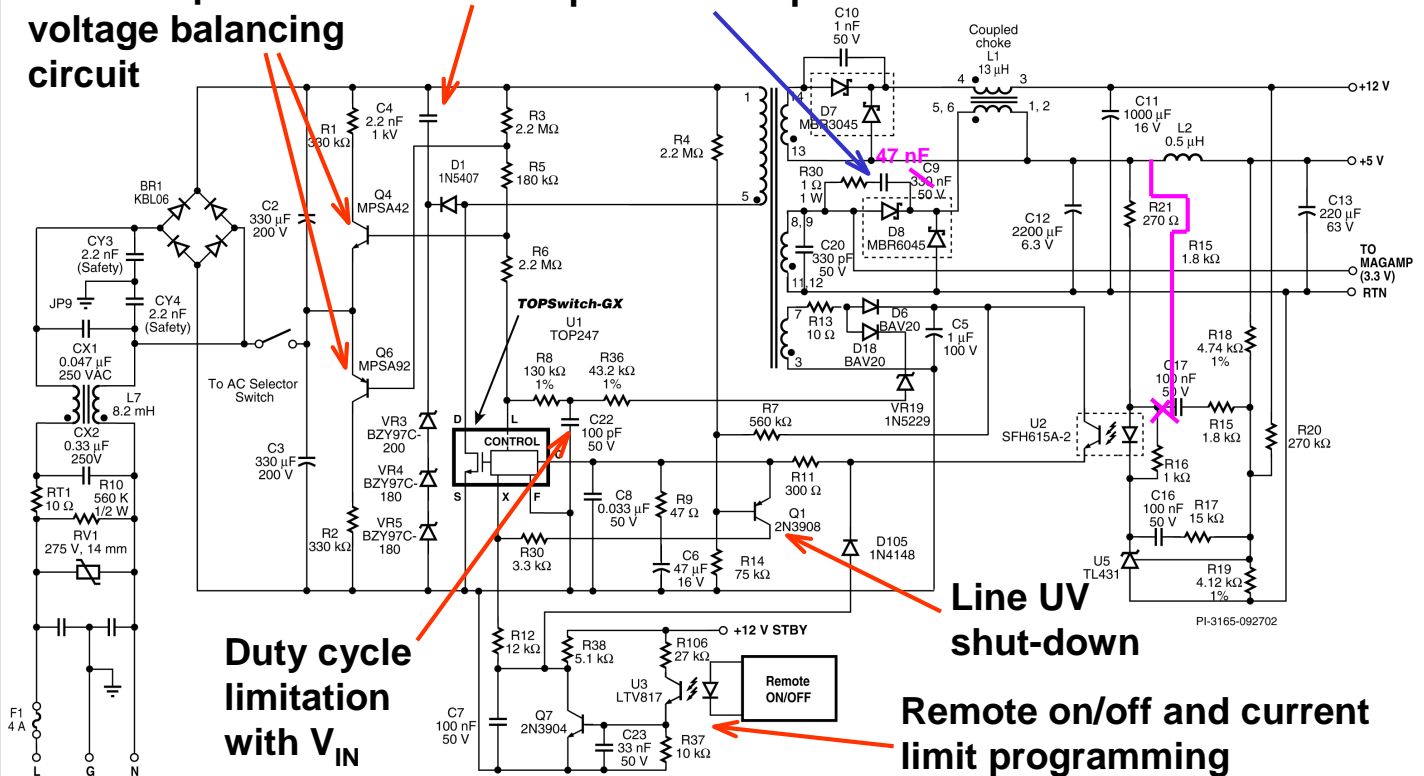


- This supply was designed to fit into an industry standard 145 W ATX case
- Note: the point at which the efficiency is 71% only occurs when the +3.3 V is heavily loaded. For supplies where a higher proportion of power will be drawn from the +12 V output (such as the 180 W SFX 12), the overall efficiency will be substantially higher

# Primary Main Converter Schematic (DI-20)

Active capacitor voltage balancing circuit

Zener capacitor clamp



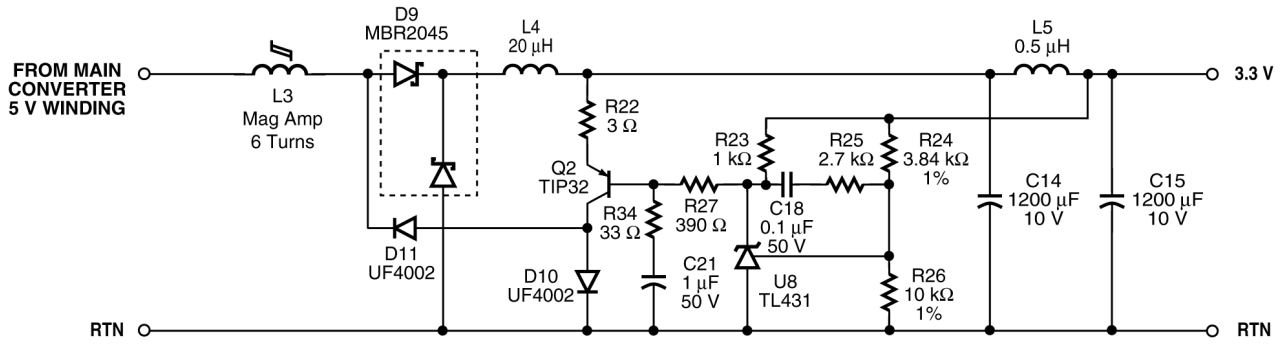
Duty cycle limitation with  $V_{IN}$

Line UV shut-down

Remote on/off and current limit programming

- Active capacitor voltage balancing circuit operates only as needed, minimizing zero load power consumption. Not required if design does not have to meet < 1 W input.
- Line UV shut-down is required for correct power sequencing between main and standby supplies. This ensures the main converter shuts down before the standby converter. For designs without a standby supply this extra circuitry is not required.
- The +12 V output is DC stacked on the +5 V output to improve the voltage centering of the +12 V output

# 3.3 Volt Magamp Schematic (DI-20)



PI-3385-093002

# Load Regulation Performance (DI-20)

Output Voltage	Voltage Range (VAC)	Load Range	Cross Regulation (%)														
			-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	10	15	
3.3 V	90-132/185-265	10 – 100%															
5 V	90-132/185-265	0 – 100%															
12 V	90-132/185-265	4 – 100%															
5 VSB	90-132/185-265	0 – 100%															

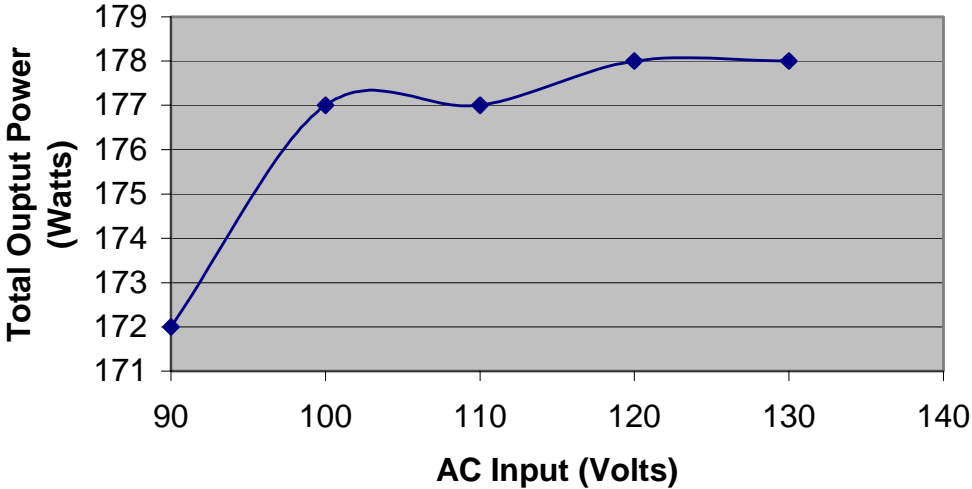
PI-3286-082902

**Excellent cross-regulation achieved through deeply continuous operation and helped by DC-stacking of the 12 V on the 5 V output**



# Overload Performance (DI-20)

Total Output Power (Watts) at Threshold of Over Power Shutdown



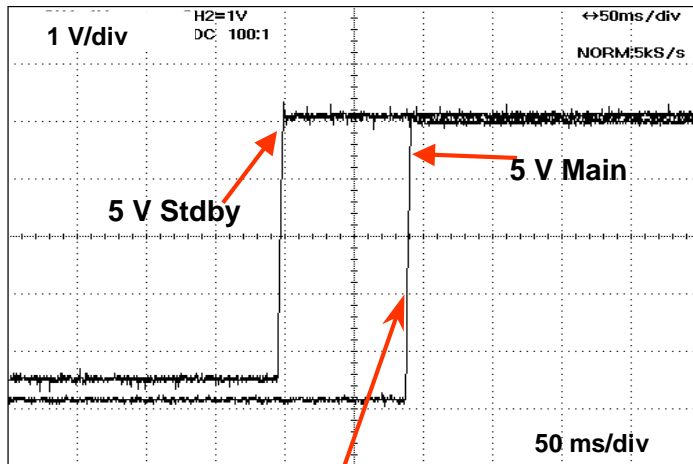
**Power limit is relatively constant with input voltage and load condition due to duty cycle reduction feature**



- Expanded scale chart - overload power only varies with line by ~3%

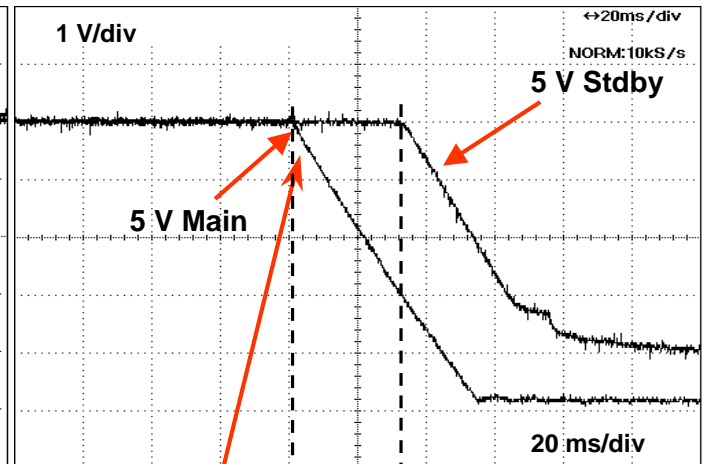
# Power Up/down Sequencing (DI-20)

Relative Start up Timing of  
5 V Standby and 5 V Main



L pin UV  
holds main supply off  
until standby started

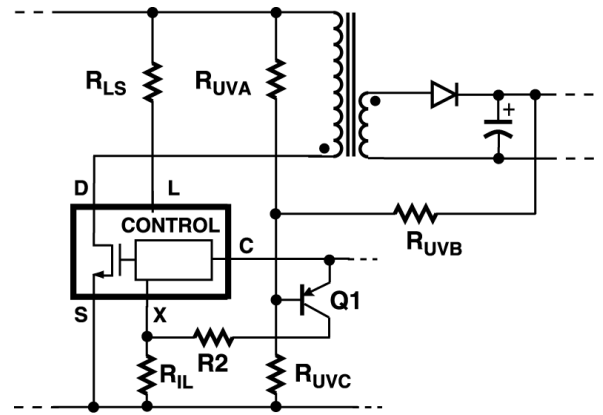
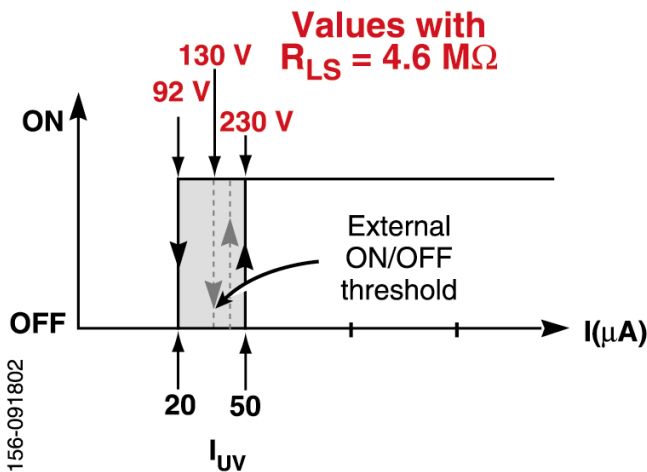
Relative Power down Timing of  
5 V Standby and 5 V Main



X pin UV  
shuts down main  
supply before standby supply

- PC Main power supplies require that the standby supply powers up first, and powers down last
- This design uses an independent external UV circuit to ensure a 17 ms power down delay between the main supply and the standby supply
- The external UV threshold is set to turn off the main power supply just below the minimum voltage needed for hold up time (140 VDC), to shut down the main supply before the standby supply loses regulation during AC turn off

## External Undervoltage using X pin

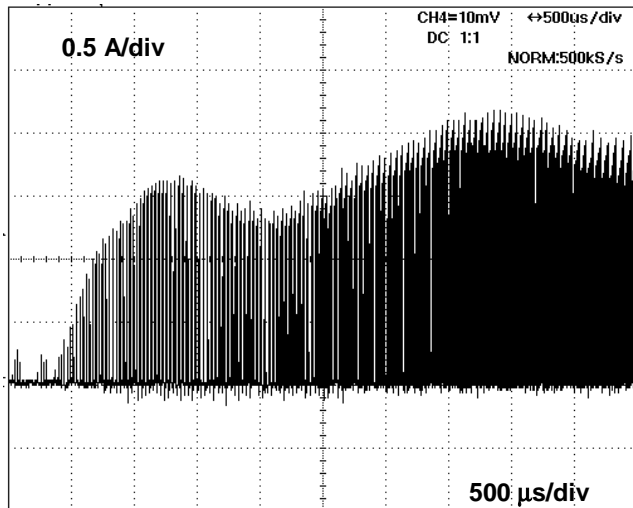


- This circuit uses the control pin voltage minus  $V_{BE}$  of Q1 as a reference to set the UV threshold, independent of the L pin threshold
- When in UV condition, Q1 pulls X pin high to turn off *TOPSwitch-GX*

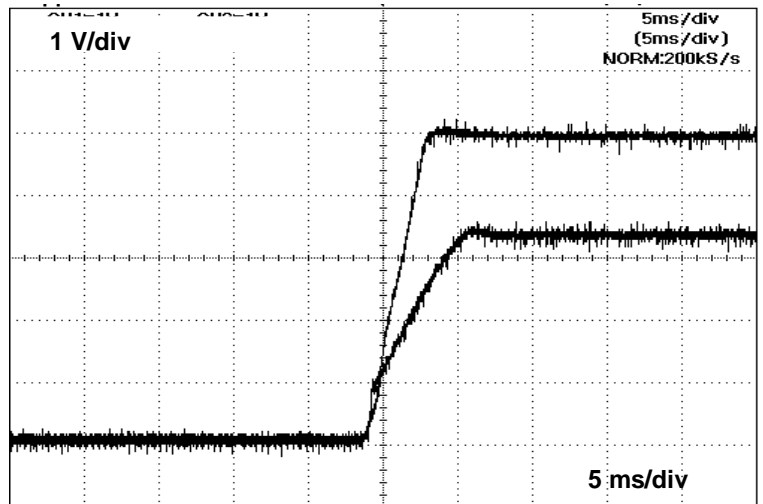
- $R_{UVB}$  gives extra hysteresis to prevent power supply restarting
- Q1 turns off the supply at 130 V to ensure at least 17 ms power down delay between main and standby
- Referencing Q1 to the CONTROL pin provides an accurate UV lockout threshold, since the CONTROL pin voltage is band-gap derived, and temperature compensated

# Drain Current Startup Envelope and Timing (DI-20)

## Drain Current at Start-up

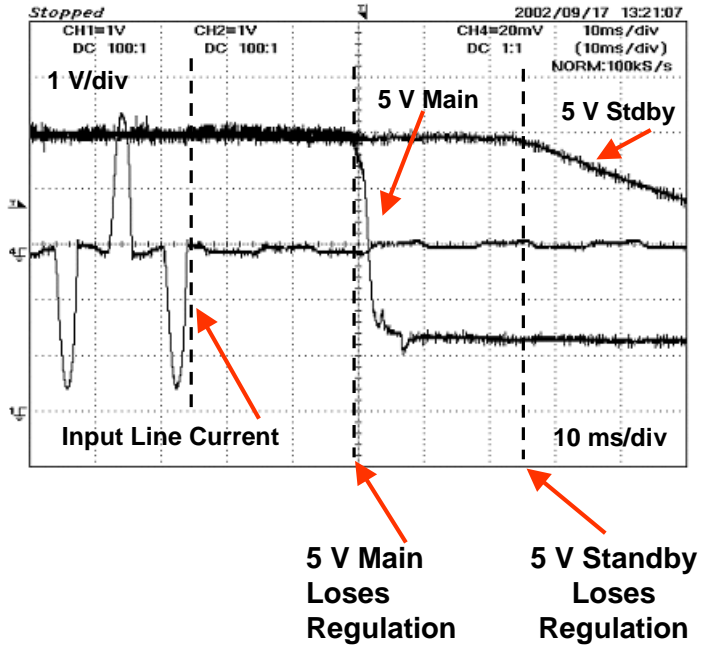


## Relative Timing 3.3 V and 5 V



- Drain current waveform shows how soft start limits duty cycle and peak current during startup

# Holdup Time



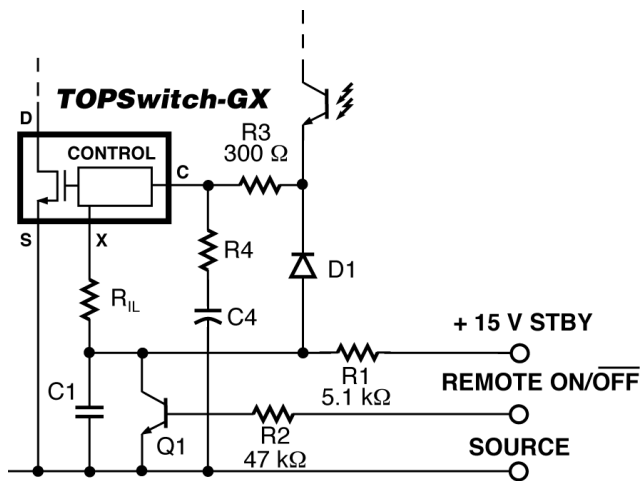
INPUT VOLTAGE	HOLDUP	LOAD
115 VAC LIGHT LOAD	750 ms	3.3 V/0.5 A 5 V/0.4 A 12 V/0.05 A
115 VAC FULL LOAD	24 ms	3.3 V/12 A 5 V/12 A 12 V/3 A
230 VAC LIGHT LOAD	780 ms	3.3 V/0.5 A 5 V/0.4 A 12 V/0.05A
230 VAC FULL LOAD	26 ms	3.3 V/12 A 5 V/12 A 12 V/3 A

PI-3127b-092002

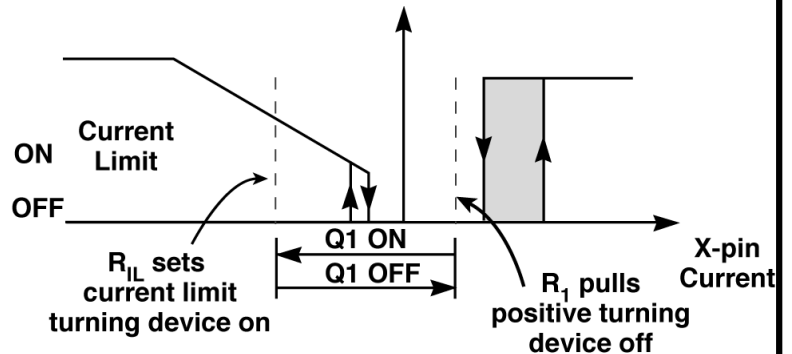


- Meets standard 16 ms low-line holdup time requirement with extra margin

## Meeting 1 W Standby Spec



PI-3224-091702



PI-3189-091702

- External low voltage bias current provided to *TOPSwitch-GX* during remote-off condition.
- External bias current turns off *TOPSwitch-GX* high voltage drain current source, minimizing device power consumption

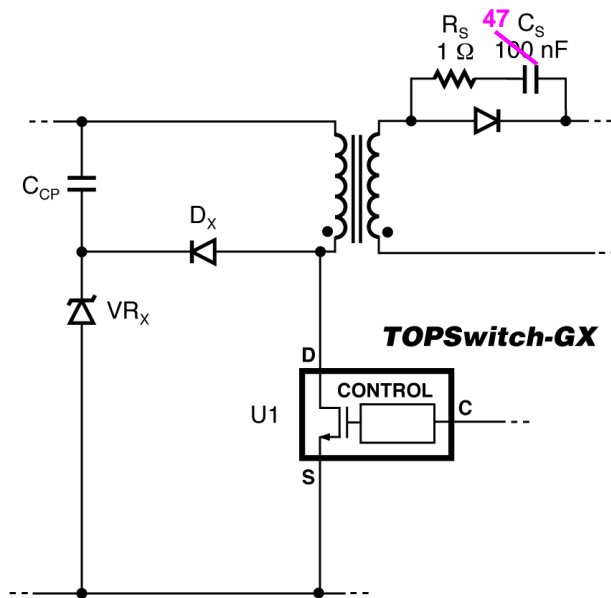
187

Filename: GX Forward 10062004.ppt



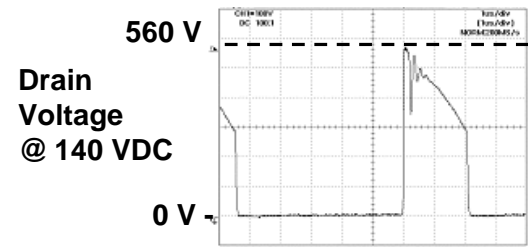
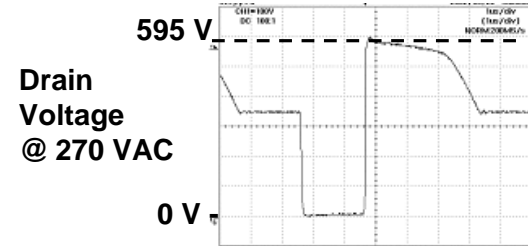
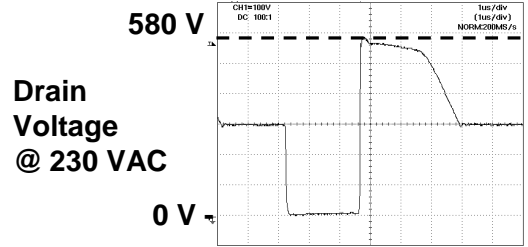
- External low voltage bias current is provided to *TOPSwitch-GX* during remote OFF condition. This turns-off the *TOPSwitch-GX* high voltage drain current source, limiting device consumption from input voltage to approximately 2 mW
- R1, D1 and R3 feed external bias current to *TOPSwitch-GX* turning off drain current source and minimizing device drain consumption
- R<sub>IL</sub> sets the current limit and Q1 turns device ON/OFF via the X pin. C1 provides decoupling
- R4 and C4 are normal CONTROL pin compensation components

# PC Main (DI-20) Drain Voltage



PI-3153-091302

**Worst case drain voltage  
remains below 600 V**

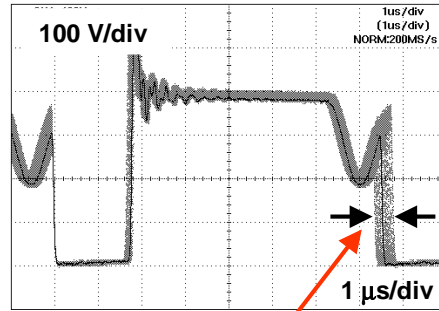
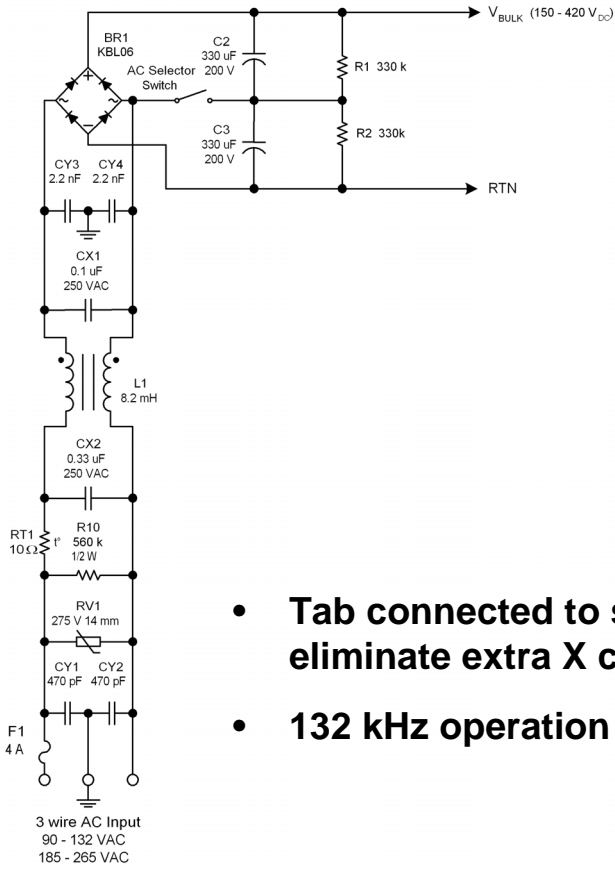


All waveforms: 100 V/div & 1  $\mu$ s/div



- Note the wide duty cycle at low voltage, and low peak drain voltage at all input voltages
- This performance is only possible with *TOPSwitch-GX*'s wide maximum duty cycle,  $DC_{MAX}$  reduction and simple Zener capacitor clamp
- Even at 270 VAC there is still >100 V margin to  $BV_{DSS}$  (700 V)
- (Measured at full load as shown. Also acceptable with 3.3 V output shorted (highest leakage inductance output. Under this condition the drain is clamped by Zener and dissipation limited either by auto-restart or secondary supervisory circuit))

# EMI Filter



$$f_{osc} \pm 4 \text{ kHz}$$

- Tab connected to source and frequency jitter help eliminate extra X cap or Y cap at mains connector
- 132 kHz operation reduces X cap size

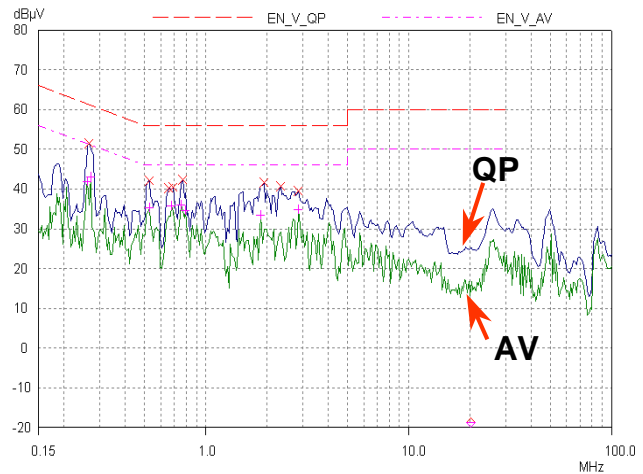
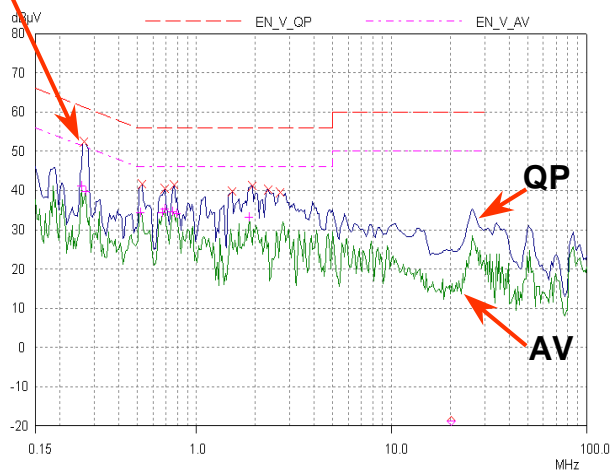
- Only one CM choke required – saves significant cost
- For simplicity only passive resistor balancing is shown

# PC Main (DI-20) - Performance EMI

230 VAC Neutral/Max Load

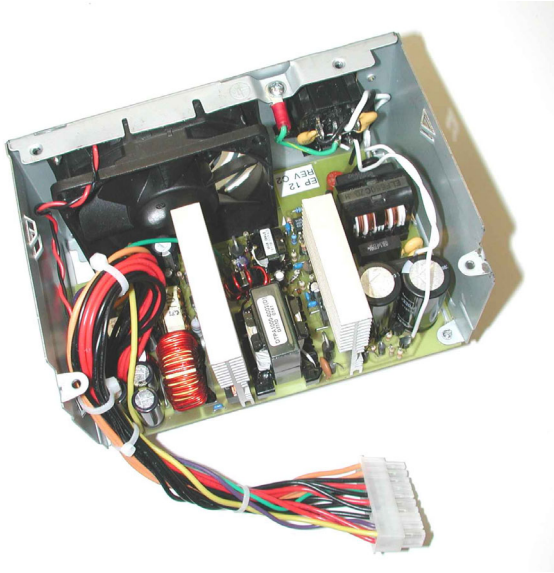
115 VAC Line/Max Load

Controlled by size of X cap



- Note: the value of the input X capacitor determines the height of the differential 2nd harmonic (at 264 kHz)

# PC ATX Power Supply (DI-20) - Summary



- **Low component count**
  - saves 20 to 30 components
- **Meets 1 W specification for standby operation**
- **Simple design both main & standby**
- **High Efficiency (71% at 90 VAC)**
- **Excellent EMI**
- **Built in features**
  - Overload protection
  - Undervoltage
  - Overvoltage
  - Remote on/off

- **DI-20 was designed around a TOP247Y device**
- **The Engineering Report (EPR-12) for this supply is available on the *PI* web site, at [www.powerint.com/appcircuits/htm](http://www.powerint.com/appcircuits/htm)**

## PC SFX12 180 W with Passive PFC Performance (DI-30)

DESCRIPTION	MAIN SUPPLY	STANDBY SUPPLY
Input Voltage (doubled)	185 to 265 VAC 90 to 132 VAC	185 to 265 VAC 90 to 132 VAC
Output Voltage/Current	3.3 V / 0.5 to 17 A 5.0 V / 1.0 to 12 A 12.0 V / 2.0 to 10A (13 Apk) -12V/0 to 0.3A	5 V / 0 to 2 A (2.5 A pk)
Output Power	180 W (200 W pk)	10 W (12.5 W pk)
Efficiency	71%	75%
No-Load Input Power (Output Power)	5 W Blue Angel 1 W Standby 30 W Energy Star	- 4.2 W (2.5 W out) - 0.91 W (0.5 W out) - 23.5 W (15.1 W out)

PI-3129-091802

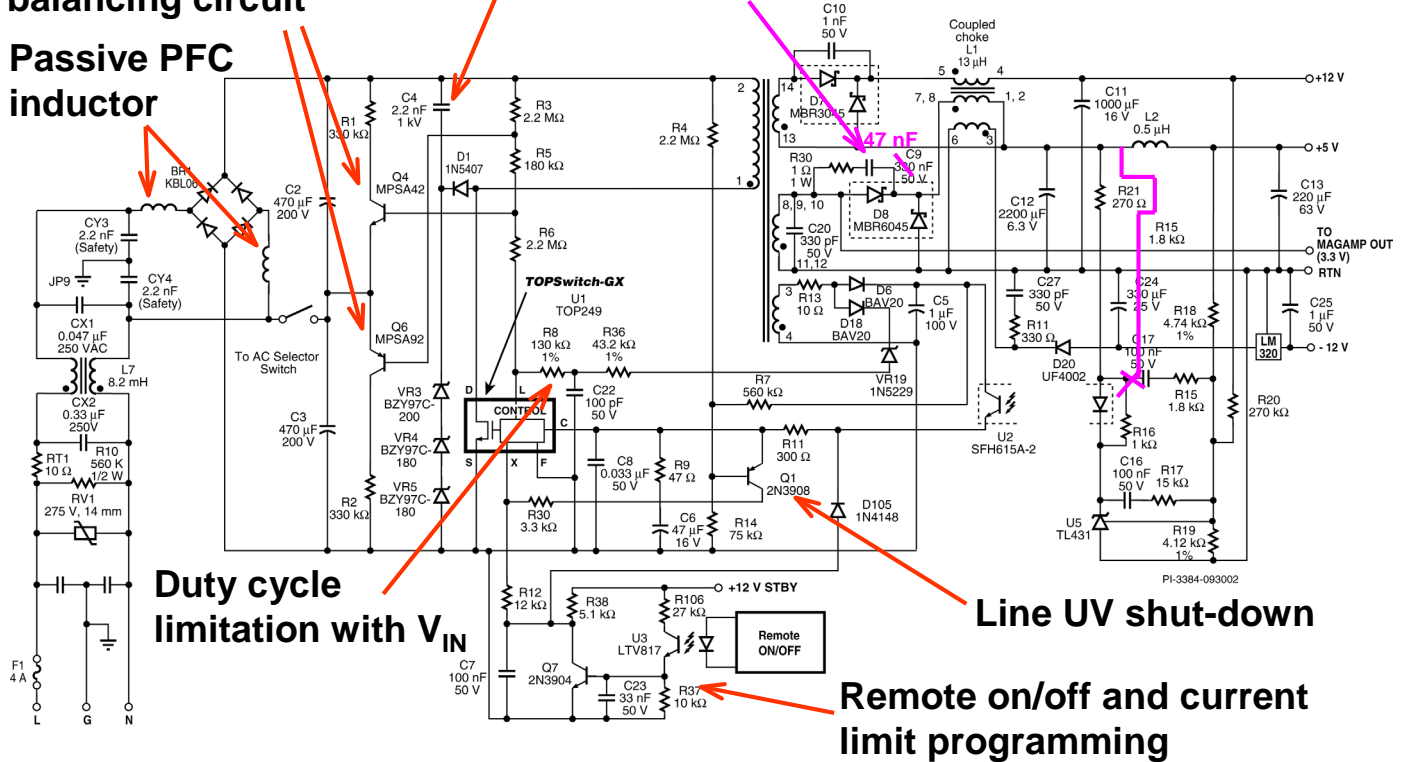
- This 180 W SFX12 PC Main supply fits in an industry standard small form factor case
- Because this supply delivers more power on the +12 V output than it does on its other outputs (compared to an ATX), it is more efficient than an ATX supply, due to the inherently lower  $I^2R$  losses on a 12 V output

# 180 W PC SFX12 Schematic (DI-30)

Active capacitor voltage balancing circuit

Zener capacitor clamp

Passive PFC inductor



Duty cycle limitation with  $V_{IN}$

Line UV shut-down

Remote on/off and current limit programming

- Active capacitor voltage balancing circuit operates only as needed, minimizing zero load power consumption

# Load Regulation Performance (DI-30)

Output Voltage	Voltage Range (VAC)	Load Range	Cross Regulation (%)														
			-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	10	15	
3.3 V	90-132/185-265	3 – 100%															
5 V	90-132/185-265	16 – 100%															
12 V	90-132/185-265	30 – 100%															
-12 V	90-132/185-265	0 – 100%															
5 VSB	90-132/185-265	0 – 100%															

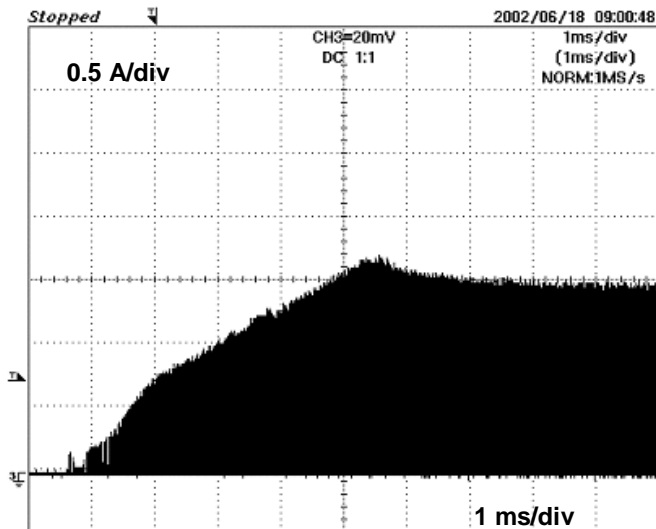
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**Excellent cross-regulation achieved through deeply continuous operation and helped by DC-stacking of the 12 V on the 5 V output**

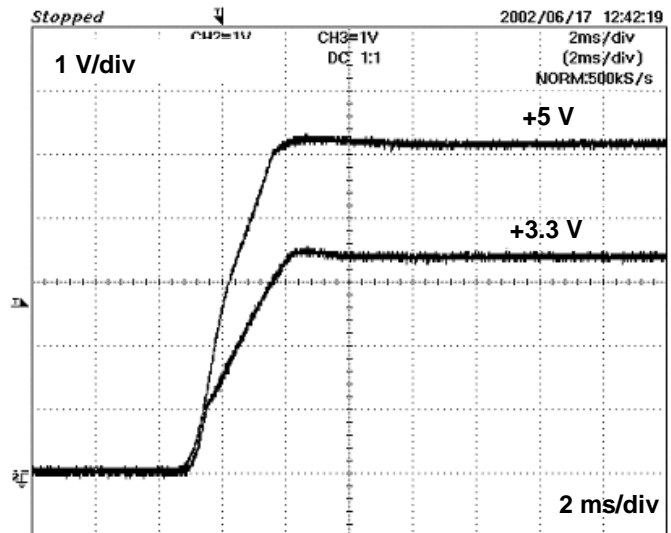


# Drain Current Start up Envelope and Timing (DI-30)

## Drain Current at Start up



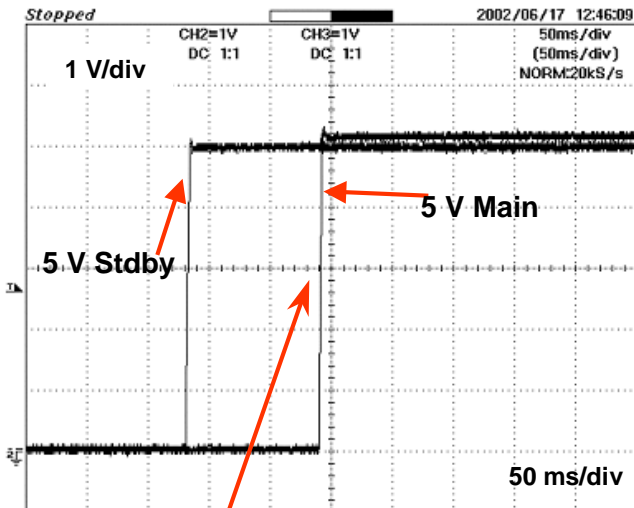
## Relative Timing 3.3 V and 5 V



- Drain current waveform shows how soft start limits duty cycle and peak current during startup
- (Primary Drain Current at Startup, activated from remote On/Off with 120 VAC input +5 V/8 A, +12 V/9 A, +3.3 V/8 A, +5 V standby/1.5 A)
- (+5 V and 3.3 V rise at turn on from remote On/Off, 120 VAC input 5 V/8 A, 3.3 V/8 A, +12 V/9 A, +5 V standby/1.5 A)

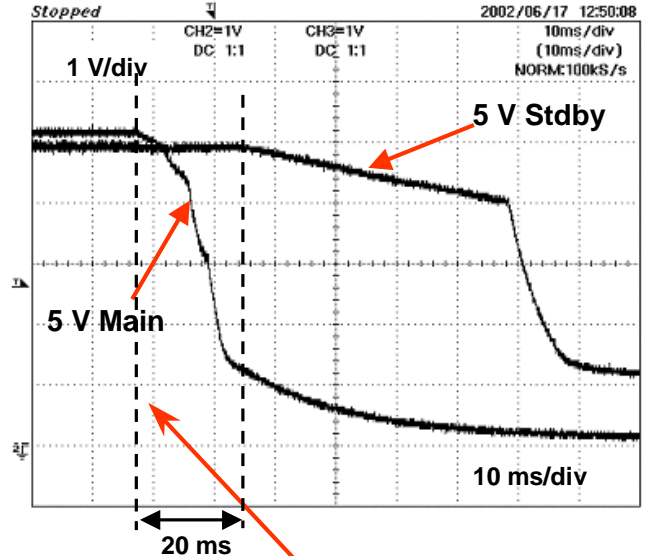
# Power Up/down Sequencing (DI-30)

## Relative Start up Timing of 5 V Standby and 5 V Main



L pin UV holds main supply off until standby started

## Relative Power down Timing of 5 V Standby and 5 V Main

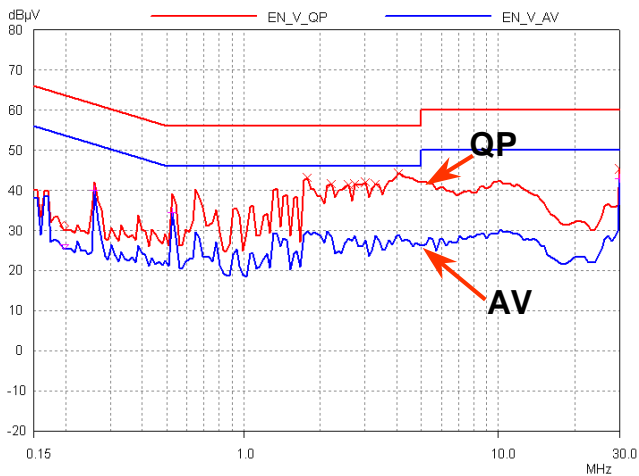


X pin UV shuts down main supply before standby supply

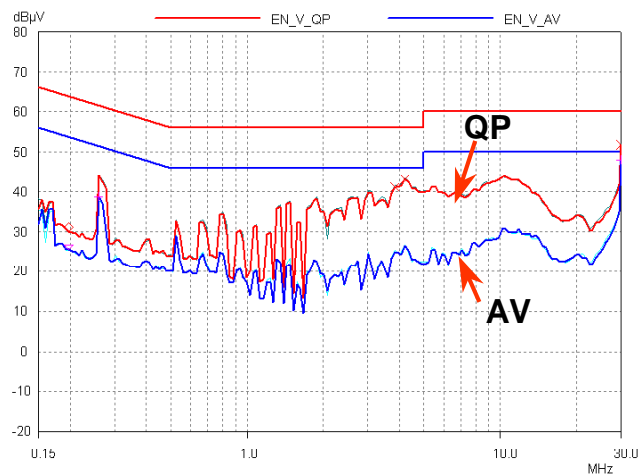
- Standby circuit covered later (see DI-14)
- PC Main power supplies require that the standby supply powers up first, and powers down last.
- This design uses an independent external UV circuit to ensure a minimum 17 ms power down delay between main and standby.
- The external UV threshold is set to turn off the main power supply just below the minimum voltage needed for hold up time (140 VDC), to shut down the main supply before the standby supply loses regulation during AC turn off.
- (5 V main and 5 V standby startup (120 VAC) Max load on all outputs)
- (+5 V and +5 V standby drop out after AC Off Max load on 5 V standby, min load on all other outputs)

# 180 W PC SFX12 (DI-30) - Performance EMI

230 VAC Neutral/Max Load



115 VAC Line/Max Load



- (230 VAC Line Input, +5 V/8 A, +5 V standby/1.5 A, +12 V/9 A, +3.3 V/8 A)
- (115 VAC Line Input, +5 V/8 A, +5 V standby/1.5 A, +12 V/9 A, +3.3 V/8 A)

# 180 W PC SFX12 Power Supply (DI-30) Summary



- **Low component count**
  - saves 20 to 30 components
- **Meets 1 W specification for standby operation**
- **Simple design, both main & standby**
- **High Efficiency (71% at 90 VAC)**
- **Excellent EMI**
- **Built in features**
  - Short circuit and open loop protection
  - Under-voltage lockout
  - Over-voltage shutdown
  - Auto-recovering thermal shutdown
  - Remote on/off capability

- **DI-30 is able to deliver 180 W, from an SFX form factor, with passive PFC**
- **The 180 W PC Mains supply was designed around a TOP249Y device**
- **Using a *TOPSwitch-GX* device significantly cost reduced the supply's EMI filter**
- **The Engineering Report (EPR-31) for this supply is available on the *PI* web site, at [www.powerint.com/appcircuits/htm](http://www.powerint.com/appcircuits/htm)**

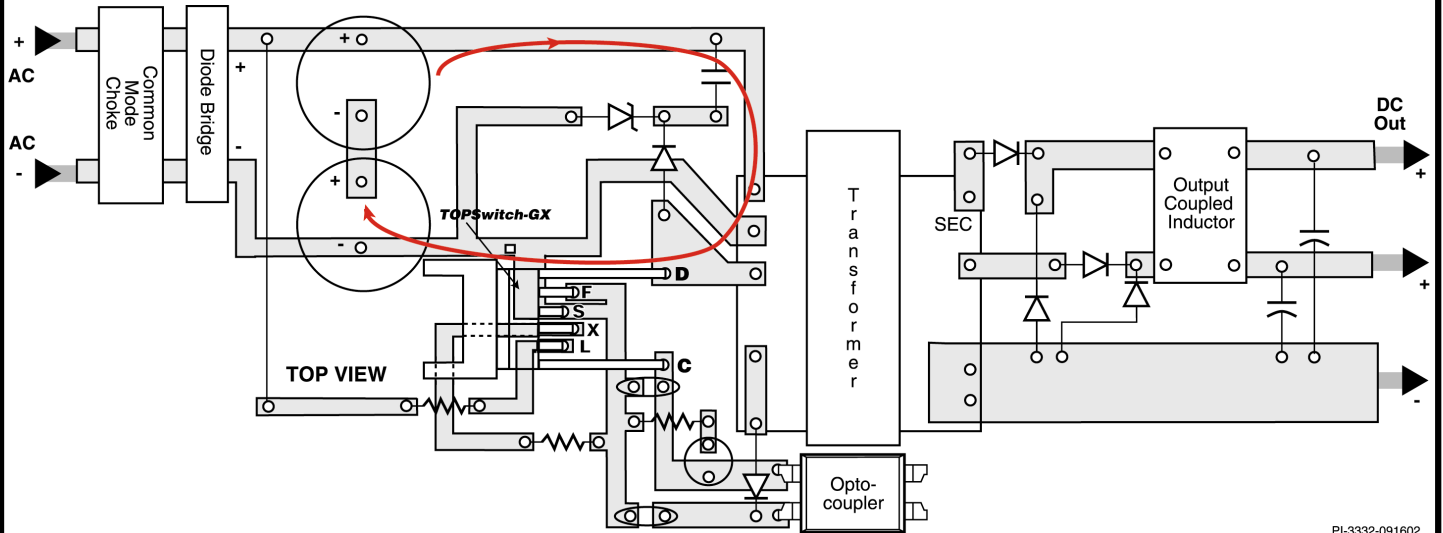
## Forward Hints & Tips

- **Maintain continuous mode operation over normal load range**
  - Swinging inductor allows continuous mode operation at light load
  - Swinging inductor has inductance that increases at low current
- **Keep the peak reset voltage < 90 % of  $BV_{DSS}$  (700 V), with sufficient margin for component tolerances**
  - Ensure that  $V_{RESET}$  is sufficient to reset the core each switching cycle
- **Use a zero gap transformer to limit leakage & maximize magnetizing inductance**
  - Use recommended clamp scheme to allow recovery of leakage & magnetizing energy

- **The inductance value of a swinging inductor varies with the amount of current that is flowing through it. This allows the converter to stay in the continuous conduction mode (CCM) at light loads**
  - The inductance of a swinging inductor is very high at low current
  - The inductance of a swinging inductor drops as the current through it increases

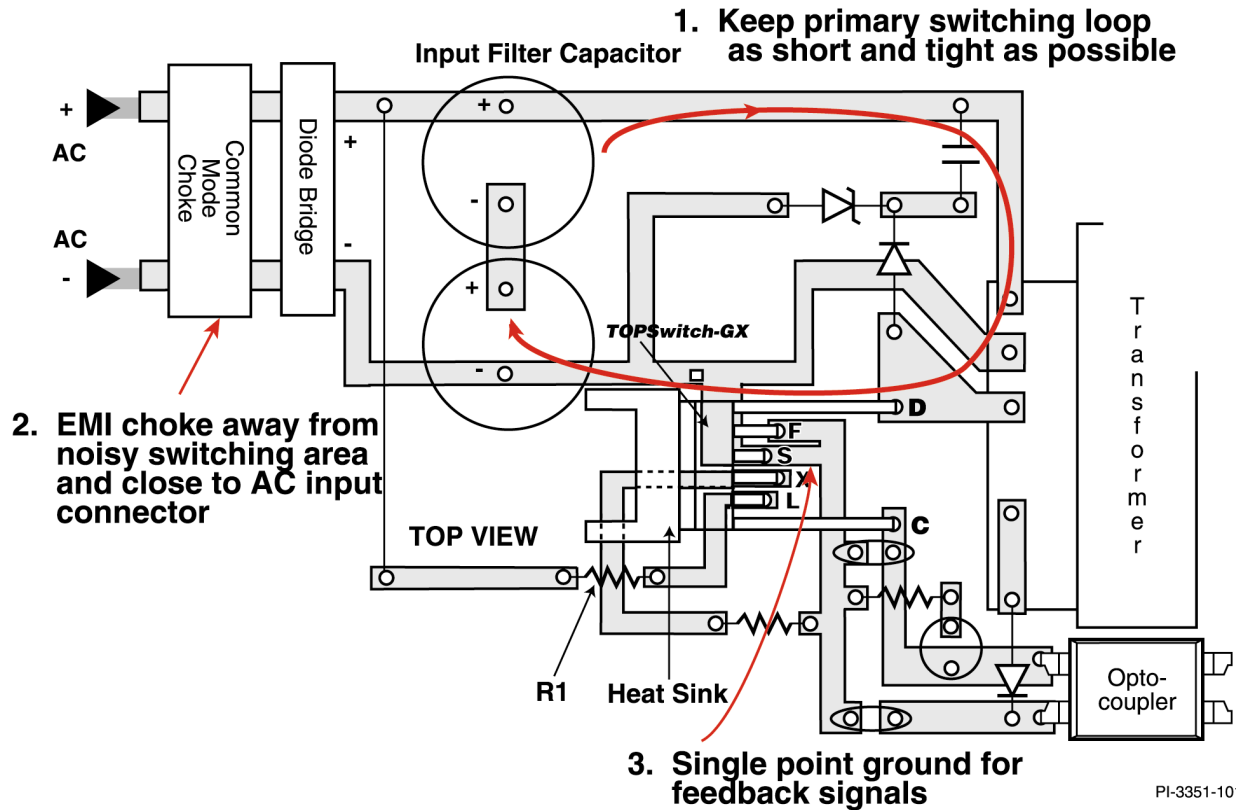
# TOPSwitch-GX - Layout Considerations

- TOPSwitch-GX is a precision, monolithic, high-current power IC
- Layout is critical for the IC to perform optimally



PI-3332-091602

# Primary Side Layout Considerations

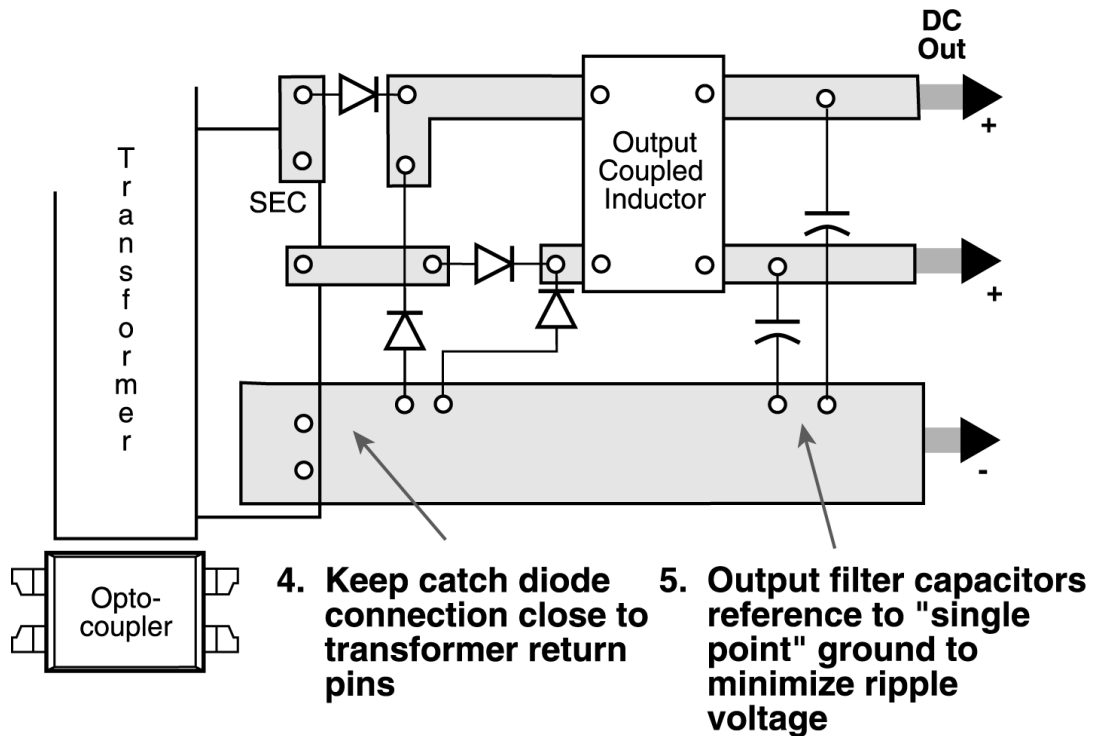


PI-3351-101802



- Additional guidelines for PCB layout are given in the *TOPSwitch-GX* Basics seminar

# Secondary Side Layout Considerations



PI-3352-102202



- Additional guidelines for PCB layout are given in the *TOPSwitch-GX* Basics seminar



**Thank you for attending our Seminar**