Design Example Report

Title	**52 W Nominal and 82 W Peak Power Multi-Output Flyback Converter with One CV and One CC Using InnoMux-2™-EP IMX2268C**
Specification	90 VAC – 265 VAC Input; 12 V / 2 Anm / 4.5 Apk, 60 V – 75 V / 380 mA Outputs
Application	32” TV PSU
Author	Applications Engineering Department
Document Number	DER-714
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Summary and Features

Unique single-stage conversion, multiple-output, flyback architecture enabling:

- High efficiency across the universal line range
- High regulation accuracy - independently regulated 12 V / 2 A nominal and 4.5 A peak CV output
- One CC (LED) output with wide string voltage range of 60 V to 75 V
- Configurable for
  - Analog dimming mode
  - Straight PWM dimming mode
  - Filtered PWM dimming mode
  - Hybrid dimming mode
- Safety features
  - Output overvoltage protection (OVP), eliminating the need for a fault protection optocoupler
  - Output power limit set independently for each output
  - Accurate thermal protection with hysteretic shutdown
  - Input voltage monitor with accurate brown-in/brown-out and overvoltage protection
- Audible noise is 24 dBA in operation mode, and 19 dBA in standby mode

InnoMux-2 is the industry first single chip AC/DC with isolated, safety-rated integrated multiple feedbacks. In addition, the pulse sharing significantly reduce the audible noise to allow it being used in quiet appliance.

The control chip incorporates isolated feedback and communication channels, combining all the benefits of secondary-side control with the simplicity of primary-side regulation.

The new architecture achieves tight cross regulation across multiple outputs and high overall efficiency while simplifying the overall system by obviating the need for post-regulation. The single-stage converter reduces board size significantly and reduces the part count compared to the equivalent conventional converter based on multiple conversion stage topology.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a Switch Mode Power Supply (SMPS) intended for TV applications. The SMPS, utilizes the Power Integration's InnoMux-2 controller. The controller implements a multiplexing power control algorithm.Energy stored in the primary winding of the transformer during primary conduction interval is subsequently delivered to only one of the converter's main outputs (CV1 or LED). More specifically, this is achieved by controlling the switch SW1 (Figure 1).Utilizing a single magnetic component (transformer TX 1), the controller directs the energy flow as needed to all outputs based on respective loading requirements, thus keeping each output accurately controlled. If the energy pulse needs to be delivered to the CV1 output, SW1 is turned ON prior to the end of the primary conduction interval. Otherwise , if SW1 is OFF, the energy is delivered to the LED output via the rectification diode D1.

The SMPS has one Constant Voltage (CV) outputs, 12 V / 2 Anm / 4.5 Apk and a single string Constant Current (CC) output, capable of delivering maximum of 0.38 A current into an LED stack with voltage from 60 V to 75 V. The current through the LED stack is controlled from zero to maximum by 2 PWM dimming signals (DIM1 and DIM2). The Power Supply Unit (PSU) can deliver total maximum continuous output power of 52 W and peak output power of 82 W, with universal mains input (from 90 VAC to 265 VAC).

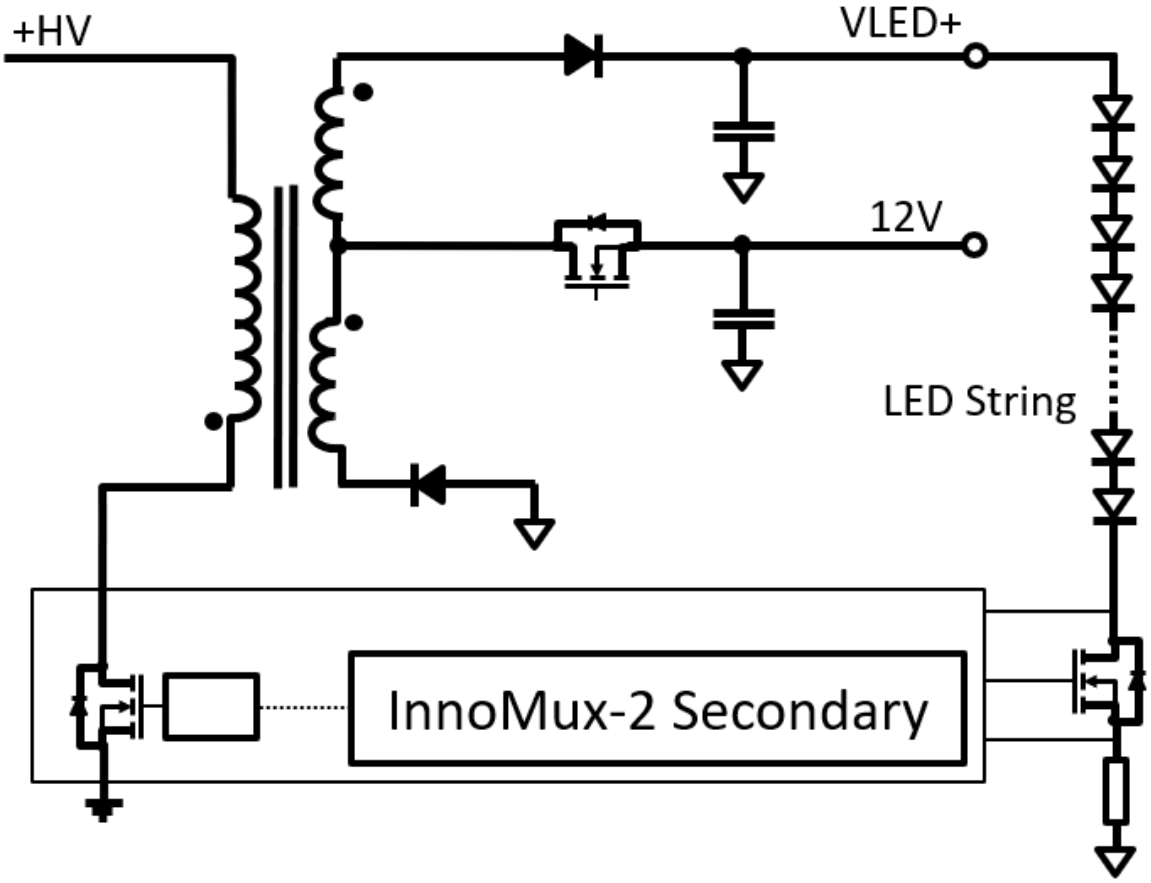


Figure 1 – DER-714 High Level Schematic.

The VCV1 & VLED pins continuously sense the output voltages. If the voltage of any of the outputs drops below regulation level, the multi-output controller InnoMux-2 sends a request for pulse to primary-side controller. This type of pulse-by-pulse regulation results in quick response and excellent cross regulation. For the described multiplexing algorithm to work correctly, it is essential that the reflected voltage of each winding must be higher than that of the preceding lower output voltage winding in order to effectively steer the power:

$$\frac{V_{CV1}}{N_{C1}} < \frac{V_{LED}}{N_{C1} + N_{LED}}$$

Transformer with stacked or independent secondaries may be used as appropriate. The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. The actual performance is illustrated in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 / 3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	11.4	12	12.6	V	±5%.
Output Ripple Voltage 1	$V_{RIPPLE1}$			120	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		2	A	
Output Peak Current 1	I_{OUT1_PK}		4.5		A	
LED Voltage	V_{OUT2}	60	72	75	V	
LED Current	I_{OUT2}	0	0.38	0.38	A	
Total Output Power						
Continuous Output Power	P_{OUT}		52		W	
Efficiency						
Full Load	η	85			%	Measured at 115 / 230 VAC, POUT 25 ºC.
No-Load Input Power				<0.3	W	Measured at 230 VAC 25 ºC, 12 V 10 mA, STDBY Pin Pulled Low.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety						
Surge Common Mode				2	kV	Combination Wave, 12 Ω Common Mode.
Surge Differential Mode				1	kV	Combination Wave, 2 Ω Differential Mode.
ESD		±2		±15	kV	Air Discharge.
		±2		±8		Contact Discharge.
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

3 Schematic

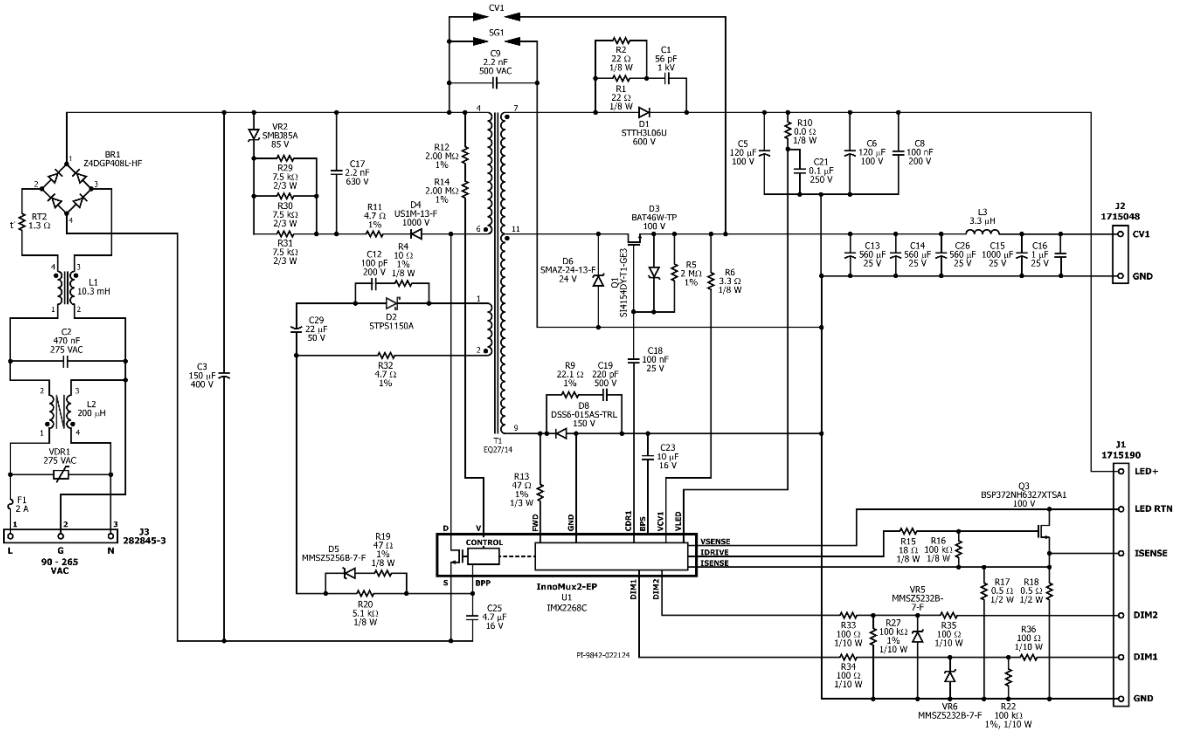


Figure 2 – Schematic.

4 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 800V, 4A, Z4-D	Z4DGP408L-HF	Comchip Technology
2	1	C1	56 pF,±5%, 1000V (1kV), Ceramic Capacitor C0G, NP0, 1206	C1206C560JDGAC7800	Kemet
3	1	C2	470 nF, 275 VAC, Film, X2	PX474K31D5	Carli Electronics
4	1	C3	150 uF, 400 V, Electrolytic, (18 x 45)	UPT2G151MHD	Nichicon
5	2	C5 C6	120 uF, 100 V, Electrolytic, Gen. Purpose, (12.5 x 20)	UHE2A121MHD6	Nichicon
6	1	C8	100 nF, 200 V, Ceramic, X7R, 1206	C1206C104K2RACTU	Kemet
7	1	C9	2200PF,±20%, 500VAC (Y1),760VAC (X1), Ceramic, Y5U	440LD22-R	Vishay
8	1	C12	100 pF, 200 V, Ceramic, COG, 0805	08052A101JAT2A	AVX Corp
9	3	C13 C14 C26	560 uF, 25 V,±20%, Al Organic Polymer, Gen. Purpose	A750MS567M1EAAE015	KEMET
10	1	C15	1000 uF, 25 V, Electrolytic, Gen. Purpose, (10 x 20)	EKMG250ELL102MJ20S	Nippon Chemi-Con
11	1	C16	1 uF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
12	1	C17	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK Corp
13	1	C18	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX Corp
14	1	C19	220pF, ±5%, 500V, Ceramic Capacitor, X7R, 0805	C0805C221JCRAC7800	Kemet
15	1	C21	0.1 uF, 250V, ±10%, Ceramic, X7R, 1206	C3216X7R2E104K160AA	TDK Corporation
16	1	C23	10 µF, ±10%, 16V, X7R, Ceramic Capacitor,MLCC 0805	CL21B106KOQNNNE	Samsung
17	1	C25	4.7 uF, ±10%, 16 V, Ceramic, X7R, 0805	GRM21BR71C475KE51L	Murata
18	1	C29	22 uF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
19	1	D1	Diode 600 V 3A Surface Mount SMB	STTH3L06U	STMicroelectronics
20	1	D2	Diode, 150 V, 1A, Surface Mount DO-214AC, SMA	STPS1150A	STMicroelectronics
21	1	D3	DIODE, SCHOTKY, 100V, 0.075A, SOD123	BAT46W-TP	Micro Commercial
22	1	D4	Diode, Avalanche, 1000 V, 1.5A, (SMA)	US1M-13-F	Diode Inc.
23	1	D5	DIODE ZENER 30V 500MW SOD123	MMSZ5256B-7-F	Diodes, Inc
24	1	D6	Zener Diode, 24 V,1 W, ±5%, (SMA)	SMAZ24-13-F	Diodes Incorporated
25	1	D8	Diode 150 V 6A DPak (2 Leads + Tab)	DSS6-015AS-TRL	IXYS
26	1	F1	2 A,250V, Slow, TR5	37212000411	Wickman
27	1	J1	6Position (1 x 6) header, 5 mm (0.196) pitch, Vertical, Screw	1715190	Phoenix Contact
28	1	J2	4 Position (1 x 4) header, 5 mm (0.196) pitch, Vertical, Screw	1715048	Phoenix Contact
29	1	J3	3 Position Wire to Board Terminal Block0.300" (7.62mm)	282845-3	TE Connectivity AMP Connectors
30	2	JP1 JP2	Wire Jumper, Non insulated, 20 AWG, 0.2 in	8020 000100	Belden
31	1	L1	CMC 10.3MH 2.0A 0.15OHM WIDE IMP	SSR21NVS-M20103	KEMET
32	1	L2	200 uH @ 100kHz, Common Mode Choke	30-00512-00	Power Integrations
33	1	L3	FIXED IND, 3.3UH, ±20%,5.2A, 16 MOHM, TH	ELC10D3R3E	PANASONIC ELECTRONIC

34		MTG_HOLES	Mounting Hole M 4		
35	1	Q1	MOSFET,N-Channel, 40V, 36A (Tc), 3.5W (Ta), 7.8W (Tc), 8-SO	SI4154DY-T1-GE3	Vishay Siliconix
36	1	Q3	MOSFET, N-Channel, 100 V ,1.8A (Ta), 1.8W (Ta),SOT223	BSP372NH6327XTSA1	Infineon Technologies
37	2	R1 R2	RES, 22 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ220V	Panasonic
38	1	R4	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
39	3	R5 R12 R14	RES, 2.00 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
40	1	R6	RES, 3.3 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ3R3V	Panasonic
41	1	R9	RES, 22.1 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF22R1V	Panasonic
42	1	R10	RES, 0 R, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole Electronics Inc
43	2	R11 R32	RES, 4.7 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8RQF4R7V	Panasonic
44	1	R13	RES, 47 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
45	1	R15	RES, 18 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ180V	Panasonic
46	1	R16	RES, 100 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
47	2	R17 R18	RES, 0.5 R,1%,0.5W, 1/2W, Thick Film, -55°C ~ 155°C,1206	RL1206FR-7W0R5L	YAGEO
48	1	R19	RES, 47 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
49	1	R20	RES, 5.1 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
50	2	R22 R27	RES,100 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603	RC0603FR-07100KL	Yageo
51	3	R29 R30 R31	RES, 7.5 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7501V	Panasonic
52	4	R33 R34 R35 R36	RES,100 Ohms ±5% 0.1W, 1/10W Chip Resistor 0603	RC0603JR-07100RL	Yageo
53	1	RT2	NTC Thermistor, 1.3 Ohms, 7 A	MF72-001.3D13	Cantherm
54	1	T1	Bobbin, EQ27/14, 11 pins, 6pri, 5sec	YT-2701	www.dgytdz.com
55	1	U1	MINNO-2 test symbol with 24 pins and EP	IMX2268C	Power Integrations
56	1	VDR1	275 Vac, 45 J, 10 mm, RADIAL	V275LA10P	Littlefuse
57	1	VR2	137V Clamp, 4.4A Ipp, Unidrirectional TVS Diode(SMBJ)	SMBJ85A	Littelfuse
58	2	VR5 VR6	DIODE ZENER 5.6V 500MW SOD123	MMSZ5232B-7-F	Diodes, Inc

5 PCB Assembly

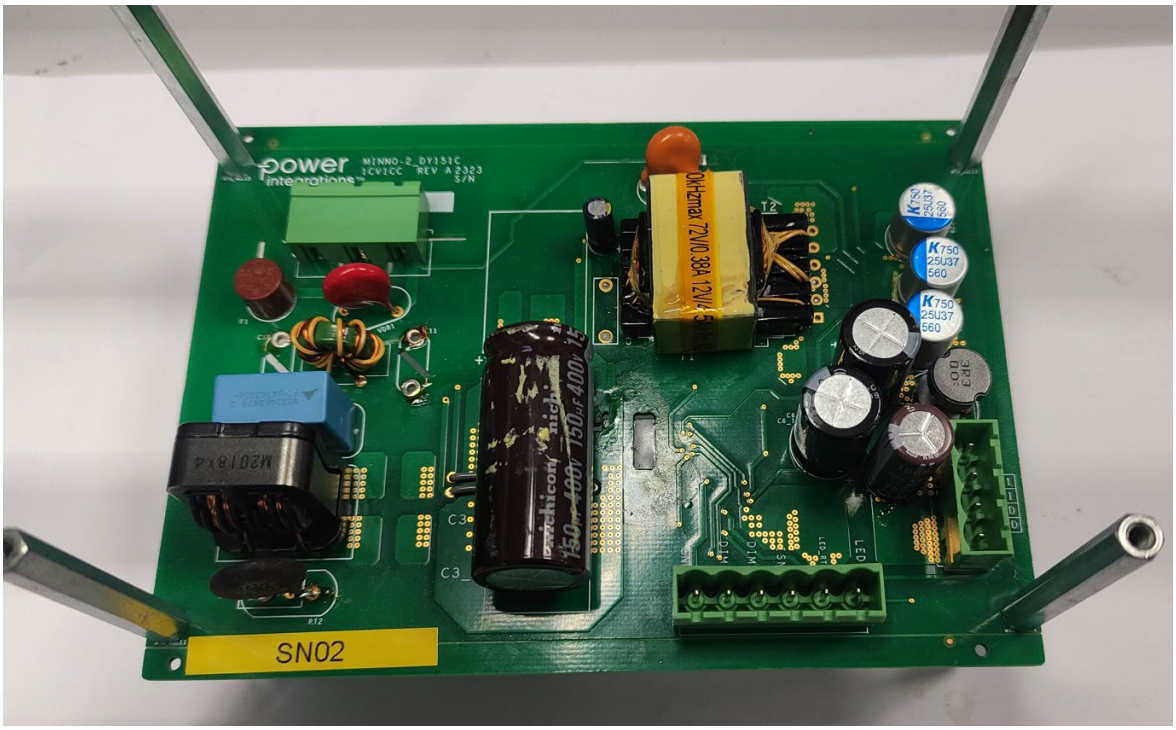


Figure 3 – PCB, Top View.

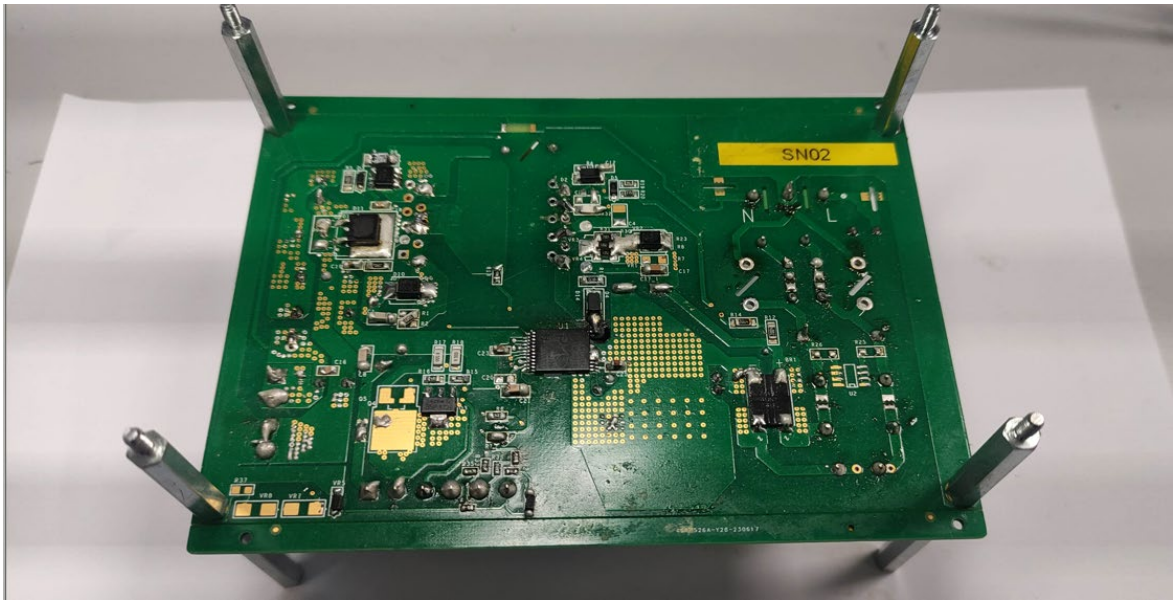


Figure 4 – PCB, Bottom View.

6 Circuit Description

6.1 Input Rectifier and EMI Filter

Fuse F1 isolates the circuit and provides protection from component failure, and the common mode chokes L1 and L2 with capacitor C2 attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC voltage across the filter capacitor C3.VDR1 provides protection against differential voltage surges. Resistor RT2 (NTC) limits the inrush current. Capacitor C9 is used to mitigate the common mode EMI.

6.2 Primary-Side

6.2.1 Primary Switch Arrangements

The transformer primary is connected between the input DC bus (TXPRI+) and the drain D of the integrated primary switch of InnoMux-2 (U1 pin 24).

A Zener type primary clamp (R11,R29,R30,R31,VR2,C17,D4) is used to limit the peak drain voltage of U1 at the instant of turn-off of the switch inside U1.

6.2.2 Primary-Side Controller Power Source and OVP Protection

The primary-side controller is part of the InnoMux-2 (U1). It is self-starting, using an internal high-voltage current source to charge the BPP capacitor C25, when AC voltage is first applied to the converter input. During normal operation (steady-state) the primary-side of the controller is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D2 and capacitor C29, and then connected to the BPP pin via a current limiting resistor R20.

6.2.3 Primary-Side OVP, Brown-In and Brown-Out Protection

A crude primary-side output overvoltage protection (OVP) is implemented by Zener diode D5 and the series resistor R19. In the event of an uncontrolled overvoltage at the output, the auxiliary winding voltage increases and causes breakdown of D5 which then causes a current to flow into the BPP pin of IC U1. If this current exceeds I_{SD} threshold, InnoMux-2 controller will latch off and prevent any further increase in output voltage.

Resistor R12 and R14 provide input voltage sense protection for under voltage and over voltage conditions.

6.2.4 Primary Peak Current Limit

The value of capacitor C25 is used to set the maximum primary current to STANDARD or to INCREASED level. In this case 4.7 μF capacitance sets the primary-side controller peak current limit to its INCREASED level of 2.6 A.

6.3 Secondary-Side

The secondary-side of the InnoMux-2 (U1) is powered from the 5 V BPS rail generated internally. Capacitor C23 is a local decoupling capacitor.

6.3.1 Primary to Secondary-Side Communication

The secondary-side of the InnoMux-2 (U1) sends a request to the primary-side controller to initiate a switching cycle, by sending a pulse via the internal FluxLink, a galvanically isolated communication channel.

6.3.2 InnoMux-2 Power Supply

During start-up the InnoMux-2 secondary-side controller is powered from LED rail via R10 or from FWD pin. There is a local decoupling capacitor C21 connected close to the VLED pin of U1. R10 and C21 are optional. An internal regulator reduces the LED+ voltage to 5 V and outputs it to the BPS bus (U1 pin 6).

In steady-state the voltage on VCV1 (U1 pin 10) exceeds $VCV1_{MIN}$ (7.4 V to 9.3 V). The internal BPS regulator input is switched from VLED to VCV1 pin to reduce power dissipation in the regulator. R6 and C20 are optional. They provide local decoupling as well as ESD protection.

6.3.3 Selection MOSFET Drive

The gate drive amplitude for the selection MOSFET Q1 is approximately equal to the voltage on the BPS rail (5 V). Consequently, logic level MOSFETs are used. Capacitor C18 is charged up to the level of the V_{CV1} from the CV1 via diode (D3) to the CDR1 pin. When the selection MOSFET needs to be gated on, CDR1 pin voltage is raised from GND to BPS, and the selection MOSFET gate voltage (the other terminal of the capacitor C18) is lifted to $V_{CV1}+V_{BPS}$.

The secondary control circuit in InnoMux-2 needs access to the idle ring waveform in order to calculate the its timing and facilitate valley switching. Such access is ensured through the FW pin by keeping Q1 on after the secondary conduction time has expired.

6.3.4 Output Control

Output rectification for the CV1 output is provided by the diode (D8) and the CV1 selection MOSFET (Q1). A Π – type LC filter (C13, C14, C26, C15 and L3) ensures low output ripple voltage. The first stage filter capacitors C13, C14, C26 have low ESR to minimize the switching noise.Small multilayer ceramic (MLCC) capacitor C16 is connected across the CV1 output terminals and provide low impedance bypass for any high frequency noise components.

Output rectification for the LED output is provided by diodes (D8 and D1). Capacitors C5 and C6 is used to provide energy storage and filtering at the LED output.

The RC snubber network R1, R2 and C1 damps high-frequency ringing across the rectifier diode D1.

The RC snubber network R9 and C19 damps high-frequency ringing across the rectifier diode D8.

Zener diode D6 is used as a voltage clamp for the transformer CV1 winding.

Zener diodes VR7 , VR8 and R37 can be used for to limit the maximum LED voltage which can be predominantly caused by the leakage in the transformer.VR7,VR8 and R37 are optional and not populated in this DER.

When the Selection MOSFET (Q1) is turned off and the SR diode (D8) is conducting, the voltage on the anode of D1 rises until it is forward biased. In this condition, all the transformer energy is directed to the LED output.

When the selection MOSFET (Q1) on, the transformer secondary windings are designed such that the voltage on the anode of D1 is below the lowest working LED string voltage. Therefore D1 will remain reverse biased and all the transformer energy is directed to the CV1 output via Q1.

The set point for the CV1 output is determined by the internal code settings, CV1 voltage is monitored via a feedback signal to the VCV1 pin of InnoMux-2.

LED+ output maximum voltage is set by the internal code. In this design it has been set to the default value 80 V. Note that the actual LED+ voltage is not set by the code and it varies depending on the LED stack voltage and the drain voltage (VSENSE) on the LED driver MOSFET (Q3).

6.3.5 LED Current Control and Dimming

The maximum LED current is set by the resistor values of R17 and R18. The application is configured for 2-wire filtered PWM dimming mode. The maximum current through the LED stack is 400 mA. It is achieved at 100% Duty Cycle on both DIM1 and DIM2.

R33,R34,R35,R36,R22,R27,VR5 and VR6 are DIM1 and DIM2 external circuitries.

Other dimming options are available, such as PWM, Analog and 1-wire dimming. For details, please see latest data sheet for InnoMux-2 on the Power Integrations website.

6.3.6 Output Power Limiting

A power limit is implemented individually for each output using the internal trim code in InnoMux-2 (U1). The power delivered to any of the outputs is restricted by limiting the maximum average frequency at which an output can receive. The frequency limit is set by the trim code bits PLIM1 and PLIM2. Namely, PLIM1 bits set the frequency limit for

output CV1, and PLIM2 bits set the frequency limit for the LED output. If the frequency is exceeded for a predetermined time interval, the InnoMux-2 controller will execute auto-restart.

6.3.7 Standby Mode

If the DIM2 input is held at 0 V the PSU enters ”Standby Mode”. The LED current is disabled and the internal LED driver circuit is powered down, reducing the controller own power consumption. Full rated power is still available at the CV1 output. The +V_LED output is maintained at a level of at least 8 V. The DIM2 input is a logic level type. If it is pulled up to above 3.3 V (5 Vmax), the LED current will be enabled.

6.3.8 Start-Up Sequence

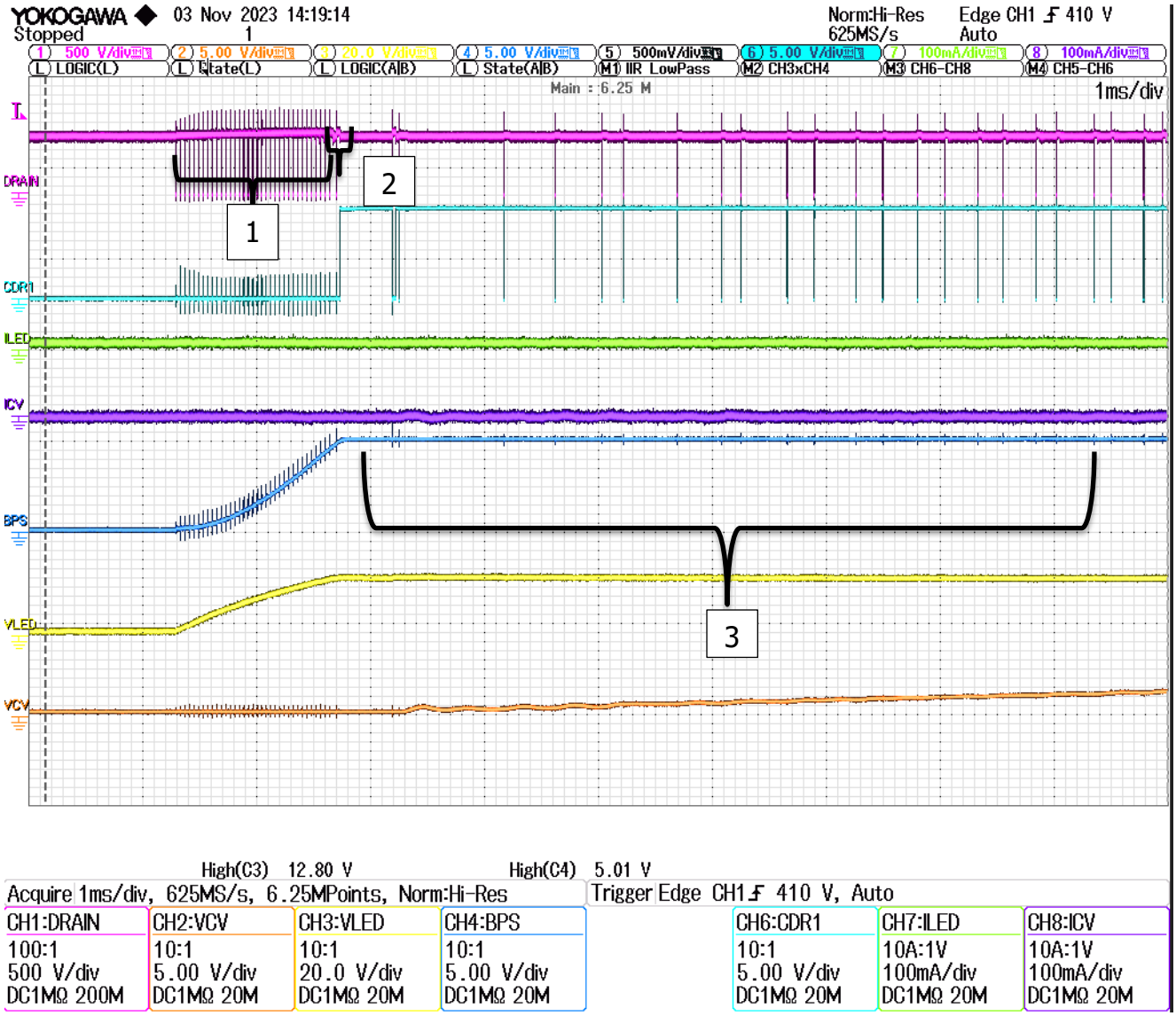


Figure 5 – First 10 ms of Start-Up.

1. Secondary-side controllers are powered-down (asleep). The primary-side controller operates open-loop at a fixed frequency about 25 kHz. The peak current is set to approximately 75% of its maximum level. If the secondary-side does not wake up and respond, the primary-side will:
   a. time out and shut down, or
   b. the primary-side bias voltage will rise high enough to trigger a bias OVP shutdown.

2. The LED output is the only output to rise significantly during interval 1. It provides power to InnoMux-2 (U1) internal secondary voltage regulator (BPS regulator), which generates the internal supply bus BPS (+5 V). Eventually the internal voltage regulator establishes 5 V at the BPS pin. U1 secondary-side controller then wakes up from its power-on-reset, and start hand-shaking with the primary controller to take over the control of InnoMux-2. Hand-shaking pulse & SEL signals to indicate the hand shake. Also need point out what happen to secondary if hand shake failed.

3. After hand-shaking, the fixed 25kHz switching frequency is ended, and InnoMux-2 (U1) switching according to the feedback and reference voltages on CV1 and LED. The CV1 voltage is linearly raised, while the LED voltage is maintained at the stay-alive voltage ($V_{STAYALIVE}$, ~8.0V) to provide input to the internal BPS regulator. While the Vcv1 is raised to the same reference percentage as the V_{LED}, InnoMux-2 (U1) starts ramping up both of the two output voltages simultaneously (V_{CV1} and V_{LED}) to their references.

4. CV1 and LED output voltages can be seen to rise simultaneously (Figure 6). At some time during interval 4, the CV1 will reach a sufficient level to power the internal BPS regulator via the VCV1 pin (U1 pin 10). The input of the BPS regulator then switches automatically to the VCV1 pin, thus reducing the power dissipation on the BPS regulator.

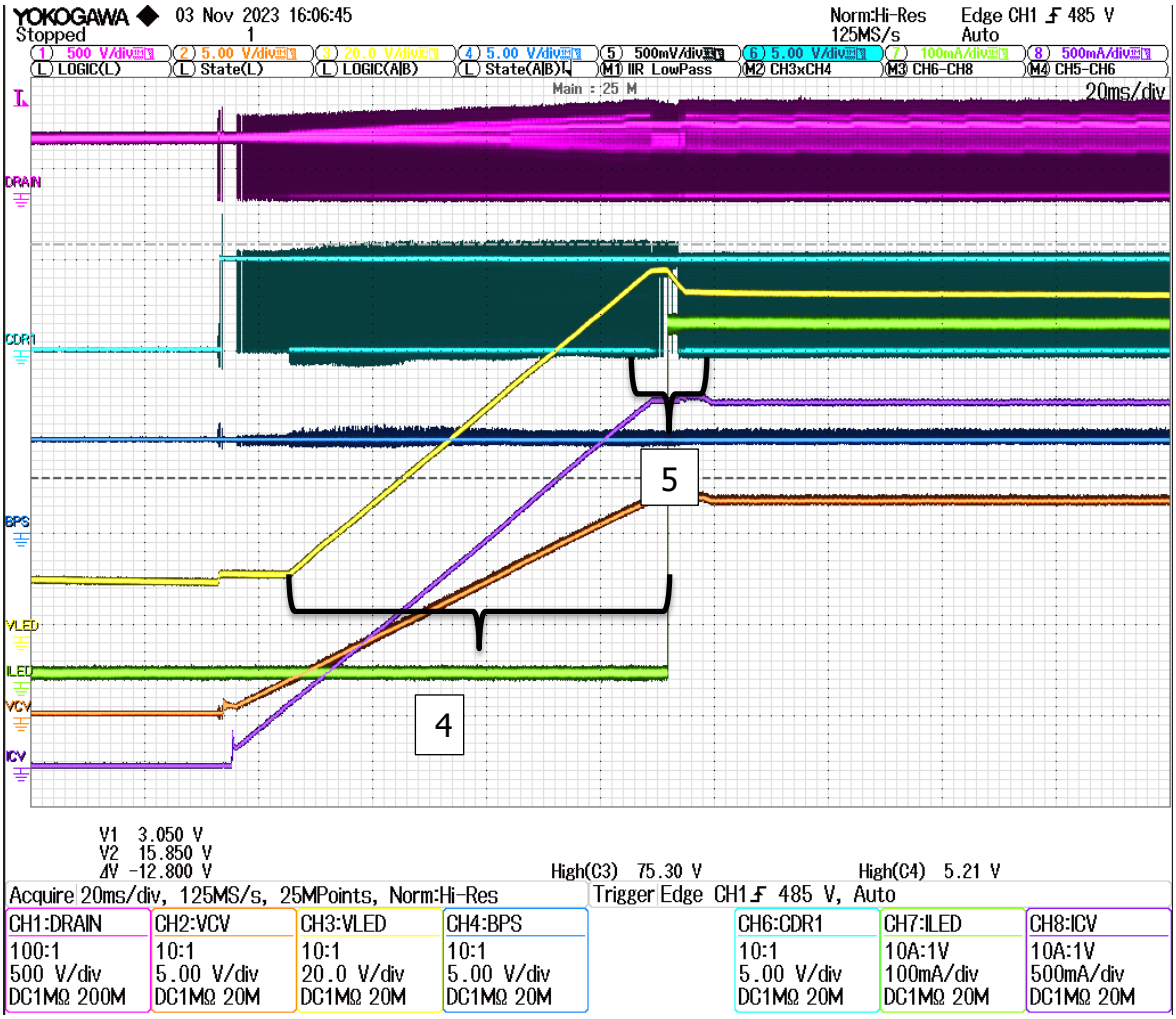


Figure 6 – Complete Start-Up Cycle Over Approximately 180 ms.

5. The LED current is enabled. Its level depends on the dimming configuration and the signal on the dimming input(s) (DIM1, DIM2). The LED current is controlled by the internal regulator (U1 pins 1, 3 and 4) and the external LED driver MOSFET (Q3). To reduce the power dissipation on the LED driver MOSFET (Q3), the InnoMux-2 controller (U1) maintains V_{LED} at a level with some minimum headroom of above the LED stack voltage. This keeps the voltage at the Vsense pins to a minimum.

7 Connection Diagram

The connection diagram on Figure 7 below shows a 2-wire filtered PWM dimming configuration. For other dimming configurations, please refer to the product datasheets.

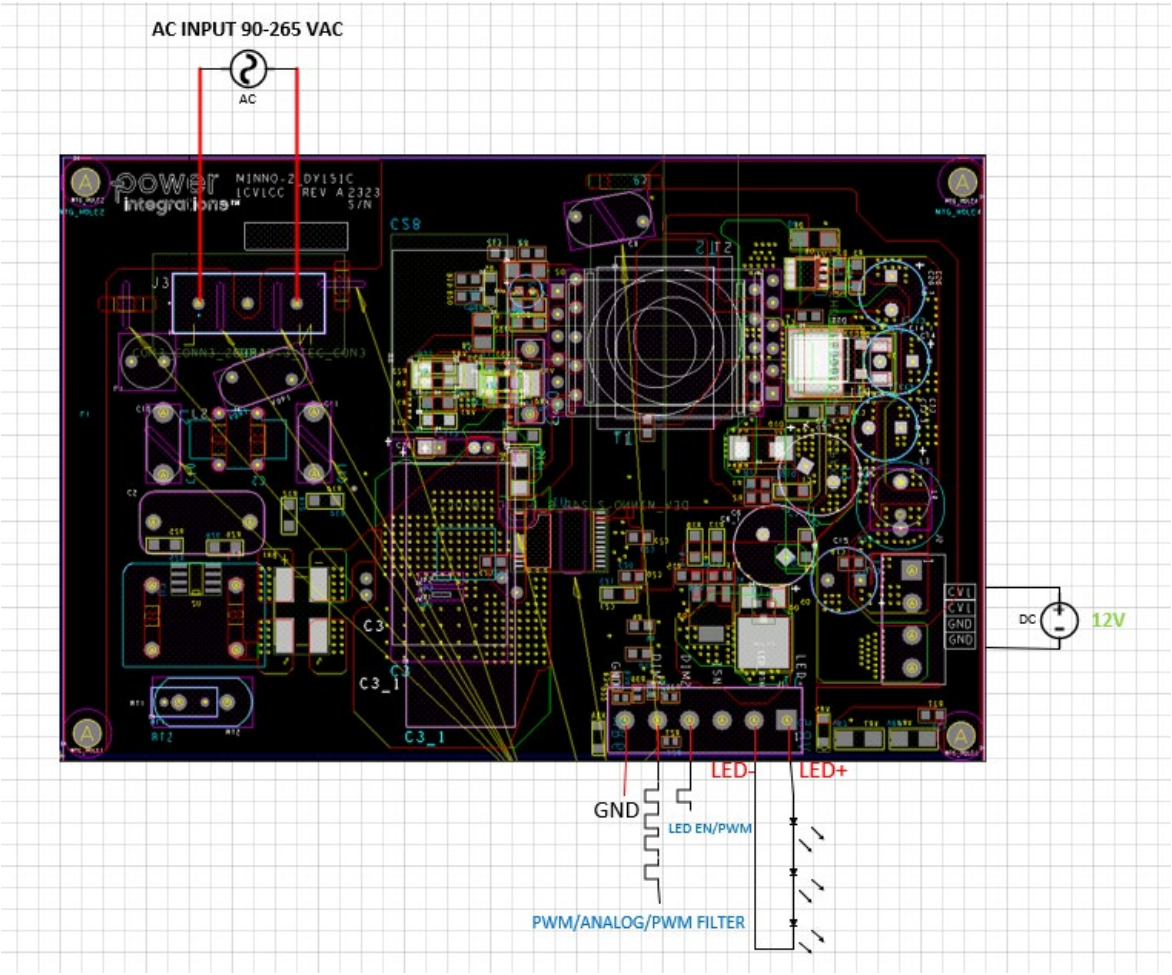


Figure 7 – Connection Diagram

8 PCB Layout

The converter PCB layout is illustrated on Figure 8, Figure 9 and Figure 10 below. PCB copper thickness is 2 oz (2.8 mils / 70 μm) was used for the PCB.

(1) FWD pin: FWD signal has large dv/dt, which can be one of the major noise source on the secondary circuit. Its PCB route should be kept away from the other signals.
(2) Ground plane: The impedance from InnoMux-2 controller's ground to ANODE terminal of secondary rectifier diode (D1) should be minimized, or separated from the power return ground. Star connection ground can be used here, to prevent the large secondary discharge current from affecting the ground level of the InnoMux-2 controller.
(3) Thermal: The primary switch in InnoMux-2 IC (U1) is cooled through the exposed pad and SOURCE pin of the IC. Care should be taken that their thermal impedance to the cooling copper of the PCB is kept to a minimum. (Figure 8).

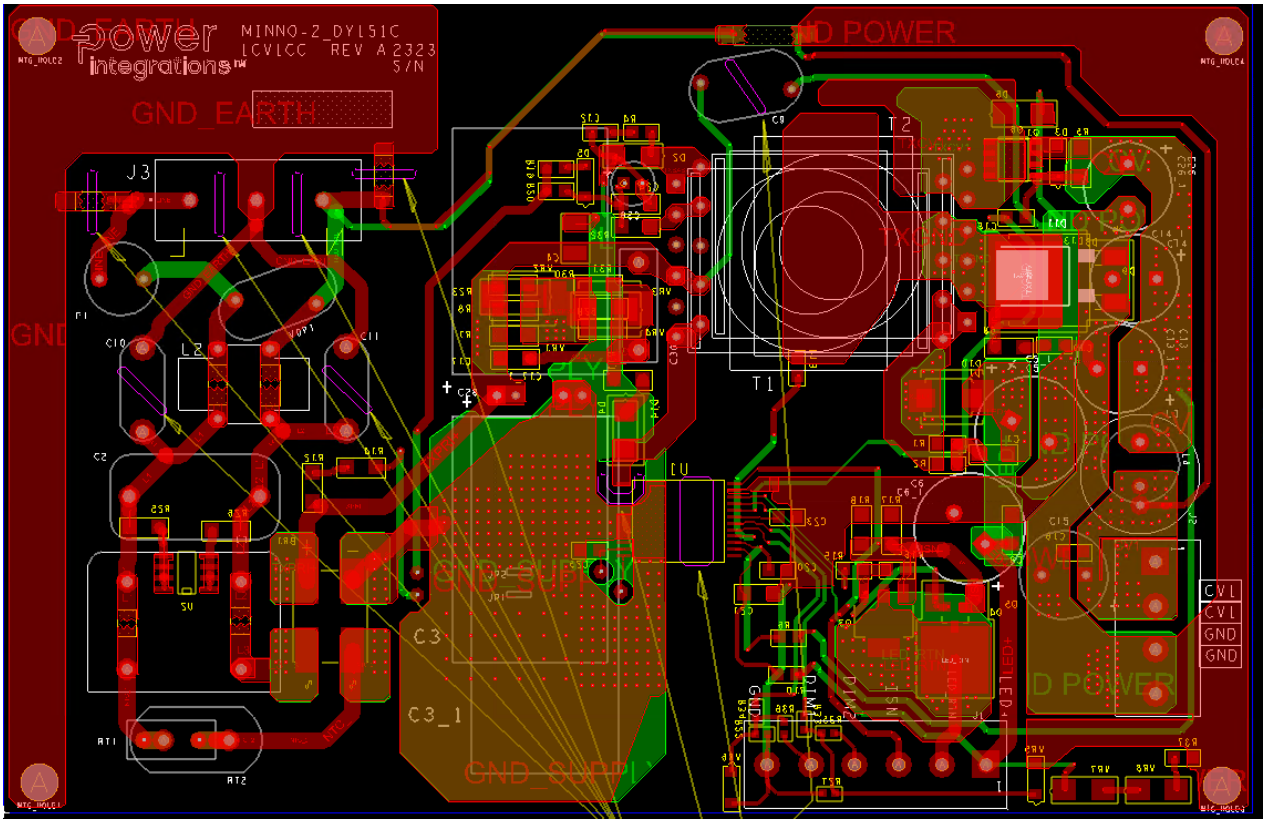


Figure 8 – Printed Circuit Layout.

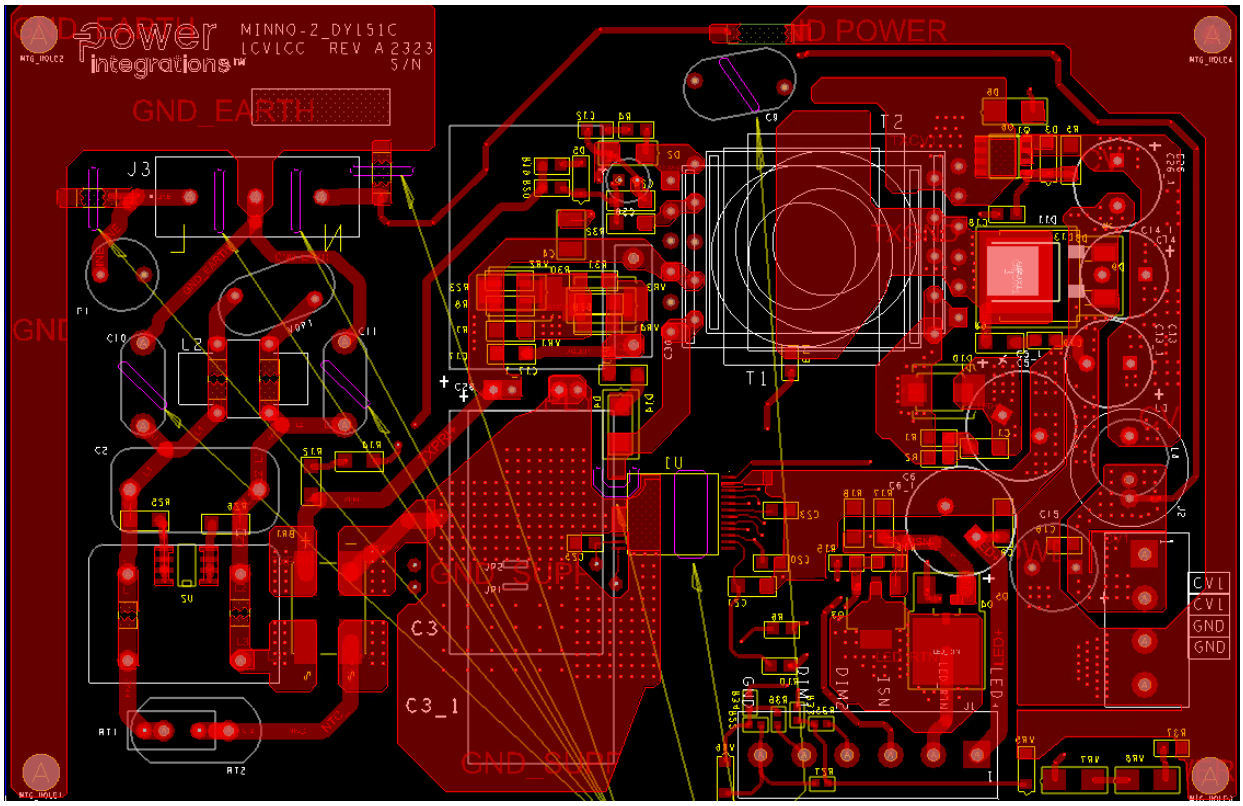


Figure 9 – Printed Circuit Layout, Bottom.

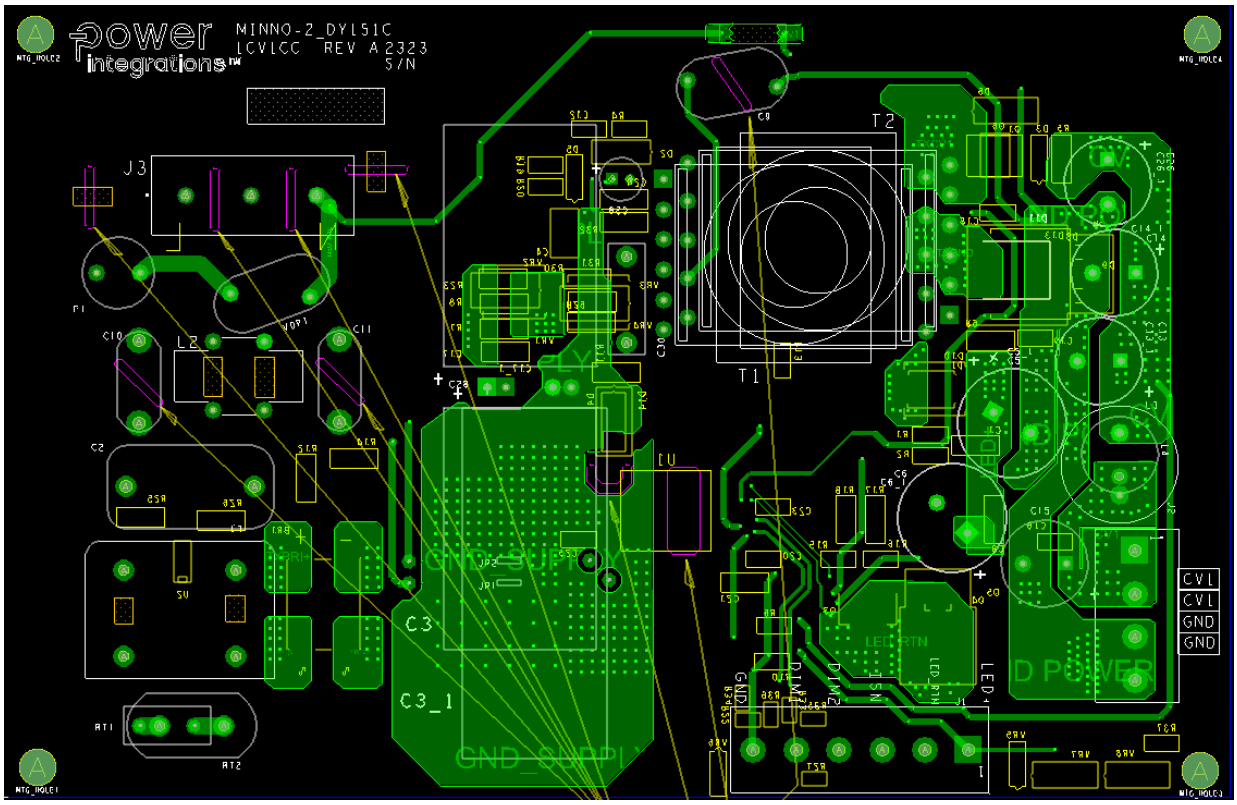


Figure 10 – Printed Circuit Layout, Top.

9 Transformer (T1) & CMC (L2) Specification

9.1 Core Information

Core EQ27/14, Guangzhou Tongyang Electronics Part No. 066260270718044

TYDZ 中国·通洋

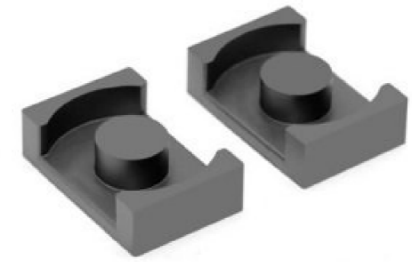
广州市通洋电子有限公司

Guangzhou Tongyang Electronics Co.,Ltd

地址：中国广东省广州市白云区松北工业区社前路56号1栋

Add:1st Building,No.56Sheqian Road,Songbe Industrial Zone,Baiyun District,Guangzhou,China

Tel:+86 020-81786686 Web:http://www.gztydz.com E-mail:ywb@gztydz.com



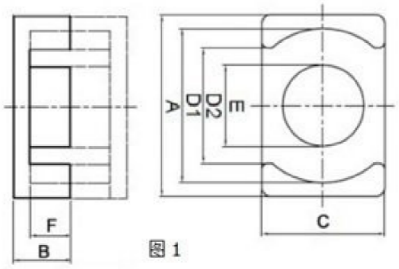


图 1

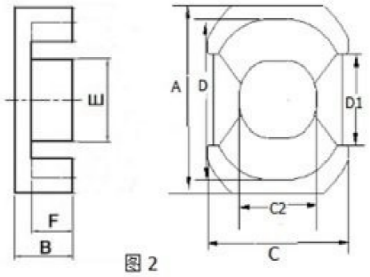


图 2

代 码 Code		066260270718044
型 号 Type		EQ27/14
尺寸（mm） Dimension	A	26.70±0.40
	B	6.85±0.20
	C	18.1±0.30
	C2	*
	D	*
	D1	23.10min
	D2	18.90min
	E	11.10±0.20
	F	4.45±0.20
	B-F	2.40±0.20
图 drawing		1
可调尺寸 adjustable dimension		
磁芯常数C1（mm^{-1}） Core Factor		0.45
有效磁路长度 Le（mm） Effective length Le		39.16
有效截面积 Ae（mm^2） Effective Area		85.88
有效体积 Ve（mm^3） Effective Volume		3363
重量 W（g/set） Weight		
电感系数 AL（nH/N2） ±25%	TY40	
	TY44	5000
	TY95	
功率损耗 Core loss	TY40	
	TY44	
	TY95	

·磁芯可按客户尺寸开模，可以开气隙。

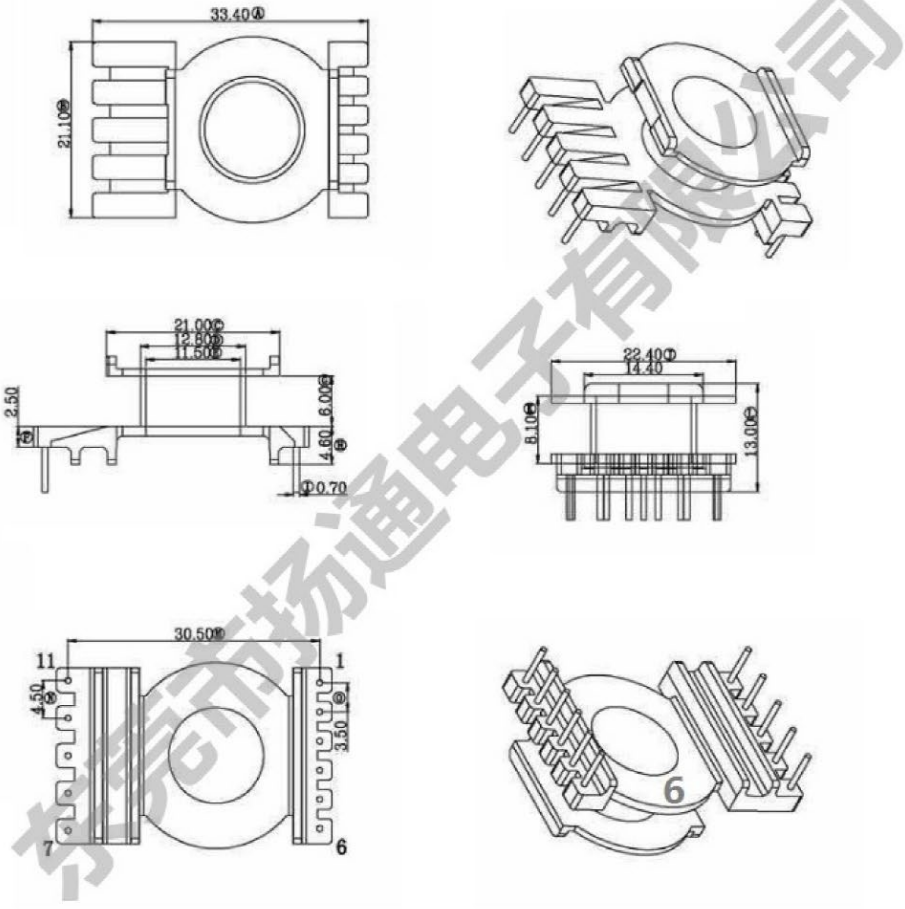
We can open the mould or grind air gap for the ferrite core as per customer's requirement and size .

Figure 11 – EQ27/14 Core.

9.2 Bobbin Information

RoHS

EQ27变压器骨架电木骨架高频骨架电源骨架YT-2701



东莞市洋通电子有限公司 广东省东莞市石碣镇,刘屋工业区			NAME	EQ27变压器骨架YT-2701 http://www.dgytdz.com/		
TEL.电话	0769-86309483	TOLERANCE	MATERIAL			PHENOLIC
FAX.传真	0769-89026473	0<L≤4 ±0.2 4<L≤16 ±0.3 16<L≤63±0.4	SCALE		DRWA BY	张 阳
			4/1		CHECK	张 艺
E--mail	wydz001@126.com	Pin pitch±0.2	UNIT	mm	DATE	2014.03.2

Figure 12 – Guangzhou Tongyang Electronics - 11 Pin Bobbin – YT-2701.

9.3 Electrical Diagram

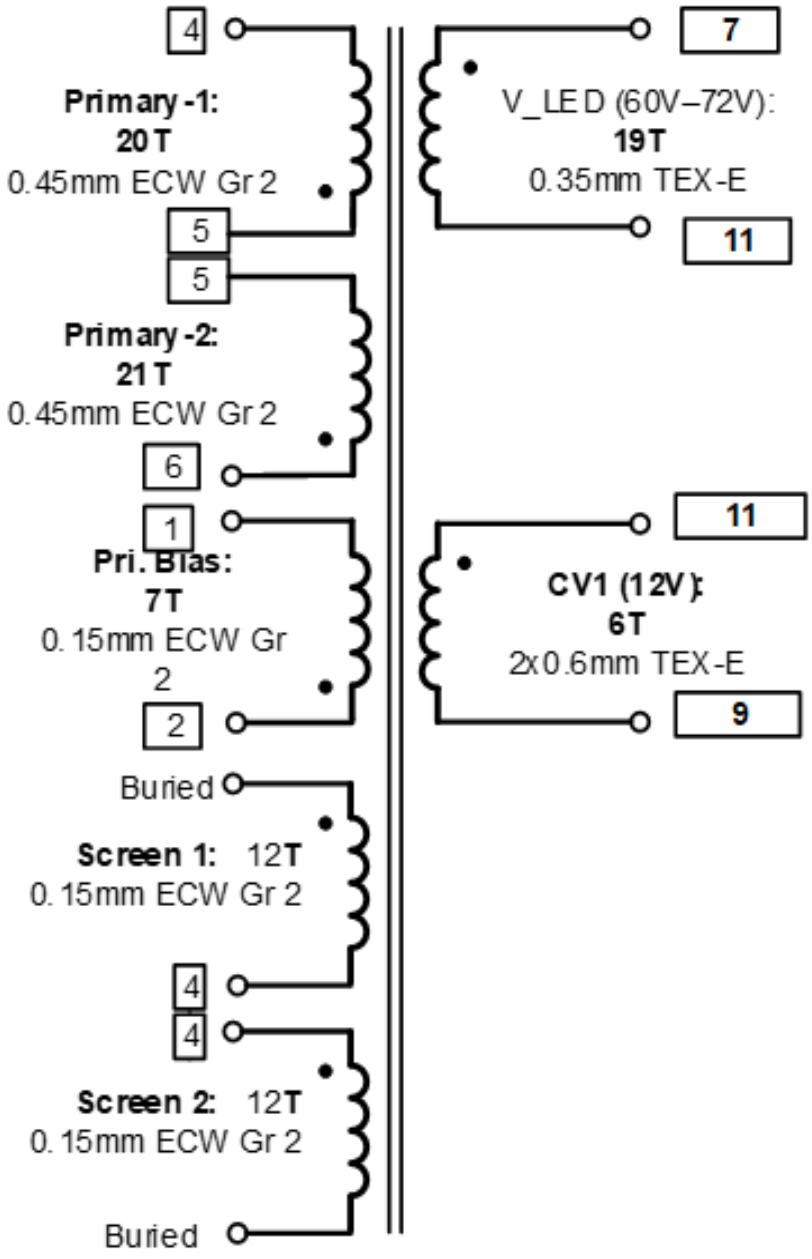


Figure 13 – Transformer Electrical Diagram.

9.4 Winding Stack Diagram

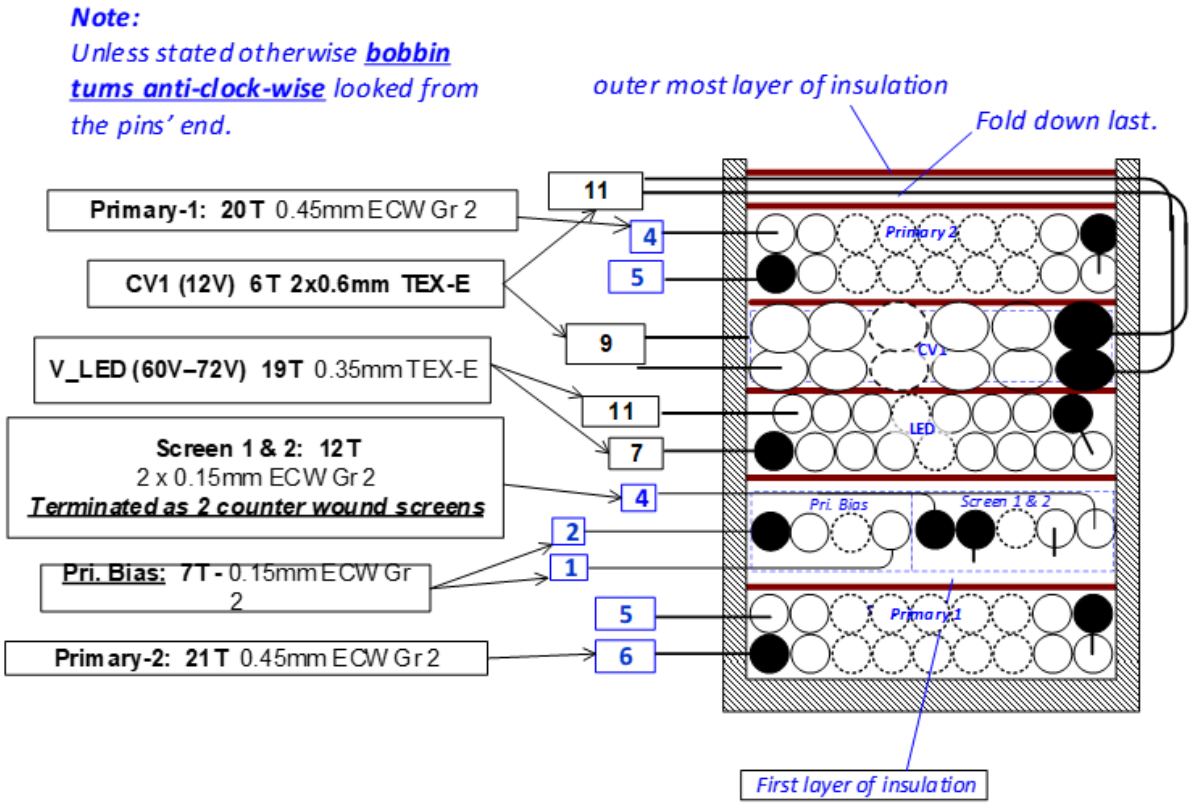


Figure 14 – Transformer Build Diagram.

9.5 Transformer Electrical Specification

Parameter	Condition	Spec.
Electrical strength	1 second, 60 Hz from pins 1-6 to 7-13.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 5 and 6, with all other windings open.	377 µH ±3%
Resonant Frequency	Between pin 5 and 6, other windings open.	1,100 kHz (Min.)
Primary Leakage Inductance	Between pin 5 and 6, with all secondary 7, 9, 11 and 13 shorte	10qH (Max.)

9.7 Materials List

Item	Description
[1]	Core: Ferroxcube Part No. EQ27/14 TY44.
[2]	Bobbin: EQ27 YT-2701
[3]	Magnet Wire: 0.45 mm ECW Gr 2.
[4]	Magnet Wire: 0.15 mm ECW Gr 2.
[5]	Magnet Wire: 0.35 mm, Triple Insulated Wire.
[6]	Magnet Wire: 0.6 mm, Triple Insulated Wire.
[8]	Barrier Tape: Polyester Film, 2.5±0.5 mil thickness, 6 mm Wide.
[9]	Varnish: MR8008B - Varnish, Insulating, Polyurethane, Transparent/Amber EMR8008B250ML Or BC-359

9.8 Transformer Construction

Layer 1&2 Primary-1	Start at pin 6, wind 21 turns of 1 wire Item [3] in 2 layers with tight tension. Terminate at pin 5.
Insulation	Place 1 layers of tape Item [8] for insulation.
Layer 3 Primary Bias	Start at pin 2, wind 7 turns of wire Item [4] with tight tension and terminate at pin 1.
Layer 3 Screen: 1&2	Start at pin 4 for screen 1 and start from a dummy pin for screen2.#wind 12T of wire Item [4] from end of bias wind with tight tension.Cut screen1 winding and bury , cut screen2 winding at the end and connect it to pin4.Take off the winding from dummy pin and bury inside the layer.Cover the buried windings with 1 layer of Item [8].
Insulation	Place 1 layer of tape Item [8] for insulation. Cut end of screen wind to leave the end buried under the tape.
Layer 4&5 LED	Start at pin 7, wind 19 turns of wire Item [5] in 2 layers with tight tension and terminate at pin 11.
Insulation	Place 1 layer of tape Item [8] for insulation.
Layer 6 CV	Start at pin 9, wind 6 turns of Item [6] in 1 layer with tight tension. Cut to leave about 5cm and tape to mandrel bobbin
Layer 7 CV	Start at pin 9, wind 6 turns of Item [6] in 1 layer with tight tension. Cut to leave about 5cm and tape to mandrel bobbin
Layer 8&9 Primary-2	Start at pin 5, wind 20 turns of 1 wire Item [3] in 2 layers with tight tension. Terminate at pin 4.
Insulation	Place 2 layers of tape Item [8] for insulation.
Finish Assembly	Gap core halves to 377 μH ±3% inductance. Insert cores and tape tightly together item [8]. Label "XXX.X μH" (XXX.X = measured primary inductance value in μH) Varnish - Item[11].

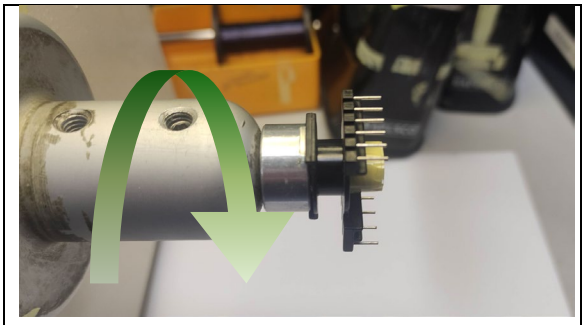
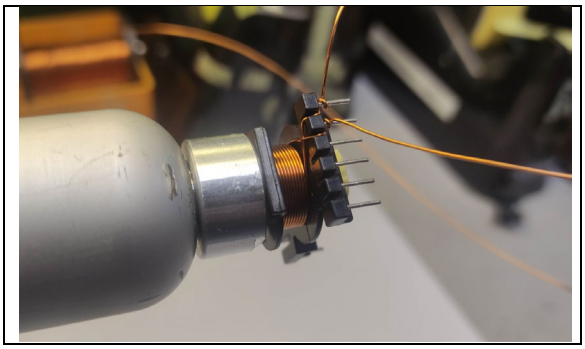
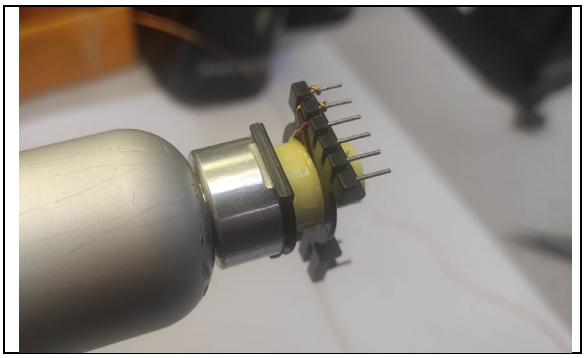
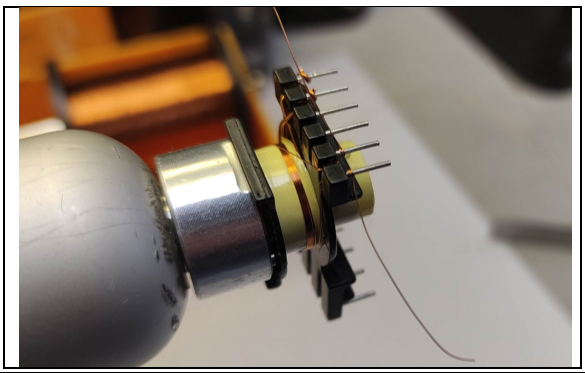
9.9 Transformer Test

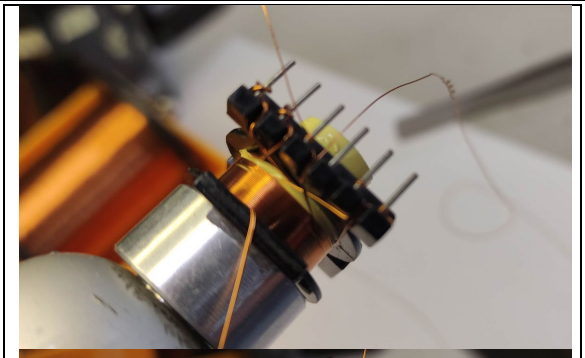
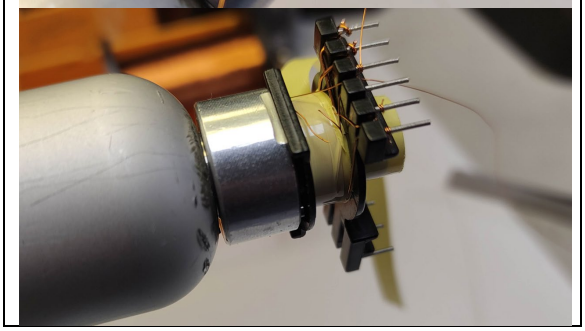
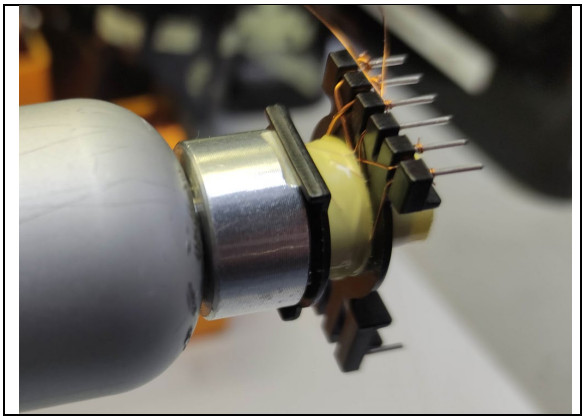
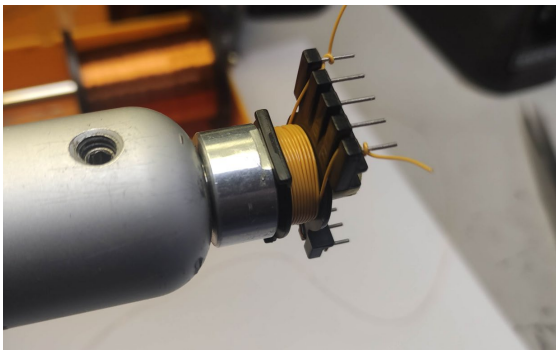
The winding measured inductance of the individual windings as well as the primary leakage inductance of the transformer are shown in the table below:

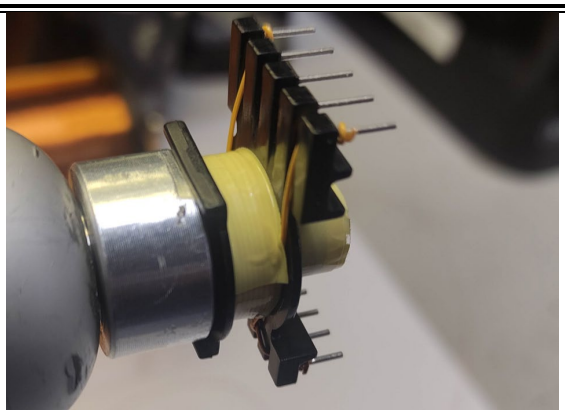
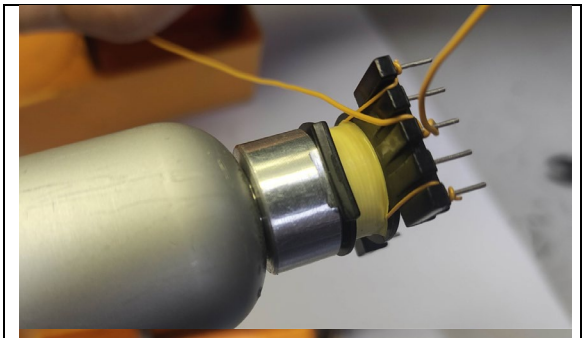
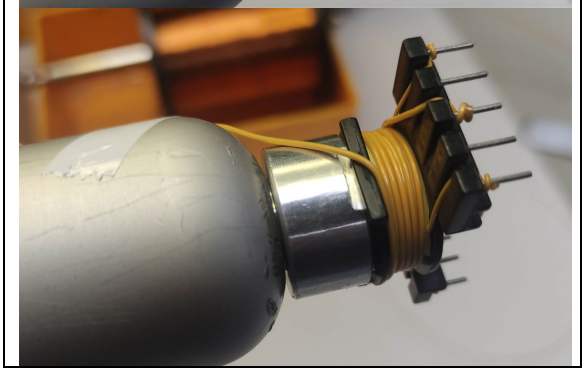
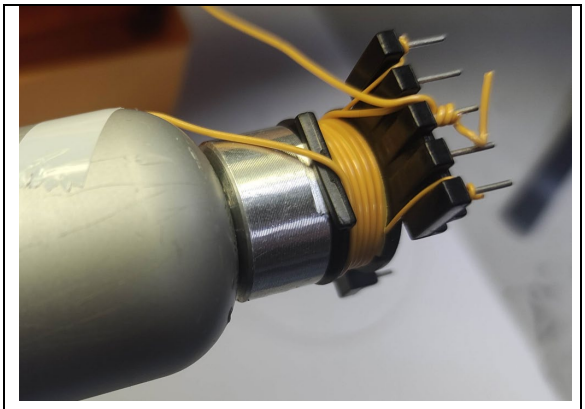
		Between Pins	**Pins Shorted**
Lpri [μH]	376	4 - 6	
LCV [μH]	8.6	11 - 9	
LLED [μH]	82	11 - 7	
L1aux [μH]	11.6	1 - 2	
Llkg1 [μH]	9.4	5 - 6	7 and 11
Llkg2 [μH]	12.2	5 - 6	9 and 11

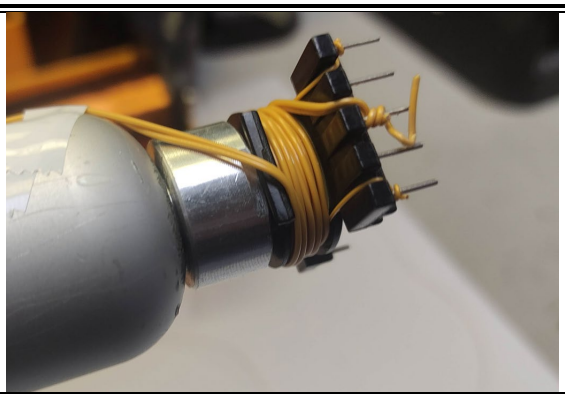
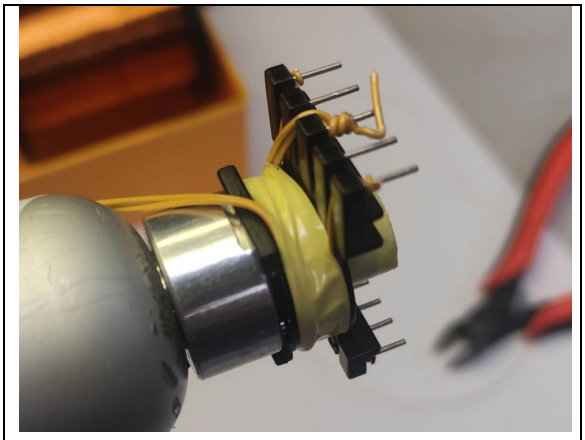
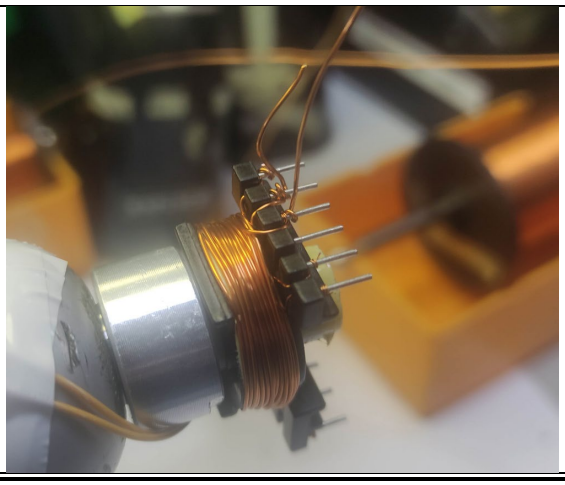
Table 1 – Winding Inductance. All measurements are done in 100 kHz at 1 V_{RMS}.

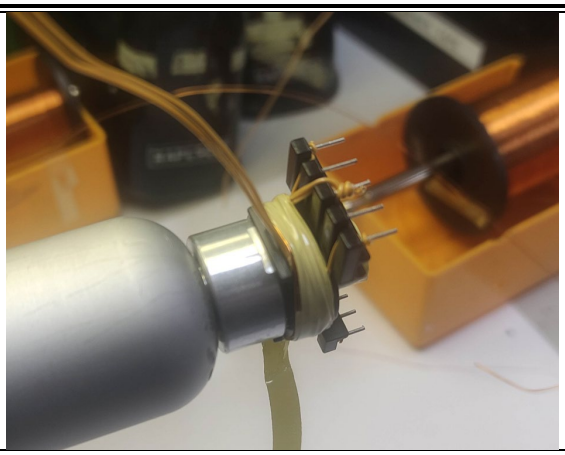
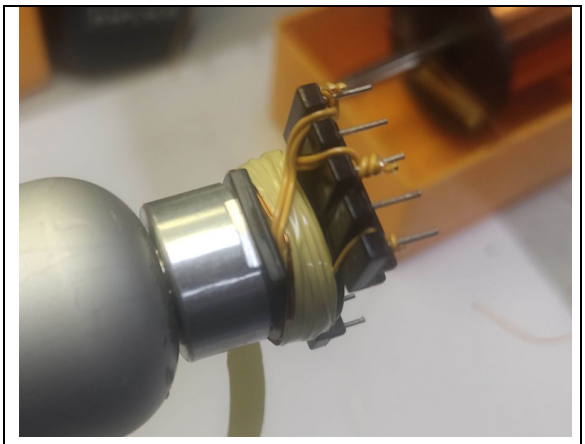
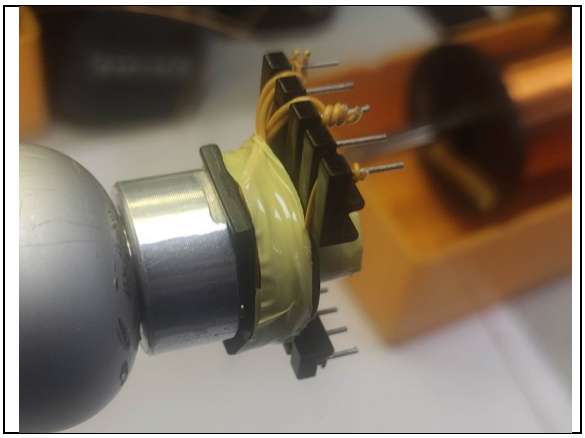
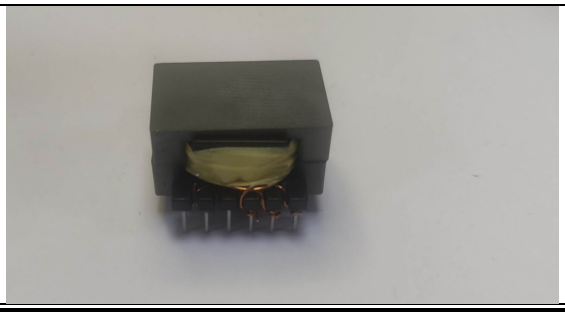
9.10 Winding Illustration

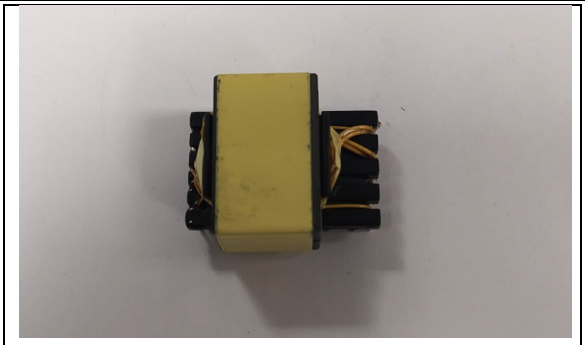
		Place the bobbin on the mandrel with the pin side to the right. Winding direction is in the clockwise direction i.e. top side moving away from operator.
Wind 1 **Primary 1** **½ Primary**		Start at pin 6, wind 21 turns of 1 wire Item [3] in 2 layers with tight tension. Terminate at pin 5.
Insulation layer		Place 1 layers of tape Item [8] for insulation.
Wind 2 **Primary Bias**		Start at pin 2, wind 7 turns of wire Item [4] with tight tension and terminate at pin 1.

Wind 3 **Screen 1&2**	 	Start at pin 4 for screen 1 and start from a dummy pin for screen2.#wind 12T of wire Item [4] from end of bias wind with tight tension.Cut screen1 winding and bury , cut screen2 winding at the end and connect it to pin4.Take off the winding from dummy pin and bury inside the layer.Cover the buried windings with 1 layer of Item [8].
Insulation layer		Place 1 layer of tape Item [8] for insulation. Cut end of screen wind to leave the end buried under the tape.
Wind 4 **LED**		Start at pin 7, wind 19 turns of wire Item [5] in 2 layers with tight tension and terminate at pin 11.

Insulation		Place 1 layer of tape Item [8] for insulation.
Wind 5 CV	 	Start at pin 9, wind 6 turns of Item [6] in 1 layer with tight tension in anticlockwise direction. Cut to leave about 5cm and tape to mandrel bobbin.
Wind 5 CV		Start at pin 9.wind 6 turns of Item[6] in 1 layer with tight tension in anticlockwise direction.

		Cut to leave 5cm of free wire and secure it to the mandrel chuck with tape
Insulation		Place 1 layer of tape Item [8] for insulation.
Wind 6 Primary 2 ½ Primary winding		Start at pin 5, wind 20 turns of 1 wire Item [3] in 2 layers with tight tension. Terminate at pin 4.

Insulation		Place 1 layer of tape Item [8] for insulation.
Terminate CV winding		Bend wire end down and take through the slot between pins 9 & 10 and terminate to pin 11.
Insulation		Place 1 layer of tape Item [8] for insulation.
Insert core		Gap core to achieve 377µH. Tape core tightly together.

		Cover with 1 layer of tape item [8]. Varnish dip and cure item [11]

9.11 CMC Specification

1) *Electrical Diagram:*

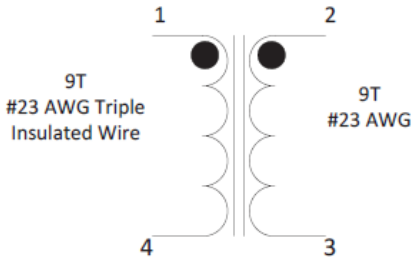


Figure 1 –Inductor Electrical Diagram.

2) *Electrical Specifications:*

Inductance	Pins 1-4 measured at 100kHz, 0.4 RMS.	200 uH +/- 10%
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted	1 uH

3) *Materials:*

Item	Description
[1]	Core: GL50 T 12X6X4-C, PI Part # 32-00315-00 BIPOLAR ELECTRONIC CO., LTD
[2]	Magnet Wire: #23 AWG
[3]	Triple Insulated wire #23 AWG

9.12 CMC Winding Illustration

Start as pin 1 for item[3] and pin 2 for item[2] .

Wind together 9 turns on core item[1].

Mark end of item[3] as pin 4 and end of item[2] as pin 3.

10 Performance

10.1 RTM Curve

RTM curve is verified in specific load points with calculating primary peak current at measured switching frequency points.

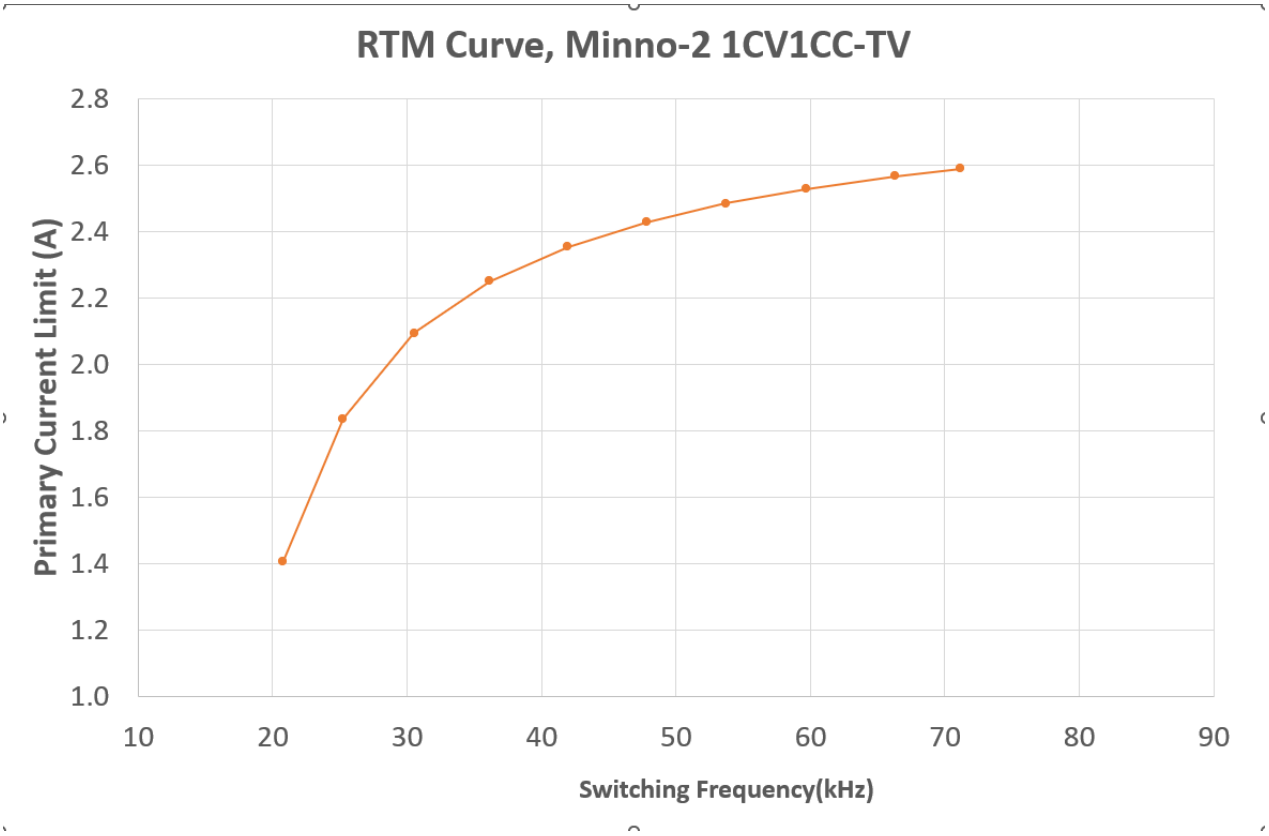


Figure 15 – Primary Current(A) vs. SW frequency at Room Temperature.

10.2 Full Load Efficiency vs. Line

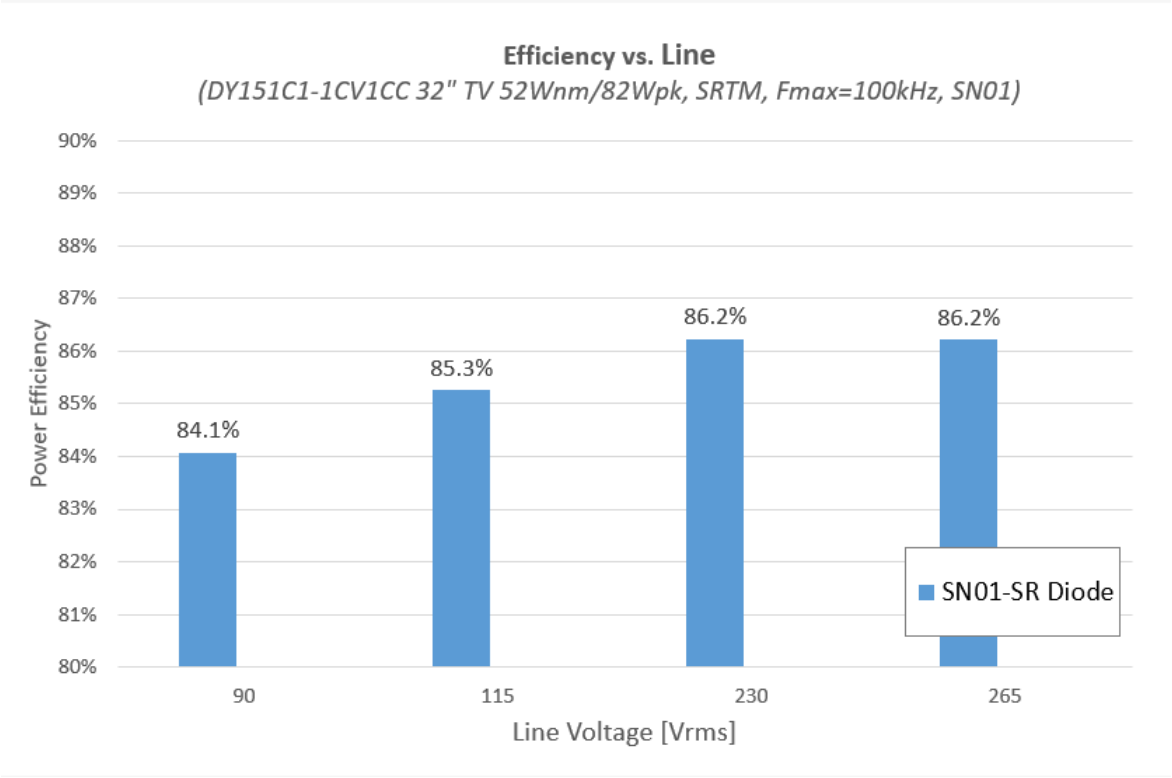


Figure 16 – Full Power Efficiency vs. Line Voltage at Room Temperature.

9.13 Efficiency vs. Load

The efficiency vs. load measurements are shown below. These were obtained for all combinations of:

- All (nominal)line voltages (90V, 115V, 230V, 265V);
- LED full current of 380mA with 11 steps for each line voltage
- CV1 full current of 2A with 11 steps for each line voltage

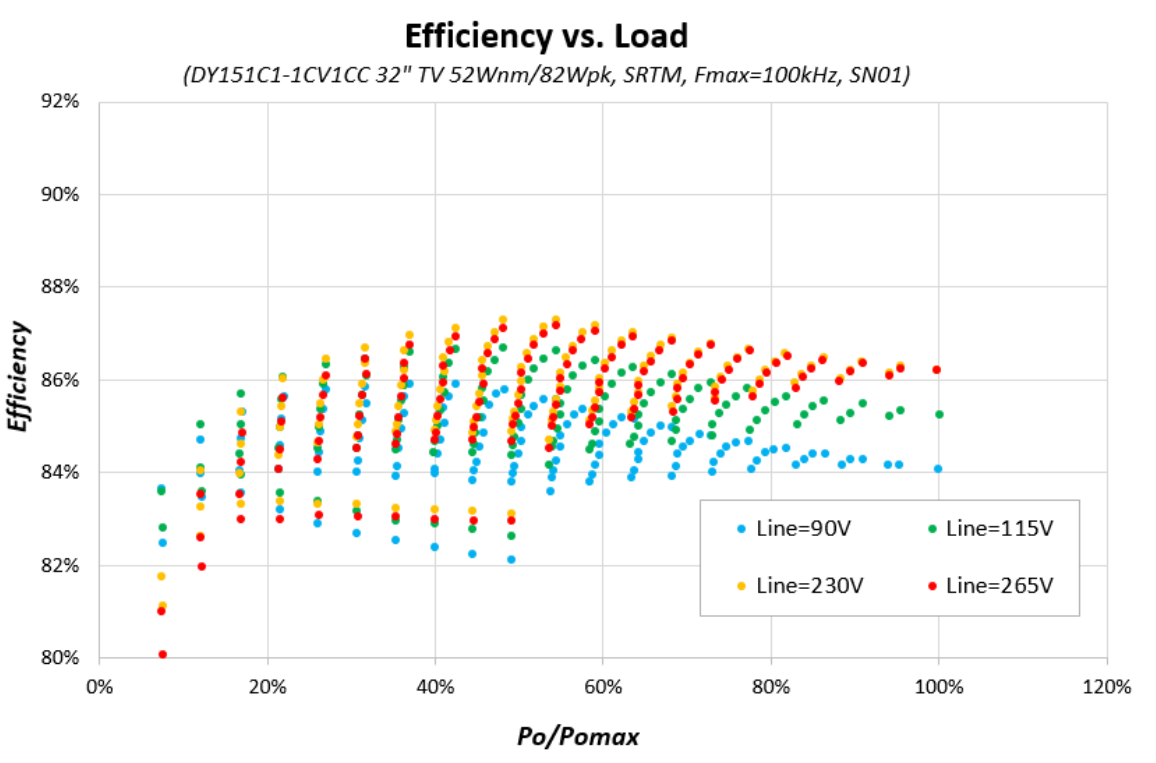


Figure 167 – Efficiency vs. Load for all line and V_{LED} variations, Room Temperature.

9.14 Output Load Regulation

The output-voltage regulation error was measured for both CV output. The current at CV output was increased from 1% to 100% of its rating in 10 steps. The current at LED output was increased from 5% to 100% of its rating in 10 steps.

- all (nominal) line voltages

The load regulation error for the CV output is shown on Figure 18 :

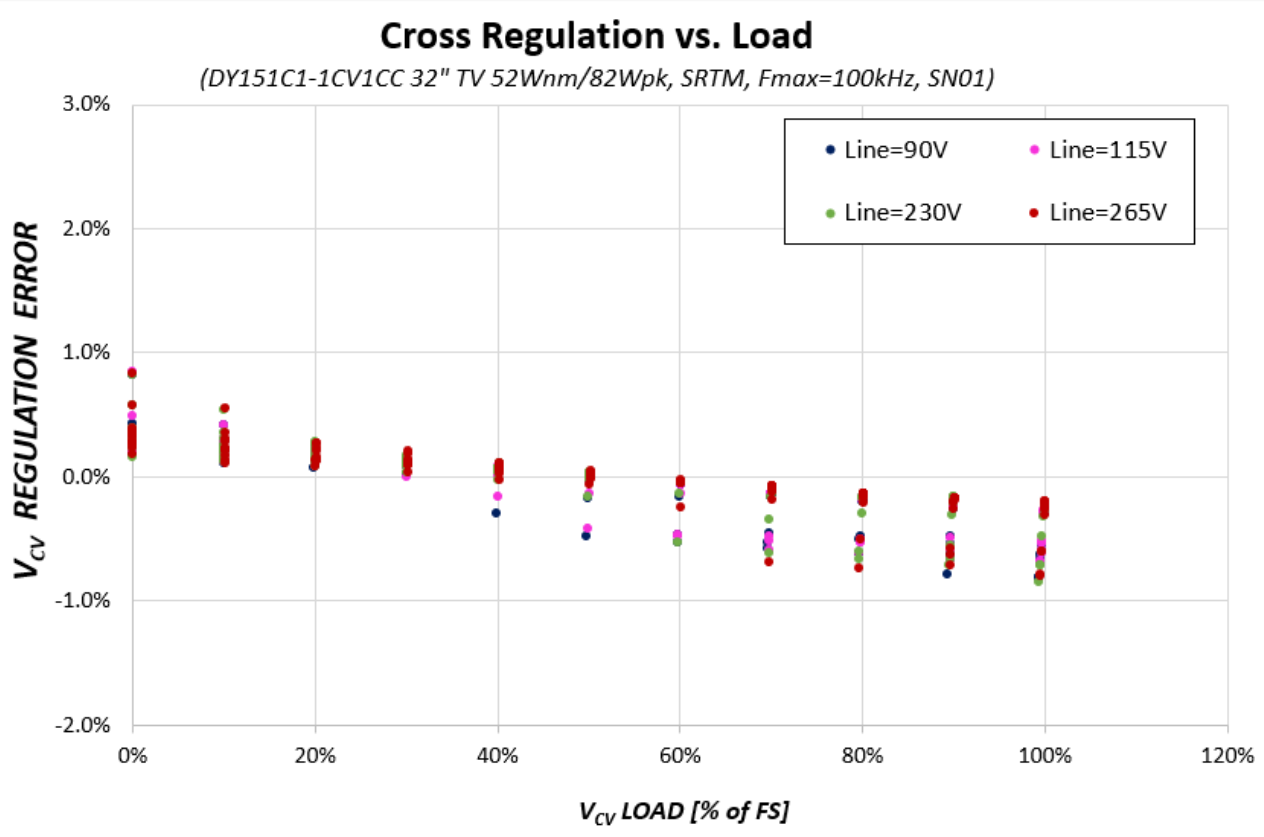


Figure 17 – VCV Output Error vs. Percentage Load, at Room Temperature.

The load regulation error for the LED output is shown on Figure 19 :

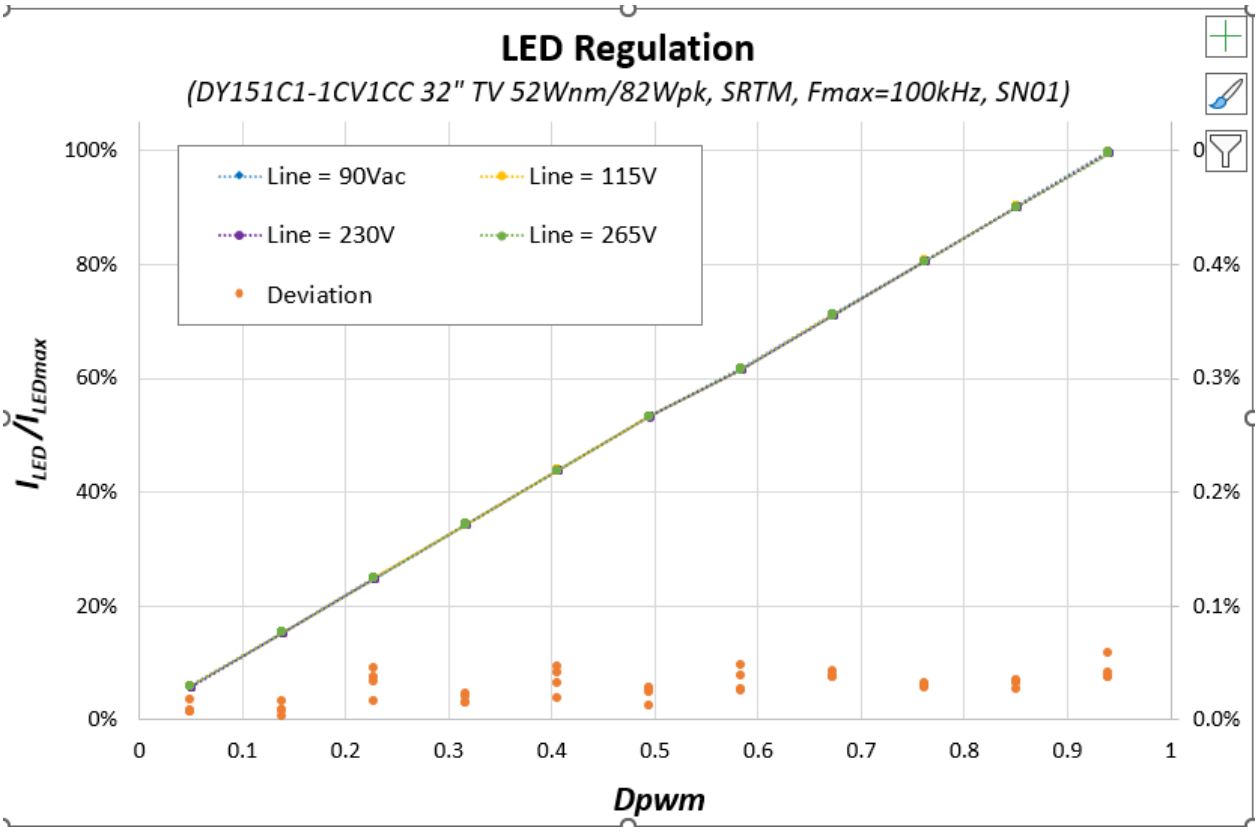


Figure 18 – ILED Output Error vs. PWM duty, at Room Temperature.

9.15 Standby Input Power (I_{LED} = 0 A)

The converter standby power was measured for all (nominal) line voltages; with the LED output disabled, and for 0 mW ~ 300 mW load on the CV output. The results are shown in Figure 20 below.

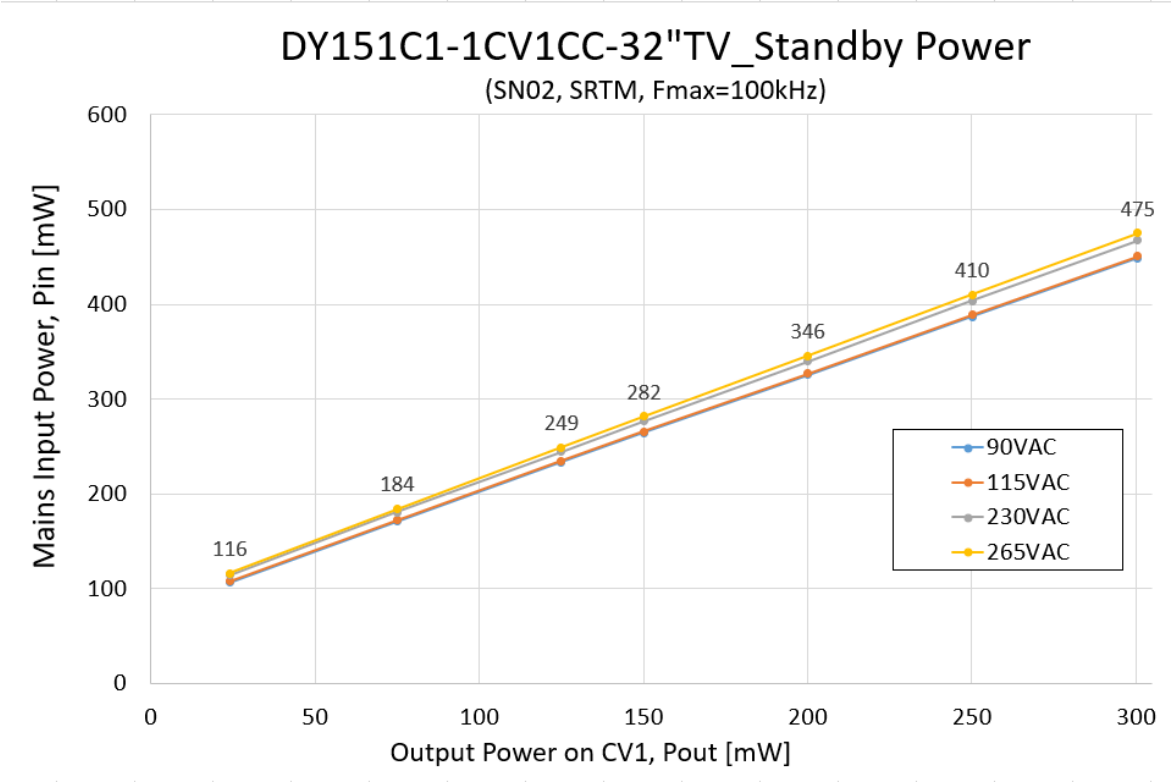


Figure 19 – Standby Power Consumption vs. Line Voltage, Room Temperature.

9.16 LED Dimming

The PSU was configured for filtered PWM dimming. The value of the LED current was measured as the duty of the PWM was increased from 10% to 100% in 10 steps. The measurements were taken at nominal LED stack voltage and repeated for:

- all line voltages;
- no load or full load on CV output;

The results are presented in Figure 21 and Figure 22.

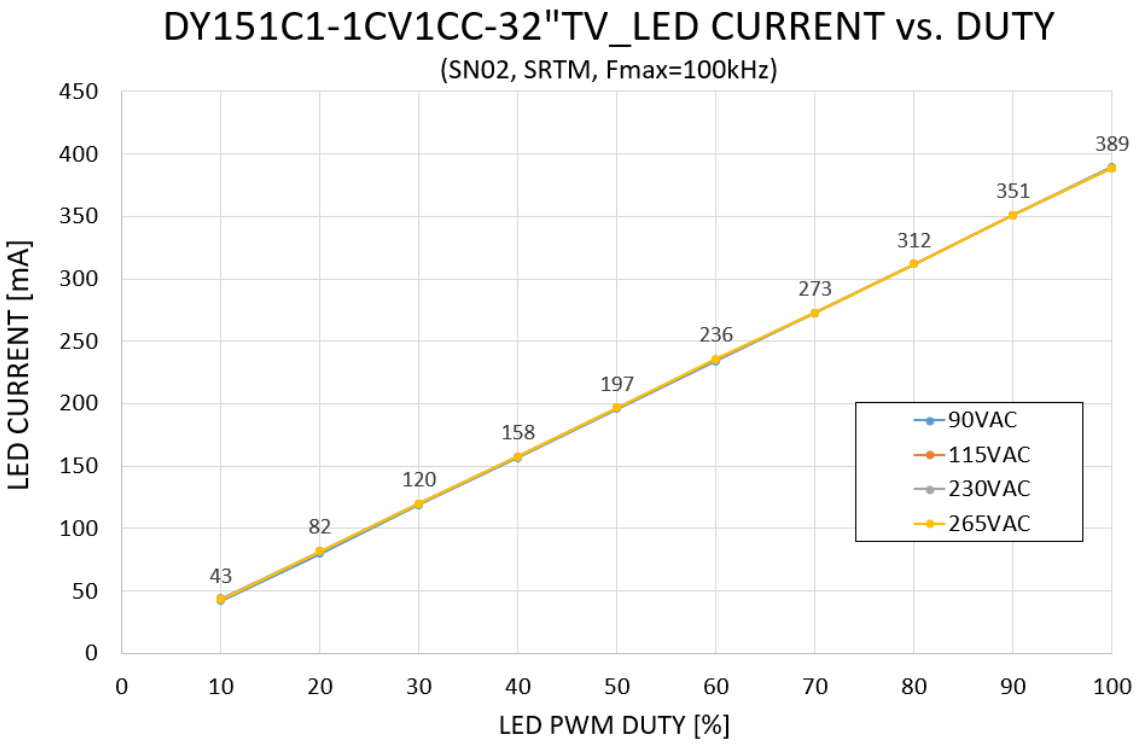


Figure 20 – Filtered PWM Dimming(CV=NoLoad)

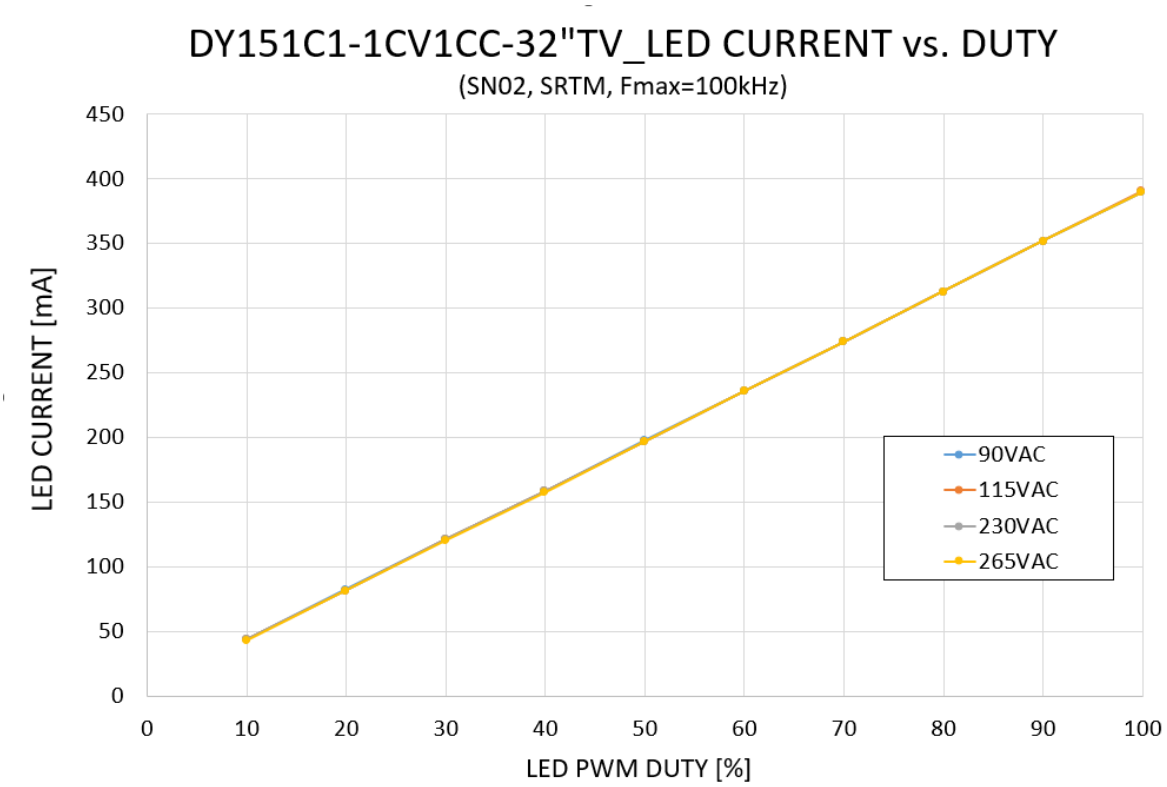


Figure 22 – Filtered PWM Dimming(CV=NomLoad)

9.17 CV Load Transient Response

CV output voltage is measured at load transient from 0,5A to 4,5A.Measurment has been done at 90VAC and 265VAC with full led load and 10% duty on led load.In all cases less than 5% voltage drop observed on CV output.

Bandwidth of the channel is 20MHz.

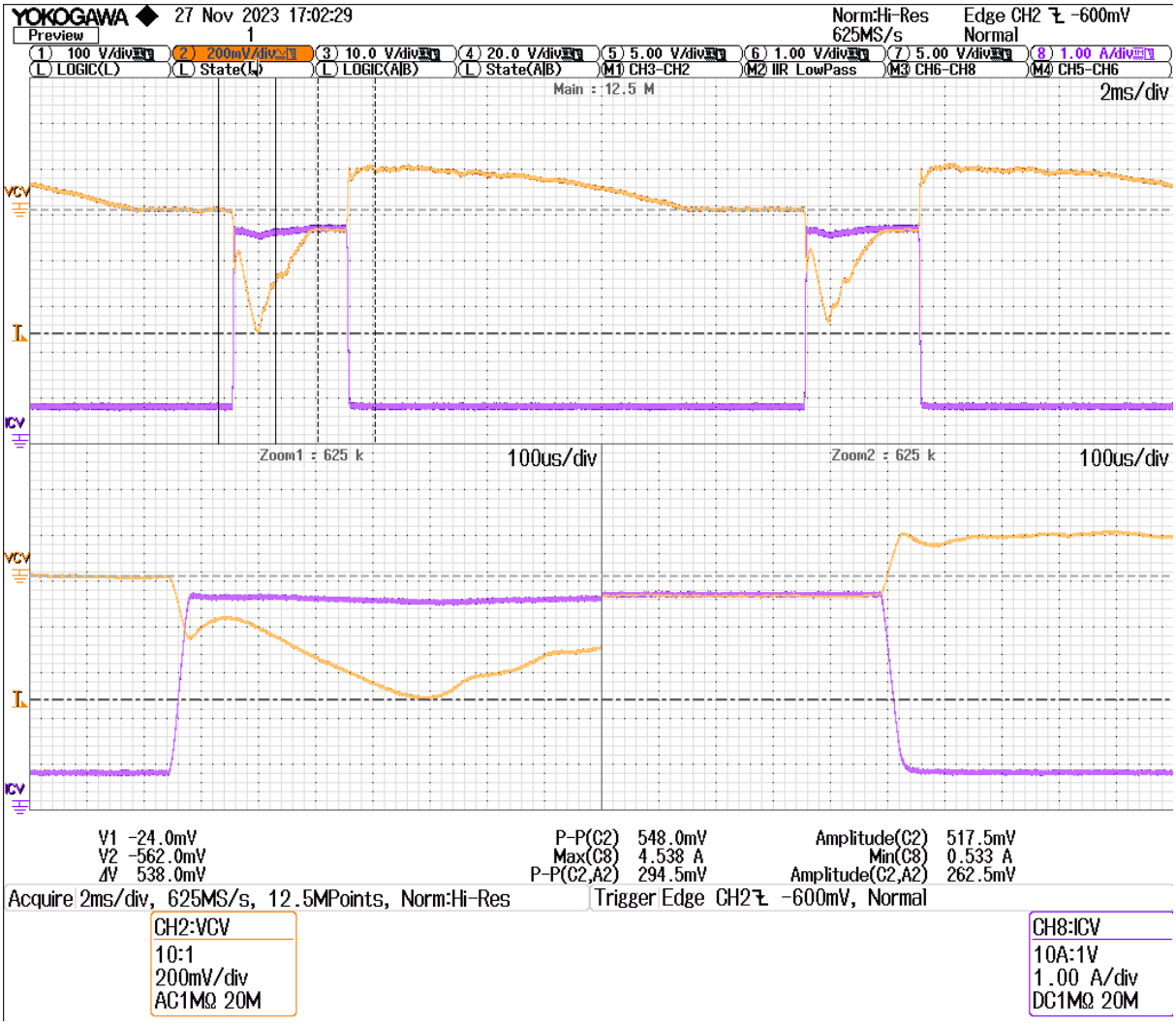


Figure 23 **– CV (12 V) Output - Load Transient under nominal LED load at 90VAC**

I_{CV}=0.5A-4.5A; Undershoot 548mV,4.56% ; Overshoot=294.5mV,2.45%

CH2: V_{CV} , CH8: I_{CV}

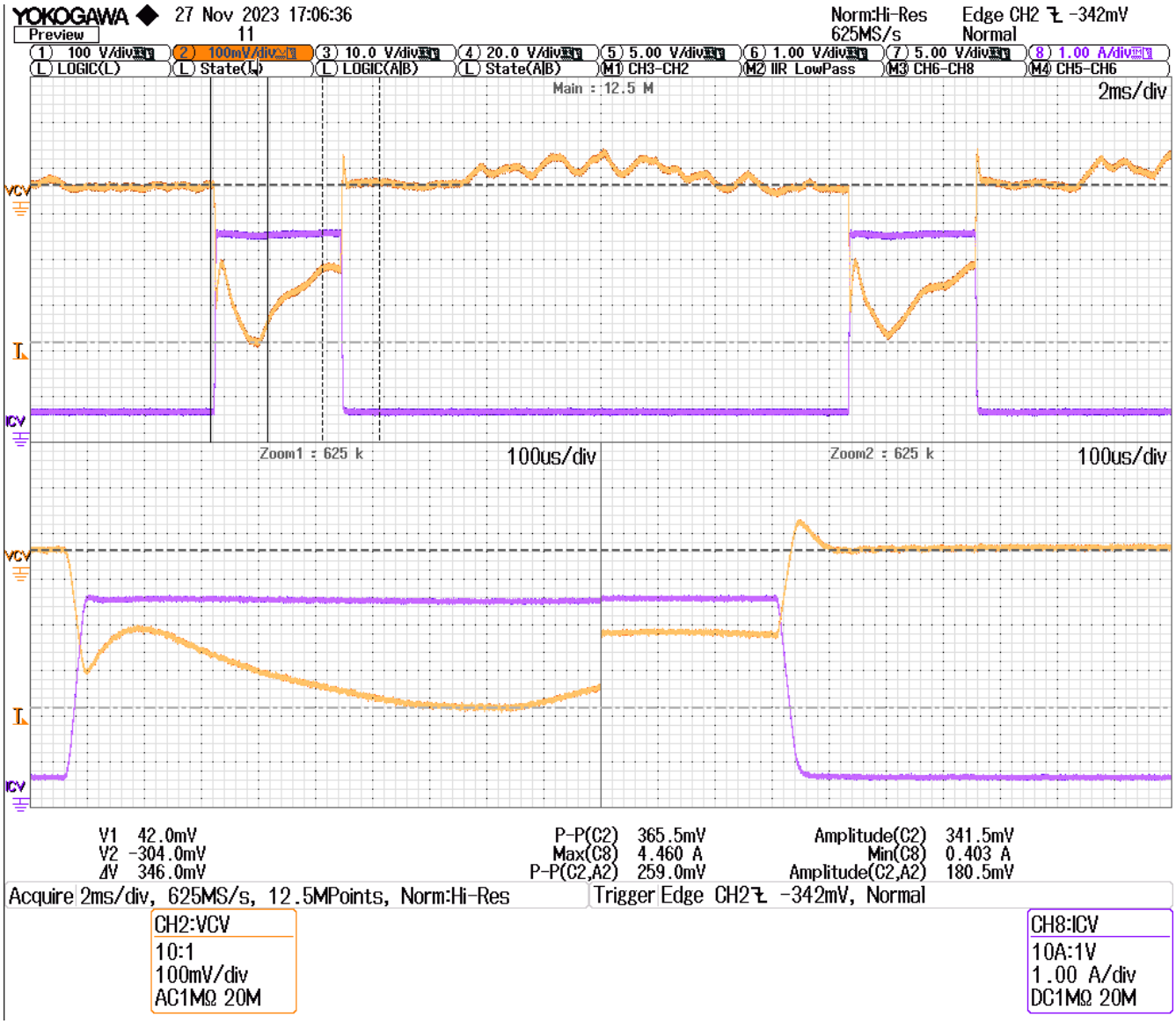


Figure 24 **– CV (12 V) Output - Load Transient under 10% duty on LED at 90VAC**

I_{CV}=0.5A-4.5A; Undershoot 366mV,3.05% ; Overshoot=259mV,2.16%

CH2: V_{CV} , CH8: I_{CV}

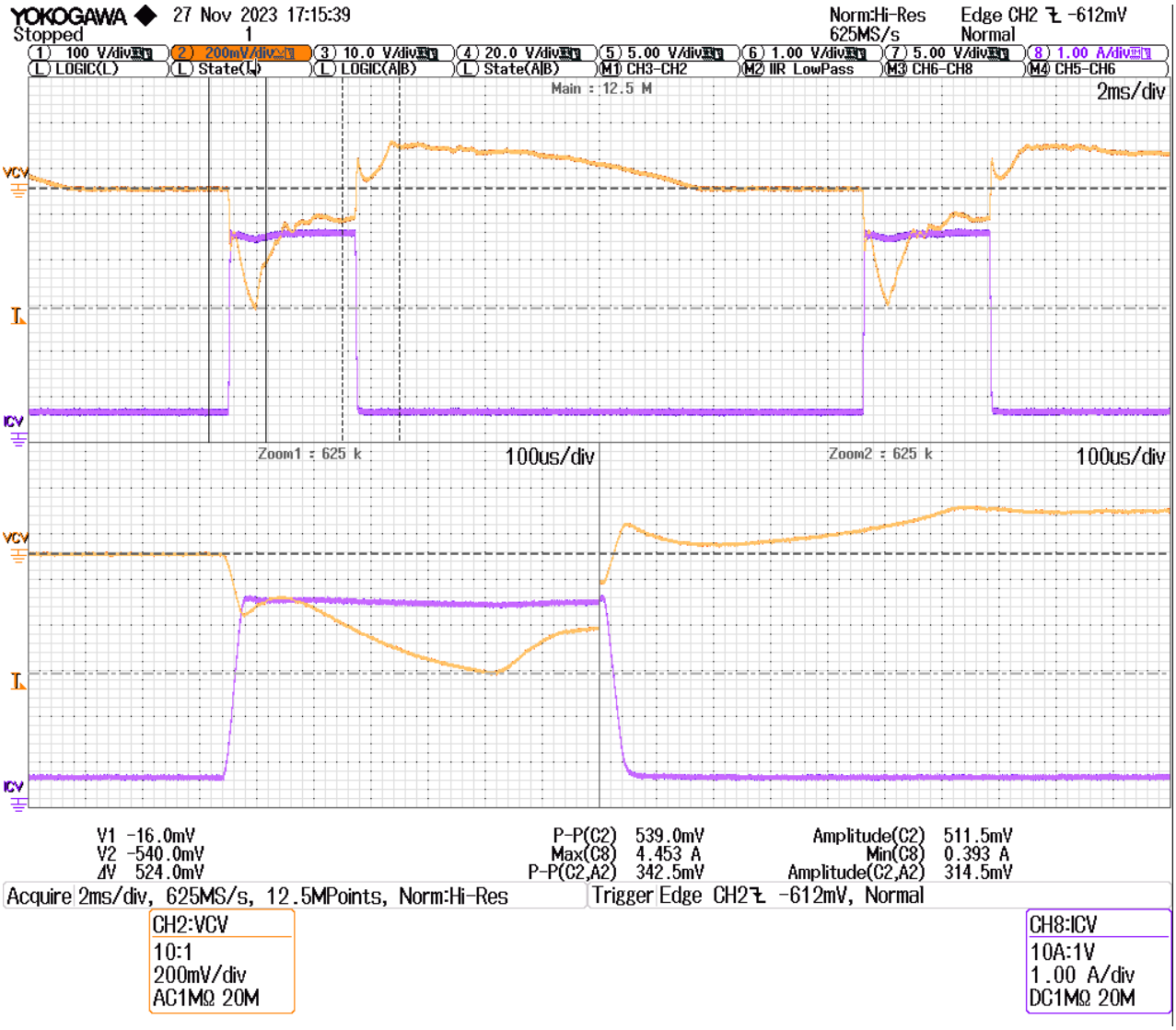


Figure 25 – CV (12 V) Output - Load Transient under nominal LED load at 265VAC

ICV=0.5A-4.5A; Undershoot 539mV,4.49% ; Overshoot=342mV,2.85%

CH2: V_{CV} , CH8: I_{CV}

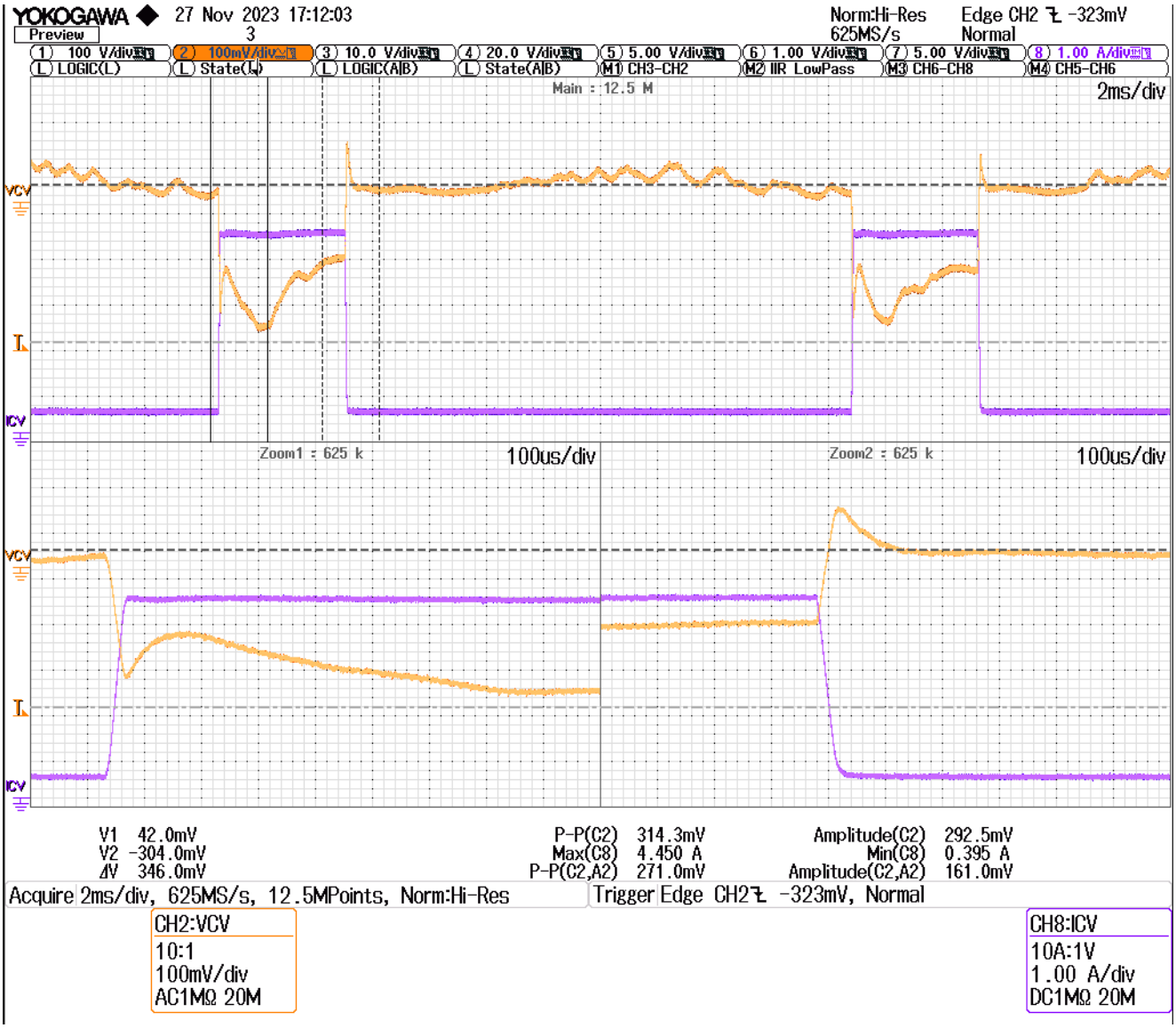


Figure 26 – CV (12 V) Output - Load Transient under 10% duty on LED load at 265VAC

ICV=0.5A-4.5A; Undershoot 314mV,2.61% ; Overshoot=271mV,2.25%

CH2: V_{CV} , CH8: I_{CV}

9.18 Switching Waveforms

9.18.1 Primary Switch Maximum Voltage

Voltages on the primary fet has been measured at 265VAC and 90VAC under nominal and peak load.

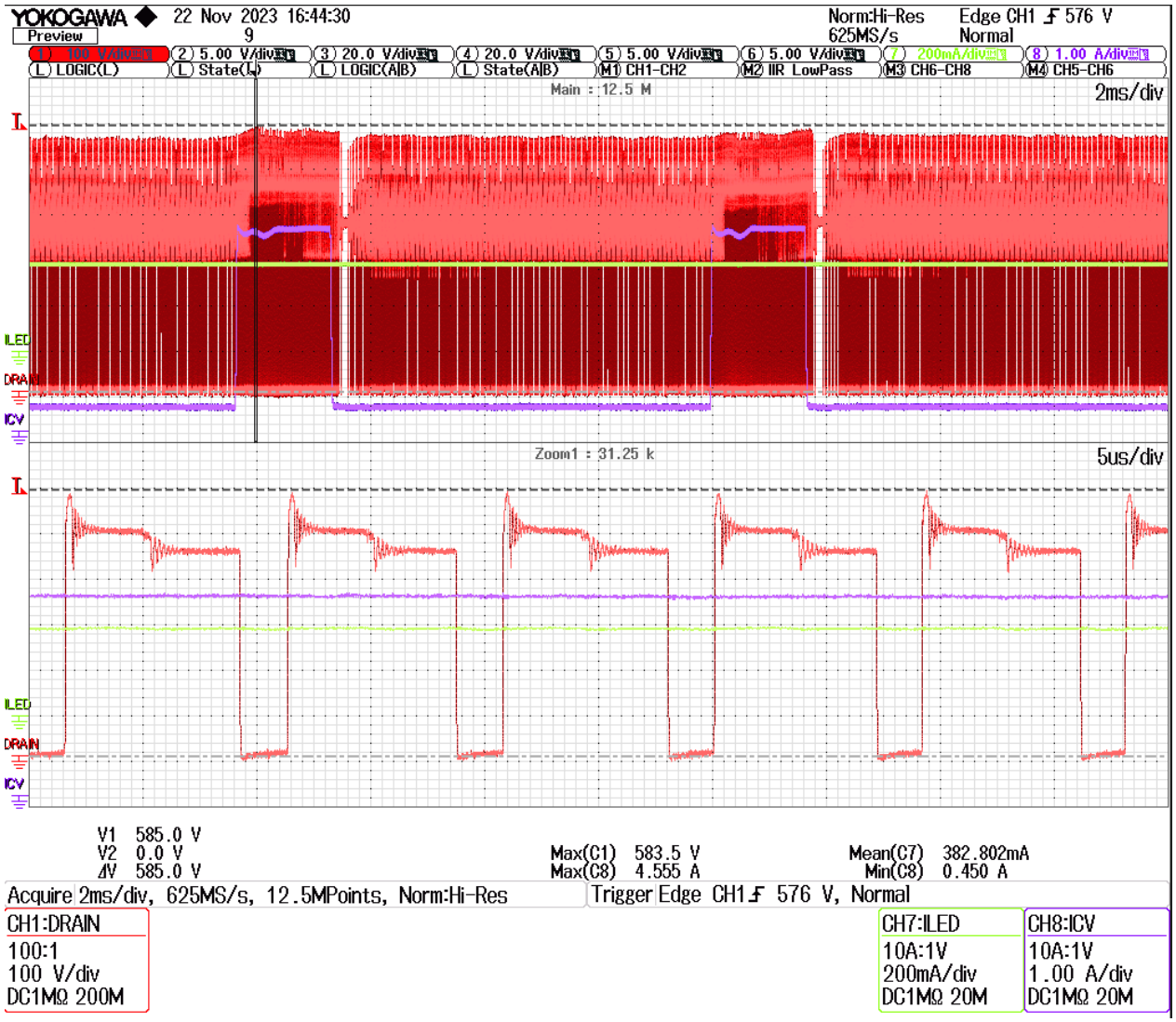


Figure 27 – Primary Switch Voltage under peak load at 265VAC

CH1: V_{drain} , CH7: I_{led} , CH8: I_{cv}

Maximum D-S voltage across the primary switch is 585V.

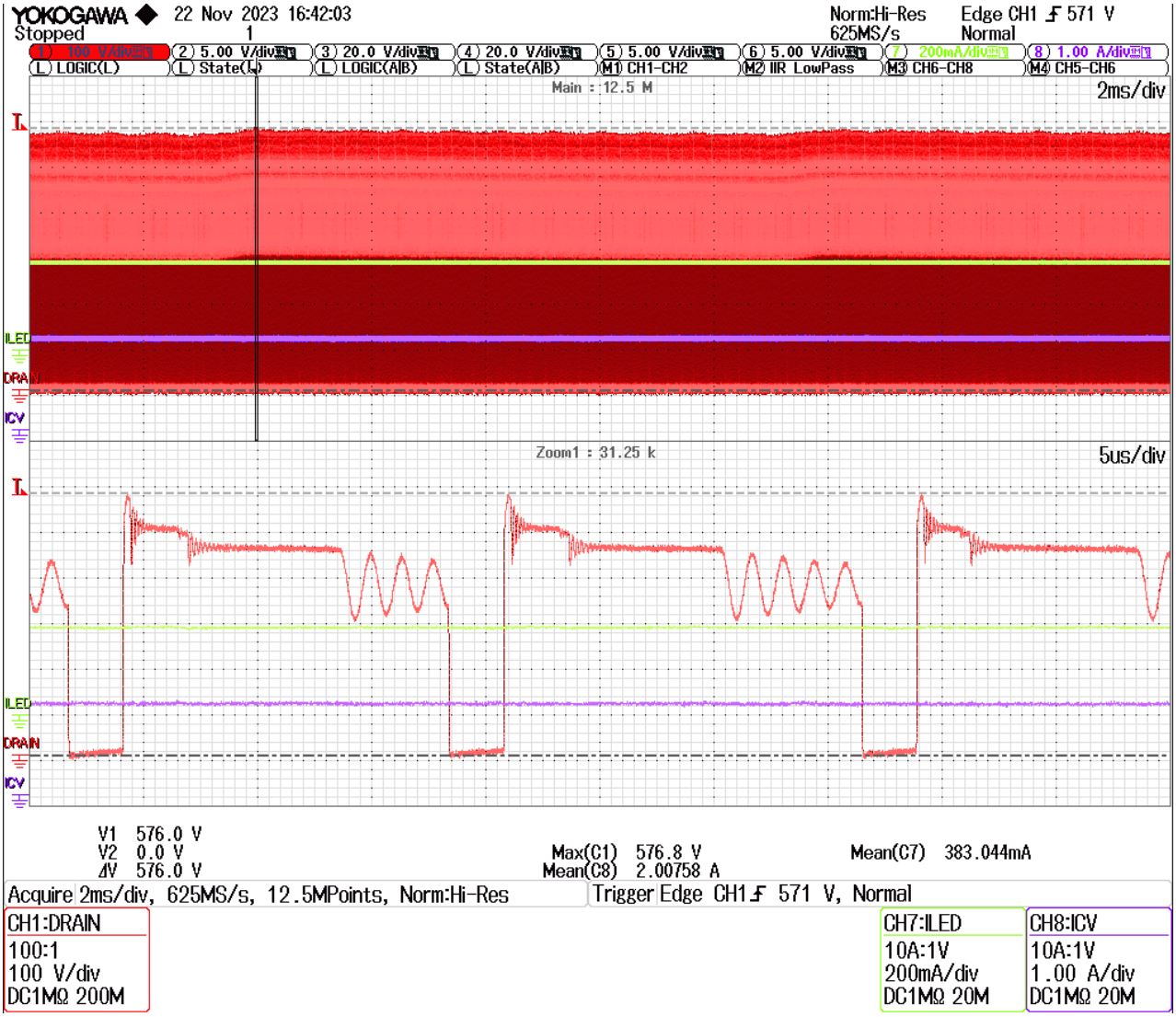


Figure 28 – Primary Switch Voltage under nominal load at 265VAC

CH1: V_{drain} , CH7: I_{led} , CH8: I_{cv}

Maximum D-S voltage across the primary switch is 577V.

Figure 29 – Primary Switch Voltage under peak load at 90VAC

CH1: V_{drain} , CH7: I_{led} , CH8: I_{cv}

Maximum D-S voltage across the primary switch is 344V.

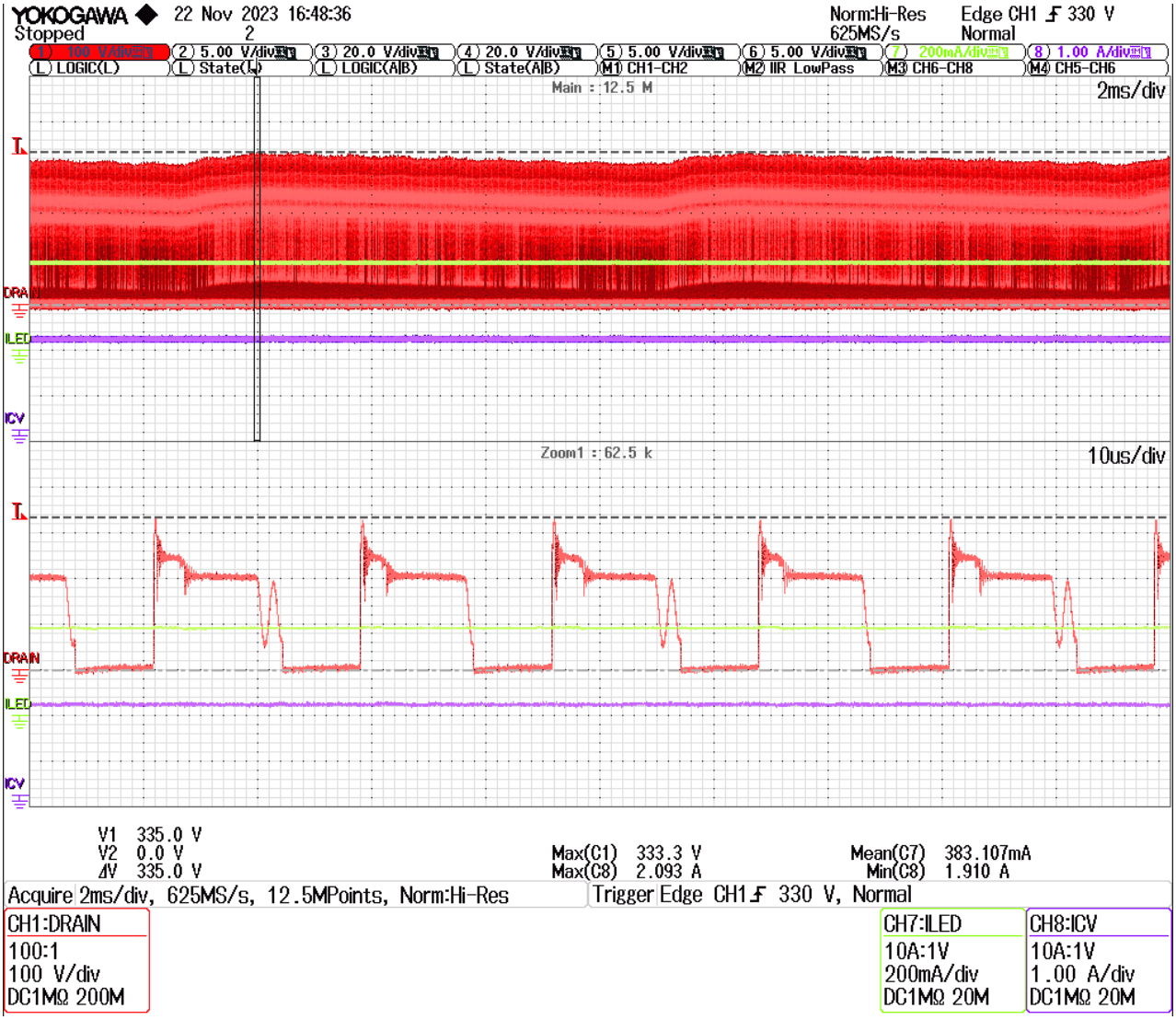


Figure 30 – Primary Switch Voltage under nominal load at 90VAC

CH1: V_{drain} , CH7: I_{led} , CH8: I_{cv}

Maximum D-S voltage across the primary switch is 333V.

9.18.2 Primary Switching Frequency

The primary switching frequency of the converter varies depending on line and load conditions. It was measured under peak load at minimum line input of 90 VAC. The maximum switching frequency occurs at the minimum DC input (110 kHz).LED channel has its nominal current , 380mA and CV channel has a peak current which is 4.5A with a 40% duty and 100Hz load step conditions.

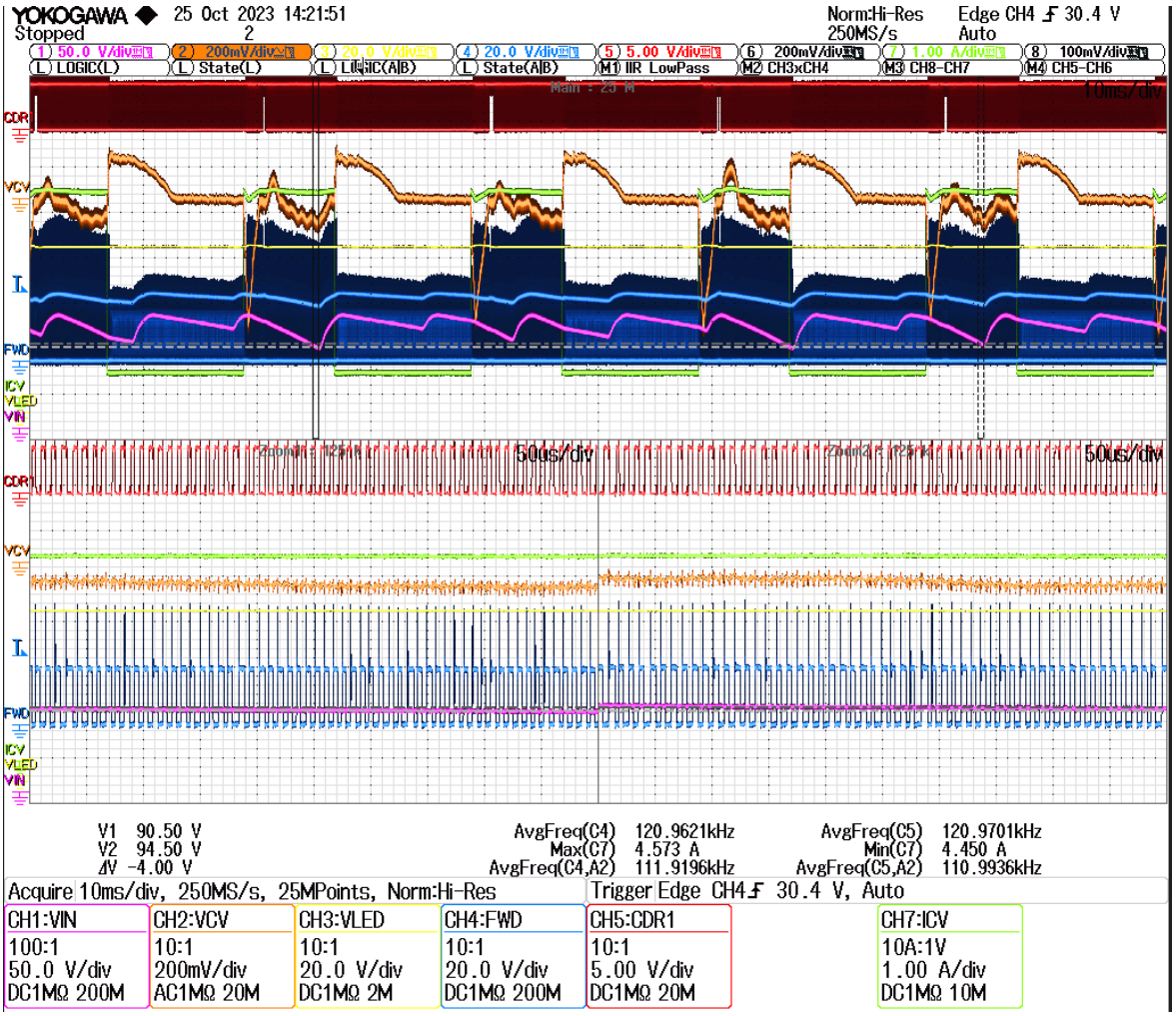


Figure 31 – Max Primary Switching Frequency (110kHz)

9.18.3 Transformer Current Waveforms

CH1	SR Current
CH5	Primary Current
CH7	ICV1
CH8	ILED

Table 1 – Scope Channel Allocation (This Section).

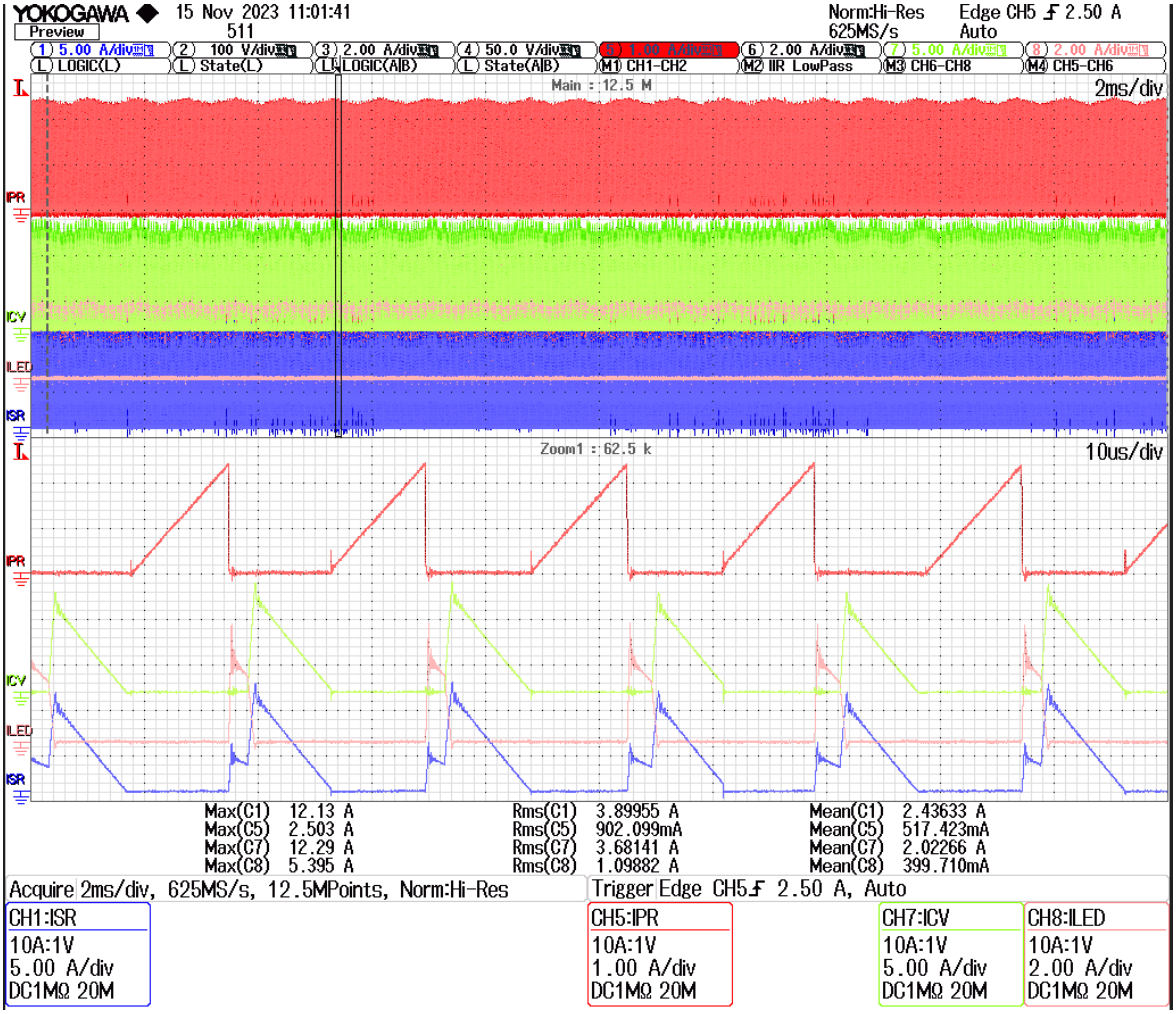


Figure 32 – Transformer Winding Currents at Minimum Input Voltage.

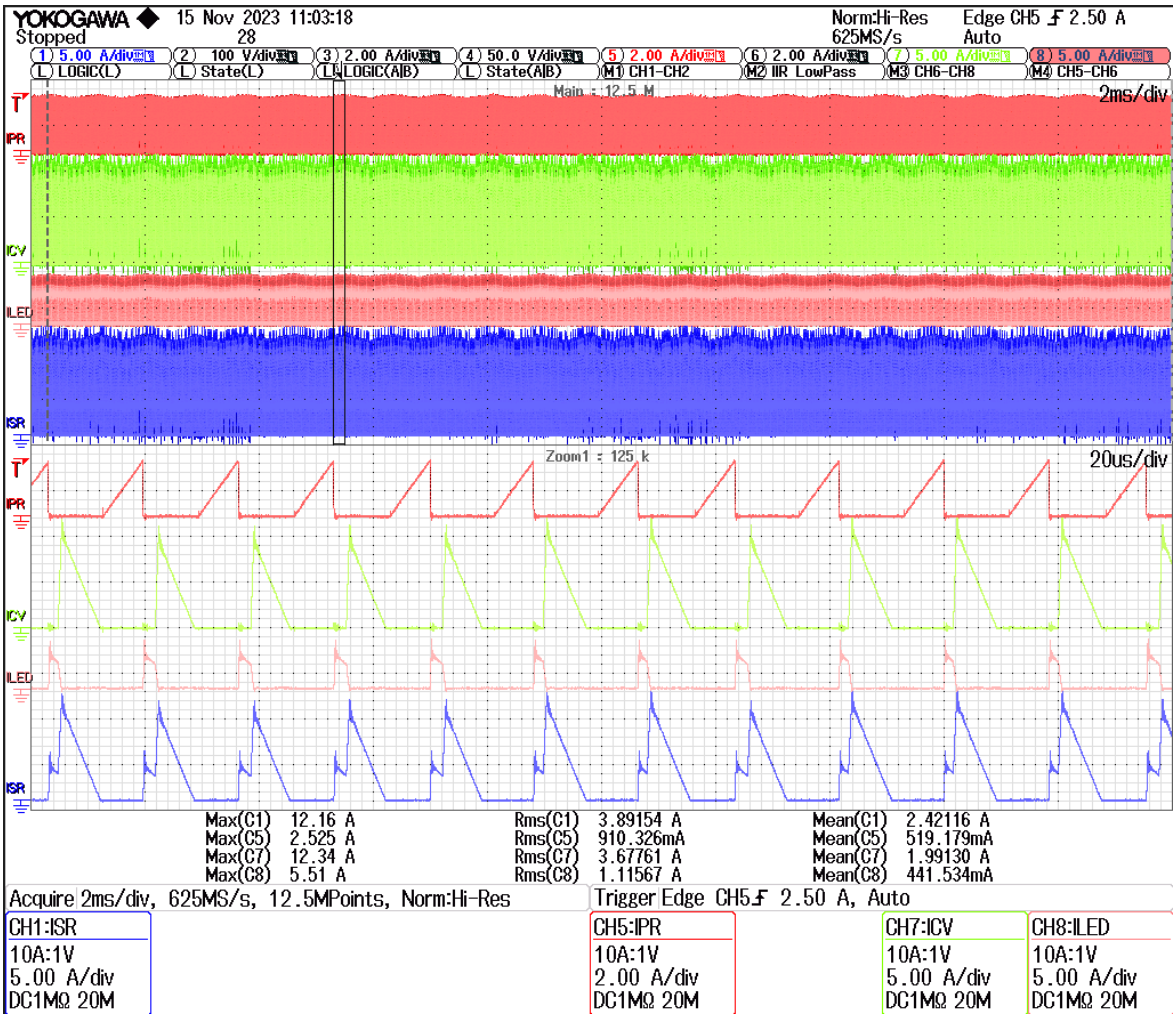


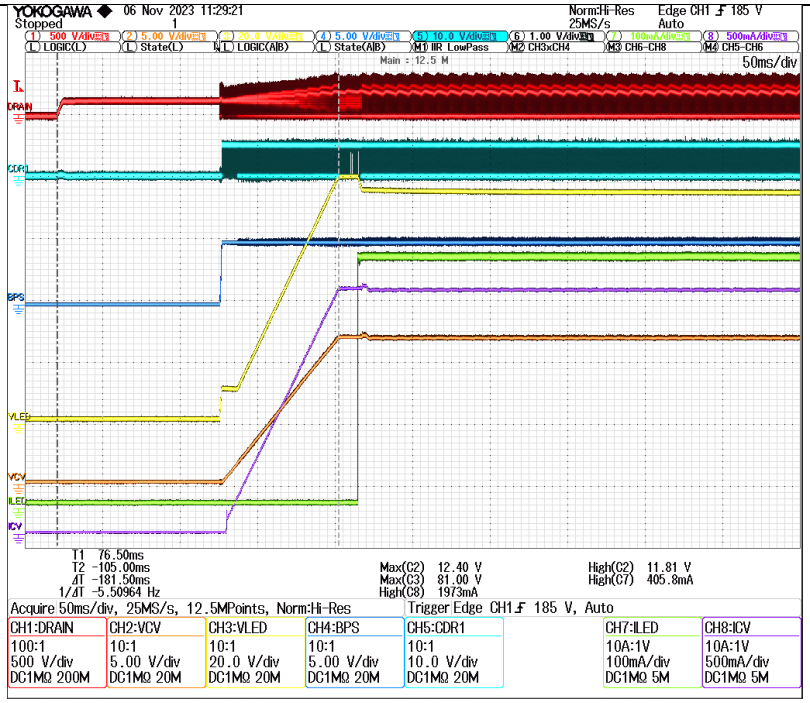
Figure 33 – Transformer Currents – Detailed View.

9.19 Start-Up

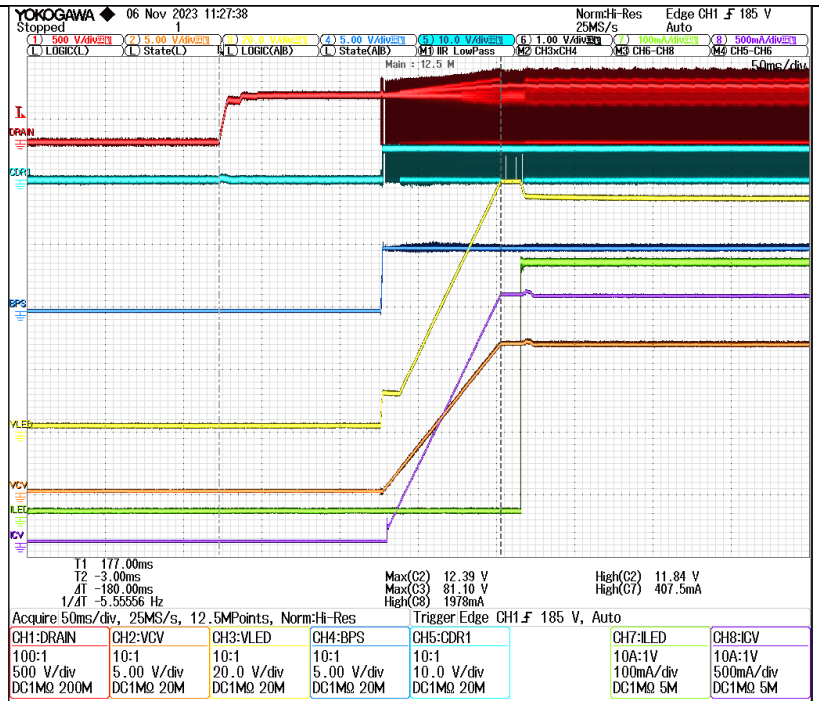
CH1	Drain voltage
CH2	CV voltage
CH3	LED voltage
CH4	BPS voltage
CH5	SEL GATE
CH7	LED current
CH8	CV current

Table 5 – Scope Channel Allocation (This Section).

9.19.1 Full Load Start-up



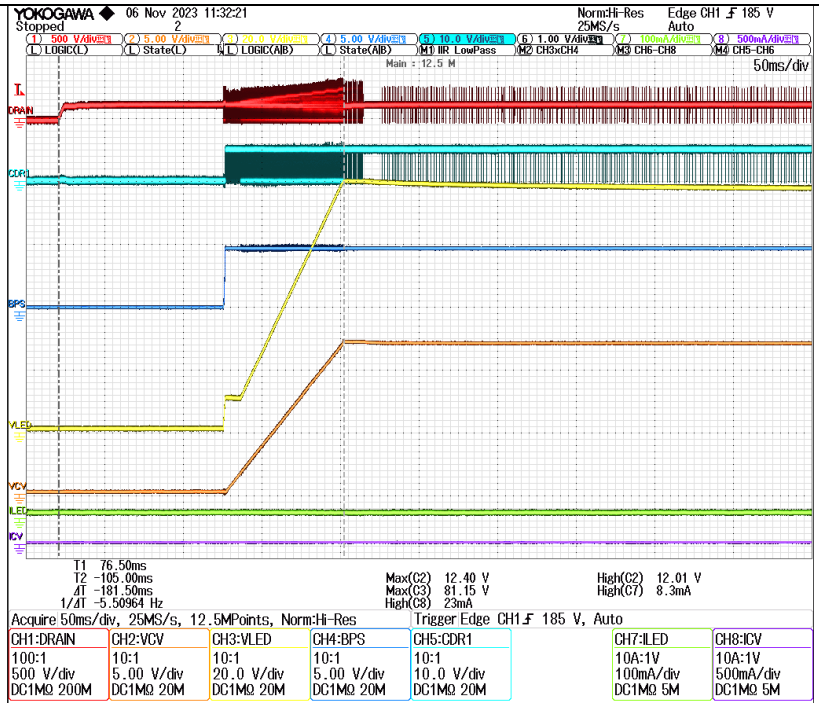
Line input 90 VAC, start-up delay 105 ms, start-up time 181 ms.



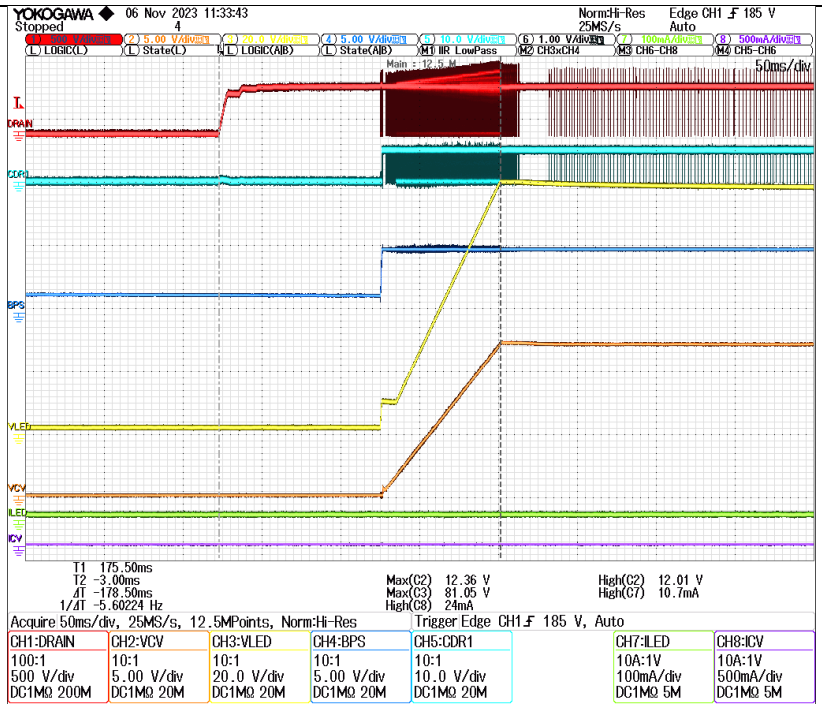
Line input 265 VAC, start-up delay 105 ms, start-up time 180 ms.

Figure 34 – Full Load Start-up.

9.19.2 No-Load Start-up



Line input 90 VAC, start-up delay 105 ms, start-up time 181 ms.



Line input 265 VAC, start-up delay 105 ms, start-up time 178 ms.

Figure 35 – No-load Start-up.

9.19.3 Start-up Under CV and LED Fault Conditions

CH2	VCV
CH3	VLED
CH4	FWD
CH5	CDR1
CH8	ILED

Table 6 – Scope Channel Allocation (This Section).

The converter was tested for start-up under two types of single fault conditions, namely:

- Short-circuit to GND at CV output;
- Short-circuit to Vled- at Vled+ output;
- Open circuit of feedbacks;

In all cases, the converter protection prevented any permanent damage to its components. The line fuse F1 remained intact. The converter went into auto restart for the duration of the fault condition. It resumed normal operation after the fault condition was removed.

Details of the start-up behavior under those fault conditions are shown in Figure 36 to Figure 51.

CV=0A	**Faults Before Start-up**							
LED=0A	**CV short to GND**		**VLED+ short to VLED-**		**CV FB open**		**LED FB open**	
	90 V	**265 V**	**90 V**	**265 V**	**90 V**	**265 V**	**90 V**	**265 V**
Protect. Def.	PLIM/ Request Not Clear	PLIM/ Request Not Clear	LED Fault (LED=380mA)	LED Fault LED=380mA)	PLIM/ Request Not Clear	PLIM/ Request Not Clear	LED Fault	LED Fault

CV=2A	**Faults Before Start-up**							
LED=380mA	**CV short to GND**		**VLED+ short to VLED-**		**CV FB open**		**LED FB open**	
	90 V	**265 V**	**90 V**	**265 V**	**90 V**	**265 V**	**90 V**	**265 V**
Protect. Def.	PLIM/ Request Not Clear	OVP	LED Fault	LED Fault	PLIM/ Request Not Clear	PLIM/ Request Not Clear	LED Fault	LED Fault

Table 7 – Protection Definitions Under Fault Conditions.

9.19.3.1 Start-up Under CV Fault Conditions

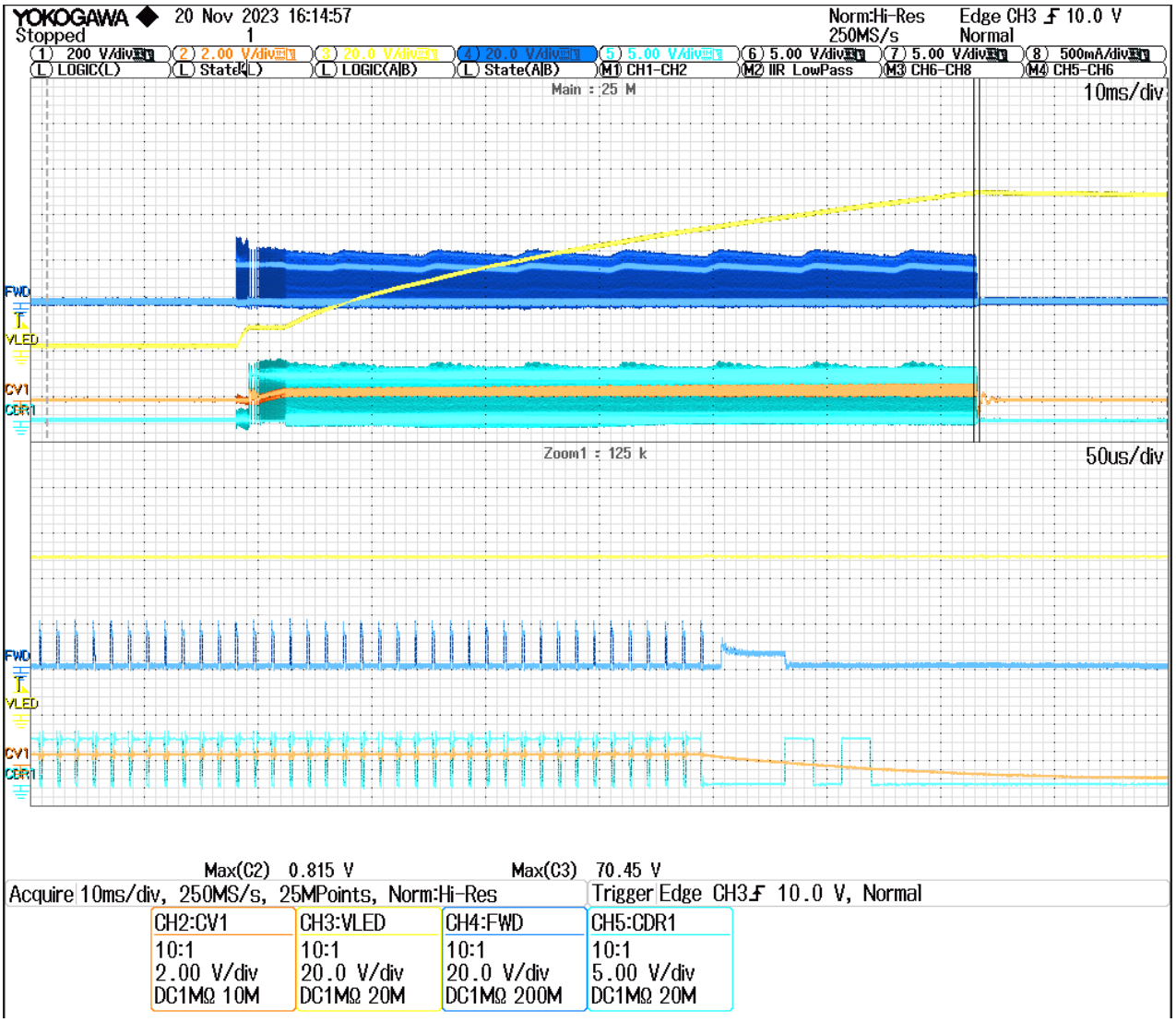


Figure 36 – Start-up With CV1 Shorted to GND. Line Input 90V , CV&LED No-Load.

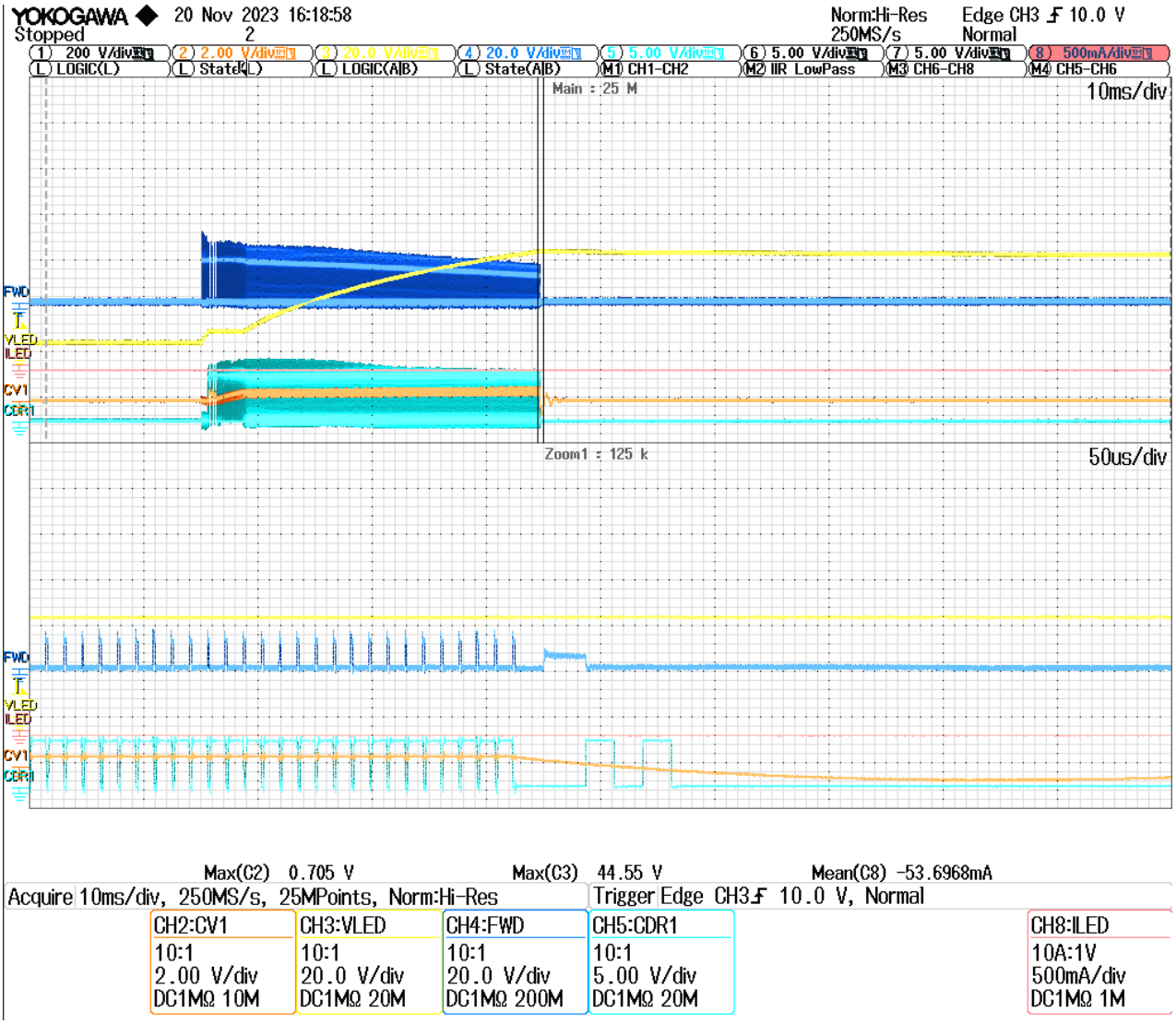


Figure 37 – Start-up With CV1 Shorted to GND. Line Input 265V , CV&LED No-Load.

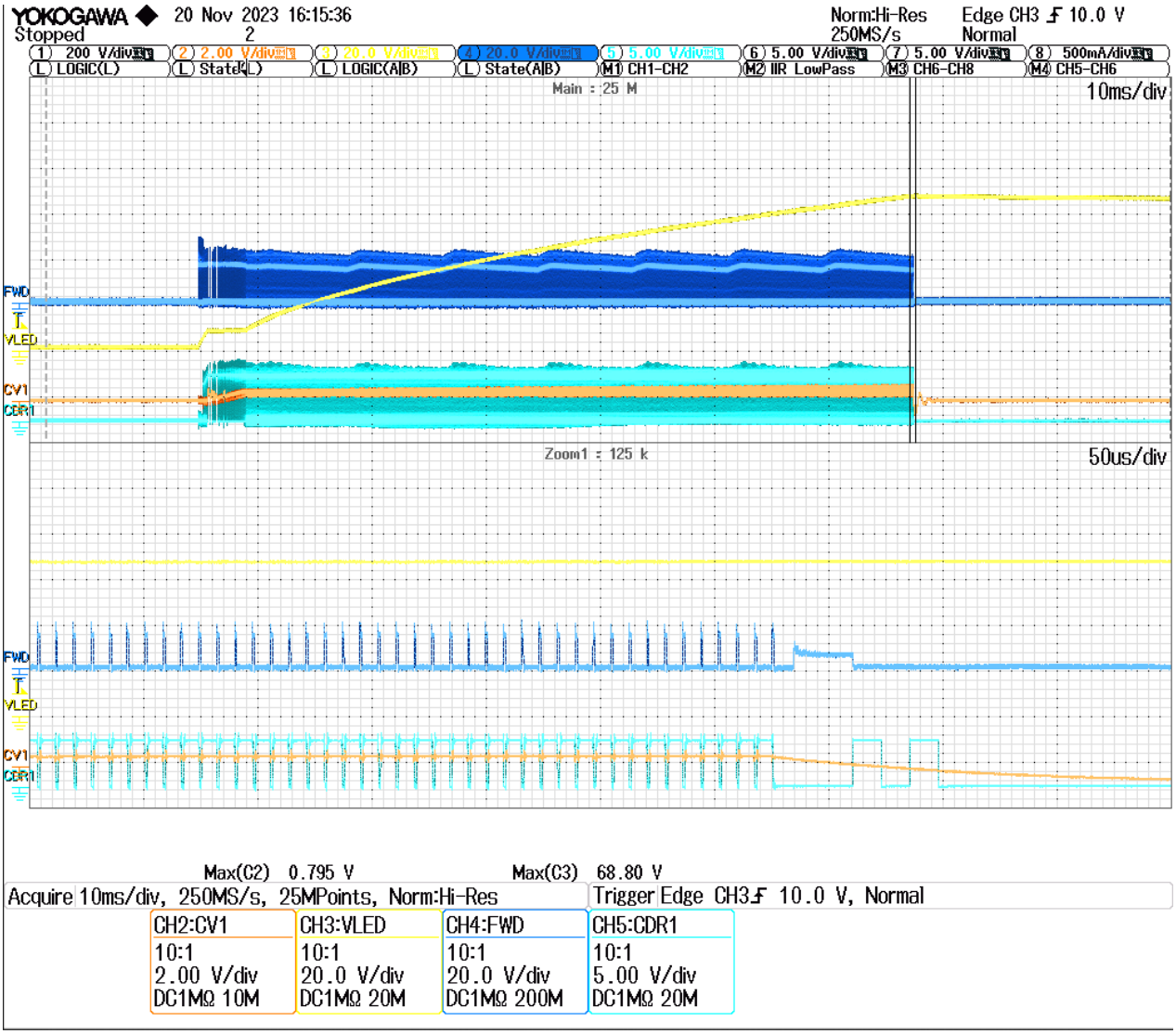


Figure 38 – Start-up With CV1 Shorted to GND. Line Input 90V, CV&LED Nominal Load.

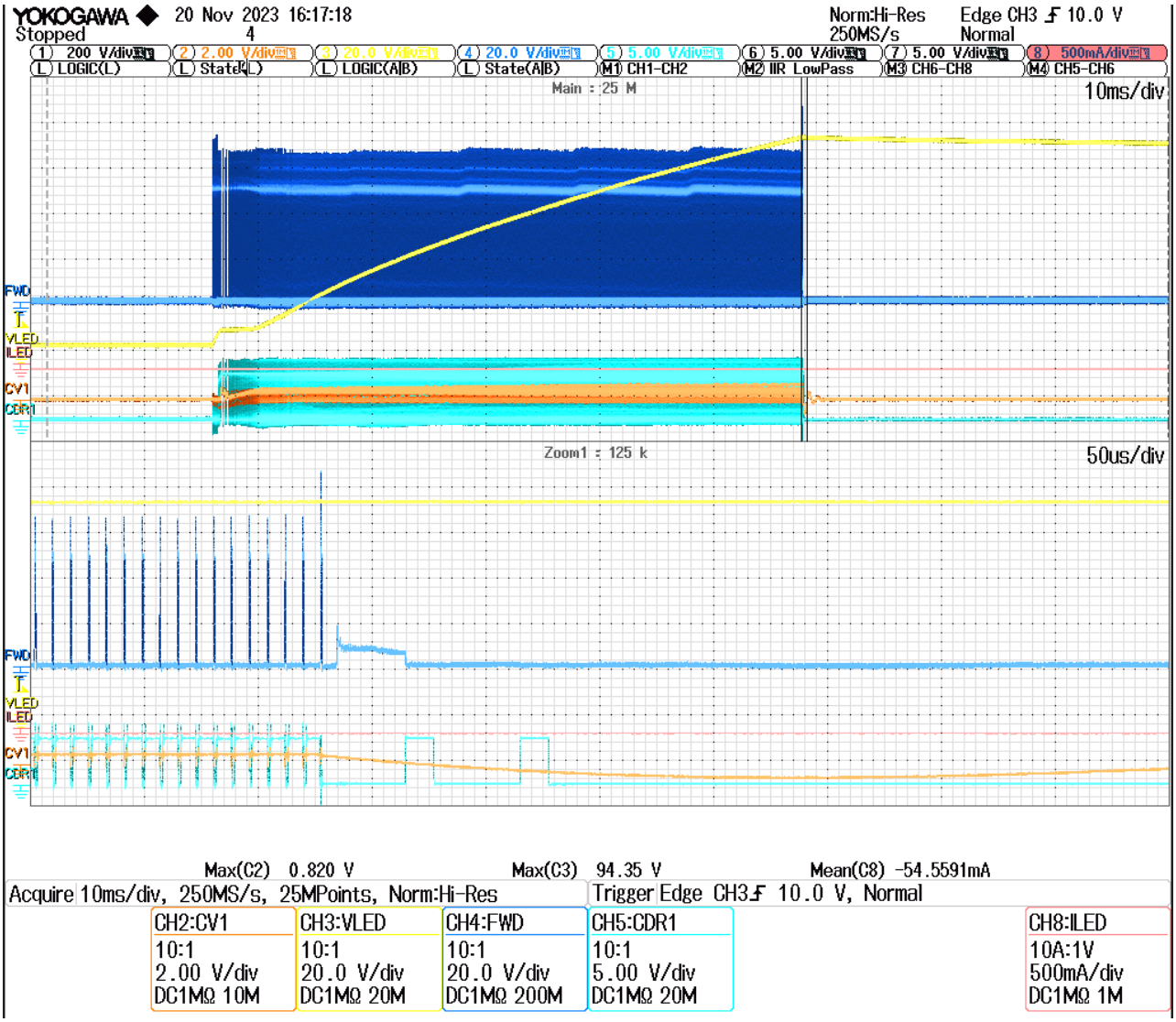


Figure 39 – Start-up With CV1 Shorted to GND. Line Input 265V , CV&LED Nominal Load.

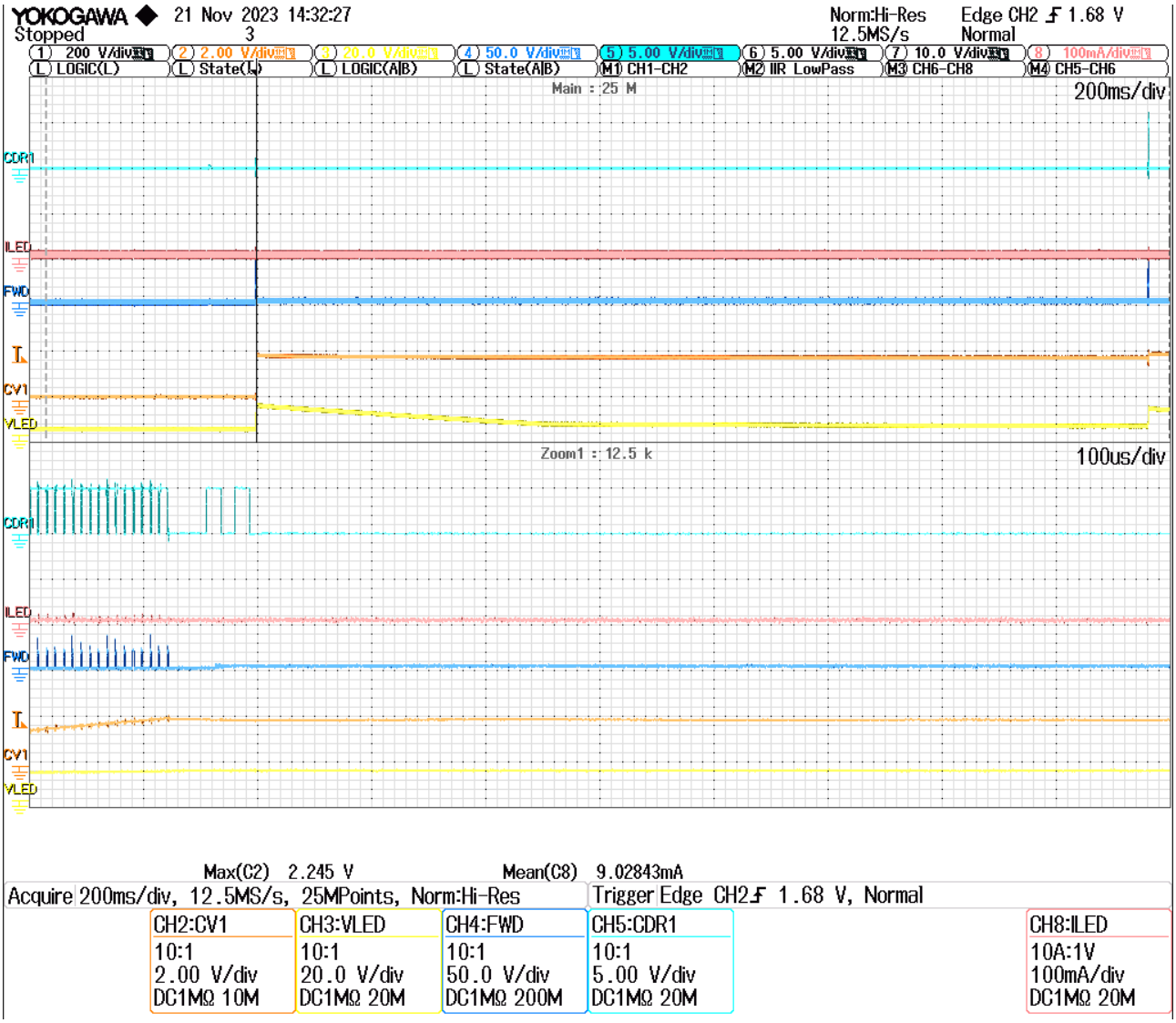


Figure 40 – Start-up With CV FB Open. Line Input 90V, CV&LED No Load.

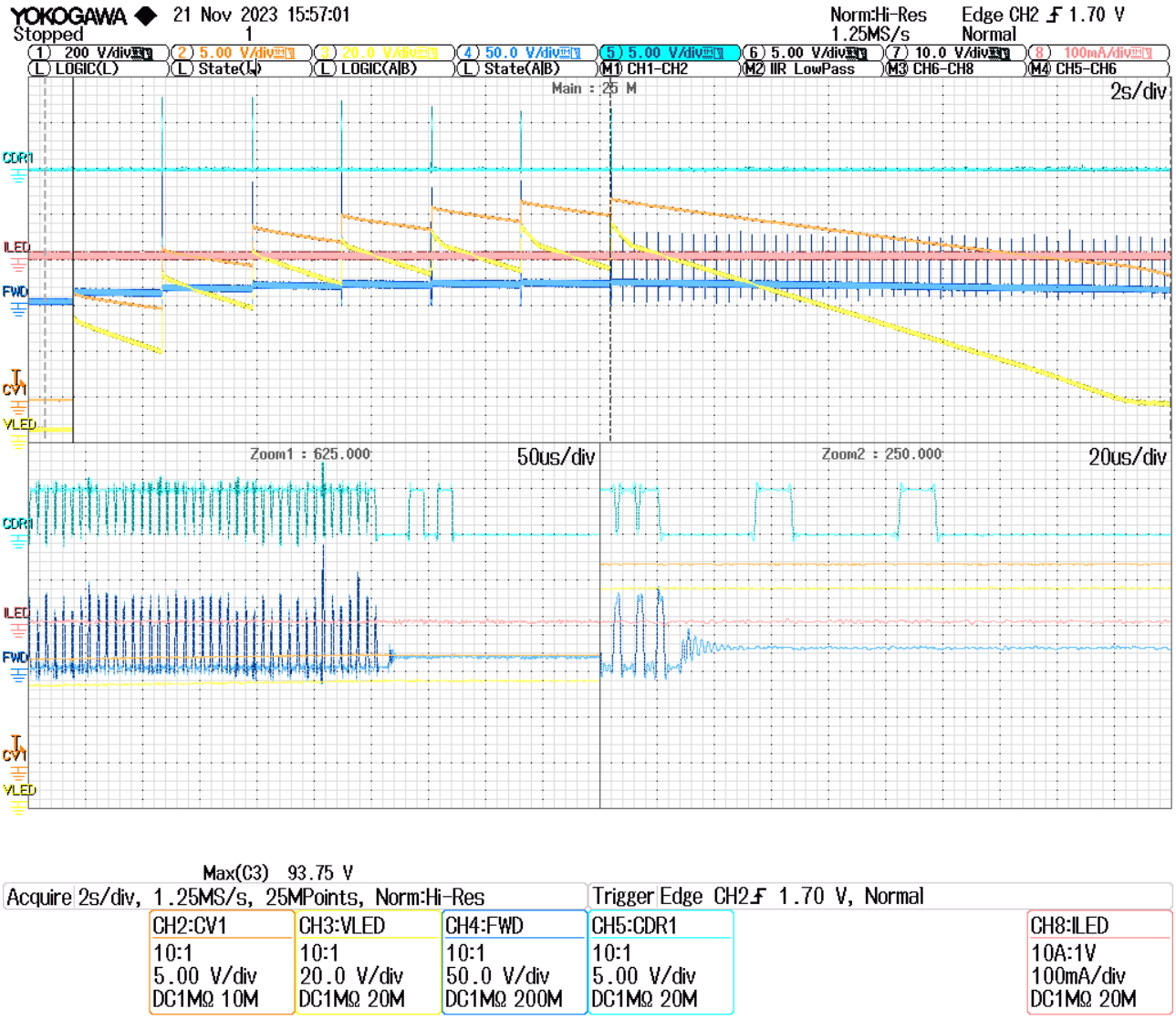


Figure 41 – Start-up With CV FB Open. Line Input 265V , CV&LED No-Load.

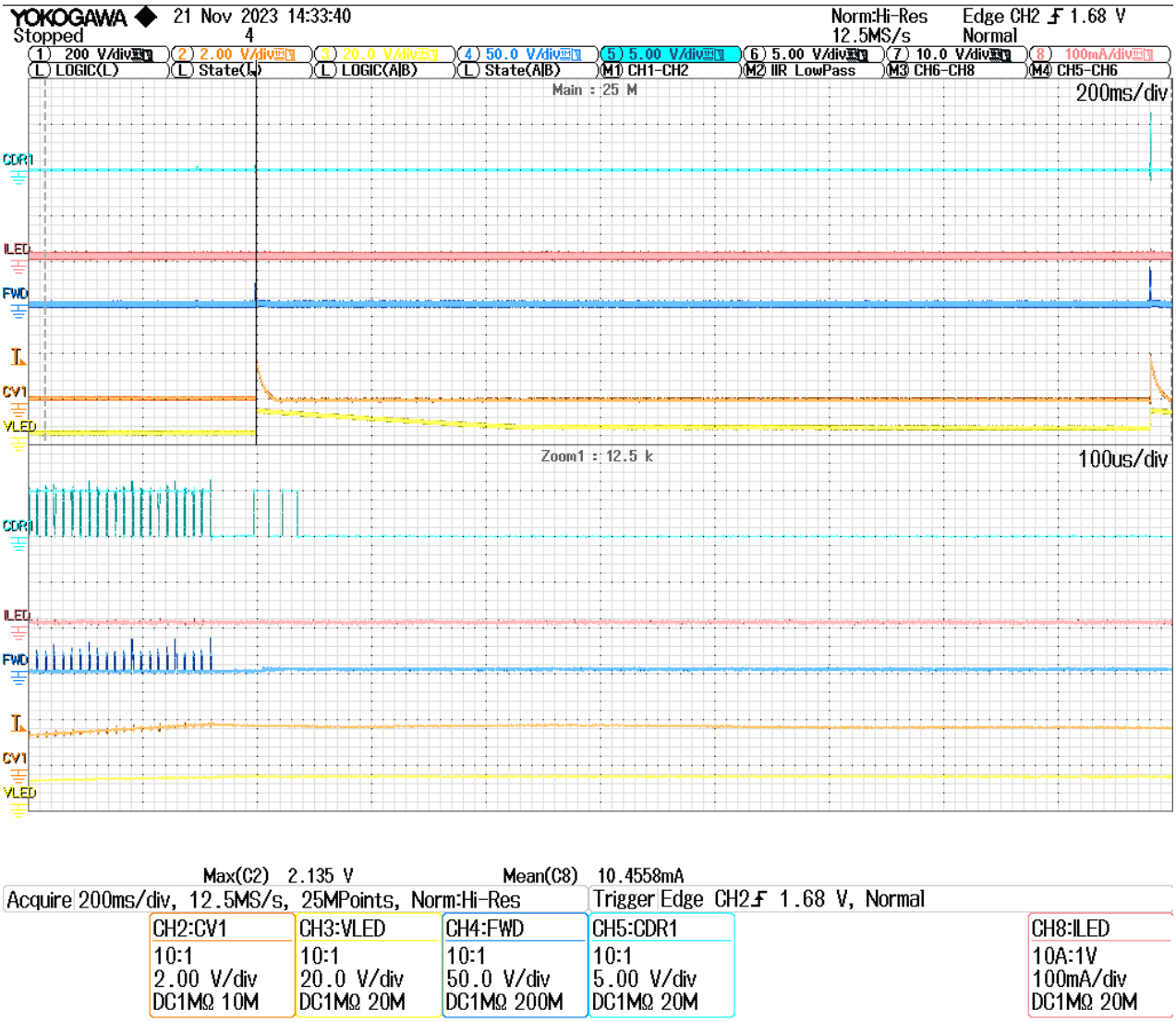


Figure 42 – Start-up With CV FB Open. Line Input 90V, CV&LED Nominal Load.

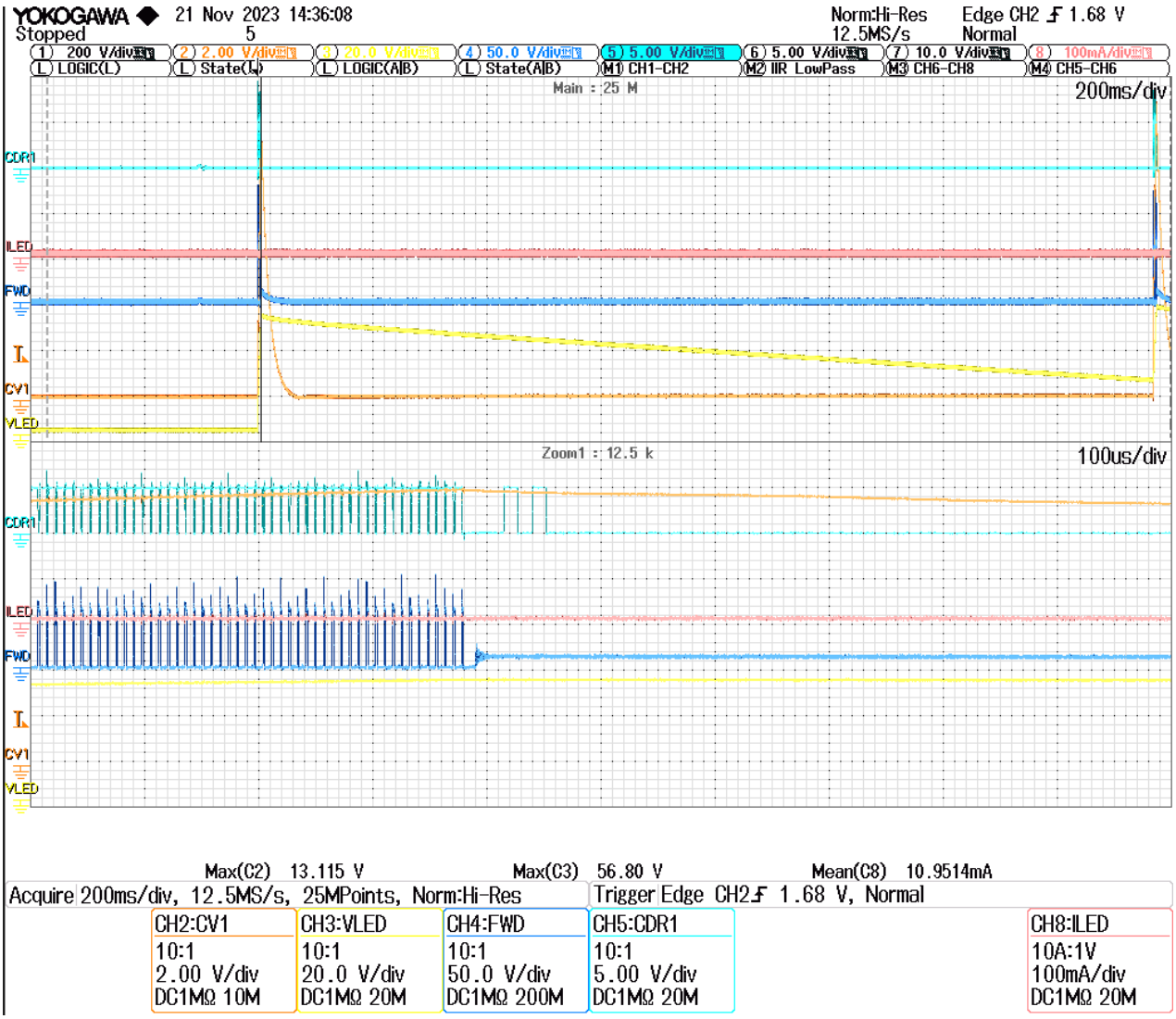


Figure 43 – Start-up With CV FB Open. Line Input 265V, CV&LED Nominal Load.

9.19.3.2 Start-up Under LED Fault Conditions

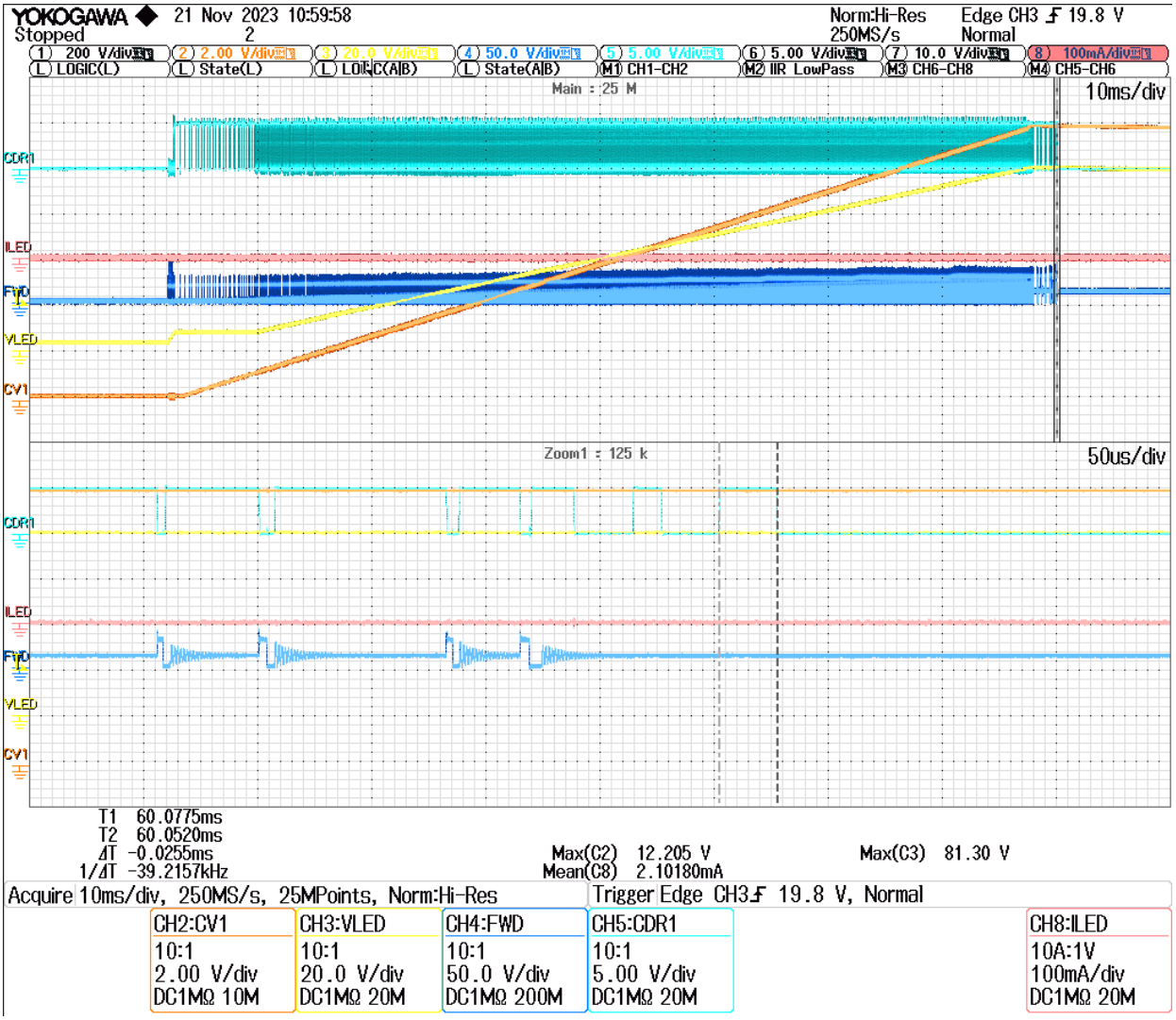


Figure 44 – Start-up With LED Output Shorted to LED Return. Line Input 90 V, CV0A, LED=380mA.

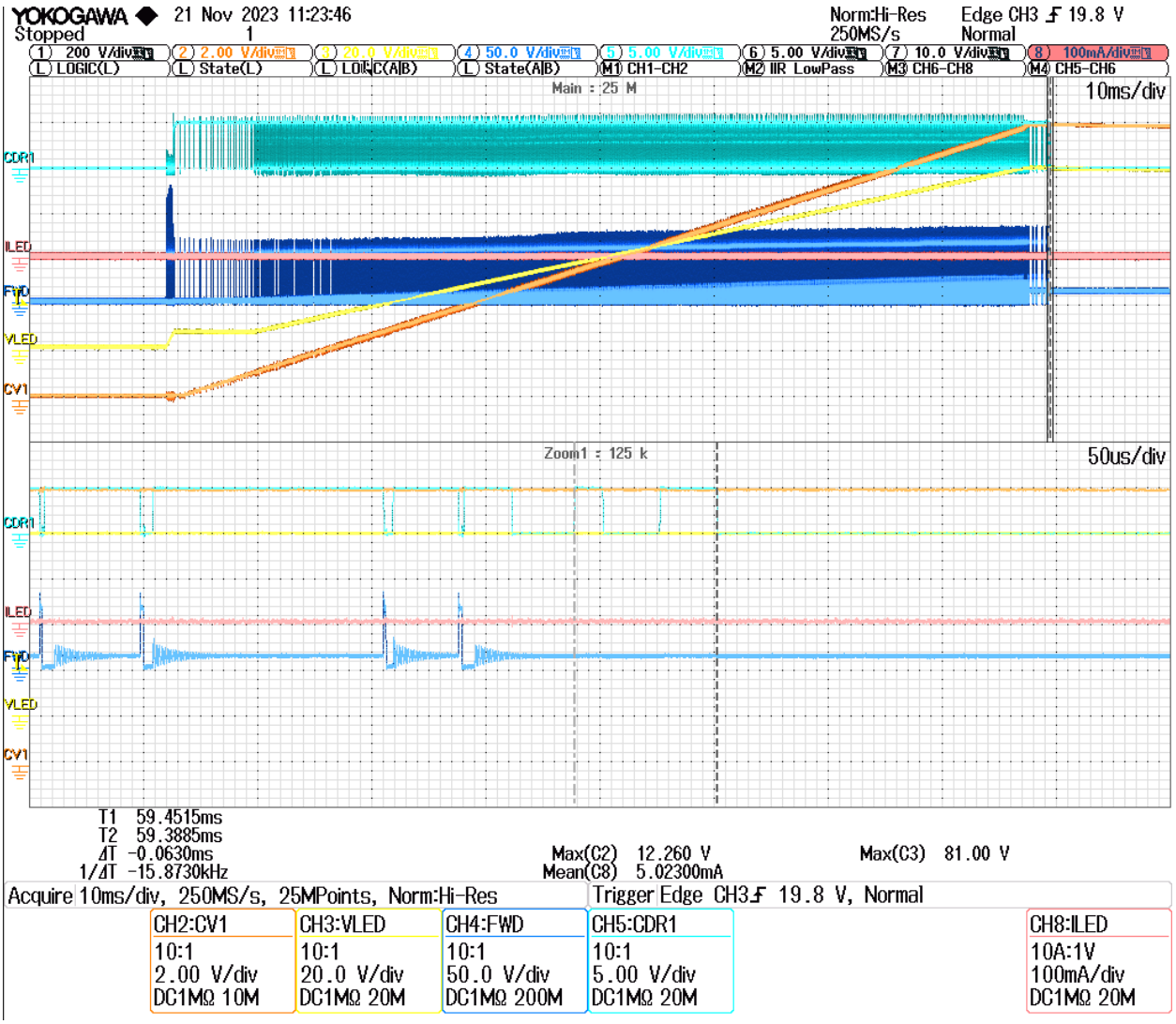


Figure 45 – Start-up With LED Output Shorted to LED Return. Line Input 265 V, CV0A, LED=380mA.

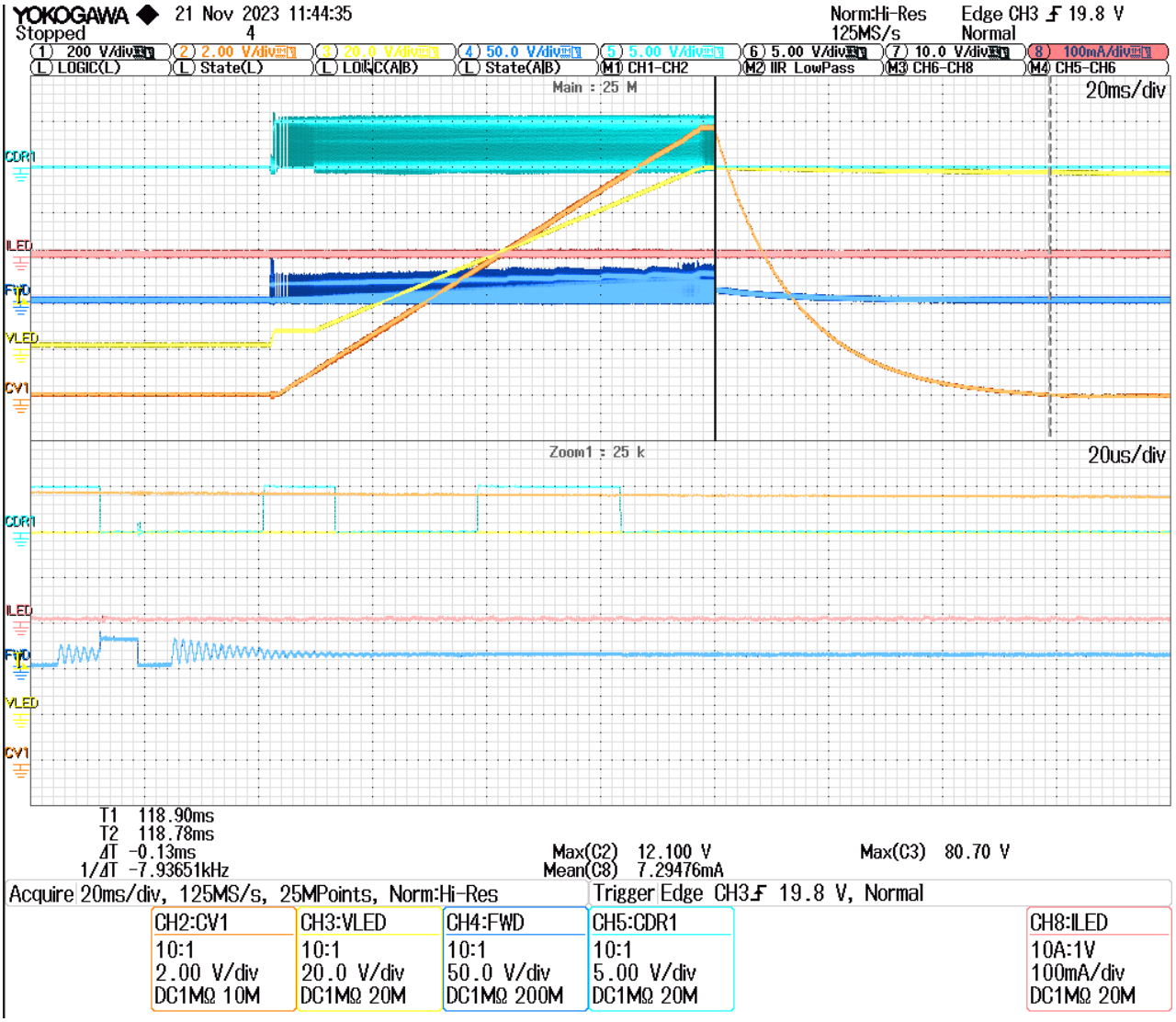


Figure 46 – Start-up With LED Output Shorted to LED Return. Line Input 90 V, CV2A, LED=380mA.

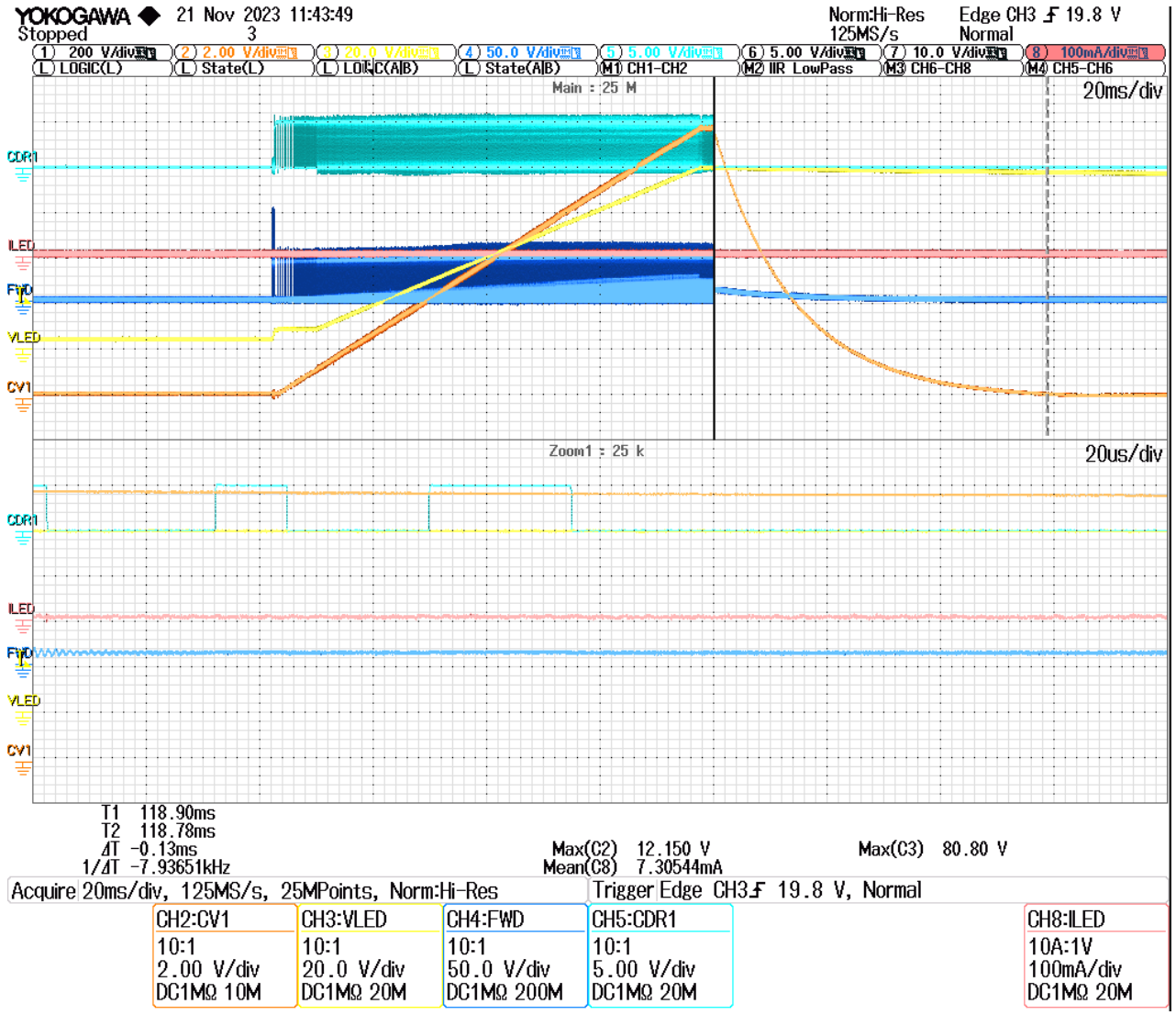


Figure 47 – Start-up With LED Output Shorted to LED Return. Line Input 265 V, CV2A, LED=380mA.

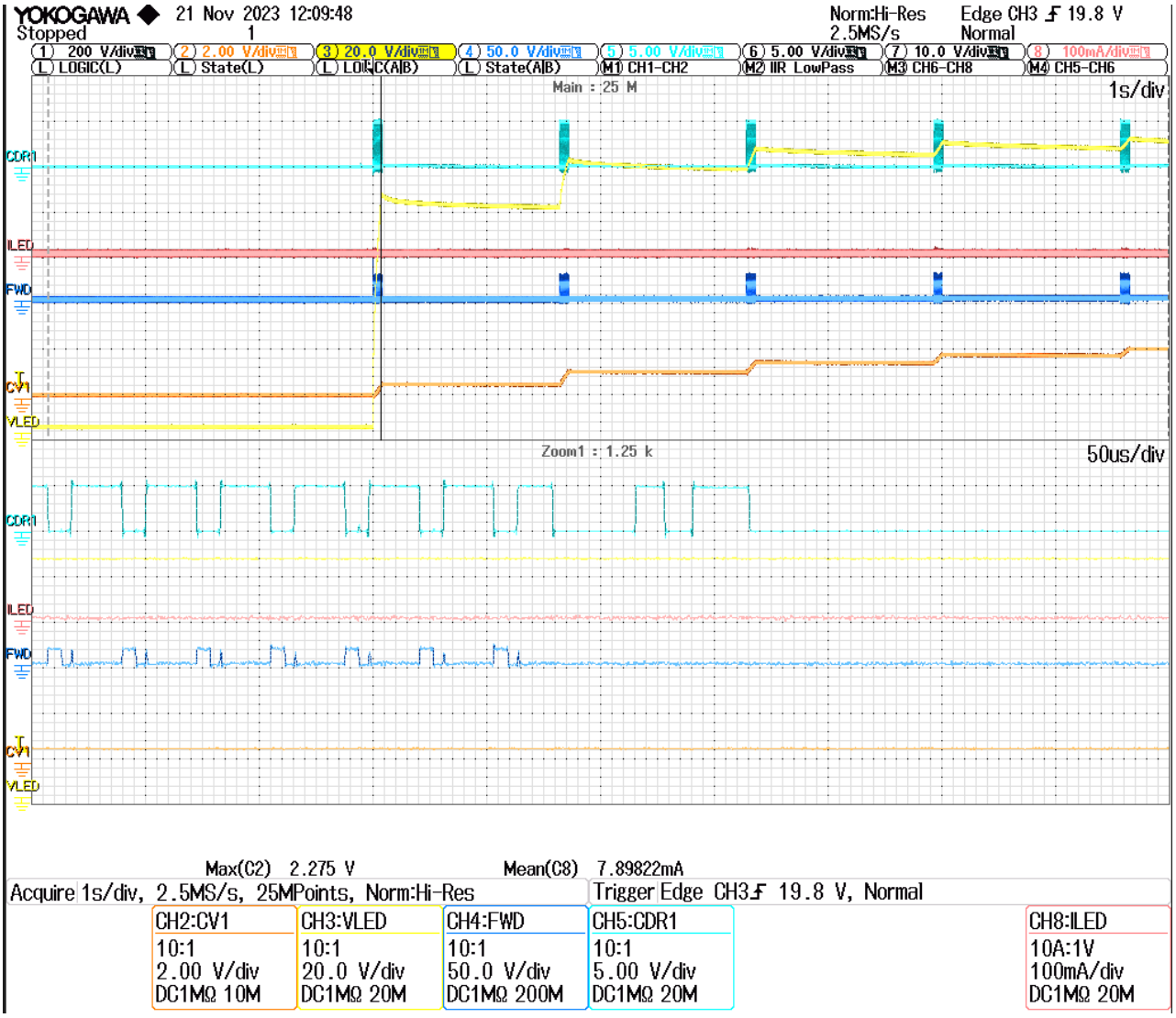


Figure 48 – Start-up With LED FB Open. Line Input 90 V, CV0A, LED=0mA.

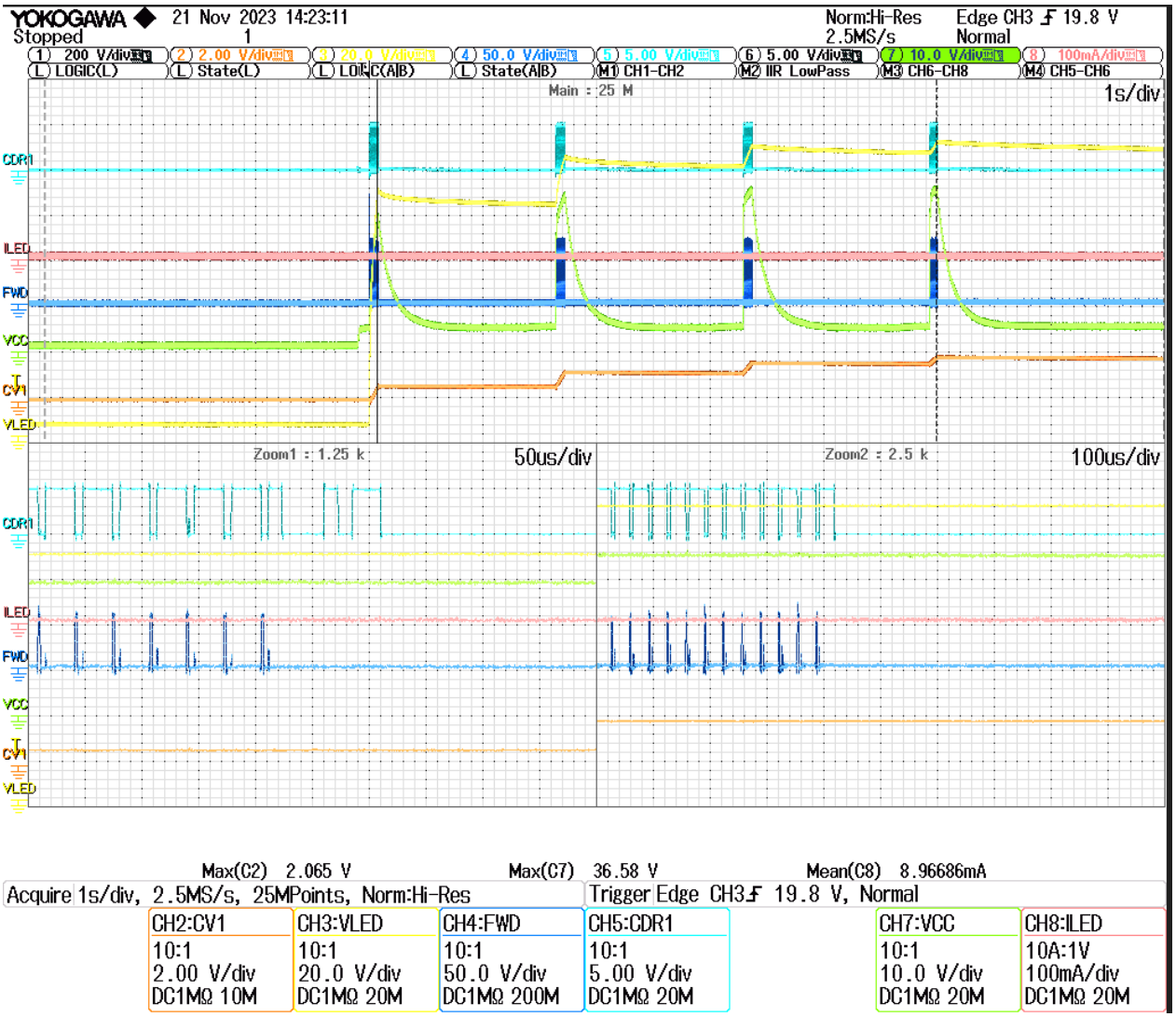


Figure 49 – Start-up With LED FB Open. Line Input 265 V, CV0A, LED=0mA.

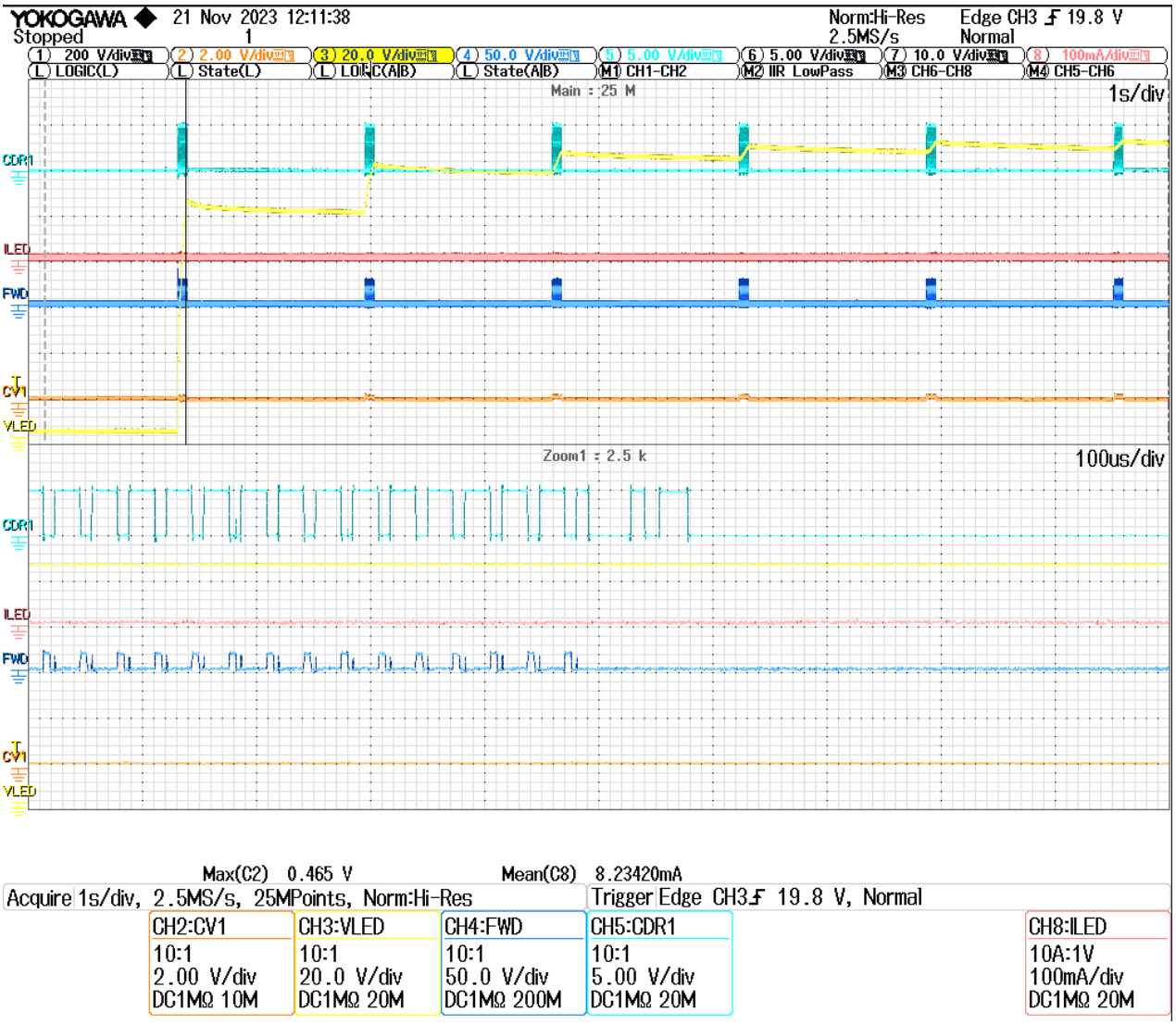


Figure 50 – Start-up With LED FB Open. Line Input 90V, CV2A, LED=380mA.

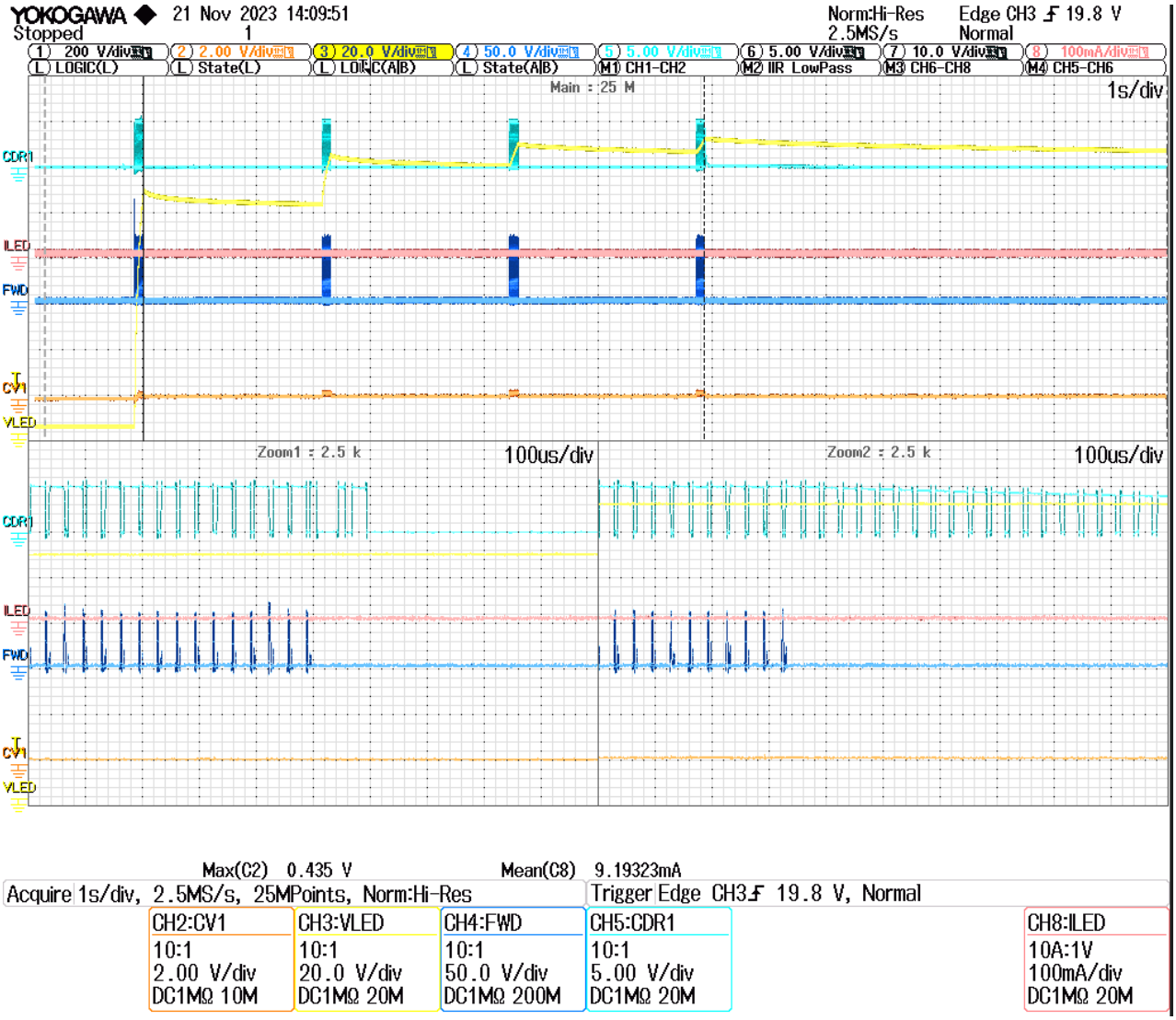


Figure 51 – Start-up With LED FB Open. Line Input 265V, CV2A, LED=380mA.

9.20 Component Peak Voltages

9.20.1 SR Diode Reverse Voltage

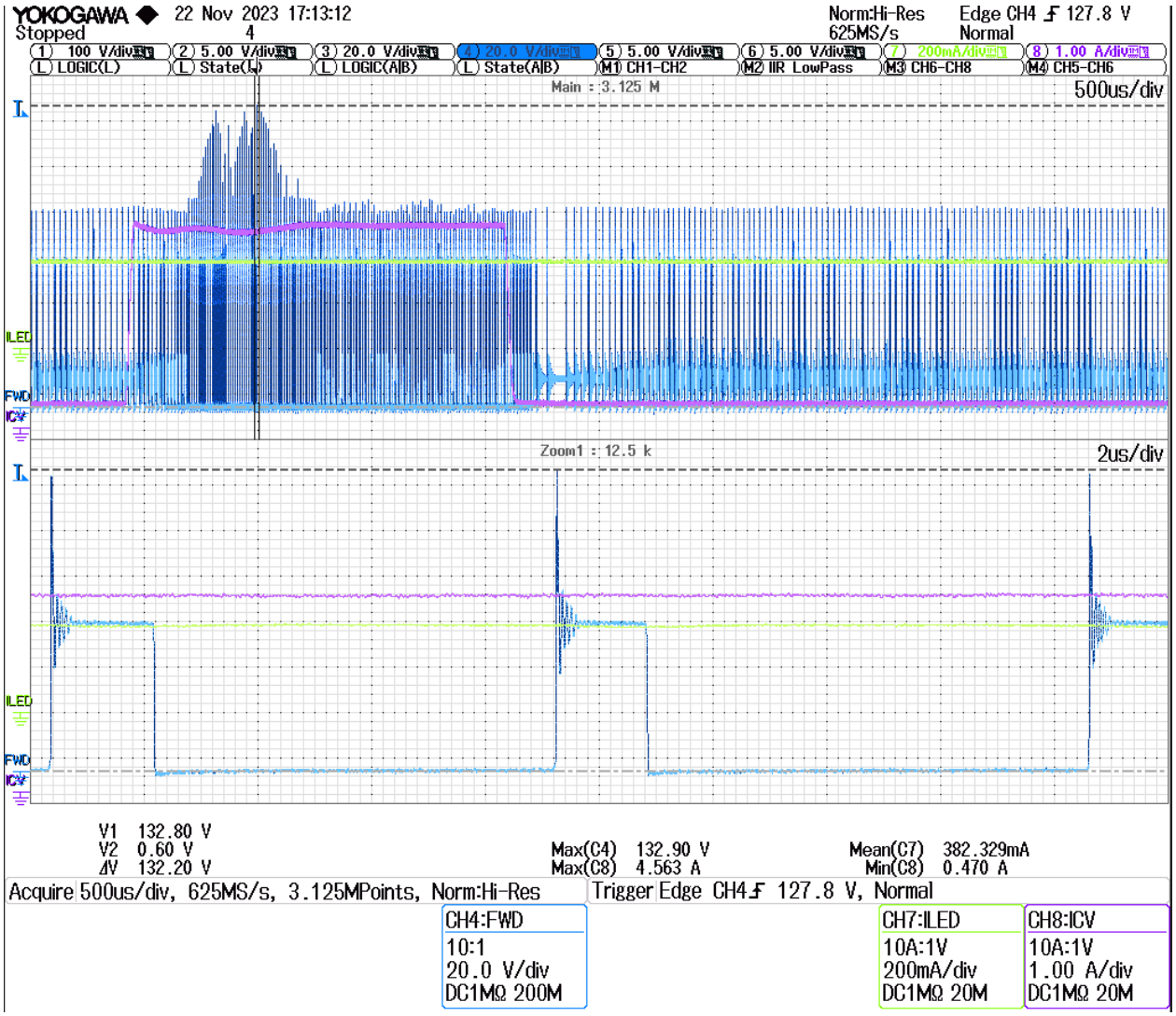


Figure 5221 – SR (D8) Reverse Voltage Under Peak Load at 265VAC.

Ch4: V_{SR} , Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the SR Diode is 133V.

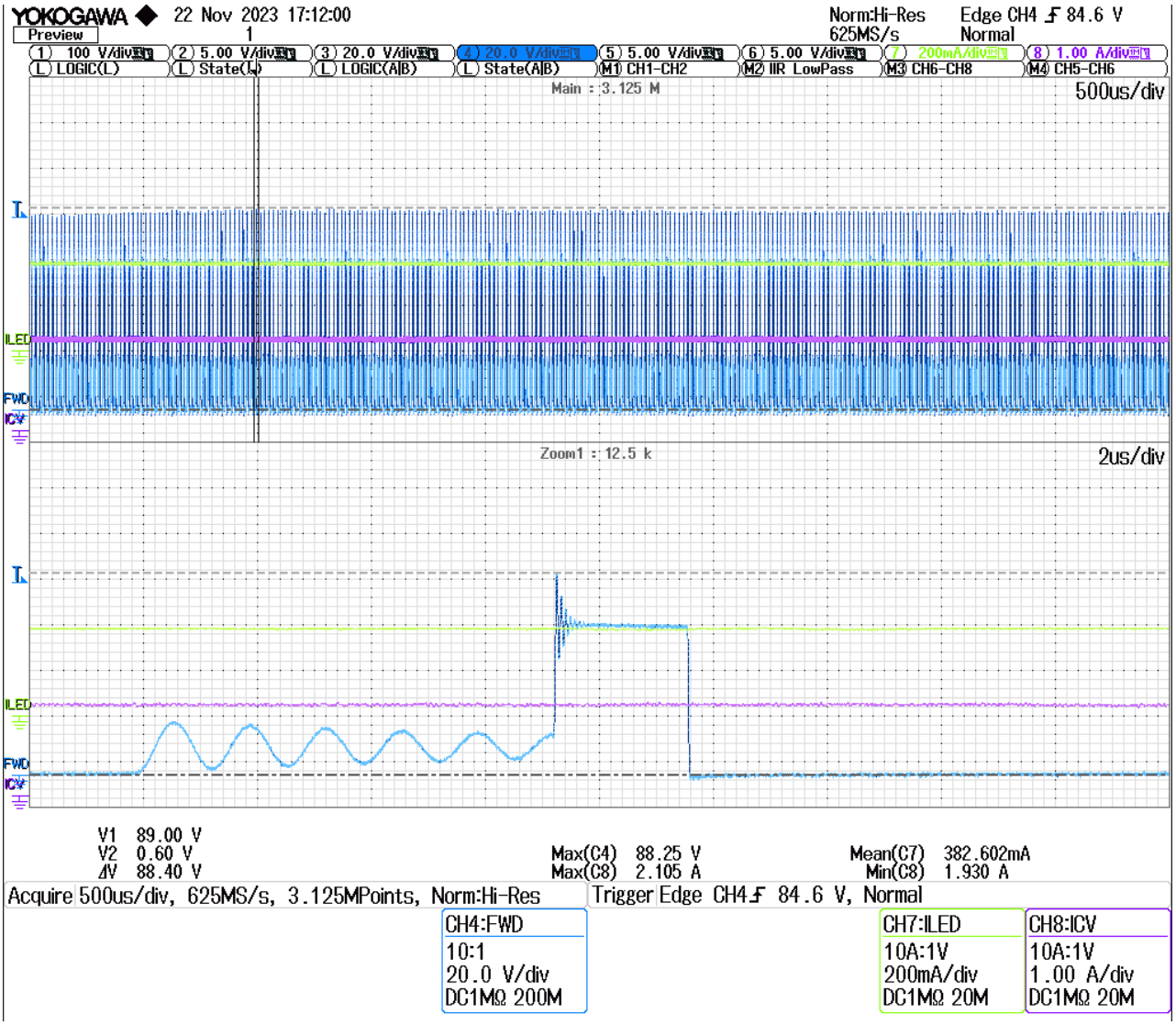


Figure 53 – SR (D8) Reverse Voltage Under Nominal Load at 265VAC.

Ch4: V_{SR} , Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the SR Diode is 89V.

Figure 54 – SR (D8) Reverse Voltage at Start-up at 265VAC.

Ch4: V_{SR} , Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the SR Diode is 125V.

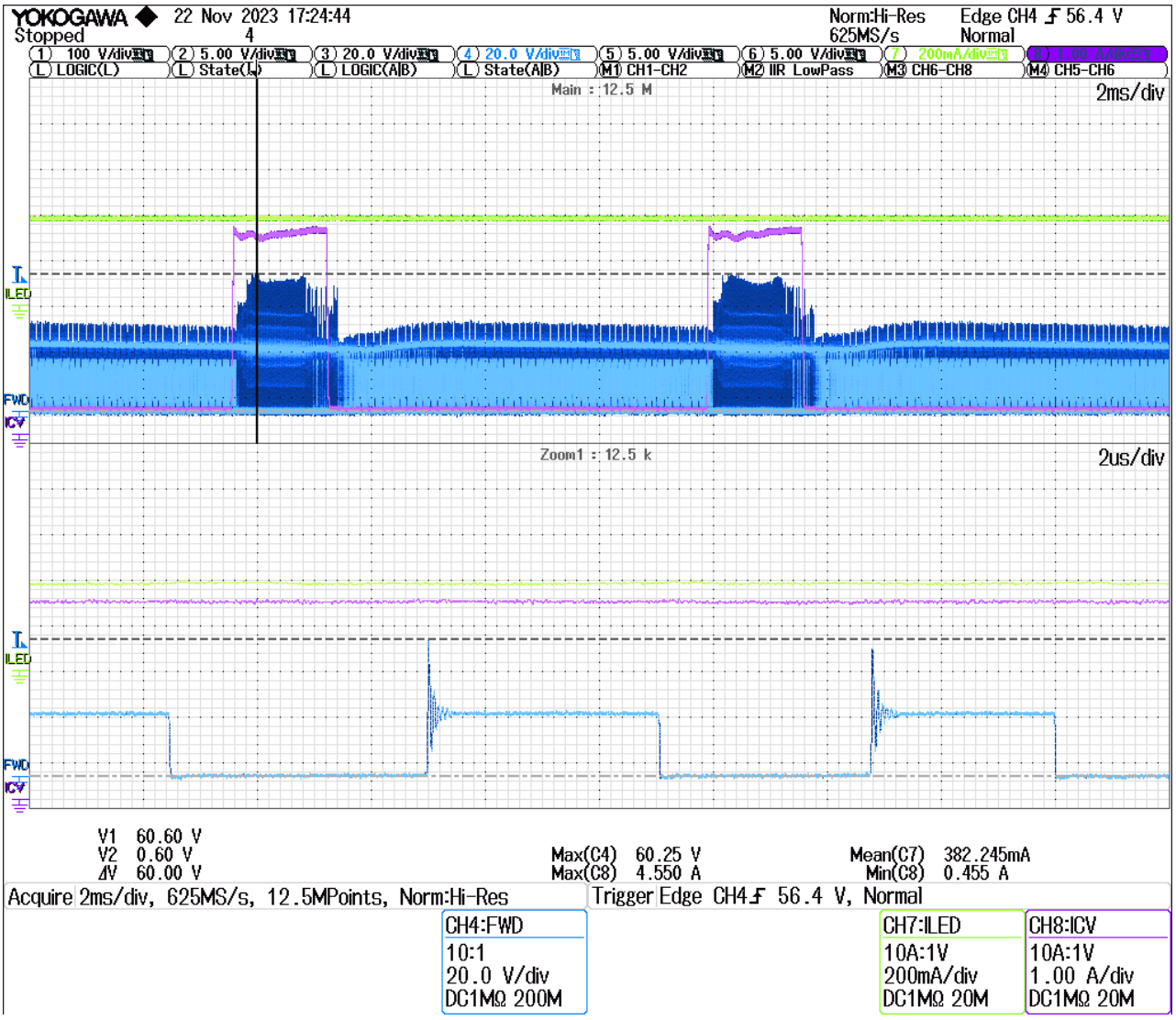


Figure 55 – SR (D8) Reverse Voltage under Peak Load at 90VAC.

Ch4: V_{SR} , Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the SR Diode is 60V.

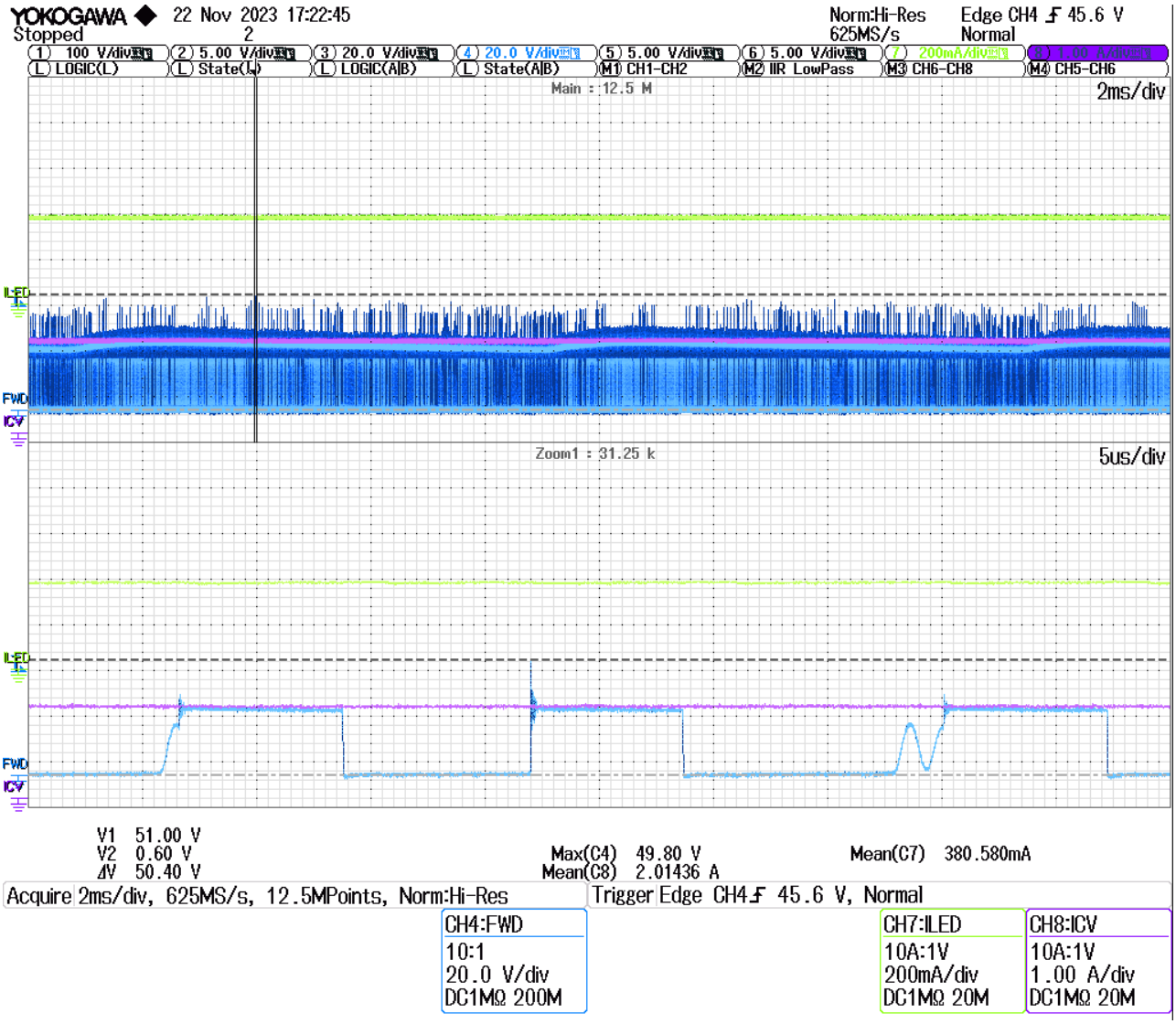


Figure 56 – SR (D8) Reverse Voltage under Nominal Load at 90VAC.

Ch4: V_{SR} , Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the SR Diode is 50V.

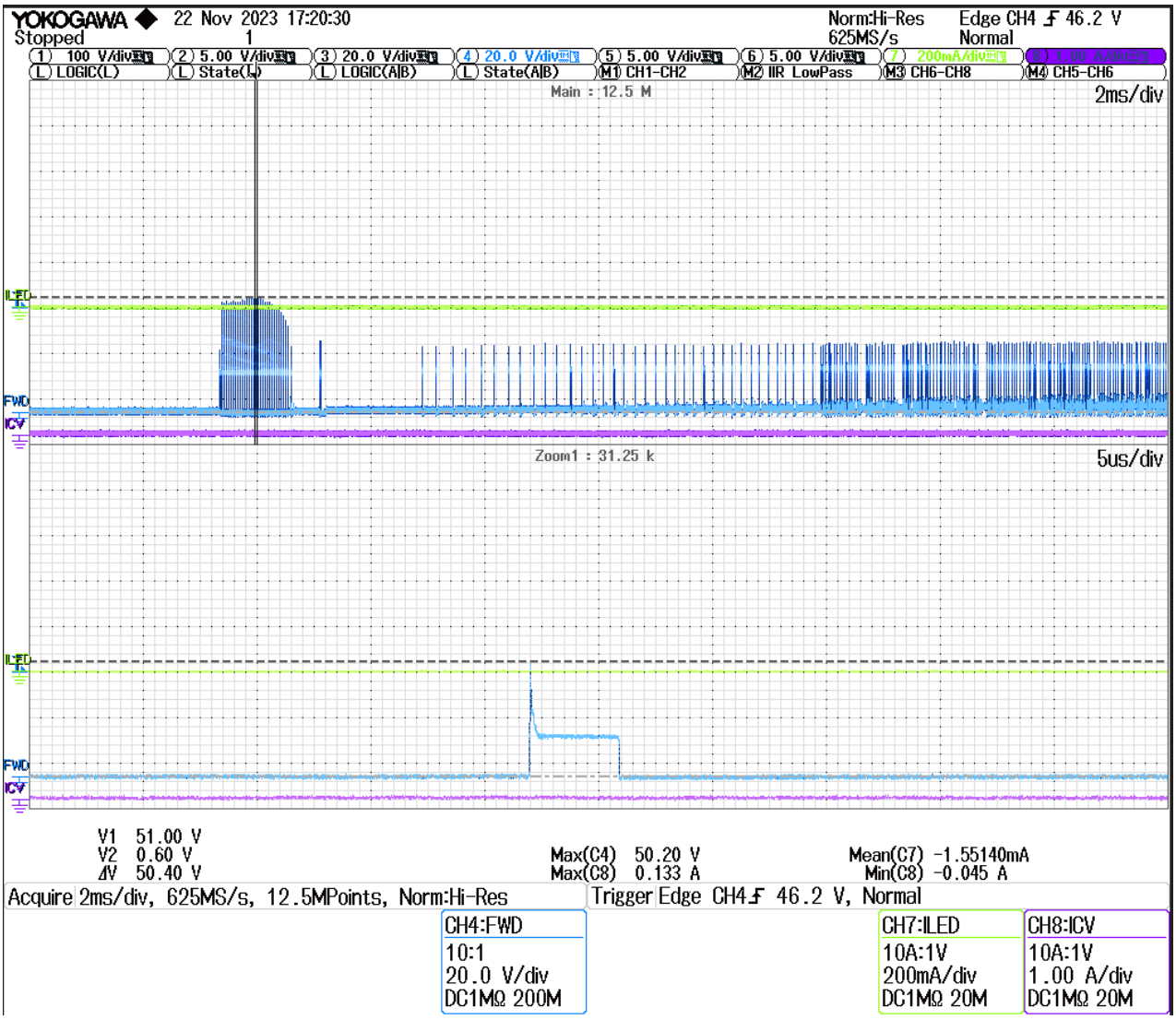


Figure 57 – SR (D8) Reverse Voltage at Start-up at 90VAC.

Ch4: V_{SR} , Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the SR Diode is 51V.

9.20.2 CV1 Selection FET Maximum Voltage

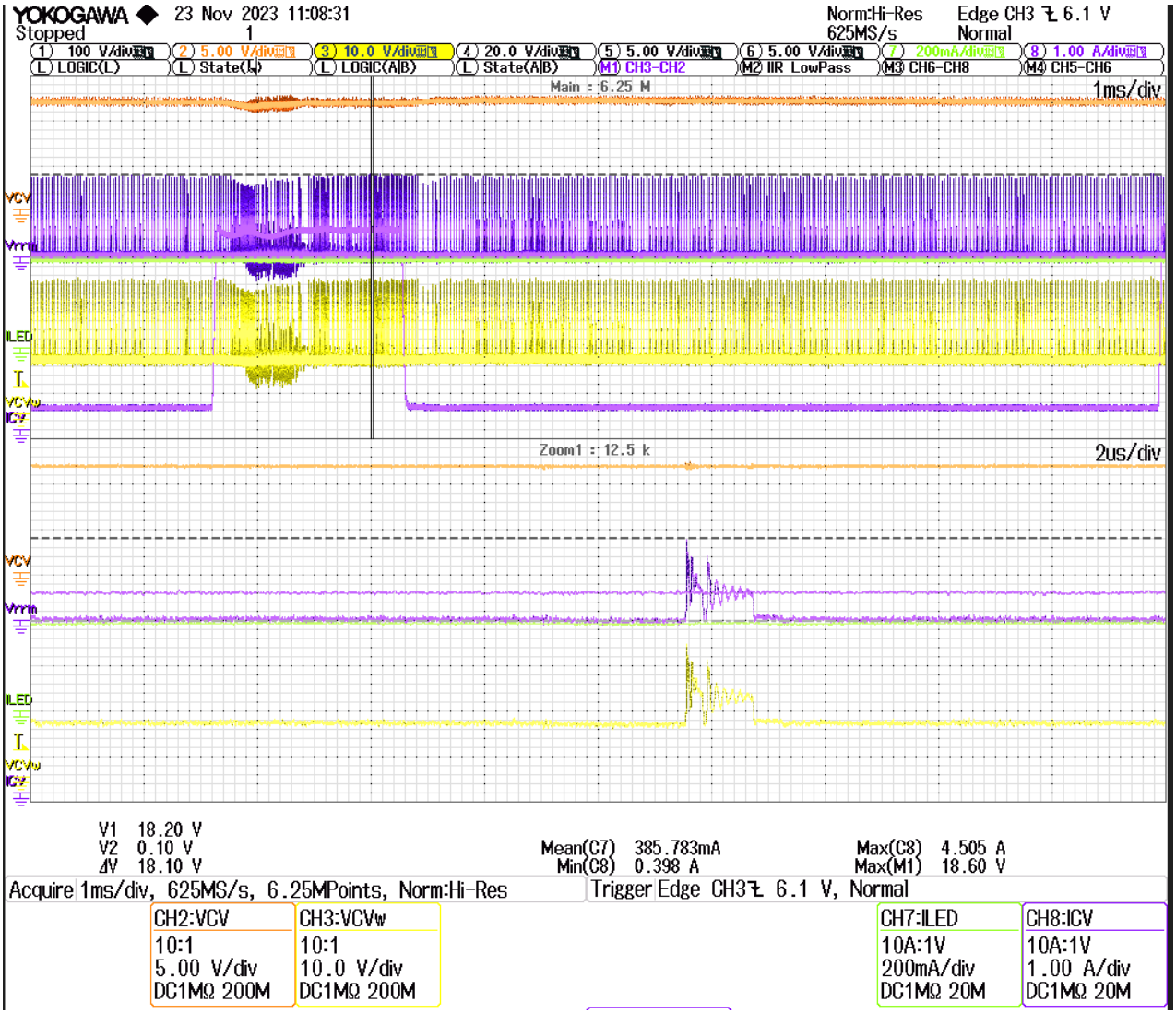


Figure 58 – CV1 Selection FET (Q1) D-S Voltage Under Peak Load at 265VAC.

Ch2: V_{CV} , Ch3: $V_{CVWinding}$, Ch7: I_{LED} , Ch8: I_{CV}

The maximum D-S voltage across the selection FET of CV1 is 18.6V .

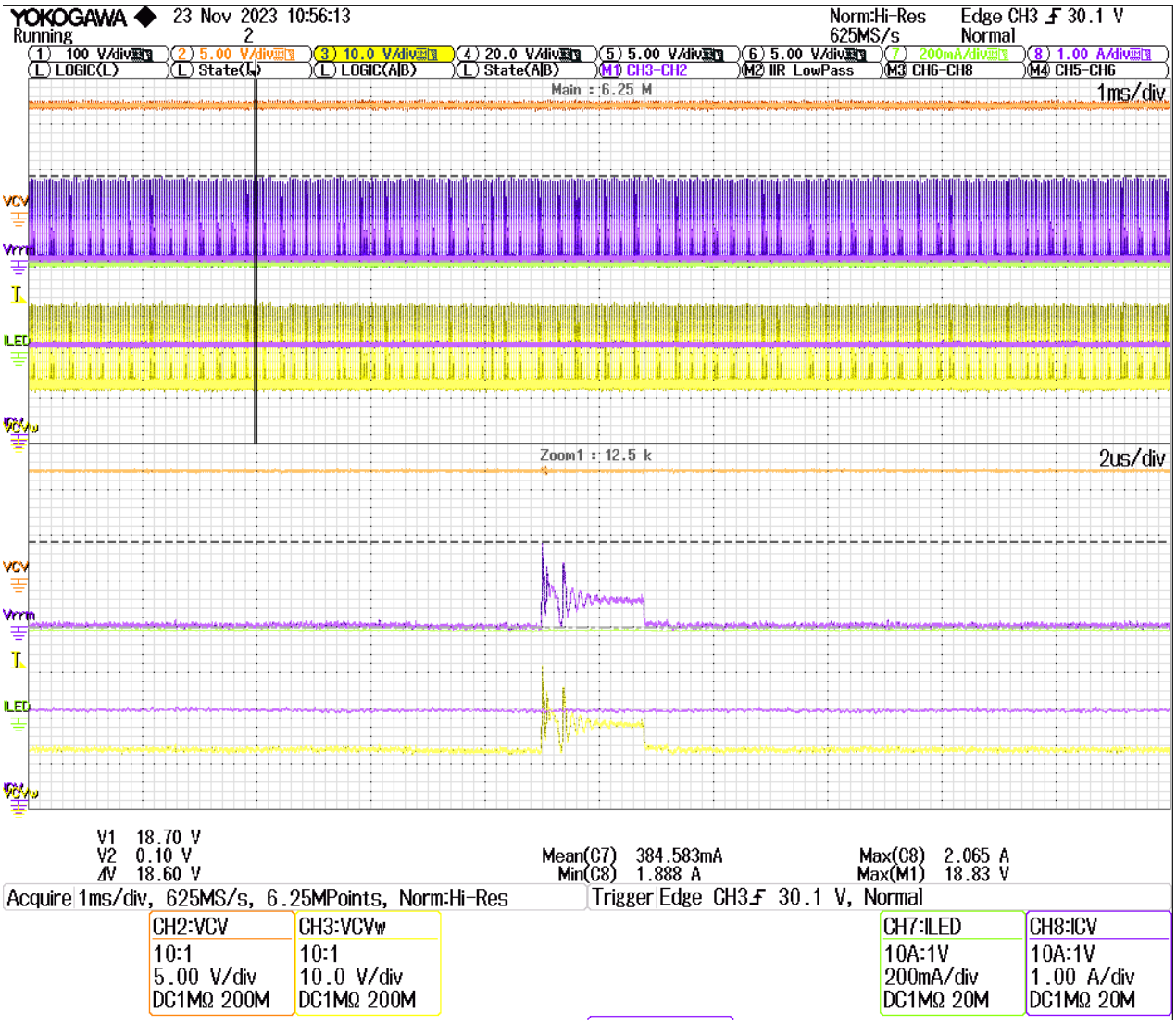


Figure 59 – CV1 Selection FET (Q1) D-S Voltage Under Nominal Load at 265VAC.

Ch2: V_{CV} , Ch3: $V_{CVWinding}$, Ch7: I_{LED} , Ch8: I_{CV}

The maximum D-S voltage across the selection FET of CV1 is 18.9V .

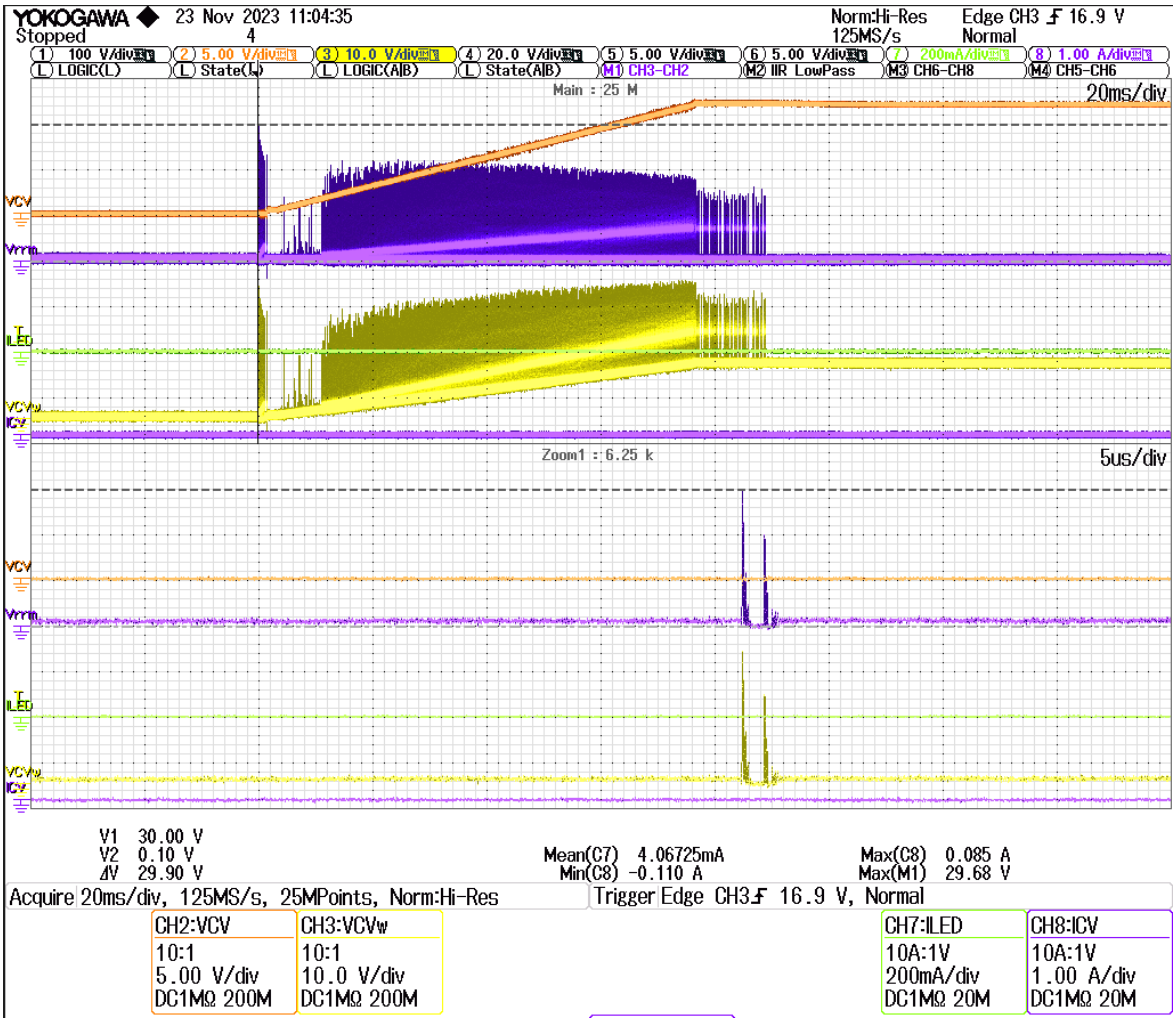


Figure 60 – CV1 Selection FET (Q1) D-S Voltage at Start-up at 265VAC.

Ch2: V_{CV} , Ch3: $V_{CVWinding}$, Ch7: I_{LED} , Ch8: I_{CV}

The maximum D-S voltage across the selection FET of CV1 is 30V .

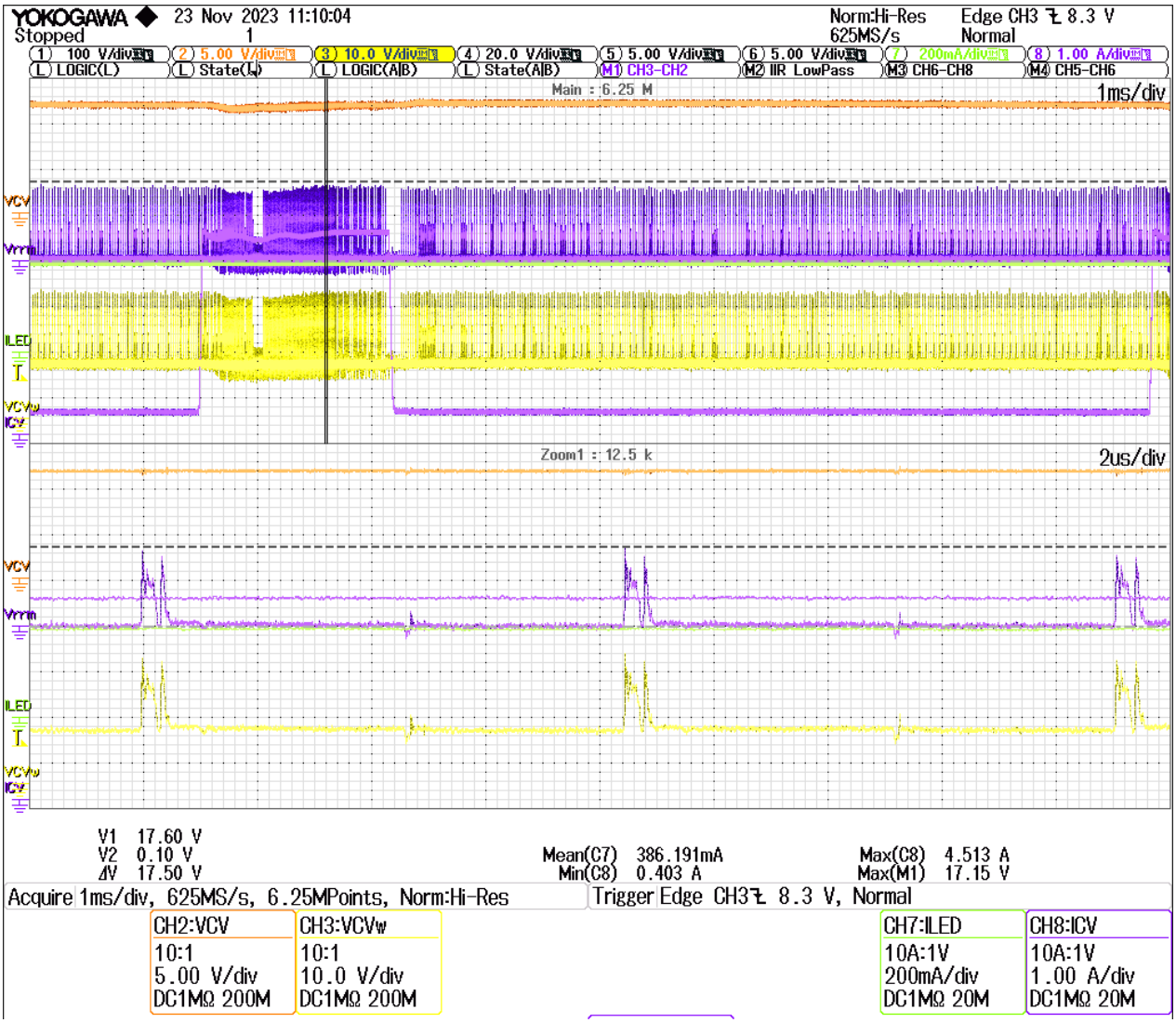


Figure 61 – CV1 Selection FET (Q1) D-S Voltage Under Peak Load at 90VAC.

Ch2: V_{CV} , Ch3: $V_{CVWinding}$, Ch7: I_{LED} , Ch8: I_{CV}

The maximum D-S voltage across the selection FET of CV1 is 17.2V .

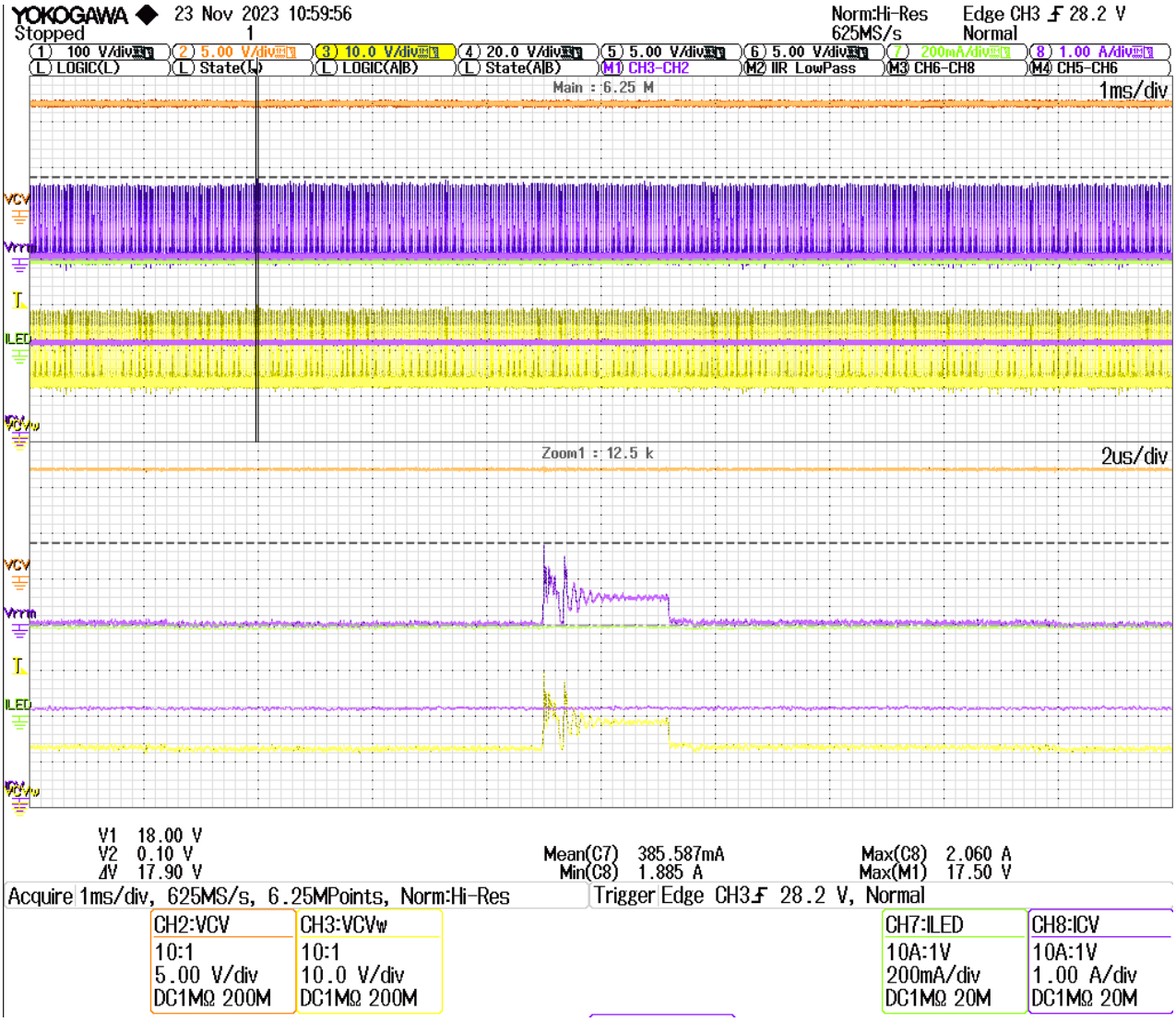


Figure 62 – CV1 Selection FET (Q1) D-S Voltage Under Nominal Load at 90VAC.

Ch2: V_{CV} , Ch3: $V_{CVWinding}$, Ch7: I_{LED} , Ch8: I_{CV}

The maximum D-S voltage across the selection FET of CV1 is 17.5V .

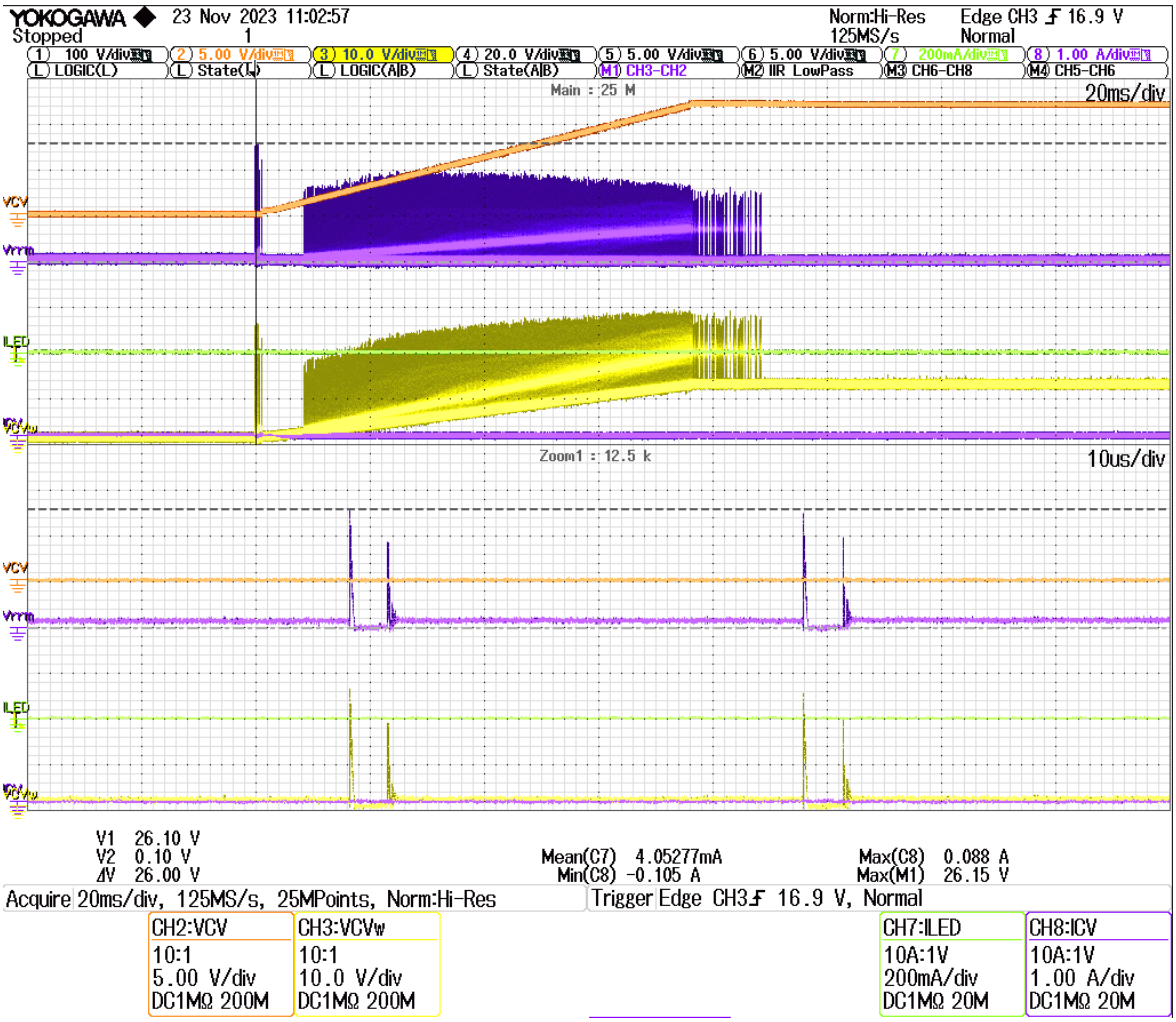


Figure 63 – CV1 Selection FET (Q1) D-S Voltage at Start-up at 90VAC.

Ch2: V_{CV} , Ch3: $V_{CVWinding}$, Ch7: I_{LED} , Ch8: I_{CV}

The maximum D-S voltage across the selection FET of CV1 is 26.2V .

9.20.3 LED Rectifier Diode Maximum Reverse Voltage

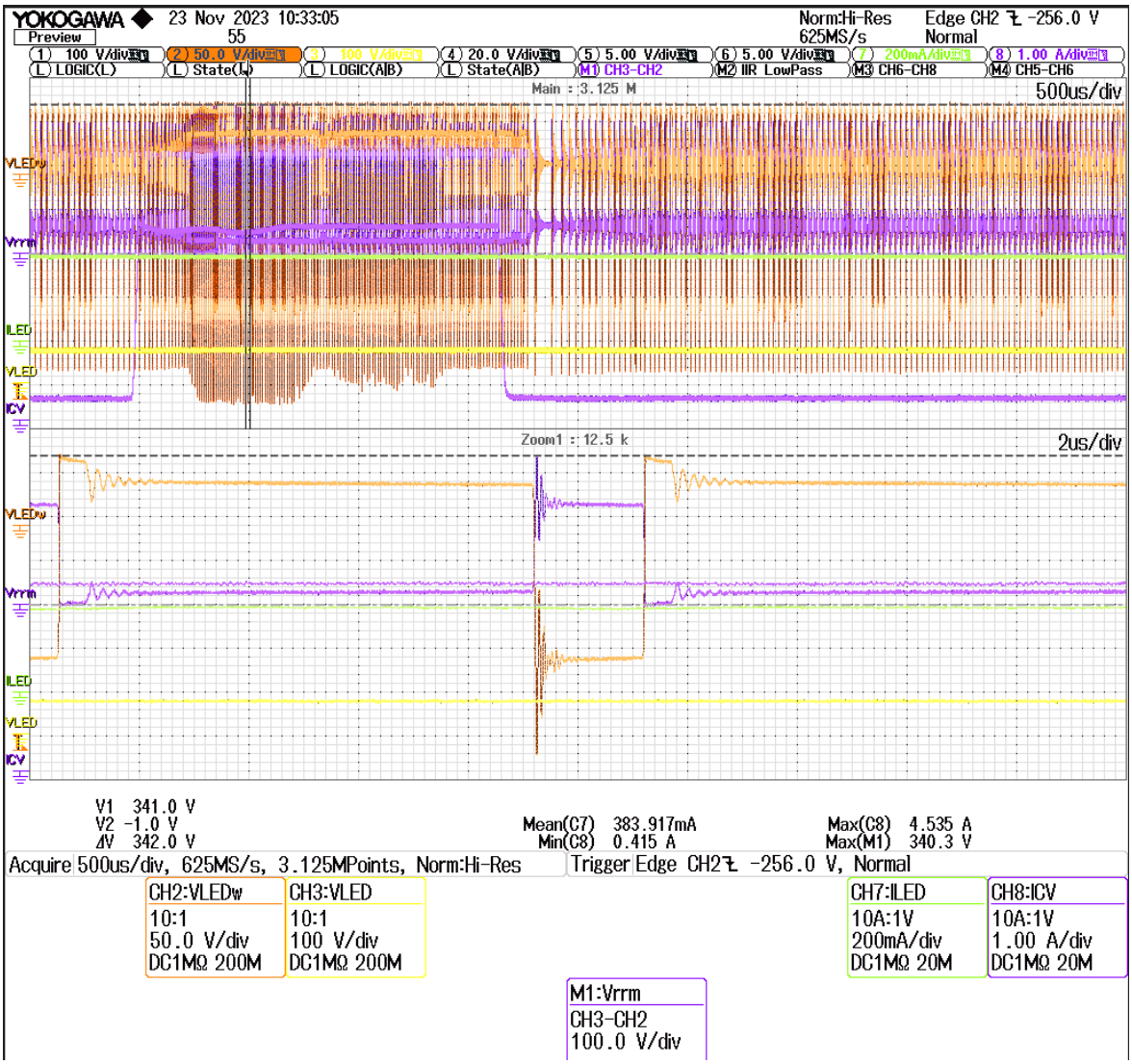


Figure 6422 – Reverse Voltage on LED Diode Under Peak Load at 265 VAC.

Ch2: $V_{LEDWINDING}$, Ch3: V_{LED} , Ch7: I_{LED} , Ch8: I_{CV} , ChM1: V_{RRM}

The worst-case peak reverse voltage across the LED rectifier diode (D3) is 340 V.

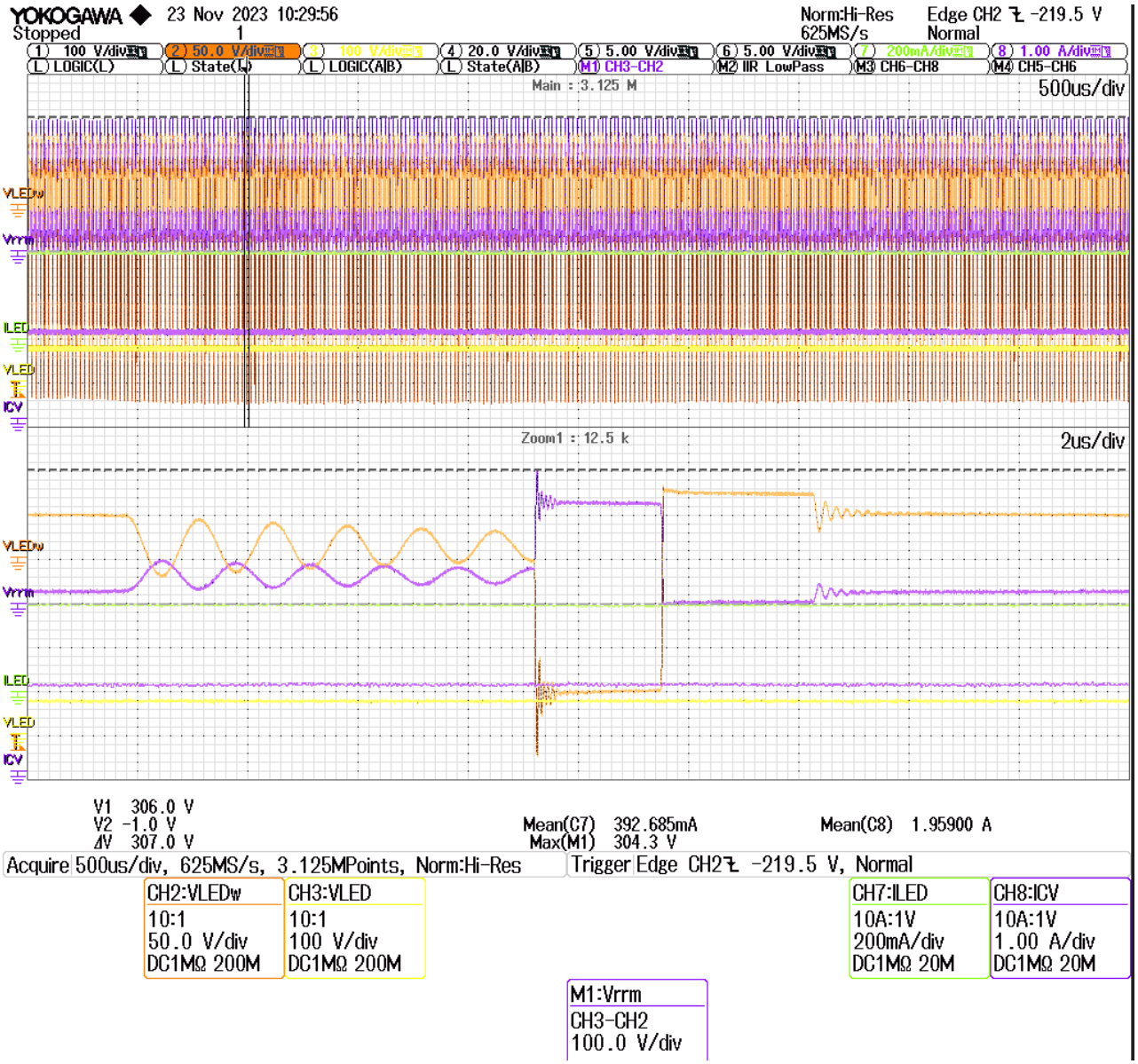


Figure 65 – Reverse Voltage on LED Diode Under Nominal Load at 265 VAC.

Ch2: $V_{LEDWINDING}$, Ch3: V_{LED} , Ch7: I_{LED} , Ch8: I_{CV} , ChM1: V_{RRM}

The worst-case peak reverse voltage across the LED rectifier diode (D3) is 304 V.

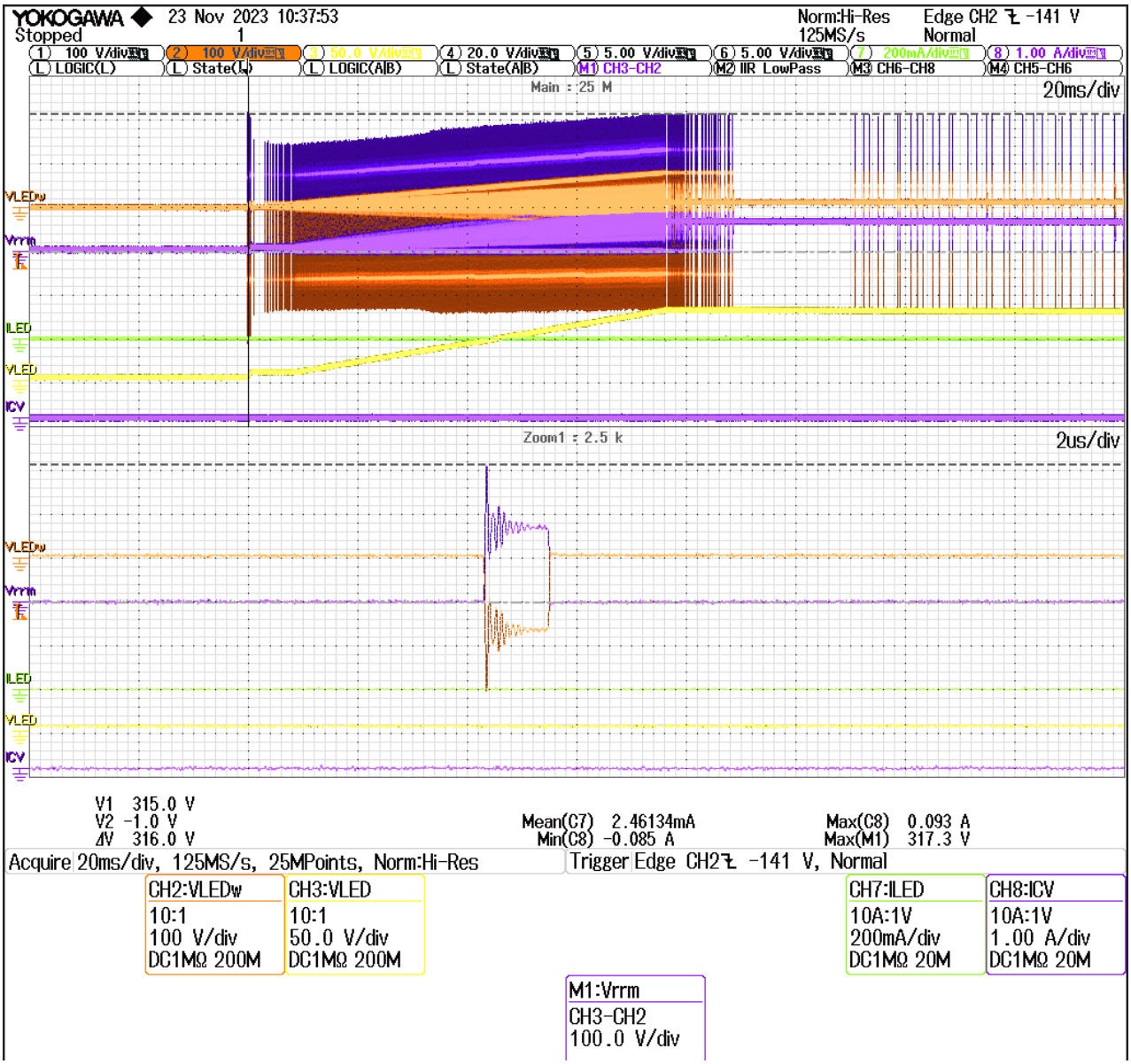


Figure 66 – Reverse Voltage on LED Diode at Start-up at 265 VAC.

Ch2: $V_{LEDWINDING}$, Ch3: V_{LED} , Ch7: I_{LED} , Ch8: I_{CV} , ChM1: V_{RRM}

The worst-case peak reverse voltage across the LED rectifier diode (D3) is 317 V.

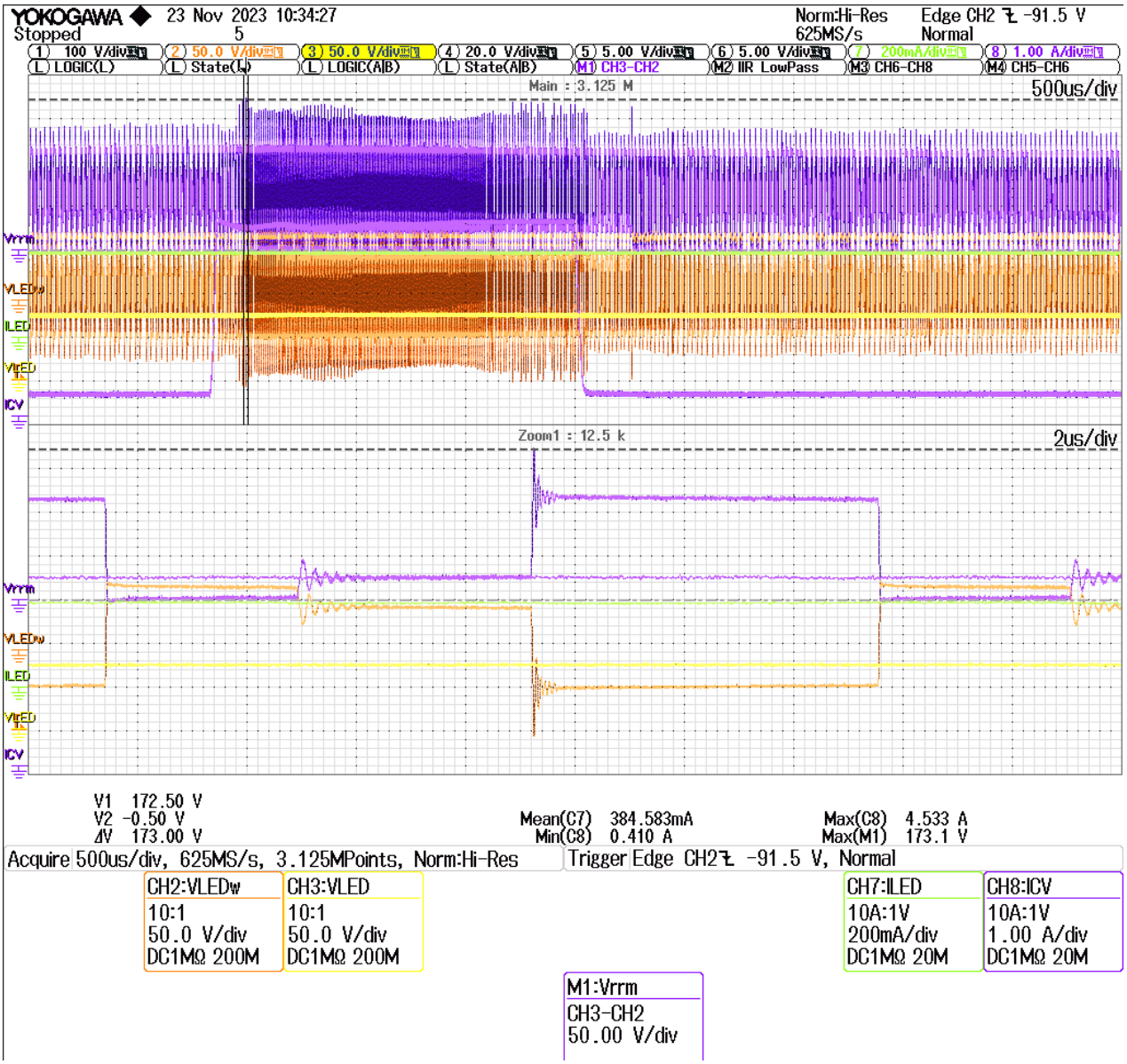


Figure 67 – Reverse Voltage on LED Diode Under Peak Load at 90 VAC.

Ch2: $V_{LEDWINDING}$, Ch3: V_{LED} , Ch7: I_{LED} , Ch8: I_{CV} , ChM1: V_{RRM}

The worst-case peak reverse voltage across the LED rectifier diode (D3) is 173 V.

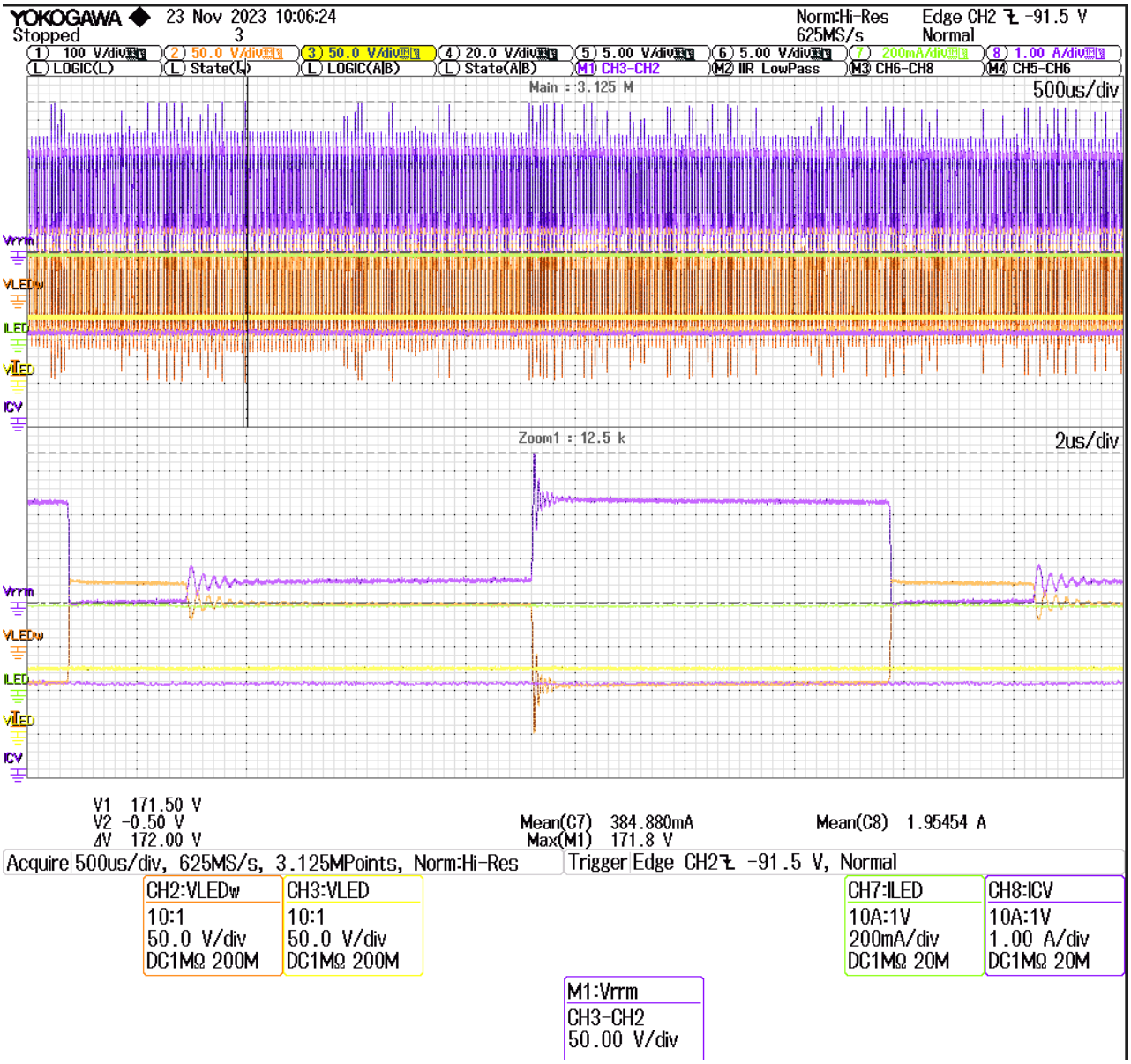


Figure 68 – Reverse Voltage on LED Diode Under Nominal Load at 90 VAC.

Ch2: $V_{LEDWINDING}$, Ch3: V_{LED} , Ch7: I_{LED} , Ch8: I_{CV} , ChM1: V_{RRM}

The worst-case peak reverse voltage across the LED rectifier diode (D3) is 171 V.

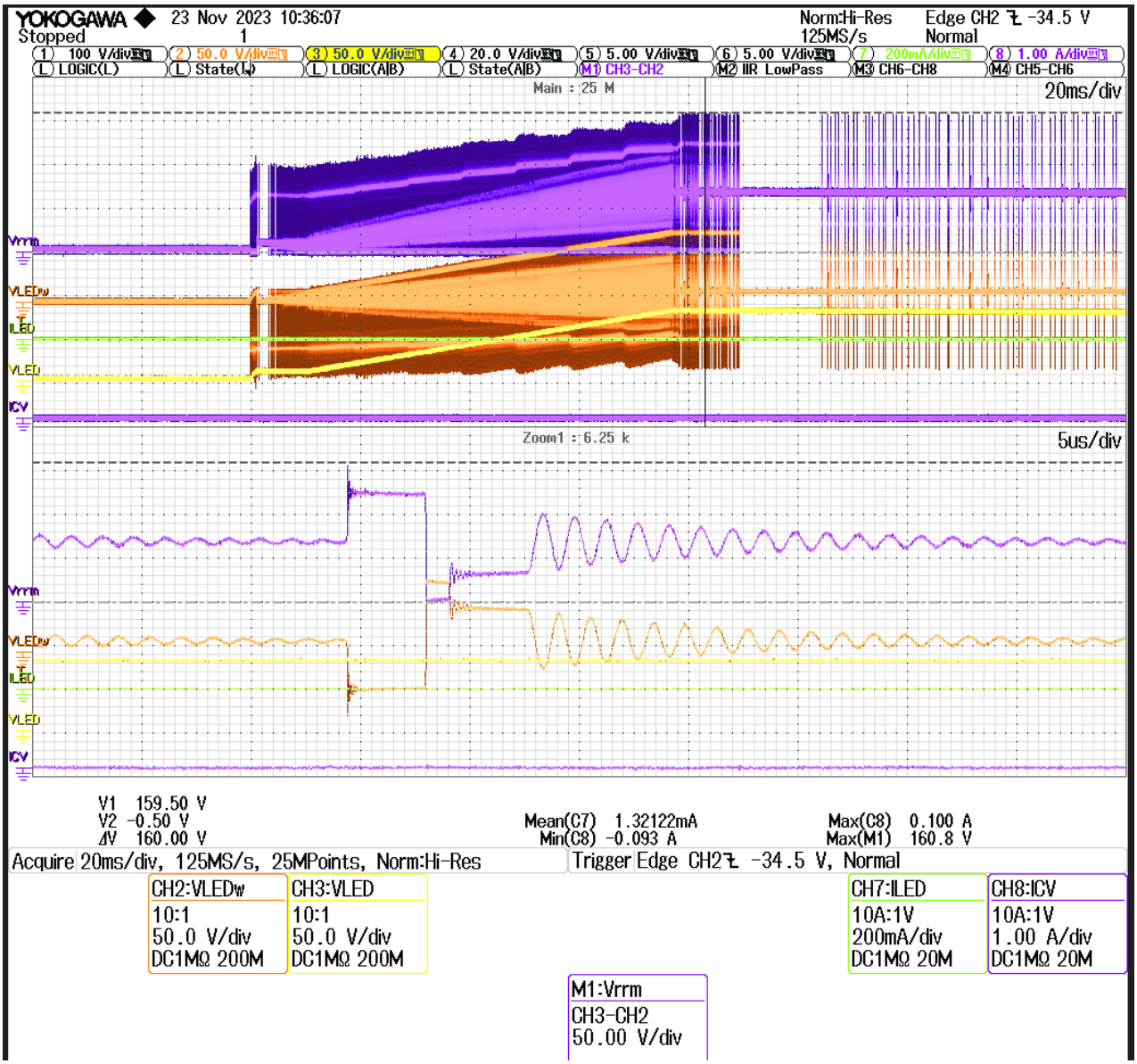


Figure 69 – Reverse Voltage on LED Diode at Start-up at 90 VAC.

Ch2: $V_{LEDWINDING}$, Ch3: V_{LED} , Ch7: I_{LED} , Ch8: I_{CV} , ChM1: V_{RRM}

The worst-case peak reverse voltage across the LED rectifier diode (D3) is 161 V.

9.20.4 BPP Rectifier Diode Reverse Voltage

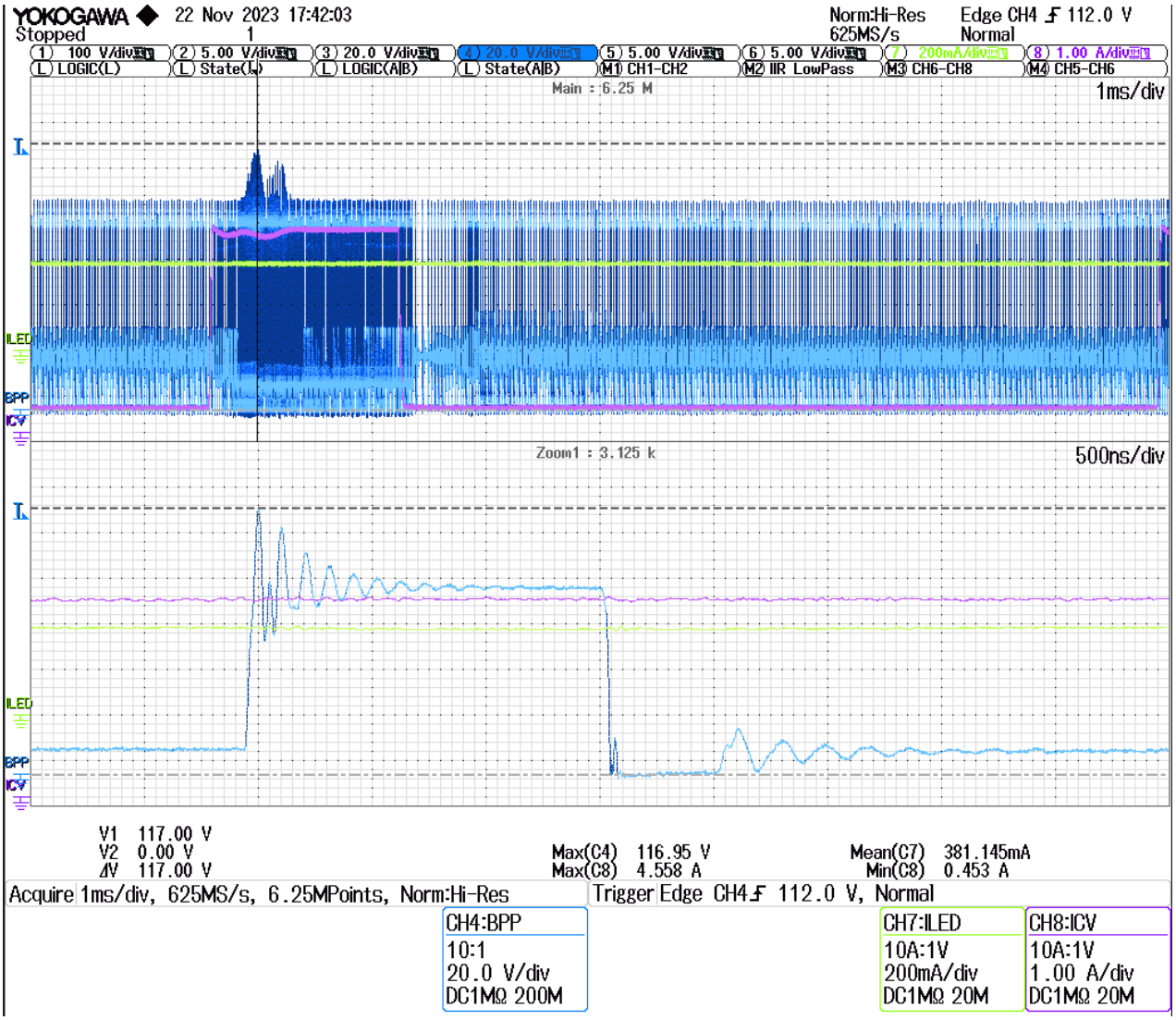


Figure 70 – Auxillary Diode Reverse Voltage Under Peak Load at 265VAC.

Ch4: $V_{BPPWNDNG}$, Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the Auxiliary winding diode is 117V.

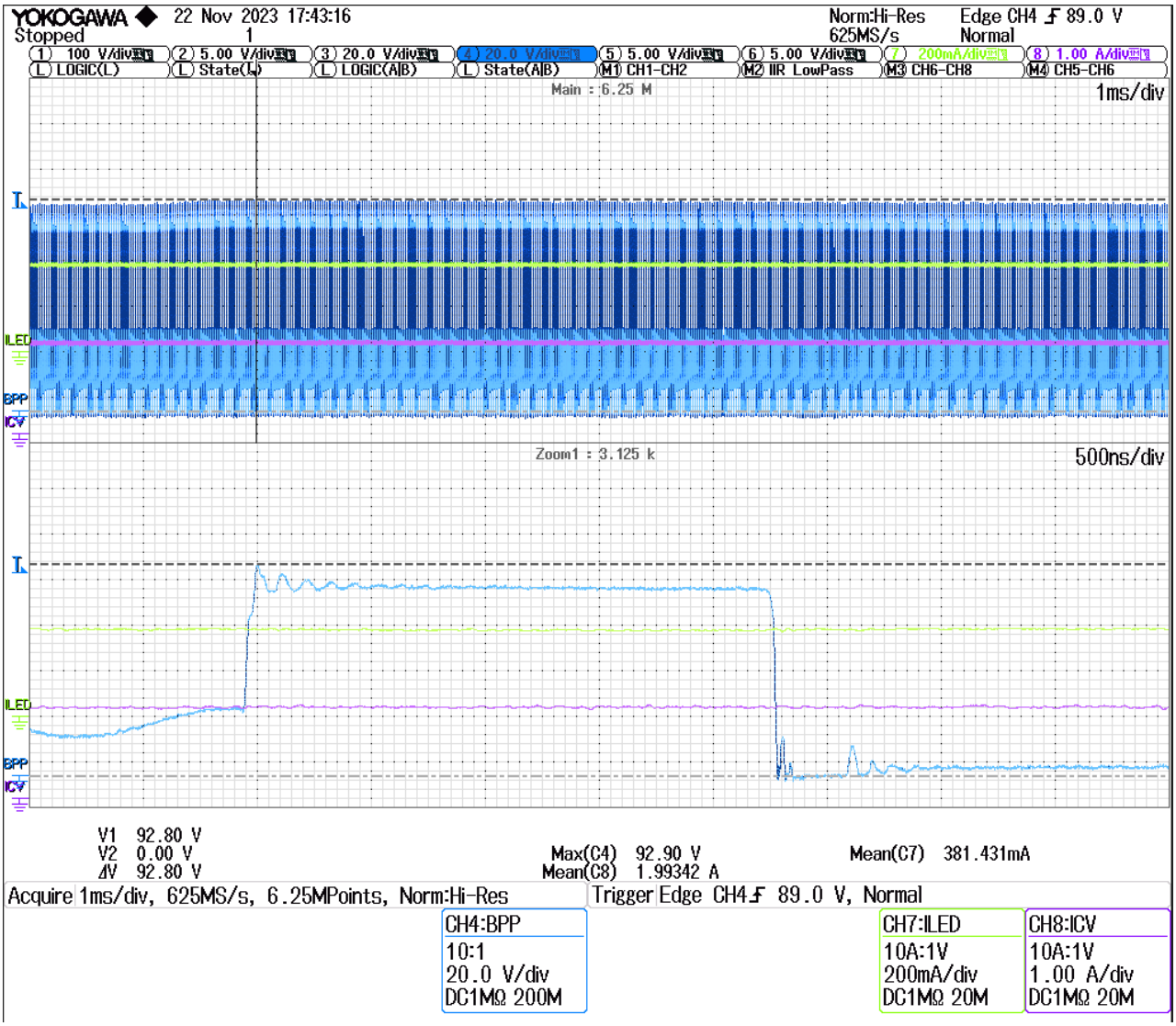


Figure 71 – Auxillary Diode Reverse Voltage Under Nominal Load at 265VAC.

Ch4: $V_{BPPWNDNG}$, Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the Auxiliary winding diode is 93V.

Figure 72 – Auxillary Diode Reverse Voltage at Start-up at 265VAC.

Ch4: $V_{BPPWNDNG}$, Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the Auxiliary winding diode is 123V.

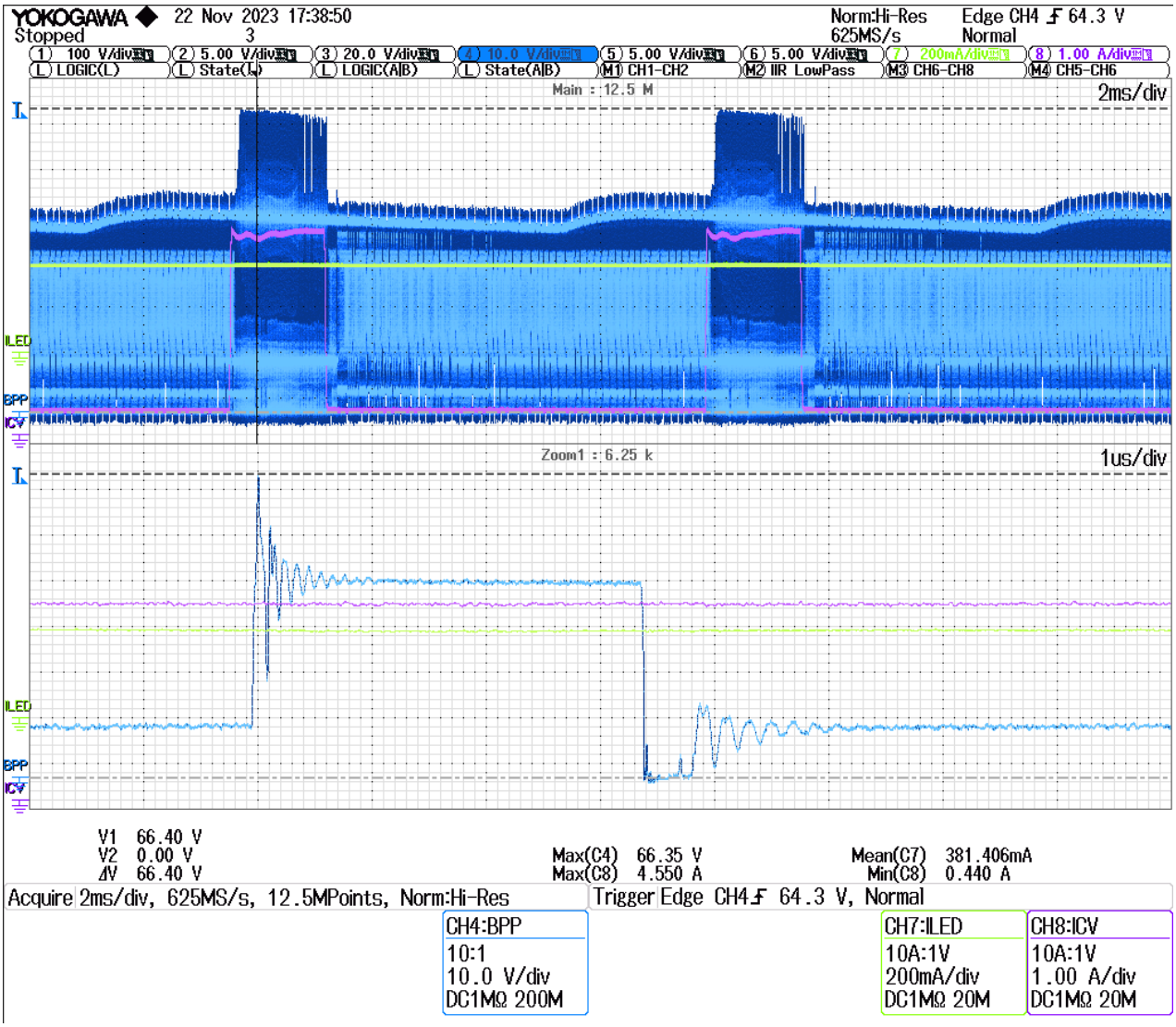


Figure 73 – Auxillary Diode Reverse Voltage under Peak Load at 90VAC.

Ch4: $V_{BPPWNDNG}$, Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the Auxiliary winding diode is 66V.

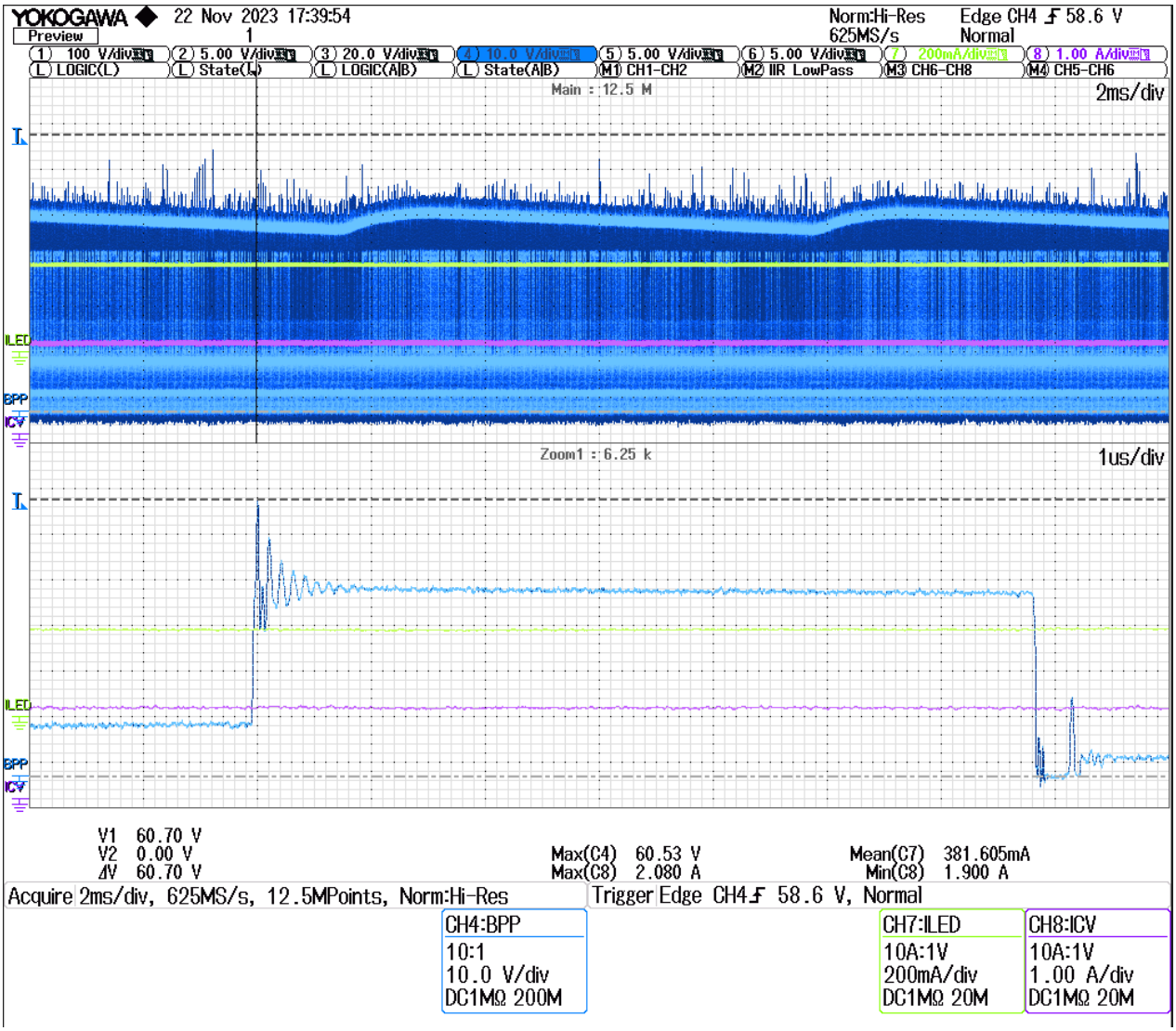


Figure 74 – Auxillary Diode Reverse Voltage under Nominal Load at 90VAC.

Ch4: $V_{BPPWNDNG}$, Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the Auxiliary winding diode is 61V.

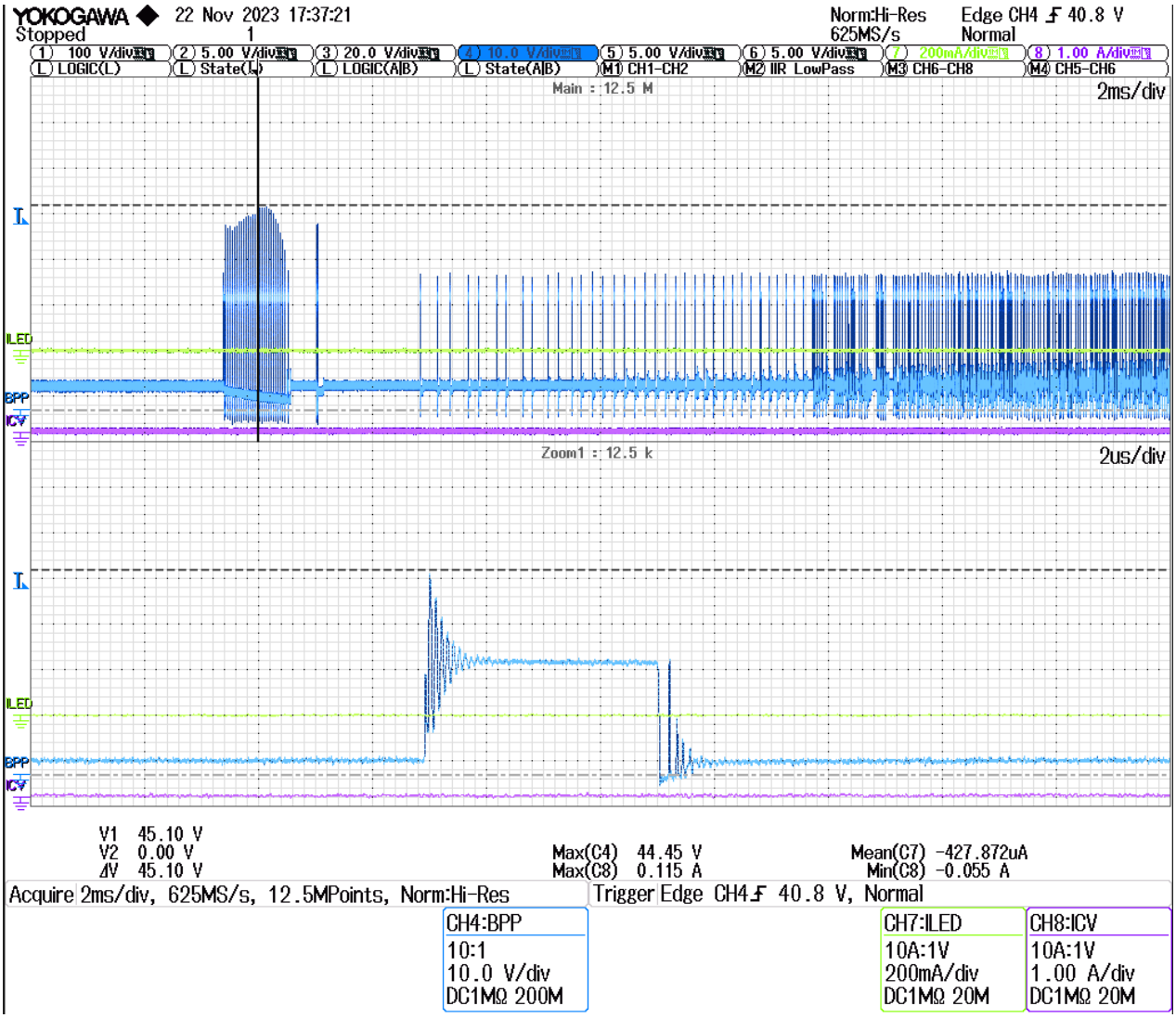


Figure 75 – Auxillary Diode Reverse Voltage at Start-up at 90VAC.

Ch4: $V_{BPPWNDNG}$, Ch7: I_{LED} , Ch8: I_{CV}

Maximum reverse voltage across the Auxiliary winding diode is 45V.

9.21 Brown – Out and Brown - In

The Brown In and Brown Out results were measured at full load on all outputs. The results are shown in the table below. Screenshots illustrating the tests are shown in Figure 49.

Brown-Out Threshold	Brown-In Threshold
[V_{RMS}]	[V_{RMS}]
63.5	73.3

Table 2 – Brown-In and Brown-Out Thresholds at Full power.

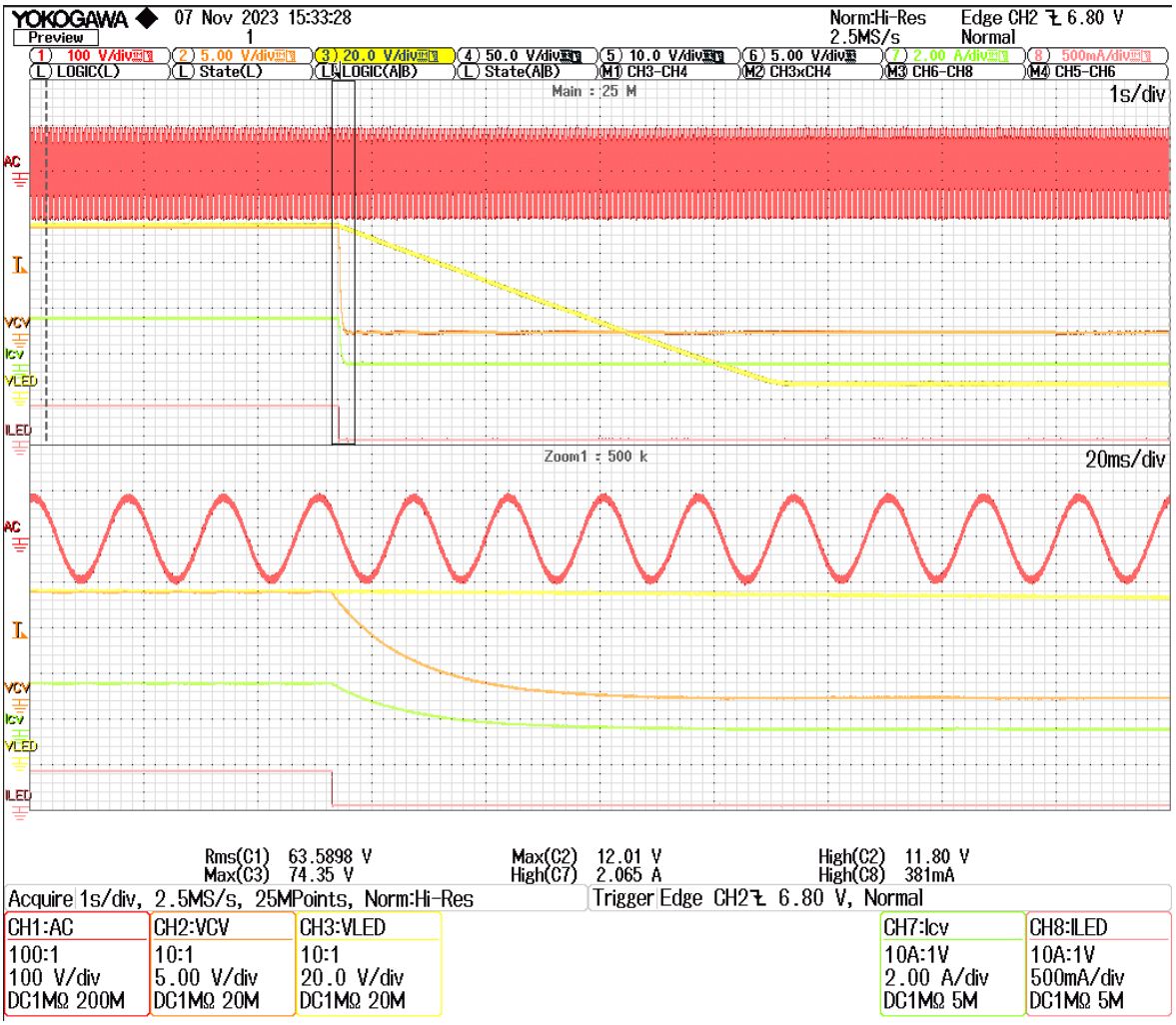


Figure 76 – Brown-Out Response at Full Power.

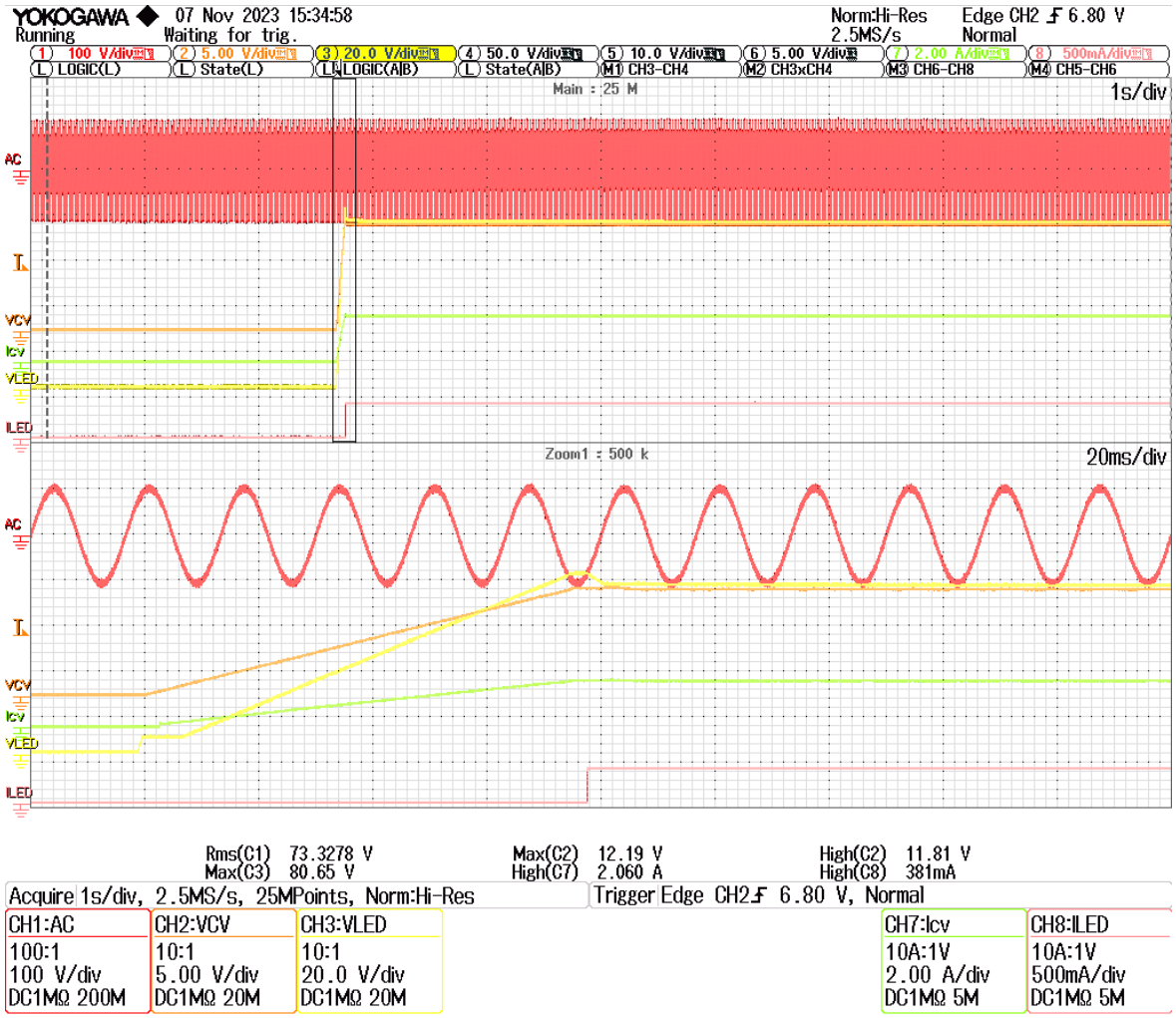


Figure 77 – Brown-In Response at Full Power.

9.22 Output Protections

9.22.1 CV Output Overvoltage Protection

The overvoltage protection threshold of the CV output was tested. Additional charge was injected into the output filter capacitor of the output under test until the converter went into a restart. The test was carried out at line voltages 115V with full LED current.

In all cases of LED no-load&full load and CV no-load&full-load , OV protection disables the system at 13.48V-13.52V which is around 112% of nominal CV voltage .

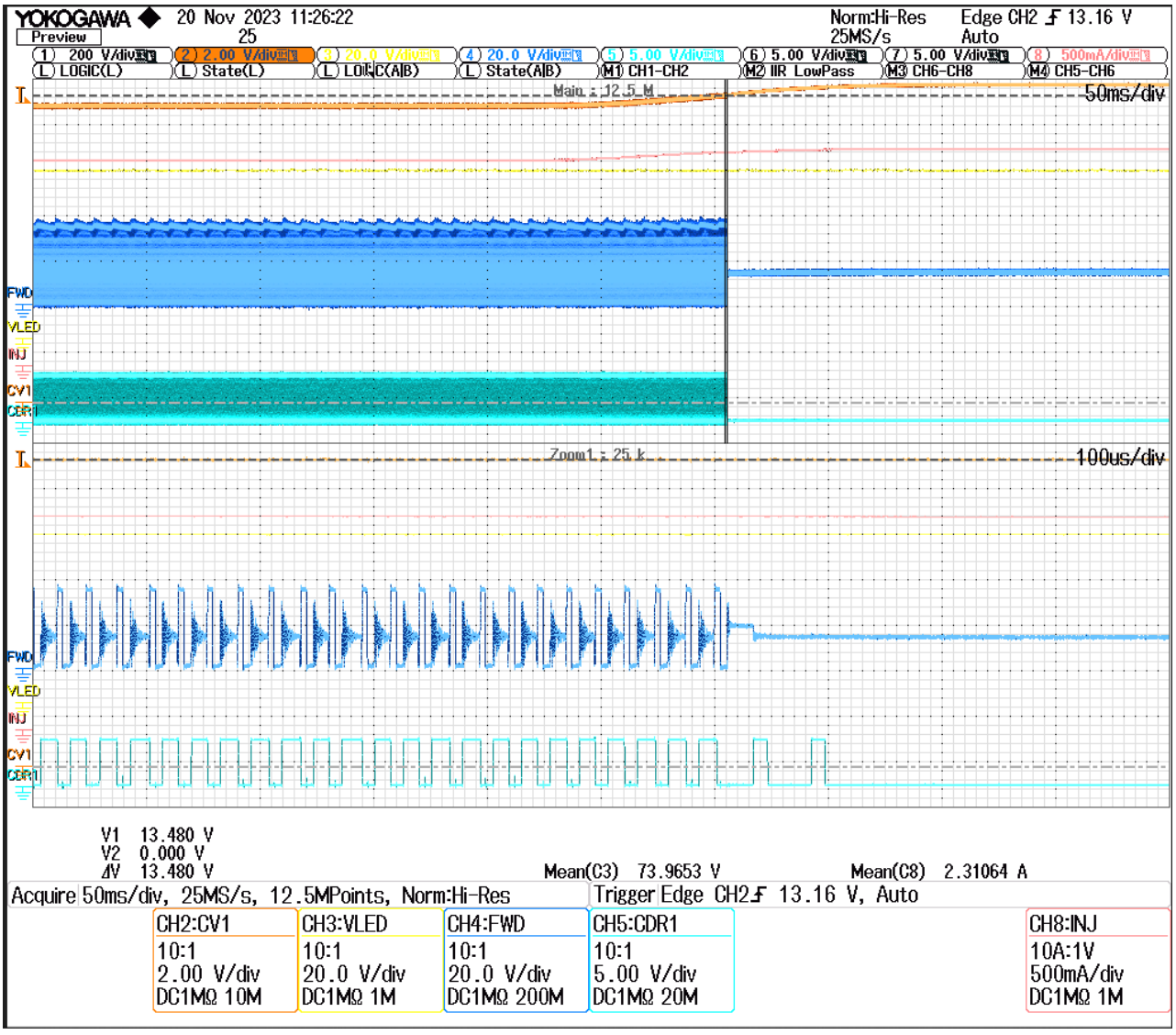


Figure 78 – CV OVP at full LED load

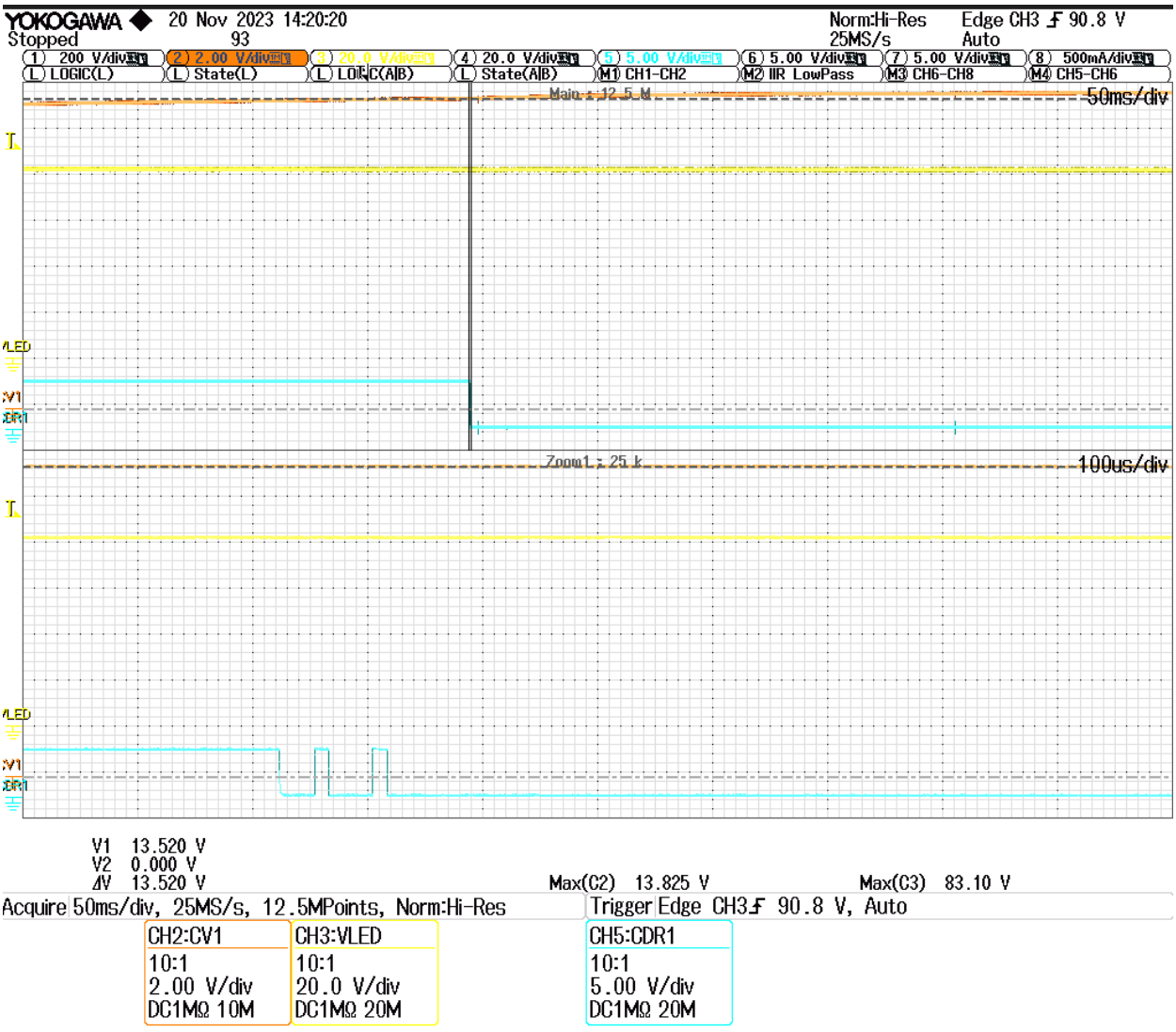


Figure 79 – CV OVP no LED load

9.22.2 LED Output Overvoltage Protection

The overvoltage protection thresholds of the LED output was tested at full power on CVoutput. CDR1 gate opens at steady-state to charge the LED capacitors for triggering LED over voltage protection.

LED OVP has been triggered at 93.4V which is 116% of LED voltage.

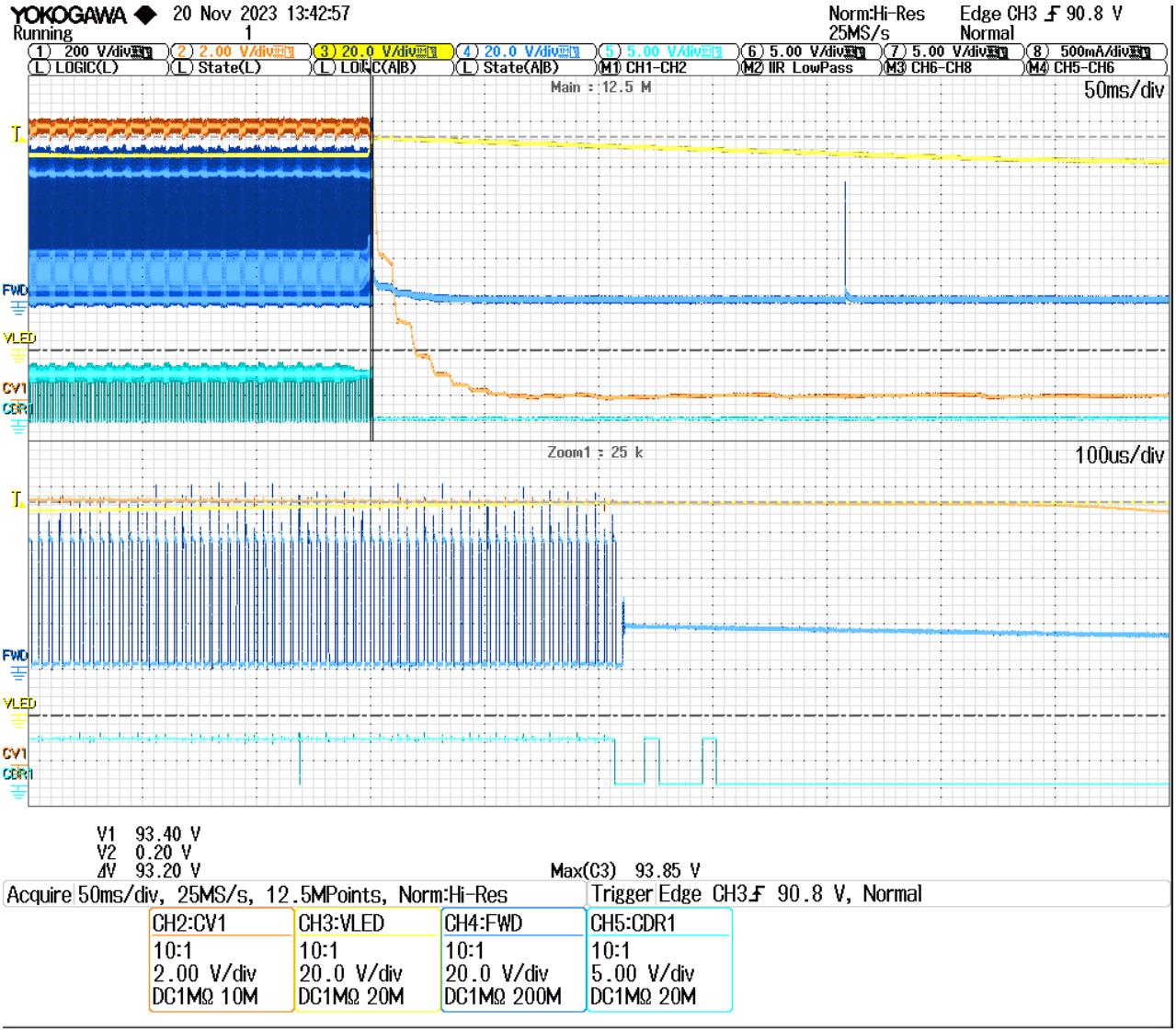


Figure 80 – LED OVP

9.23 Output Ripple Measurements

9.23.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe were utilized in order to reduce noise pick-up. Details of the probe modification are provided in Figure 59.

The probe adapter is shown in Figure 59. It includes a coaxial cable with two parallel capacitors connected to the points of measurement. The capacitors include a 0.1 μF / 100 V ceramic type and a 10 μF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.

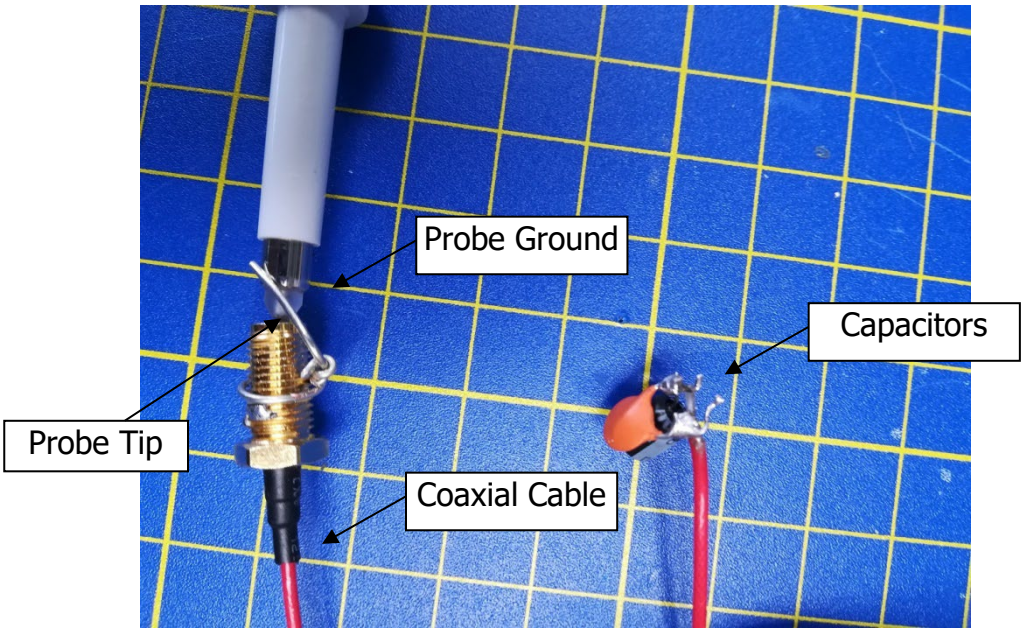


Figure 81 – Oscilloscope Probe Used in Ripple Measurement.

9.23.2 CV Output Ripple

9.23.2.1 Test Set-up

- 90 VAC – 265 VAC
- Output 12 V @ 24 W and LED_72 V @ 27, 36 W
- 200 MHz bandwidth in the scope, 100 nF ceramic capacitor and 10 μF @ 50 V electrolytic capacitor with sniffing connected to output pin

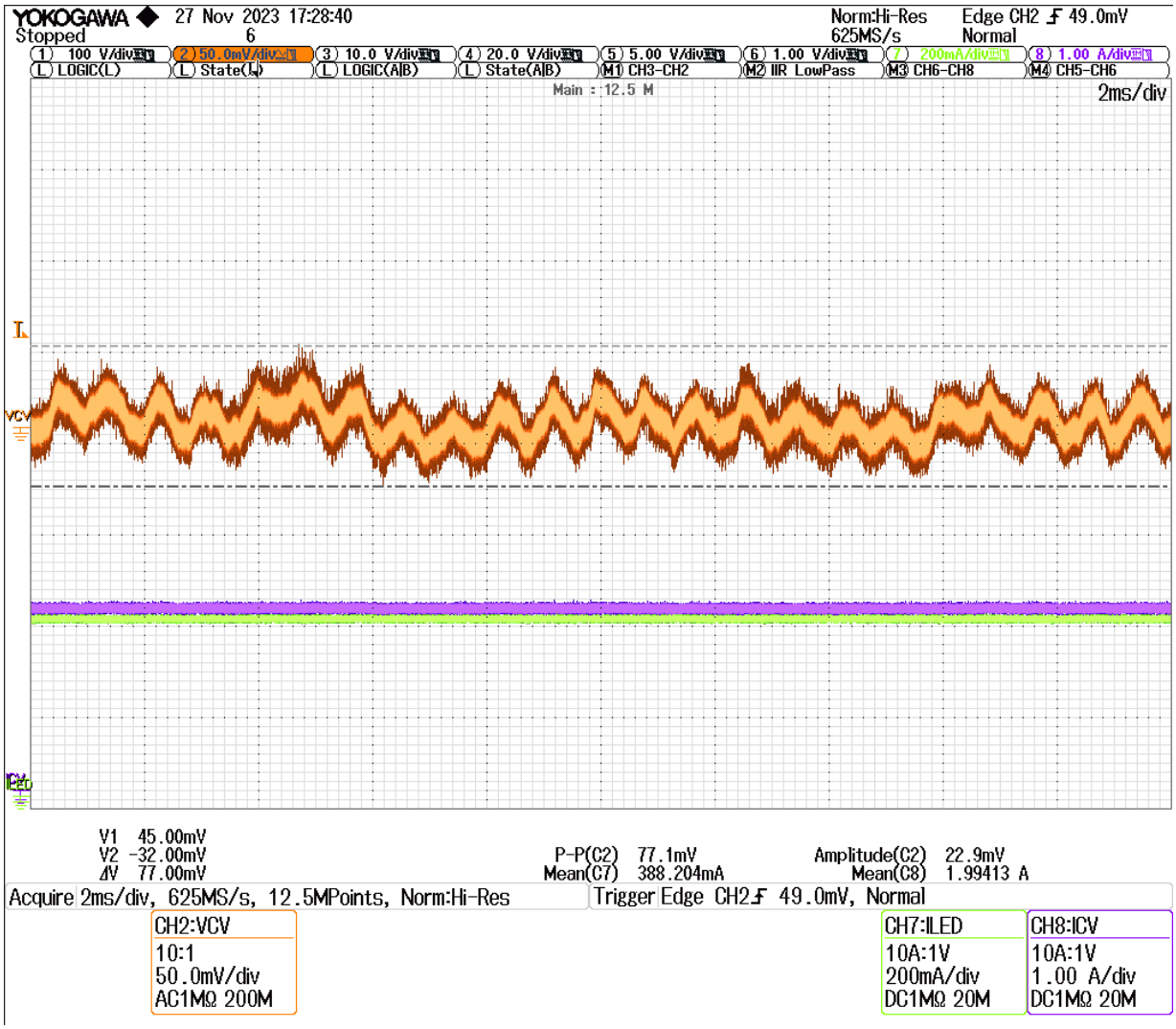


Figure 82 – VCV Ripple and Noise under nominal load at 90VAC.

CH2: V_{CV} , CH7: I_{LED} , CH8: I_{CV}

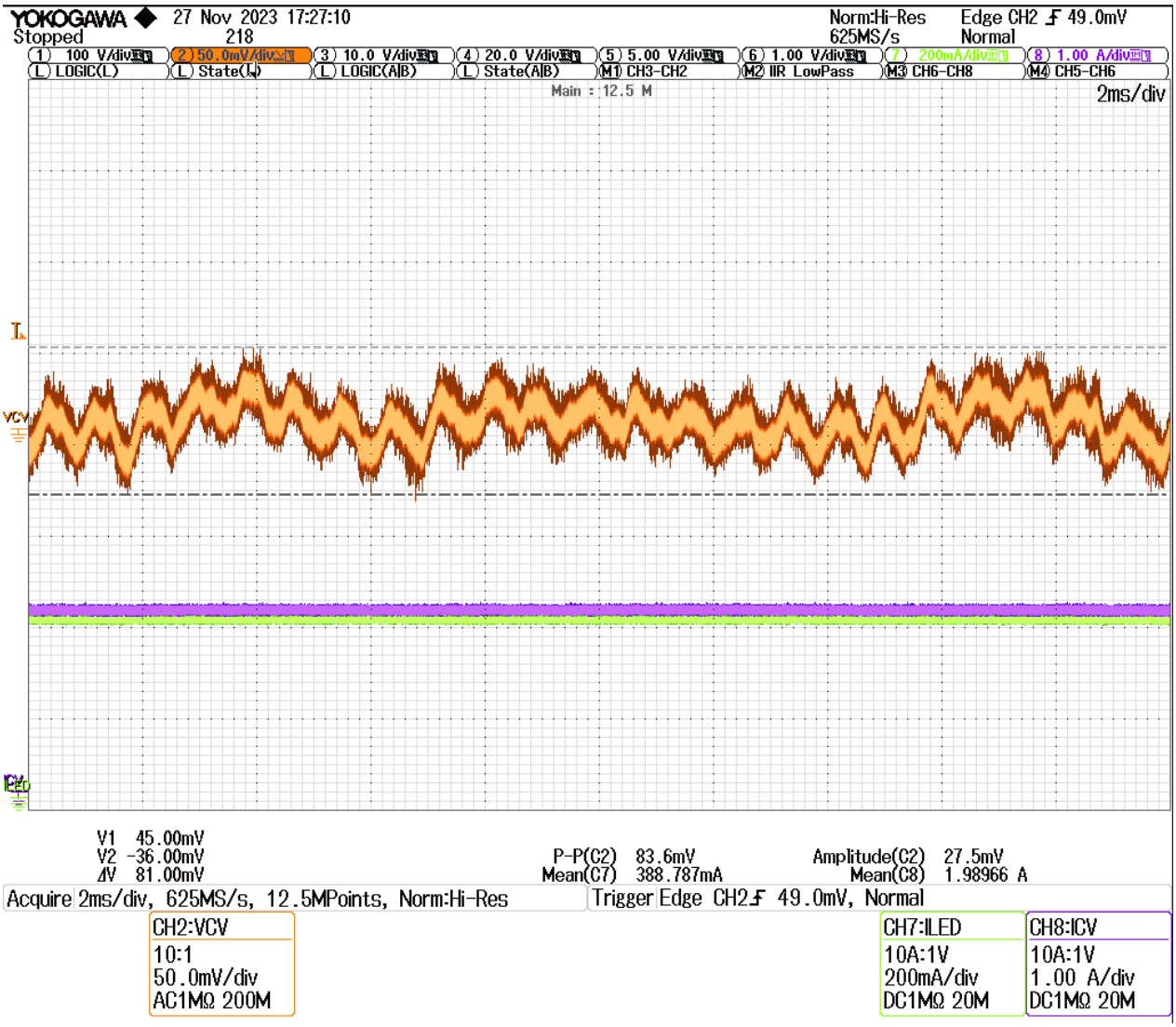


Figure 83 – VCV Ripple and Noise under nominal load at 265VAC.

CH2: V_{CV} , CH7: I_{LED} , CH8: I_{CV}

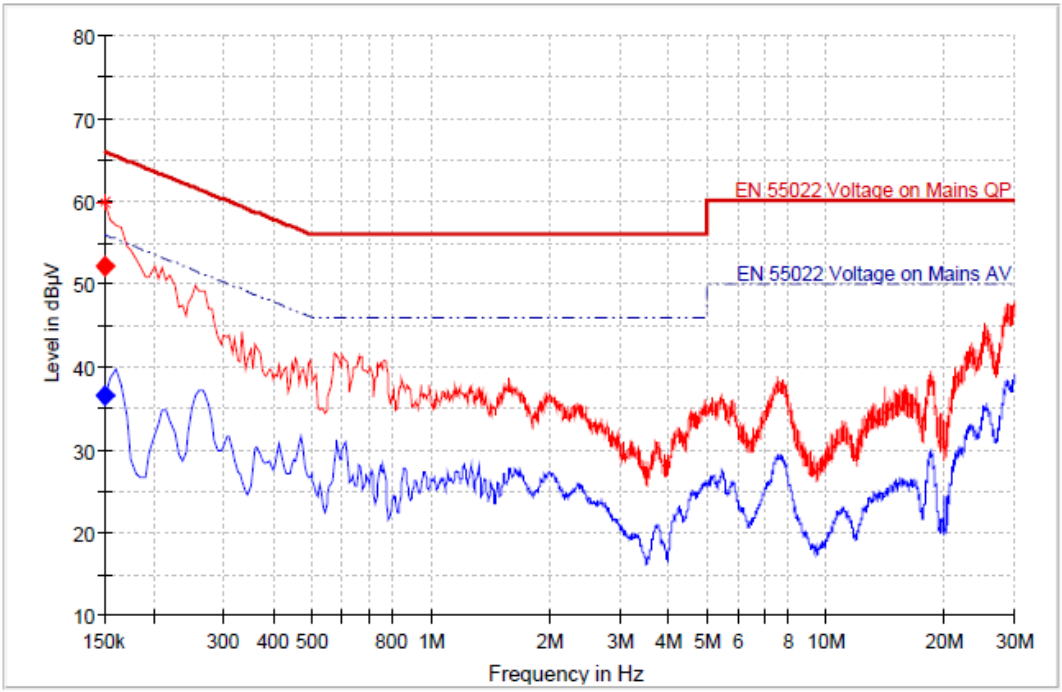
The worst case ripple and noise at the CV output of the converter was measured as 84mV_{P-P} at 200MHz bandwidth at the connector output.

10 Conducted EMI

The EMI scans were carried out at full power.PE connection was not considered in the test to simulate a TV system.

The conducted emissions were more than 8 dB below the limits set by CISPR22B / EN55022B.

10.1 Line Input 115 VAC

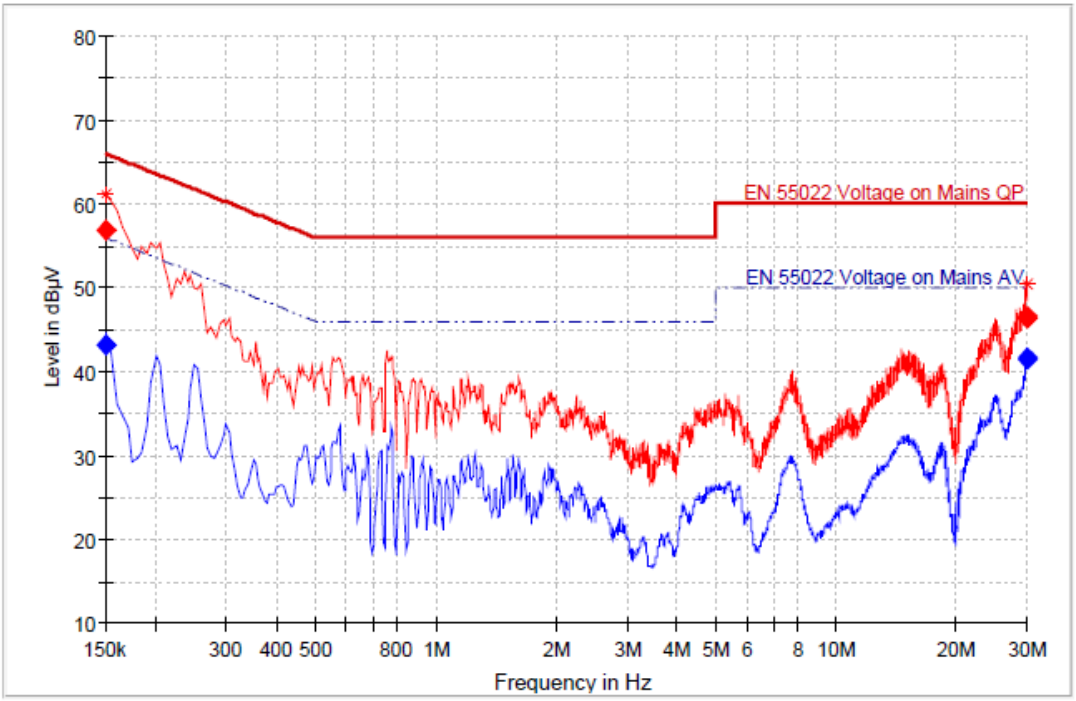


Final Result

Frequency (MHz)	QuasiPeak (dBµV)	Average (dBµV)	Limit (dBµV)	Margin (dB)	Bandwidth (kHz)	Line	Filter	Corr. (dB)
0.150000	---	36.56	56.00	19.44	10.000	N	ON	20.3
0.150000	52.13	---	66.00	13.87	10.000	N	ON	20.3

Figure 84 – EMI Test Results at 115 V.

10.2 Line Input 230 VAC



Final Result

Frequency (MHz)	QuasiPeak (dBµV)	Average (dBµV)	Limit (dBµV)	Margin (dB)	Bandwidth (kHz)	Line	Filter	Corr. (dB)
0.150000	---	43.12	56.00	12.88	10.000	N	ON	20.3
0.150000	56.83	---	66.00	9.17	10.000	N	ON	20.3
29.935000	---	41.54	50.00	8.46	10.000	N	ON	20.4
29.935000	46.57	---	60.00	13.43	10.000	N	ON	20.4
29.965000	---	41.59	50.00	8.41	10.000	N	ON	20.4
29.965000	46.44	---	60.00	13.56	10.000	N	ON	20.4

Figure 85 – EMI Test Results at 230 V.

11 Thermal Performance

There are no heat sinks in cooling arrangements of the assembly. Copper pours are used for the cooling of the control IC. No forced air-cooling was deployed during test. The temperatures of the hottest components in the assembly are shown in Table.

Ambient temperature is 23±2°C .

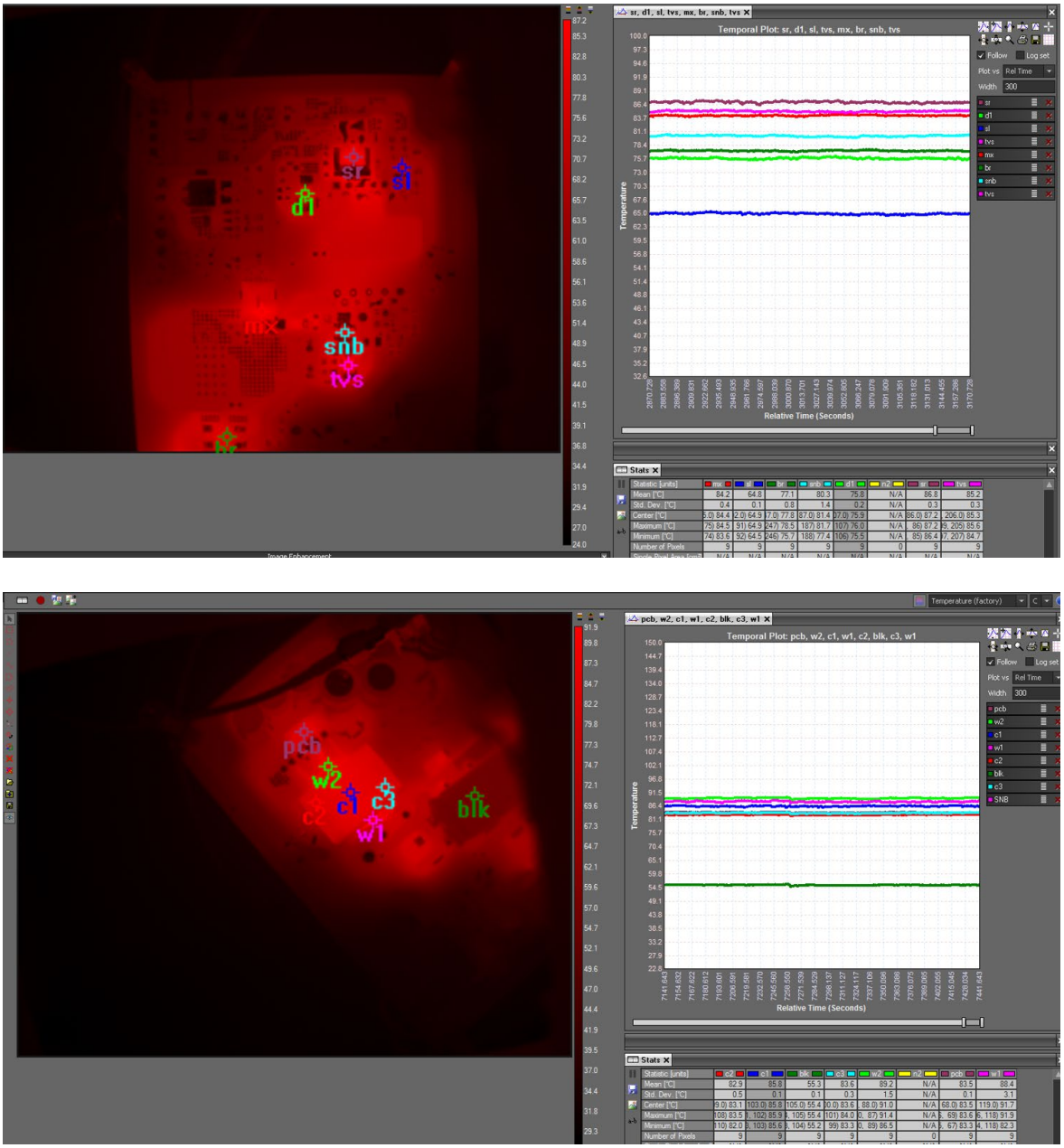
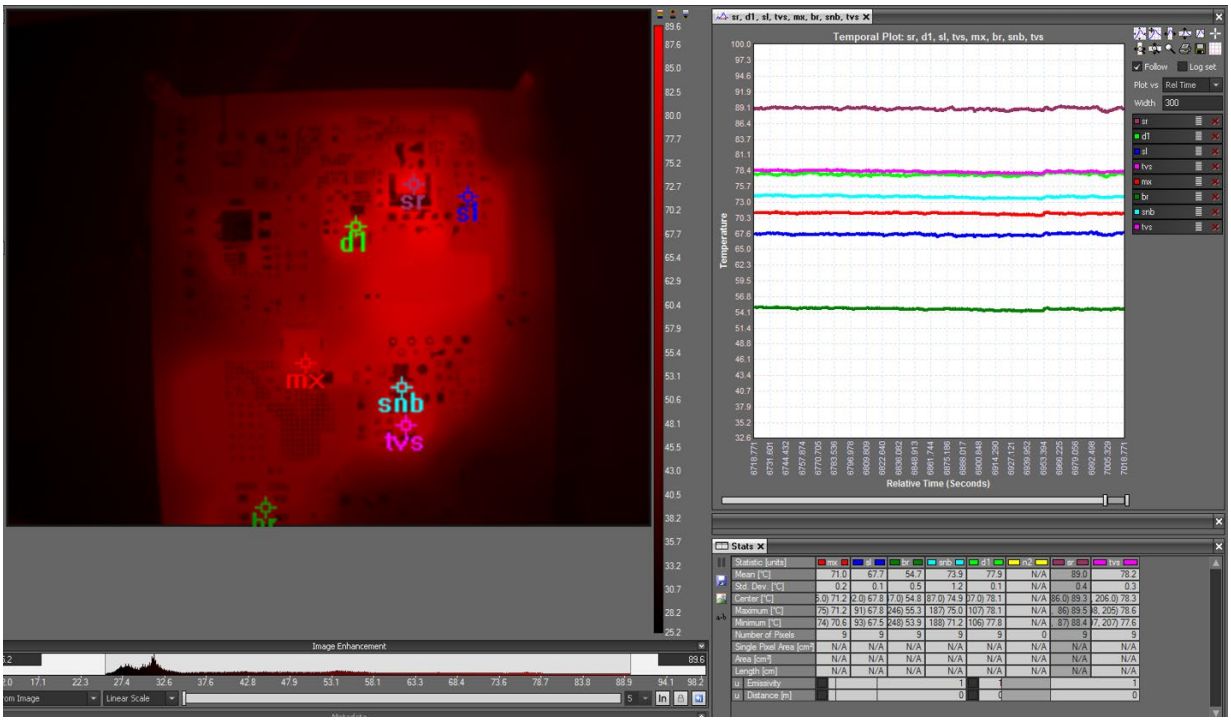
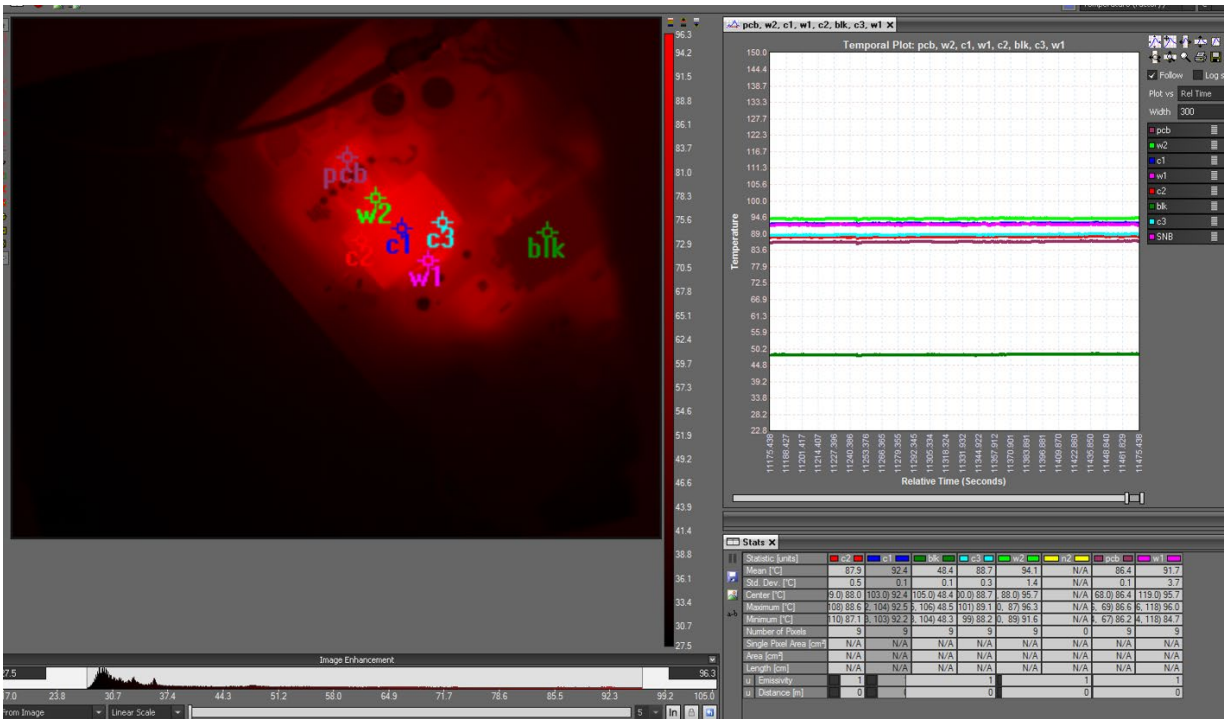


Figure 86 – Line = 90 V Nominal Power - Thermal Image – Bottom&Top Views.

PART	U1 IC	BR1 BRIDGE	VR2 SNUB TVS	SNUB RES	D1 LED DIODE	Q1 SEL FET	D8 SR DIODE	TRF CORE	TRF WINDING
T [ºC]	84.2	77.8	85.2	80.3	75.8	64.8	87.2	85.9	91
ΔT [ºC]	63.2	56.8	64.2	59.3	54.8	43.8	66.2	64.9	70

Table 9 – Line = 90 V Full Power – Component Case Temperatures.


sr
d1
sl
mx
snb
tvs
br
Temporal Plot: sr, d1, sl, tvs, mx, br, snb, tvs
Temperature
Relative Time (Seconds)
Stats
Image Enhancement


pcb
w2
c1
c3
c2
w1
blk
Temporal Plot: pcb, w2, c1, w1, c2, blk, c3, w1
Temperature
Relative Time (Seconds)
Stats
Image Enhancement

PART	U1 IC	BR1 BRIDGE	VR2 SNUB TVS	SNUB RES	D1 LED DIODE	Q1 SEL FET	D8 SR DIODE	TRF CORE	TRF WINDING
T [ºC]	71	54.7	78.2	73.9	77.9	67.7	89.5	92.4	94.1
ΔT [ºC]	50	33.7	57.2	52.9	56.9	46.7	69.5	71.4	73.1

Table 9 – Line = 265 V Full Power – Component Case Temperatures.

12 Audible Noise Performance

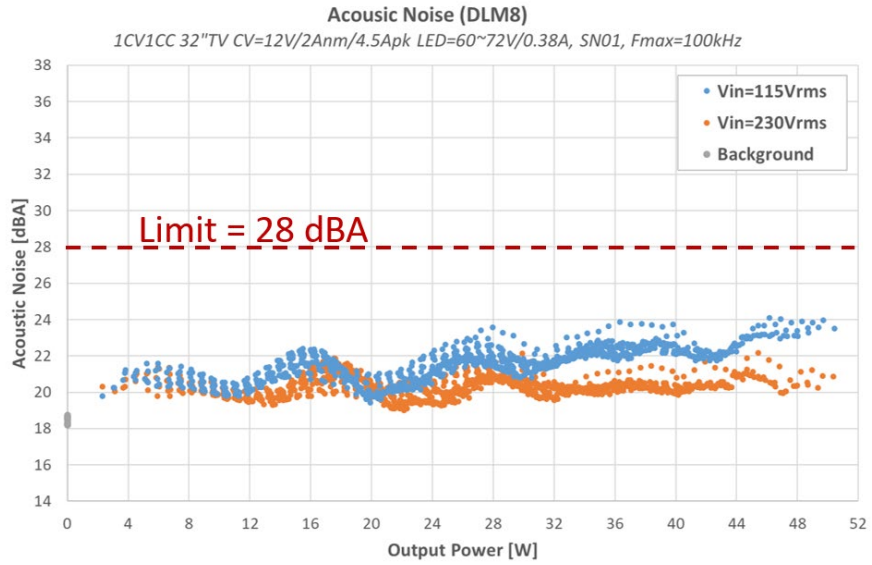


Figure 87 – Audible Noise at normal operation mode.

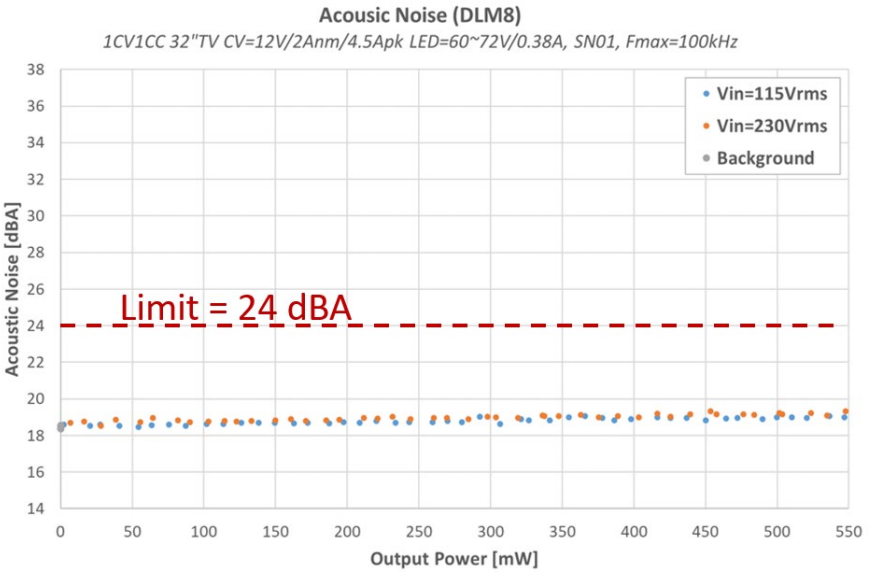


Figure 88 – Audible Noise at standby mode.

13 Combination Wave Surge Test

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 5 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

13.1 Differential Mode Surge (L1 to L2), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result
+1000	L1 to L2	0	Pass
-1000	L1 to L2	0	Pass
+1000	L1 to L2	90	Pass
-1000	L1 to L2	90	Pass
+1000	L1 to L2	180	Pass
-1000	L1 to L2	180	Pass
+1000	L1 to L2	270	Pass
-1000	L1 to L2	270	Pass

Table 10 – Differential Mode Surge Test Result.

13.2 Common Mode Surge (L1 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result
+2000	L1 to PE	0	Pass
-2000	L1 to PE	0	Pass
+2000	L1 to PE	90	Pass
-2000	L1 to PE	90	Pass
+2000	L1 to PE	180	Pass
-2000	L1 to PE	180	Pass
+2000	L1 to PE	270	Pass
-2000	L1 to PE	270	Pass

Table 11 – Common Mode Surge Test Result – L1 to PE.

PE is connected to secondary GND to perform common mode test.

13.3 Common Mode Surge (L2 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result
+2000	L2 to PE	0	Pass
-2000	L2 to PE	0	Pass
+2000	L2 to PE	90	Pass
-2000	L2 to PE	90	Pass
+2000	L2 to PE	180	Pass
-2000	L2 to PE	180	Pass
+2000	L2 to PE	270	Pass
-2000	L2 to PE	270	Pass

Table 12 – Common Mode Surge Test Result – L2 to PE.

PE is connected to secondary GND to perform common mode test.

13.4 10.16.4 Common Mode Surge (L1+L2+PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result
+2000	L2 to PE	0	Pass
-2000	L2 to PE	0	Pass
+2000	L2 to PE	90	Pass
-2000	L2 to PE	90	Pass
+2000	L2 to PE	180	Pass
-2000	L2 to PE	180	Pass
+2000	L2 to PE	270	Pass
-2000	L2 to PE	270	Pass

Table 13 – Common Mode Surge Test Result – L1,L2 and PE

PE is connected to secondary GND to perform common mode test.

13.5 ESD Test

The unit was tested with ±15 kV air discharge and ±8 kV contact discharge with 10 strikes for each condition at the following locations at 230VAC and 115VAC:

- VCV+
- VCV-

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

Contact Discharge	ESD Location	Input Voltage	Test Result
+8kV	VCV+	115VAC	Pass
-8kV	VCV+	230VAC	Pass
+8kV	VCV-	115VAC	Pass
-8kV	VCV-	230VAC	Pass

Table 14 – Contact Discharge Test Result.

Air Discharge	ESD Location	Input Voltage	Test Result
+15kV	VCV+	115VAC	Pass
-15kV	VCV+	230VAC	Pass
+15kV	VCV-	115VAC	Pass*
-15kV	VCV-	230VAC	Pass

* power supply might initiate AR

Table 15 – Air Discharge Test Result.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
26-Feb-24	YL	0.1	Draft Release.	Apps

For the latest updates, visit our website: www.power.com

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