2SML0220D2E0(C)
SCALE-iFlex LT Family

Module Adapted Gate Driver (MAG) for Half-Bridge Power Modules via Electrical Interface

Product Highlights

Highly Integrated, Compact Footprint
- Ready-to-use dual-channel gate driver solution optimized for power modules up to 1700 V blocking voltage
- To be controlled by IMC, e.g. 2SIL1200T2A0(C)
- 1.5 W output power per channel at maximum ambient temperature
- ± 20 A maximum gate current
- Supply voltage to be provide by IMC, e.g. 2SIL1200T2A0(C)
- Operation altitude up to 2000 m
- Optimized for paralleling of up to 6 power modules
- - 40 °C to 85 °C operating ambient temperature

Protection / Safety Features
- Short circuit protection ($V_{CE(SAT)}$ monitoring)
- Overvoltage protection by Advanced Active Clamping (AAC)
- Undervoltage lock-out (UVLO)
- Conformal coating applied on both sides of the PCB

Full Safety and Regulatory Compliance
- Clearance and creepage distances between both sides meet requirements for functional isolation according to IEC 61800-5-1
- RoHS compliant

Applications
- Wind and photovoltaic power
- Industrial drives

Description

The SCALE-iFlex LT gate driver family consists of a central Isolated Master Control (IMC) and Module Adapted Gate Driver (MAG) together with a cable set. The IMC is designed for operation of power modules with a blocking voltage of up to 3300 V, whereas the MAGs are available in various variants optimized for different power modules of different suppliers and chip technologies in the voltage classes from 1200 V to 1700 V.

SCALE-iFlex LT enables easy paralleling of up to six power modules of EconoDUAL™ 3, NX, Dual XT, 2-Pack and equivalent 17 mm types, providing high flexibility and system scalability with minimum development effort.

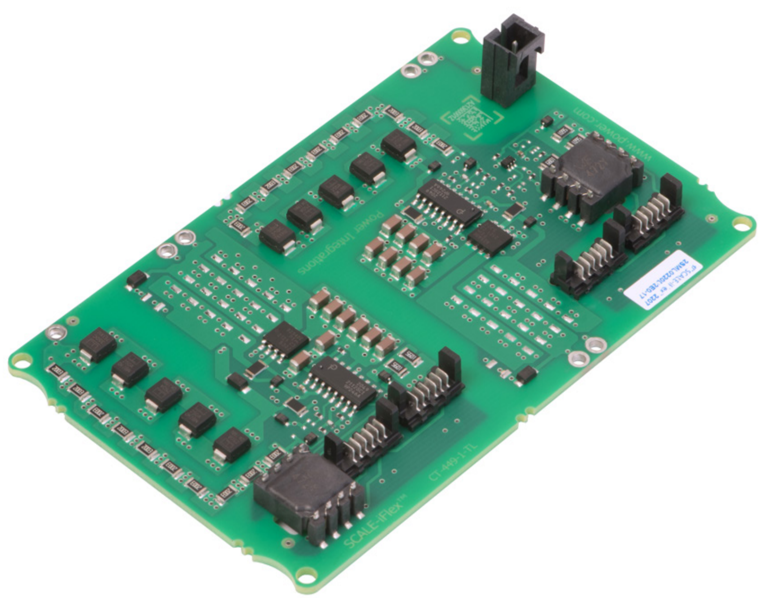

Figure 1. Board Photo of 2SML0220D2E0(C).

EconoDUAL™ 3 is a registered trademark of Infineon Technologies AG

Pin Functional Description

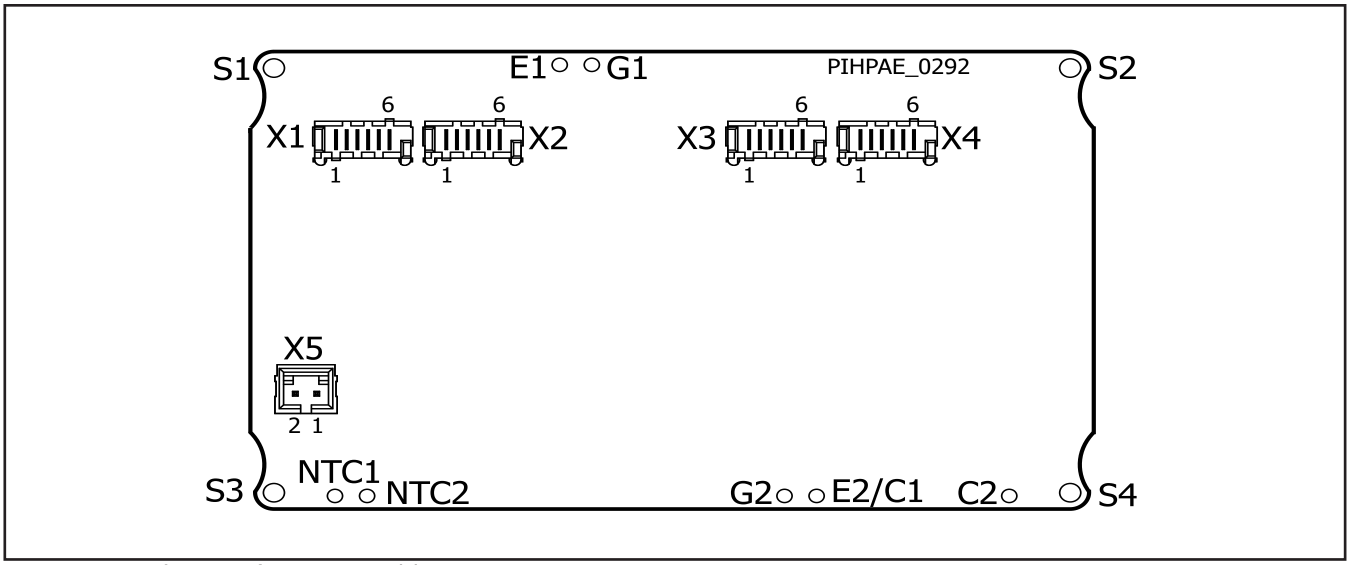

Figure 2. Pin Configuration of 2SML0220D2E0(C).

Connections to Power Module

2SML0220D2E0(C) MAGs are directly soldered to power modules.

E1
Auxiliary emitter contact of lower-side channel switch.

G1
Gate contact of lower-side channel switch.

E2C1
Auxiliary emitter contact of high-side channel switch.

G2
Gate contact of high-side channel switch.

Screw holes S1, S2, S3 and S4
Screw holes for mechanical fixation of the board to the power module.

NTC1, NTC2
Contacts to module internal NTC.

C2
Auxiliary collector contact of high-side channel switch.

Connector X1
Molex 90779-0002 Picoflex Header; Connection from MAG to IMC or previous MAG for gate driver high-side channel.

Connector X2
Molex 90779-0002 Picoflex Header; Connection from MAG to next MAG (if any) for gate driver high-side channel.

Connector X3
Molex 90779-0002 Picoflex Header; Connection from MAG to next MAG (if any) for gate driver low-side channel.

Connector X4
Molex 90779-0002 Picoflex Header; Connection from MAG to IMC or previous MAG for gate driver low-side channel.

Connector X5
Molex 171971-0002 Header 2Pin; NTC connector for read out of internal NTC.

Functional Description of 2SML0220D2E0(C)

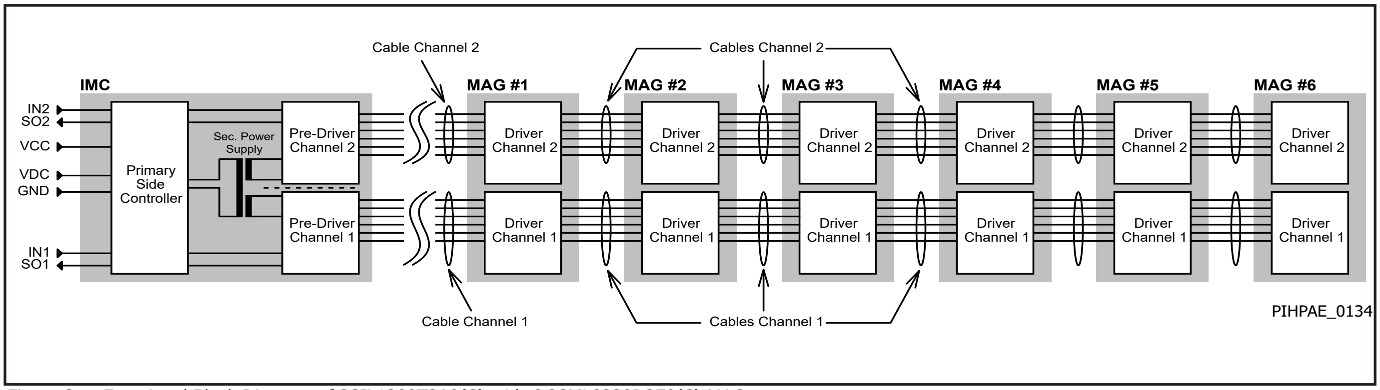

Figure 3. Functional Block Diagram of 2SIL1200T2A0(C) with 6 2SML0220D2E0(C) MAGs.

The 2SML0220D2E0(C) (MAGs) are dual-channel plug-and-play gate drivers for 17 mm power modules. The MAGs are fully mechanically and electrically adapted to the IGBT modules. They work in conjunction with the IMC to drive up to 6 parallel-connected power modules (one MAG per power module is necessary).

Power Supplies

The isolated voltages for the gate driver channels of the MAG are generated by the integrated DC/DC converter of the IMC. The positive rail of the gate driver channels has the voltage level V_{VISO}, while the negative rail is at V_{COM}. Both are referenced to the emitter potential at terminal E1 or E2C1 of the driven power semiconductor.

Gate Voltage

SCALE-iFlex LT possesses a voltage regulator for the positive (turn-on) rail of the gate drive. Internal current sources actively regulate the positive gate-emitter voltage independently of actual load conditions within the maximum specified ratings. As a result of this, the on-state gate-emitter voltage of the power semi-conductor in steady state equals the positive supply voltage V_{VISO}.

The off-state gate-emitter voltage $V_{GE(OFF)}$ in steady-state equals the voltage V_{COM}. This voltage is load dependent. It has its lowest value under no load conditions and increases slightly (getting less negative) with increasing load.

In the event of an under-voltage lock-out condition the gate driver changes the control of the positive rail towards control of the negative rail V_{COM}. By this, potential parasitic turn-on events of the power semiconductor are avoided.

Short-Circuit Protection

The SCALE-iFlex LT gate uses the semiconductor desaturation effect to detect short-circuits.

The desaturation is monitored on each MAG by using a resistor sensing network. To detect a short-circuit, the collector-emitter voltage is checked after the response time t_{RES} at turn-on. If the voltage is higher than the programmed threshold voltage $V_{CE(SAT)}$, the driver identifies this as a short-circuit condition. The monitored power semi-conductor is switched off immediately and a fault signal is transmitted to the IMC. Paralleled MAGs detect desaturation conditions with minimum time delays and turn off the corresponding power semiconductor.

It should be noted that the response time t_{RES} is dependent on the DC-link voltage. It remains constant between about 50% to 100% of the maximum DC-link voltage but increases at lower DC-link voltages. Please refer to the relevant data sheet section.

Note: The desaturation function is for short-circuit detection only and cannot provide over-current protection. However, over-current detection has a lower time priority and can be easily provided by the application.

Gate Clamping

In the event of a short-circuit condition, the gate voltage is increased due to the high dv_{CE}/dt between the collector and emitter terminals of the driven power semiconductor. This dv_{CE}/dt drives a current through the Miller-capacitance (capacitance between the gate and collector) and charges the capacitance, which eventually leads to a gate-emitter voltage higher than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor. To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage each MAG employs gate-clamping circuitry. The gate clamping provides a voltage similar to V_{VISO} (15 V) to the gate. As the effective short-circuit current is a function of the gate-emitter voltage, the short-circuit current is limited. As consequence, the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits, enabling a safe turn-off of the device.

Cable Terminals (X1, X2, X3, X4)

All MAGs have two connector terminals per channel.

The first MAG needs to be connected to the secondary-side of the IMC. Channel 1 from the IMC needs to be connected to channel 1 of the MAG (X1 or X2). Accordingly, channel 2 of the IMC with channel 2 of the MAG (X3 or X4). Note that it is also possible to connect channel 1 of the IMC with channel 2 of the MAG and vice-versa.

In case more than one MAG is used, the first MAG needs to be connected with the second MAG. Accordingly, the second MAG with the third MAG and so on. Note that X1 and X2 respectively X3 and X4 are fully identical and can be exchanged.

Cables

SCALE-iFlex LT gate drivers require a set of cables to establish the electrical connection between the IMC and the first MAG and between paralleled MAGs. The usage of cables allows for flexible positioning of the IMC within the application. Furthermore, it allows adapting to various pitches between paralleled power modules.

Cables recommendations are given in the data sheet of the IMC.

Advanced Active Clamping (AAC)

Active clamping is a technique designed to partially turn on the power semiconductor in case the collector-emitter voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation. Figure 4 illustrates the general behavior of active clamping and its voltage thresholds.

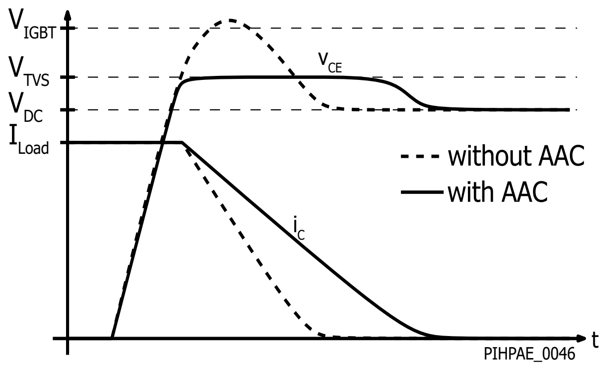

Figure 4. Advanced Active Clamping

Basic active clamping topologies implement a single feedback path from the power semiconductor collector/drain through transient voltage suppressor (TVS) diodes to the power semiconductor gate. The gate driver contains Power Integrations' Advanced Active Clamping (AAC) based on this principle: When active clamping is activated, the turn-off MOSFET of the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature is mainly integrated in the secondary-side ASIC of the gate driver.

It should be noted that AAC should not be activated during regular operation to avoid excessive heating of the transient voltage suppressor diodes.

Conformal Coating

The electronic components of the gate driver 2SML0220D2E0C are protected by a layer of acrylic conformal coating with a typical thickness of 50µm using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.

Note: The accumulation of standing water (e.g. through condensation) on top of the coating layer must be prevented. Standing water will diffuse through the coating over time and will eventually form a thin film between the PCB surface and coating layer, causing leakage currents to increase. Such currents will interfere with the performance of the gate driver

Absolute Maximum Ratings

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Max	Units
Absolute Maximum Ratings[1]					
Gate Output Power Per channel[2]	P_{GX}			1.5	W
Switching Frequency[3]	f_{SW}			10	kHz
DC-Link Voltage	$V_{DC(LINK)}$	Continuous (1.7 kV driver versions)		1200	V
		Continuous (1.2 kV driver versions)		800	V
Operating Voltage	V_{CE}	1.7 kV driver versions		1700	V
		1.2 kV driver versions		1200	V
Common-Mode Transient Peak Voltage	$V_{\Delta E}$	Between parallel connected emitters		50	V_{peak}
Common-Mode Time-Voltage-Area	∫|dv|*dt	Between parallel connected emitters		20	µVs
Storage Temperature[4]	T_{ST}		-40	50	°C
Operating Ambient Temperature	T_A		-40	85	°C
Surface Temperature[5]	T			125	°C
Relative Humidity	H_R	No condensation		93	%
Altitude of Operation[6]	A_{OP}			2000	m

NOTES:
1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. Actually achievable maximum power depends on several parameters and may be lower than the given value. It has to be validated in the final system. It is mainly limited by the maximum allowed surface temperature.
3. This limit applies to the whole product family. The actual achievable switching frequency may be lower for specific gate driver variants and has to be validated in final system as it is additionally limited by maximum gate output power in conjunction with the maximum allowed surface temperature.
4. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
5. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value to ensure long-term reliability of the product.
6. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Characteristics

Parameter	Symbol	Conditions $V_{VDC} = V_{VCC}$ = 15 V (2SIL1200T2A0-33), T_A = 25 °C		Min	Typ	Max	Units
Power Supply							
Power Supply Monitoring Threshold (Secondary-Side)	$UVLO_{VISO}$	Referenced to respective terminal E1 or E2C1	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	
			Hysteresis	0.35			
	$UVLO_{COM}$		Clear fault (resume operation)		-5.15		V
			Set fault (suspend operation)		-4.85		
			Hysteresis		0.3		
Gate Ouput							
Turn-On Gate Voltage	$V_{GE(ON)}$	P_X = 265 mW (IMC), referenced to terminal E1 or E2C1			15		V
		P_X = 10 W (IMC), referenced to terminal E1 or E2C1			15		
Turn-Off Gate Voltage	$V_{GE(OFF)}$	P_X = 265 mW (IMC), referenced to terminal E1 or E2C1			-9.4		V
		P_X = 10 W (IMC), referenced to terminal E1 or E2C1			-7.8		
Short Circuit Protection							
Static V_{CE}-Monitoring Threshold	$V_{CE(SAT)}$	1.7 kV driver versions			44		V
Response Time (10% V_{GE} to 90% V_{GE})	t_{RES}	10% to 90% of V_{GE} (with 1.7 kV)	DC-link voltage= 1200 V		6		µs
			DC-link voltage= 600 V		6.1		
Delay to Turn-Off Power Semiconductor After Short-Circuit Detection	$t_{PD(SOx)}$				0.1		µs

Characteristics (cont.)

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Units
Electrical Isolation						
Creepage Distance	$CPG_{S\text{-}S}$	Secondary-side to secondary-side	6.5			mm
Clearance Distance	$CLR_{S\text{-}S}$	Secondary-side to secondary-side	6.5			mm
Mounting						
Hole size	d_{M3}	Terminals S1 – S4		2.7		mm
Bending	l_{BEND}	According to IPC			0.75	%

Mounting Instruction

2SML0220D2E0(C) is mounted and soldered on top of the target module.

It is recommended to follow mounting instructions from the corresponding power semiconductor manufacturer.

To ensure proper cooling by natural or forced convection minimum clearance of 50 mm of the MAG top side is required. This includes also that the AC and/or DC bus bars are not covering parts or the entire MAG top side.

Product Dimensions of 2SML0220D2E0(C)

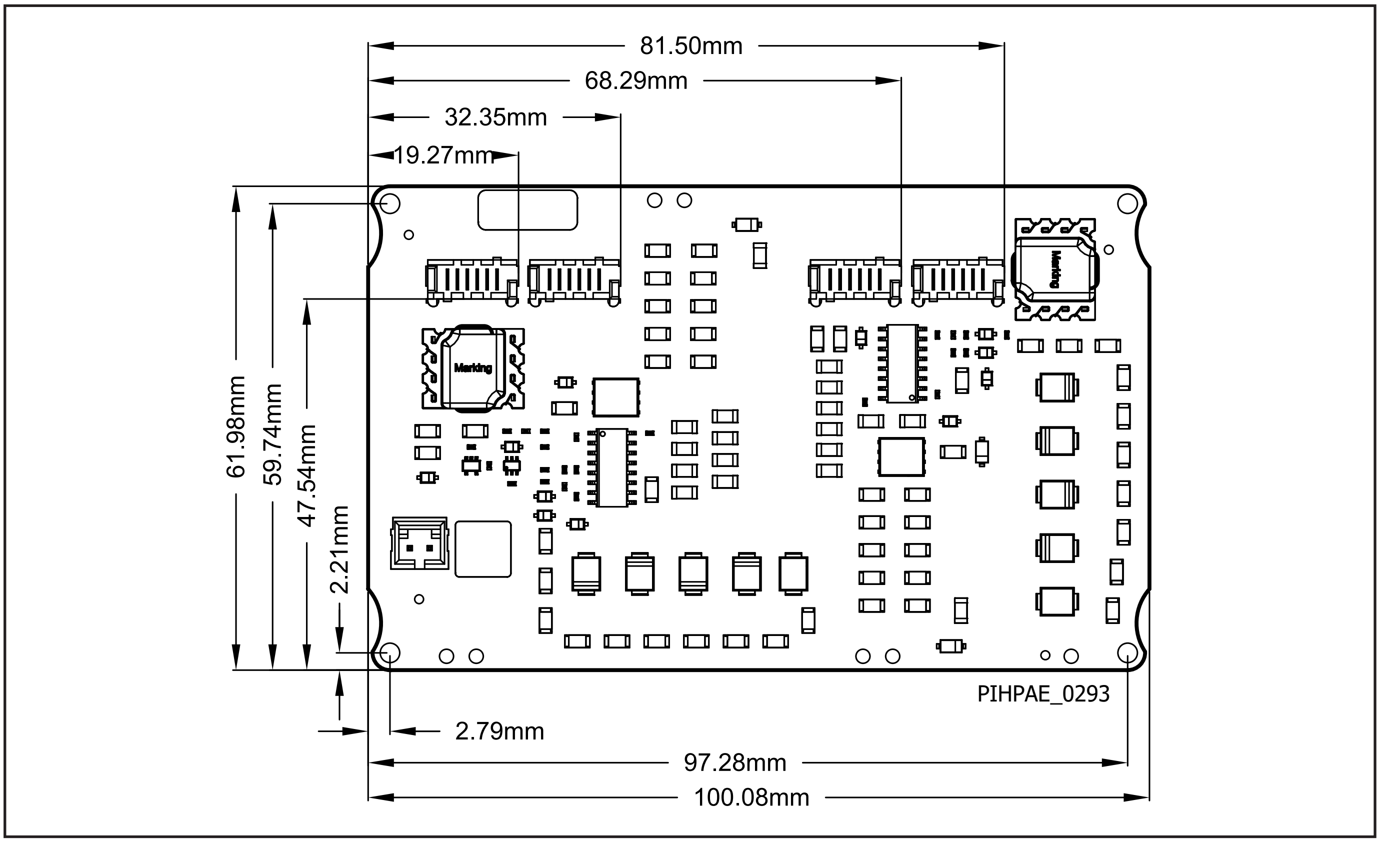

Figure 5. Top View of 2SML0220D2E0(C).

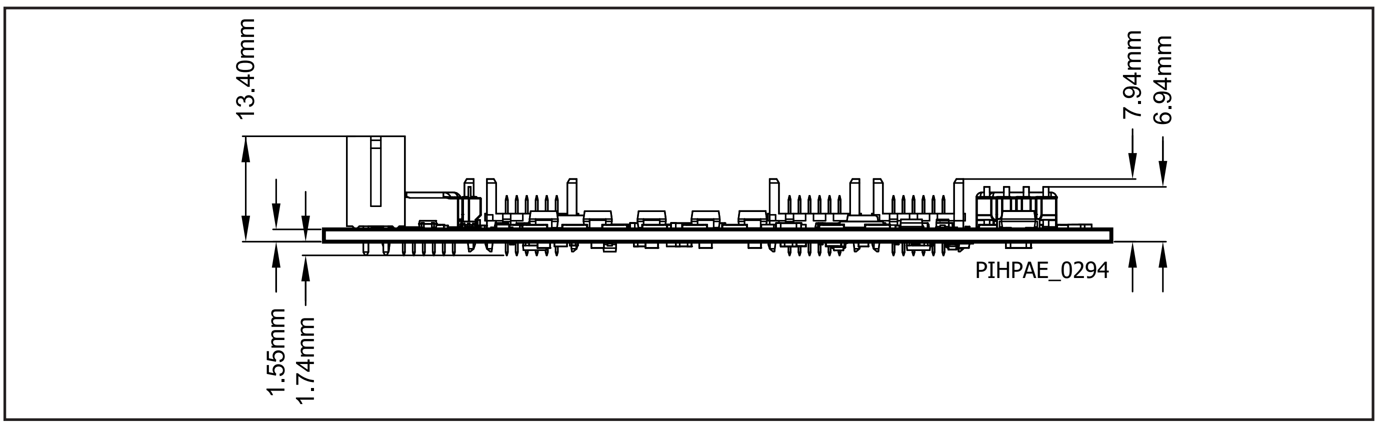

Figure 6. Side View of 2SML0220D2E0(C).

Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances described in Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Product details

Part Number	Power Module	Voltage Class	Current Class	Package	IGBT Supplier	$R_{G(on)}$	$R_{G(off)}$
2SML0220D2E0(C)-FF600R17ME4	FF600R17ME4	1700 V	600 A	EconoDUAL™ 3	Infineon	1.02 Ω	1.5 Ω
2SML0220D2E0(C)-DIM600M1HS17-PA500	DIM600M1HS17-PA500	1700 V	600 A	EconoDUAL™ 3	Dynex	1.02 Ω	1.5 Ω
2SML0220D2E0(C)-FF900R12ME7_B11	FF900R12ME7_B11	1200 V	900 A	EconoDUAL™ 3	Infineon	0.6 Ω	1.82 Ω
2SML0220D2E0(C)-2MBI800XNE120-50	2MBI800XNE-120-50	1200 V	800 A	2-Pack	Fuji Electric	0.54 Ω	4.4 Ω
2SML0220D2E0(C)-FF600R12ME4	FF600R12ME4	1200 V	600 A	EconoDUAL™ 3	Infineon	1.5 Ω	2.2 Ω

Revision	Notes	Date
A	Final Datasheet.	07/24

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