Optimizing Efficiency and Output Regulation for a Dual-Output Flyback With a 1700 V GaN Switch

Han Cui, Yi Li | Power Integrations, USA

Abstract

For industrial applications requiring high-input voltages, silicon carbide (SiC) switches have traditionally been the preferred choice, particularly for input voltages approaching 1000 VDC. However, new high-voltage GaN technology offers an alternative high-efficiency solution.

This paper focuses on optimizing efficiency and output regulation for a 60 W single-stage flyback power supply featuring dual outputs, each offering better than 1 percent regulation across a wide input voltage range of 300 VDC to 1000 VDC and utilizing a 1700 V GaN switch. The circuit achieves zero-voltage switching (ZVS) without additional circuitry, reducing switching losses and allowing the power supply to provide more than 90 percent efficiency across the input range.

1. Introduction

In traditional multi-output flyback converters, achieving accurate output regulation is difficult without the addition of DC-DC post regulators due to cross-regulation effects. The introduction of the second power conversion stage not only reduces system efficiency but also increases component count and PCB size.

This paper presents a single-stage topology that achieves precise regulation without the need for additional circuitry.

1.1 Circuit Topology

The proposed design is a 60 W single-stage, dual-output flyback converter utilizing a novel control method provided by the InnoMux™-2 IC from Power Integrations®. The input range is 300 VDC to 1000 VDC and the outputs are 5 V, 2.5 A and 24 V, 2 A. The 1700 V GaN switch is incorporated into the primary-side switcher IC. Each output is independently regulated through dedicated feedback.

Stacked windings are used in the transformer as shown in Fig. 1. By precisely controlling the selection MOSFET (SEL), the secondary discharge energy is directed only to the output that requests it, thereby improving regulation accuracy for both outputs.

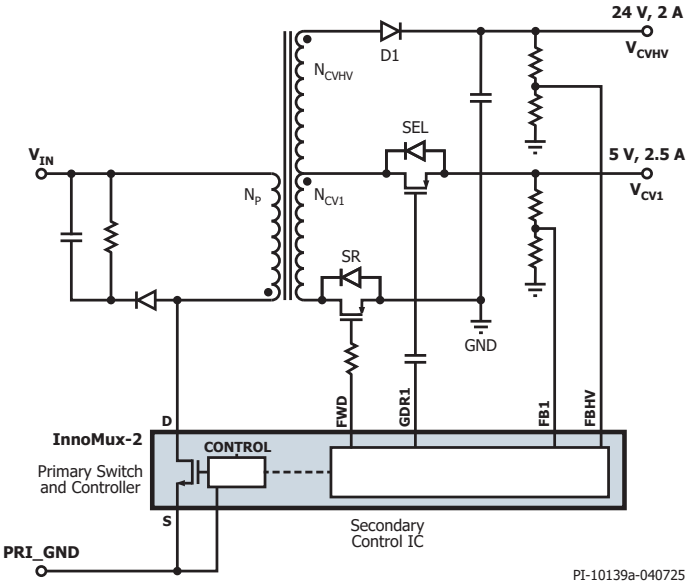

Fig. 1 Single-stage, dual-output flyback converter

1.2 Fundamental Design Principles

To ensure that energy is directed only to the CV1 output when the selection MOSFET is turned on, the output reflected voltages must satisfy:

$$VOR_{cv1} < VOR_{cvhv} \quad (1)$$

$$VOR_{cv1} = V_{SEL1\_Drain} \frac{Np}{Ncv1} \quad (2)$$

$$VOR_{cvhv} = (V_{cvhv} + V_{fwd\_D1}) \frac{Np}{Ncv1 + Ncvhv} \quad (3)$$

Where $V_{SEL1\ Drain}$ is the drain-source voltage of the selection FET (SEL); $V_{fwd\ D1}$ is the forward voltage of the top output diode D1.

$$V_{D1\_anode} = V_{SEL1\_Drain} \frac{Ncv1 + Ncvhv}{Ncv1} \quad (4)$$

$$V_{D1\_anode} < V_{cvhv} + V_{fwd\_D1} \quad (5)$$

This ensures that when the SEL FET is on, the voltage induced on D1 anode V_{D1_anode} is low enough to keep D1 reverse-biased, ensuring that energy is directed only to the CV1 output.

2. Minimizing Cross-Regulation

2.1 Overspill Effect

The proposed topology minimizes cross-regulation by ensuring energy is delivered only to the output requiring it; however, in cases where CVHV operates under no or light load while CV1 is fully loaded, a small amount of unintended energy may spill into CVHV, as the result of a phenomenon referred to as “overspill.”

This condition may arise when the SEL FET is on, and all energy is expected to be directed to the CV1 output. Due to leakage inductance in the transformer and parasitic capacitance in the system, a transient high voltage is induced on the CVHV transformer terminal (D1 anode). If this voltage exceeds V_{cvhv} + V_{fwd_D1}, D1 becomes forward-biased and begins conducting, a small portion of the secondary current is then “spilled” to CVHV, affecting accuracy.

This condition can be expressed as:

$$V_{D1\_anode\_transient} > V_{cvhv} + V_{fwd\_D1} \quad (6)$$

Where $V_{D1\_anode\_transient}$ represents the transient voltage induced on the anode of D1 due to primary-secondary energy transition. When Eq. (6) is satisfied, an unintended current discharge flows into the CVHV output. This unwanted discharge will cause the output voltage to rise, reducing regulation accuracy.

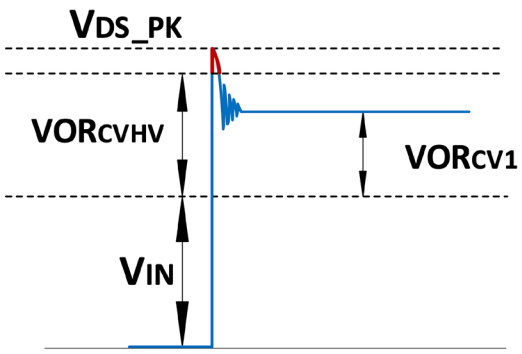

Fig. 2 Peak drain-source voltage on the primary switch when SEL FET is on

As shown in Fig. 2, on the primary side the "overspill" condition occurs when the transient voltage across the primary winding $V_{DS\ PK}$ exceeds $V_{OR\ CVHV} + V_{IN}$. This condition is expressed as follows:

$$V_{DS\_PK} - V_{IN} > V_{OR\_CVHV} \qquad (7)$$

Where $V_{DS\ PK}$ is the transient voltage across the primary switch drain-source at primary turn-off; V_{IN} is the input DC voltage.

2.2 Optimizing Regulation by Eliminating Overspill

Overspill can be prevented by maintaining D1 in a reverse-biased state during secondary discharge to CV1. This requires:

$$V_{DS\_PK} < V_{OR\_CVHV} + V_{IN} \qquad (8)$$

While parasitic elements may influence the accuracy of Eq. (8), it serves as a good design rule for minimizing overspill effects.

3. Zero-Voltage Switching

Switching loss on the primary switch is a second-order effect that becomes critical at high-input voltage. Zero-voltage switching (ZVS) is achieved for the 1700 V GaN switch without additional circuitry by leveraging the SR FET.

3.1 Discontinuous Conduction Mode ZVS

ZVS is limited to discontinuous conduction mode (DCM) as a reverse current must be generated before the primary switch turns on. In power supply design, lower input voltages typically favor continuous conduction mode (CCM) to minimize RMS current, thus reducing conduction losses. This design operates exclusively in DCM to optimize switching losses across the entire 300 VDC to 1000 VDC input range.

3.2 Operating Principles

The ZVS operation, illustrated in Fig. 3 and Fig. 4, follows these steps:

1. Before the primary switch turns on, the SR FET is turned on for a brief period, creating a reverse current on the secondary side.

2. After the SR FET turns off, the reverse current is commutated to the primary side, discharging the primary switch drain-source voltage $V_{DS\ Pri}$. When $V_{DS\ Pri}$ approaches zero, the primary switch turns on, achieving ZVS.

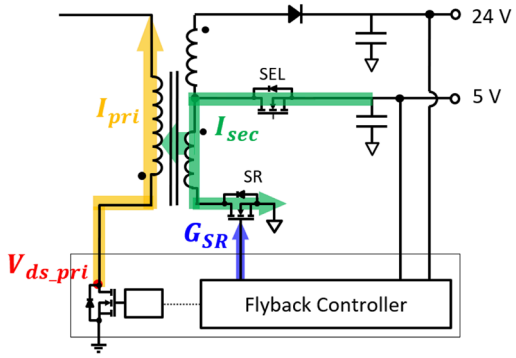

Fig. 3 ZVS operation

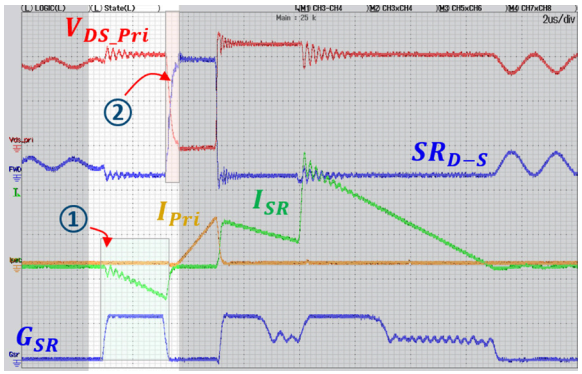

Fig. 4 ZVS waveform

4. Results

4.1 Evaluation Board

A prototype evaluation board was built with the following specifications:

- Input: 300 VDC to 1000 VDC
- Outputs:
  - 5 V, 2.5 A
  - 24 V, 2 A
- Output regulation: <±1 percent
- Efficiency: >90 percent across the input range

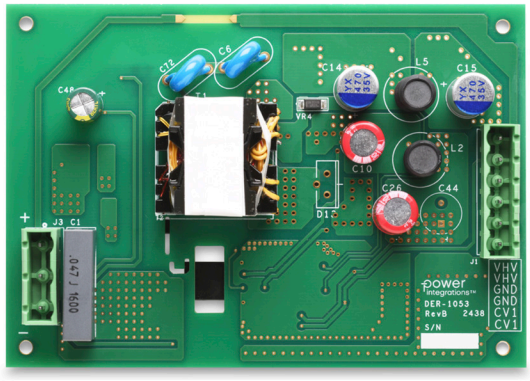

Fig. 5 Evaluation board top side [1]
(Reference Design RDR-1053, InnoMux-2 IC IMX2253F-H415)

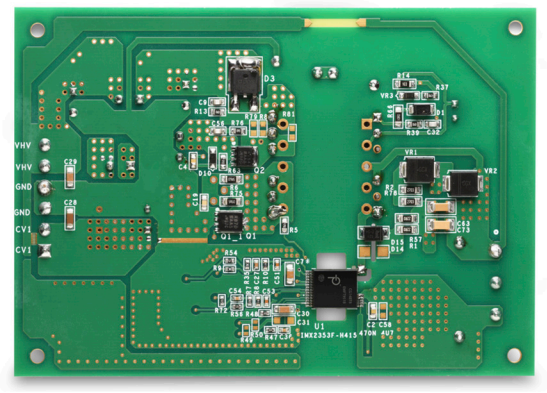

Fig. 6 Evaluation board bottom side [1]

4.2 Output Regulation

Output regulation performance was evaluated with and without the overspill effect. Testing was conducted across varying load conditions on both outputs, ranging from no load to full load. As shown in Fig. 8 and Fig. 10, when the primary switch drain-source voltage $V_{DS\ PK}$ remains below $V_{OR\ CVHV} + V_{IN}$, the regulation accuracy on CVHV output is kept within ±1 percent across load and line.

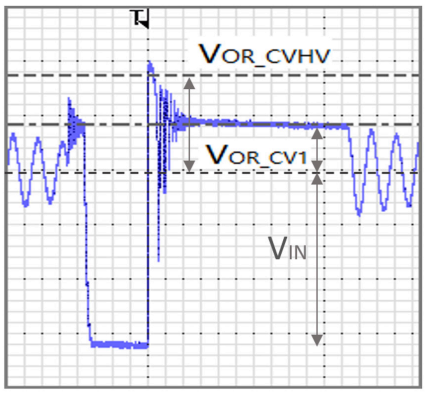

Fig. 7 Primary switch transient drain-source voltage, $V_{DS\ PK} > V_{OR\ CVHV} + V_{IN}$, with overspill effect

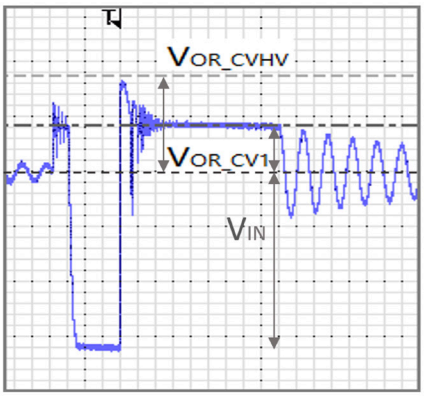

Fig. 8 Primary switch transient drain-source voltage, $V_{DS\ PK} < V_{OR\ CVHV} + V_{IN}$, no overspill effect

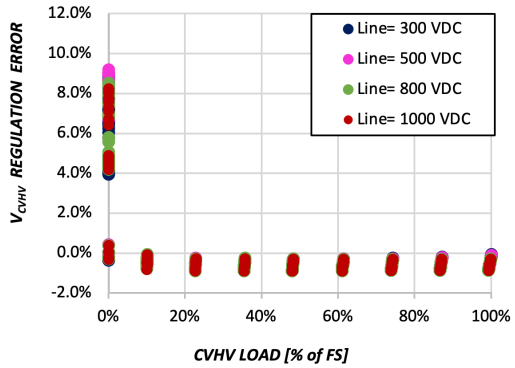

Fig. 9 CVHV output voltage regulation with overspill effect, 0 percent -100 percent load on CV1 (5 V) & CV2 (24 V)

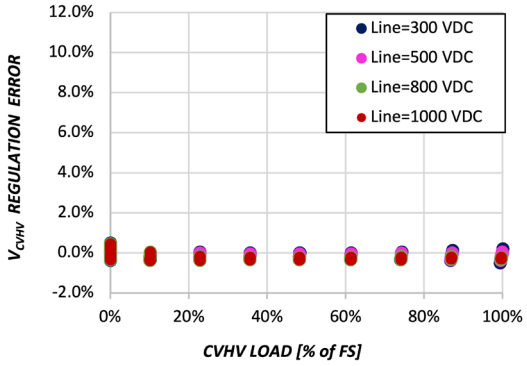

Fig. 10 CVHV output voltage regulation with no overspill effect, 0 percent – 100 percent load on CV1 (5 V) & CV2 (24 V)

4.2 Efficiency

Figure 11 shows the efficiency with and without ZVS. It is notable that at 1000 VDC, the implementation of ZVS results in an efficiency improvement of more than 1 percent.

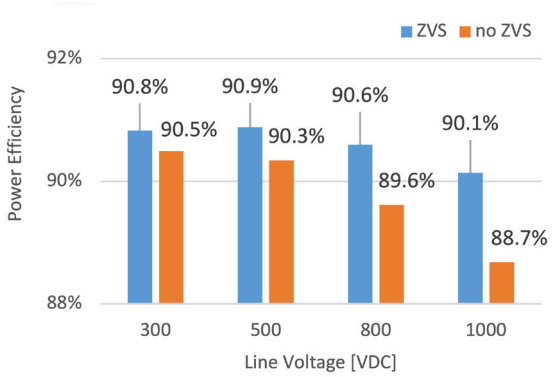

Fig. 11 Efficiency improvement with ZVS

4.3 Thermal Performance

In addition to the efficiency improvements, ZVS also significantly enhances thermal performance.

At 1000 VDC, ZVS reduces the rise in IC temperature from 81.6 °C to 22.3 °C – a nearly 80 percent reduction; while at 800 VDC, the decrease is around 60 percent. At 300 VDC and 500 VDC, thermal improvement is less significant as the main source of heat comes from conduction loss rather than switching loss. This is confirmed by the higher IC temperature rise at 300 VDC than at 500 VDC despite the benefit of ZVS due to the dominance of conduction loss. ZVS is most beneficial in high-voltage applications.

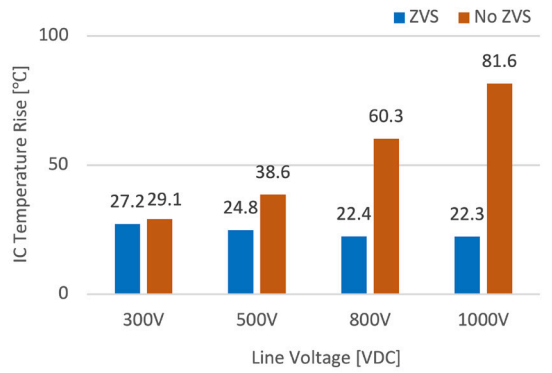

Fig. 12 IC temperature rise improvement with ZVS, tested at room temperature 25 °C

5. Conclusion

This paper presents a single-stage, dual-output flyback converter utilizing a 1700 V GaN switch, demonstrating significant improvements in efficiency and output regulation for high-input voltage applications. This novel control method eliminates the need for secondary-stage regulators while still achieving better than ±1 percent regulation across the 300 VDC to 1000 VDC input range.

The implementation of ZVS effectively reduces switching losses, leading to a measured efficiency above 90 percent across line. The reduction in switching losses also brings significant thermal performance gains, particularly at higher voltages. These results highlight the advantages of high-voltage GaN technology in industrial power conversion, offering an efficient alternative to traditional SiC-based solutions.

References

[1] Power Integrations, “RDR-1053 - 60 W Dual-Output Flyback Power Supply for Industrial Applications Using InnoMux2-EP (1700 V PowiGaN),” [Accessed: Feb. 13, 2025]. https://www.power.com/design-support/design-examples/rdr-1053-60-w-dual-output-flyback-power-supply-1000-vdc-industrial-using-innomux2-ep-1700v-powigan.

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