Title	**50 W Flyback Converter with Two Independently Regulated Outputs Using InnoMux™2-EP IMX2378F-H415**
Specification	90 VAC – 265 VAC Input; 12 V / 1.67 A and 24 V / 1.25 A Outputs
Application	Independently Regulated Multi-Output PSU
Author	Applications Engineering Department
Document Number	RDR-1043
Date	October 07, 2025
Revision	D

Summary and Features

Unique single-stage, multi-output flyback architecture:

- Eliminates Post-regulators
- High efficiency across line
- Accurate independently regulated 12 V and 24 V outputs
  - ±1% voltage accuracy across line and load
- Safety features
  - Output overvoltage protection (OVP)
  - Thermal protection with hysteretic shutdown
  - Input voltage monitor with brown-in/brown-out and line overvoltage protection

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This report describes a dual output off-line flyback power supply intended for appliances, industrial applications, or smart meters, and utilizes the IMX2378F-H415 from the InnoMux2-EP family of ICs.

The power supply has two Constant Voltage (CV) outputs: 1.67 A, 12 V and 1.25 A, 24 V, and can deliver a total maximum output power of 50 W across universal mains input (90 VAC to 265 VAC). This design shows the high efficiency and accurate output regulation achieved by the multiplexing power control algorithm of the InnoMux-2 IC. The design demonstrates a high level of integration and high efficiency possible for a multi-output design using this technology.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

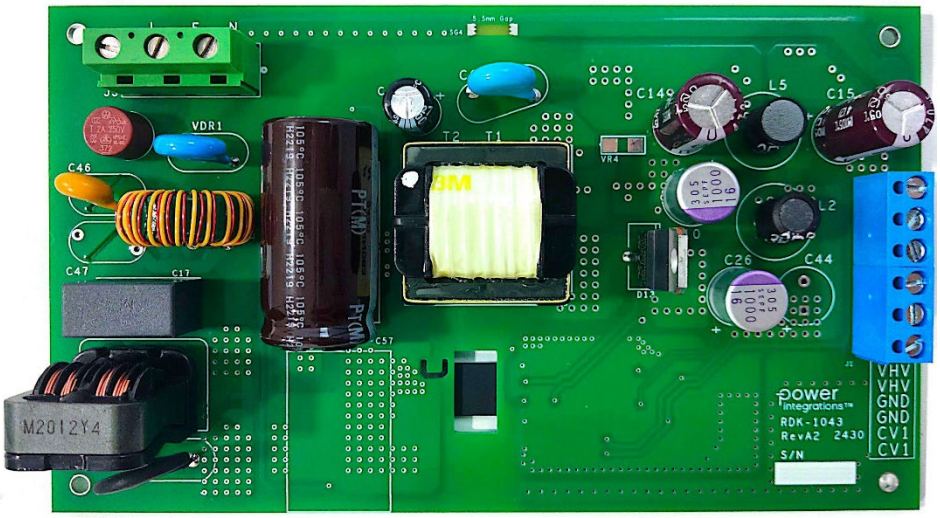


Figure 1 – Populated Circuit Board, Top.

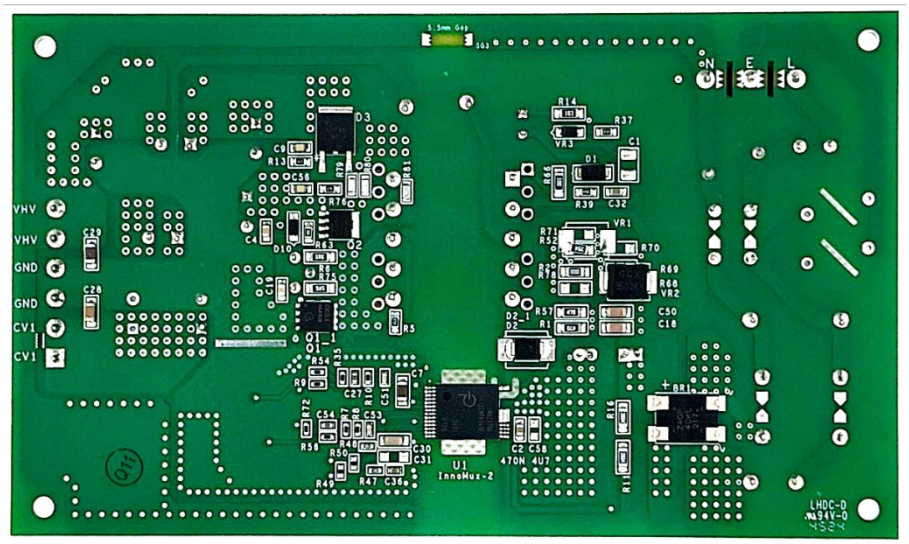


Figure 2 – Populated Circuit Board, Bottom.

Note:
List of unpopulated component positions (not included in the schematic)
C1 – provision for additional high frequency filtering in primary bias
R49, R50 and C31 - provision for a network to be used if VCV2 (pin 12) is required to provide the supply voltage for the secondary controller
C44 – position for additional output capacitor for the VCV1 output
C47 – provision for additional Y capacitor in EMI filter
C57 – provision for additional bulk capacitor (C3)
C58 – provision for additional BPP capacitor (C2)
D2_1 – provision for a larger primary snubber diode (D1)
Q1_1 – provision for an SR FET (Q1) with a different package
R68, R69, R70, R71, R78 and VR1 – provision for different primary snubber configurations
T2 – provision for a PQ26/20 sized transformer
VR4 - provision for a Zener diode in the transformer's output going to CV1

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is shown in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	11.4	12	12.6	V	±5%.
Output Ripple Voltage 1	$V_{RIPPLE1}$			240	mV_{pk-pk}	±1%, 20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		1.67	A	
Output Voltage 2	V_{OUT2}	22.8	24	25.2	V	±5%.
Output Ripple Voltage 2	$V_{RIPPLE2}$			960	mV_{pk-pk}	±2%, 20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0		1.25	A	
Output Power	P_{OUT}		50		W	
Efficiency						
Full Load	η		90		%	Measured at 230 VAC, 25 ºC.
Standby Input Power				<0.3	W	Measured at 230 VAC, 25 ºC, 5 V, 30mA.
Environmental						
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.
Audible Noise Limit, in operation				<28	dBA	Measured at 115 VAC, 230 VAC. 0 to 50 W load, 3 % increment.
Audible Noise Limit, in standby				<24	dBA	Measured at 115 VAC, 230 VAC. CVHV output = 0 A. CV1 = 0 mW to 250 mW.

Table 1 – Power Supply Specifications.

3 Schematic

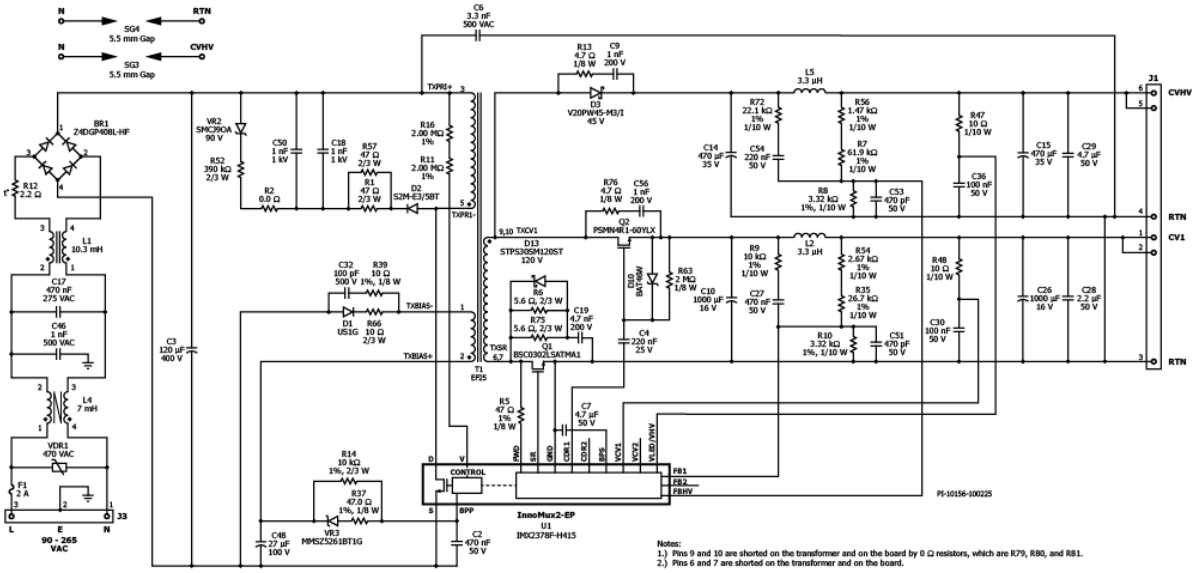


Figure 3 – Schematic.

4 Circuit Description

4.1 Input Rectifier and EMI Filter

A two-stage EMI filter is used, L1 and C17, for low frequency and L4, C46 and C47 for high frequency.

The bulk storage capacitor C3 provides DC voltage smoothing after the bridge rectifier BR1. Varistor VDR1 provides protection against differential voltage surges. Resistor R12 (NTC) limits the inrush current during power up. Fuse F1 prevents the PSU from drawing excessive current from the mains in the event of catastrophic circuit failure.

4.2 Primary-Side

4.2.1 Primary Switch Switching Circuit

The transformer primary is connected between the input DC bus (T1, pin 3) and the drain D of the integrated primary switch of the InnoMux2-EP IC (U1, pin 28). The primary current loop closes at the negative terminal of C2 via the S pin (tab) of U1 (pin 19). An R2CD type primary clamp (D2, R1, R57, R2, R52, VR2, C18 and C50) is used to limit the peak drain voltage on the primary switch induced by the transformer leakage inductance and output trace inductance when the switch turns off.

4.2.2 Primary-Side Controller Power Source and OVP Protection

The primary-side controller is part of the InnoMux2-EP IC (U1) single chip solution. It is self-starting, using an internal high-voltage current source connected to the DRAIN pin to charge the BPP capacitor, C2, when AC voltage is first applied to the converter input. During normal operation (steady-state), the primary-side of the controller is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D1 and capacitor, C48. Resistor R66 limits transient current. The primary auxiliary output is connected to the BPP pin via current limiting resistor R14.

4.2.3 Primary-Side OVP, Brown-In and Brown-Out Protection

Primary-side output overvoltage protection (OVP) is implemented via a Zener diode, VR3 and series resistor, R37. In the event of an uncontrolled overvoltage at the output, the increased voltage across the bias winding causes the Zener diode, VR3, to conduct increasing the current into the BPP pin. If this current exceeds I_{SD} = 7.5 mA, OVP protection is triggered, and the controller implements a latched shutdown.

Resistors, R11 and R16, provide line voltage sensing for brown-in and brown-out and are set to approximately 75 VAC and 65 VAC respectively.

4.2.4 Primary Peak Current Limit

The value of capacitor C2 is used to set the maximum primary current to STANDARD or to INCREASED level. In this case, 470 nF capacitance sets the primary-side controller peak current limit to its STANDARD level of 1.7 A.

4.3 Secondary-Side

The secondary-side of the InnoMux2-EP IC (U1) is powered from the BPS rail which is internally regulated to 5 V. Capacitor C7 is a local decoupling capacitor.

4.3.1 Secondary to Primary Communication

The secondary-side of the InnoMux2-EP IC (U1) sends switching requests to the primary-side controller via the internal FluxLink™ galvanically isolated communication channel.

4.3.2 InnoMux2-EP Power Supply

During start-up, the InnoMux2-EP secondary-side controller is powered from VHV via R47. A local decoupling capacitor C36, connected close to the VHV pin of U1. Resistor R47 and capacitor C36 are optional and provide additional ESD protection. An internal regulator lowers the VHV voltage to 5 V and supplies it to the BPS bus (U1, pin 6).

In steady state, when the voltage on VCV1 (U1, pin 11) rises above the BPS source threshold $V_{BPS(VCV1)}$ (~7.9 V), the power input of the internal BPS regulator is switched from VHV to VCV1. Resistor R48 and capacitor C30 provide local decoupling and ESD protection.

4.3.3 Synchronous Rectifier (SR) MOSFET Drive

The SR pin is used to drive the SR MOSFET (Q1) when the transformer is delivering energy to the secondary circuit. The gate voltage of the SR MOSFET is reduced before the end of secondary discharge, to keep sufficient SOURCE to DRAIN voltage across the SR MOSFET. This prevents premature turn off the SR MOSFET.

In DCM operation the SR MOSFET (Q1) is turned on for a short period shortly before the primary switch is turned on. This action generates a reverse current in the CV1 secondary winding, which then causes a reverse current flow in the transformer on the primary-side due to commutation when the SR MOSFET is turned off. This reverse current discharges the voltage across the primary switch reducing it to close to zero, allowing the primary switch to turn on at zero-voltage. This is described as SR-ZVS and substantially reduces switching loss.

4.3.4 Selection MOSFET Drive for Q2

The gate drive for the selection MOSFET Q2 is approximately equal to the voltage on amplitude of the BPS rail (5 V). Consequently, logic level MOSFETs must be used. When CDR1 is low, capacitor C4 is charged up to the level of V_{CV1} from the CV1 output via diode D10. When the selection MOSFET Q2 needs to be turned on, the voltage on the CDR1 pin is raised from GND to BPS potential causing the gate voltage of the selection MOSFET to rise to $V_{CV1}+V_{BPS}$.

4.3.5 Output Control

Rectification for the CV1 output is provided by the synchronous rectifier MOSFET (Q1) and the CV1 selection MOSFET (Q2). To ensure low output ripple voltage, a π – type LC filter (C10, C26 and L2) is employed. A low ESR capacitor, C10, is used in the first stage to reduce the ripple current. Capacitor, C26, is an Al-polymer type and minimizes switching noise. Additionally, a multilayer ceramic (MLC) capacitor C28 is connected across the CV1 output terminals to provide a low-impedance bypass for high-frequency noise.

Output rectification for the CVHV output is provided by SR FET (Q1) and diode (D3). Very low-ESR capacitors, C14 and C15, provide energy storage and filtering at the output. An inductor, L5, is inserted between C14 and C15 to reduce the ripple and noise at the CVHV output.

The RC snubber network (R6, R75, C19 and D13) damps high-frequency ringing across the SR MOSFET Q1. This ringing is a result of the transformer leakage inductance and the secondary trace inductance acting with the MOSFET parasitic capacitance to cause oscillation. The RC snubber network, R76 and C56, damp high-frequency ringing across the CV1 selection MOSFET Q2, while the RC snubber network, R13 and C9, reduces high-frequency transient voltages across the CVHV diode (D3).

When both the selection MOSFET (Q2) and the SR FET (Q1) are turned on, the transformer secondary winding turns ratios ensure the voltage on the anode of D3 is below VCVHV. As a result, D3 remains reverse-biased, and all transformer energy is directed to the CV1 output through Q1.

When the selection MOSFET (Q2) is turned off, and SR MOSFET (Q1) is turned on, the voltage on the anode of D3 rises until it is forward-biased. In this state, all the transformer energy is then directed to CVHV output.

The VCV1 output voltage is set by R35, R54, R10 and C51 with control provided to FB1 (U1, pin 1). Loop compensation is necessary due to L2 and is provided by R9 and C27. The VCVHV output voltage is set by R7, R56, R8 and C53 with the control signal provided to FBHV (U1, pin 8). Loop compensation is necessary due to L5 and is provided by R72 and C54.

5 PCB Layout

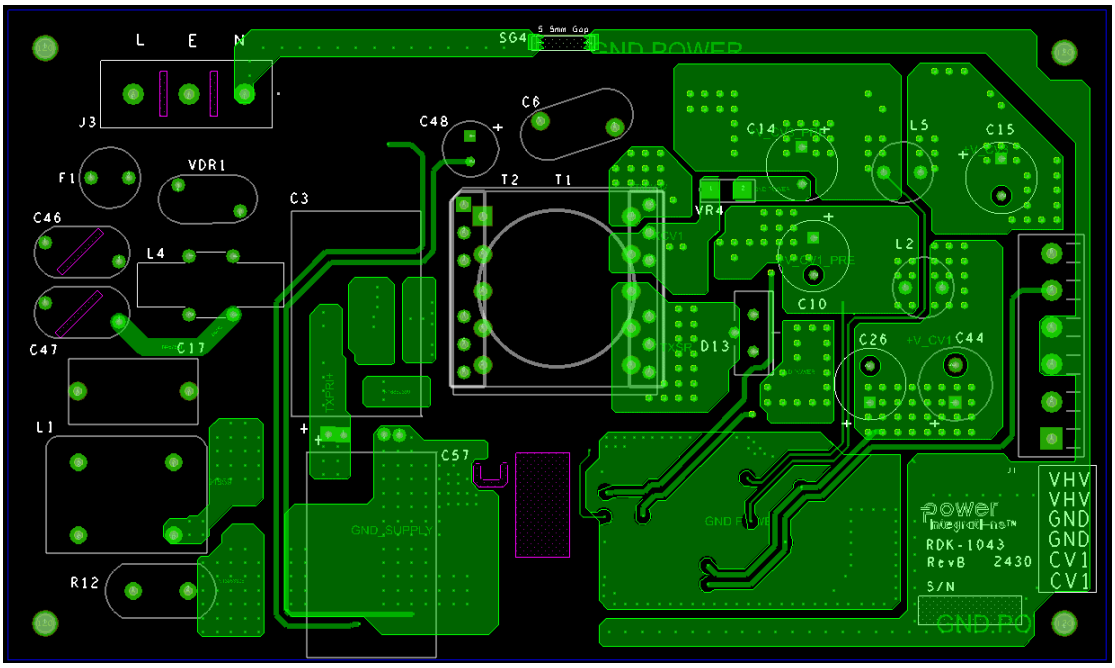


Figure 4 - Printed Circuit Board Layout, Top.

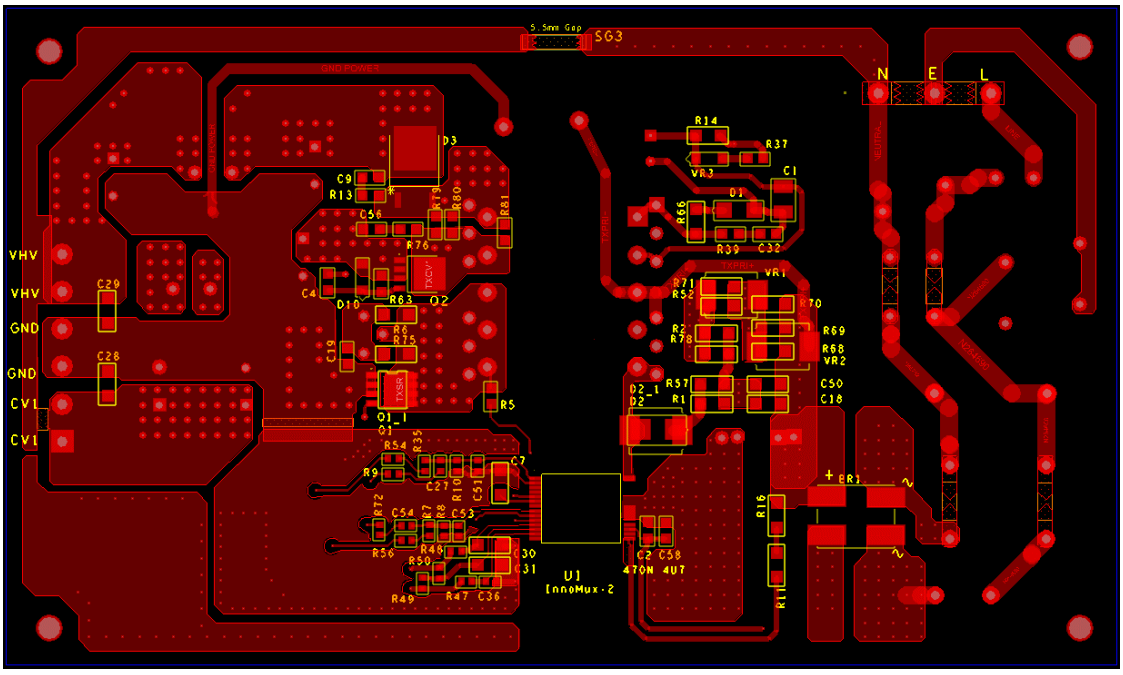


Figure 5 - Printed Circuit Board, Bottom.

6 Bill of Materials

Item	Ref Des	Description	Mfg Part Number	Mfg
1	BR1	RECT BRIDGE, GP, 800V, 4A, Z4-D	Z4DGP408L-HF	Comchip Tech
2	C2	470 nF, ±10%,50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung
3	C3	120 uF, 400 V, Electrolytic, (18 x 35.5)	UPT2G121MHD6	Nichicon
4	C4	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
5	C6	3300 pF,500 VAC, Film, X1Y1	DE1E3RA332MA4BQ01F	Murata
6	C7	4.7 uF, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
7	C9	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX Corp
8	C10	1000 µF, ±20%, 16 V, Aluminum - Polymer Capacitors Radial, Can, 12mOhm 5000 Hrs @ 105°C, (10 x 13)	16SEPF1000M+T	Panasonic
9	C14	470 uF, 35 V, Electrolytic, Low ESR, 23 mOhm, (10 x 20)	UHD35470MPD	Nichicon
10	C15	470 uF, 35 V, Electrolytic, Low ESR, 23 mOhm, (10 x 20)	UHD35470MPD	Nichicon
11	C17	470 nF, 275 VAC, Film, X2	80-R46KI347050P1M	Kemet
12	C18	1 nF, 1000 V, Ceramic, X7R, 1206	CC1206KKX7RCBB102	Yageo
13	C19	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX Corp
14	C26	1000 µF, ±20%, 16 V, Aluminum - Polymer Capacitors Radial, Can, 12mOhm 5000 Hrs @ 105°C, (10 x 13)	16SEPF1000M+T	Panasonic
15	C27	470 nF, 50 V, Ceramic, X7R, 0603	UMK107B7474KA-TR	Taiyo Yuden
16	C28	2.2 uF, ±10%,50 V, Ceramic, X7R, 1206 (3216 Metric)	CL31B225KBHNNNE	Samsung
17	C29	4.7 uF, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
18	C30	100 nF, 50 V, Ceramic, X7R, 1206	CC1206KRX7R9BB104	Yageo
19	C32	100 pF, 500 V, Ceramic, NP0, 0805	501R15N101KV4T	Johanson Die
20	C36	0.1 µF (100 nF) ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	GCM188R71H104KA57D	Murata
21	C46	1 nF, 500Vac, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay BC Components
22	C48	27 uF, ±20%, 100 V, Al Electrolytic, Gen. Purpose, Can, (8mm x 13mm)	EEU-FS2A270B	Panasonic
23	C50	1 nF, 1000 V, Ceramic, X7R, 1206	CC1206KKX7RCBB102	Yageo
24	C51	470 pF, ±10%, 50V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60mm x 0.80mm)	CL10B471KB8NFNC	Samsung
25	C53	470 pF, ±10%, 50V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60mm x 0.80mm)	CL10B471KB8NFNC	Samsung
26	C54	220 nF 50 V, Ceramic, X7R, 0603	CGA3E3X7R1H224K	TDK Corp
27	C56	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX Corp
28	D1	DIODE ULTRA FAST, GPP, 400V, 1A SMA	US1G-13-F	Diodes, Inc
29	D2	Diode 1000 V 1.5A Surface Mount DO-214AA (SMB)	S2M-E3/5BT	Vishay
30	D3	Diode, Schottky, 45 V, 20A, Surface Mount SlimDPAK, TO-252AE	V20PW45-M3/I	Vishay
31	D10	DIODE, SCHOTKY, 100V, 0.075A, SOD123	BAT46W-TP	Micro Com
32	D13	Diode, Schottky, 120 V, 30 A, Through Hole, TO-220AB	STPS30SM120ST	ST
33	F1	2 A,250V, Slow, TR5	37212000411	Wickman
34	J1	CONN TERM BLOCK 5.08MM 6POS, Screw - Leaf Spring, Wire Guard	OSTTA064163	On Shore Tech
35	J3	3 Position Wire to Board Terminal Block, Horizontal with Board, 0.300" (7.62mm) Through Hole	282845-3	TE Connect
36	L1	CMC 10.3MH 2.0A 0.15OHM WIDE IMP	SSR21NVS-M20103	KEMET
37	L2	3.3 uH, 5.5 A	RL622-3R3K-RC	JW Miller
38	L4	7 mH, ±10%, Toroidal Common Mode Choke	30-00652-00	Power Integrations
39	L5	3.3 uH, 5.5 A	RL622-3R3K-RC	JW Miller
40	Q1	MOSFET, N-Channel 120 V 12A (Ta), 99A (Tc) 156W (Tc) Surface Mount PG-TDSON-8-7, TDSON-8-7	BSC0302LSATMA1	Infineon
41	Q2	MOSFET, N-Channel 60 V 100A (Tc) 238W (Tc) Surface Mount LFPAK56, Power-SO8, SC-100, SOT-669, SOT-669-4	PSMN4R1-60YLX	Nexperia
42	R1	RES, 47 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J470V	Panasonic
43	R2	RES, 0 R, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
44	R5	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic

Item	Ref Des	Description	Mfg Part Number	Mfg
45	R6	RES, 5.6 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J5R6V	Panasonic
46	R7	RES, 61.9 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF6192V	Panasonic
47	R8	RES, 3.32 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3321V	Panasonic
48	R9	RES, 10.0 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
49	R10	RES, 3.32 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3321V	Panasonic
50	R11	RES, 2.00 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
51	R12	Inrush Current Limiter, 2.2 Ohms ±20%, 7 A, 0.591" (15.00mm)	B57237S0229M051	EPCOS - TDK
52	R13	RES, 4.7 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
53	R14	RES, 10 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J103V	Panasonic
54	R16	RES, 2.00 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
55	R35	RES, 26.7 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2672V	Panasonic
56	R37	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
57	R39	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
58	R47	RES, 10 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
59	R48	RES, 10 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
60	R52	RES, 390 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J394V	Panasonic
61	R54	RES, 2.67 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2671V	Panasonic
62	R56	RES, 1.47 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1471V	Panasonic
63	R57	RES, 47 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J470V	Panasonic
64	R63	RES, 2 M, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ205V	Panasonic
65	R66	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
66	R72	RES, 22.1 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2212V	Panasonic
67	R75	RES, 5.6 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J5R6V	Panasonic
68	R76	RES, 4.7 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
69	R79	RES, 0 Ohms Jumper, Chip Resistor, 0805 (2012 Metric) Metal Element	5106	Keystone Electronics
70	R80	RES, 0 Ohms Jumper, Chip Resistor, 0805 (2012 Metric) Metal Element	5106	Keystone Electronics
71	R81	RES, 0 Ohms Jumper, Chip Resistor, 0805 (2012 Metric) Metal Element	5106	Keystone Electronics
72	T1	Bobbin, EF25, Horizontal, 10 pins (5.08 mm ls)	P-2550	Pin Shine
73	U1	InnoMux2-EP, IMX2378F, InSOP-T28D	IMX2378F-H415	Power Integrations
74	VDR1	470 V, 2.5 kA, Varistor, 1 Circuit, Through Hole Disc 10mm	MOV-10D471K	Bourns
75	VR2	TVS Diode, Unidirectional, 90V Reverse Standoff, 146V Clamp, 10.3A Ipp, Surface Mount SMC (DO-214AB)	SMCJ90A	TAIWAN SEMI
76	VR3	DIODE ZENER 47V 500MW SOD123	MMSZ5261BT1G	ON Semi

Table 2 – Bill of Materials.

7 Transformer (T1) Specification

7.1 Core Information

E 25/13/7 (EF 25)

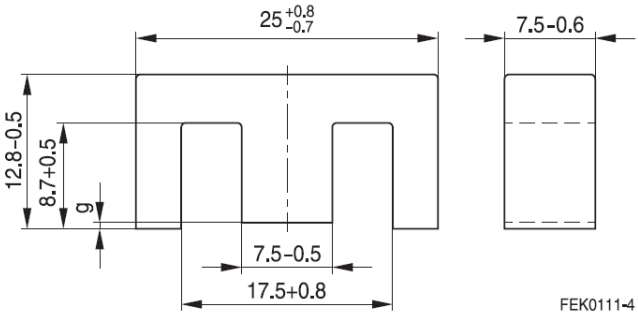
Core **B66317**

- To IEC 63093-8
- Delivery mode: single units

Magnetic characteristics (per set)

$\Sigma l/A$ = 1.1 mm^{-1}
l_e = 57.5 mm
A_e = 52.5 mm^2
A_{min} = 51.5 mm^2
V_e = 3020 mm^3

Approx. weight 16 g/set



Ungapped

Material	A_L value nH	μ_e	P_V W/set	Ordering code
N30	2900 +30/–20%	2530		B66317G0000X130
N27	1750 +30/–20%	1520	< 0.59 (200 mT, 25 kHz, 100 °C)	B66317G0000X127
N87	1850 +30/–20%	1620	< 1.60 (200 mT, 100 kHz, 100 °C)	B66317G0000X187
N97	1950 +30/–20%	1700	< 1.40 (200 mT, 100 kHz, 100 °C)	B66317G0000X197

Figure 6 – EF25 Core Information.

7.2 Bobbin Information

E 25/13/7 (EF 25)	
Accessories	**B66208**

Horizontal version (B66208B,B66208R)

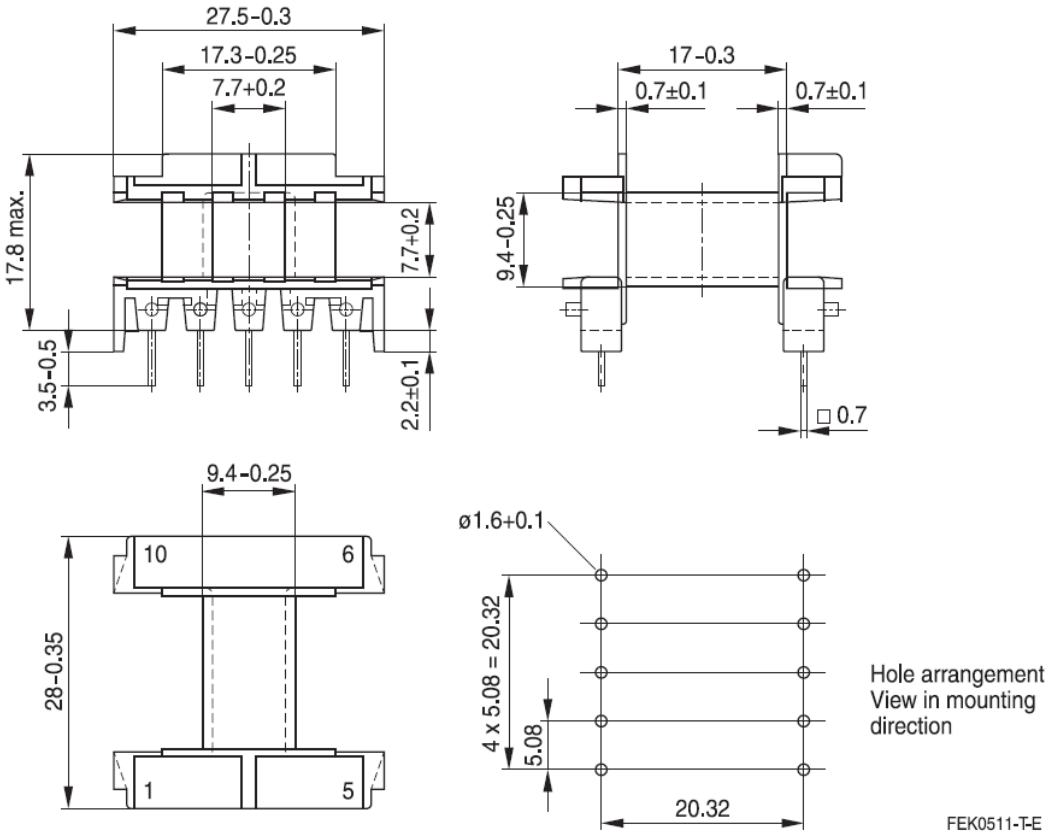


Figure 7 – EF25 Bobbin Information.

7.3 Electrical Winding Diagram

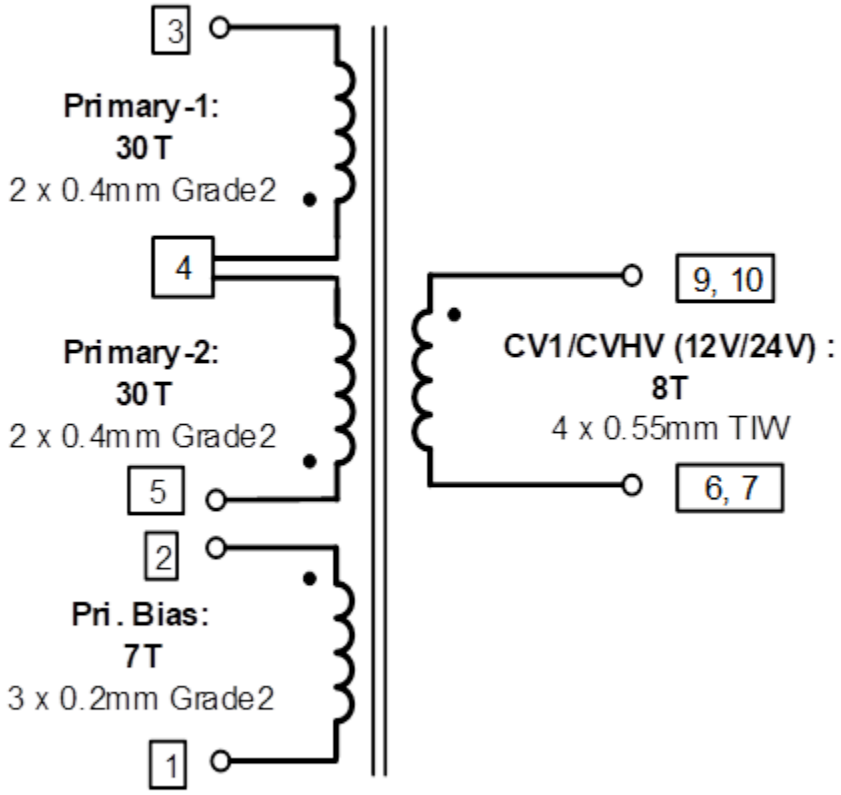


Figure 8 – Transformer Electrical Diagram.

7.4 Transformer Electrical Specification

Parameter	Condition	Spec.
Electrical strength	1 second, 60 Hz from pins 1-5 to 6-10.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 3 and 5, with all other windings open.	450 µH ±5%
Resonant Frequency	Between pin 3 and 5, other windings open.	1,100 kHz (Min.)
Primary Leakage Inductance	Between pin 3 and 5, with all secondary 6, 7, 8, 9 and 10 shorted.	10 µH (Max.)

Table 3 – Transformer Electrical Specifications.

7.5 Winding Stack Diagram

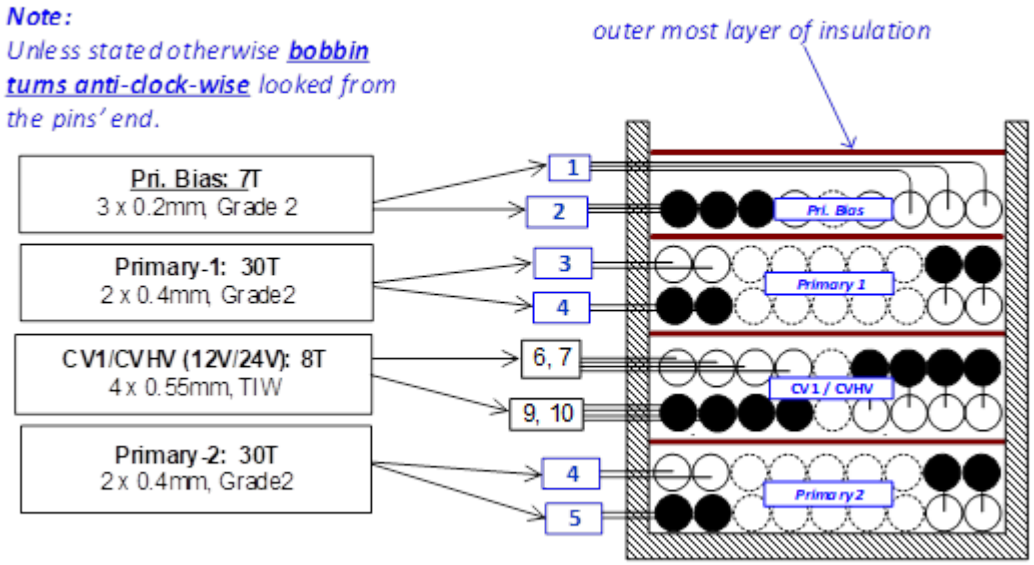


Figure 9 – Transformer Build Diagram.

7.6 List of Materials

Item	Description
[1]	Core: EF25.
[2]	Bobbin with Cover: EF25, 10pins (5/5).
[3]	Magnet Wire: 0.2 mm, Grade 2 ECW.
[4]	Magnet Wire: 0.4 mm, Grade 2 ECW.
[5]	TEX-E Wire: 0.55 mm, Triple Insulated.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 11.5 mm Wide.
[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 12 mm Wide.
[8]	Tape: 3M 1298 Polyester Film, 1 mil thick, 8.5 mm Wide.
[9]	Varnish: Recommended, E962-A (alternative: Dolph BC-359).
[10]	Glue: Recommended, H907 (alternative: Devcon 5-minute Epoxy).

Table 4 – Transformer Materials List.

8 Transformer Design Spreadsheet

InnoMux2_EP_031924; Rev.1.5; Copyright Power Integrations 2024	INPUT	INFO	OUTPUT	UNITS	DESCRIPTION
Power Supply Basic Parameters					RDK-1043, TX=EF25, revA4
OUTPUT CONFIGURATION	CV1_CVHV		CV1_CVHV		Output configuration
DC INPUT VOLTAGE	NO		NO		Yes = DC input; No = AC input
VAC MIN			90	V	Minimum AC input voltage
VAC NOM			115	V	Nominal AC input voltage
VAC MAX			265	V	Maximum AC input voltage
PO			50.04	W	Total output power @ nominal load condition
PIN			56.86	W	Input power @ nominal load condition
PTRF			53.79	W	Power processed by the transformer @ nominal load condition
FL			60	Hz	AC line frequency
VMAX			374.8	V	Maximum rectified input voltage
N			0.88		Estimated converter efficiency
Z			0.55		Secondary loss allocation
USE SR	Auto		YES		Use synchronous rectification
Input Section					
CIN	120		120	uF	Input capacitance
VMIN			100.8	V	Minimum DC input voltage calculated at VAC MIN and nominal power
VMIN AVG			115.5	V	Rectified average input voltage calculated at VAC MIN and nominal power
CV1 Specification					
OUTPUT TYPE			CV		Output control type
VOUT CV1	12.00		12.00	V	CV1 voltage
IOUT CV1	1.670		1.670	A	CV1 current
IOUT CV1 [PEAK POWER]	1.670		1.670	A	CV1 current for peak power requirement
CONNECTION TYPE CV1	Auto		SINGLE_WINDING		Winding connection type
CVHV Specification					
OUTPUT TYPE			CVHV		Output control type
VOUT CVHV	24.00		24.00	V	CVHV voltage
IOUT CVHV	1.250		1.250	A	CVHV current
IOUT CVHV [PEAK POWER]	1.250		1.250	A	CVHV current for peak power requirement
CONNECTION TYPE CVHV	SINGLE_WINDING		SINGLE_WINDING		Winding connection type
Other Design Conditions					
FS TARGET	100.00		100.00	kHz	Target maximum frequency at VMIN and peak power
KP TARGET	0.810		0.810		Minimum KP target at VMIN and peak power
BP MAX			0.33	T	Maximum allowed peak flux density at VMIN and peak power
MAXIMUM VOR	190.0		190.0	V	Reflected output voltage maximum limit
PI Device Variables					
DEVNAME	Auto		IMX2378F-H415		Device name
BVDSS			750	V	Drain to source breakdown voltage
PACKAGE			InSOP 28D		Device package
DEVICE_MODE	Standard		Standard		Device current limit mode
ILIMIT TOL	5.00		5.00	%	Current limit tolerance
ILIMIT MIN		Info	1.615	A	The specified ILIMIT MIN differs from the datasheet's value.

ILIMIT TYP	1.700	Info	1.700	A	Standard part: 1.6 A. Custom feature code necessary. Please contact local PI Sales Office for further details.
ILIMIT MAX		Info	1.785	A	The specified ILIMIT MAX differs from the datasheet's value.
FS LIMIT			110.00	kHz	Controller maximum switching frequency in steady-state condition
FS ABS MAX			145.00	kHz	Controller absolute maximum switching frequency in transitory condition
RDSON			0.78	Ohm	Drain to source on-time resistance
VDS			0.92	V	On-state drain to source voltage
Transformer Parameters					
Core and Bobbin Parameters					
CR TYPE	Custom		Custom		Core type (Compare transformer values against datasheet as it may differ per manufacturer.)
CR PN	EF25		EF25		Core part number
BB TYPE	EF25		EF25		Bobbin type
PRIMARY PINS	5		5		Number of primary pins in the bobbin
SECONDARY PINS	5		5		Number of secondary pins in the bobbin
BW	15.60		15.60	mm	Bobbin width
BFW	3.95		3.95	mm	Bobbin height
AE	52.5		52.5	mm^2	Core cross-sectional area
LE	57.5		57.5	mm	Core magnetic path length
VE	3020.0		3020.0	mm^3	Core volume
AL	1750		1750	nH/T^2	Ungapped core specific inductance
Inductance and Core Gap					
LP TOL			5.00	%	Primary inductance tolerance
LP MIN			427.7	uH	Minimum primary inductance
LP TYP			450.2	uH	Nominal primary inductance
LP MAX			472.7	uH	Maximum primary inductance
LG			0.490	mm	Estimated gap length
Construction Parameters					
NP	60		60		Primary winding total number of turns
NS SINGLE WINDING	8		8		Single winding output number of turns
BM			0.260	T	Maximum flux density in steady-state conditions (@FS MAX) and nominal power condition
BP			0.276	T	Peak flux density in transitory conditions (@FS ABS MAX)
VOR CV1			90.0	V	Primary reflected output voltage during CV1 output conduction
VOR CVHV			187.5	V	Primary reflected output voltage during CVHV output conduction
VOR MARG CVHV-CV1 ACTUAL			97.50	V	Minimum actual VOR margin between CVHV output and CV2 output reflected voltage
Operating Parameters Worst (Nominal Power)					
FS MAX		Warning	101	kHz	Calculated switching frequency exceeds target. Increase FS TARGET or relax hard engine bounds
FS MIN			77	kHz	Minimum operating switching frequency across all tolerance corners
KP		Warning	0.763		Calculated KP is below target. Decrease KP TARGET or relax hard engine bounds
VOR MAX			187.5	V	Actual maximum reflected voltage
DMAX			0.533		Maximum duty cycle
TON			6.828	us	Maximum controller ON time
TOFF			6.096	us	Minimum controller OFF time

VDRAIN PEAK			632	V	Estimated off-state drain to source peak voltage (considers 70 V spike)
VDRAIN PLATEAU			562	V	Off-state drain to source plateau voltage
VDS ON			1.00	V	On-state drain to source voltage
IAVG PRIMARY			0.54	A	Primary switch average current
IAVG DIODE BRIDGE			0.48	A	Average diode bridge current (DC input current)
Peak Currents (Nominal Power)					
PRIMARY IP			1.75	A	Peak primary current @ nominal load condition
CV1 OUTPUT IP			8.63	A	CV1 output peak current @ nominal load condition
CVHV OUTPUT IP			13.14	A	CVHV output peak current @ nominal load condition
RMS Currents (Nominal Power)					
INPUT IRMS			1.17	A	Input RMS current @ nominal load condition
PRIMARY IRMS			0.79	A	Primary winding RMS current @ nominal load condition
CV1 OUTPUT IRMS			3.35	A	CV1 RMS current @ nominal load condition
CV1 OUTPUT WINDING IRMS			5.00	A	CV1 winding RMS current @ nominal load condition
CVHV OUTPUT IRMS			3.72	A	CVHV RMS current @ nominal load condition
CVHV OUTPUT WINDING IRMS			3.72	A	CVHV winding RMS current @ nominal load condition
Ripple Currents (Nominal Power)					
INPUT I RIPPLE RMS			1.07	A	Input capacitor RMS ripple current @ nominal load condition
CV1 I RIPPLE RMS			2.91	A	CV1 output RMS ripple current @ nominal load condition
CVHV I RIPPLE RMS			3.50	A	CVHV output RMS ripple current @ nominal load condition
Bias Parameters					
Primary Bias					
NB	7		7	turns	Primary bias winding turns
V BIAS MIN			9.8	V	Minimum primary bias voltage
V BIAS MAX			21.2	V	Maximum primary bias voltage
VFD BIAS PRI			0.70	V	Primary bias rectifier voltage forward drop
PIV BIAS PRI			64.9	V	Primary bias rectifier peak inverse voltage
R BIAS			12.12	kOhms	Bias resistor
IBPP MIN			0.40	mA	Bias current at V BIAS MIN
IBPP MAX			1.33	mA	Bias current at V BIAS MAX
USE OUTPUT OVP	NO		NO		Use output overvoltage protection on primary bias
Component Ratings					
Secondary Switches					
CVHV RECTIFIER	Diode		Diode		CVHV rectifier type
SR PRV			62.0	V	Synchronous rectifier maximum peak reverse voltage
SR IRMS			5.00	A	Synchronous rectifier RMS current
SF CV1			24.0	V	CV1 selection FET maximum peak reverse voltage
OBD CVHV			24.0	V	CVHV blocking diode maximum peak reverse voltage
OBD VF CVHV			1.00	V	CVHV output blocking diode forward voltage drop

9 Common Mode Choke (L4) Specification

9.1 Electrical Diagram

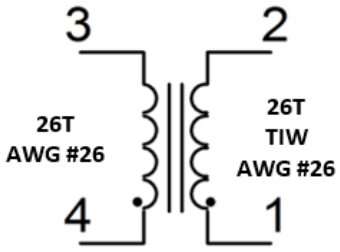


Figure 10 - Inductor Electrical Diagram.

9.2 Electrical Specifications

Parameter	Test Condition	Specification
Inductance	Pins 1-2 or pins 4 to 3 measured at 1 $V_{PK-PK,}$ 100 kHz frequency with all other windings open.	7 mH ±10%
Leakage Inductance	Pins 1-2, with 4-3 shorted.	0.42 µH
Core effective Inductance		9000 nH/N^2(min)

9.3 List of Materials

Item	Description
[1]	Toroid Core: 30-00398-00
[2]	TIW Wire: #26 AWG.
[3]	Magnet Wire: #26 AWG

9.4 Illustration

Figure 11 - Common Mode Choke L4.

Note: Wind 26 turns of item 2 and 3 in bifilar wound from the list of materials as shown in Figure 11

10 Performance

10.1 Full Load Efficiency vs. Line

Full load efficiency vs. line voltage is shown in figure 12. NTC resistor (R12) was shorted out for all efficiency testing. Tests were performed at room temperature under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CV1 = 12 V @ 1.67 A (100%)
- CVHV = 24 V @ 1.25 A (100%)

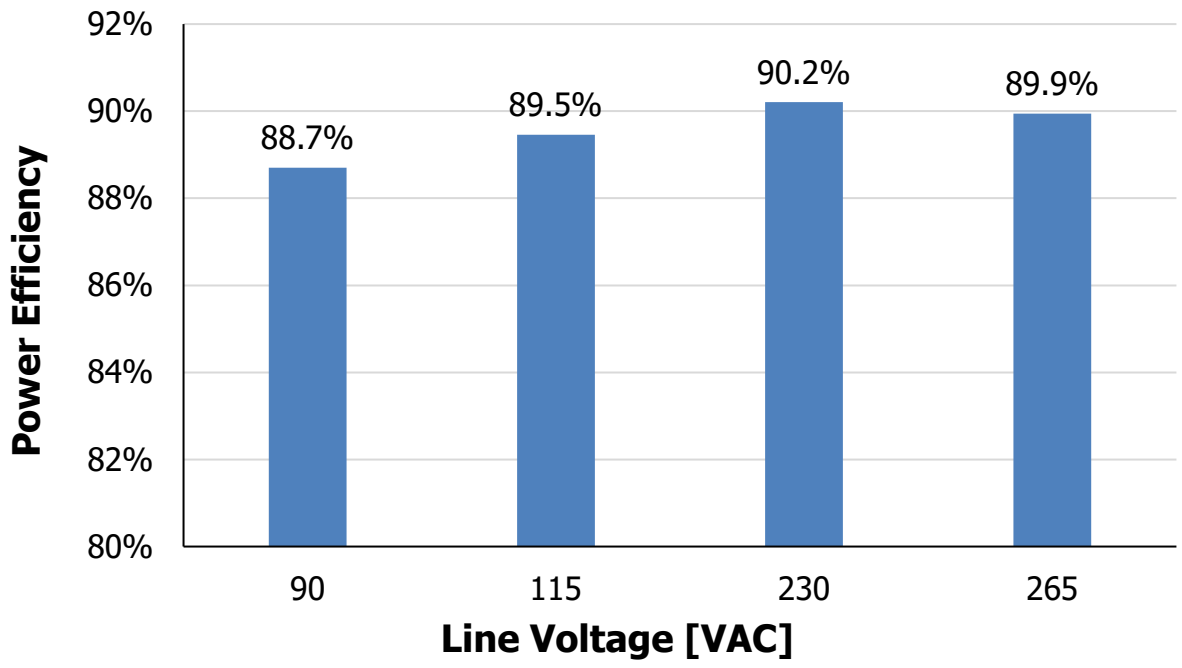


Figure 12 – Full Load Efficiency vs. Line Voltage at Room Temperature.

10.2 Efficiency vs. Load

The efficiency vs. load measurements are shown in figure 13. NTC resistor (R12) was shorted out for all efficiency testing. Tests were performed at room temperature under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CV1 = 12 V @ 0 A to 1.67 A (0 to 100%) with 5% load increments
- CVHV = 24 V @ 0 A to 1.25 A (0 to 100%) with 5% load increments

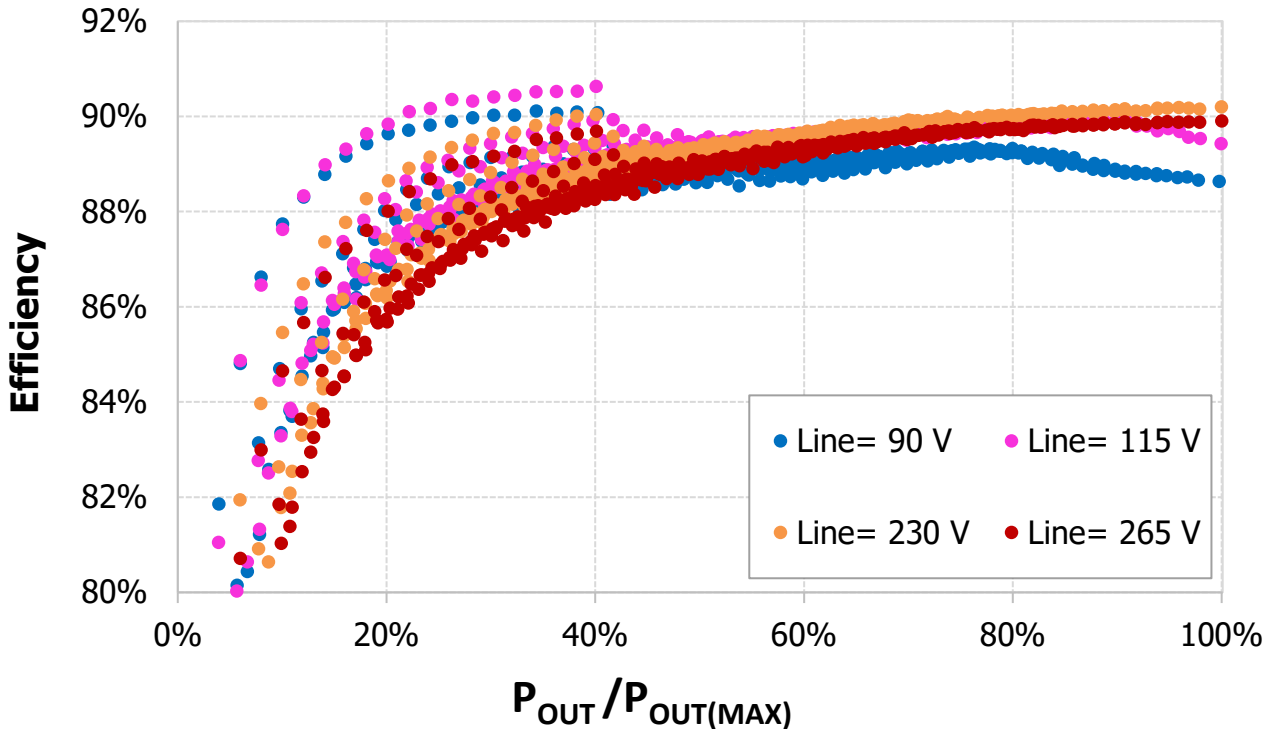


Figure 13 – Efficiency vs. Load for All Line Inputs, Room Temperature.

10.3 Output Load Regulation

The CV1 output voltage regulation error vs. load are shown in figure 14. Tests were performed at room temperature under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CV1 = 12 V @ 0 A to 1.67 A (0 to 100%) with 5% load increments
- CVHV = 24 V @ 0 A and 1.25 A (0 and 100%) with 5% load increments

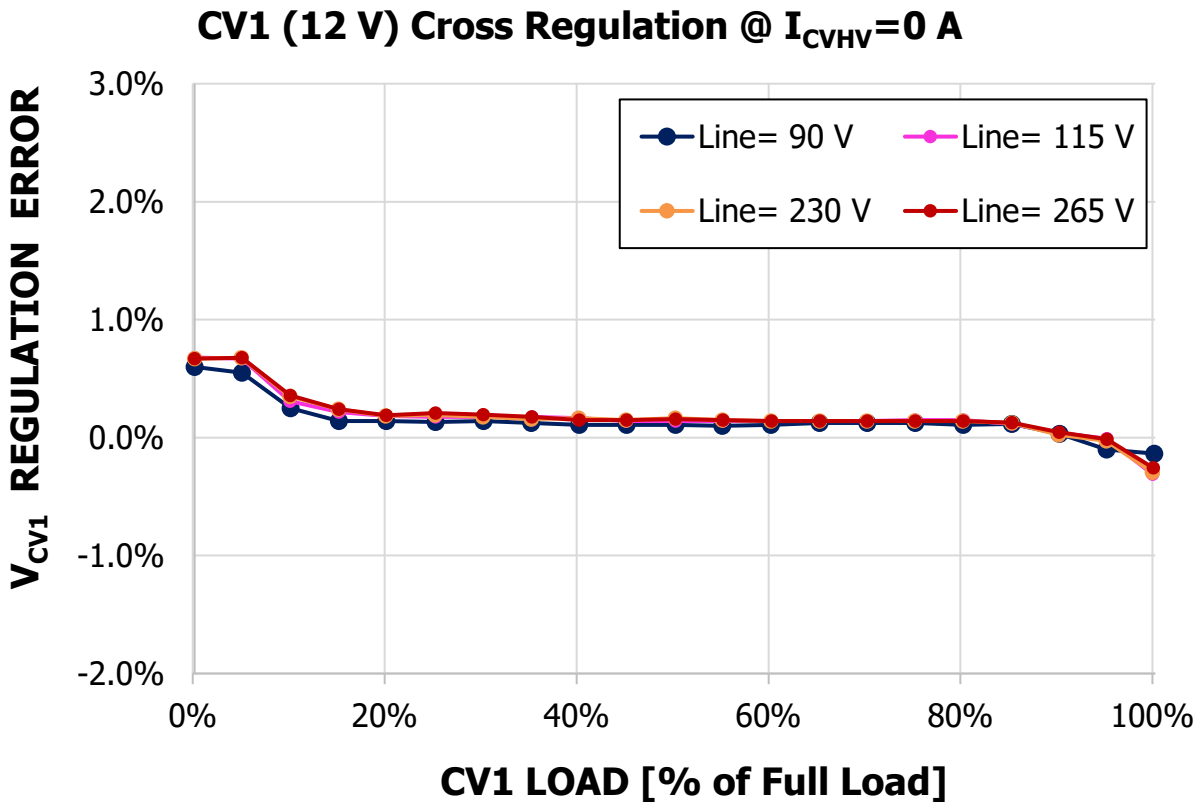


Figure 14 – CV1 Output Voltage Regulation Error vs. Load at 0A.

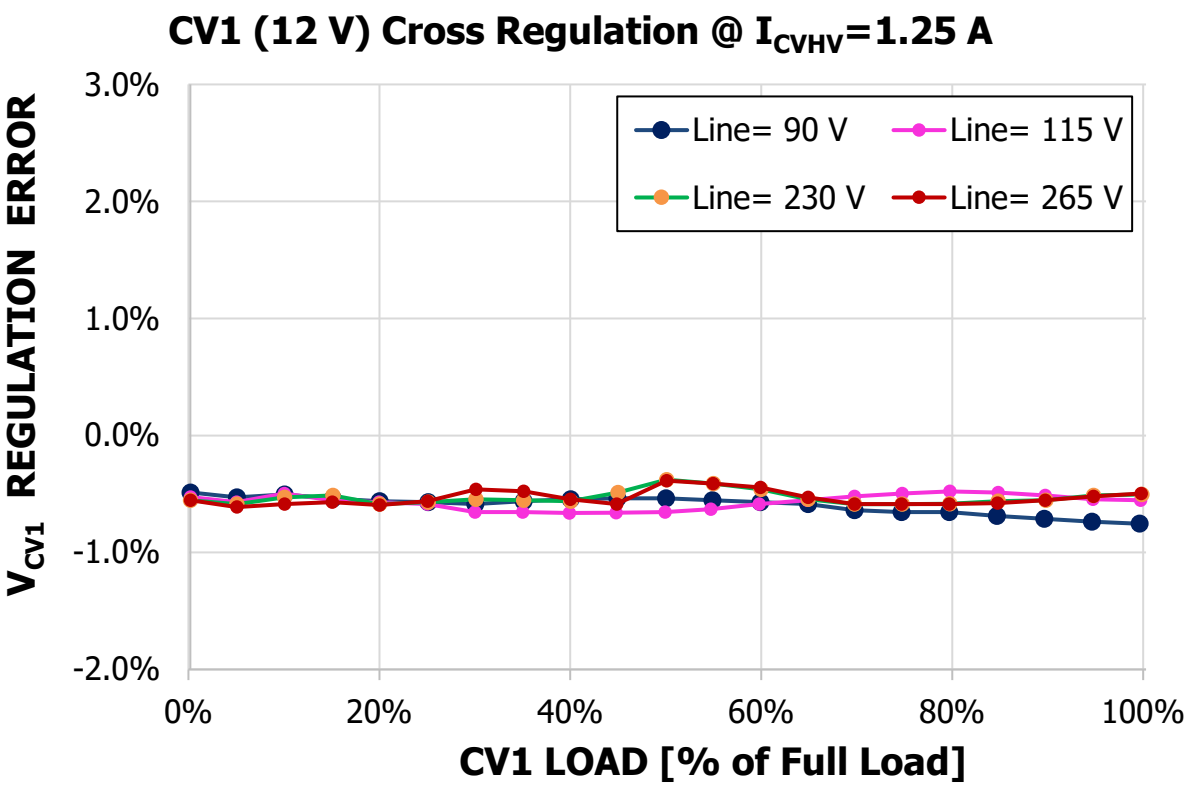


Figure 15 – CV1 Output Voltage Regulation Error vs. Load at 1.25A.

The CVHV output voltage regulation error vs. load is shown in figures 16 and 17. Tests were performed at room temperature under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CVHV = 24 V @ 0 A to 1.25 A (0 to 100%) with 5% load increments
- CV1 = 12 V @ 0 A and 1.67 A (0 and 100%) with 5% load increments

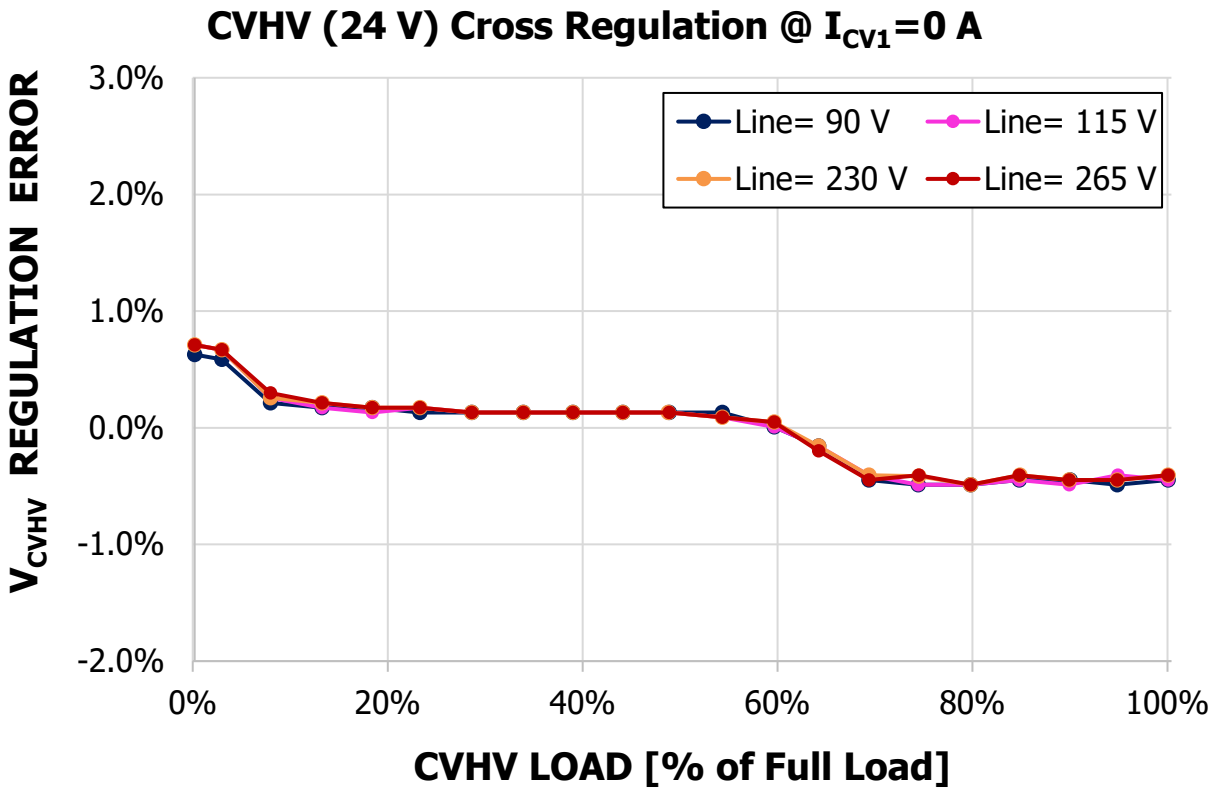


Figure 16 – CVHV Output Voltage Regulation Error vs. Load at 0A.

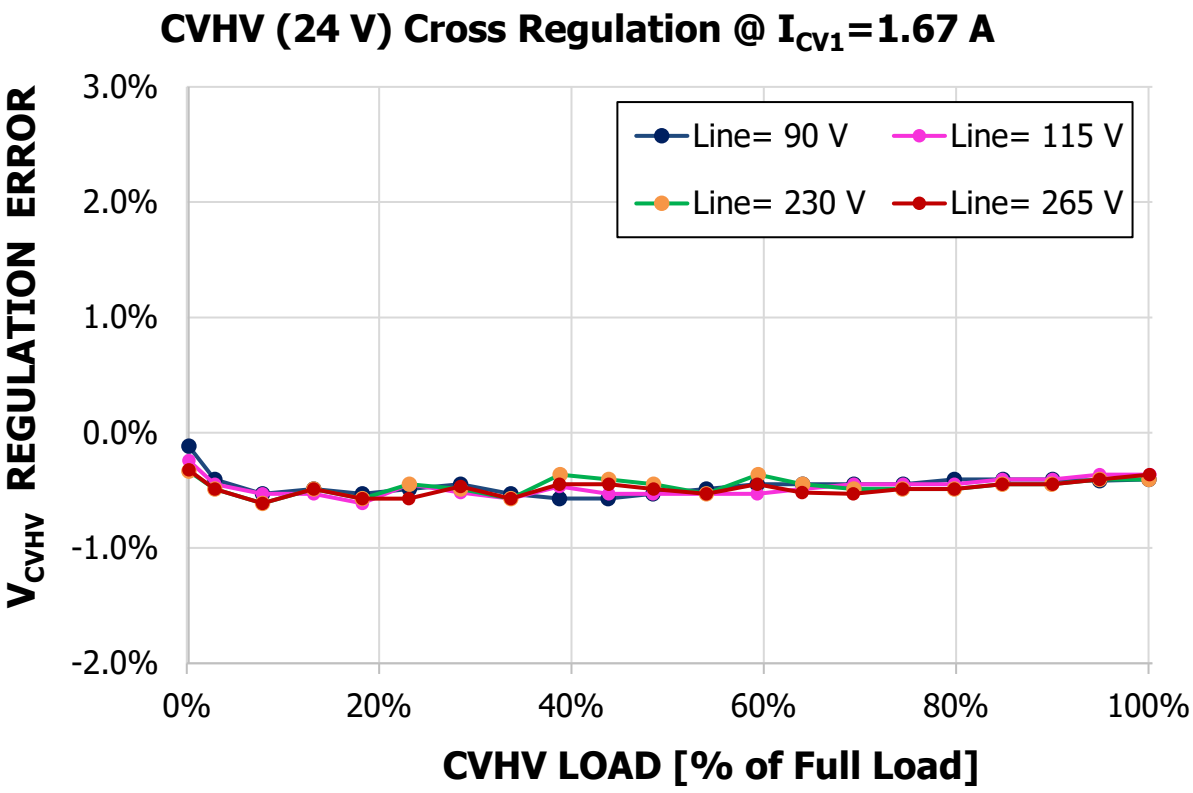


Figure 17 – CVHV Output Voltage Regulation Error vs. Load at 1.67A.

10.4 No-Load and Standby Input Power (I_{CVHV} = 0 A)

The output power vs. input power in standby condition is shown in figure 18. Tests were performed at room temperature under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CVHV output = 0 A or 0 mW
- CV1 output = 0 mW to 350 mW

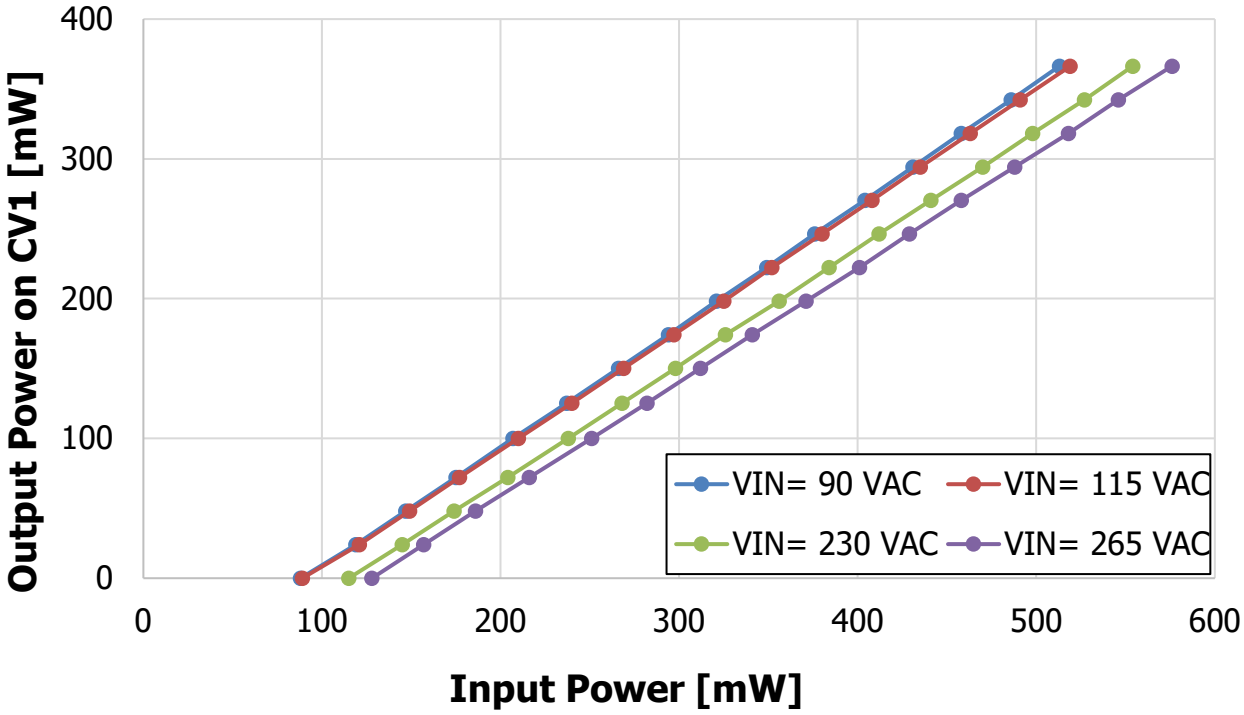


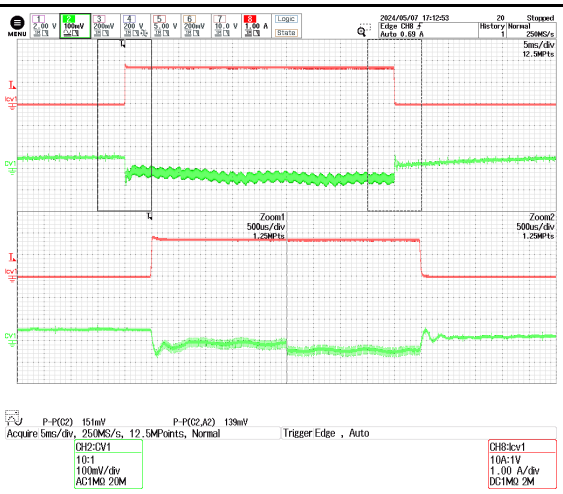
Figure 18 – Standby Input Power vs. Output Power (CV1).

10.5 Load Transient Response

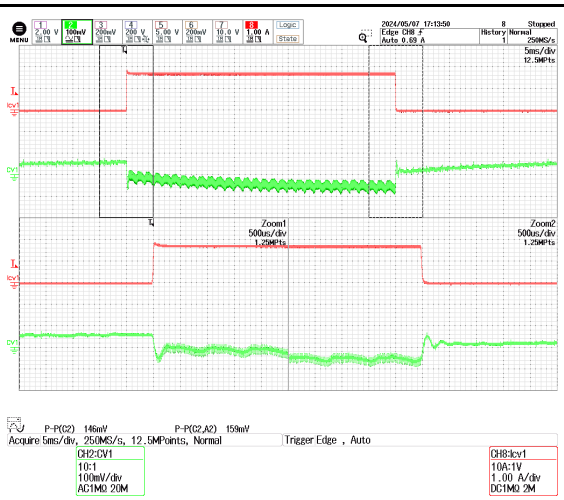
10.5.1 CV1 Step Load Transient

A load transient test was performed under the following conditions:

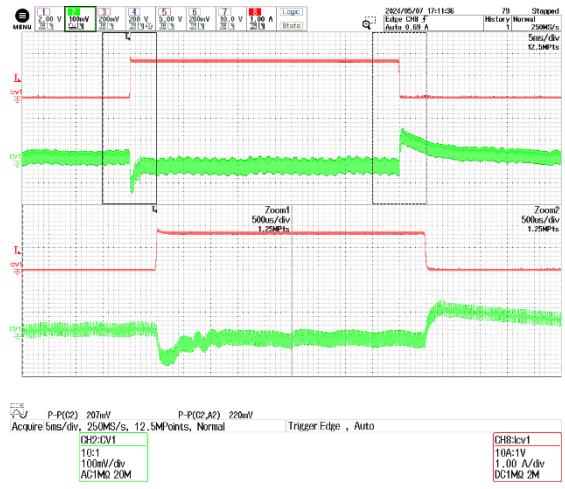
- Line voltage: 90 VAC and 265 VAC
- CV1 load step 0 A -->1.67 A -->0A, slew rate = 120 mA/µsec, load on time = 100 msec, load off time = 100 ms
- CVHV = 0 A and 1.25 A



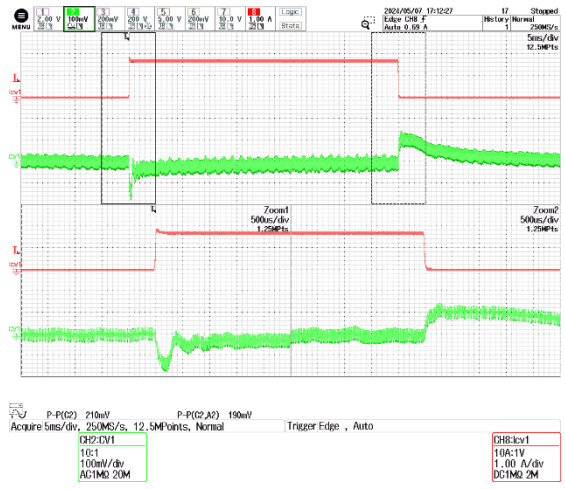
90VAC, ICV1 = 0 A -> 1.67 A (100%) -> 0 A.
ICVHV = 0 A.
Overshoot: 139 mV (1.2%).
Undershoot: -151 mV (-1.3%).



265 VAC, ICV1 = 0 A -> 1.67 A (100%) -> 0 A.
ICVHV = 0 A.
Overshoot: 159 mV (1.3%).
Undershoot: -146 mV (-1.2%).



90 VAC, ICV1 = 0 A -> 1.67 A (100%) -> 0 A.
ICVHV = 1.25 A.
Overshoot: 220 mV (1.8%).
Undershoot: -207 mV (-1.7%).



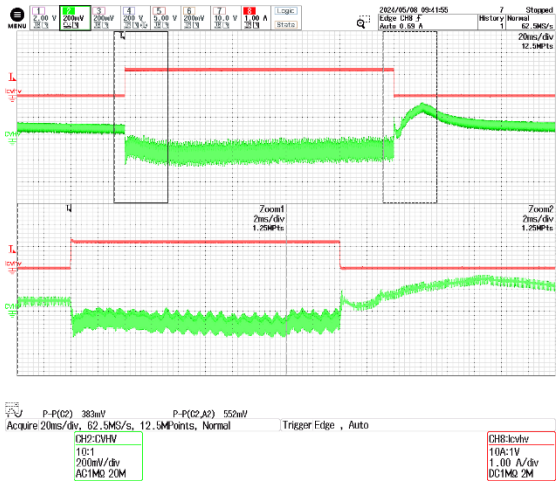
265 VAC, ICV1 = 0 A -> 1.67 A (100%) -> 0 A.
ICVHV = 1.25 A.
Overshoot: 190 mV (1.6%).
Undershoot: -210 mV (-1.8%).

Figure 19 – CV1 (12 V) Load Transient.

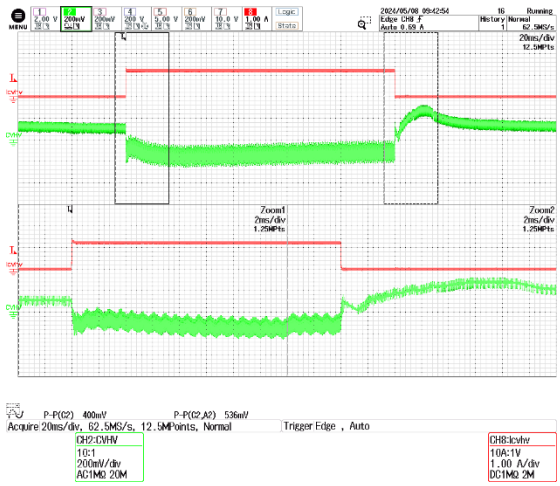
10.5.2 CVHV Step Load Transient

A load transient test was performed under the following conditions:

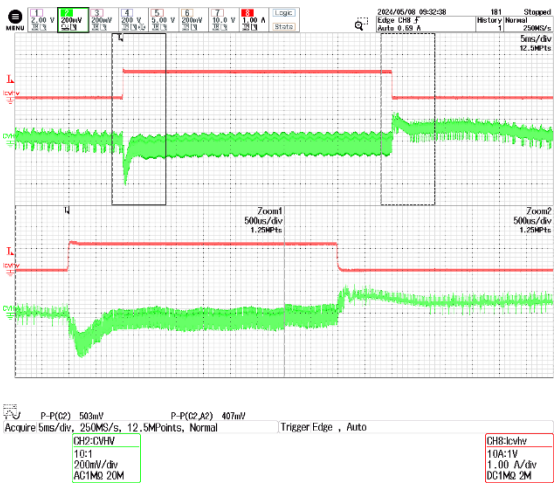
- Line input voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CV1 = 0 A and 1.67 A
- CVHV load step 63 mA-->1.25 A-->63 mA
- Slew rate = 120 mA/µsec
- Load on time = 100 msec, Load off time =100 msec



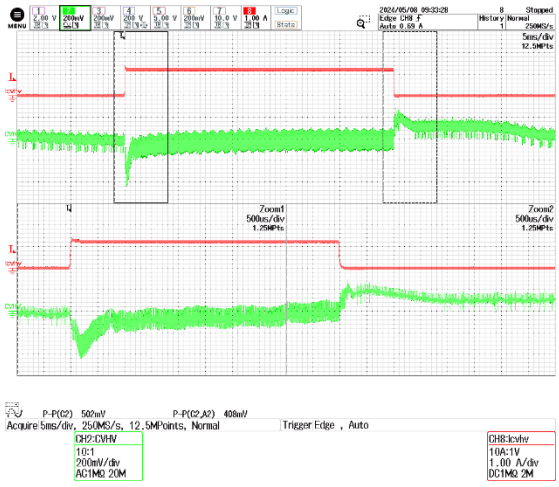
90 VAC, ICVHV = 63 mA -> 1.25 A -> 63 mA.
ICV1 = 0 A.
Overshoot: 552 mV (2.3%).
Undershoot: -383 mV (-1.6%).



265 VAC, ICVHV = 63 mA -> 1.25 A -> 63 mA.
ICV1 = 0 A.
Overshoot: 536 mV (2.2%).
Undershoot: -400 mV (-1.7%).



90 VAC, ICVHV = 63 mA -> 1.25 A -> 63 mA.
ICV1 = 1.67 A.
Overshoot: 407 mV (1.7%).
Undershoot: -503 mV (-2.1%).



265 VAC, ICVHV = 63 mA -> 1.25 A -> 63 mA.
ICV1 = 1.67 A.
Overshoot: 408 mV (1.7%).
Undershoot: -502 mV (-2.1%).

Figure 20 – CVHV (24 V) Load Transient.

10.6 Switching Waveforms

10.6.1 Primary Switch Maximum Voltage

The primary switch (U1) maximum-voltage test was performed under the following conditions:

- Line input voltage 265 VAC
- Full load on both outputs:
  - CV1 = 12 V @ 1.67 A
  - CVHV = 24 V @ 1.25 A
- 100 MHz bandwidth selected on the oscilloscope

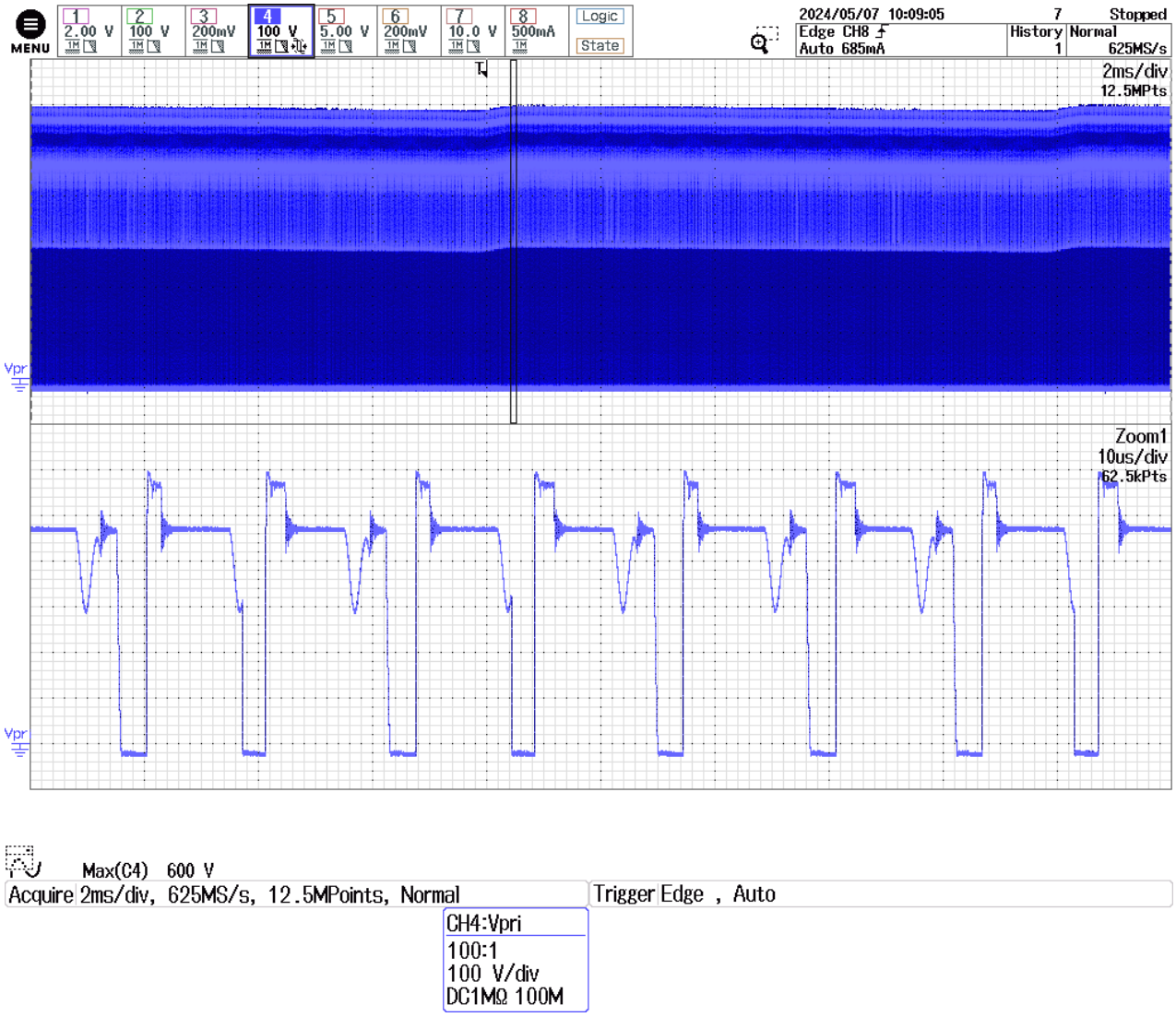


Figure 21 – Primary Switch Worst Case Peak Voltage, V_{PRI_PK} = 600 V.

10.6.2 SR FET Voltage Waveform

The SR FET (Q1) maximum voltage test was performed under the following conditions:

- 265 VAC input line voltage
- CV1 (12 V) load step from 0 A to 1.67 A
- CVHV (24 V) load at 1.25 A
- 100 MHz bandwidth selected on the oscilloscope

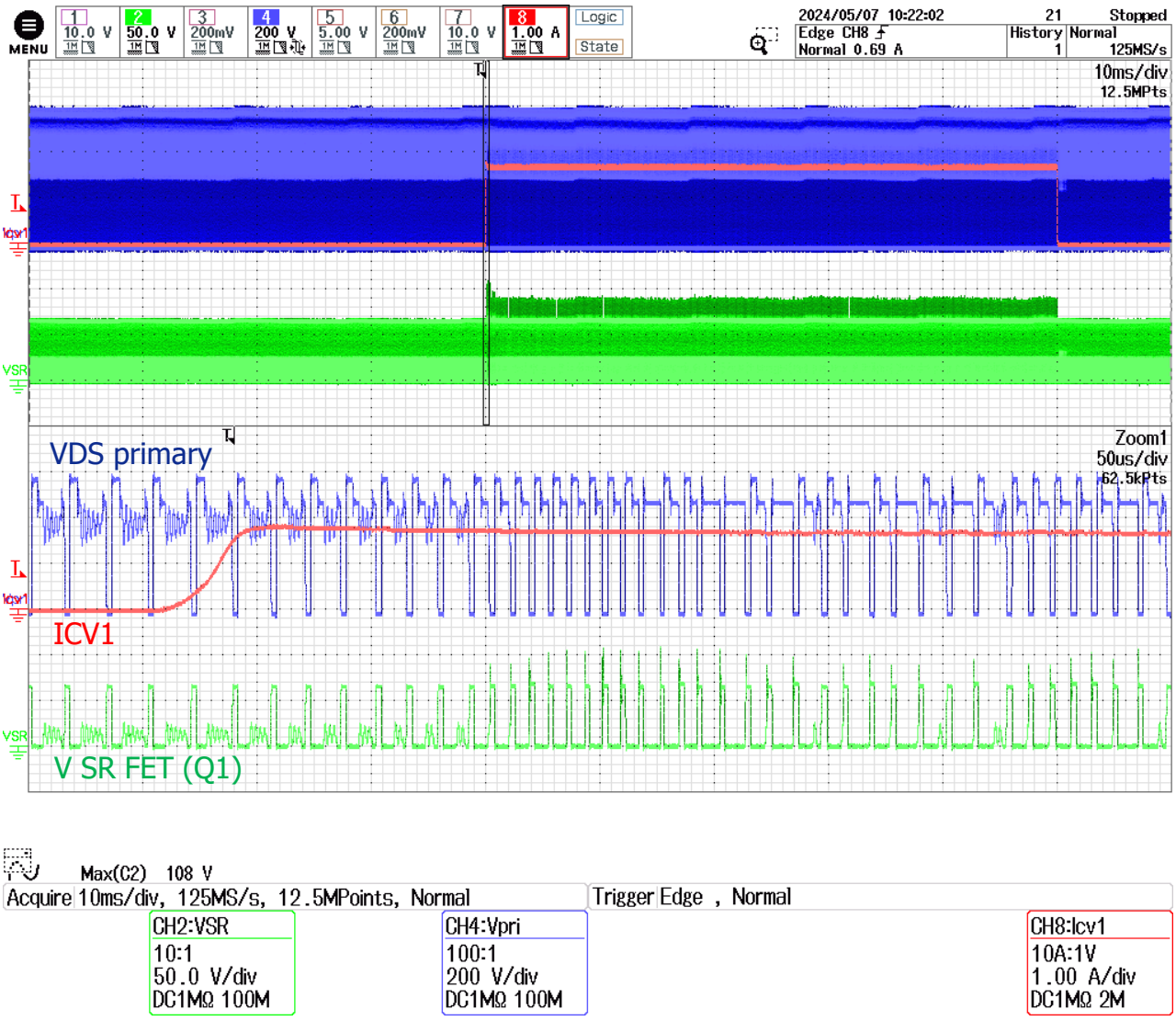


Figure 22 – SR FET Worst Case Peak Voltage, V_{SR_PK} = 108 V.

10.6.3 Selection FET Voltage Waveform

The Selection FET (Q2) maximum voltage test was performed under the following conditions:

- 265 VAC input line voltage
- Startup with full load on both outputs:
  - CV1 = 12 V @ 1.67 A
  - CVHV = 24 V @ 1.25 A
- 100 MHz bandwidth selected on the oscilloscope

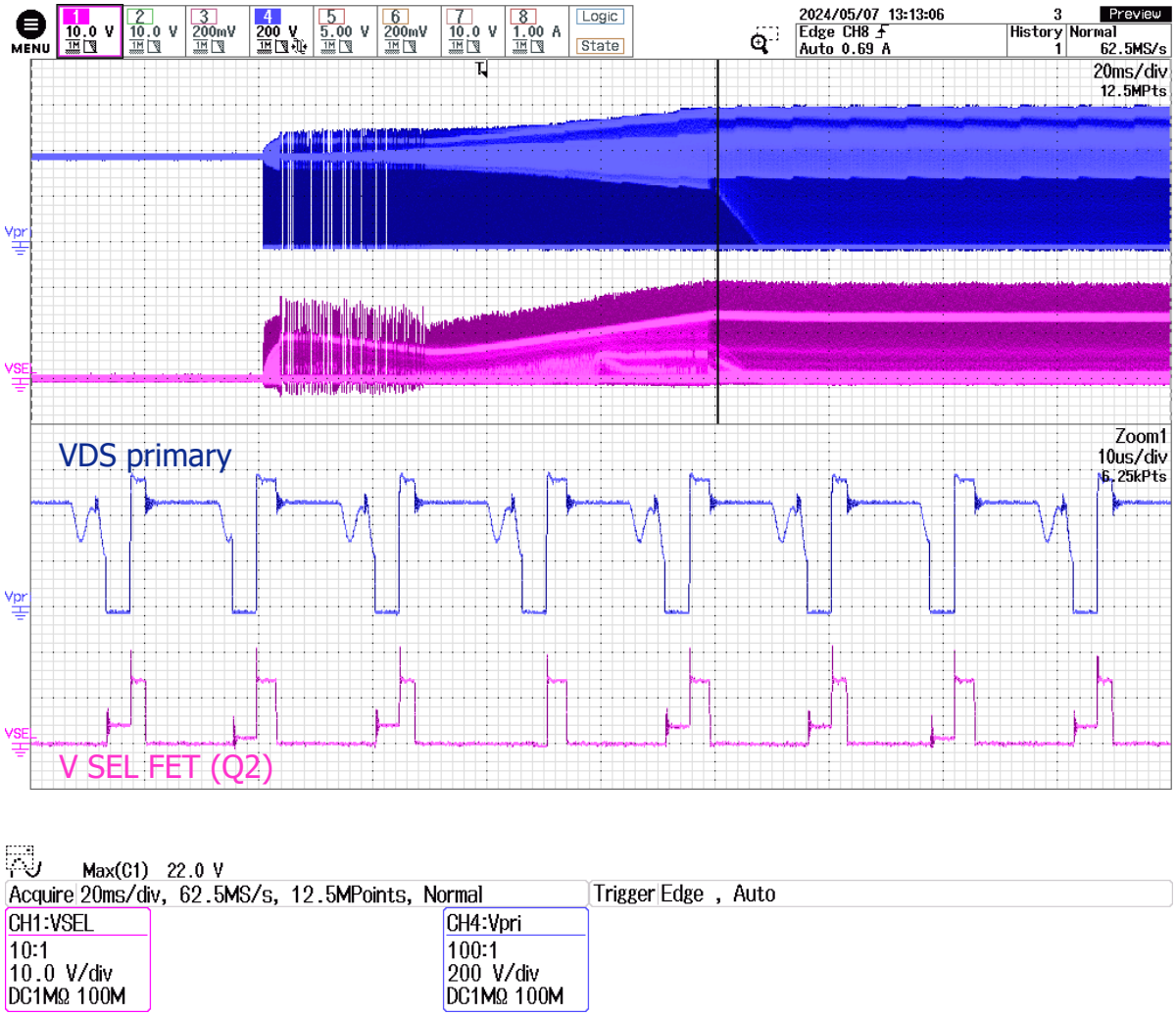


Figure 23 – Selection FET Worst Case Peak Voltage, V_{SEL_PK} = 22.0 V.

10.6.4 CVHV Diode Reverse Voltage Waveform

The CVHV Diode (D3) maximum reverse voltage test was performed under the following conditions:

- 265 VAC input line voltage
- Start-up with full load on both outputs:
  - CV1 = 12 V @ 1.67 A
  - CVHV = 24 V @ 1.25 A
- 100 MHz bandwidth selected on the oscilloscope

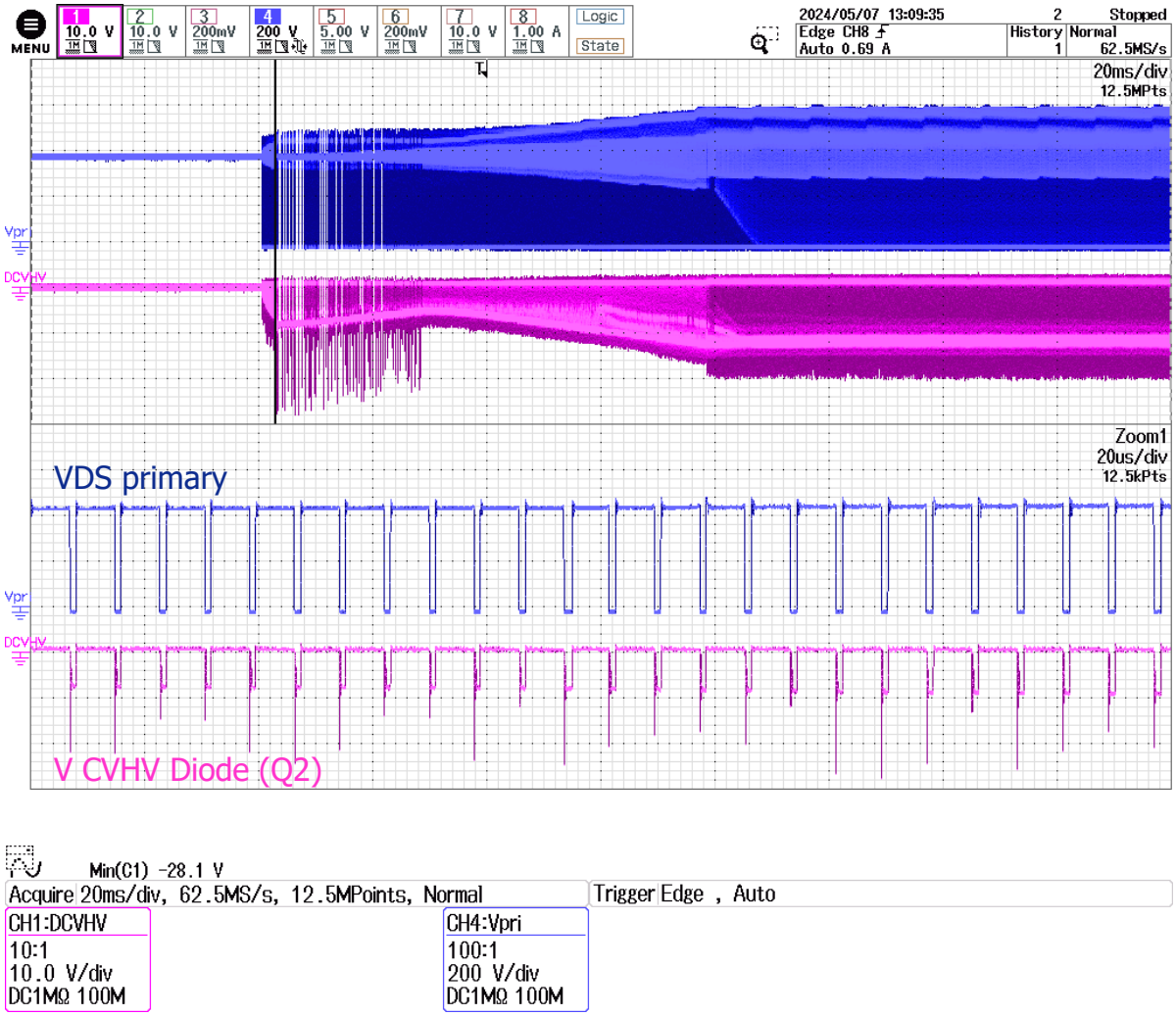


Figure 24 – CVHV Diode Worst Case Reverse Voltage, V_{D3_PK} = 30 V.

10.6.5 BPP Rectifier Diode Reverse Voltage Waveform

A BPP rectifier diode (D1) maximum reverse voltage test was performed under the following conditions:

- 265 VAC input line voltage
- Start-up with full load on both outputs:
  - CV1 = 12 V @ 1.67 A
  - CVHV = 24 V @ 1.25 A
- 100 MHz bandwidth selected on the oscilloscope

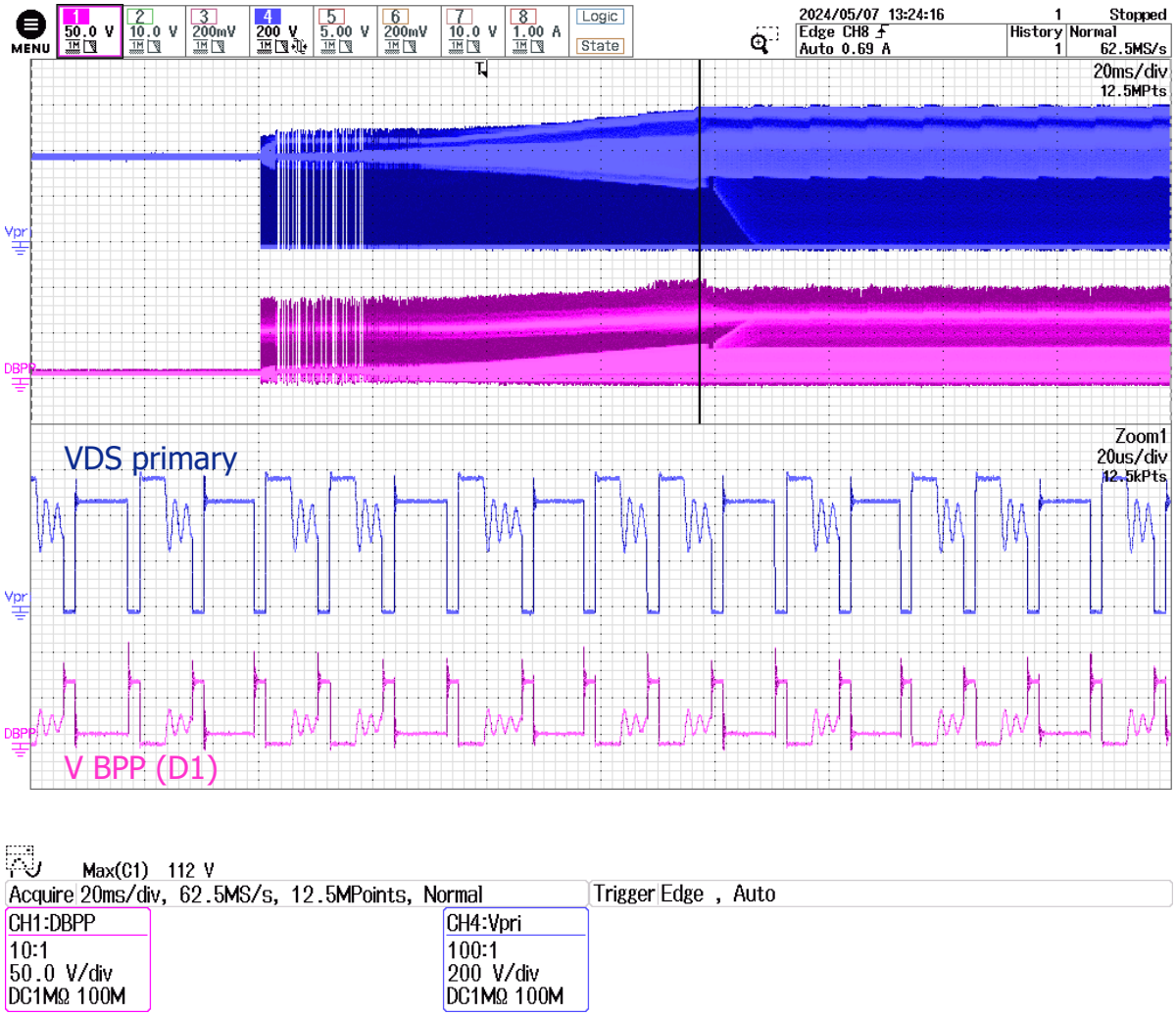


Figure 25 – BPP Rectifier Diode Worst Case Reverse Voltage, V_{D1_PK} = 112 V.

10.6.6 Primary Switching Frequency

The primary switching frequency of the converter varies depending on the line and load conditions. Frequency was measured under maximum load at minimum line input (90 VAC). Maximum switching frequency occurs at the minimum bulk voltage with a maximum instantaneous frequency of 90.3 kHz. Under the same conditions over a mains cycle, the average switching frequency is 88.6 kHz.

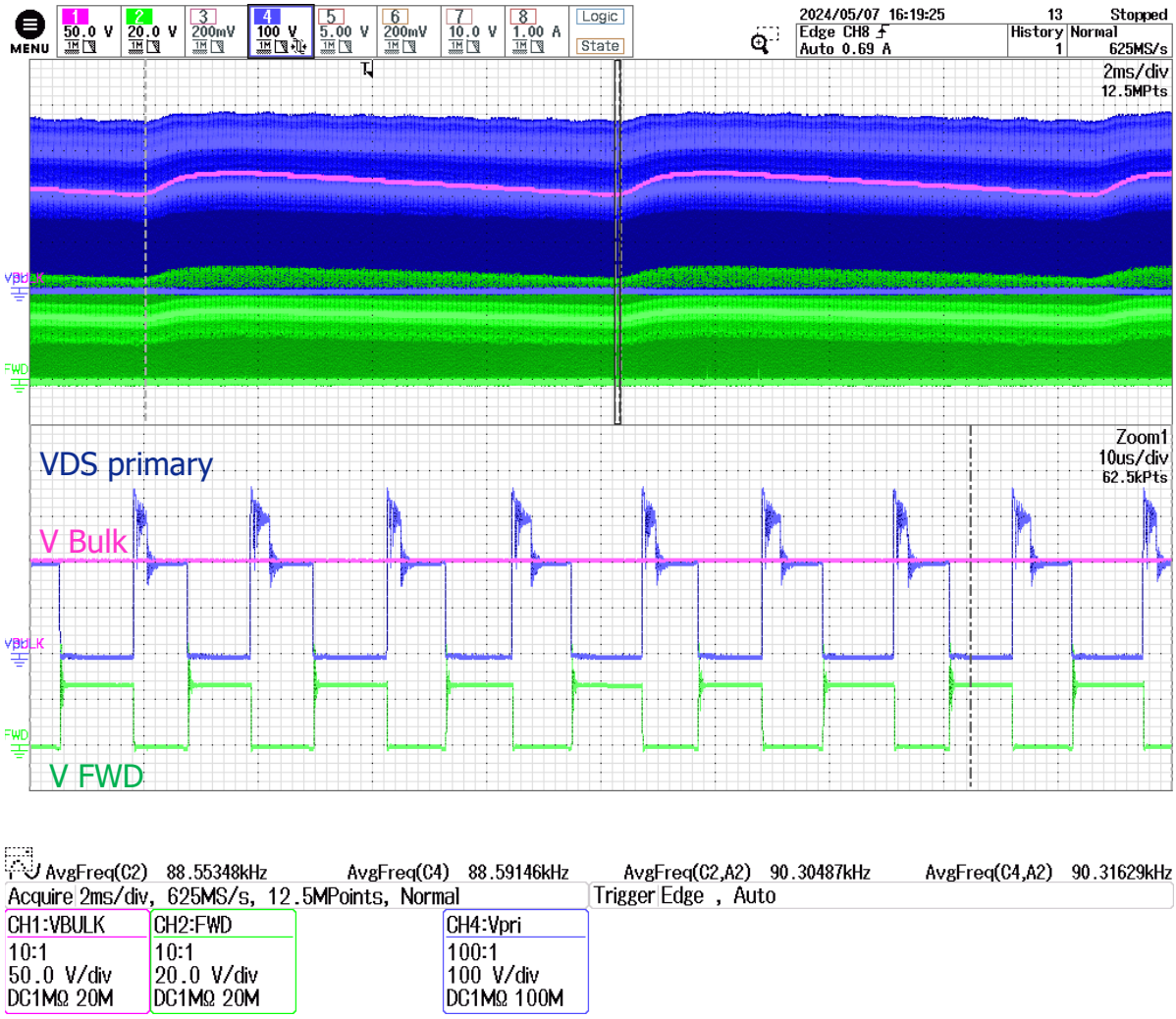


Figure 26 – Primary Switching Frequency at 90 VAC Input Line Voltage.

10.6.7 Maximum Voltage Stress

The voltage waveforms on each key component, i.e. MOSFETs & diodes, were checked to confirm that the maximum voltage stress was below the respective ratings. The maximum voltage stress can occur under different combinations of input mains voltages and output loads, as well as during startup up or during transient conditions. Most applications require 10% ~ 20% margin between maximum voltage stress and component absolute maximum ratings. Tables shows the voltage stress on each key-component under worst-case conditions.

Component	Part Number	Component Rating [V_{pk}]	Measured Maximum Voltage Stress	
			[V_{pk}]	[%]
InnoMux2 (U1)	IMX2378F-H415	750	600	**80%**
SR FET (Q1)	BSC0302LS	120	108.0	**90%**
Selection FET (Q2)	PSMN4R1-60YL	60	22.0	**37%**
CVHV Diode (D3)	V20PW45	45	28.1	**62%**
BPP Diode (D1)	US1G	400	112	**28%**

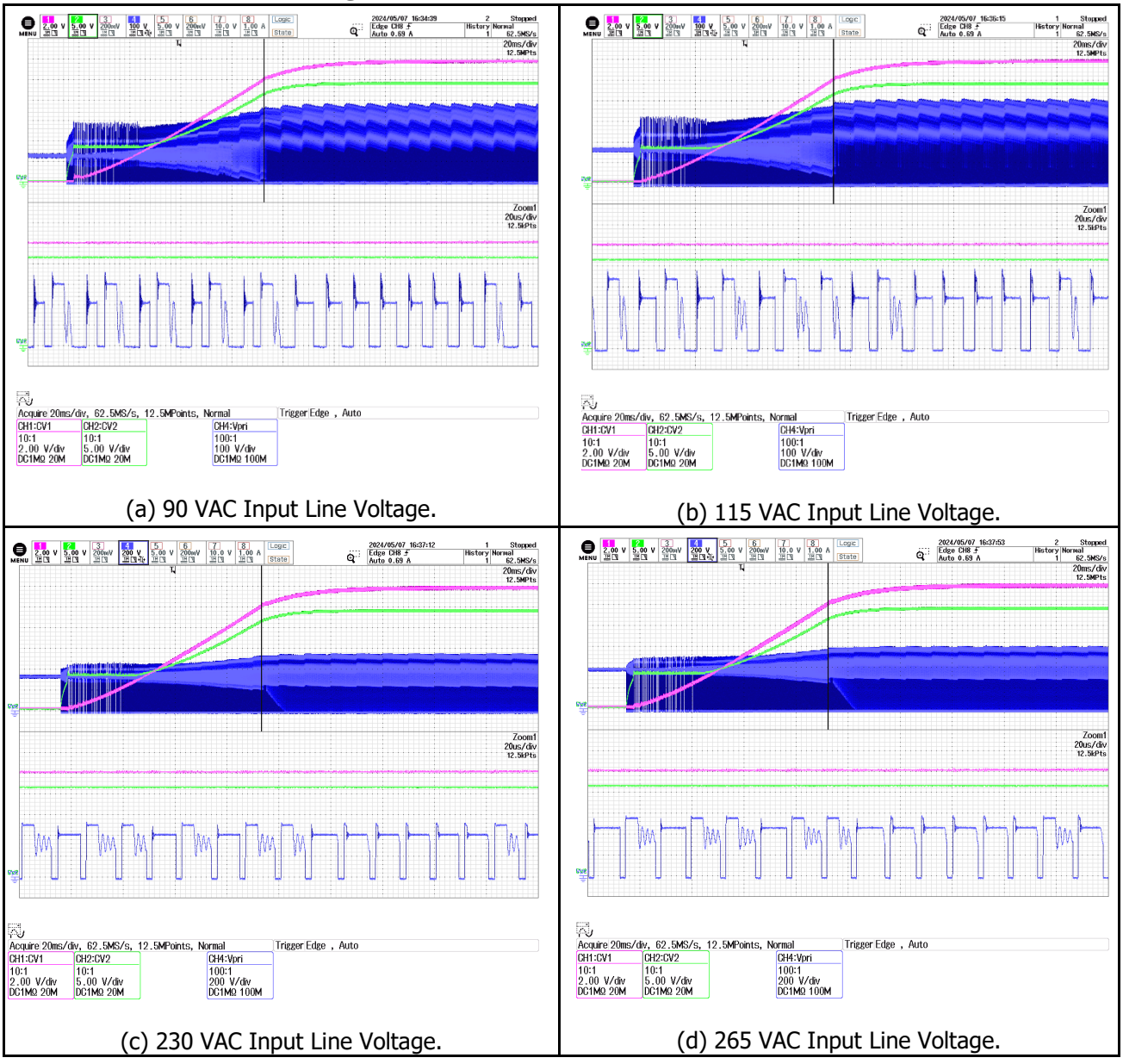
Table 5 – Measured Maximum Voltages on key components.

10.7 Start-Up

10.7.1 Full Load Start-up

A full load start-up test was performed under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- Full load on both outputs:
  - CV1 = 12 V @ 1.67 A
  - CVHV = 24 V @ 1.25 A



(a) 90 VAC Input Line Voltage.

(b) 115 VAC Input Line Voltage.

(c) 230 VAC Input Line Voltage.

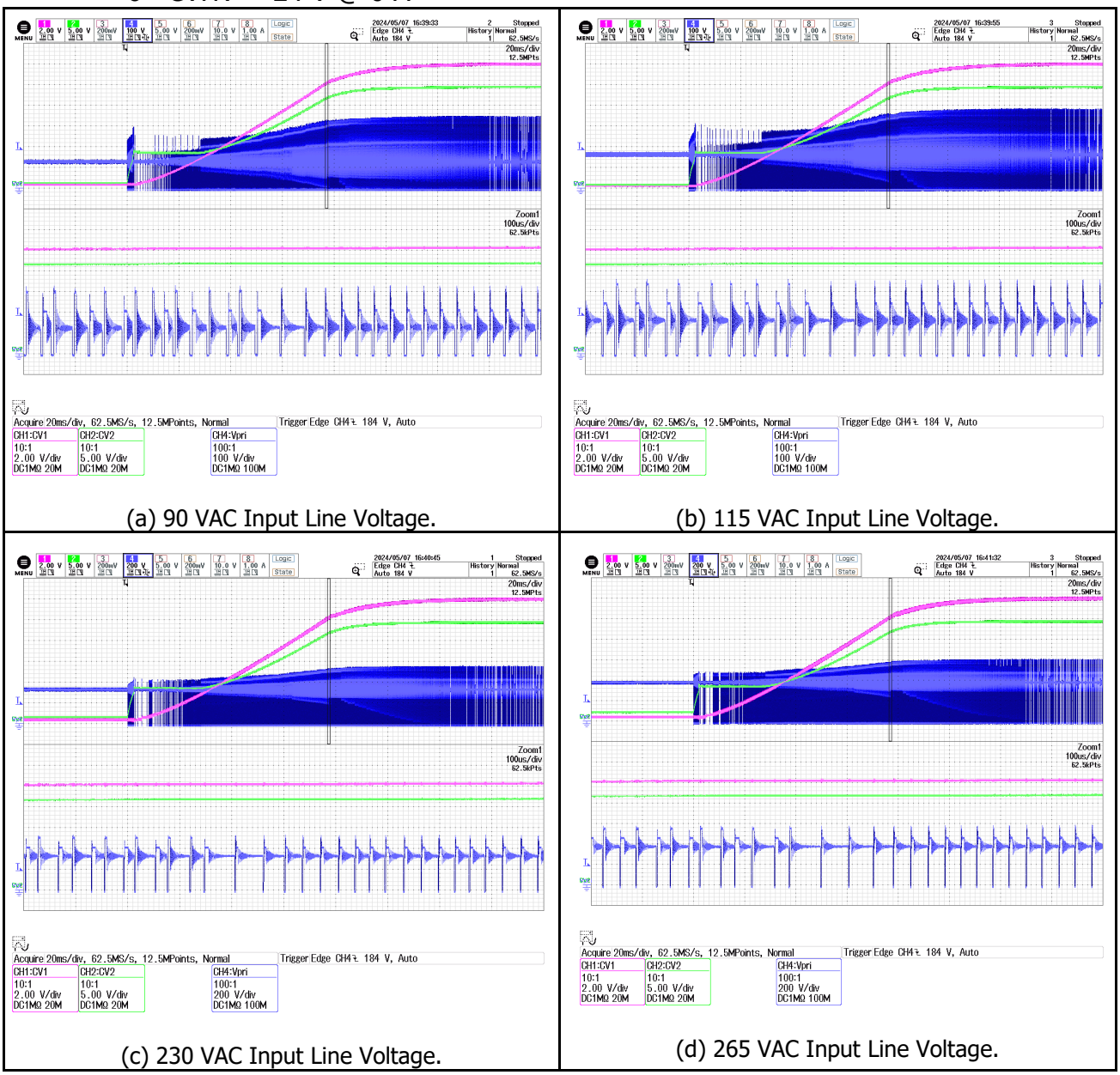
(d) 265 VAC Input Line Voltage.

Figure 27 – Full Load Start-up.

10.7.2 No-Load Start-up

A no load start-up test was performed under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- No load on either output:
  - CV1 = 12 V @ 0 A
  - CVHV = 24 V @ 0 A



(a) 90 VAC Input Line Voltage.

(b) 115 VAC Input Line Voltage.

(c) 230 VAC Input Line Voltage.

(d) 265 VAC Input Line Voltage.

Figure 28 – No-load Start-up.

10.7.3 Start-up Under Single Fault Conditions

The start-up into a fault condition was tested using the following conditions:

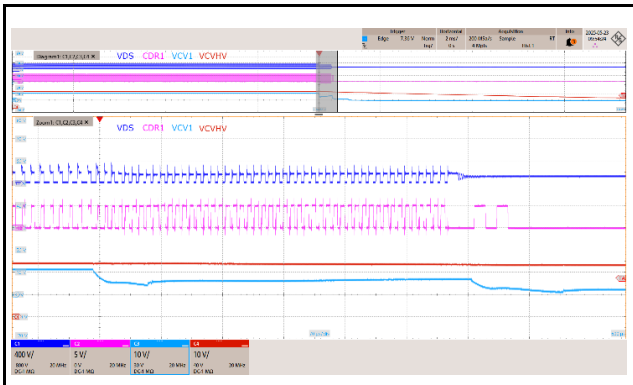
- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- Full load on both outputs:
  - CV1 = 12 V @ 1.67 A
  - CVHV = 24 V @ 1.25 A

The fault conditions tested are:

- Short circuit to GND on CV1 and CVHV

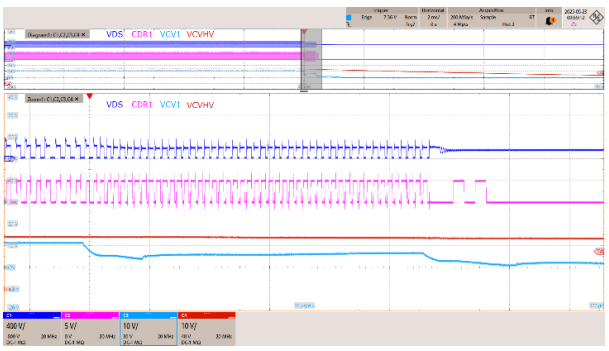
In both cases, the power supply was able to prevent damage to any component. Line fuse F1 remained intact. When the fault was applied, the power supply entered auto-restart. The unit was able to resume normal operation after the fault condition was removed.

10.7.3.1 Startup with CV1 shorted to GND



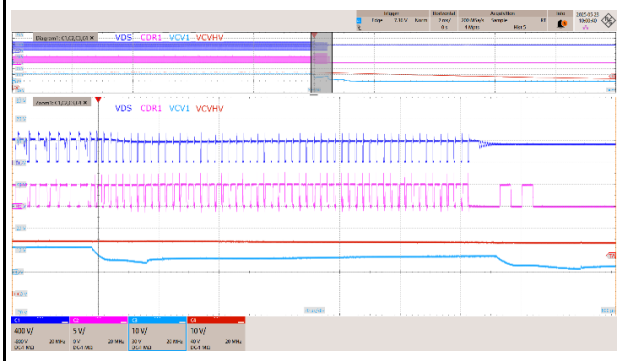
CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div
Time Division: 2 ms/div
Zoom: 50 us/div

(a) 90 VAC Input Line Voltage



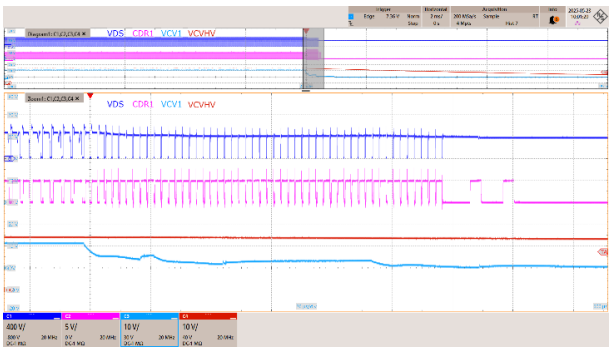
CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div
Time Division: 2 ms/div
Zoom: 50 us/div

(b) 115 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div
Time Division: 2 ms/div
Zoom: 50 us/div

(c) 230 VAC Input Line Voltage

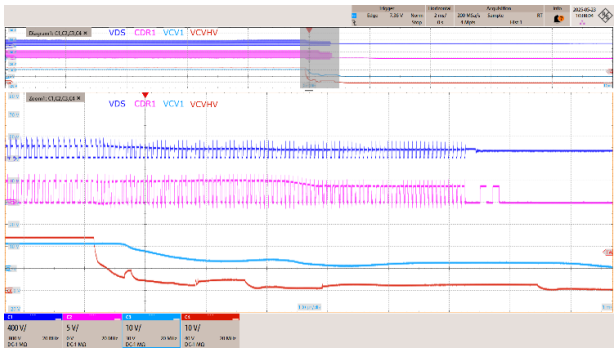


CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div
Time Division: 2 ms/div
Zoom: 50 us/div

(d) 265 VAC Input Line Voltage

Figure 29 - Start-up with CV1 Shorted to GND at 90, 115, 230 and 265 VAC.

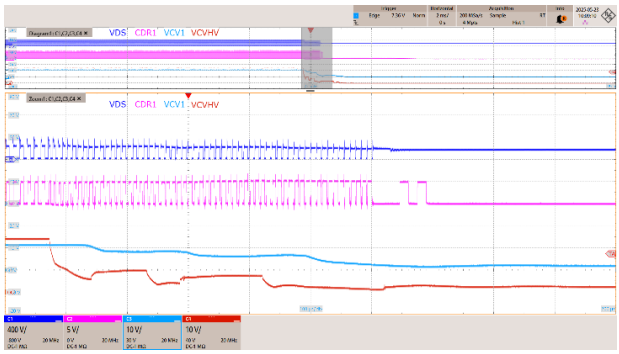
10.7.3.2 Startup with CVHV shorted to GND



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

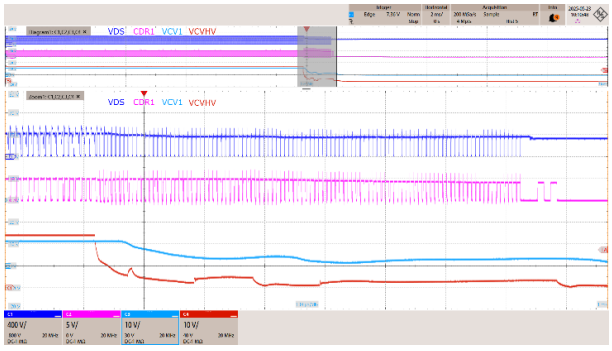
(a) 90 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

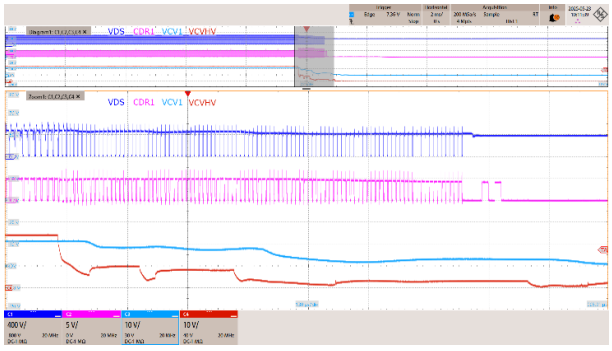
(b) 115 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

(c) 230 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

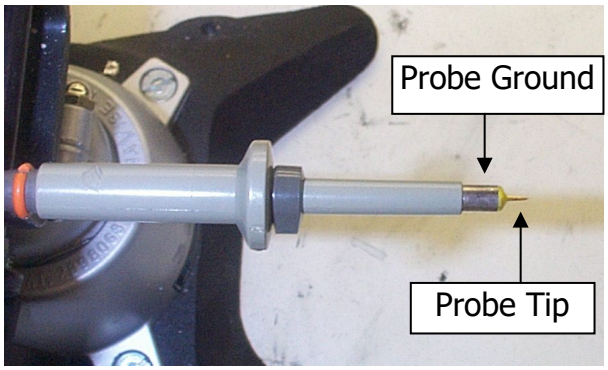
(d) 265 VAC Input Line Voltage

Figure 30 - Start-up with CVHV Shorted to GND at 90, 115, 230 and 265 VAC.

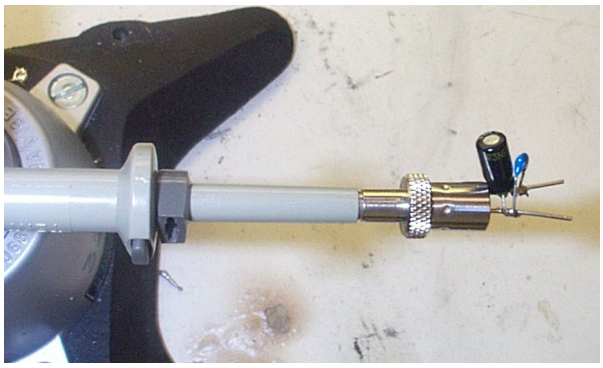
10.8 Output Ripple Measurements

10.8.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to reduce noise pick-up. The probe adapter is shown in the figures below. It includes a coaxial cable with two parallel capacitors connected to the points of measurement. The capacitors include a 0.1 μF / 100 V ceramic type and a 10 μF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.



End Cap and Ground Lead Removed.



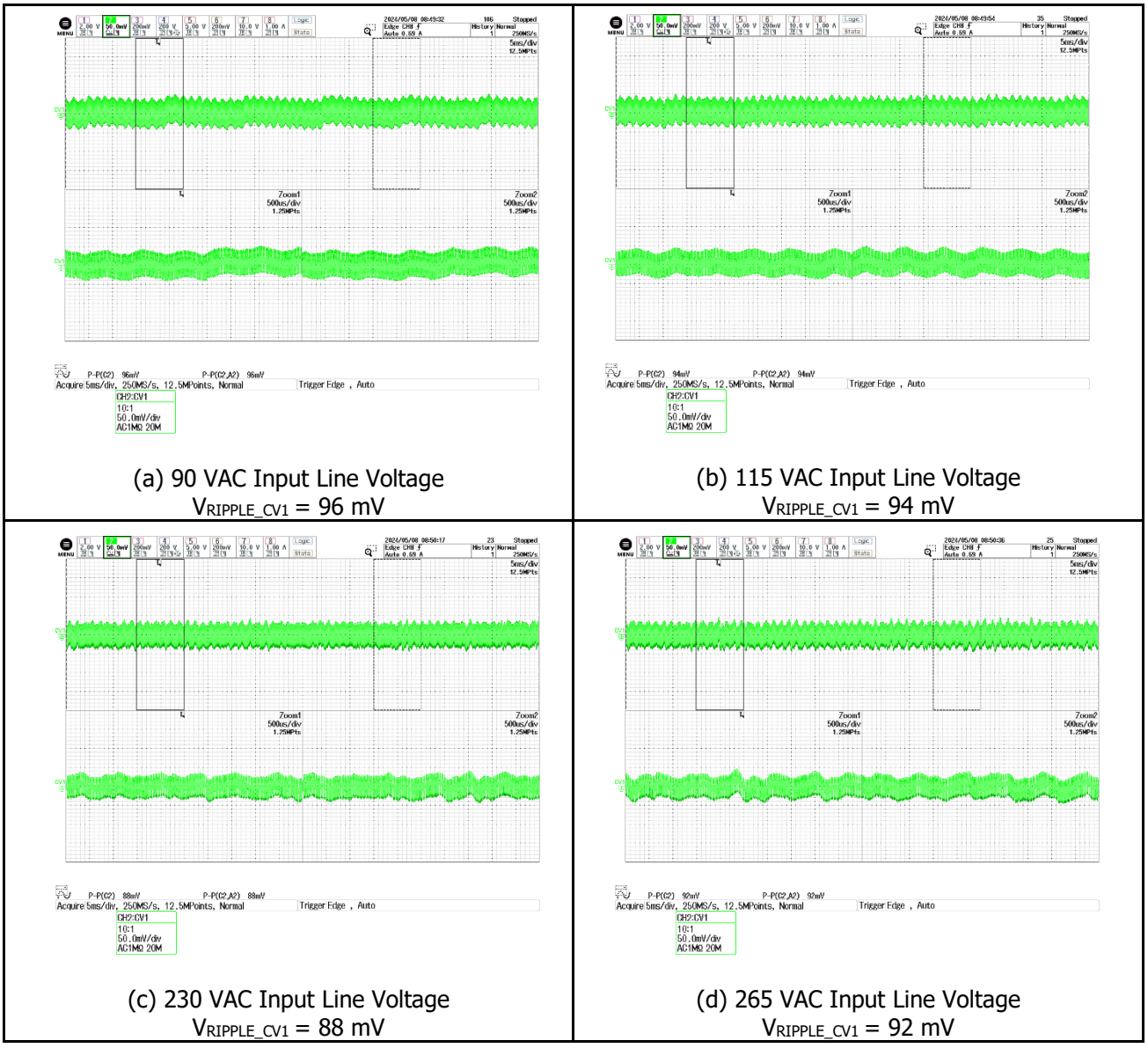
Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

Figure 31 – Oscilloscope Probe Prepared for Ripple Measurement.

10.8.2 CV1 and CVHV Output Ripple

The CV1 and CVHV output ripple are tested under the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CV1 = 12 V @ 1.67 A
- CVHV = 24 V @ 1.25 A
- 20 MHz bandwidth selected on the oscilloscope



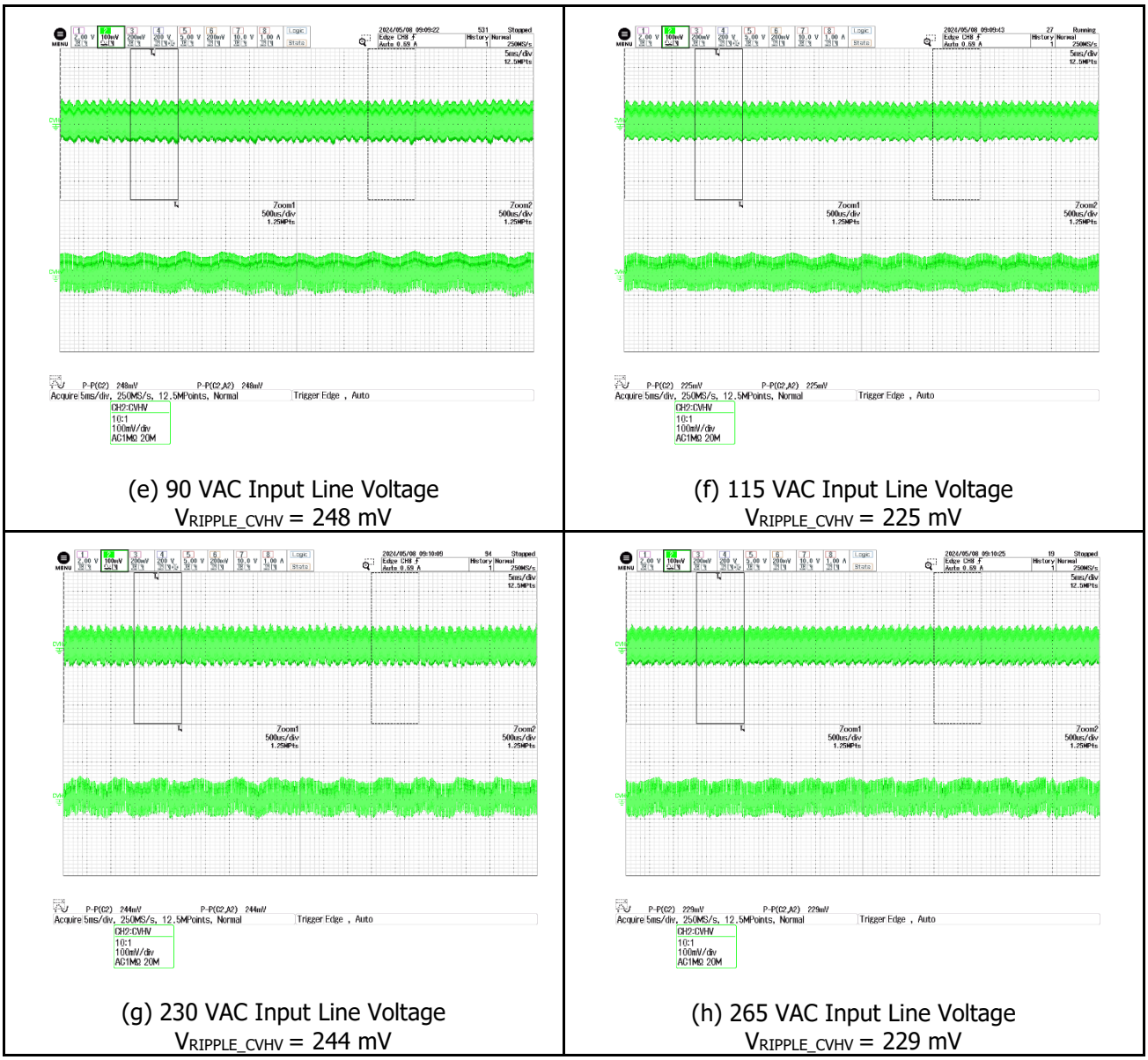
(a) 90 VAC Input Line Voltage
V_{RIPPLE_CV1} = 96 mV

(b) 115 VAC Input Line Voltage
V_{RIPPLE_CV1} = 94 mV

(c) 230 VAC Input Line Voltage
V_{RIPPLE_CV1} = 88 mV

(d) 265 VAC Input Line Voltage
V_{RIPPLE_CV1} = 92 mV

Figure 32 - VCV1 Ripple and Noise at 90, 115, 230 and 265 VAC.



(e) 90 VAC Input Line Voltage
V_{RIPPLE_CVHV} = 248 mV

(f) 115 VAC Input Line Voltage
V_{RIPPLE_CVHV} = 225 mV

(g) 230 VAC Input Line Voltage
V_{RIPPLE_CVHV} = 244 mV

(h) 265 VAC Input Line Voltage
V_{RIPPLE_CVHV} = 229 mV

Figure 33 – VCVHV Ripple and Noise at 90, 115, 230 and 265 VAC.

10.9 Output Protections

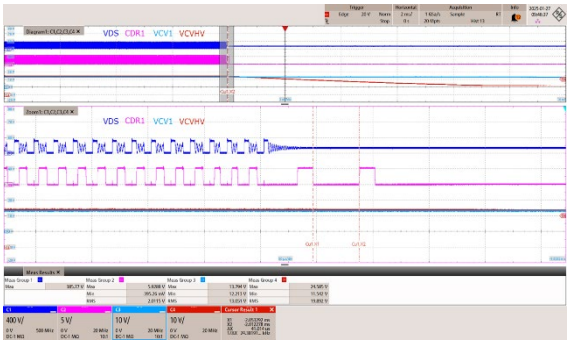
10.9.1 CV1 Output Overvoltage Protection

The overvoltage protection thresholds of CV1 were tested with full load on CVHV and no-load on CV1. Additional charge was injected into the output filter capacitor of the output under test until the converter went into an auto-restart. The test was carried out with the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC and 265 VAC
- CV1 = 12 V @ 0 A
- CVHV = 24 V @ 1.25 A

V_{IN}	V_CVHV	CV1 OVP	
[VAC]	[V]	[V]	[%]
90	24.4	13.8	115
115	24.4	13.8	115
230	24.4	13.8	115
265	24.4	13.8	115

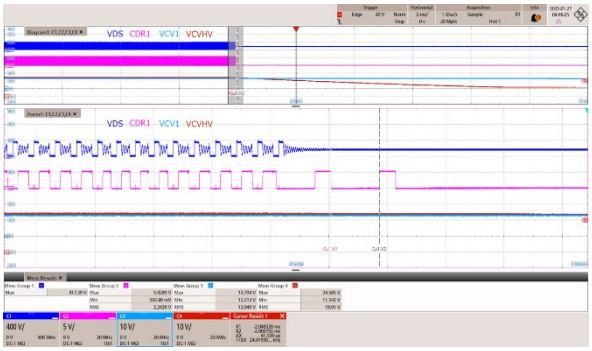
Table 6 - CV1 Outputs OVP Test.



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

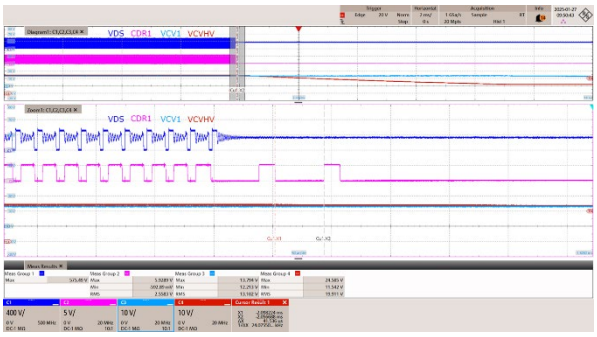
(a) 90 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

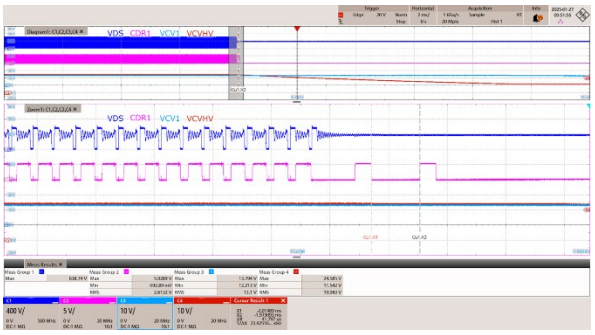
(b) 115 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

(c) 230 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

(d) 265 VAC Input Line Voltage

Figure 34 - CV1 Output at 90, 115, 230, 265 VAC.

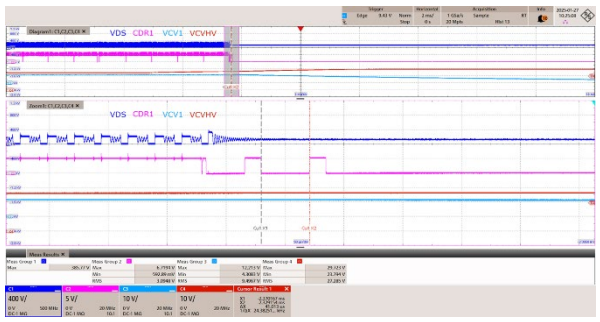
10.9.2 CVHV Output Overvoltage Protection

The overvoltage protection thresholds of CVHV were tested with full load on CV1 and no load on CVHV. Additional charge was injected into the output filter capacitor of the output under test until the converter went into an auto-restart. The test was carried out with the following conditions:

- Line voltages 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CV1 = 12 V @ 1.67 A
- CVHV = 24 V @ 0 A

V_{IN}	V_CV1	CVHV OVP	
[VAC]	[V]	[V]	[%]
90	12.0	29.7	120
115	12.0	29.7	120
230	12.0	29.7	120
265	12.0	29.7	120

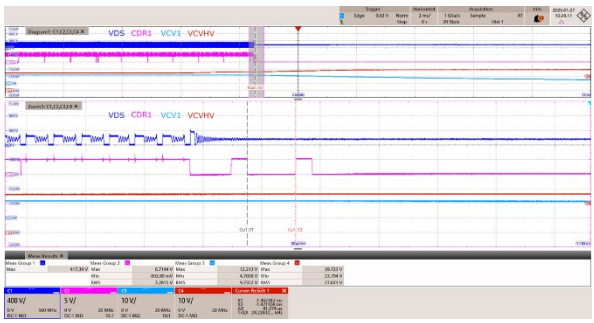
Table 7 - CVHV Output OVP Test.



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

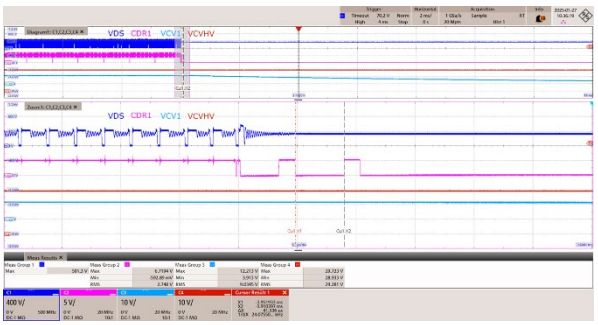
(a) 90 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

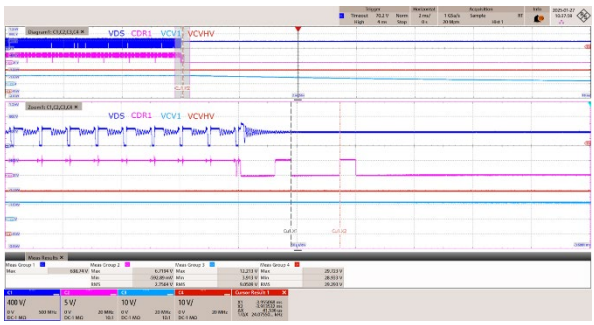
(b) 115 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

(c) 230 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: V_{CVHV}, 10 V/div

Time Division: 2 ms/div
Zoom: 50 us/div

(d) 265 VAC Input Line Voltage

Figure 35 - CVHV Output OVP at 90, 115, 230, and 265 VAC.

10.9.3 CV1 Overload Protection

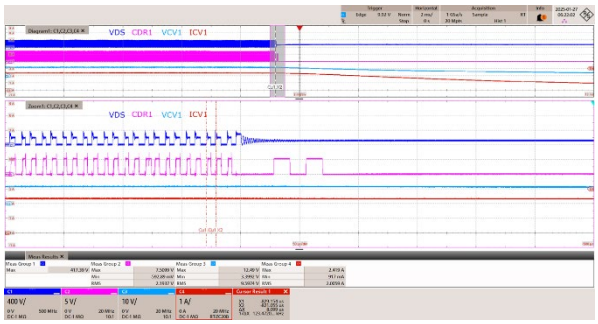
The overload protection thresholds of CV1 were tested with full load on CVHV. The load on CV1 was increased above specification until the converter went into an auto-restart. The results are shown in table 8.

The test was carried out with the following conditions:

- Line voltage: 90 VAC, 115 VAC, 230 VAC, 265 VAC
- CVHV = 24 V @ 1.25 A

V_{IN}	$ICV1_{MAX}$	$ICV1_{MAX}/ICV1_{PK}$	Switching Frequency
[VAC]	[A]	[%]	[kHz]
90	2.42	145	123
115	2.93	175	116
230	3.64	218	112
265	3.84	230	115

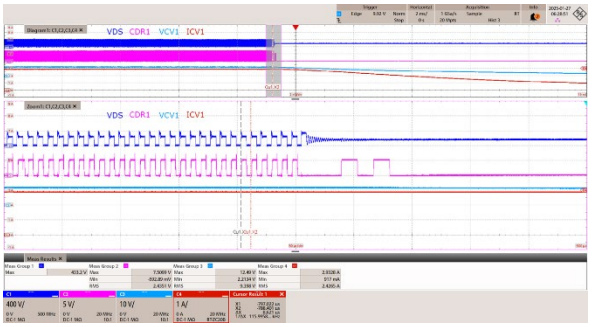
Table 8 - CV1 Total Output Power Limit.



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
C CH4: I_{CV1}, 1 A/div

Time Division: 2 ms/div
Zoom: 50 us/div

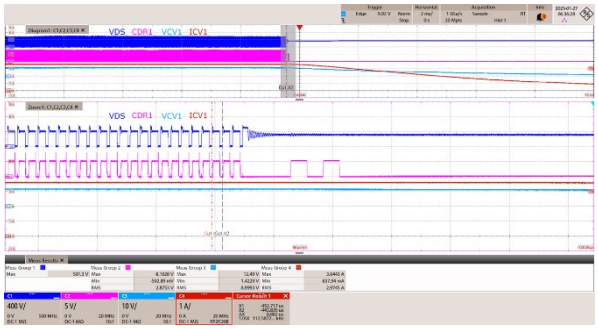
(a) 90 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: I_{CV1}, 1 A/div

Time Division: 2 ms/div
Zoom: 50 us/div

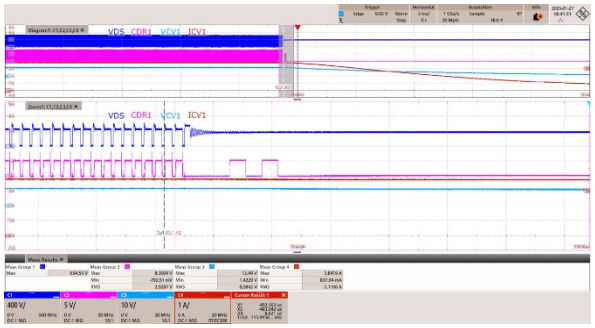
(b) 115 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: I_{CV1}, 1 A/div

Time Division: 2 ms/div
Zoom: 50 us/div

(c) 230 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: I_{CV1}, 1 A/div

Time Division: 2 ms/div
Zoom: 50 us/div

(d) 265 VAC Input Line Voltage

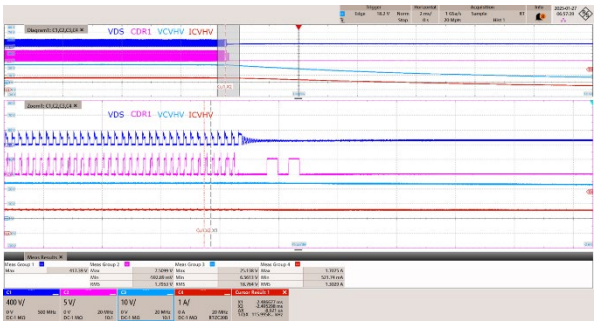
Figure 36 - CV1 Overload Protection at 90, 115, 230 and 265 VAC.

10.9.4 CVHV Overload Protection

The overload protection thresholds of CVHV were tested with full load on CV1. The load on CVHV was increased above specification until the converter went into an auto-restart. The test was carried out with all nominal line voltages 90 VAC, 115 VAC, 230 VAC and 265 VAC. The results are shown in table 9.

V_{IN}	$ICVHV_{MAX}$	$ICVHV_{MAX}/ICVHV_{PK}$	Switching Frequency
[VAC]	[A]	[%]	[kHz]
90	1.71	137	116
115	1.98	158	113
230	2.38	190	116
265	2.46	197	113

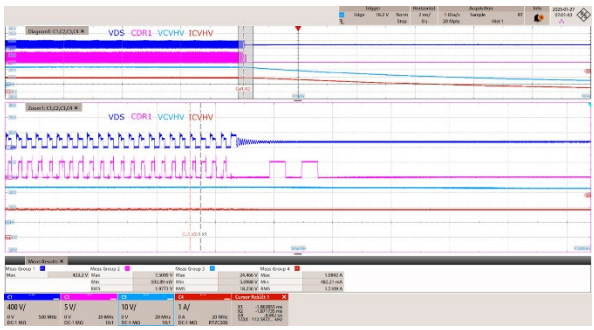
Table 9 - CVHV Total Output Power Limit.



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: I_{CV1}, 1 A/div

Time Division: 2 ms/div
Zoom: 50 us/div

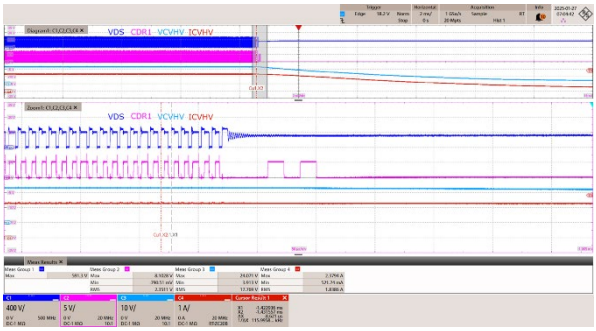
(a) 90 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: I_{CV1}, 1 A/div

Time Division: 2 ms/div
Zoom: 50 us/div

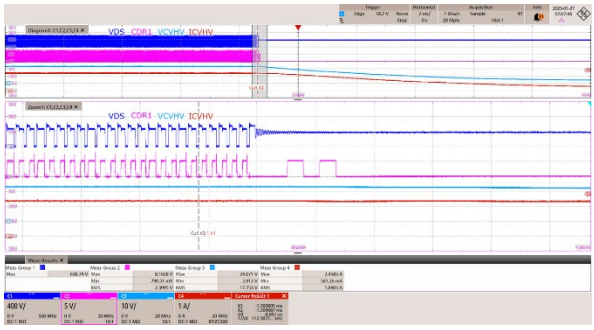
(b) 115 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: I_{CV1}, 1 A/div

Time Division: 2 ms/div
Zoom: 50 us/div

(c) 230 VAC Input Line Voltage



CH1: V_{DRAIN}, 400 V/div
CH2: V_{CDR1}, 5 V/div
CH3: V_{CV1}, 10 V/div
CH4: I_{CV1}, 1 A/div

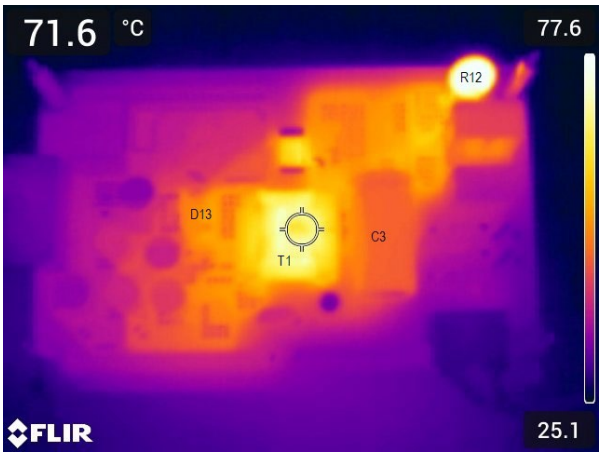
Time Division: 2 ms/div
Zoom: 50 us/div

(d) 265 VAC Input Line Voltage

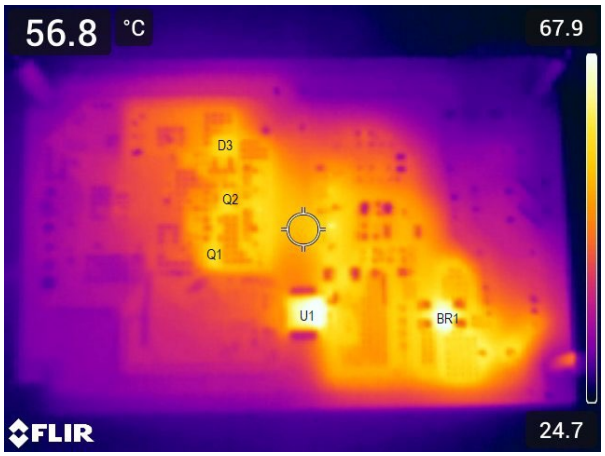
Figure 37 - CVHV Overload Protection at 90, 115, 230 and 265 VAC.

10.10 Thermal Performance

There are no external heatsinks required for this design. PCB copper is used for cooling of the InnoMux2-EP IC. No forced air-cooling was deployed during any test. The temperatures of the hottest component in the assembly are shown below.



(a) Top View

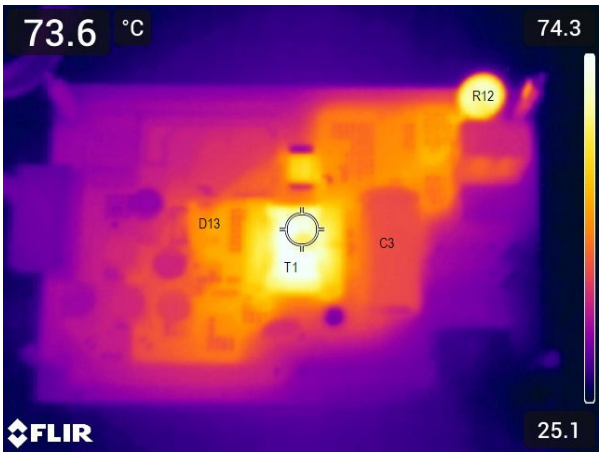


(b) Bottom View

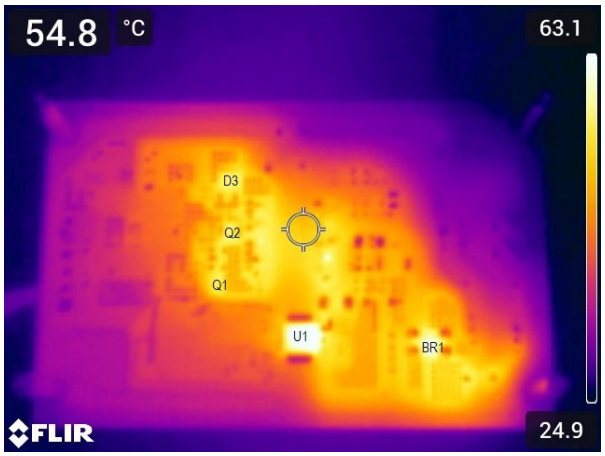
Figure 38 – Thermal Image, 90 VAC, Full Load.

Component	Description	Temperature [˚C]
		V_{IN} = 90 VAC
U1	InnoMux2	71.5
Q2	Selection FET	60.5
D3	CVHV Diode	59.5
Q1	SR FET	60.1
BR1	Bridge	69.4
D13	SR snub diode	56.8
T1	Trf winding	75.6
T1	Trf core	71.6
R12	NTC	79.1
C3	Bulk Capacitor	49.6
	Ambient	24.4

Table 10 - Component Temperature at 90 VAC and Full Load.



(a) Top View

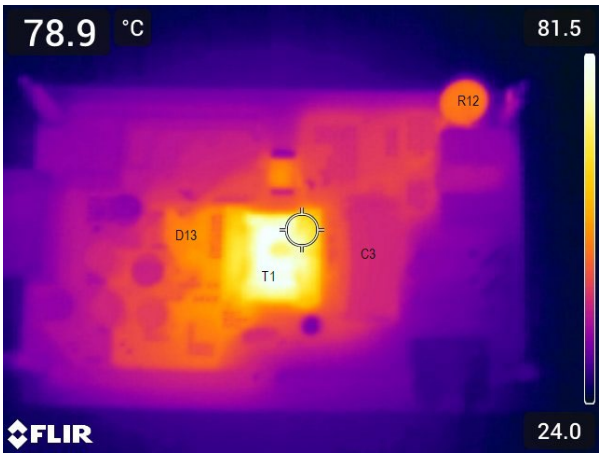


(b) Bottom View

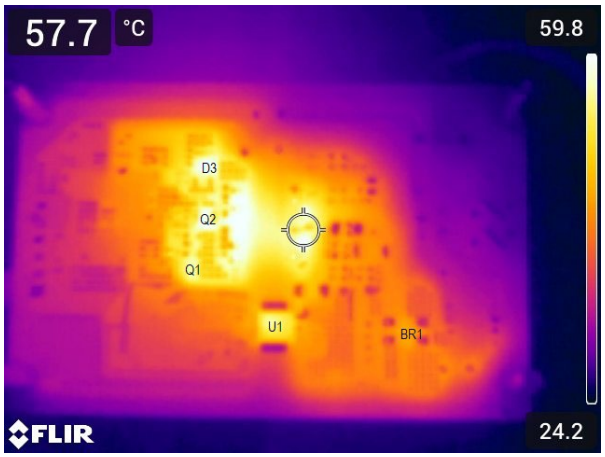
Figure 39 – Thermal Image, 115 VAC, Full Load.

Component	Description	Temperature [˚C]
		V_{IN} = 115 VAC
U1	InnoMux2	62.5
Q2	Selection FET	57.8
D3	CVHV Diode	58.8
Q1	SR FET	58.2
BR1	Bridge	61.9
D13	SR snub diode	54.5
T1	Trf winding	74.4
T1	Trf core	69.2
R12	NTC	70.6
C3	Bulk Capacitor	44.5
	Ambient	23.9

Table 11 - Component Temperature at 115 VAC and Full Load.



(a) Top View

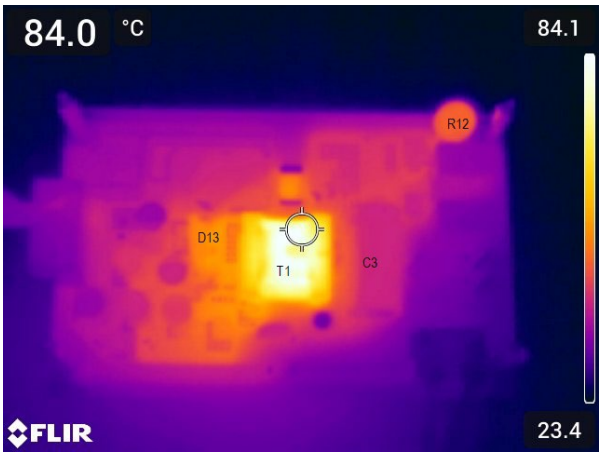


(b) Bottom View

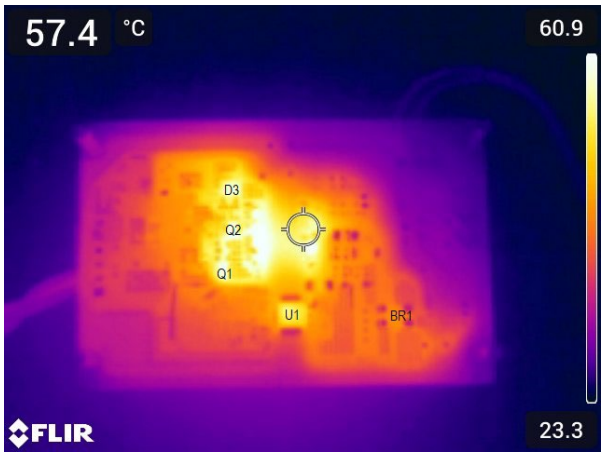
Figure 40 – Thermal Image, 230 VAC, Full Load.

Component	Description	Temperature [˚C]
		V_{IN} = 230 VAC
U1	InnoMux2	57.3
Q2	Selection FET	61.2
D3	CVHV Diode	60.6
Q1	SR FET	59.7
BR1	Bridge	46.5
D13	SR snub diode	58.0
T1	Trf winding	83.7
T1	Trf core	78.5
R12	NTC	53.1
C3	Bulk Capacitor	41.1
	Ambient	23.7

Table 12 - Component Temperature at 230 VAC and Full Load.



(a) Top View



(b) Bottom View

Figure 41 – Thermal Image, 265 VAC, Full Load.

Component	Description	Temperature [˚C]
		V_{IN} = 265 VAC
U1	InnoMux2	60.6
Q2	Selection FET	64.2
D3	CVHV Diode	62.9
Q1	SR FET	63.8
BR1	Bridge	47.2
D13	SR snub diode	57.8
T1	Trf winding	85.1
T1	Trf core	79.5
R12	NTC	50.4
C3	Bulk Capacitor	41.1
	Ambient	22.0

Table 13 - Component Temperature at 265 VAC and Full Load.

Component	Description	Component Temperatures [˚C]			
		V_{IN} = 90 V	V_{IN} = 115 V	V_{IN} = 230 V	V_{IN} = 265 V
U1	InnoMux2	71.5	62.5	57.3	60.6
Q2	Selection FET	60.5	57.8	61.2	64.2
D3	CVHV Diode	59.5	58.8	60.6	62.9
Q1	SR FET	60.1	58.2	59.7	63.8
BR1	Bridge	69.4	61.9	46.5	47.2
D13	SR snub diode	56.8	54.5	58.0	57.8
T1	Trf winding	75.6	74.4	83.7	85.1
T1	Trf core	71.6	69.2	78.5	79.5
R12	NTC	79.1	70.6	53.1	50.4
C3	Bulk Capacitor	49.6	44.5	41.1	41.1
-	Ambient	24.4	23.9	23.7	22.0

Table 14 – Summary of Key Component Temperature (Full Load).

10.11 Audible Noise

The Audible noise test setup is show in figure 42 and figure 43.

10.11.1 Test Setup

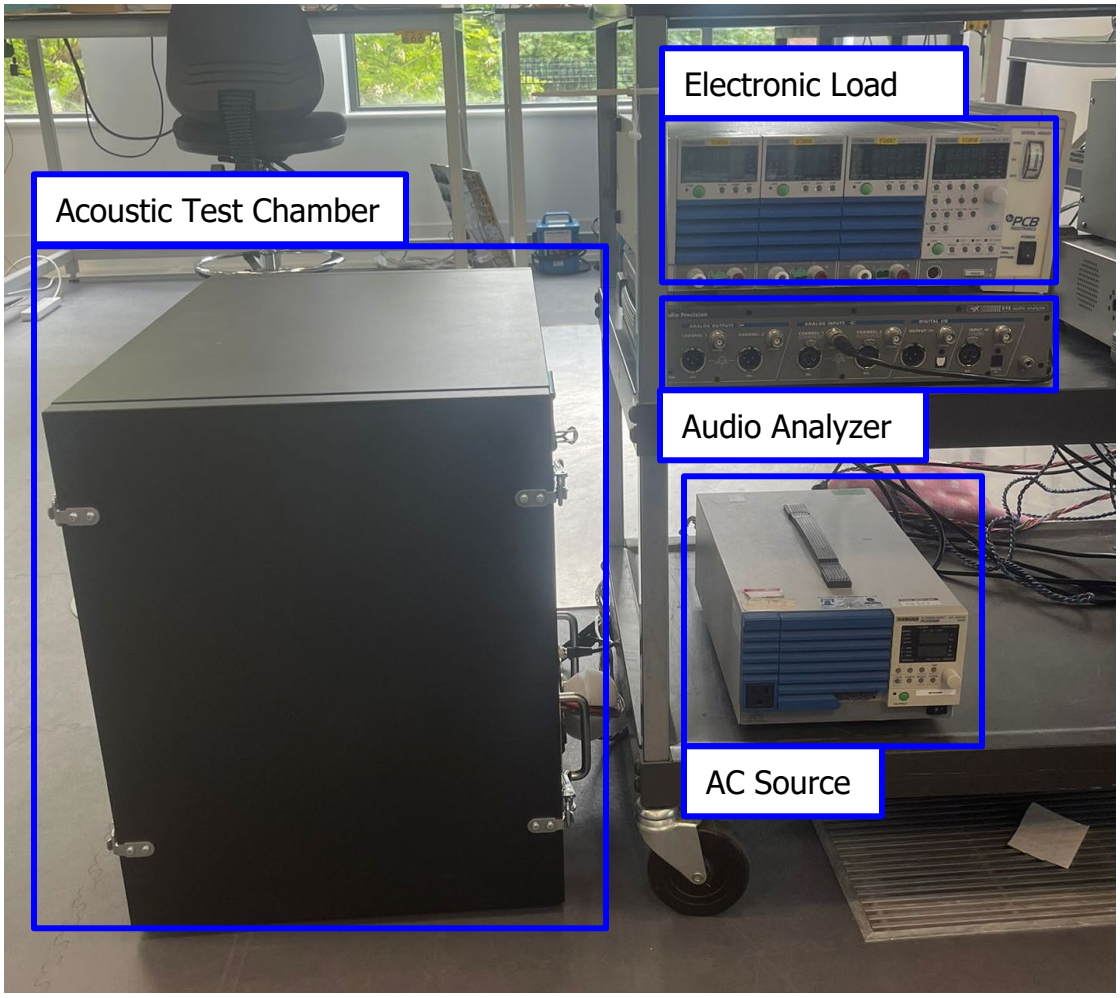


Figure 42 - Audible Noise Test Station

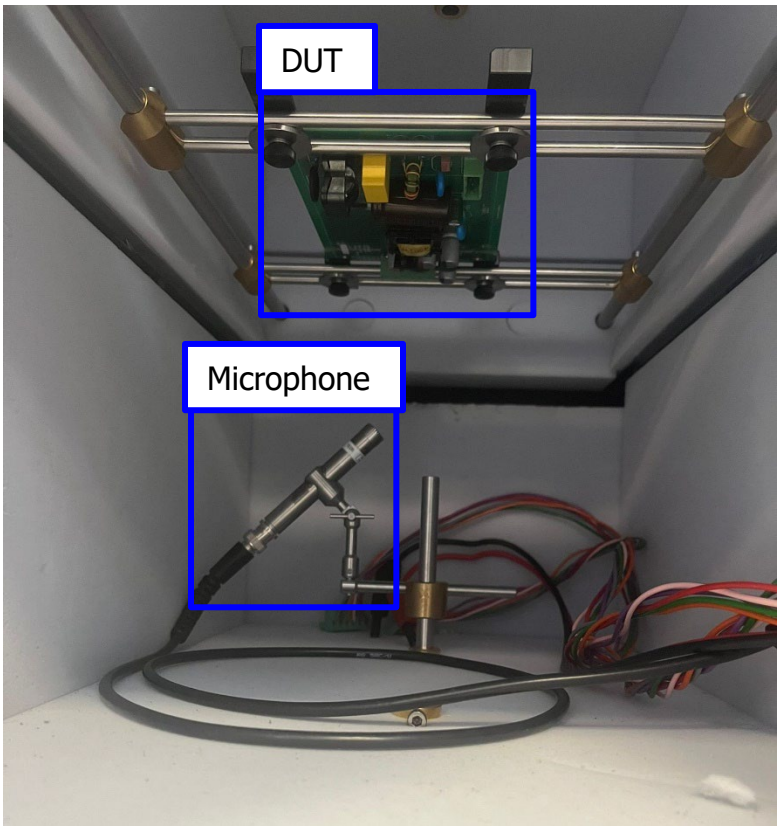


Figure 43 - Acoustic Test Chamber Setup.

10.11.2 Equipment Used

1. Acoustic Test Chamber GRAS AL0030
2. Microphone Audio Precision 426M12
3. AC Source Kikusui PCR500M 500VA
4. Electronic Load Kikusui 482A21

10.11.3 Test Results

The audible noise vs. load measurements is shown in figure 44. These were obtained for all combinations of:

- Low and high mains line voltages 115 VAC and 230 VAC
- CV1 = 12 V @ 1.67 A, 0 to 100% with 3% load increment
- CVHV = 24 V @ 1.25 A, 0 to 100% with 3% load increment
- NTC resistor and input CMCs shorted. These components may generate audible noise which will interfere with measurement of the audio performance of the switching circuit. In the real application, the noise contribution of these standard-off-the-shelf components would need to be assessed and possibly replaced by low-noise alternatives.

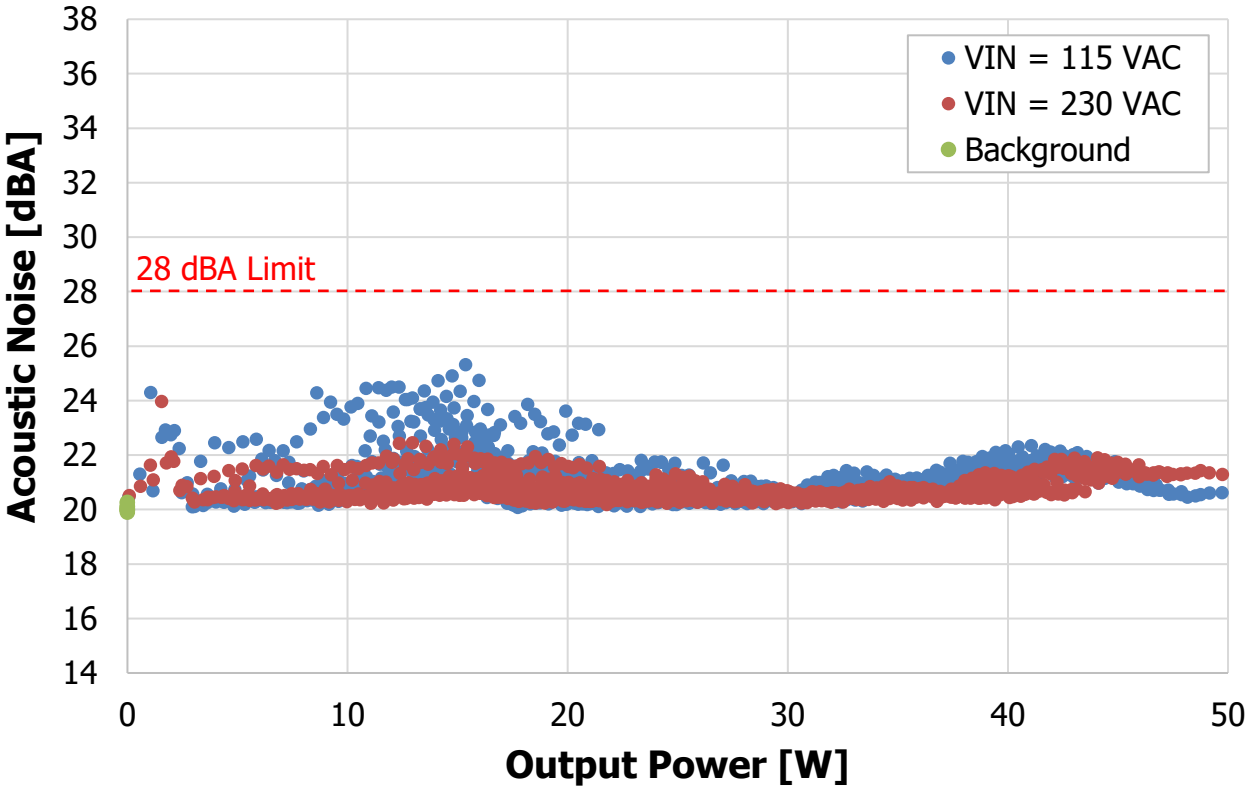


Figure 44 – Audible Noise in Operation.

The audible noise vs. output power in standby mode was measured at room temperature. These were obtained for combinations of:

- Low and high mains line voltages 115 VAC and 230 VAC
- CVHV output = 0 A
- CV1 output = 0 mW to 250 mW
- NTC resistor and input CMCs shorted. These components may generate audible noise which will interfere with measurement of the audio performance of the switching circuit. In the real application, the noise contribution of these standard-off-the-shelf components would need to be assessed and possibly replaced by low-noise alternatives.

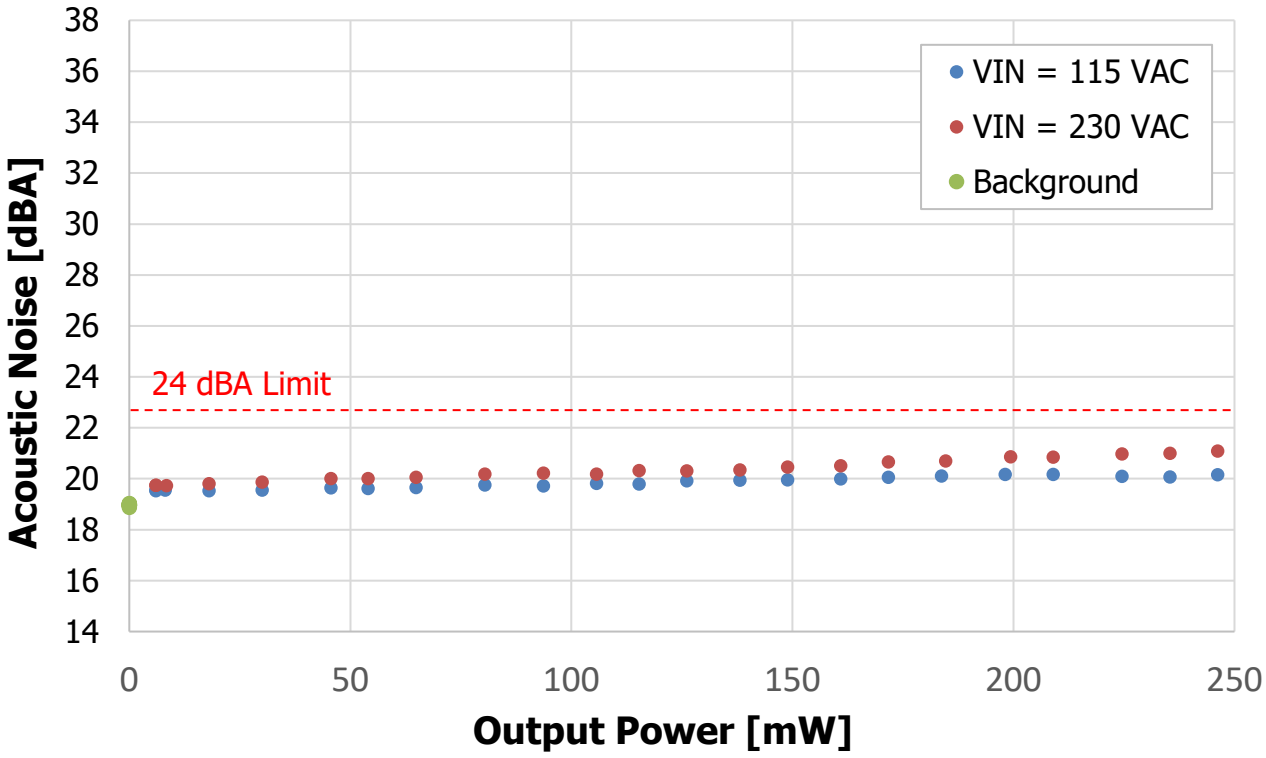


Figure 45 – Standby Power Consumption vs. Input Line Voltage.

10.12 Conducted Emissions

Conducted EMI measurement were performed at 115 VAC and 230 VAC, full power:

- CV1 = 12 V @ 1.67 A
- CVHV = 24 V @ 1.25 A

Measurements were taken with and without earth connection.

10.12.1 Test Setup

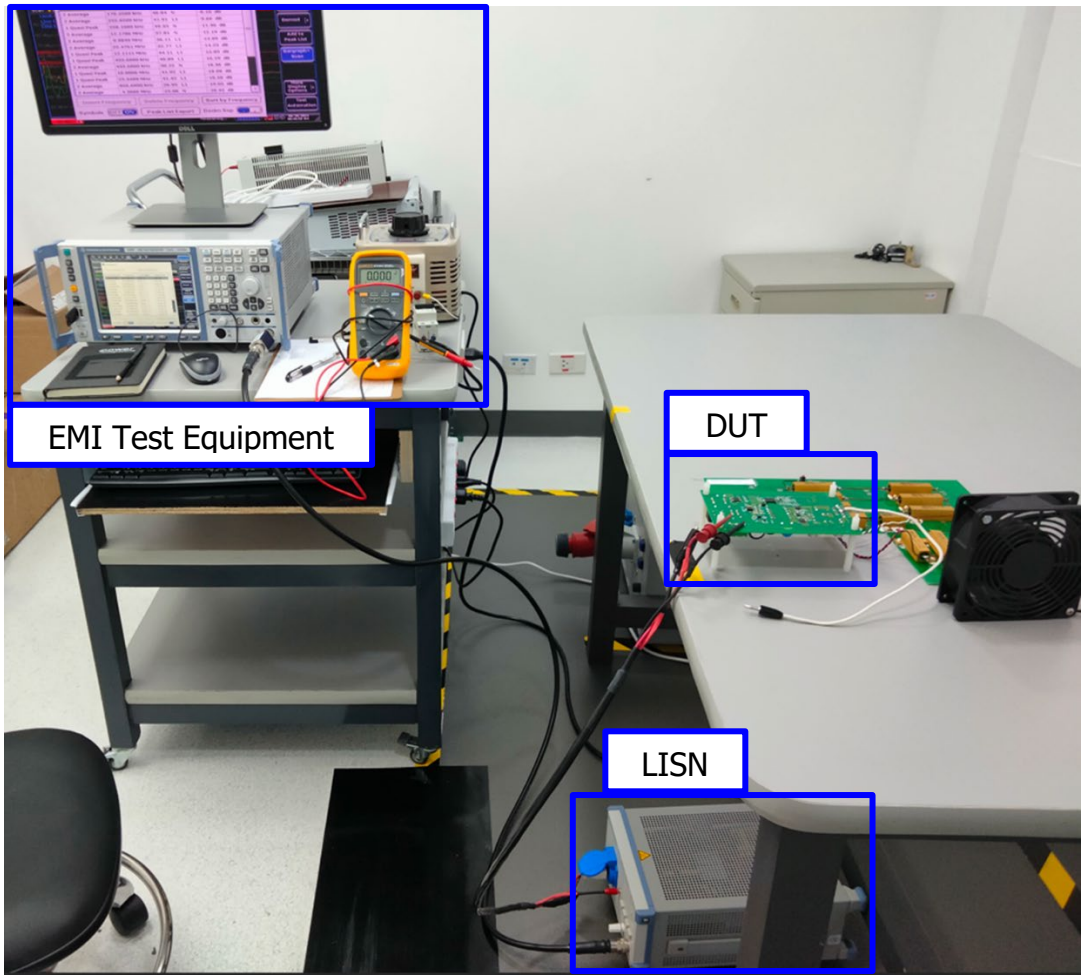


Figure 46 – Conducted Emission Test Setup.

10.12.2 Equipment Used

1. Rohde and Schwarz ENV216 two-line V-network
2. Rohde and Schwarz ESRP EMI Test Receiver

10.12.3 Test Results with earth connection.

The earth was connected to the board's input earth and the output secondary ground.

10.12.3.1 115 VAC Line Input

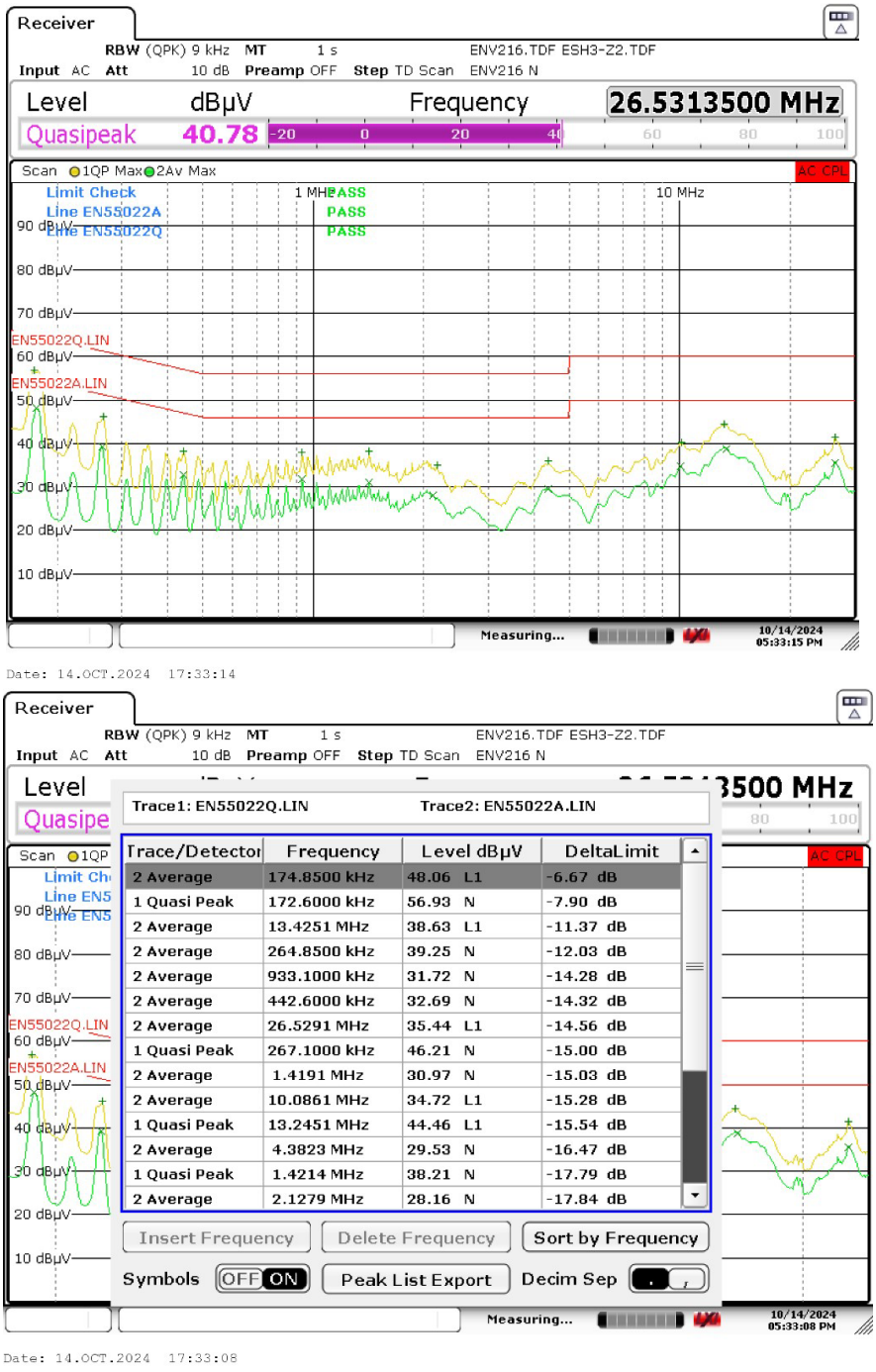


Figure 47 – Conducted Emission Scan at 115 VAC, earthed.

10.12.3.2 230 VAC Line Input

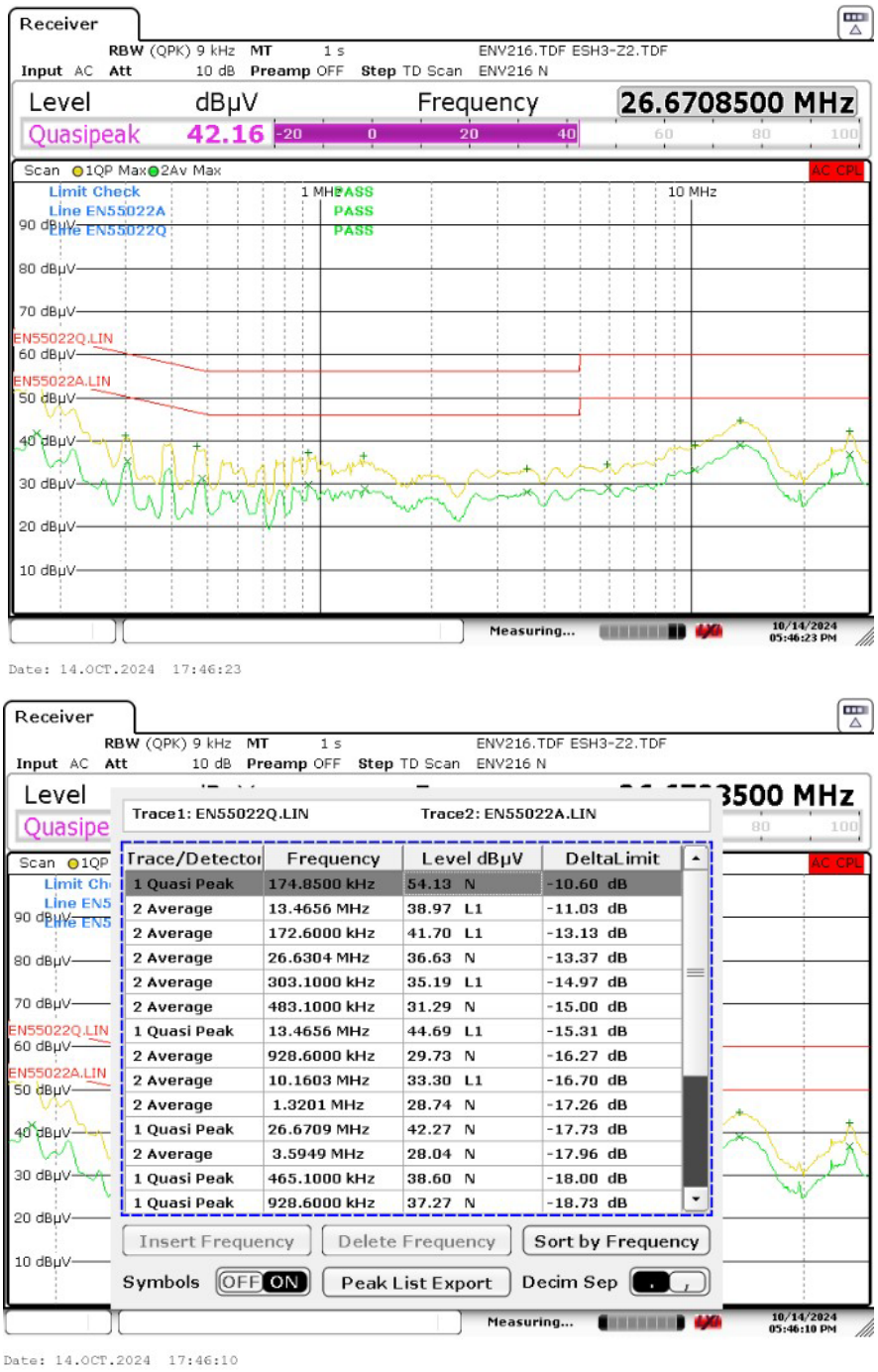


Figure 48 – Conducted Emission result at 230 VAC, earthed.

10.12.4 Test Results without an earth connection.

10.12.4.1 115 VAC Line Input

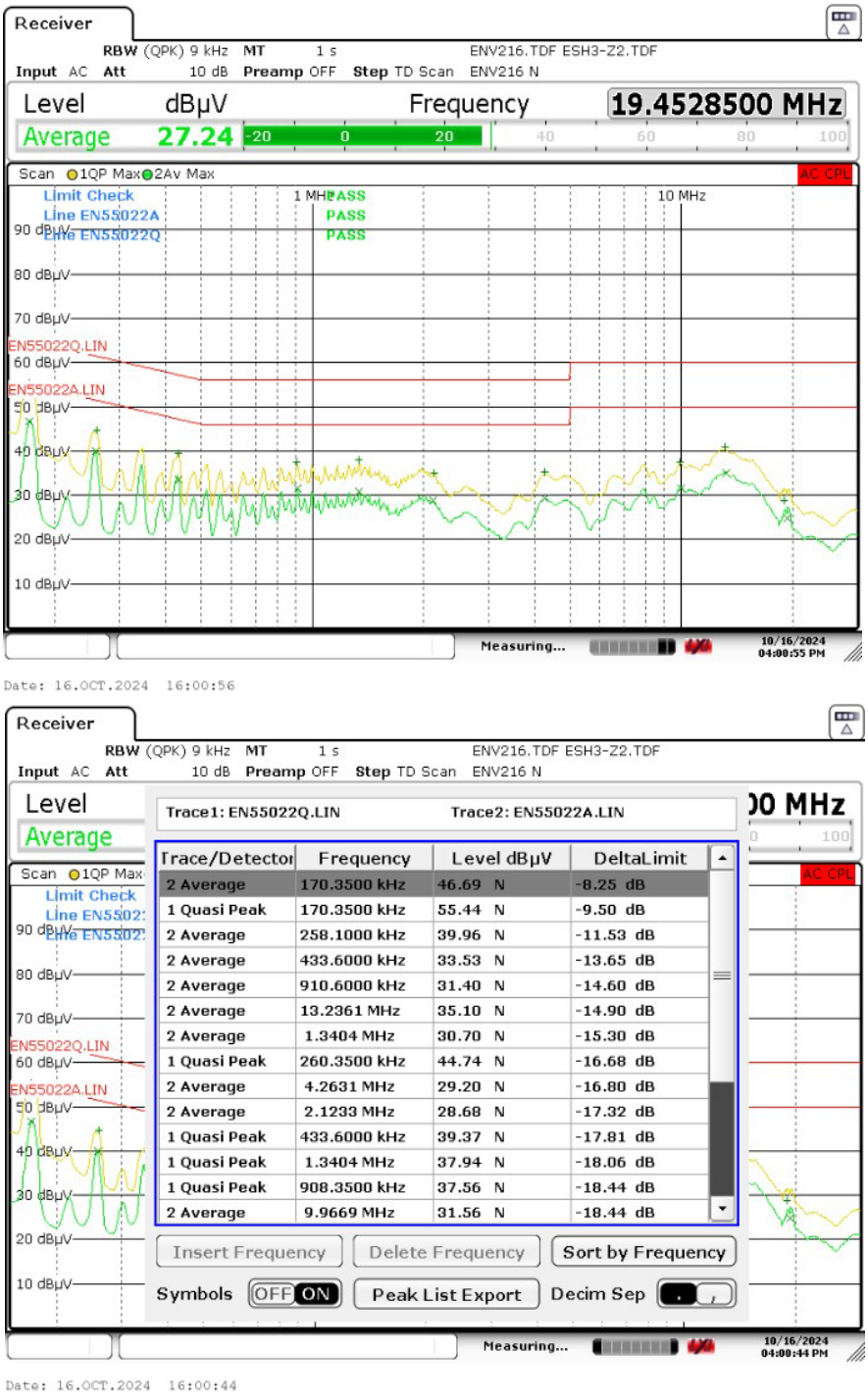


Figure 49 – Conducted Emission result at 115 VAC, floating earth.

10.12.4.2 230 VAC Line Input

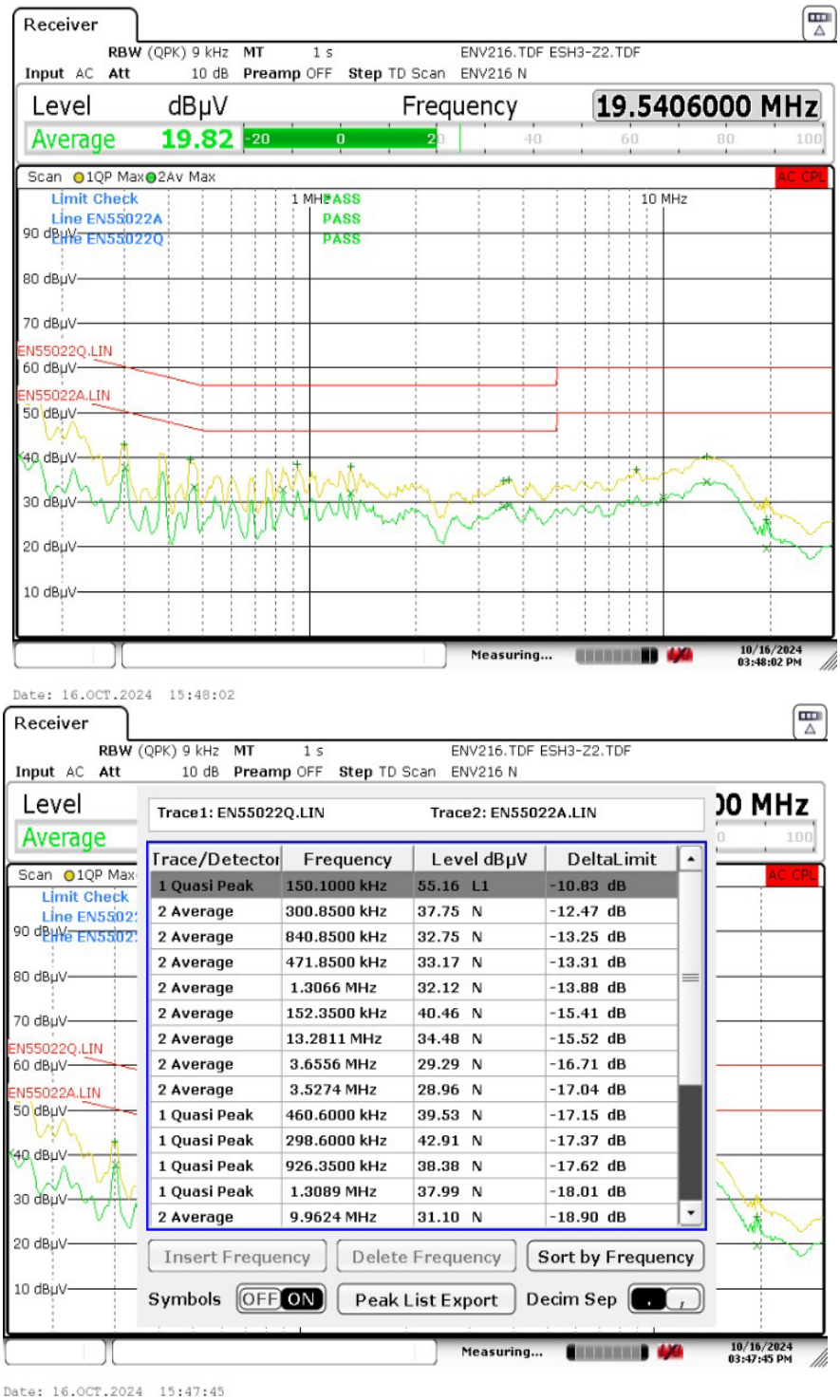


Figure 50 – Conducted Emission result at 230 VAC, floating earth.

10.13 Electrostatic Discharge (ESD)

An ESD test was performed with 230 VAC line input at full load (12 V 1.67 A, 24 V 1.25 A).

Each test strike was applied directly to the power supply outputs. LED indicators were used to show output condition after each strike.

A test failure was defined as an auto-restart (AR) fault or an output latch-off that needed operator intervention to recover, or a complete loss of function that was not recoverable.

10.13.1 Test Setup

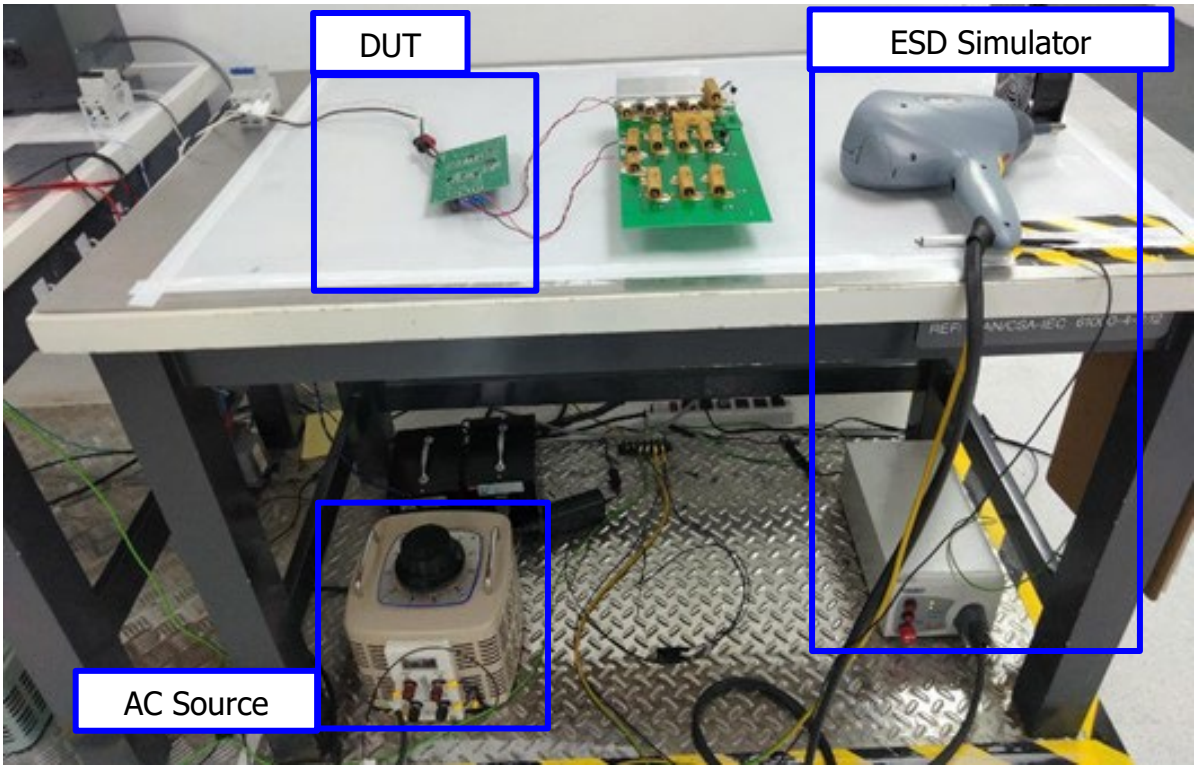


Figure 51 - ESD Test Setup.

10.13.2 Test Result

10.13.2.1 Contact Discharge Test Result

Contact Discharge Voltage (kV)	ESD Point	No. of Strikes	Test Result
+8.8	CV1	10	PASS
	CVHV	10	PASS
	GND	10	PASS
-8.8	CV1	10	PASS
	CVHV	10	PASS
	GND	10	PASS

Table 15 - Contact Discharge Result.

10.13.2.2 Air Discharge Test Result

Air Discharge Voltage (kV)	ESD Point	No. of Strikes	Test Result
+16.5	CV1	10	PASS
	CVHV	10	PASS
	GND	10	PASS
-16.5	CV1	10	PASS
	CVHV	10	PASS
	GND	10	PASS

Table 16 - Air Discharge Result.

10.14 Combinational Wave Surge Test

A surge test was performed with 230 VAC line input at full load (12 V 1.67 A, 24 V 1.25 A).

A test failure was defined as an auto-restart (AR) fault or an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

10.14.1 Test Setup

For Differential mode test, PE was floating. Whereas for the Common mode, Ring Wave and EFT test, PE was connected to secondary output ground and input PE of the board.

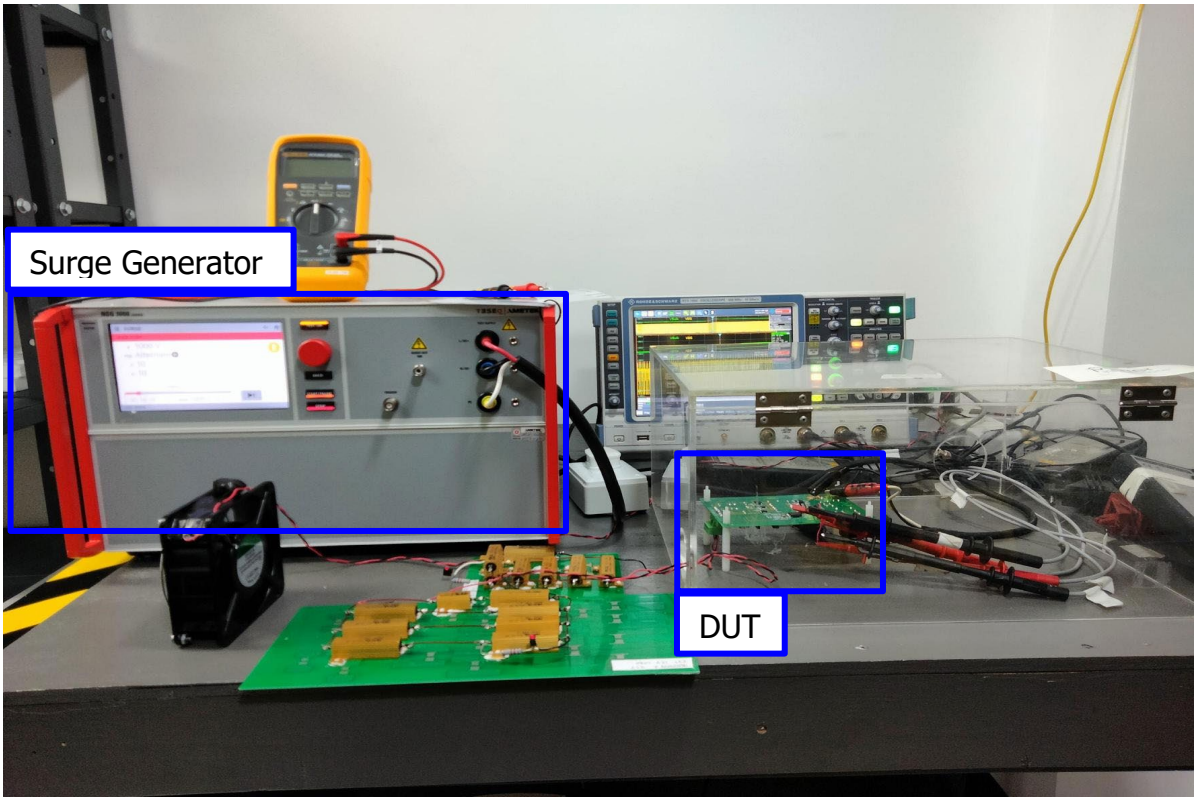


Figure 52 - Surge Test Setup.

10.14.2 Test Results

10.14.2.1 Common Mode Test Result

Surge Voltage Level (kV)	Angle (º)	IEC Coupling	No. of Strikes	Generator Impedance (Ω)	Test Result
+3.0	0	L, N to PE	10	12	PASS
	90	L, N to PE	10	12	PASS
	270	L, N to PE	10	12	PASS
-3.0	0	L, N to PE	10	12	PASS
	90	L, N to PE	10	12	PASS
	270	L, N to PE	10	12	PASS

Table 17 - Common Mode Test Result.

10.14.2.2 Differential Mode Test Result

Surge Voltage Level (kV)	Angle (º)	IEC Coupling	No. of Strikes	Generator Impedance (Ω)	Test Result
+2.0	0	L, N	10	2	PASS
	90	L, N	10	2	PASS
	270	L, N	10	2	PASS
-2.0	0	L, N	10	2	PASS
	90	L, N	10	2	PASS
	270	L, N	10	2	PASS

Table 18 - Differential Mode Test Result.

10.14.2.3 Ring Wave Test Result

Surge Voltage Level (kV)	Angle (º)	IEC Coupling	No. of Strikes	Generator Impedance (Ω)	Osc. Period (s)	Test Result
+2.0	0	L, N to PE	10	12	60	PASS
	90	L, N to PE	10	12	60	PASS
	270	L, N to PE	10	12	60	PASS
-2.0	0	L, N to PE	10	12	60	PASS
	90	L, N to PE	10	12	60	PASS
	270	L, N to PE	10	12	60	PASS

Table 19 – Ring wave Test Result.

10.14.2.4 Electrical Fast Transient (EFT) Test Result

Surge Voltage Level (kV)	Angle (º)	IEC Coupling	Frequency (kHz)	Burst Time (ms)	Repetition Time (ms)	Duration (s)	Test Result
+3.0	0	L, N to PE	5	15	300	120	PASS
	90	L, N to PE	5	15	300	120	PASS
	270	L, N to PE	5	15	300	120	PASS
	0	L, N to PE	100	0.75	300	120	PASS
	90	L, N to PE	100	0.75	300	120	PASS
	270	L, N to PE	100	0.75	300	120	PASS
-3.0	0	L, N to PE	5	15	300	120	PASS
	90	L, N to PE	5	15	300	120	PASS
	270	L, N to PE	5	15	300	120	PASS
	0	L, N to PE	100	0.75	300	120	PASS
	90	L, N to PE	100	0.75	300	120	PASS
	270	L, N to PE	100	0.75	300	120	PASS

Table 20 - EFT Test Result.

11 Revision History

Date	Author	Revision	Description & Changes	Reviewed
10-May-24	YL	A	Initial Release.	Apps & Mktg
22-Oct-24	YL	B	Updated schematic and major updates on contents	Apps & Mktg
23-Nov-24	YL	C	BOM Update	Apps & Mktg
07-Oct-2025	WT	D	Added sections: 9 - Common Mode Choke (L4) Specification 10.7.3 - Startup Under single fault condition 10.9 - Output Protections 10.12 - Conducted Emissions 10.13 - Electrostatic Discharge (ESD) 10.14 - Combinational Wave Surge Test Updated sections: 1 - Introduction 6 - Bill of Materials 3 – Update Schematic	Apps & Mktg

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