Application Note AN-106Q for Automotive Applications InnoSwitch3-AQ Family

Design Guide

1 Introduction

Power supplies used in automotive applications are usually subject to much harsher conditions than those used in commercial or industrial stationary applications. Automotive power supplies are often exposed to wide temperature ranges, shock and vibration, foreign particles and contaminants, and high levels of EMI. BUS voltages can go as high as 1000 VDC for electric vehicles, so the effects of high-voltage DC and transients must also be considered. Depending on the load, input voltage, and location of a power supply in a vehicle, the conditions stated earlier must be considered to ensure a safe, stable, and reliable power supply operation.

In many automotive applications, the power supply is part of the functional safety concept according to ISO26262. Reliability through proper design is mandatory. This application note considers a design supporting ISO26262.

The InnoSwitch™3-AQ family of ICs dramatically simplifies the design and manufacture of isolated flyback power converters in automotive applications. The InnoSwitch3-AQ family combines primary and secondary controllers and safety-rated feedback into a single IC allowing accurate output voltage regulation even with a wide input voltage range of 30 VDC to >1000 VDC.

InnoSwitch3-AQ devices incorporate multiple protection features, including input line over- and undervoltage protection[1], output overvoltage and over-current limiting, and over-temperature protection. The devices' ability to start up from 30 V input makes them ideal for functional safety critical emergency power supplies.

The InnoSwitch3-AQ IC combines a high-voltage power switch (MOSFET, SiC MOSFET or PowiGaN™) along with both primary-side (high-voltage side) and secondary-side (low-voltage side) controllers in one device. The architecture incorporates a novel inductive coupling feedback scheme (FluxLink™) with reinforced isolation to provide a safe, reliable way to transmit accurate output voltage and current information from the secondary to the primary controller.

The primary controller on the InnoSwitch3-AQ IC is a quasi-resonant (QR) flyback controller that can operate in and seamlessly switch between continuous conduction mode (CCM), boundary mode (CrM), and discontinuous conduction mode (DCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, a 5 V regulator on the PRIMARY BYPASS pin, an audible noise reduction engine for light load operation, bypass overvoltage detection circuit, current limit selection circuitry, over-temperature protection, leading edge blanking, and a high-voltage switch (either 750 V, 900 V or 1700 V).

The InnoSwitch3-AQ secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, constant voltage (CV) and constant current (CC) controller, a 4.4 V regulator on the SECONDARY BYPASS pin, QR mode circuitry, oscillator and timing circuits and numerous integrated protection features.

2 Scope

This application note is intended to guide engineers in designing an isolated DC-DC flyback power supply using the InnoSwitch3-AQ family of devices for automotive applications. This application note uses the Power Integrations PIXls designer tool for InnoSwitch3-AQ devices. The PIXls designer is part of the PI Expert Suite™ of software tools developed to simplify the process of designing with Power Integrations' products. PIXls is a spreadsheet-based tool that takes a user's specifications and calculates critical design parameters needed to complete a power supply design. (PIXls is available at https://piexpertonline.power.com)

This Application Note Contains the Following Sections/ Topics:

1. Step-by-step design checklist for PIXls, component selection, and layout for automotive applications.
2. Electrical design guide for high input voltage power supplies according to IEC 60644-1
3. Transformer design and component selection for high-voltage and wide ambient temperature operating range (-40 °C to 105 °C)
4. Layout recommendations for high EMI immunity
5. Circuit design, layout, and transformer guidelines
6. Circuit suggestions for additional protection

3 Related Documents and Standards

/1/ InnoSwitch3-AQ Family data sheet, Rev G. 09/2022

/2/ AN-72 InnoSwitch3 Family Design Guide, Rev F. 09/2022

/3/ IEC 60664-1:2020

Insulation coordination for equipment within low-voltage supply systems

Part 1: Principles, requirements and tests

/4/ IEC 60664-4:2005
Insulation coordination for equipment within low-voltage supply systems
Part 4: Consideration of high-frequency voltage stress.

[1] V Pin OV trigger is disabled by default in INN3947CQ and INN3949CQ

4 Typical Application Schematic

Figure 1 shows the typical application schematic for an isolated flyback converter using the InnoSwitch3-AQ controller. Unless otherwise specified, references to components in this document shall refer to the designators shown in Figure 1. The schematic shown will apply to most applications. Changes in the component count for some circuit sections shall depend on the target application's specifications.

1. Input capacitors (C_{Inx}) – series/parallel combination will depend on input voltage range and filtering requirements.
2. Snubber network (C_{SNx}, R_{SNx}, R_{Sx}, and D_{CLAMPx}) – series/parallel combinations of the snubber network will vary according to input voltage range and output power requirements.
3. Output capacitors (C_{OUTx}) – the number of parallel capacitors will depend on output voltage ripple and operating life.
4. SR FETs – the number of units in parallel depends on temperature rise and efficiency targets.

Component values and ratings will vary according to specific application specifications.

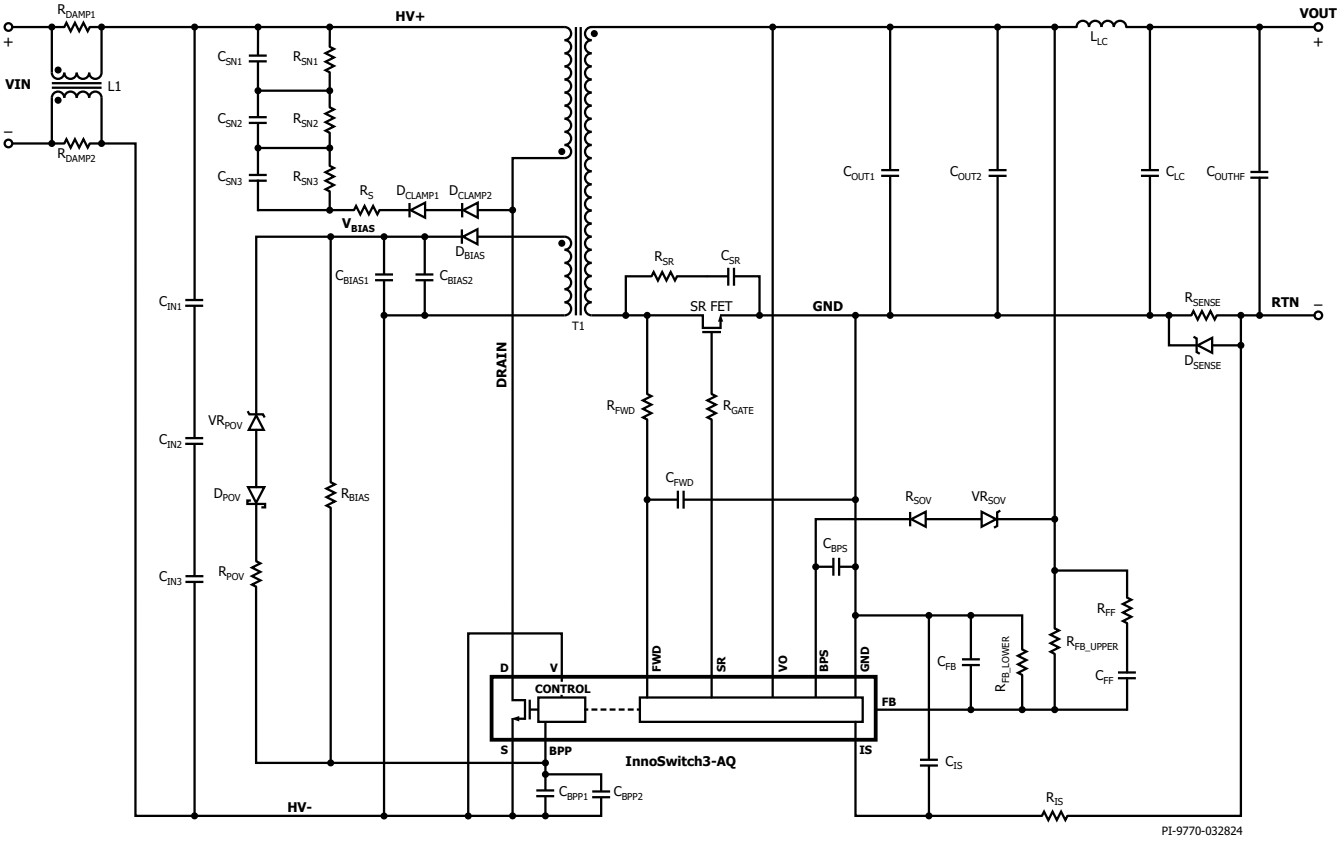

Figure 1. InnoSwitch3-AQ Typical Application Schematic.

5 Design Checklists

This section contains checklists that designers can follow to ensure all relevant points when designing using the InnoSwitch3-AQ are addressed before a prototype is built. The checklist is split into multiple parts:

1. PIXIs
2. Component Selection
3. Layout

It is recommended that designers review each item in the checklist to reduce development time by increasing the likelihood of a specifications -compliant prototype (may require minor tuning during testing).

Part 1: PIXIs Design Checklist

Go to https://piexpertonline.power.com to access the PIXIs design spreadsheet

IMPORTANT!

When using PIXIs, no WARNINGS must be shown on the INFO column of the spreadsheet. If warnings are present, the reason for the warning and tips on resolving it will be given in the right most column of the spreadsheet.

DESIGNS WITH WARNINGS ARE NOT CONSIDERED VIABLE.

✓	#	Parameter	Comments	Page
	1	**Set Desired Output Voltage (VOUT):** Output voltage should be from 5 V to 24 V	For VOUT >24 V, contact Power Integrations for more details.	11
	2	**Input all Desired Operating Conditions:** Set at least two operating conditions - the maximum and minimum input voltage with its respective maximum output current.	a) Up to 9 operating conditions can be specified. PIXIs will try to find the best solution to meet all conditions. b) Use default values for EFFICIENCY (0.85) and Z_FACTOR (0.5)	11
	3	**Select Primary Controller:** Use the power table in the InnoSwitch3-AQ data sheet as a guide to select the appropriate device.	See Section 6.2 of this document for more details.	12
	4	**Select Controller Current Limit Mode:** Choose between STANDARD and INCREASED.	In general: STANDARD - if the power output is well within the device's capability or cooling is a challenge INCREASED - if a higher power is required, especially at minimum input or if thermal management is not an issue. See Section 6.2 for more design options and considerations.	12
	5	**Set Maximum Switching Frequency:** Recommended initial values are 400 VDC Systems: 65 kHz for 60 W and above, 85 kHz for lower power 800 VDC Systems: 35 kHz for 35 W or higher, 45 kHz for lower power.	This value can be iterated until an acceptable design is achieved. See Section Worst-Case Electrical Parameters for more details.	13
	6	**V_{OR}: In general, set V_{OR} to 10x to 12.5x of VOUT**	See Table 3 in Section Worst-Case Electrical Parameters for a list of suggested V_{OR} values.	14
	7	**Primary Inductance Tolerance (LPRIMARY_TOL)**	Use 5% to 7% tolerance for higher transformer production yield.	14
	8	**SR FET:** Use the SR FET automatically chosen by PIXIs.	If another SR FET is used, it should meet the following requirements: a) 1.265 V ≤ $V_{TH(MIN)}$ ≤2.5 V b) $R_{DS(ON)}$ > (0.01 x V_{OUT})/(I_P x V_{OR}) where I_P is the primary peak current limit (PIXIs Row 78) c) SR FET diode reverse recovery, T_{RR} < 40 ns d) It is not recommended to use FETs with breakdown voltage > 150 V (limited by FWD pin voltage rating) e) See Section 7.5 for more details on SR FET selection.	17
	9	**Transformer Core Selection:** Select core from the database. Ensure Bmax ≤ 3800 mT Core material should be one of the following: 3C95, 3C96, PC95, N95 or equivalent.	If the desired core is not on the PIXIs database, check the core size for power handling capability by following the steps in Section 8.1.	35

✓	#	Parameter	Comments	Page
	10	**Primary Components Selection Section** Select OV/UV mode. Input desired OV/UV thresholds and use calculated components.	Check the data sheet to see if the device has UV-only protection or both OV and UV.	17
	11	**Secondary Component Selection Section** Use PIXls computed values for the feedback network resistors and capacitor.	For high-precision voltage regulation requirements (<1% tolerance across temperature), see the Precision Voltage Regulation Circuit in Section 9.6	45
	12	**Set Point Analysis** Use set point analysis to check operating points and loading conditions.	Check the following tolerance combinations. There should be no warnings issued by PIXls (PIXls rows 225-227). a. VINMIN, ILIMIT,MAX, LPMAX b. VIN,MAX, ILIMIT,MIN, LPMIN	21
	13	**Check InnoSwitch3-AQ IC Power Loss and Temperature Rise** Calculate the expected operating temp of the InnoSwitch3-AQ IC using the parameters from PIXls.	See Section 6.7.1 on how to calculate temperature rise. If the calculated operating temperature is ≥130 °C at maximum ambient temperature, iterate the design to reduce temperature (e.g., adjust switching frequency, change InnoSwitch3-AQ device.	22
	14	**Magnetics Builder** a) Check if windings fit inside the selected core/ bobbin. Fill must be 80% or less to ensure manufacturability b) Use estimated power loss to calculate the estimated temperature rise of the transformer.	Adjust wire gauge and turns ratio in PIXls if fill or loss is too high. See Section 6.6 for details.	19
Part 2: Component Selection (Component designators refer to Figure 1 in Section 4)				
✓	#	Parameter	Comments	Page
	1	**Input CMC (L1) and Damping Resistors (R_{DAMPx})** a) Use CMC with the highest inductance available that can meet the required maximum input voltage and current. b) Damping resistors should be at least Thick Film, 1206 SMD resistors. The use of surge-capable resistors is recommended	See Section 9.1 for the calculation of damping resistors.	36
	2	**Input Capacitors (C_{INx})** a) Use 68 nF to 150 nF, 1206, MLCC, X7R, rated ≥500 V b) Minimum of 3 in series	Larger capacitors can be used if the capacitor has soft termination. Place C_{IN} in the layout in such a way as to reduce the primary loop.	-
	3	**Primary Snubber Circuit (R_{SNx}, C_{SNx}, D_{CLAMPx}, R_S)** a) If the transformer prototype is ready, calculate snubber based on actual measured primary leakage inductance. b) If no transformer is available yet, assume leakage (L_{lk}) to be 1% of $L_{PRIMARY}$ for designs 35 W and higher. Otherwise, use 1.5% assumed leakage.	a) See Section 7.2 for snubber topology, design calculations, and component selection.	29
	4	**Primary Bias Voltage (C_{BIASx}, D_{BIAS}, R_{BPP})** a) D_{BIAS} - use 200 V, 200 mA, Fast-recovery diode (BAS21GWX or equivalent) b) C_{BIAS} - use two 10 µF, 50 V, 1206, X7R MLCC capacitors. c) R_{BIAS} - use 0603 or 0805, Thick Film SMD resistor.	Place the bias voltage components close to the transformer pins to minimize the bias loop. Place R_{BIAS} close to C_{BPP}. See Section 7.3 for the calculation of optimum R_{BIAS}.	30
	5	**BPP Capacitor (C_{BPP})** a) STANDARD current limit - use 100 nF and 470 nF capacitors in parallel. b) INCREASED current limit - use 100 nF and 4.7 µF capacitors in parallel. c) Use only 0805 or 1206 SMD package, X7R or C0G, rated ≥ 25 V, Fail open, MLCC capacitors.	Place BPP caps as close as possible to the InnoSwitch3-AQ IC and on the same layer. See Section 7.1 for more details.	29

✓	#	Parameter	Comments	Page
	6	**SR FET Snubber (C_{SR}, R_{SR}):** SR Snubber should be tuned during prototype testing. Recommended starting values are: a) For C_{SR}, use 220 pF, 250 V, 1206, X7R MLCC b) For R_{SR}, use 20 Ω, 1206, Thick Film SMD resistor.	The values given here are starting values. Adjust SR FET Snubber values during prototype testing. See Section 7.6 for more details.	33
	7	**Secondary Synchronous Rectifier (SR FET)**	Estimate power loss using PIXIs values for the SR FET, then specify copper cooling area size before starting the layout.	-
	8	**FWD Pin RC Network (R_{FWD}, C_{FWD})** Recommended values: a) For C_{FWD}, use 100 pF, 250 V, 1206, X7R MLCC b) For R_{FWD}, use 47 Ω, 0805 or 1206, Thick Film SMD resistor.	During prototype testing, if the FWD pin voltage spike is near 150 V (> 85%), R_{FWD} can be increased to 100 Ω and C_{FWD} to 330 pF. Place C_{FWD} and R_{FWD} very close to the FWD pin and on the same layer as the InnoSwitch. See Section 7.7 for more information.	34
	9	**BPS Capacitor (C_{BPS})** Use 2.2 µF, 0805 or 1206 SMD package, X7R or C0G, rated ≥25 V, MLCC capacitors.	The BPS capacitor must be placed close to the BPS and GND pins and on the same layer as the InnoSwitch. See Section 7.4 for more information.	31
	10	**SR FET Gate Resistor (R_{GATE})** a) Default value is 0 Ω b) Use 0603, Thick Film SMD Resistor.	Place R_{GATE} next to the GATE pin of the SR FET. If oscillations are observed in the SR GS pin or SR VDS has large spikes, R_{GATE} can be increased up to 5.6 Ω. If parallel SR FETs are necessary to meet thermal requirements, each SR FET must have its own gate resistor with a value < 4.7 Ω.	-
	11	**Feedback Network (R_{FB_UPPER}, R_{FB_LOWER}, C_{FB})** a) Use values calculated by PIXIs b) Use 0402 or 0603, 1% tolerance or better, Thick Film SMD Resistors. c) Use 0603 or 0805, X7R or C0G, 25 V, X7R MLCC for CFB	Place feedback network components close to the InnoSwitch3-AQ IC.	17
	12	**Current Sense Resistor (R_{SENSE})** a) R_{SENSE} = 35 mV/ $I_{OUT(MAX)}$ b) Use 1206 or larger package, 1% tolerance or better, current sense chip resistors.	a) Use multiple resistors in parallel for consistent current limit across temperature for high current applications (>3 A). b) R_{SENSE} must be placed close to the InnoSwitch3. If this is not possible, use a Kelvin connection and properly route the signal to the IS pin. c) $I_{OUT(MAX)}$ should be higher than the highest-rated output current. A value 10% - 20% higher than $I_{OUT(MAX)}$ may be used to ensure that there is adequate margin between the protection threshold and the rated output current.	-
	13	**Current Sense Filter (R_{IS}, C_{IS})** a) For C_{IS}, use 1 µF to 4.7 µF, 0805, X7R or C0G, ≥ 25 V, MLCC. b) For R_{IS}, use 10 Ω, 0402 or 0603, 1% tolerance or better, Thick Film resistors.	Component placement should be beside the IS pin and on the same layer. For C_{IS}, a 1 µF capacitor is suitable for most applications. In some designs, the value may be increased to 4.7 µF depending on the circuit board layout and noise filtering needed for the IS pin signal.	-

✓	#	Parameter	Comments	Page
	14	**Output Capacitors (C_{OUT})** a) Use 220 µF to 330 µF per ampere of load current b) Use only Polymer and Hybrid Polymer Electrolytic Capacitors.	a) Multiple capacitors in parallel can be used to reduce output ripple voltage b) Ensure the total current ripple rating of the output capacitors is greater than the maximum secondary ripple current c) Calculate capacitor life according to manufacturer recommendations d) Place output capacitors in the layout to reduce the secondary loop. See Section 7.8 for more details.	34
	15	**High-Frequency Output Filter Capacitor (C_{OUTHF})** Use 0.1 µF to 10 µF, 1206, X7R or C0G, 50V, MLCC	Place this capacitor where the load connects to the power supply. The load of the power supply must never bypass this capacitor. The selection of the most appropriate value depends on the measured ripple and EMI.	-
	16	**Primary-Sensed Overvoltage Protection (D_{POV}, VR_{POV}, R_{POV})** a) Optional but recommended for functional safety b) For D_{POV}, use a 100 V, 200 mA, Standard recovery, SMD diode c) For VR_{POV}, see Figure 43 to calculate the required breakdown voltage d) For R_{POV}, use a 47 Ω, 0603, 1% to 5% tolerance, thick film SMD resistor.	Place primary sensed overvoltage components near the InnoSwitch3-AQ IC. See Section 9.2 for the schematic and details.	43
	17	**Secondary-Sensed Overvoltage Protection (D_{SOV}, VR_{SOV}, R_{SOV})** a) For D_{SOV}, use a 100 V, 200 mA, Standard recovery, SMD diode b) For VR_{SOV}, see Figure 43 to calculate the required breakdown voltage. c) For R_{SOV}, use a 47 Ω, 0603, 1% to 5% tolerance, thick film SMD resistor	Place secondary-sensed overvoltage components near the InnoSwitch3-AQ IC. See Section 9.3 for details.	43
	18	**IS Pin Protection Diode (D_{SENSE})** Use a Schottky diode with at least 50 A non-repetitive peak current. The diode voltage rating can be ≤ 40 V.	Needed during events such as an output short circuit with very low impedance where IS-pin voltage may exceed the absolute maximum rating of the pin. See Section 9.4	43

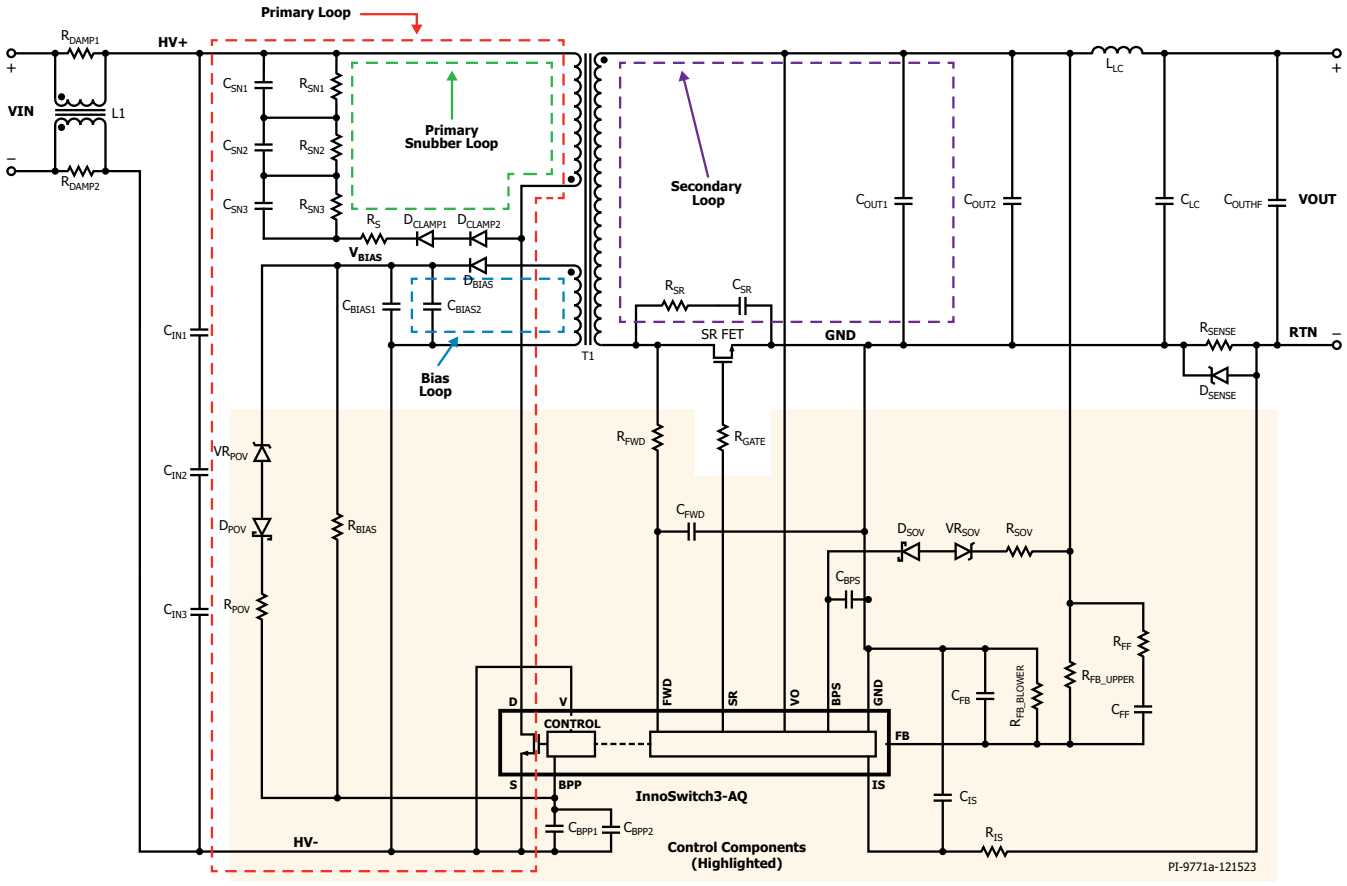

Figure 2. Schematic Showing Critical Loops and Control Components.

Part 3: PCB Placement and Layout (Refer to Figure 2 for identification of critical loops and control components)				
✓	#	Components/Nets	Comments	Page
	1	**Creepage and Clearance** Calculate creepage and clearance requirements according to IEC 60664-1/4.	a) Functional/basic isolation for primary-to-primary b) Reinforced isolation for secondary-to-primary c) Creepage and clearance calculations should be done for all nodes with high voltage between them. See Section 10 for recommended minimum creepage and clearance values d) Ensure pollution degree, altitude of operation, and humidity is considered based on the target application environment.	47
	2	**Control Components (highlighted in Figure 2)** Should be placed as close to the InnoSwitch as possible. Placement should follow the following placement priority: 1) C_{BPP}, C_{BPS}, C_{FWD}, C_{FB} and C_{IS} 2) R_{BIAS} (beside C_{BPP}), R_{FWD} (beside C_{FWD}) 3) R_{FB_LOWER} (beside C_{FB}) and R_{IS} (beside C_{IS}) 4) R_{FB_UPPER}, R_{FF} and C_{FF} 5) Primary and secondary OV components.	a) Ideally, all control components should be on the same layer as the InnoSwitch IC. If this is not possible, ensure priority 1 and 2 components are placed in the same layer as the InnoSwitch b) All secondary control components connected to GND must connect to the IC GND pin through the C_{BPS} pad.	48 to 59
	3	**Control Components Routing** Keep routes between control components short. Avoid vias if possible.	See Section 12 for layout examples.	
	4	**Input CMC** Keep the input and output nodes of the CMC as far away as possible to prevent noise from coupling through the power lines	See Section 12 for layout examples.	
	5	**Input Capacitors** Place input capacitors close to the transformer and InnoSwitch to minimize the primary loop.	If the InnoSwitch and input capacitors are not on the same layer, increase the number of vias connecting the SOURCE pin of the InnoSwitch IC to the capacitors. Do the same for the capacitor to transformer pin connection. See Figure 37a.	
	6	**Snubber Network** Position snubber components close together to minimize the primary snubber loop.	a) The anode of D_{CLAMP} should connect directly to the DRAIN of the InnoSwitch IC b) R_{SN} and C_{SN} should connect directly to the input capacitors, not the transformer HV+ pin. See Section 12.	
	7	**Bias Voltage Components** Place bias components (C_{BIASx}, D_{BIAS}) close to the transformer bias winding pins to minimize the bias loop.	a) Connect the SOURCE/HV- pad of C_{BIAS} directly to the SOURCE/HV- pad of C_{IN} b) Isolate this track from the SOURCE polygon, which carries the primary switching current c) Route V_{BIAS} directly beside or overlapping the C_{BIAS} to C_{BPP} SOURCE/HV- track d) If routed overlapping, these tracks should be on adjacent copper layers. See Section 12.	
	8	**SR FET and Output Capacitors** Place near the secondary transformer pins to minimize the secondary loop area.	a) When parallel FETs are used, place SR FETs close together. b) Ensure SR FETs have adequate copper cooling area to keep SR FET junction temperature within limits. c) If possible, have the cooling area present on all layers. d) Do not overlap the SR FET drain cooling area with other nodes, such as the GND plane, because this node has high dv/dt signals. See Section 12.	

✓	#	Components/Nets	Comments	Page
	9	**SR FET RC Snubber** Place beside the SR FET, preferably on the same layer.	If two SR FETs in parallel are used, place the SR FET RC snubber between the two MOSFETs. See Section 12.	Page 48 to 59
	10	**R_{SENSE} and D_{SENSE}** Position R_{SENSE} to allow the shortest and most direct path to the R_{IS} and C_{IS} pin. D_{SENSE} can be placed beside R_{SENSE}.	a) Protect R_{SENSE} from noisy nodes such as the SR FET drain b) Route the signal from R_{SENSE} to R_{IS} in such a way as to avoid noisy tracks, such as the track from the SR FET drain to R_{FWD} c) Avoid crossing other tracks containing high frequency signals such as the SR gate signal and VOUT.	
	11	**High dv/dt Nodes** Minimize the copper area and track length for the following high dv/dt nodes: a) InnoSwitch DRAIN b) Track from SR FET to R_{FWD} (use lower track width).	Do not overlap high dv/dt nodes with any other node.	
	12	**High di/dt Loops** Aside from tight component placement, routing of high di/dt loops should be done to reduce the area enclosed by the loop. See Figure 2.	a) Large loops can generate large magnetic fields that can couple to nearby conductors. A larger loop will also be susceptible to noise from nearby magnetic fields b) Minimize the length and loop area of the following: Primary loop, Secondary loop, Bias loop, and Primary snubber loop. See Section 12.	
	13	**Reference Planes and Return Paths**	Control signals must always be routed with a well-defined return path. The return path is usually an unbroken GND plane located on the adjacent layer where the signal is routed. Ensure the control signals are routed so the GND plane copper is always directly below the track. If this is not possible, tracks not overlapping a GND plane must be paired with a GND track routed together with the signal track and located on the same layer. See Section 12.	
	14	**Vias**	Signals that go through vias and continue on a layer not adjacent to the signal's original GND plane must be accompanied by a GND via. This via allows the return current to easily transfer to a different GND plane or return path track. See Section 12. Multiple vias are recommended for critical control signals or power lines for reliability. Multiple vias are also recommended for tracks with high current or high di/dt to reduce via resistance and inductance, respectively.	

✓	#	Components/Nets	Comments	Page
	15	**Intersecting Signals**	If unavoidable, signals that intersect and are located on different layers must always have a GND plane between their layers. Ideally, each signal layer must have its own GND plane on an adjacent layer.	Page 48 to 59
	16	**Secondary GND Plane**	The GND plane should connect to the GND pin of the InnoSwitch3-AQ IC only through the BPS pin capacitor GND pad. Multiple vias should be used to reduce the inductance from the GND plane to the GND pin. GND nodes from anywhere else in the circuit can connect directly to the GND plane through a via as long as return paths are well defined and do not intersect. See Section 12 for examples.	
	17	**Signal Measurement Points**	Connect control signals to appropriate measurement points. a) The output voltage (VOUT) signal must be tapped from the pad of the output capacitor b) Tap the SR Drain-Source voltage with a dedicated track from R_{FWD} directly to the drain pad of the SR MOSFET.	

6 PIXIs Design Details

When using the PIXIs tool, it is important to iterate the design until no more warnings are present. Warnings can be addressed by following the guidance given in the right most column of the spreadsheet. Once all warnings are cleared, use the magnetics designer tool to optimize the transformer and then generate the design documents that can be used to create a prototype transformer.

6.1 Application Variables and Operating Conditions

Enter the desired output voltage and the target output power for each input voltage set point. Up to 9 operating conditions can be specified and PIXIs will attempt to solve for a design that will satisfy all operating points. Figure 3 shows the Application Variables section of the PIXIs for InnoSwitch3-AQ devices.

For power supplies with a specified operating input range but has output power requirements below the minimum, it is recommended to enter only the nominal range in the Operating Conditions fields and then use Set-point Analysis to evaluate the design at lower input voltages. See the Set-point Analysis section for an example.

PIXIs Designer | Magnetics Designer

	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
	APPLICATION VARIABLES					Design Title
3	VOUT	12.00		12.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	5.000		5.000	A	Output current 1
7	POUT1			60.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
10						
11	**OPERATING CONDITION 2**					
12	VINDC2	300.00		300.00	V	Input DC voltage 2
13	IOUT2	5.000		5.000	A	Output current 2
14	POUT2			60.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
17						
18	**OPERATING CONDITION 3**					
19	VINDC3	60.00		60.00	V	Input DC voltage 3
20	IOUT3	0.500		0.500	A	Output current 3
21	POUT3			6.00	W	Output power 3
22	EFFICIENCY3			0.85		Converter efficiency for output 3
23	Z_FACTOR3			0.50		Z-factor for output 3

Figure 3. Enter the Desired VOUT and Output Power for Each Corresponding Input Voltage.

Notes:

1. **VOUT** – Recommended VOUT range is from 5 VDC to 24 VDC
   - The InnoSwitch3-AQ VOUT pin has an absolute maximum voltage of 27 V. For designs requiring outputs >24 VDC, please contact Power Integrations customer support.
2. **VINDC** – Maximum input voltage is 1100 VDC while the minimum is 30 VDC**.**
3 **EFFICIENCY** – Use the default values for the first iteration of the design. This can be adjusted to match bench measurements once a prototype is available.
4. **Z-FACTOR** – Power Supply Loss Allocation Factor – Equal to the ratio of the losses in the secondary-side over the total converter losses. Use the default value for IOUT of 3 A and below. A value of 0.65 can be used for higher output currents. If there is a need to optimize calculations, a power loss budget measured from the prototype can be used to determine the actual secondary losses, and the Z-factor can be iterated in the spreadsheet**.**
5. If line undervoltage protection is disabled (V pin shorted to SOURCE pin), the power supply will start to operate at 30 VDC input. Use the INPUT VOLTAGE SET-POINT ANALYSIS section of the PIXIs to determine the expected maximum output power at this operating point.
6. For wide-range input designs (e.g., 30 VDC to 1000 VDC), higher power requirements at the minimum input voltage will limit the maximum output power at higher input voltages due to increased switching losses (deep DCM operation at high input voltage, no valley switching, higher switching frequency).
7. It is not necessary to fill up all operating conditions fields. Required power at the minimum and maximum input voltages will suffice.

6.2 Primary Controller Selection

Use the Table 1 InnoSwitch3-AQ Output Power Table to select the appropriate InnoSwitch3-AQ IC for the design.

Adjust the DEVICE_CODE field to the chosen InnoSwitch3-AQ device. For the ILIMIT_MODE, select between STANDARD or INCREASED.

In general, INCREASED current limit is selected when designing near the maximum power capability of the device or when higher power is needed in the lower input ranges of the design.

The primary controller selection section is shown in Figure 4. Upon selecting the current limit and device code, the device's characteristics are listed in the succeeding cells based on data sheet values.

Design Notes:

1. It is possible to design for higher power versus the values stated in the power table if thermal management measures are implemented to keep the package temperature below 125 °C.
2. Always estimate the total power loss in the device (switching + conduction losses) to appropriately size the cooling copper area of the SOURCE node.
3. Refer to the InnoSwitch3-AQ data sheet for information on the devices' thermal impedance and Drain-Source capacitance.

Output Power Table

Product[2]	Maximum Recommended Input DC Rail	Output Power (W) At Working Voltage[1]			
750 V MOSFET		30 VDC	60 VDC	400 VDC	800 VDC
INN3977CQ	520 V	10	20	30	–
900 V MOSFET		30 VDC	60 VDC	400 VDC	800 VDC
INN3996CQ	650 V	7	14	20	–
900 V PowiGaN Switch		30 VDC	60 VDC	400 VDC	800 VDC
INN3997CQ[3]	650 V	10	20	55	–
INN3999CQ[3]	650 V	10	30	85	–
INN3990CQ[3]	650 V	10	40	100	–
1700 V SiC Switch		30 VDC	60 VDC	400 VDC	800 VDC
INN3947CQ	1200 V	10	23	50	50
INN3949CQ	1200 V	10	40	70	70

Table 1. Output Power Table.

Notes:
1. Maximum output power is dependent on the design. Power delivery is calculated assuming that package temperature must be < 125 °C and that the design uses suitable thermal strategies (e.g. PCB copper area and/or a thermal interface to enclosure).
2. Packages: InSOP-24D.
3. UL, TUV, CQC approvals are pending. AEC qualification completion in process.
4. Transients may exceed this value.

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DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
APPLICATION VARIABLES					Design Title
68					
PRIMARY CONTROLLER SELECTION					
70 ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
71 VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72 DEVICE_GENERIC			INN39X9		Device selection
73 DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74 PDEVICE_MAX			70	W	Device maximum power capability
75 RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25°C
76 RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125°C
77 ILIMIT_MIN			1.981	A	Primary switch minimum current limit
78 ILIMIT_TYP			2.130	A	Primary switch typical current limit
79 ILIMIT_MAX			2.279	A	Primary switch maximum current limit
80 VDRAIN_ON_PRSW			0.24	V	Primary switch on-time voltage drop
81 VDRAIN_OFF_PRSW			1180	V	Peak drain voltage on the primary switch during turn-off

Figure 4. InnoSwitch3-AQ Device and Current Limit Setting in the Primary Controller Selection Section of PIXIs.

6.3 Worst-Case Electrical Parameters

Most iterations will be done in this spreadsheet section until a suitable transformer design is achieved. For the first iteration of the design, the default values of FSWITCHING_MAX, VOR, and LPRIMARY_TOL can be used. Once a transformer core is selected, the user can adjust the value of these variables until PIXIs clears all warnings.

FSWITCHING_MAX

This parameter is the target maximum operating switching frequency of the design. It accounts for all operating points and is evaluated at full load. The maximum switching frequency of the InnoSwitch3-AQ IC during normal operation is 100 kHz, while the typical overload detection frequency is 110 kHz. During normal operating conditions, the switching frequency at full load should be at least 10% below the overload detection frequency.

Below are the suggested 1st iteration FSWITCHING_MAX values:

Input Voltage Range	Output Power	SWITCHING_MAX 1st Iteration
30 V to 1000 V	≤ 35 W	30 kHz to 45 kHz
400 V DC BUS	≥ 60 W	65 kHz
	≤ 60 W	85 kHz
800 V DC BUS	≥ 35 W	35 kHz
	≤ 35 W	45 kHz

Table 2. Suggested Maximum Frequency Values for 1st Design Iteration.

Generally, the maximum switching frequency can be set higher if the input voltage range is smaller since valley switching will be possible throughout the whole input range. This will allow for lower switching losses even at high frequencies.

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
▸	APPLICATION VARIABLES					Design Title
68						
▸	PRIMARY CONTROLLER SELECTION					
84						
▾	WORST CASE ELECTRICAL PARAMETERS					
86	FSWITCHING_MAX	70000	Info	70000	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
87	VOR	150.0		150.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			1.657		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.232		Primary switch duty cycle
91	TIME_ON_MIN			0.98	us	Minimum primary switch on-time
92	TIME_ON_MAX			11.22	us	Maximum primary switch on-time
93	TIME_OFF			11.01	us	Primary switch off-time
94	LPRIMARY_MIN			516.6	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			543.8	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			571.0	uH	Maximum primary magnetizing inductance
98						
99	PRIMARY CURRENT					
100	IAVG_PRIMARY			0.218	A	Primary switch average current
101	IPEAK_PRIMARY			2.113	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			2.113	A	Primary switch ripple current
104	IRMS_PRIMARY			0.554	A	Primary switch RMS current

Figure 5. Worst-Case Electrical Parameters for the User's Operating Conditions.

V_{OR} (Reflected Output Voltage)
V_{OR} is the voltage seen across the primary winding during the SR FET conduction time. It is approximately equal to the output voltage multiplied by the transformer turns ratio and is a user-defined parameter used by PIXIs in its design calculations.

$$V_{OR} = \frac{N_P}{N_S} V_{OUT}$$

where

N_P = primary turns

N_S = secondary turns

The V_{OR} affects multiple critical design parameters relating to the transformer design and SR FET selection and can thus be used to keep said parameters within limits. The V_{OR} can also be fine-tuned to remove warnings in the spreadsheet. For optimization purposes, the following factors should be considered:

- Higher V_{OR} allows increased power delivery at minimum input voltage.
- Higher V_{OR} reduces the voltage stress on the output diodes or SR FETs, which may allow the use of a lower voltage rated SR FET.
- Higher V_{OR} generally results in a larger leakage inductance, reducing power supply efficiency.
- Higher V_{OR} increases peak and RMS current on the secondary side, which may increase secondary-side copper, diode and SR FET losses.

There are exceptions to the guidance above, such as for designs with very high output currents where the V_{OR} should be reduced to obtain the highest efficiency.

Higher output voltage (above 15 V) designs should use higher V_{OR} to keep the voltage stress across the SR FET within acceptable limits. Higher V_{OR} is often also necessary for designs with high-voltage inputs (>600 V).

The optimal selection of the V_{OR} value depends on the specific application and is based on a compromise between the above mentioned factors.

When the Application Variables and Primary Controller Selection have been finalized, FSWITCHING_MAX and V_{OR} are the parameters that primarily determine the primary inductance in the spreadsheet.

K_P (Mode of Operation)
K_P is a measure of how discontinuous or continuous the primary current waveform is for a specific operating point. K_P below 1 indicates CCM operation, while K_P above 1 indicates DCM operation.

Each set-point in the design will correspond to a specific K_P value. Some set-points may result in CCM operation, while others could be in DCM. The K_P shown in the worst-case electrical parameters section of PIXIs corresponds to the design's most CCM operation (smallest K_P value).

The value of K_P should be in the range of $0.5 < K_P < 6$. Testing across multiple designs has shown that a K_P value between 0.6 and 1.0 results in the highest efficiencies across all output and load conditions.

Primary Inductance Tolerance, LPRIMARY_TOL (%)
This parameter is the assumed primary inductance tolerance. A value of 5% is used by default. If the transformer vendor provides this information, this may be overridden.

A value of 7% can be easily achieved and is a reasonable value for most magnetics vendors. A value of 3% will help improve production tolerance but will be more challenging to mass produce. Designing for 5% tolerance is recommended since it results in lower unit-to-unit variation for efficiency and is easy for most magnetics manufacturers to achieve.

The spreadsheet automatically calculates the other electrical parameters in this section. It can be used to select the other components in the circuit, such as the input CMC, output rectifier (SR FET), and output capacitors.

Primary Current
IPEAK_PRIMARY – Peak primary current
IPEDESTAL_PRIMARY – Primary MOSFET current at the start of a switching cycle in CCM
IAVG_PRIMARY – Primary MOSFET average current
IRIPPLE_PRIMARY – Primary MOSFET ripple current
IRMS_PRIMARY – Primary MOSFET RMS current

VOUT (V)	400 V BUS (900 V Device)		800 V BUS (1700 V Device)	
	V_{OR} (V)	Required SR FET BV_{DSS} (V)	V_{OR} (V)	Required SR FET BV_{DSS} (V)
5	50	80	60	120
8	80		100	
12	120	100	150	
15	150		190	
18	180		225	
24	240		280	150

Table 3. Suggested 1st Iteration V_{OR} Values for Different Operating Conditions.

6.4 Transformer Construction Parameters

Inputs: CORE, AE, LE, AL, VE, BOBBIN, AW, BW, MARGIN

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
	TRANSFORMER CONSTRUCTION PARAMETERS					
109	**CORE SELECTION**					
110	CORE	EQ30		EQ30		Core selection
111	CORE NAME			EQ30-3C96		Core code
112	AE			108.0	mm^2	Core cross sectional area
113	LE			46.0	mm	Core magnetic path length
114	AL			4900	nH	Ungapped core effective inductance per turns squared
115	VE			4970	mm^3	Core volume
116	BOBBIN NAME			EQ30 - 1 (P5-S5)		Bobbin name
117	AW			60.1	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW			8.40	mm	Bobbin width
119	BH			7.15	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
121						
122	**PRIMARY WINDING**					
123	NPRIMARY			38		Primary winding number of turns
124	BPEAK			3245	Gauss	Peak flux density
125	BMAX			2899	Gauss	Maximum flux density
126	BAC			1450	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			377	nH	Typical gapped core effective inductance per turns squared
128	LG			0.333	mm	Core gap length
129						
130	**SECONDARY WINDING**					
131	NSECONDARY			3		Secondary winding number of turns
132						
133	**BIAS WINDING**					
134	NBIAS			3		Bias winding number of turns

Figure 6. PIXIs Transformer Construction Parameters Section.

CORE

By default, if the core-type cell is left empty, the spreadsheet will select the smallest available core in its database suitable for the continuous (average) output power specified. If a user prefers to use a core not included in the database, the area product method can set the minimum criteria for core selection. The formula for the area product (A_P) is given below:

$$A_P = A_E A_W = \frac{L_{PRI} I_{PK(PRI)} \sum_I \frac{N_I}{N_{PRI}} I_{RMS(I)}}{B_{MAX} J K}$$

where

A_P = core area product
A_E = core effective area
A_W = core winding area
L_{PRI} = nominal primary inductance (LPRIMARY_TYP)
$I_{PK(PRI)}$ = primary peak current (IPEAK_PRIMARY)
N_I = secondary turns for winding i (NSECONDARY)
N_{PRI} = primary turns (NPRIMARY)
$I_{RMS(I)}$ = RMS current for output winding i
B_{MAX} = desired maximum flux density (core material specification)
J = winding current density (4-6 A/m^2)
K = winding fill factor (0.5 to 0.8)

For the current density, lower values will result in higher efficiency due to lower copper loss but might require a larger winding area. The winding factor is the ratio of the copper to non-copper regions of the winding area cross-section. Lower values will be easier to manufacture.

The formula can be modified to use V_{OUT} and V_{OR} when calculating for a single output design:

$$A_P = A_E A_W = \frac{L_{PRI} I_{PK(PRI)} \left(\frac{V_{OUT}}{V_{OR}} \right) I_{RMS(SEC)}}{B_{MAX} J K}$$

where

$I_{RMS(SEC)}$ = secondary RMS current at full load (see Step 5)

The A_p of the chosen core should be greater than or equal to the value computed above. Once a custom core is selected, enter its parameters in PIXls with its corresponding bobbin's window area and width. Ensure B_{MAX} is well below the core material's saturation level at any temperature.

The core's thermal impedance (R_{TH}) must first be determined to compute for transformer temperature rise. The R_{TH} can be taken from the core's manufacturer data sheet or estimated using the equation below:

$$R_{TH} = 53 \times (V_{CORE})^{-0.54} \text{in} \frac{K}{W}$$

where

V_{CORE} = core volume in cm^3 (data sheet value)

Once the thermal impedance is found, the transformer temperature rise can be estimated by taking the transformer loss from the Windings Info window in the PIXls Magnetics Designer tab (see Figure 9). Temperature rise can be calculated as follows:

$$T_{RISE(TRANSFORMER)} = R_{TH} \times P_{TOTAL(TRANSFORMER)LOSS} \text{ in } ^\circ C$$

Note that the value calculated here is only an estimate of the average temperature rise of the transformer and must be verified through testing. In addition, windings are expected to have a temperature rise of around 10 – 15 °C higher than the average.

MARGIN (Safety Margin, mm)
This section can be set to 0 mm since transformer designs for automotive applications typically require the use of triple-insulated wires for the secondary to pass reinforced isolation and partial discharge requirements. Using fully insulated wires (FIW) in the primary is recommended.

NPRIMARY
This is the number of turns needed for the main primary winding of the transformer, calculated based on V_{OR} and secondary turns.

BPEAK
A maximum value of 3800 Gauss is recommended to limit the peak flux density at the maximum current limit and 132 kHz operation. During an output-short condition, the output voltage is almost zero, and minimal reset of the transformer occurs during the FET off-time. This could cause the transformer flux density to "staircase" beyond the normal operating level. A value of 3800 Gauss at the selected device's maximum current limit and built-in protection features of the InnoSwitch3-AQ provides sufficient margin to prevent core saturation under output short-circuit conditions.

BMAX
Low-frequency operation during light load conditions can generate frequencies in the audible range within the transformer, especially if a long core is used. To limit audible noise, the transformer should be designed such that the maximum core flux density is below 3000 Gauss (300 mT). This guideline and dip varnishing can significantly attenuate audible noise.

BAC
The AC flux density can be used for calculating core loss.

NSECONDARY
The minimum number of secondary turns such that the peak operating flux density, BPEAK, is kept below the recommended maximum of 3800 Gauss (380 mT). In general, entering a number in the override cell is unnecessary except in designs where a lower operating flux density is desired.

6.5 Primary and Secondary Components Selection

Inputs: UVOV Type, BROWN-IN REQUIRED, UNDERVOLTAGE ZENER DIODE, SRFET1

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5 PRIMARY COMPONENTS SELECTION	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
139	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
140	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
141	**UNDERVOLTAGE PARAMETERS**					
142	BROWN-IN REQUIRED	58.00		58.00	V	Required DC bus brown-in voltage threshold
143	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
144	VZ			9.10	V	Zener diode reverse voltage
145	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
146	ILKG			2.00	uA	Zener diode maximum reverse leakage current
147	BROWN-IN ACTUAL			44.31 - 57.15	V	Actual brown-in voltage range using standard resistors
148	BROWN-OUT ACTUAL			37.98 - 51.07	V	Actual brown-out voltage range using standard resistors
149	**OVERVOLTAGE PARAMETERS**					
150	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
151	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
152	VF				V	OV diode forward voltage
153	VRRM				V	OV diode reverse voltage
154	PIV				V	OV diode peak inverse voltage
155	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
156	**DC BUS SENSE RESISTORS**					
157	RLS_H			1.62	MΩ	Connect five 324 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
158	RLS_L			261	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
159						
160						
161	**BIAS WINDING**					
162	VBIAS			9.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			87.95	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	uF	Bias winding rectification capacitor
166	CBPP			4.70	uF	BPP pin capacitor

Figure 7. Primary Components Selection Section.

UVOV Type
Selection field for desired input lockout mode. Check the InnoSwitch3-AQ IC if the device chosen in Step 4 supports UV, OV, or both. For automotive applications with very high input voltages, either this feature is not used, or UV Only mode is selected. If unused, connect the V pin to the SOURCE node of the InnoSwitch3-AQ and ignore the UNDERVOLTAGE PARAMETERS, OVERVOLTAGE PARAMETERS, and DC BUS SENSE RESISTORS section of the spreadsheet.

BROWN-IN REQUIRED
This is the input DC voltage at which the power supply will turn on if UV lockout is enabled. Typically set to 30 V for emergency power supply applications.

UNDERVOLTAGE ZENER DIODE
A Zener diode is used to clip the voltage across the V pin when the input voltage increases far above the brown-in value, as shown in Figure 8. This effectively disables OV detection by limiting the current entering the V pin when past the brown-in value. Select a diode from the drop-down menu and calculate the power dissipation in the Zener when the input voltage is at a maximum. Ensure power derating requirement is satisfied.

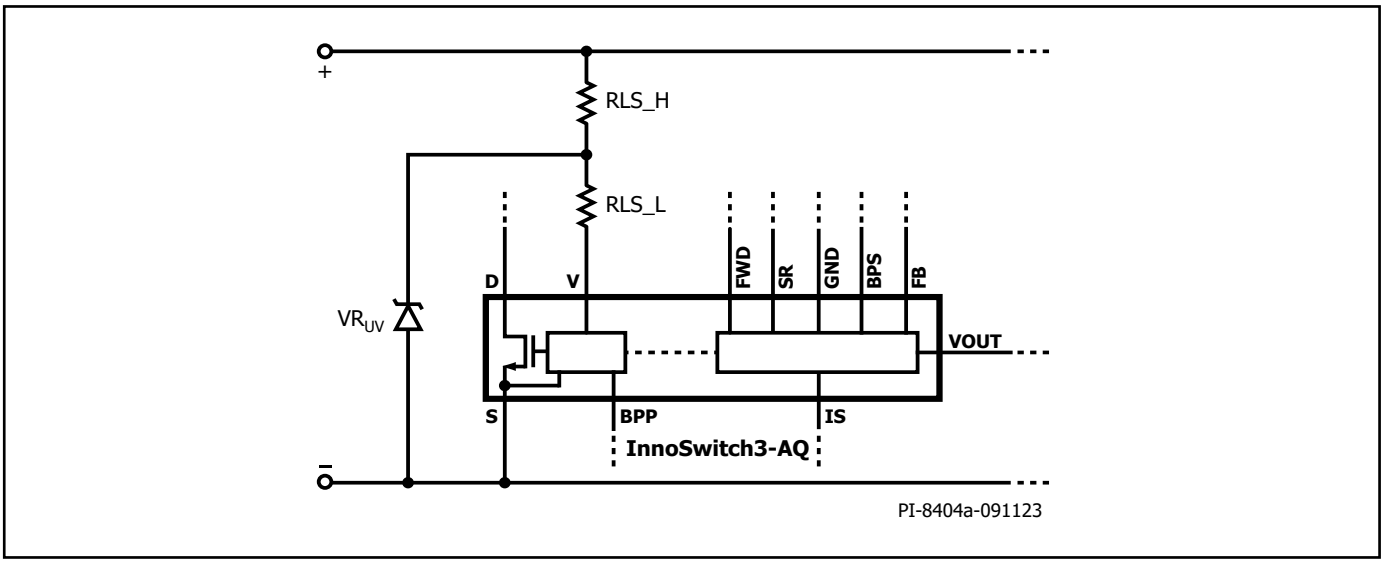

Figure 8. Circuit to Clamp the V Pin for Input Line UV-Only Protection.

RLS_H and RLS_L (DC BUS Sense Resistors)
PIXIs automatically calculates RLS_H and RLS_L according to the desired UV voltage level. RLS_H is the total resistor value needed to enable the InnoSwitch3-AQ IC at the desired brown-in voltage. This value should be split into multiple resistors for high input voltage applications to meet the resistor's power rating, voltage rating, and clearance, creepage requirements.

VBIAS
The rectified bias voltage is based on the number of bias winding turns calculated in Section 7.4. It is recommended not to override this value.

VF_BIAS

PIXIs uses a value of 0.7 V by default. This can be changed to match the forward voltage of the actual diode used to rectify the output from the bias winding.

FEEDBACK COMPONENTS (RFB_UPPER, RFB_LOWER, CFB_LOWER)
PIXIs automatically calculates the output feedback network to meet the desired output regulation voltage. It is recommended that these values be used as is.

SRFET
Several synchronous rectifier MOSFETs (SR FET) are provided in the drop-down menu. The breakdown voltage (VBREAKDOWN_SRFET) and on-time drain resistance (RDSON_SRFET) of the selected SR FET will be displayed in the spreadsheet.

If the desired MOSFET to be used is not on the list, selection of the SR FET should follow the criteria set in Section 9.4.

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DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
SECONDARY COMPONENTS SELECTION					
171 FEEDBACK COMPONENTS					
172 RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
173 RFB_LOWER			11.80	kΩ	Lower feedback resistor
174 CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor

Figure 9. Secondary Components Selection (Feedback Network).

6.6 Magnetics Designer

At this stage, the transformer can be evaluated using the Magnetics Designer tab in PIXls. Within the Magnetics Designer are windows that allow adjustments to the transformer design or generate documentation files. Figure 10 shows the Magnetics Designer tab and detail windows. The functions of each window are detailed here:

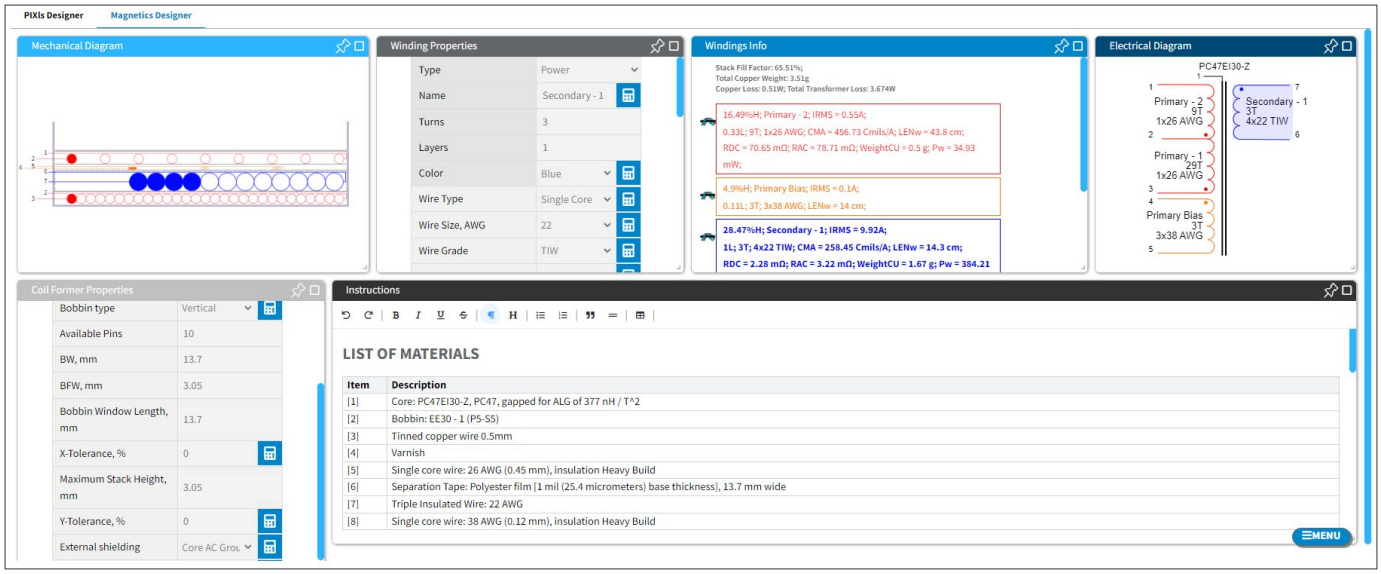

Figure 10. PIXls Magnetics Designer Window.

Mechanical Diagram
This window shows the cross-sectional view of half of the bobbin winding area. The image is a visual guide for whoever builds the transformer on the winding order and direction, location and the number of tape layers needed, and the pin where each winding terminates. The image also illustrates the current fill factor of the transformer and gives the designer an idea of construction complexity.

Windings Info
This section displays the calculated worst-case values of current density, RMS current, and power loss. Parameters such as DC resistance, AC resistance, and estimated wire length needed for each specific winding are also shown. The top section of this window displays the worst-case core loss, copper loss, and fill factor. Together with the mechanical diagram, the information from this window gives essential information on the manufacturability of the transformer design.

Winding Properties
This window allows the user to change the type and number of wires used in each winding used in the design. Clicking a winding in the Electrical Diagram window will display said winding's properties in this window. Optimization can be done here by adjusting the wire properties and checking the results in the Windings Info window. This is especially true if copper loss constitutes most of the transformer losses.

Electrical Diagram
Electrical diagram of the transformer design. Click a specific winding to see its information in the Winding Properties window.

Coil Former Properties
Window showing information on the coil former used.

Instructions
Once the transformer design is finalized, PIXls automatically generates a set of instructions on how to build the transformer. This can be used to guide manufacturers or added to design documentation. Aside from build instructions, the BOM for the transformer is also included here.

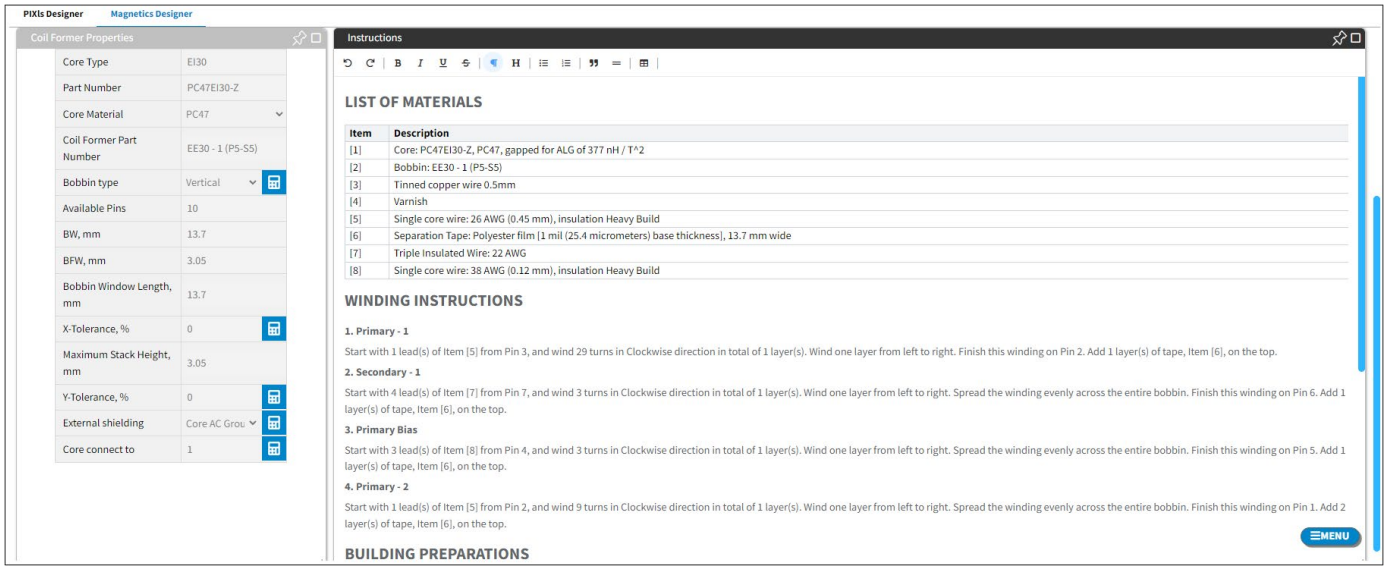

Figure 11. Magnetics Builder Instructions Window.

6.7 Input Voltage Set-points Analysis

Inputs: USER_VINDC, USER_ILIMIT, USER_LPRIMARY, POUT, EFIFICIENCY, Z_FACTOR
In this section, the designer can simulate the resulting primary current, flux density, and switching frequency as a function of input voltage, output power, InnoSwitch3-AQ current limit, and inductor value. This section can be used to determine worst-case values of primary current, frequency, and flux density, which are relevant in other areas of the design, such as calculation and sizing of the input filters, snubber design, component selection, and PCB layout. This section is also helpful when verifying the peak power capability of the design at very low input voltages.

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
	INPUT VOLTAGE SET-POINTS ANALYSIS					
224	**TOLERANCE CORNER**					
225	USER_VINDC	1000		1000	V	Input DC voltage corner to be evaluated
226	USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
227	USER_LPRIMARY	TYP		543.8	uH	Primary inductance corner to be evaluated
228						
229	**OPERATING CONDITION SELECTION**					
230	POUT			60.00	W	Output power to be evaluated
231	EFFICIENCY			0.85		Converter efficiency to be evaluated
232	Z FACTOR			0.50		Z-factor to be evaluated
233	FSWITCHING			60259	Hz	Maximum switching frequency at the output power to be evaluated
234	KP			2.143		Measure of continuous/discontinuous mode of operation
235	MODE_OPERATION			DCM		Mode of operation
236	DUTYCYCLE			0.065		Primary switch duty cycle
237	TIME_ON			1.086	us	Primary switch on-time
238	TIME_OFF			15.509	us	Primary switch off-time
239						
240	**PRIMARY CURRENT**					
241	IAVG_PRIMARY			0.065	A	Primary switch average current
242	IPEAK_PRIMARY			1.996	A	Primary switch peak current
243	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
244	IRIPPLE_PRIMARY			1.996	A	Primary switch ripple current
245	IRMS_PRIMARY			0.295	A	Primary switch RMS current
246						
247	**MAGNETIC FLUX DENSITY**					
248	BPEAK			2811	Gauss	Peak flux density
249	BMAX			2574	Gauss	Maximum flux density
250	BAC			1287	Gauss	AC flux density (0.5 x Peak to Peak)
251						
252						

Figure 12. PIXls Input Voltage Set-Point Analysis Section.

6.7.1 Estimating InnoSwitch3-AQ Temperature Rise

It is recommended that the temperature rise of the InnoSwitch3-AQ IC be estimated before proceeding with the design to check that InnoSwitch3-AQ IC will not go into OTP across all operating conditions. The method for estimating temperature rise is outlined below.

Important Notes When Estimating Temperature Rise:

a. For very wide input voltage range designs (e.g., 30 VDC to 1000 VDC input voltage designs), the calculation of losses and temperature rise should be done at the highest input voltage and maximum output load. This is because, for wide-range designs, the converter is deep into DCM at the higher input voltages that valley switching no longer occurs. Consequently, the total InnoSwitch3-AQ loss will be dominated by switching losses.

b. For designs with a relatively small input range (e.g., 150 VDC to 500 VDC), worst-case losses tend to be at the minimum input voltage because valley switching lowers switching losses and conduction losses dominate. Losses can also be higher if the converter operates in CCM at lower input voltages. Therefore, temperature rise calculations should be done at the minimum input voltage and maximum output load.

Steps to Estimate InnoSwitch3-AQ Temperature Rise

1. **Get data from PIXIs for the Desired Operating Condition using Set Point Analysis**
   Relevant data are the switching frequency (Line 233), primary RMS current (Line 245), and the input voltage (Line 225).
   For the example in Figure 12, we get the following data:

   FSWITCHING: 60256 Hz
   IRMS_PRIMARY: 0.295 A
   Input Voltage: 1000 V (at 1000 V unit is in deep DCM, so no valley switching occurs)

2. **Check the Drain Capacitance Power Plots for the InnoSwitch3-AQ Device Used and Estimate the Switching Loss**
   The drain capacitance power curves shown in Figure 13 are for a switching frequency of 100 kHz. The switching loss for a specific operating point can be estimated by scaling the value from the plot according to the operating point switching frequency.

$$P_{LOSS(INNOSWITCHING)} = \frac{FSWITCHING}{100\ kHZ} \times \text{Drain Capacitance Power at } V_{IN}$$

For the operating point in (1), the switching loss is found to be (see Figure 13)

$$P_{LOSS(INNOSWITCHING)} = \frac{60.256\ kHz}{100\ kHZ} \times 580\ mW = 349.5\ mW$$

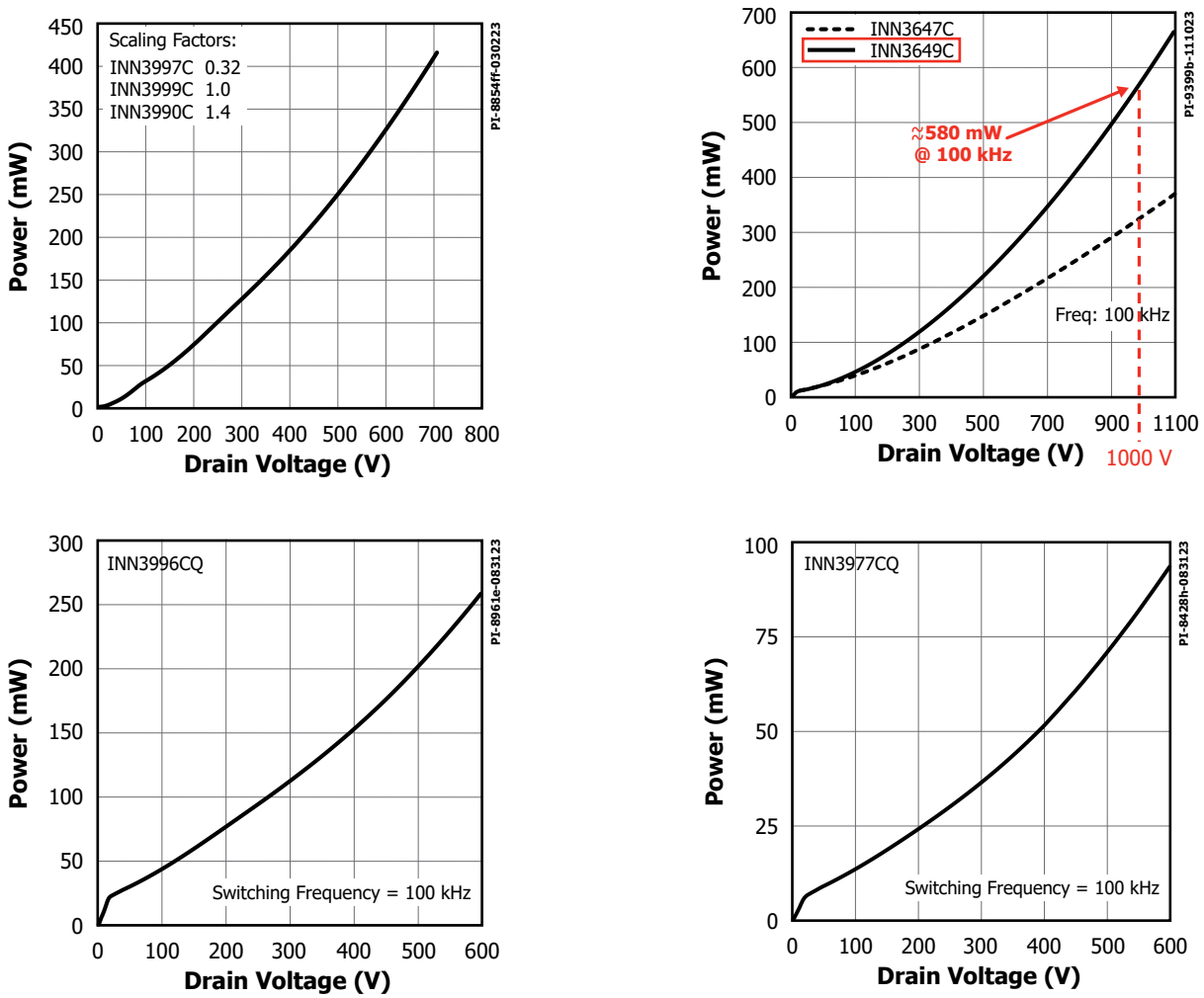

Figure 13. Drain Capacitance Power at 100 kHz for Various Devices from the InnoSwitch3-AQ Family of ICs.

3. **Check Line 76 of PIXIs to get the $R_{DS(ON)}$ of the InnoSwitch3-AQ Device at 125 °C**

   For the INN3949CQ, $R_{DS(ON)MAX}$ = 1.1 Ω

4. **Calculate Power Total Power Loss Using the Following Equations:**

$$P_{LOSS(INNO)} = P_{LOSS(INNOSWITCHING)} + P_{LOSS(INNOCONDUCTION)}$$

$$P_{LOSS(INNO)} = P_{LOSS(INNOSWITCHING)} + I_{PRI(RMS)}^2 R_{DS(ON)MAX}$$

using our example, we get

$$P_{LOSS(INNO)} = 349.5\ mW + (0.295)^2(1.1) = 349.5\ mW + 95.7\ mW$$

$$P_{LOSS(INNO)} = 445.2\ mW$$

5. **Calculate Thermal Rise Using R_{TH} from the Data Sheet**
   The data sheet specifies thermal resistance information for the InnoSwitch for specific copper cooling area connected to the SOURCE pin. Assuming a 1 square inch cooling area, the junction-ambient thermal resistance is $R_{TH(JA)}$ = 70 °C/W.

   For a loss of 445.2 mW, the temperature rise of the InnoSwitch3-AQ IC will be:

$$T_{RISE} = R_{TH(JA)} P_{LOSS(INNO)} = 70 \times 0.4452 = 31.16\ °C$$

The junction temperature at 25 °C ambient will be

$$T_J = T_{AMB} + T_{RISE} = 25 + 31.16 = 56.16\ °C$$

At 105 °C ambient, the estimated temperature rise will be

$$T_J = T_{AMB} + T_{RISE} = 105 + 31.16 = 136.16\ °C$$

Which is still below the thermal shutdown limits of the InnoSwitch3-AQ IC (T_{SD} = 142 °C). All thermal calculations must be verified during bench testing.

Thermal Resistance

Thermal Resistance: INN3977CQ, INN3996CQ, INN3997CQ, INN3999CQ and INN3990CQ
(θ_{JA})..... 76 °C/W[1], 65 °C/W[2]
(θ_{JC})..... 8 °C/W[3]
INN3947CQ
(θ_{JA})..... 92 °C/W[1], 64 °C/W[2]
(θ_{JC})..... 19 °C/W[3]
INN3949CQ
(θ_{JA})..... 76 °C/W[1], 70 °C/W[2]
(θ_{JC})..... 11 °C/W[3]

Notes:
1. Soldered to 0.36 sq.inch (232 mm²) 2 oz.(610 g/m²) copper clad.
2. Soldered to 1 sq.inch (645 mm²), 2 oz.(610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.

Figure 14. Thermal Resistance of InnoSwitch3-AQ Devices for Given Copper Cooling Area.

6.7.2 Estimating Maximum Peak Power at Minimum Input Voltage

As mentioned earlier, PIXIs works to find a solution to satisfy all operating conditions specified in the Application Variables section of the tool. This means that across all operating and loading conditions, as well as all tolerance corners, PIXIs will find a solution that will allow the InnoSwitch3-AQ ICs to control the output using the InnoSwitch3-AQ's variable current limit-variable frequency control scheme. In general, for a given input voltage and loading combination, variable current limit-variable frequency control is operational if the INFO fields of TIME_ON (PIXIs Row 237) and TIME_OFF (PIXIs Row 238) do not show any "Info" or "Warning" flags. If a "Warning" is issued, the converter will not be able to deliver the required power for that specific condition. Thus, said condition is outside of the converter's operating range. However, an "Info" message in the TIME_ON row could mean that the converter can still regulate the output at the desired loading condition.

An "Info" flag in the TIME_ON row means the controller has transitioned from variable current limit-variable frequency control to fixed on-time control. The controller fixes the on-time of the InnoSwitch3-AQ IC to as low as 11.75 µs and controls the output by increasing the frequency to deliver more power. This can be helpful when evaluating a design to check its peak power capability at the minimum input voltage limit or lower up to 30 VDC.

For example, the design in Figure 3 requires 6 W at 60 VDC input. However, using Set-point Analysis, we can see that at 60 V input, the converter can still deliver up to 55 W shown in Figure 15. Further increasing the output power to 56 W (Figure 16) causes PIXIs to issue a warning for TIME_OFF, which means the output can no longer be regulated at this condition.

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5 INPUT VOLTAGE SET-POINTS ANALYSIS	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
224	TOLERANCE CORNER					
225	USER_VINDC	60		60	V	Input DC voltage corner to be evaluated
226	USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
227	USER_LPRIMARY	TYP		543.8	uH	Primary inductance corner to be evaluated
228						
229	OPERATING CONDITION SELECTION					
230	POUT	53.00		53.00	W	Output power to be evaluated
231	EFFICIENCY			0.85		Converter efficiency to be evaluated
232	Z FACTOR			0.50		Z-factor to be evaluated
233	FSWITCHING			61104	Hz	Maximum switching frequency at the output power to be evaluated
234	KP			0.637		Measure of continuous/discontinuous mode of operation
235	MODE_OPERATION			CCM		Mode of operation
236	DUTYCYCLE			0.718		Primary switch duty cycle
237	TIME_ON		Info	11.750	us	Primary switch on-time has been capped at 11.75us and the controller switching frequency has increased as a result
238	TIME_OFF			4.616	us	Primary switch off-time

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5 INPUT VOLTAGE SET-POINTS ANALYSIS	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
224	TOLERANCE CORNER					
225	USER_VINDC	60		60	V	Input DC voltage corner to be evaluated
226	USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
227	USER_LPRIMARY	TYP		543.8	uH	Primary inductance corner to be evaluated
228						
229	OPERATING CONDITION SELECTION					
230	POUT	55.00		55.00	W	Output power to be evaluated
231	EFFICIENCY			0.85		Converter efficiency to be evaluated
232	Z FACTOR			0.50		Z-factor to be evaluated
233	FSWITCHING			64482	Hz	Maximum switching frequency at the output power to be evaluated
234	KP			0.597		Measure of continuous/discontinuous mode of operation
235	MODE_OPERATION			CCM		Mode of operation
236	DUTYCYCLE			0.718		Primary switch duty cycle
237	TIME_ON			11.137	us	Primary switch on-time
238	TIME_OFF			4.372	us	Primary switch off-time

Figure 15. Set-Point Analysis at 60 V Input, 53 W and 55 W Output Power is Possible but must be Evaluated for Thermal Performance.

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DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
INPUT VOLTAGE SET-POINTS ANALYSIS					
224 TOLERANCE CORNER					
225 USER_VINDC	60		60	V	Input DC voltage corner to be evaluated
226 USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
227 USER_LPRIMARY	TYP		543.8	uH	Primary inductance corner to be evaluated
228					
229 OPERATING CONDITION SELECTION					
230 POUT	56.00		56.00	W	Output power to be evaluated
231 EFFICIENCY			0.85		Converter efficiency to be evaluated
232 Z FACTOR			0.50		Z-factor to be evaluated
233 FSWITCHING			66356	Hz	Maximum switching frequency at the output power to be evaluated
234 KP			0.578		Measure of continuous/discontinuous mode of operation
235 MODE_OPERATION			CCM		Mode of operation
236 DUTYCYCLE			0.718		Primary switch duty cycle
237 TIME_ON			10.823	us	Primary switch on-time
238 TIME_OFF		Warning	4.247	us	Primary switch off-time is less than 4.37us. The device will not be able to deliver the output power

Figure 16. Set-point Analysis at 60 V Input, 56 W Output – Warning Flag for TIME_OFF Means Output Cannot be Regulated.

6.7.3 Alternative Design Method for Converters with Power Requirements at Low Input Voltages

Sometimes it may be challenging to generate a viable design that requires a specific amount of power at very low input voltages. For this, it is recommended to calculate a design using only the nominal input range from the specifications as input to the Application Variables section of PIXls and then use the Set-point Analysis section to check if the power requirements can be met at lower voltages.

As an example, a power supply design has the following power requirements:

1. Input voltage: 30 VDC to 900 VDC – however nominal input voltage range is only from 300 VDC to 900 VDC.
2. Output voltage: 15 VDC.
3. Output power: 15 W across the whole input range (30 VDC to 900 VDC).

Instead of calculating a solution using 30 VDC to 900 VDC as input, we omit the 30 VDC operating condition and only use the 300 VDC to 900 VDC operating conditions in PIXIs:

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
	APPLICATION VARIABLES					**Design Title**
3	VOUT	15.00		15.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	900.00		900.00	V	Input DC voltage 1
6	IOUT1	1.000		1.000	A	Output current 1
7	POUT1			15.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
10						
11	**OPERATING CONDITION 2**					
12	VINDC2	300.00		300.00	V	Input DC voltage 2
13	IOUT2	1.000		1.000	A	Output current 2
14	POUT2			15.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
17						
18	**OPERATING CONDITION 3**					
19	VINDC3			0.00	V	Input DC voltage 3
20	IOUT3			0.000	A	Output current 3
21	POUT3			0.00	W	Output power 3
22	EFFICIENCY3			0.00		Converter efficiency for output 3
23	Z_FACTOR3			0.00		Z-factor for output 3

Figure 17. Limit Operating Conditions to Nominal Input Range Only (300 VDC to 900 VDC).

Using an INN3949CQ IC, 50 kHz maximum switching frequency, a VOR of 180 V, and an EFD25 core will yield a PIXls sheet shown in Figure 18 below.

	PRIMARY CONTROLLER SELECTION					
70	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
71	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25°C
76	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125°C
77	ILIMIT_MIN			1.981	A	Primary switch minimum current limit
78	ILIMIT_TYP			2.130	A	Primary switch typical current limit
79	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.06	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1110	V	Peak drain voltage on the primary switch during turn-off
	WORST CASE ELECTRICAL PARAMETERS					
86	FSWITCHING_MAX	50000		50000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	180.0		180.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			9.130		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.062		Primary switch duty cycle
91	TIME_ON_MIN			0.40	us	Minimum primary switch on-time
92	TIME_ON_MAX			1.45	us	Maximum primary switch on-time
93	TIME_OFF			18.79	us	Primary switch off-time
94	LPRIMARY_MIN			203.3	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			214.0	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			224.7	uH	Maximum primary magnetizing inductance
98						
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			0.054	A	Primary switch average current
101	IPEAK_PRIMARY			1.971	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.971	A	Primary switch ripple current
104	IRMS_PRIMARY			0.267	A	Primary switch RMS current
	TRANSFORMER CONSTRUCTION PARAMETERS					
109	**CORE SELECTION**					
110	CORE	EFD25		EFD25		Core selection
111	CORE NAME			EFD25/13/9-3C96		Core code
112	AE			58.0	mm^2	Core cross sectional area
113	LE			57.0	mm	Core magnetic path length
114	AL			2000	nH	Ungapped core effective inductance per turns squared
115	VE			3300	mm^3	Core volume
116	BOBBIN NAME			EFD25/13/9 - 2 (P5-S5)		Bobbin name
117	AW			40.2	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW			16.40	mm	Bobbin width
119	BH			3.11	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
121						
122	**PRIMARY WINDING**					
123	NPRIMARY			24		Primary winding number of turns
124	BPEAK			3766	Gauss	Peak flux density
125	BMAX			3125	Gauss	Maximum flux density
126	BAC			1562	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			372	nH	Typical gapped core effective inductance per turns squared

Figure 18. Results for 300 VDC to 900 VDC, 15 V 15 W Design.

The design can then be evaluated at 30 VDC using Set-point Analysis to verify if it can deliver the required 15 W at 30 VDC. As shown in Figure 19, the resulting converter will provide the full 15 W at 30 VDC but with a slight increase in frequency compared to the maximum value inputted in the FSWITCHING_MAX field of PIXIs (Line 86). Ultimately, component losses and temperature rise should still be evaluated across all operating conditions before this design can be considered viable.

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	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
	APPLICATION VARIABLES					Design Title
3	VOUT	15.00		15.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	900.00		900.00	V	Input DC voltage 1
6	IOUT1	1.000		1.000	A	Output current 1
7	POUT1			15.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
10						
11	**OPERATING CONDITION 2**					
12	VINDC2	300.00		300.00	V	Input DC voltage 2
13	IOUT2	1.000		1.000	A	Output current 2
14	POUT2			15.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
17						
18	**OPERATING CONDITION 3**					
19	VINDC3			0.00	V	Input DC voltage 3
20	IOUT3			0.000	A	Output current 3
21	POUT3			0.00	W	Output power 3
22	EFFICIENCY3			0.00		Converter efficiency for output 3
23	Z_FACTOR3			0.00		Z-factor for output 3

Figure 19. Set-Point Analysis at 30 V input, 15 W Output for the Design Shown in Figure 18.

7. Critical External Components Selection

7.1 PRIMARY BYPASS Pin Capacitor (C_{BPP})

This capacitor is the supply decoupling capacitor for the primary-side controller and is also used to select the current limit for the internal power switch. A 0.47 µF or 4.7 µF capacitor sets STANDARD or INCREASED current limit, respectively. Use only 0805 or 1206 surface-mount X7R or C0G multilayer ceramic capacitors for C_{BPP} with a minimum voltage rating of 25 V. This capacitor should be placed as close as possible to the IC.

It is recommended to use two capacitors in parallel in automotive applications to comply with functional safety requirements. Use a parallel combination of 100 nF with 470 nF for STANDARD current limit and 100 nF in parallel with 4.7 µF for INCREASED current limit. Note that if the 4.7 µF capacitor fails (assuming the capacitor cracks or fails open) in the latter combination, the current limit of the unit will revert to STANDARD during the next power cycle resulting in reduced power delivery capacity.

If only one capacitor is used for C_{BPP}, never use fail-open capacitors.

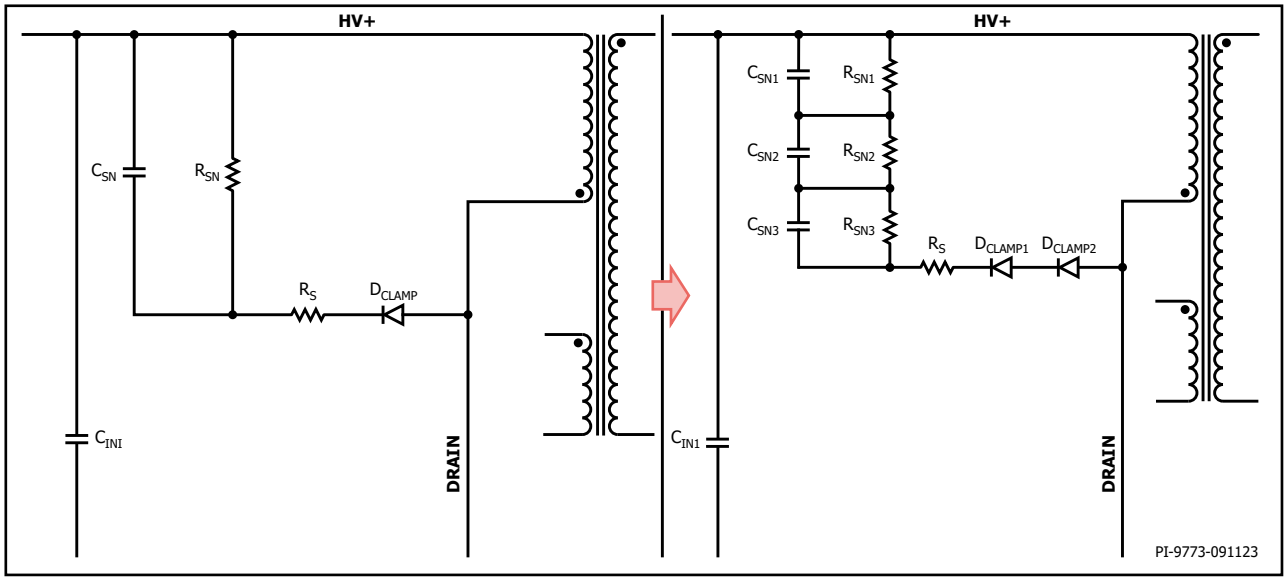


Figure 20. R2CD Snubber Basic Schematic (left) and Actual Sample Implementation for High-Voltage Applications (right).

7.2 Primary Clamp Network (D_{CLAMP}, R_S, R_{SN}, and C_{SN})

The primary clamp network protects the primary switch from large voltage spikes during turn-off. These transient voltages are due to the high primary current di/dt during turn-off, leakage inductance in the transformer, and stray inductances in the primary loop. Figure 20 shows the basic schematic of an R2CD snubber, the most commonly used flyback clamp configuration. For automotive applications, it is often necessary to use series components to meet voltage derating and creepage requirements. For automotive applications, the snubber should limit the peak drain voltage of the InnoSwitch Drain-Source voltage to 80% of BV_{DSS} at the worst conditions.

The clamp diode, D_{CLAMP}, must have a reverse recovery time of less than 500 ns (fast recovery). Resistor R_S offers a degree of damping, preventing excessive ringing due to the resonance between the leakage inductance and C_{SN}. Resistor R_{SN} bleeds off the energy stored inside the capacitor, C_{SN}. The values of capacitor C_{SN} and resistors R_S and R_{SN} depend on specific design parameters and are thus required to be optimized for each new design.

As a general rule, minimizing the value of C_{SN} and maximizing the value of R_{SN} is advised. The value of R_S should be large enough to dampen the ringing within an acceptable time.

The following equations can be used to calculate the R2CD clamp component values:

$$R_{SN} = \frac{V_{SN}^2}{\frac{1}{2} I_{PK}^2 L_{LK} \frac{V_{SN} f_{SW}}{V_{SN} - V_{OR}}}; \quad C_{SN} = \frac{V_{SN}}{R_{SN} f_{SW} \Delta V_{SN}}; \quad R_S = \sqrt{\frac{L_{LK}}{C_{SN}}}$$

where

V_{SN} = Average voltage across clamp capacitor/resistor
≤ (0.8 × BV_{DSS}) – $V_{IN(MAX)}$
I_{PK} = Peak switching current
f_{SW} = Switching frequency
L_{LK} = Transformer leakage inductance
V_{OR} = Reflected output voltage
ΔV_{SN} = V_{SN} Ripple voltage (5-10%)

Use the Input Set Point Analysis section of PIXIs to determine the variables listed above. The snubber should be designed to cover all possible operating points, so multiple set points should be evaluated to determine the maximum values of the variables used. The voltage rating of the diode should be assessed at the highest input voltage, while the values of the resistors and capacitors should be calculated at the operating point where maximum power dissipation occurs.

The clamp circuit is highly dependent on actual transformer leakage and primary side loop inductances, so it is important to tune the values of the clamp once a hardware prototype is available.

Table 4 below can be used as a guide for the number of series R_{SN} needed for any given clamp voltage, V_{SN}.

Number of R_{SN} Series Resistors Needed	Maximum V_{SN} Allowed	
	250 V Rated Resistors	200 V Rated Resistors
1	210 V	170 V
2	425 V	340 V
3	635 V	510 V

Table 4. Number of Series Resistors Needed for Varying Voltage Ratings and V_{SN}.

The number of parallel resistors can be calculated using the equation below:

$$\text{Number of } R_{SN} \text{ string in parallel} = \frac{I_{PK}^2 L_{LK} f_{SW}}{\text{Resistor power rating} \times \text{Number of resistors in series}}$$

7.3 Bias Supply Components (D_{BIAS}, C_{BIAS}, R_{BIAS})

The InnoSwitch3-AQ family of devices has a high-voltage internal regulator allowing it to start up when the bias supply is not yet available. This internal regulator draws current from the DRAIN pin to charge the BYPASS pin (BPP) capacitor to VBPP whenever the power MOSFET is off. When the power MOSFET is on, the device operates from the energy stored in the BPP pin capacitor.

After start-up, the supply of the InnoSwitch3-AQ primary must come from the bias supply. The external bias must be designed to inject sufficient current into the BPP pin so the high-voltage internal regulator turns off after unit start-up. An optimized bias supply has the added benefit of higher light load efficiency and no-load consumption as low as a few mW.

The external bias circuit consists of the transformer bias winding (N_{BIAS}), a diode (D_{BIAS}), bias supply filter capacitors (C_{BIAS1} and C_{BIAS2}), and a BPP current limiting resistor (R_{BIAS}), as shown in Figure 21.

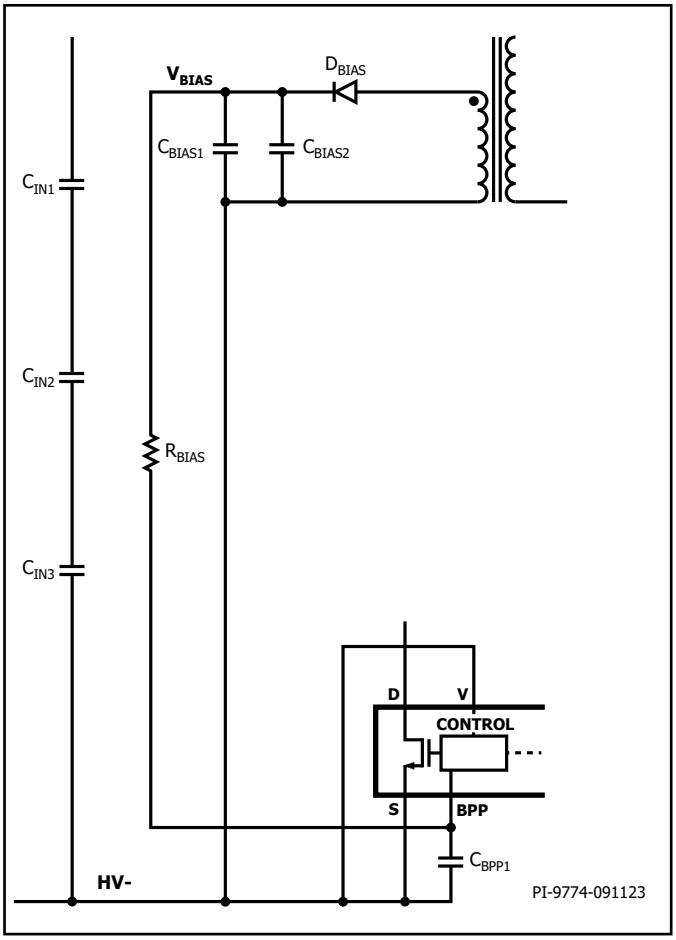


Figure 21. BPP External Bias using a Single Resistor.

The bias circuit should be designed to meet the following requirements:

1. Supply enough current into the BPP pin at no-load (I_{BPP} > 489 µA) and during normal operation (I_{BPP} will depend on operating switching frequency) such that the high-voltage internal regulator does not need to turn on.
2. Ensure that the current injected into the BPP pin during normal operation does not exceed the BYPASS shutdown threshold current (I_{SD}), which will trigger auto-restart.

The value of the bias voltage at no-load can be estimated using the following equation:

$$V_{BIAS} = \frac{N_{BIAS}}{N_{SEC}} V_{OUT} - V_{DBIAS}$$

The transformer bias winding turns (N_{BIAS}) and bias filter capacitors must be chosen such that the bias voltage, V_{BIAS}, is at least 8 V at no-load conditions. Two 10 µF ceramic capacitors are recommended. The regulation of V_{BIAS} varies according to load current and coupling of the bias winding to the primary, so the transformer must be optimized to achieve good cross-regulation between the main output, V_{OUT}, and V_{BIAS}. The value of R_{BIAS} should satisfy the following equations:

$$R_{BIAS} = \frac{V_{BIAS(NOLOAD)} - V_{SHUNT}}{I_{S1(MAX)}}$$

$$I_{S1} + (I_{S2} - I_{S1})\left(\frac{f_{SW}}{132\ kHz}\right) < \frac{V_{BIAS(FULLLOAD)} - V_{SHUNT}}{R_{BIAS}} < I_{SD}$$

where

V_{SHUNT} = BPP voltage when current is injected into the BPP pin
I_{S1} = BPP supply current at no-load
I_{S2} = BPP supply current at 132 kHz (refer to data sheet)
f_{SW} = maximum switching frequency at full load

The value of R_{BIAS} can be optimized for no-load consumption or maximum efficiency once a prototype is available.

7.4 SECONDARY BYPASS Pin Capacitor (C_{BPS})

This capacitor is the decoupling capacitor for the secondary-side controller. Use an 0805 or 1206, 2.2 µF, ≥ 25 V, MLCC capacitor for C_{BPS}. The SECONDARY BYPASS (BPS) pin voltage must reach 4.4 V before the output voltage reaches its target value. Higher C_{BPS} values could lead to output voltage overshoot during start-up. Values lower than 1.5 µF will cause unpredictable operation; hence, using 1.5 µF and below is not recommended. The capacitor must be placed adjacent to the IC pins. The ≥25 V rating and 0805 or 1206 package requirements are necessary to guarantee sufficient capacitance during operation since the capacitance of ceramic capacitors drops with increasing DC bias. Use X7R or C0G dielectrics for best results.

7.5 Output Synchronous Rectifier MOSFET (SR FET)

The InnoSwitch3-AQ IC features a built-in synchronous rectifier (SR) driver that enables the use of low-cost, low-voltage MOSFETs for synchronous rectification increasing system efficiency. The SR FET is placed in the return line since the SR driver is referenced to the output GND. GND is the typical threshold that ensures the SR FET will turn off ($V_{SR(TH)}$) at the end of the flyback conduction time. There is a slight delay between the flyback cycle's commencement and the SR FET's turn-on to avoid current shoot-through. During SR FET conduction, the energy stored in the inductor is transferred to the load, and the current will continue to drop until the voltage across the $R_{DS(ON)}$ of the SR FET drops to 0 V. At this point, the SYNCHRONOUS RECTIFIER pin will pull the gate low to turn off the SR FET instantaneously. Minimal current will flow through the SR FET body diode during the remainder of the flyback time (see Figure 22). In continuous conduction mode (CCM), the SR FET is turned off before a feedback pulse is sent to the primary to demand a switching cycle.

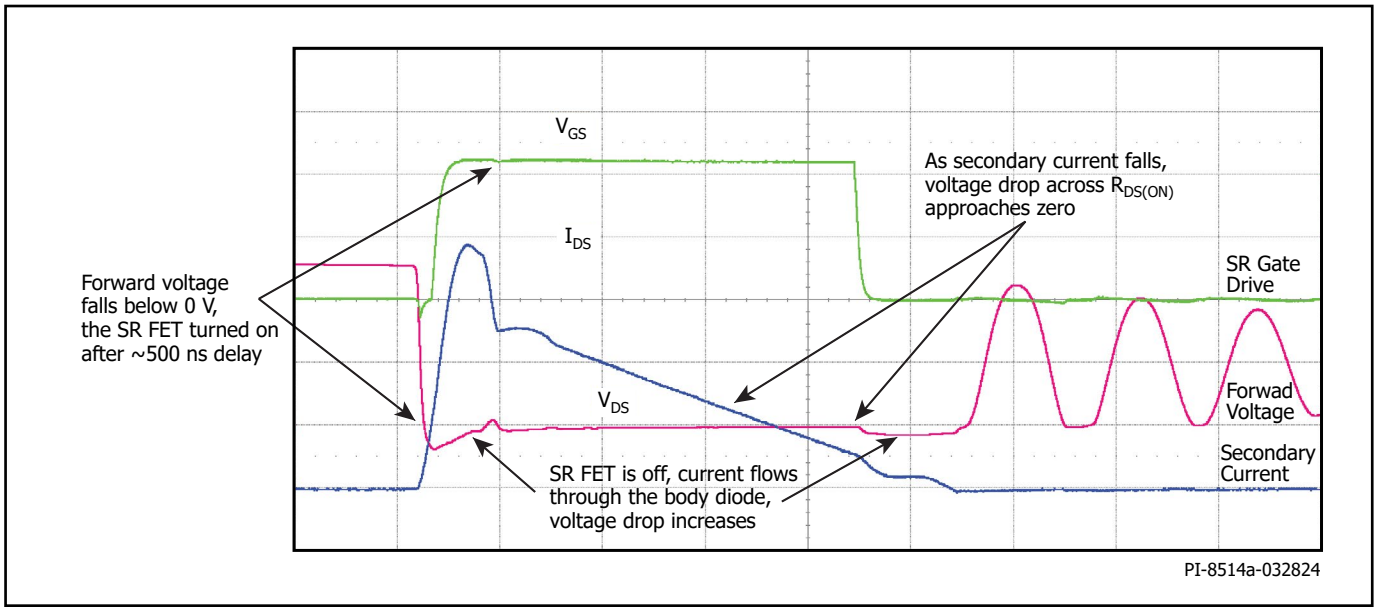
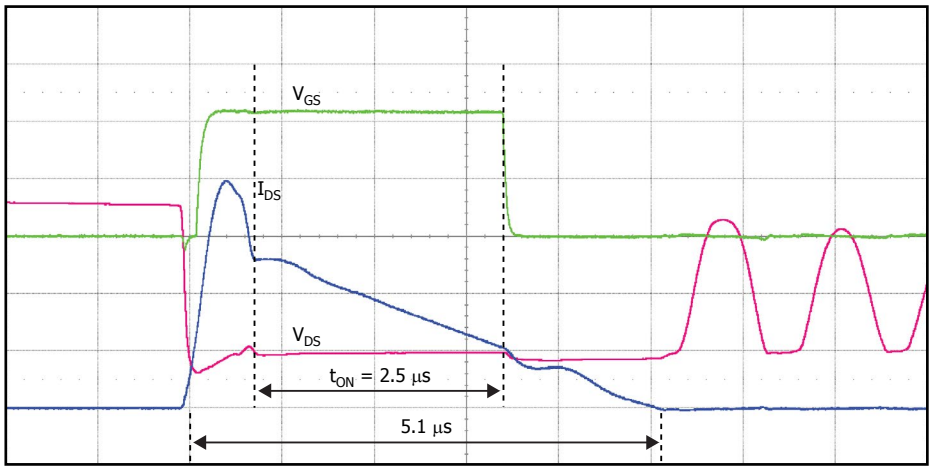


Figure 22. FET Turn-ON and Turn-OFF Events During DCM Operation.

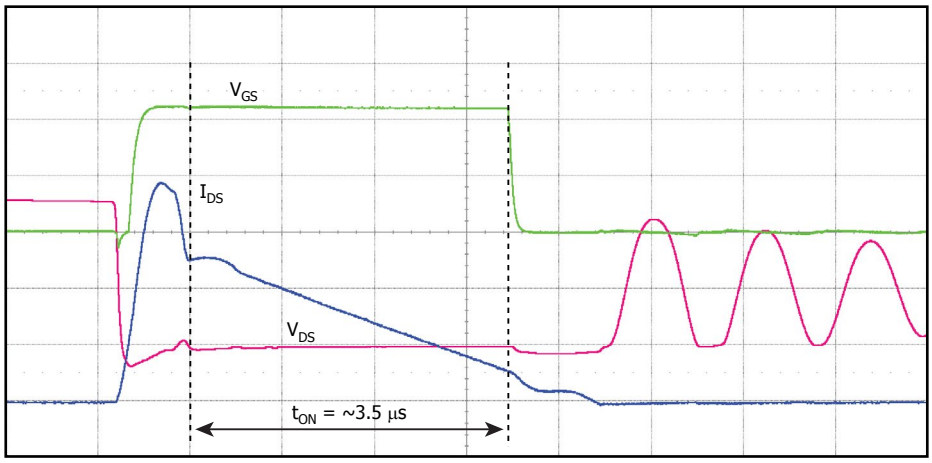
The SR FET driver uses the BPS pin for its supply rail, whose voltage is typically 4.4 V. Therefore, an SR FET with a high threshold voltage is unsuitable. SR FETs with a minimum gate voltage threshold within 1.5 V to 2.5 V are recommended. However, data sheet characteristic curves should be reviewed to ensure that the MOSFET channel is adequately enhanced for a 4.4 V gate drive to achieve the desired $R_{DS(ON)}$.

Since the termination of the ON-time of the SR FET is based on when the Drain-Source voltage of the FET reaches 0 V during the conduction cycle, using an SR MOSFET with ultra-low $R_{DS(ON)}$ (<5 mΩ) may result in early termination of the SR FET drive signal. This will cause the secondary current to conduct through the SR FET body diode instead, causing a slight reduction in system efficiency (see Figure 23).



PI-8516-050918

$R_{DS(ON)}$ = 7.5 mΩ Shows Short SR FET Conduction Time of 2.5 µs.



PI-8515-050918

$R_{DS(ON)}$ = 16 mΩ Shows Long SR FET Conduction Time of 3.5 µs.

Figure 23. Effects of $R_{DS(ON)}$ on SR FET Conduction Time.

The lowest SR FET Drain-to-Source on-resistance can be approximated using the following formula:

$$R_{DS(ON)} \geq \frac{0.01 \times V_{OUT}}{I_P \times V_{OR}}$$

A higher $R_{DS(ON)}$ will result in higher loss and temperature, whereas a low $R_{DS(ON)}$ will cost more. $R_{DS(ON)}$ value is best determined based on the temperature rise of the MOSFET for a value of $R_{DS(ON)}$ that is selected.

The voltage rating of the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) calculated by PIXIs. The spreadsheet estimates the SR FET PIV by the DC output voltage to the applied maximum input DC BUS voltage multiplied by the primary-to-secondary turns ratio of the transformer. This value is displayed as VDRAIN_OFF_SRFET. The actual SR FET PIV should be measured during prototyping to confirm sufficient margin compared to the BV_{DSS} of the chosen SR FET.

$V_{DSMAX(SRFET)} \geq 1.4 \times$ VREVERSE_RECTIFIER1 (Line 186 of PIXIs)

A Schottky or fast-recovery diode for output rectification in place of the SR FET is possible. For this, the SR pin must be connected to the secondary GND pin of the InnoSwitch. Diode rectifiers are often preferred for low-cost designs or those with high-voltage outputs.

The DC current rating of the diode must be at least double that of the average output current. Increasing the SR FET or diode current rating and its cooling area may be necessary depending on the temperature rise and the duration of peak load conditions.

Another critical parameter in selecting the SR FET is its body diode's reverse recovery time (T_{RR}). The reverse recovery characteristics of the SR FET's body diode can influence the voltage stress level on the drain when the primary FET switches on. An SR FET with a slow body diode (> 40 ns T_{RR}) can have as much as twice the voltage stress compared to ones with a fast body diode. The recommended SR FET body diode maximum reverse recovery time (T_{RR}) is less than 40 ns.

7.6 SR FET Snubber

At the instance of voltage reversal across the primary winding due to the primary FET turn-on, the interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) can lead to oscillations in the SR voltage waveform. This ringing can be suppressed using a series RC snubber connected in parallel to the SR FET drain and source terminals, as shown in Figure 24. A snubber resistor of 2 Ω to 10 Ω may be used (higher resistance values will lead to a significant drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs. The value of the RC snubber should also be tuned during hardware testing.

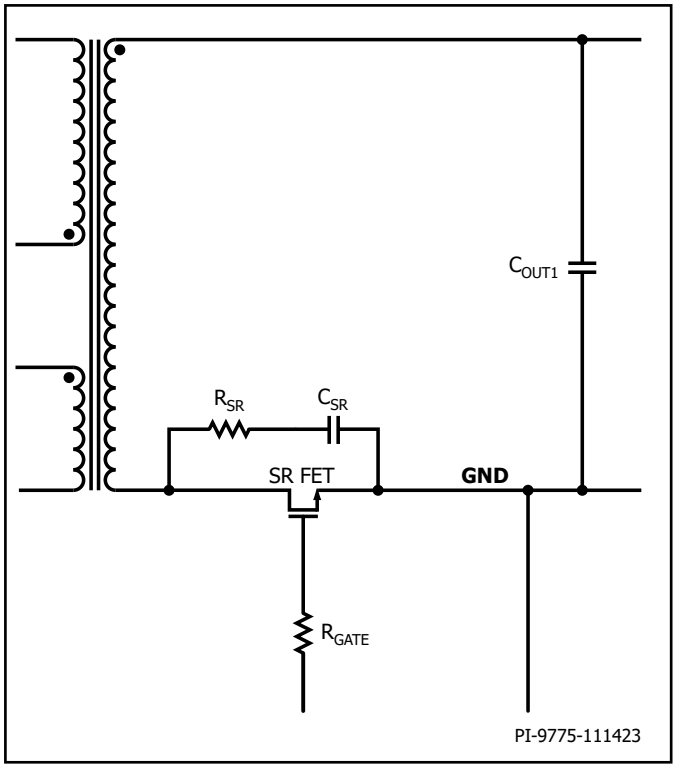


Figure 24. SR FET Snubber (C_{SR} and R_{SR}).

Calculation of the SR snubber can also be done using the following steps once a prototype is available:

1. With no SR snubber installed, set the input voltage to the minimum. Turn on the power supply and set the output load to 100%.
2. Using a scope probe, measure the frequency of the SR Drain-Source oscillation during turn-off (f_{RING}). See Figure 25.
3. Calculate the estimated secondary leakage inductance, L_{SLKG}, using the measured frequency and the following equation:

$$L_{SLKG} = \frac{1}{(2\pi f_{RING})^2 C_P}$$

where

C_P = effective stray capacitance of SR FET. C_{DS} of SR FET can be used – check the device data sheet for information.

4. The SR FET snubber values can then be calculated using the following equations:

$$C_{SR} = 3C_P$$
$$R_{SR} = \sqrt{\frac{L_{SLKG}}{4C_P}}$$

Power dissipation of R_{SR} can be solved by using the following:

$$P_{RSR} = C_{SR} \times V_{DS,SR(MAX)}^2 \times FSWITCHING$$

5. Test the computed snubber and tune accordingly. Increasing C_{SR} and R_{SR} will lower the turn-off peak voltage but reduce efficiency. On the other hand, lower R_{SR} values will prolong the SR FET's turn-off oscillation.

Figure 25. Measure the Frequency of Oscillation of the SR FET VDS During Turn-Off Ringing (encircled) to Solve for SR FET Snubber Values.

7.7 FORWARD Pin Resistor and FWD Filter Capacitor (R_{FWD}, C_{FWD})

The FORWARD pin (FWD) is used to sense the drain voltage of the SR FET and is critical for precise turn-on and turn-off control. This pin is also used to charge the BPS pin capacitor when the output voltage is lower than the BPS voltage. The FORWARD pin should be connected to the Drain terminal of the synchronous rectifier MOSFET (SR FET) through a resistor R_{FWD}.

A 47 Ω to 100 Ω resistor is recommended to ensure sufficient secondary supply current and works for a wide range of output voltages. A lower resistor value is not recommended, as it can affect device operation and synchronous rectification timing.

Care should be taken to ensure that the voltage on the FORWARD pin never exceeds its absolute maximum voltage of 150 V. Since the FORWARD pin monitors the drain voltage of the SR FET, the peak voltage experienced by the FORWARD pin is also the Drain-Source voltage of the SR FET during turn-off, including the voltage spike.

If the SR FET used is rated for higher than 150 V, and the spike voltages across the SR FET Drain-Source exceeds the FWD pin maximum voltage rating, it is recommended that a filter be used to protect the FWD pin (C_{FWD}). A ceramic capacitor large enough to filter the leading-edge spike of the SR FET Drain-Source voltage can be connected in parallel with the FWD pin and secondary GND. A 100 pF to 330 pF, 1206, 250 V, X7R ceramic capacitor will suffice for most applications. The presence of parasitic components, such as leakage reactance of the secondary, leads to ringing on the drain pin of the SR FET. This ringing can interfere with the operation of the IC. The resulting waveforms and acceptance criteria are shown in the data sheet. In case the ringing is found to cause early termination of the SR FET, the FWD pin resistor may be increased to 150 Ω.

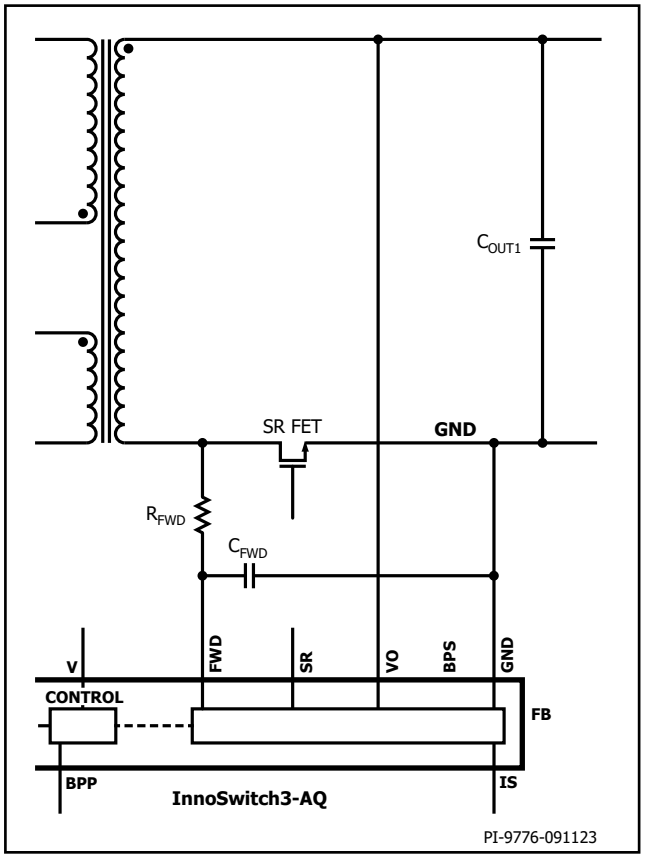


Figure 26. R_{FWD} and C_{FWD} for FWD Pin Current Limiting and Filtering.

7.8 Output Filter Capacitance (C_{OUT})

The current ripple rating of the output capacitor should be greater than the calculated value in the spreadsheet, IRIPPLE_CAP_OUTPUT. If a single suitable capacitor is not available, then multiple capacitors in parallel can be used to achieve the required ripple current rating. Ensure that the ripple rating matches the ambient operating temperature of the power supply design.

For automotive applications, surface-mount aluminum-polymer solid capacitors are recommended. These capacitors have a relatively compact size, stable characteristics across temperatures, very low ESR, and a high RMS ripple current rating.

Aluminum-polymer solid capacitors are recommended for applications expected to operate at very low temperatures (as low as -40˚C) to prevent significant increase in output voltage ripple. A common rule for selecting capacitor value is 220 µF to 330 µF of capacitance per ampere of output current.

8 Transformer Design Guidelines

The transformer design must ensure the power supply delivers the rated power at the lowest input voltage. It is recommended that a K_P close to 0.9 at the minimum expected DC BUS voltage be used for most InnoSwitch3-AQ designs. A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but causes higher switching losses in the primary-side switch resulting in higher InnoSwitch3-AQ temperatures. The benefits of quasi-resonant switching diminish with a further reduction of K_P. PIXls spreadsheet and the incorporated Magnetics Designer Tool can be used to optimize transformer design.

8.1 Transformer Core Selection

Transformer core geometry (size) should be sufficient to deliver the required power of the design. The Area Product (AP) approach could be used to verify whether a core size is suitable for a specific application.

Core material should also be taken into consideration. Core materials optimized for the application's switching frequency and operating temperature should be selected. Automotive application maximum ambient operating temperatures usually range from 85 °C to 105 °C. Examples of core materials with relatively flat core loss across the above-mentioned operating temperature range are the 3C95, 3C96 and 3C97 from Ferroxcube, as shown in Figure 27. Suitable materials from other vendors such as EPCOS and TDK are N87, N97 and PC44.

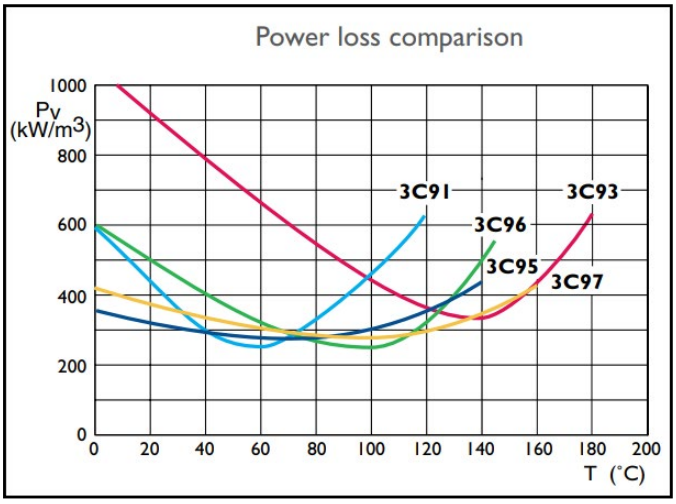


Figure 27. Core Loss Per Unit Volume vs. Operating Temperature for Various Core Materials.

8.2 Maximum Operating Flux Density

A maximum value of 3800 Gauss at the peak device current limit (at 132 kHz) is recommended to limit the peak flux density at start-up and under output short-circuit conditions. A value of 3800 Gauss at the selected device's peak current limit and the built-in protection features of InnoSwitch3-AQ IC provide sufficient margin to prevent core saturation under said conditions. Ensure that the saturation flux density of the core material selected is higher than 3800 Gauss across the design's operating temperature range. If a ferrite material with a lower saturation flux density is selected, the maximum operating flux density should be reduced accordingly.

8.3 Transformer Wire Selection

To achieve compact transformer designs while maintaining reinforced isolation between primary and secondary, it is recommended to use fully insulated wires (FIW) on the primary/high-voltage windings and triple insulated wires (TIW) on the secondary/low-voltage windings.

FIW offers the same level of insulation as the TIW but comes with a smaller overall diameter, making winding a lot easier and reducing the overall winding stack-up height.

Since both the primary (FIW) and secondary (TIW) wire's isolation are both considered reinforced, the use of insulating tape in between layers of the windings can be reduced to a minimum (or even eliminated), improving the overall leakage inductance of the transformer.

Wire diameter can be optimized using the PI Xls Magnetics Designer tab. Both primary and secondary wires should be selected to minimize the resulting copper losses.

8.4 Transformer Leakage Inductance and Winding Capacitance

Magnetic core geometry and winding configuration significantly influence the leakage inductance. To minimize leakage inductance, the primary winding should be wound completely along the bobbin's winding width. The secondary should be wound as close to the primary, using minimal to no insulating tape. Another way to improve the leakage inductance is to select a wire diameter size to reduce the number of winding layers while maintaining sufficient current density.

For some designs, it is more beneficial to slightly increase the current density of the transformer wires to reduce the number of windings resulting in a reduction in leakage inductance. This can often lead to higher efficiency and reduced component stresses, especially in the primary-side switch.

The interwinding capacitance of the transformer should also be minimized to reduce common mode noise from coupling across the isolation boundary. There is an inverse relationship between transformer leakage inductance and winding capacitance; if the interwinding capacitance is reduced, leakage inductance will increase.

Ultimately, optimization should be done once a prototype board is available. The transformer prototype should be iterated until a unit that meets specifications and is repeatable is achieved.

8.5 Partial Discharge (PD) and Hi-Pot Test for Transformers

It is recommended that transformers be tested for both Partial Discharge and Hi-Pot. Hi-Pot testing measures the dielectric breakdown of the primary-to-secondary isolation used in the transformer but cannot provide information on the reliability of the isolation over time. Successful PD testing ensures high-quality materials are used in the design, reducing the risk of failure over time during actual operation. Refer to IEC 60664-1 and IEC 61800-5-1 for details on performing PD test and calculating the required test voltages according to the application.

9. Supplementary Circuits

9.1 Input Line Filters (Common-Mode Choke (CMC) or Differential LC Filters)

9.1.1 Input CMC Filter

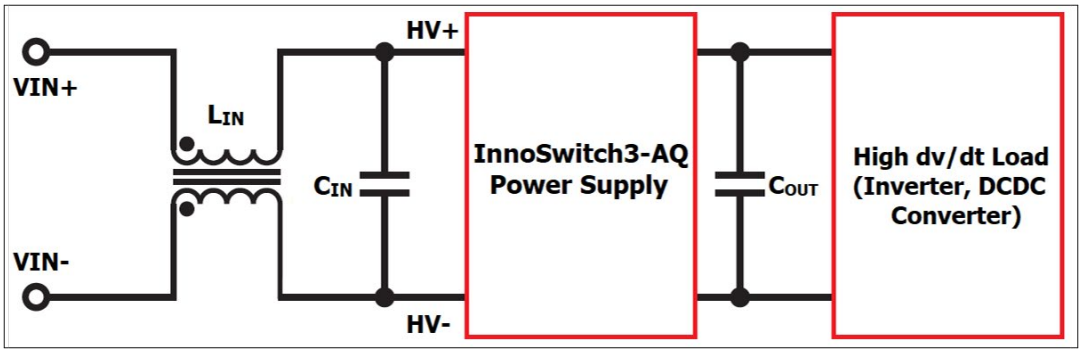


Figure 28. Typical Input CMC Filter for Loads with High Common Mode Noise or High dv/dt (without damping).

For applications where the flyback converter supplies a circuit with high dv/dt switching, such as high-power DC/DC converters or inverters, adding a CMC at the input side of the power supply is highly recommended, as shown in Figure 28. Typical input CMC filter for loads with high common mode noise or high dv/dt (without damping). The CMC prevents common-mode noise from passing through the power supply circuit, which can affect the proper operation of the InnoSwitch3 IC. The value of the CMC to be used is dependent on the following factors:

1. The spectral content of the CMC noise
2. The interwinding capacitance of the flyback transformer
3. Parasitic capacitances present in the system

Figure 29 is a simplified diagram of one phase of an inverter system where an InnoSwitch3-based flyback converter (PSU) supplies power to the gate drive units (GDUs) controlling a Power Module (IGBT or SiC). It shows the possible path common mode noise generated by high dv/dt at the bottom switch Emitter/Source node can take due to the presence of parasitic capacitances both in the PSU and GDU. Although high dv/dt switching is also present at the Collector/Drain nodes of both switches, due to the way power modules are constructed, there exists a relatively large capacitance between the Drain/Collector of the switches to the module baseplate (C10 and C11) which is usually connected to chassis ground. With the output capacitance of the upper switch (C8), capacitors C10 and C11 effectively form a low-impedance loop that effectively shorts the noise current generated from the Emitter/Source node of the upper switch, preventing it from propagating further. This means the dv/dt at the low side switch Emitter/Source becomes the primary source of common mode noise, and an excellent way to reduce said noise from entering the PSU and interfering with the InnoSwitch3-AQ IC's operation is to use a CMC at the converter's input as shown in Figure 30.

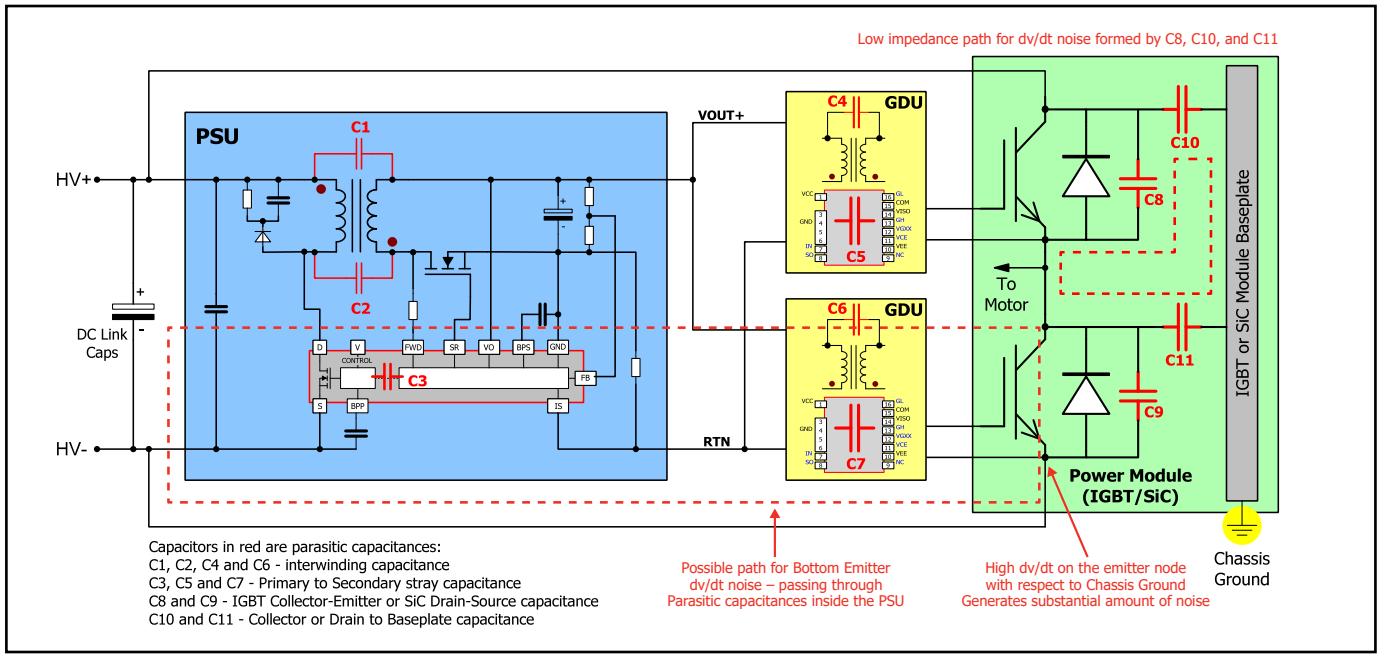


Figure 29. Parasitic Capacitances in an Inverter System and Noise Paths Due to High dv/dt.

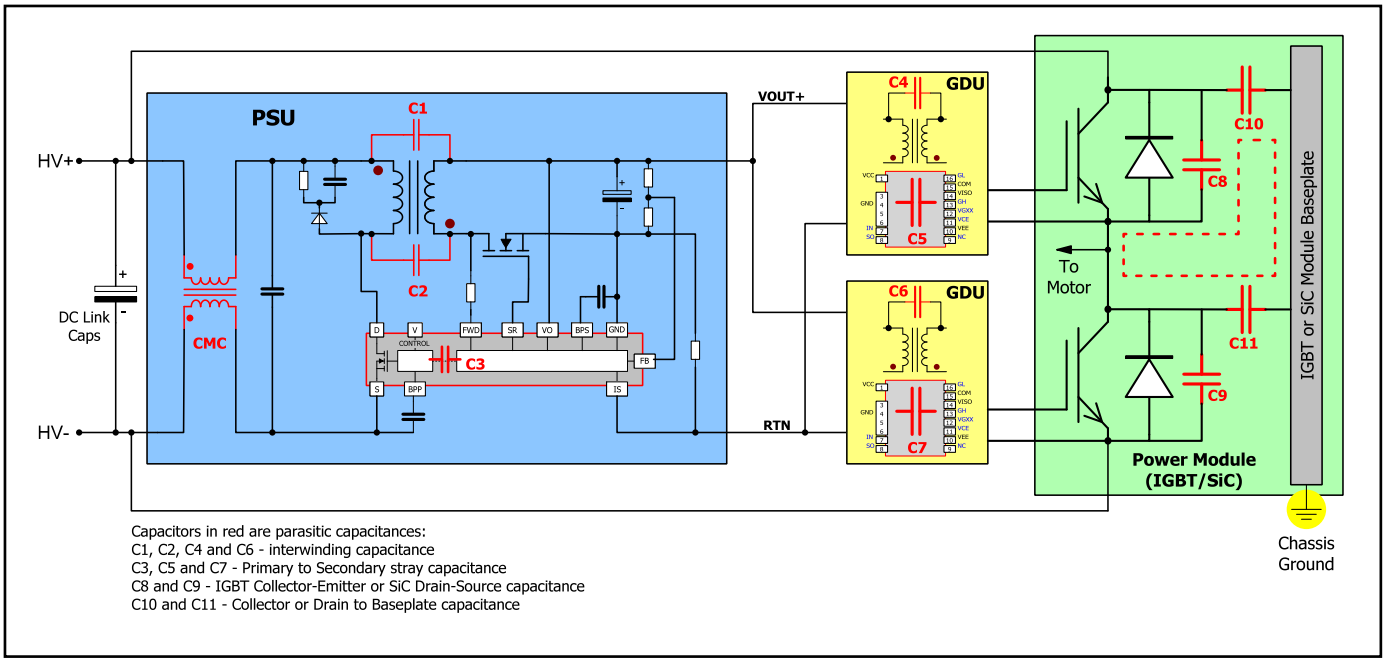


Figure 30. A CMC at the Input of the InnoSwitch3-AQ Power Supply Reduces dv/dt Noise from Inverter.

It is often challenging to accurately determine the parasitic capacitances of a system, so in general, the largest inductance value CMC is used as long as it complies with the following:

1. The CMC current rating should be at least 1.5 times the maximum primary RMS current of the flyback converter. This occurs at the minimum input voltage delivering nominal output power.
2. Ensure that the winding-to-winding insulation of the CMC complies with IEC 60664-1 and other relevant standards. Check that the CMC pads meet clearance and creepage requirements and that the winding-to-winding isolation passes both Hi-Pot and PD testing requirements.
3. The CMC must be AECQ-qualified and should satisfy environmental requirements.

The leakage inductance of a CMC manifests itself as a differential inductor in series with the CMC, so choosing a CMC with a large leakage inductance and calculating the corresponding C_{IN} will result in a filter with both common- and differential-mode blocking with minimal component count.

9.1.2 Input Differential LC Filter with Damping

An input LC filter is used if there is significant differential mode noise present at the input or if there is a need to prevent the switching noise from the power supply from polluting the input BUS. The basic rules for the design of the filter are as follows:

1. The filter's cut-off frequency is usually set at 1/10th of the switching frequency or one decade away from the desired frequency to be attenuated. The cut-off frequency is given by:

$$f_0 = \frac{1}{2\pi\sqrt{L_{DM}C_{DM}}}H_Z$$

2. The input impedance of the power supply should be much greater than the characteristic impedance of the LC filter.

$$Z_{DM} \leq \frac{1}{10}Z_{IN}$$

$$Z_{DM} = \sqrt{\frac{L_{DM}}{C_{DM}}}; Z_{IN} = \frac{V_{IN}^2 \times \text{Efficiency}}{P_{OUT}}$$

In typical power supplies, the ESR of an electrolytic capacitor is often enough to dampen the peaking of the gain at the cut-off frequency of an LC filter. For high-voltage input automotive power supplies, the input capacitor used is often a ceramic type with very low ESR. This results in a filter with a high Q-factor resulting in a very high cut-off frequency gain. Damping should be added to the filter network to prevent oscillations at the input, which might affect converter operation.

A parallel RC damping network is impractical for high-voltage inputs because it requires a larger value damping capacitor and a long string of series resistors. A more practical approach is the series damping shown in Figure 31.

Use the following equations to solve for L_{DAMP} and the optimum R_{DAMP}. The first step is to solve for n using the input impedance of the power converter. Once n is known, the optimum R_{DAMP} and L_{DAMP} can be solved.

$$|Z_{DAMPED}| = \frac{1}{10}Z_{IN} = Z_{DM}\sqrt{2n(1+2n)}$$

$$R_{DAMP} = Z_{DM}\sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}}$$

$$L_{DAMP} = nL_{DM}$$

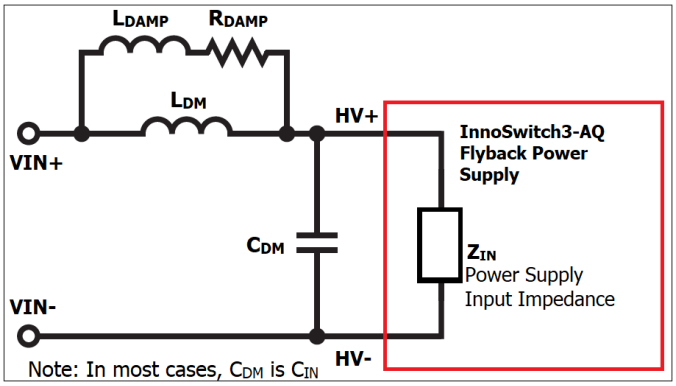


Figure 31. Input LC filter with Series Damping.

L_{DAMP} from Figure 31 can be removed, leaving only R_{DAMP} in parallel with L_{DM} to dampen the input LC filter, as shown in Figure 32. A downside to this approach is that the resistor introduces a high frequency zero, reducing the gain roll-off from -40 dB/decade to -20 dB/decade at:

$$f_Z = R_{DAMP}/2\pi L_{DM}$$

From f_Z, the filter essentially becomes a single-pole low-pass filter. R_{DAMP} is chosen such that the peak impedance of the filter will never exceed 1/10th of the converter input impedance.

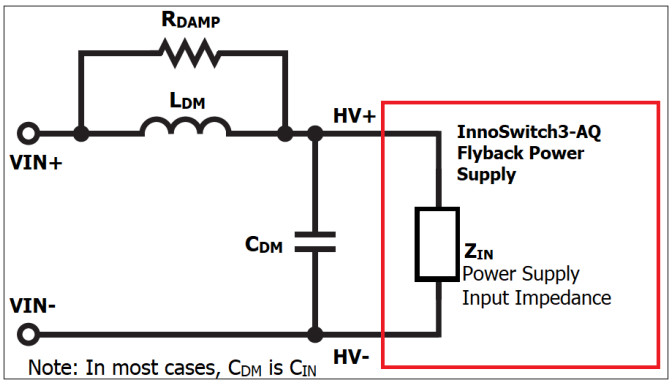


Figure 32. Input LC Filter with Simplified Damping.

For 400 V systems that require fewer capacitors in series to meet derating requirements, parallel damping (Figure 33) can also be an option.

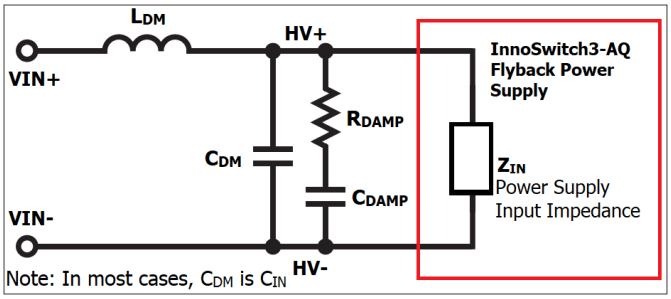


Figure 33. Input LC Filter with Parallel Damping.

The damping components R_{DAMP} and C_{DAMP} can be calculated using the following equations:

$$|Z_{DAMPED}| = \frac{1}{10} Z_{IN} = \frac{Z_{DM}\sqrt{2(2+n)}}{n}$$

$$R_{DAMP} = Z_{DM}\sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}}$$

$$C_{DAMP} = nC_{DM}$$

A resistor in series with the filter inductor can also be used as damping for high-voltage input power supplies with low input current (low output power), as shown in Figure 34. Use the lowest value resistor that can provide ample reduction of filter gain at the filter cross-over frequency. Higher resistor values will provide more damping but incur more losses and voltage drop. This resistor can also limit the inrush current to the power supply during V_{IN} turn-on. If the topology in Figure 34 is used, the following should be taken into consideration:

1. Power rating of the resistor, R_{IN}: Ensure the resistor can handle the power dissipation at minimum V_{IN} and maximum P_{OUT}.
2. Pulsed current rating: The resistor should be rated to handle the inrush current during start-up.
3. Voltage rating: R_{IN} will "see" the full V_{IN} voltage when C_{IN} is discharged.

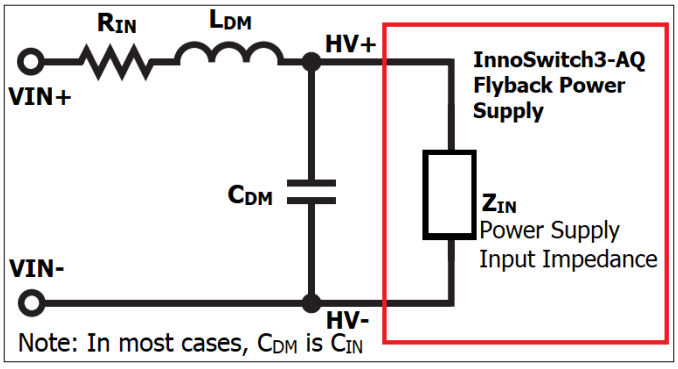


Figure 34. LC Filter Damping Using a Resistor in Series with L_{DM}.

9.1.3 Sample Design of Damping for Input Filter

A 30 VDC to 1000 VDC input, 15 V 35 W output power supply is observed to have oscillations in the input voltage at certain loading conditions, as shown in the figures below. The oscillations affect the power supply regulation due to the noise causing secondary to primary request pulse grouping.

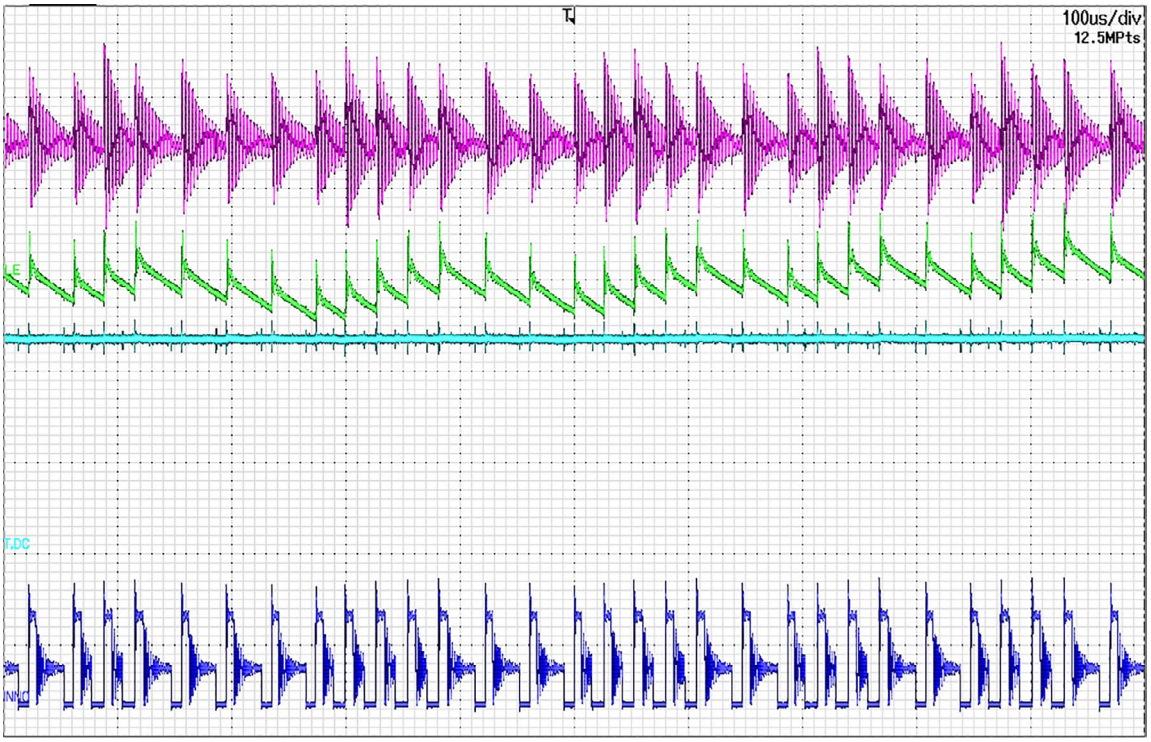


Figure 35. V_{IN} Oscillation (Top Trace, AC Coupled) Affecting Output Ripple and Regulation at V_{IN} = 200 VDC, P_{OUT} = 35 W.

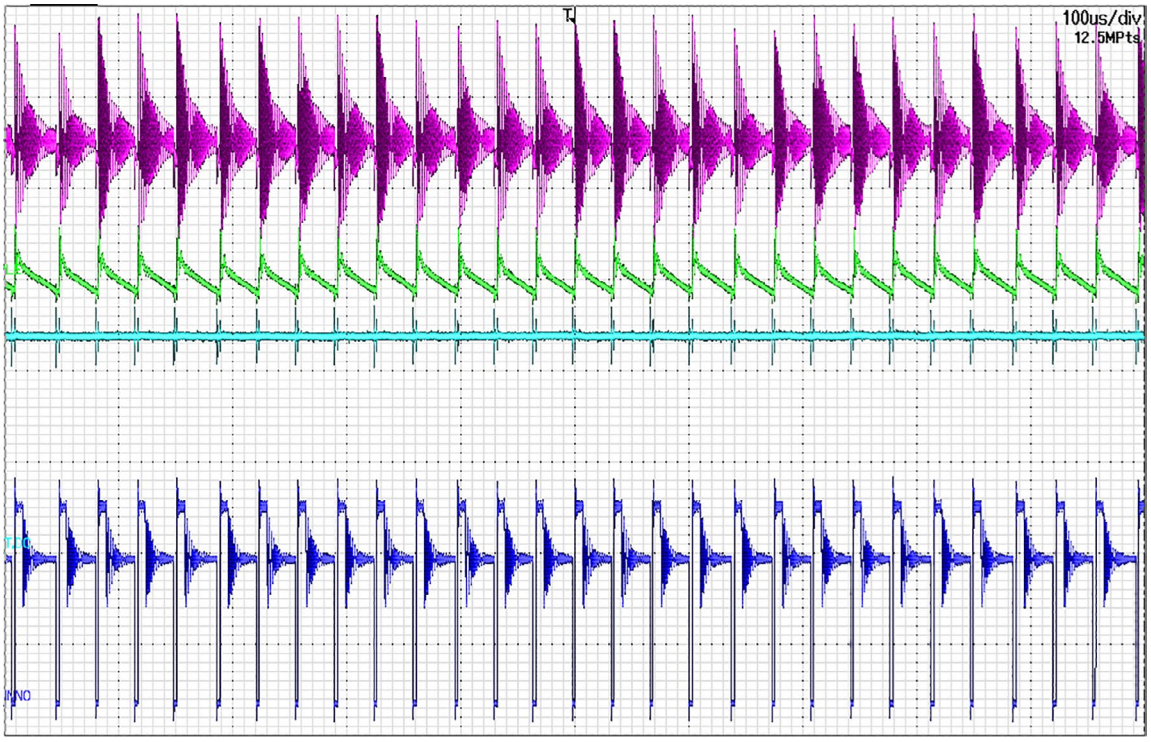


Figure 36. V_{IN} Oscillation (Top Trace, AC Coupled) Affecting Output Ripple and Regulation at V_{IN} = 800 VDC, P_{OUT} = 35 W.

The oscillation is due to the high gain at the LC filter's cut-off frequency formed by the input CMC leakage inductance and input capacitors. Using the equations given, series damping is used to reduce the oscillations.

1. Calculate the power supply input impedance using the lowest V_{IN}, Efficiency, and output power. Actual measurements can also be used to determine Z_{IN}.

To design the input filter, $Z_{DM} \leq \frac{1}{10} Z_{IN}$ must be satisfied,

$$Z_{IN} = \frac{V_{IN}^2 \times \text{Efficiency}}{P_{OUT}} = \frac{(120\ V)^2 \times 0.85}{35\ W} = 349.71\ \Omega$$

$$Z_{DM} = \sqrt{\frac{L_{DM}}{C_{DM}}} = \sqrt{\frac{4.9\ \mu H}{50\ nF}} = 9.899\Omega$$

L_{DM} was measured from the CMC used in the design, while $C_{DM} = C_{IN}$

2. Given the values of Z_{IN} and Z_{DM}, the value of n in the following equation can be solved:

$$\frac{1}{10} Z_{IN} = Z_{DM} \sqrt{2n(1+2n)}$$

$$\frac{1}{10}(349.71\Omega) = (9.899\Omega)\sqrt{2n(1+2n)}$$

This results in two values of n:

$$n_1 = 1.533$$

$$n_2 = -2.033$$

Use n with the positive value and solve for R_{DAMP} and L_{DAMP}

$$n_1 = 1.533 \rightarrow R_{DAMP} = 19.77\Omega,\ L_{DAMP} = 7.582\mu H$$

3. Divide the values by two and connect in parallel to each CMC winding, as shown in Figure 37 below.

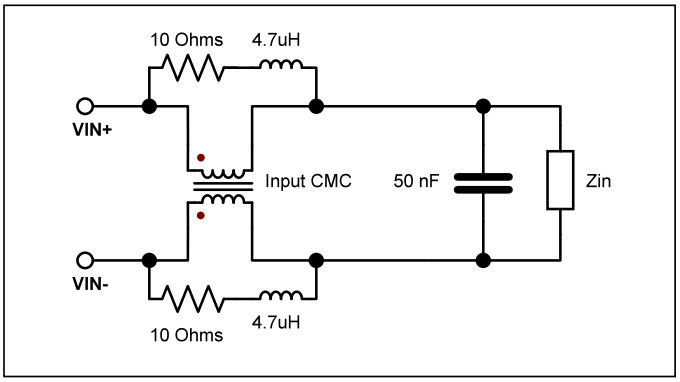


Figure 37. CMC with Calculated Series Damping Components.

4. Verify the frequency response through simulation, then check the actual results. Select the configuration that allows for the best performance across all operating conditions.

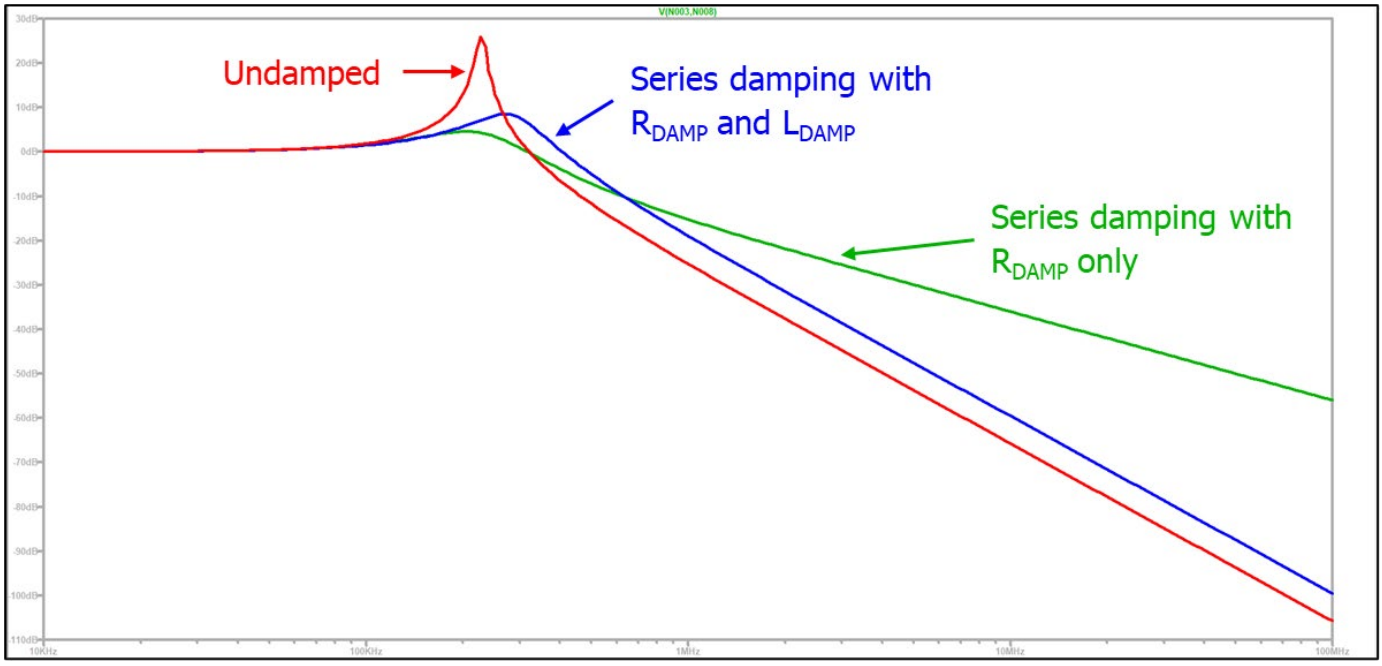


Figure 38. Frequency Response for no Damping (Red), Series RL Damping (Blue) and R-Only Damping (Green).

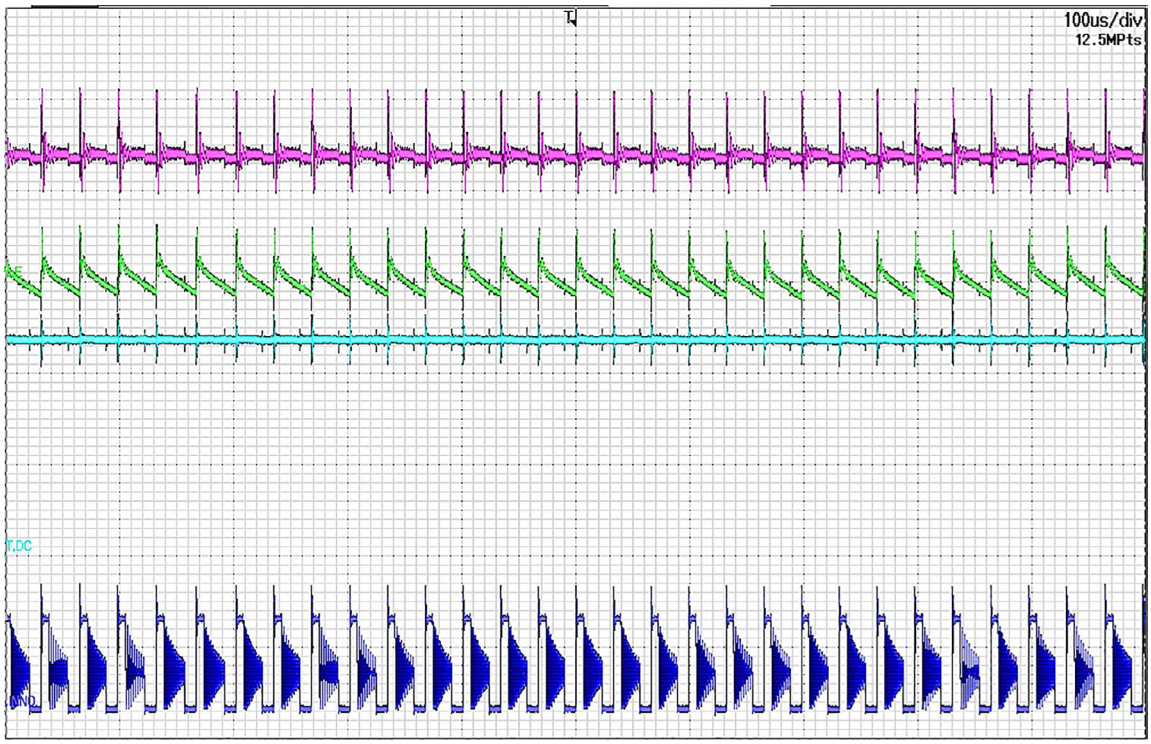


Figure 39. Damped V_{IN} Oscillation (Top Trace, AC Coupled) at V_{IN} = 200 VDC, P_{OUT} = 35 W.

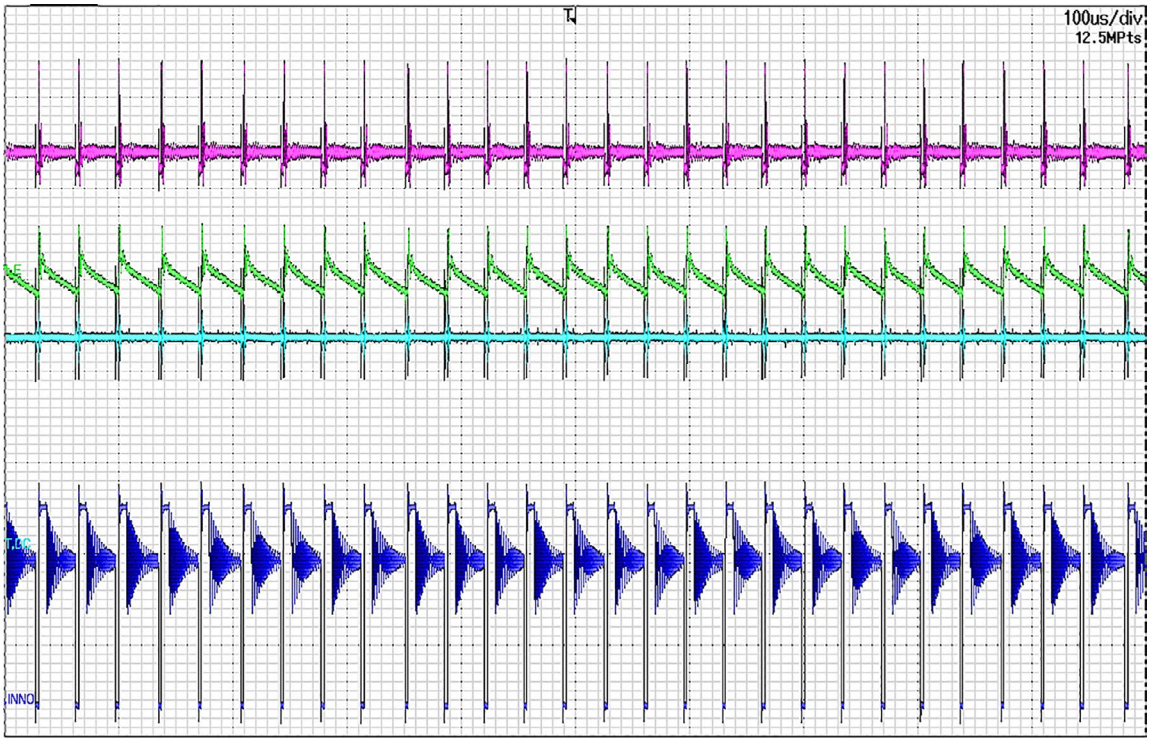


Figure 40. Damped V_{IN} Oscillation (Top Trace, AC Coupled) at V_{IN} = 800 VDC, P_{OUT} = 35 W.

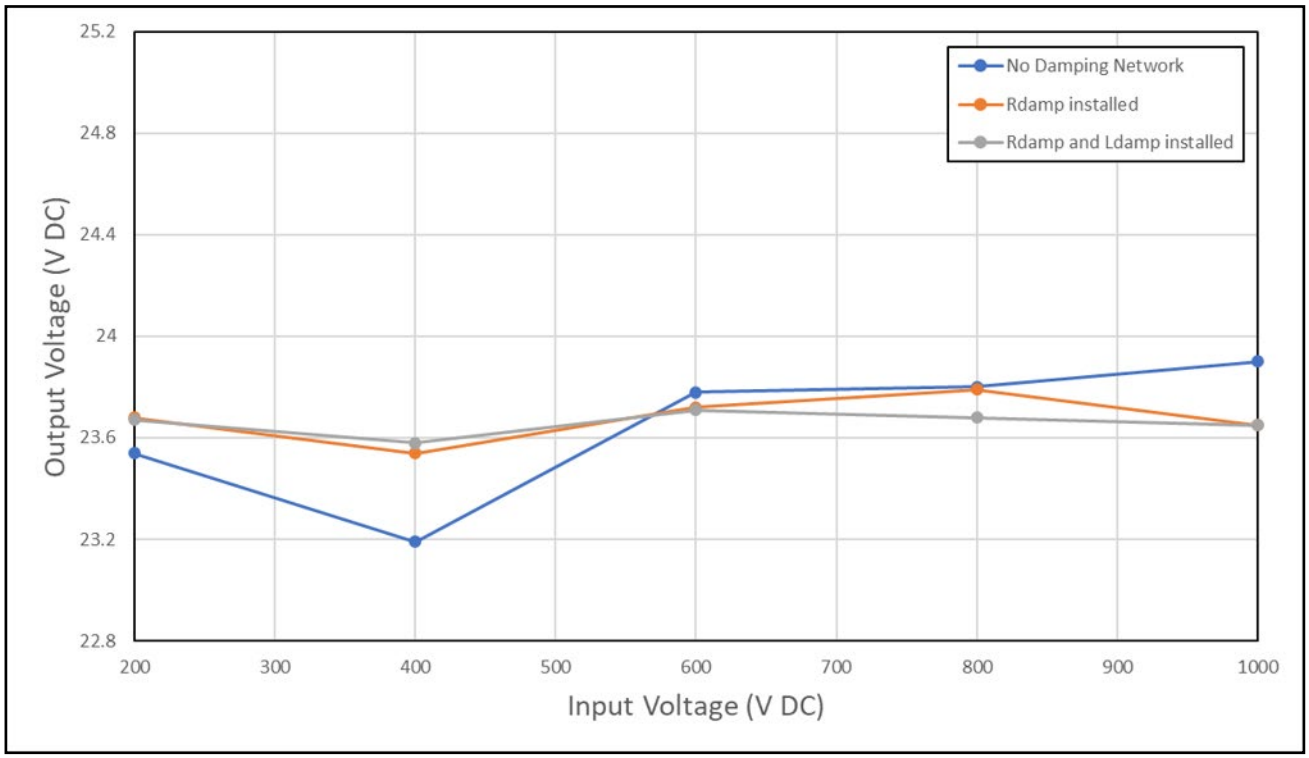


Figure 41. Comparison of Output Voltage Line Regulation with and Without Damping (35 W Load).

9.2 Primary-Sensed Overvoltage Protection (D_{POV}, VR_{POV}, R_{POV})

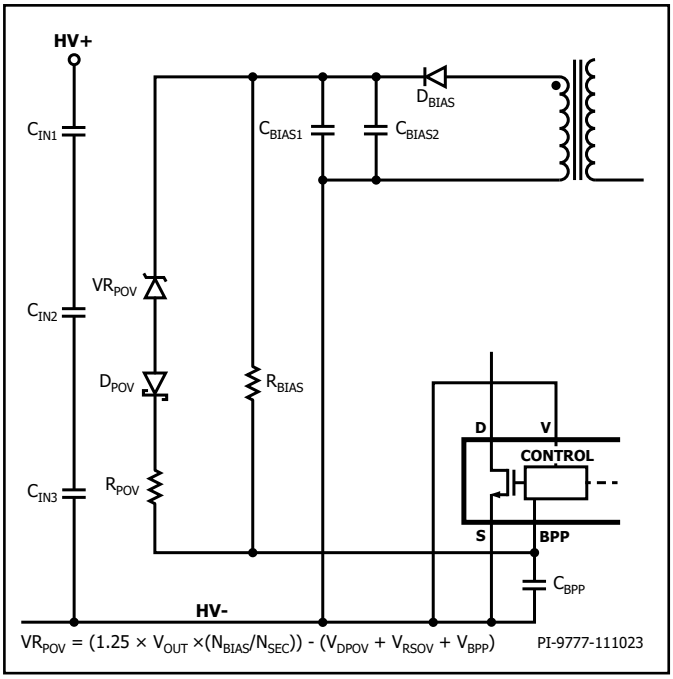


Figure 42. Primary-Sensed OVP Schematic.

The InnoSwitch3-AQ IC is equipped with an internal latch-off that is triggered if a current greater than or equal to a threshold current, I_{SD}, flows into the BPP pin. Primary-sensed output OVP can be realized by connecting a series resistor (R_{POV}) and a Zener diode (VR_{POV}) from V_{BIAS} to the BPP pin, as shown in Figure 42. The value of V_{BIAS} varies depending on the bias diode's (D_{BIAS}) recovery type, coupling of the bias winding with the output winding, and the resulting ringing on the bias winding voltage waveform. Fast and ultra-fast recovery diodes result in higher V_{BIAS} than standard recovery diodes. Therefore, the rectified bias winding voltage should be measured during prototyping. This measurement should be made at the lowest input voltage with full output load. This measured V_{BIAS} should be used to select the components required to provide primary sensed OVP.

The Zener diode VR_{POV} must be selected with a clamping voltage approximately 6 V lower than the value of V_{BIAS} where OVP is expected to be triggered. R_{POV} should be chosen such that in the event of a single point fault, such as shorting of the VR_{POV} Zener, the resulting BPP pin current does not exceed the absolute maximum current rating of the BPP pin while ensuring a current higher than I_{SD} is injected into the BPP pin during an output overvoltage event. D_{POV} prevents C_{BIAS} from loading the internal tap during start-up and can be a standard recovery, small-signal diode. The accuracy of the primary-side OVP is highly dependent on the coupling between the bias and secondary winding. Thus, the value used for VR_{POV} and R_{POV} should be trimmed during prototype testing across all temperature and loading conditions.

9.3 Secondary-Sensed Overvoltage Protection

Output overvoltage can also be triggered on the secondary side of the InnoSwitch3 controller by injecting a current greater than $I_{BPS(SD)}$ into the SECONDARY BYPASS pin. Secondary OVP can be implemented using the circuit shown in Figure 43. R_{SOV} should be selected such that in the event of a single point fault, such as shorting of the VR_{SOV} Zener, the resulting BPS pin current does not exceed the absolute maximum current rating of the BPS pin. OVP is typically set to trigger at 125% of V_{OUT}. When selecting VR_{SOV}, the temperature coefficient and tolerance of the Zener should be evaluated, and a sufficient margin should be kept (at least 3 V – 5 V) between the OV trigger threshold and the normal operating output voltage. Care should be taken to ensure that the fault protection will trigger at a voltage lower than the absolute maximum voltage rating of the VOUT pin and the surge voltage rating of the output capacitors. In addition, the voltage ratings of other components, such as the SR FET, should not be exceeded when the voltage reaches the OVP detection threshold.

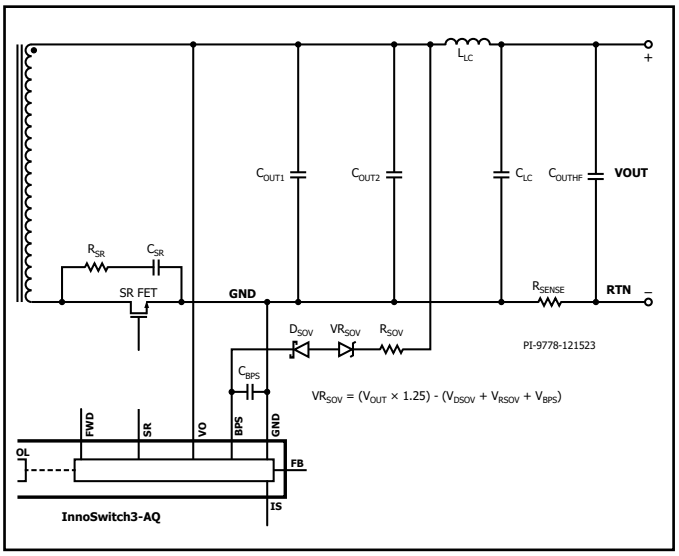


Figure 43. Secondary-Sensed OVP Schematic.

9.4 CURRENT SENSE Pin Output Short Protection

For applications with relatively high output voltage, large output capacitance, and very low output trace impedance, there is a possibility of exceeding the maximum voltage rating of the IS pin during short-circuit events. To protect the sense resistor and IS pin from failing during output shorts, it is recommended that a diode be placed in parallel with the sense resistor R_{SENSE} as shown in Figure 44. D_{IS} should be selected to withstand the large current discharge from the capacitors during the first few milliseconds of a short circuit event. A diode with a sufficiently high I_{FSM} rating should be selected such that the short-circuit current does not exceed the diode said rating.

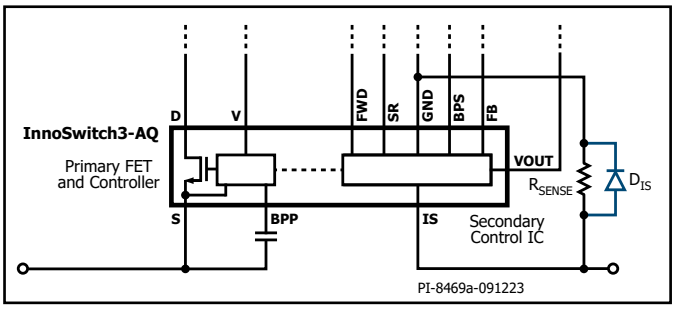


Figure 44. Protection Diode for IS Pin and R_{SENSE}.

9.5 Primary-Side Enable/Disable Circuit with UVLO

The V pin of the InnoSwitch3-AQ IC can be used to implement a Remote Enable/Disable function using the circuit in Figure 45. This circuit also includes a BPP UVLO that ensures the InnoSwitch3-AQ IC starts properly, even when supplied with a non-monotonic input voltage. Non-monotonic input voltages may exist when residual voltage less than 20 V is present between the HV+ and HV- terminals for an extended period. The external UVLO will prevent the InnoSwitch3-AQ IC logic circuits from powering up until HV+ exceeds a chosen turn-on threshold and will shut down when HV+ falls below the turn-off threshold. For the example shown, the turn-on threshold is between 26 V to 29 V, while the turn-off threshold is between 20 V to 23 V.

The operation of the circuit is described below:

1. IC1 contains two independent comparators with an internal reference voltage of 400 mV. OUTA and OUTB are open-drain outputs. OUTA goes low if a voltage less than 400 mV is present at INA+. Otherwise, OUTA turns off (high impedance). The inverse logic applies to the B-channel. If INB- is below 400 mV, OUTB is off and goes low otherwise.
2. When HV+ is below the turn-on threshold, the IN+ node should be below 400 mV. This keeps the OUTA pin state low, clamping BPP to the breakdown voltage of VR1, which is 2.7 V, preventing the InnoSwitch3-AQ IC from starting up. If Q1 is OFF (EN/DIS signal is LOW), the voltage at INB- is determined by voltage dividers R5, R6, and R7 and should also be below 400 mV. This sets the OUTB pin to HIGH, disconnecting R9. If Q1 is already ON (EN/DIS signal is HIGH), INB- will always be below 400 mV, meaning R9 will always be floating until the EN/DIS signal is de-asserted.
3. Once HV+ exceeds the desired turn-on voltage (corresponding to 400 mV at the INA+ pin), the OUTA pin will immediately go HIGH, disconnecting VR1 and allowing BPP to increase to around 5.2 V. This increase in BPP voltage will also increase the current through R3, further raising the voltage at INA+ and adding a certain level of hysteresis. At this point, the InnoSwitch3-AQ will begin its 82 ms start-up and wait-and-listen sequence before switching. If Q1 is off, as soon as BPP increases to 5.2 V, the voltage at INB will also increase. However, the increase in INB- voltage will be delayed by capacitor C1. Once INB- exceeds 400 mV, OUTB will go low, causing R9 to shunt current from the V pin and trigger a UV fault. This will cause the InnoSwitch3-AQ IC not to start switching and thus keep the converter off. The toggling of OUTB from HIGH to LOW should happen within 30 ms to 40 ms after HV+ exceeds the turn-on threshold to prevent the InnoSwitch3 from releasing unwanted pulses. However, if Q1 is on when HV+ reaches the turn-on threshold, OUTB will not change state, no UV fault will be triggered, and the power supply will immediately start switching after 82 ms.

All component values shown in Figure 45, except for R_{IN}, R2, R3, and R4, can be used as is for any design or application. R_{IN}, R2, R3, and R4 should be calculated such that IN+ is at 400 mV when HV+ reaches the desired turn-on threshold. Keep R_{IN} in the few megaohms range to reduce losses in the voltage divider network while also meeting the bias current requirements of the comparator inputs. R3 should also be chosen according to the desired amount of hysteresis.

A BJT should be used for Q1 to directly control the Enable/Disable function from a micro-controller. Assert the EN/DIS signal HIGH to enable the power supply and set LOW to turn it off.

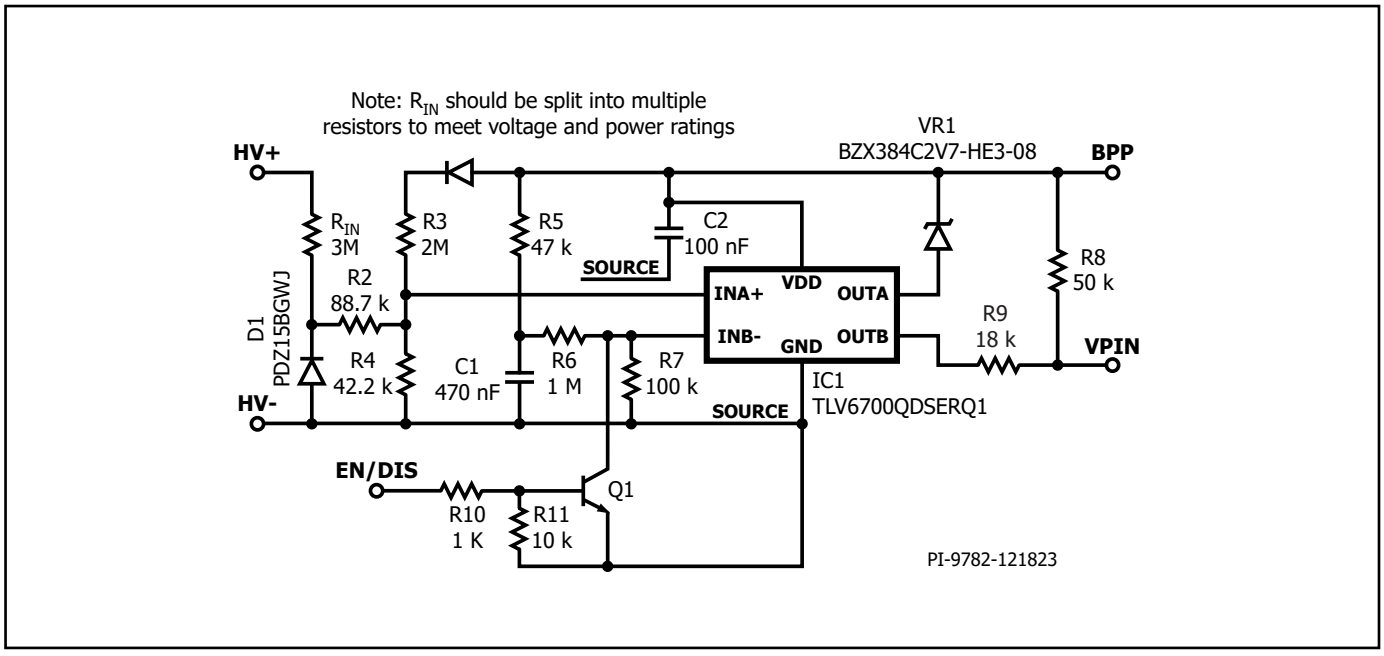


Figure 45. Enable/Disable Circuit with UVLO (For 400 V Input Voltage, UVLO Cut-In from 26 V to 29 V, 20 V < Turn-Off < 23 V).

9.6 Precision Voltage Regulation

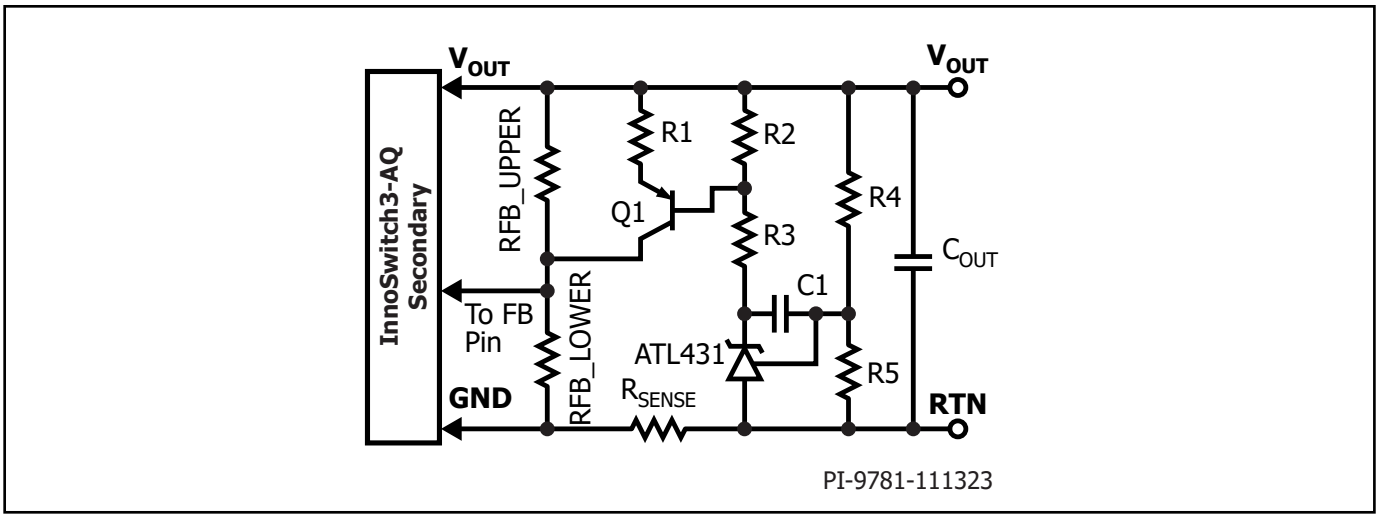


Figure 46. Precision Voltage Regulation Circuit using ATL431.

The internal feedback reference of the InnoSwitch3-AQ is a little over 1% across temperature – low enough for most applications. For applications where less than 1% regulation is desired, the circuit in Figure 46 can be used. This auxiliary circuit uses the ATL431 to effectively generate a variable resistor (Q1 and R1) parallel to RFB_UPPER, adjusting the output voltage against the TL431's internal high-precision reference. RFB_UPPER and RFB_LOWER are the original voltage divider resistors from the InnoSwitch3-AQ feedback network.

To use this design, RFB_LOWER and RFB_UPPER are calculated to generate an output voltage 10% higher than the desired regulation value. It is recommended that RFB_LOWER be set around 10 kΩ.

$$V_{FB(REF)} = 1.265\ V = \frac{RFB_{LOWER}}{RFB_{LOWER} + RFB_{UPPER}}(1.1 \times V_{OUT})$$

Resistors R4 and R5 are calculated to generate the desired output voltage level given a reference of 2.5 V seen at the C1, R4, and R5 junction. The value of R5 should not exceed 56 kΩ.

$$V_{TL431(REF)} = 2.5\ V = \frac{R5}{R4 + R5}(V_{OUT})$$

R1, R2, and R3 set the quiescent point and range of the variable resistor formed by R1 and Q1. The quiescent point of Q1 and the ATL431 should be placed far from saturation to allow the circuit to have ample output swing. Resistors R2 and R3 should also satisfy the self-bias requirement of the ATL431. The following formulas can be used as a guide for calculating resistors R1, R2, and R3.

$$V_{K(ATL431)} = V_{REF(ATL431)} + (0.3 \times (V_{OUT} - V_{REF(ATL431)}))$$

$$V_{B(Q1)} = V_{REF(ATL431)} + (0.6 \times (V_{OUT} - V_{REF(ATL431)}))$$

$$I_{R1} = \frac{V_{FB(REF)}}{RFB_{LOWER}}\left(1 - \frac{V_{OUT} - V_{FB(REF)}}{1.1 \times (V_{OUT} - V_{FB(REF)})}\right)$$

$$I_{K(ACTUAL)} >> I_{B(Q1)} + I_{K(ATL431)MIN}$$

where

$V_{K(ATL431)}$ = ATL431 cathode voltage
$V_{REF(ATL431)}$ = ATL431 reference voltage = 2.5 V
$V_{FB(REF)}$ = InnoSwitch3-AQ FB pin reference voltage = 1.265 V cathode voltage
$V_{B(Q1)}$ = Q1 base voltage
$I_{K(ACTUAL)}$ = Actual ATL431 cathode current used for calculation of the design
$I_{B(Q1)}$ = Q1 base current
$I_{K(ATL431)MIN}$ = minimum cathode current for proper ATL431 operation (see data sheet)

Capacitor C1 sets the bandwidth of the feedback, usually set at a maximum of 50 Hz since this circuit only aims to correct the DC error of V_{OUT}.

9.7 Other Design Considerations

9.7.1 Primary to Secondary Y Capacitors

It is not recommended to use Y capacitors connecting the primary SOURCE node to the secondary GND node, especially if the power supply is used in a noisy system such as an inverter. Common mode currents generated in high-voltage environments with high dv/dt can reach levels up to a few amps or tens of amps (depending on parasitic capacitance values), high enough to create significant voltage drops across signal copper traces. Adding a Y capacitor creates a low impedance path for common mode noise from the secondary to the primary, diverting common-mode current to the flyback circuitry, which may degrade the InnoSwitch3-AQ IC's performance.

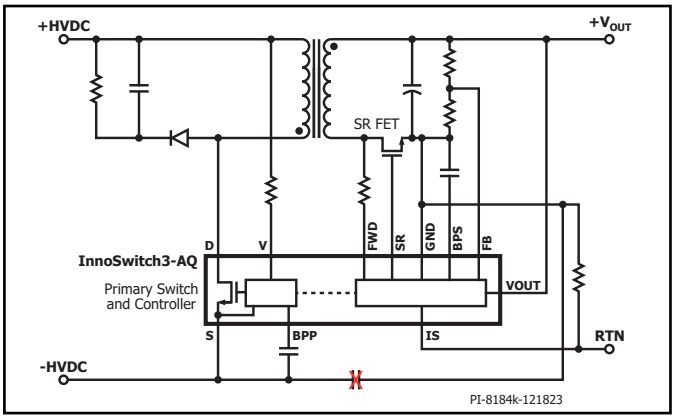


Figure 47. Do Not Use Y Capacitors Between Primary and Secondary Ground to Prevent Common Noise from Passing Through the Power Supply Circuit.

9.7.2 Non-Isolated Power Supply Designs

For applications where the load shares a common ground with the primary of the InnoSwitch3-AQ IC, it is not recommended to connect the SOURCE node in the primary to the GND node in the secondary. Doing this might create ground loops, as shown in Figure 48, causing unwanted current to flow through the InnoSwitch3 circuitry that could affect its operation. Like the Y capacitor, shorting the SOURCE pin to GND will also provide a low-impedance path for noise from the load to pass through the InnoSwitch3-AQ circuit.

Keep the output rails of the InnoSwitch3-AQ IC isolated from the primary within the power supply circuit block. Common grounding should occur at the point of load, not within the power supply block.

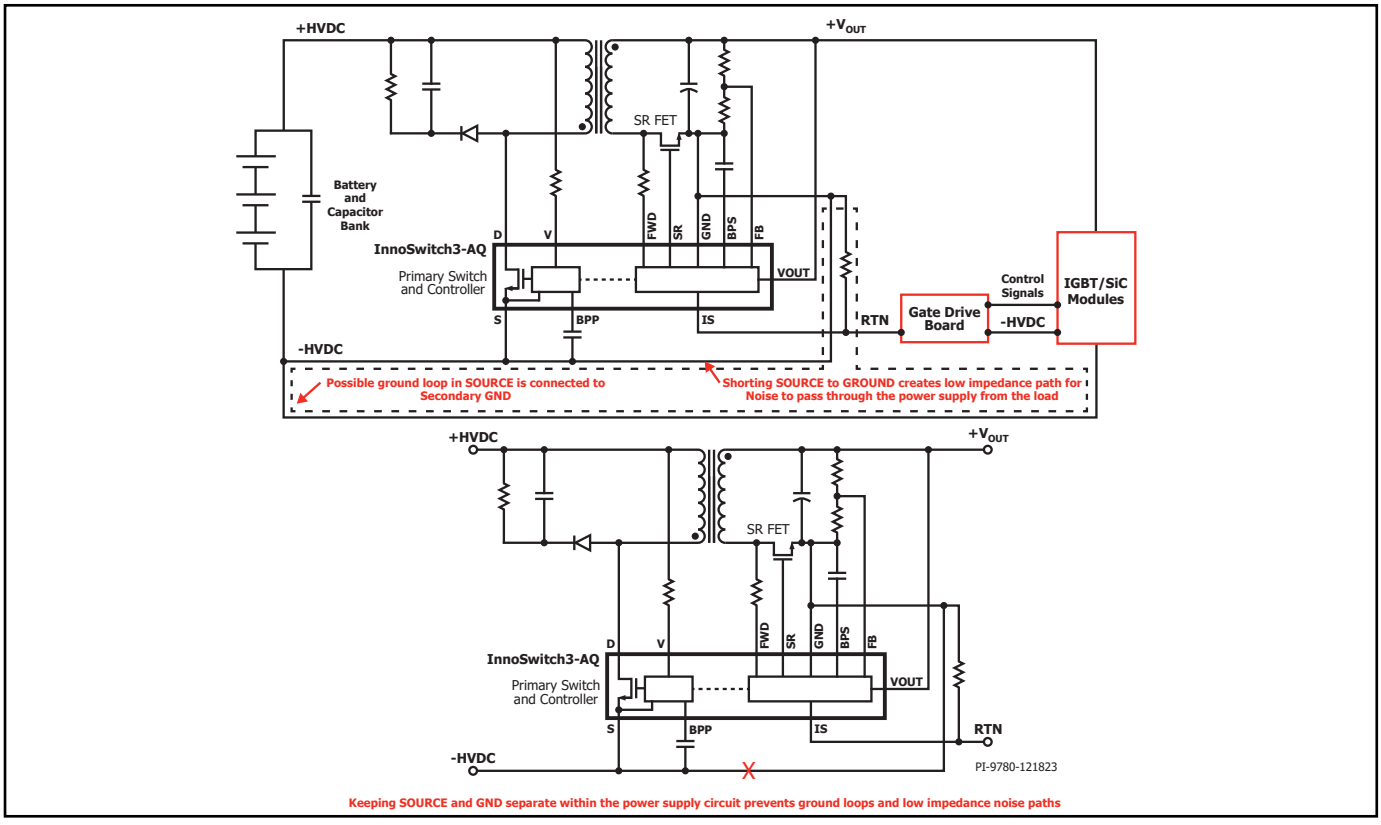


Figure 48. Ground Loops can be Created if the Flyback Primary is Connected to the Secondary GND for Loads with Common Ground to the Primary.

10. Creepage and Clearance

Table 5 below summarizes the minimum recommended clearance and creepage requirements that must be followed when designing the layout for the power supply. The table considers the IEC 60664-1 standard and lists values for various input voltages, V_{OR}, InnoSwitch3-AQ device, and other relevant factors. Example nodes to consider when calculating creepage and clearances are the following (non-exhaustive list):

1. Input voltage positive and negative rails (HV+ and HV-).
2. InnoSwitch3-AQ DRAIN to HV+ or HV-.
3. Nodes with high-voltage potentials, such as between snubber components (C_{SNUB}, R_{SNUB}, D_{SNUB}) and C_{IN}.
4. Primary to Secondary.
5. Primary to Chassis Ground.
6. Secondary to Chassis Ground.

Standard	Max Altitude	PCB CTI	Impulse Voltage	Chip	Input Voltage	V_{OR}	Device BVDSS	System Voltage (85% of BVDSS)	Clearance (mm)				Creepage (mm)			
									Pollution Degree = 1		Pollution Degree = 2		Pollution Degree = 1		Pollution Degree = 2	
									Minimum Basic Clearance	Minimum Reinforced Clearance	Minimum Basic Clearance	Minimum Reinforced Clearance	Minimum Basic Clearance	Minimum Reinforced Clearance	Minimum Basic Clearance	Minimum Reinforced Clearance
IEC 60664-1 Vsystem frequency < 30 kHz	5500 (C_{HA} = 1.59)	CTI IIIa 175 to 400	(OVC I) 2500 V	INN3977CQ	400	100	750	638	2.4	4.8	2.4	4.8	2.4	4.8	2.4	6.4
				INN3996CQ	500	150	900	765	2.4	4.8	2.4	4.8	2.4	4.8	3.3	6.6
				INN3997CQ	500	150	900	765								
				INN3999CQ	500	150	900	765								
				INN3990CQ	500	150	900	765								
				INN3947CQ	1000	225	1700	1445	2.4	4.8	2.4	4.8	4.1	8.2	6.2	12.4
				INN3949CQ	1000	225	1700	1445								
			(OVC 2) 4000 V	INN3977CQ	400	100	750	638	4.8	8.7	4.8	8.7	4.87	8.7	4.8	8.7
				INN3996CQ	500	150	900	765	4.8	8.7	4.8	8.7	4.8	8.7	4.8	8.7
				INN3997CQ	500	150	900	765								
				INN3999CQ	500	150	900	765								
				INN3990CQ	500	150	900	765								
				INN3947CQ	1000	225	1700	1445	4.8	8.7	4.8	8.7	4.8	8.7	6.2	12.4
				INN3949CQ	1000	225	1700	1445								

Table 5. Recommended Minimum Creepage and Clearance Values for Different Conditions and Devices According to IEC 60664-1.

11. Layout Guidelines

A switch-mode power converter's safe and proper operation depends on the PCB layout due to the circuit's fast switching voltages and currents. When used in automotive applications, especially in electric vehicles, the need for a robust layout is even more pronounced due to the harsh environment in which the design is expected to operate. Depending on the final application, the power supply layout must be designed while considering the following:

1. If the power supply is near or used to supply the inverter, the layout must be robust against EMI from the inverter, BUS bars, phase lines, and other possible noise sources.
2. Before starting the layout, the creepage and clearance rules must be calculated according to IEC 60664-1/3. The designer must determine the voltages on each node in the schematic and apply the necessary clearance and creepage rules in the layout software's DRC Rules. Ensure that footprints meet clearance/ creepage rules, especially if the PCB has a lower CTI than the corresponding component's body. Calculating creepage and clearance requires careful interpretation of the relevant standards and is beyond the scope of this document.
3. A set of DFM, DFA, and DFT rules must also be prepared to reduce manufacturing defects and allow for easy testing of the finished board.
4. Automotive designs typically use 4-layer PCBs at the minimum. Single- and double-layer boards are not recommended. Before layout, the board stack-up must also be determined.

11.1 PCB Stack-Up

PCB stack-up refers to the arrangement of insulating layers and conductive traces that comprise a printed circuit board (PCB). The stack-up is designed to meet the electrical and mechanical requirements of the PCB and typically consists of multiple layers of copper and dielectric materials.

A typical PCB stack-up may include the following layers:

1. **Signal Layer:** The layer of the PCB that carries the signal traces.
2. **Power and Ground Planes:** Copper layers dedicated to carrying power and ground connections. They provide a stable power supply and reduce the noise and electromagnetic interference that can affect the operation of sensitive components.
3. **Inner Signal Layers:** Additional copper layers that carry signal traces.
4. **Prepreg:** Layers of insulating material that bond the copper layers together.
5. **Core:** The central layer of the PCB that accounts for most of the PCB's thickness and strength.

The PCB stack-up is particularly important in PCB layout of power supplies because it can significantly impact the power supply's performance, efficiency, and reliability. Below are some general guidelines when setting up the stack-up for a power supply design:

1. **Power Tracks:** Tracks that carry a significant amount of current can use all copper layers in parallel in their section of the PCB.
2. **Thermal Pads:** Same as power tracks, thermal pads can utilize all layers within their vicinity connected by multiple thermal vias to reduce thermal impedance between copper layers.
3. **Signal Traces and Ground Planes:** Signal traces can be placed on the outer or inner layers but must always be adjacent to an unbroken ground plane. Power planes are often not necessary within the layout of the power supply.
4. **High-Voltage Nodes:** Designing the PCB to minimize Conductive Anodic Filament (CAF) related failures is essential for power supplies with high voltage inputs. This can either be done through anti-CAF layout rules or the use of CAF-resistant laminates.

11.2 Conductive Anodic Filaments

Conductive Anodic Filaments (CAFs) are conductive pathways that can form between adjacent conductive layers in a printed circuit board (PCB). These pathways develop when an electrically conductive material, such as copper, begins to dissolve in the presence of moisture, oxygen, and electrical potential. The dissolved material can form a filament-like structure connecting adjacent conductive layers in the PCB.

CAFs can be a severe reliability issue for PCBs, particularly in applications where the PCB is exposed to moisture or high humidity. The formation of CAFs can lead to short circuits or other electrical failures, which can cause the PCB to malfunction or fail.

Several factors can contribute to the formation of CAFs, including the presence of contaminants or impurities in the PCB materials, exposure to moisture or high humidity, and the application of high voltage gradients. To mitigate the risk of CAFs, PCB designers and manufacturers must take several precautions, such as using high-quality materials with low ionic contamination, using protective coatings to prevent moisture ingress, and optimizing the PCB design.

Listed below are PCB design rules to minimize the risk of CAF formation:

1. For nodes with >600 V potential between them, the use of slots is preferred. If slots are impossible for space reasons, CAF holes can be implemented instead. The holes must be staggered, overlap by at least 10%, and be at least 2-3 rows, as shown in Figure 49.

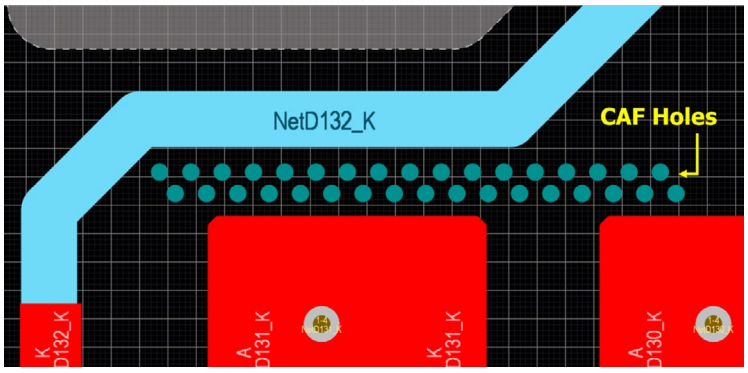


Figure 49. CAF Holes with Two Rows.

2. If the use of slots or CAF holes is not possible, the following distances between live nodes should be implemented:

   a. **Continuous voltage <250 V between nodes:**
   No minimum distance is required.

   b. **Continuous voltage from 250 V to 600 V:**
   Plated thru-hole or via to copper: ≥2.3 mm (ideally ≥ 3 mm)
   Copper to copper on the same layer: >1.5 mm
   Copper on different layers separated by at least two prepregs or one core: 0 mm

   c. **Continuous voltage from 600 V to 1500 V:**
   Plated thru-hole or via to copper:
   > 2.3 mm + (1 mm per 150 V above 600 V)
   Copper to copper:
   > 1.5 mm + (1 mm per 150 V above 600 V)

   d. **Continuous voltage above 1500 V:**
   Slots or CAF holes must be used. The slot is meant to deflect a CAF filament at least twice by 90°.

If it is impossible to follow the rules above, the design must be given special consideration. It may be best to perform a continuous test at high humidity and temperature (85°C/85%) to allow for a better assessment of the design.

11.3 Thermal Management Considerations

When designing for thermal management of the power supply, the following should be considered:

1. **Copper Area**
   Thermal impedance generally decreases as copper area is increased. However, the decrease in thermal impedance versus area follows an exponential curve. This means that at some point, further increases in the copper area will lead to less and less reduction in thermal impedance. The recommended maximum copper area for single-sided copper foils used for cooling is 600 mm^2 to 800 mm^2. A per-layer copper foil surface area between 1200 mm^2 to 2000 mm^2 is the recommended maximum for multiple-layer boards. The multiple layers should be tied using thermal vias to reduce the thermal impedance between layers.

The temperature gradient in a copper foil also exponentially decreases as the distance from the heat source is increased. Therefore, the cooling area should be as close to the heat source as possible.

2. **Thermal Vias**
   As mentioned above, the temperature gradient along the copper cooling area reduces exponentially with distance. Therefore, to effectively reduce thermal impedance, vias should be placed as close to the heat source as possible. If allowed, it is recommended that the thermal vias be placed on the pad of the InnoSwitch3-AQ SOURCE pin. When via-in-pad is used, counter measures must be taken to prevent solder wicking during assembly.

   Like the copper foil, the decrease in thermal impedance slows down as the number of vias increases. Therefore, putting excessively many thermal vias in the copper foil is unnecessary. Other factors that affect via thermal impedance are the following:

   a. Board thickness – thinner boards will have shorter vias leading to lower thermal impedance.
   b. Via diameter – Larger via holes have lower thermal impedance. 0.3 mm is the recommended maximum hole size for via in pad to reduce solder wicking.
   c. Via spacing – Via spacing should be between 1 mm to 1.5 mm. The recommended value is 1.2 mm. Spacing lower than 1 mm is not recommended due to increased cost but reduced benefits in thermal impedance reduction.

3. **Board Thickness**
   A thicker board will have a lower thermal impedance if the copper cooling area is small since thermal conduction in the horizontal direction will take precedence over vertical conduction. A thinner board is preferred if the copper area is large or in multiple layers and tied with vias since heat flow will be through the board instead of along the board.

4. **Heat Spreaders / Sinks**
   If the PCB copper area is not enough to cool the components in the power supply, the heat sources can be interfaced with a heat spreader or heat sink (usually the metal enclosure of the system) with a thermal pad. This will require component placement that will allow easy interfacing of the heat sources to the heat spreader. If this method of thermal management is used, ensure that the electrical isolation requirements are respected.

5. **Other Considerations**
   Multiple heat sources – If possible, keep heat sources away from each other to prevent hotspots. Care should be taken for high-power designs to manage the heat generated by the transformer and InnoSwitch3-AQ IC since both components are often located close to each other. The same is true for the SR FETs and output capacitors.

   Copper thickness – thicker copper foil will have lower thermal impedance. This is more apparent as the size of the copper area is increased.

   Track widths – For tracks that carry significant amounts of current, ensure that the track width and copper weight are enough to meet the required current carrying capacity without excessive heating.

12 Layout Examples

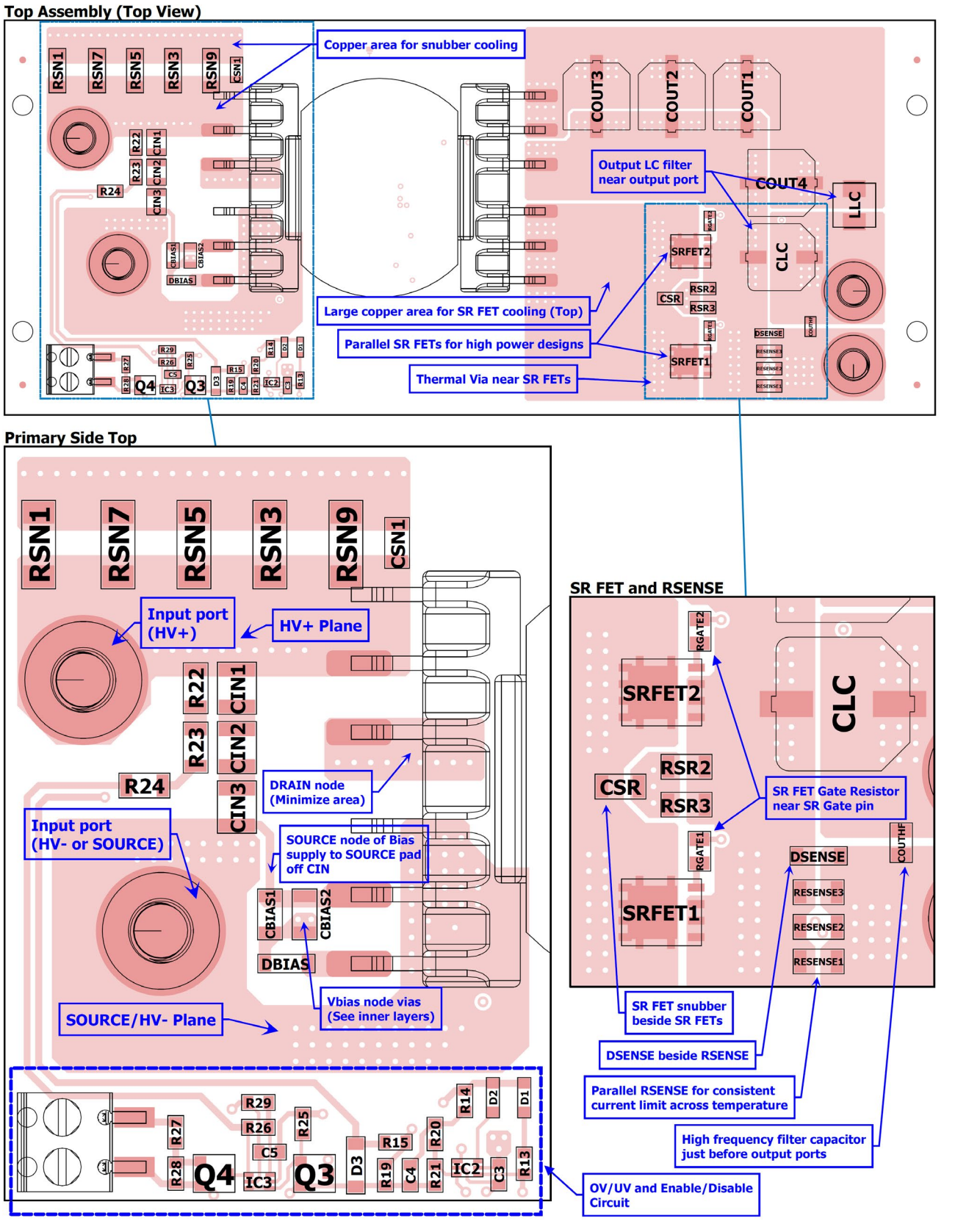


Figure 50. Layout Example Showing Implementation of Suggested Placement and Routing Guidelines. This Layout has Components on Both the Top and Bottom Layers (Top Assembly of DER-953Q).

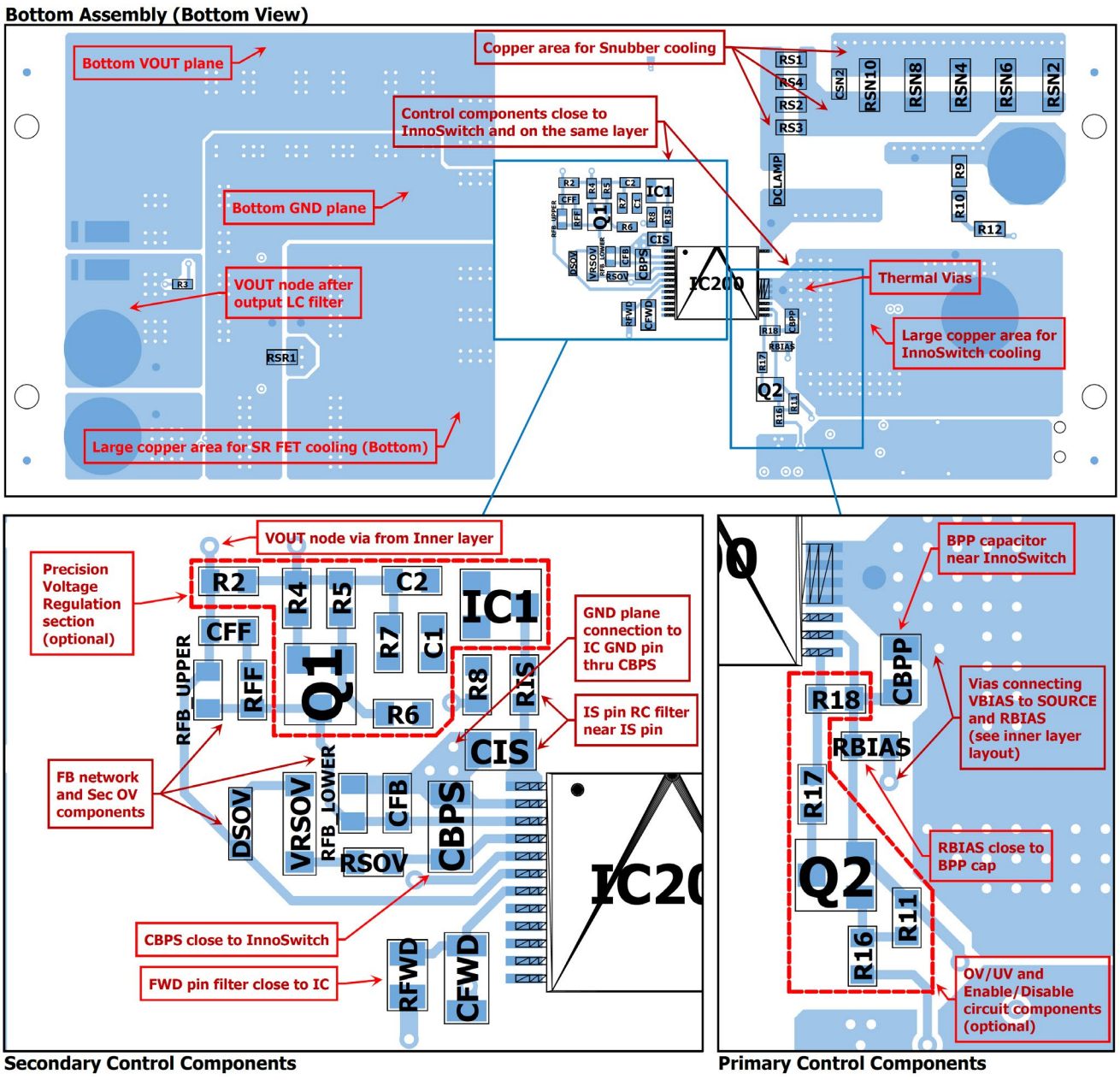


Figure 51. Layout Example Showing Implementation of Suggested Placement and Routing Guidelines. This Layout has Components on Both the Top and Bottom Layers. (Bottom Assembly of DER-953Q).

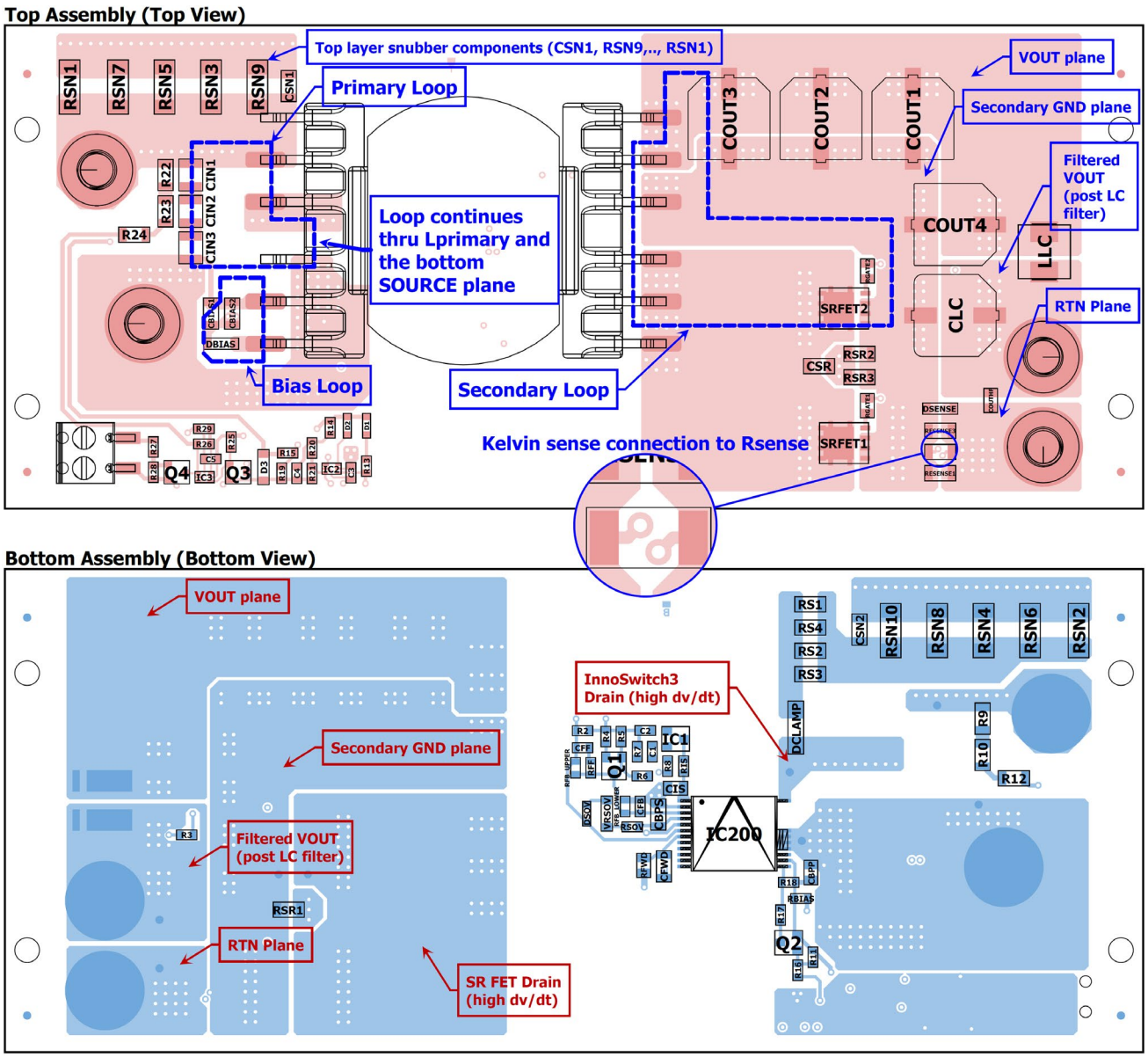


Figure 52. Current Loops and High dv/dt Nodes (DER-953Q Top and Bottom Assembly).

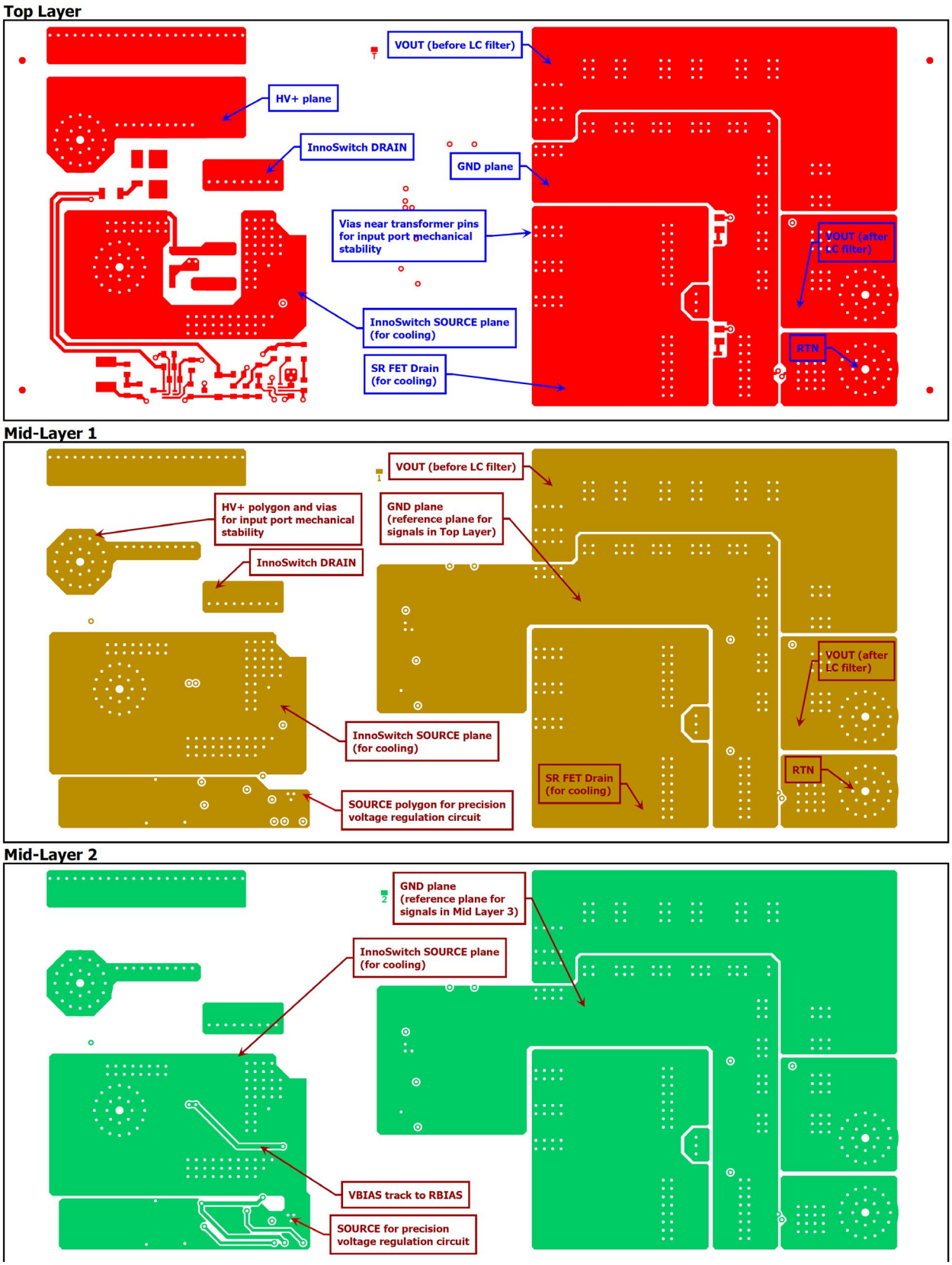


Figure 53. DER-953Q Copper Layers (Top, Mid-layer 1, Mid-layer 2).

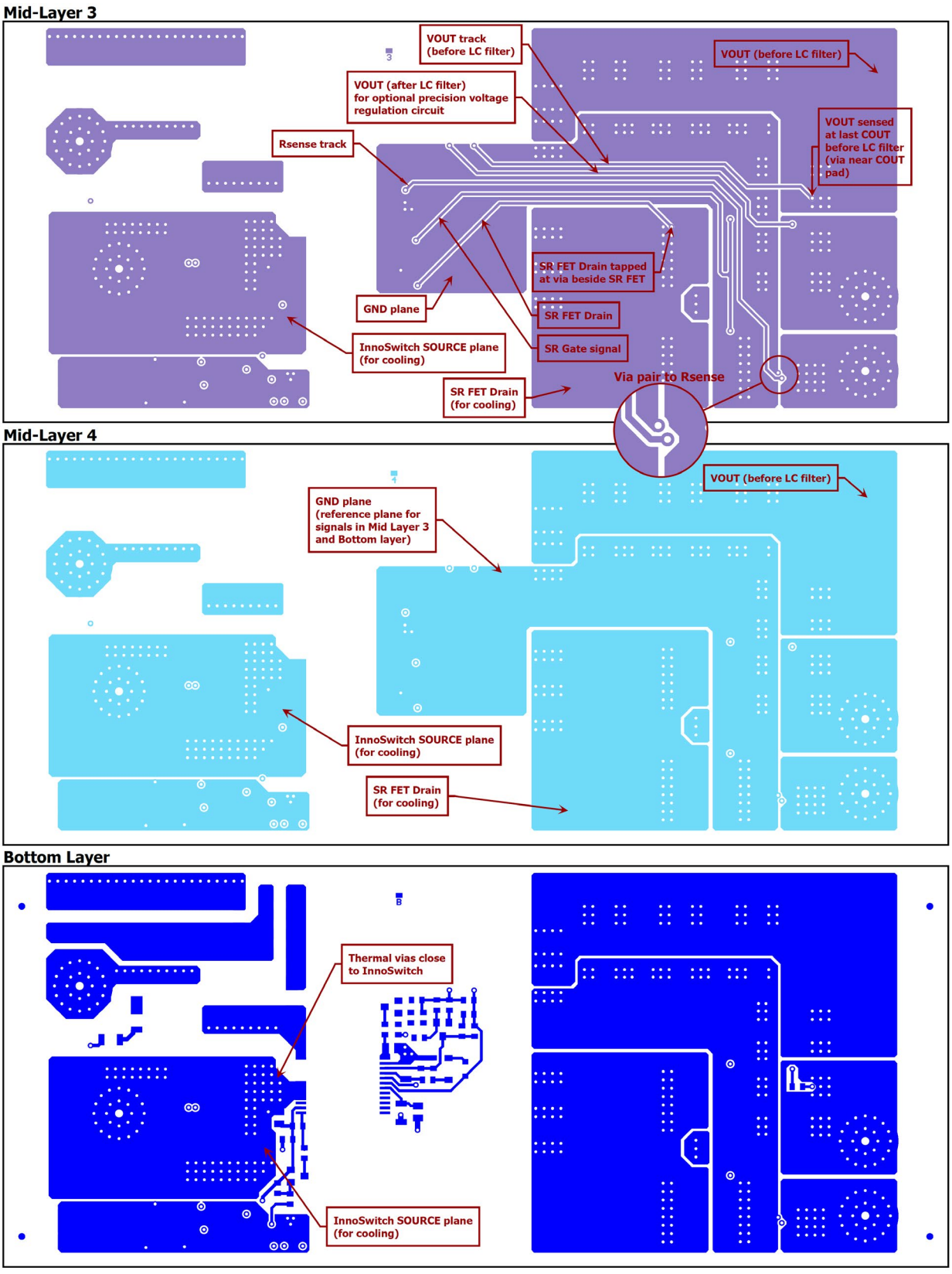


Figure 54. DER-953Q Copper Layers (Mid-layer 3, Mid-layer 4, Bottom).

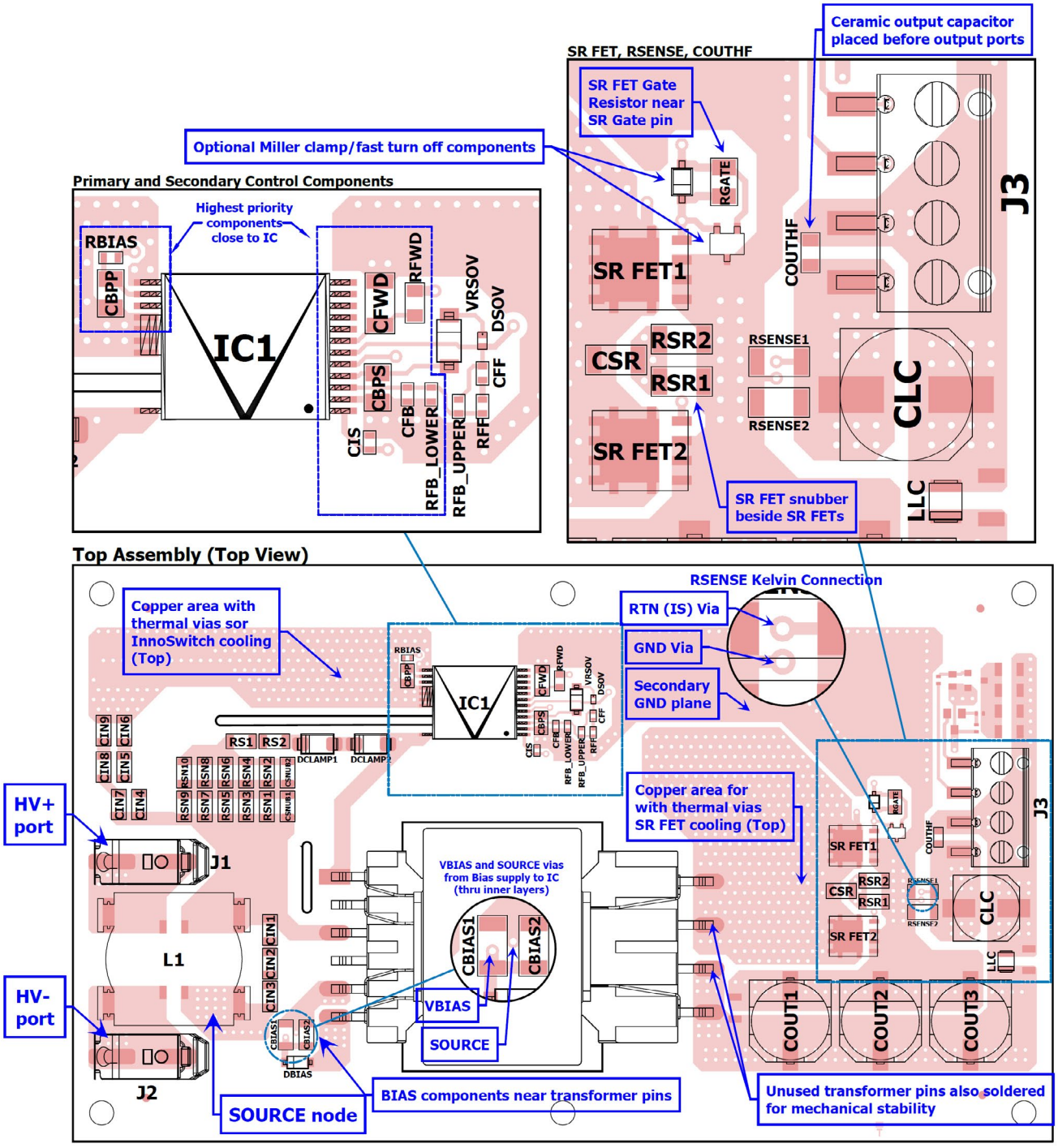


Figure 55. Layout Example for Design with Top Assembly Only (DER-948Q - Top).

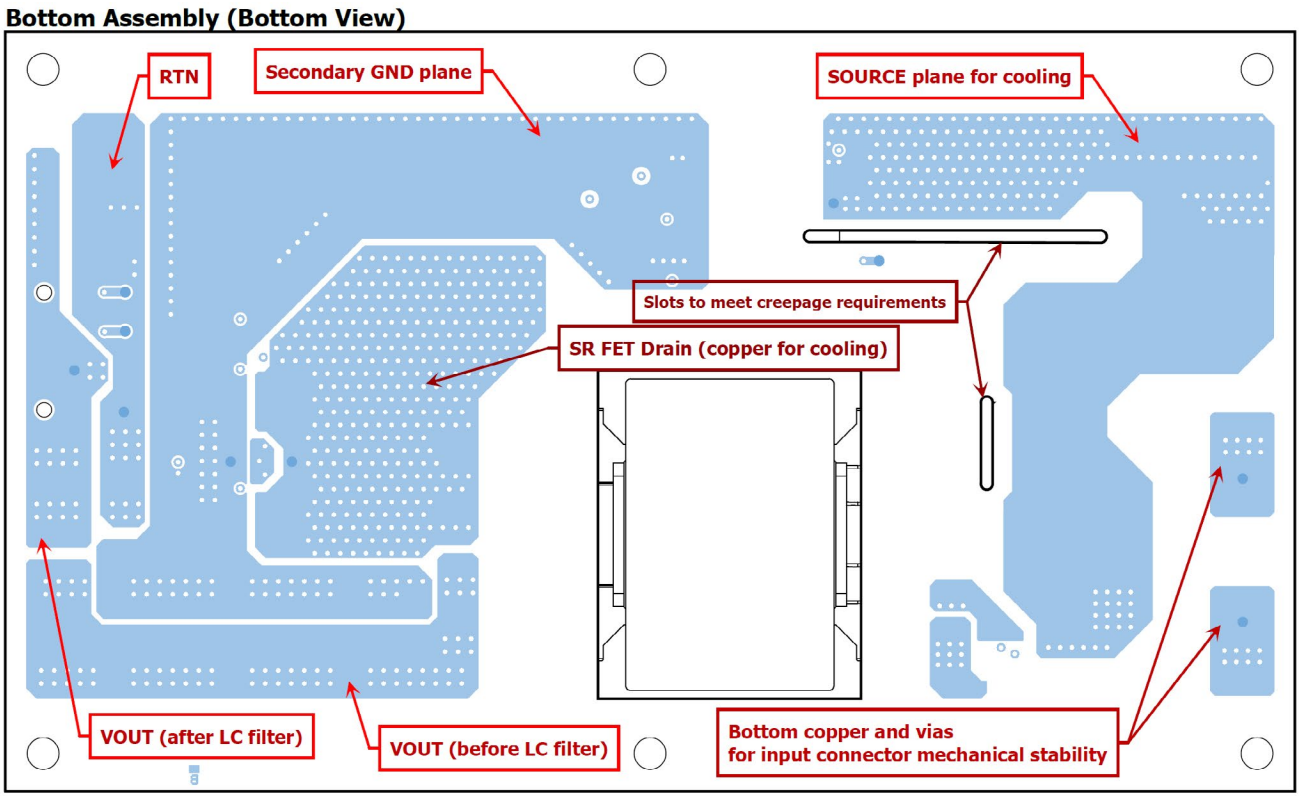


Figure 56. Layout Example for Design with Top Assembly Only (DER-948Q - Bottom).

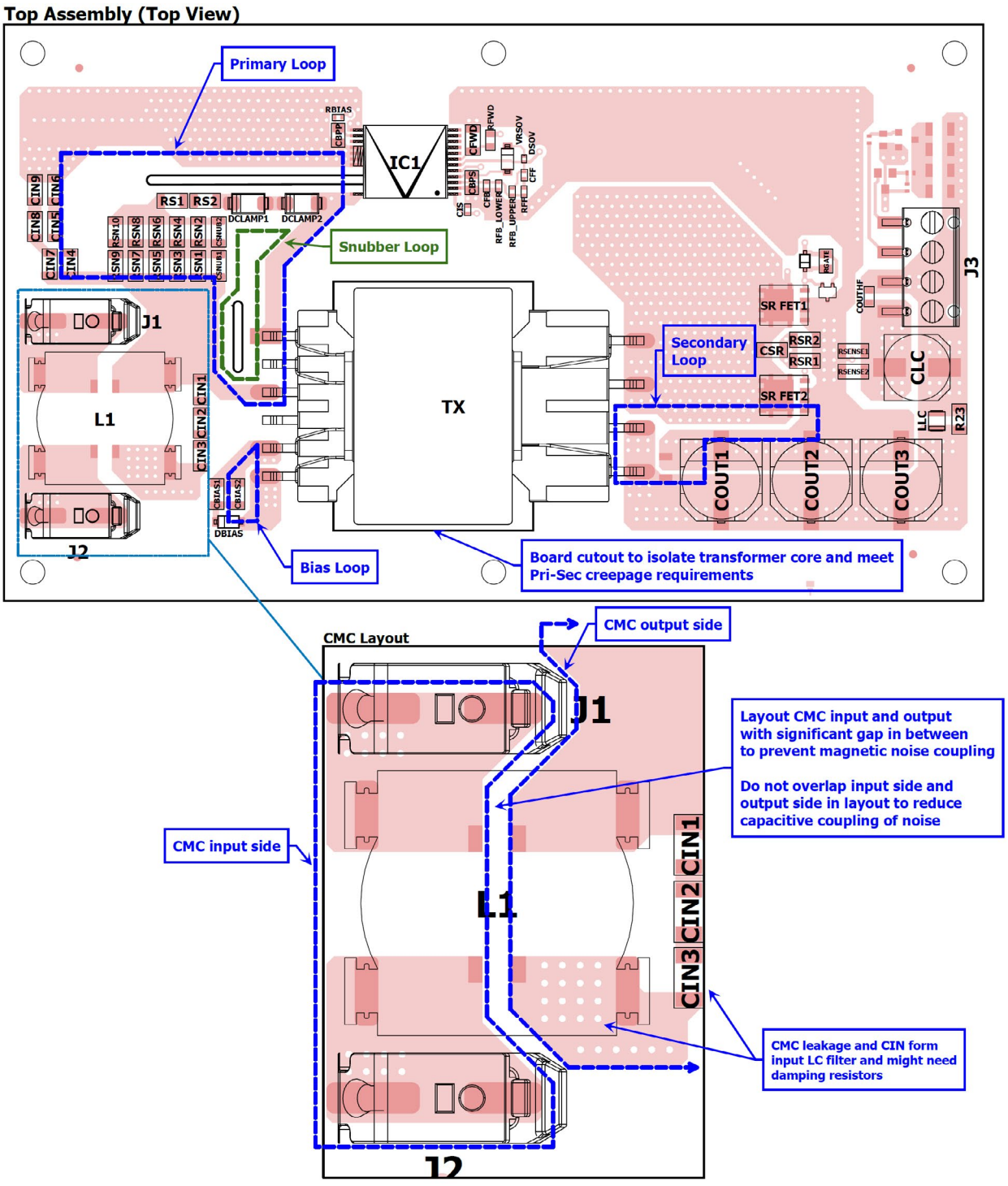


Figure 57. DER-948Q Layout Critical Loops and CMC Layout.

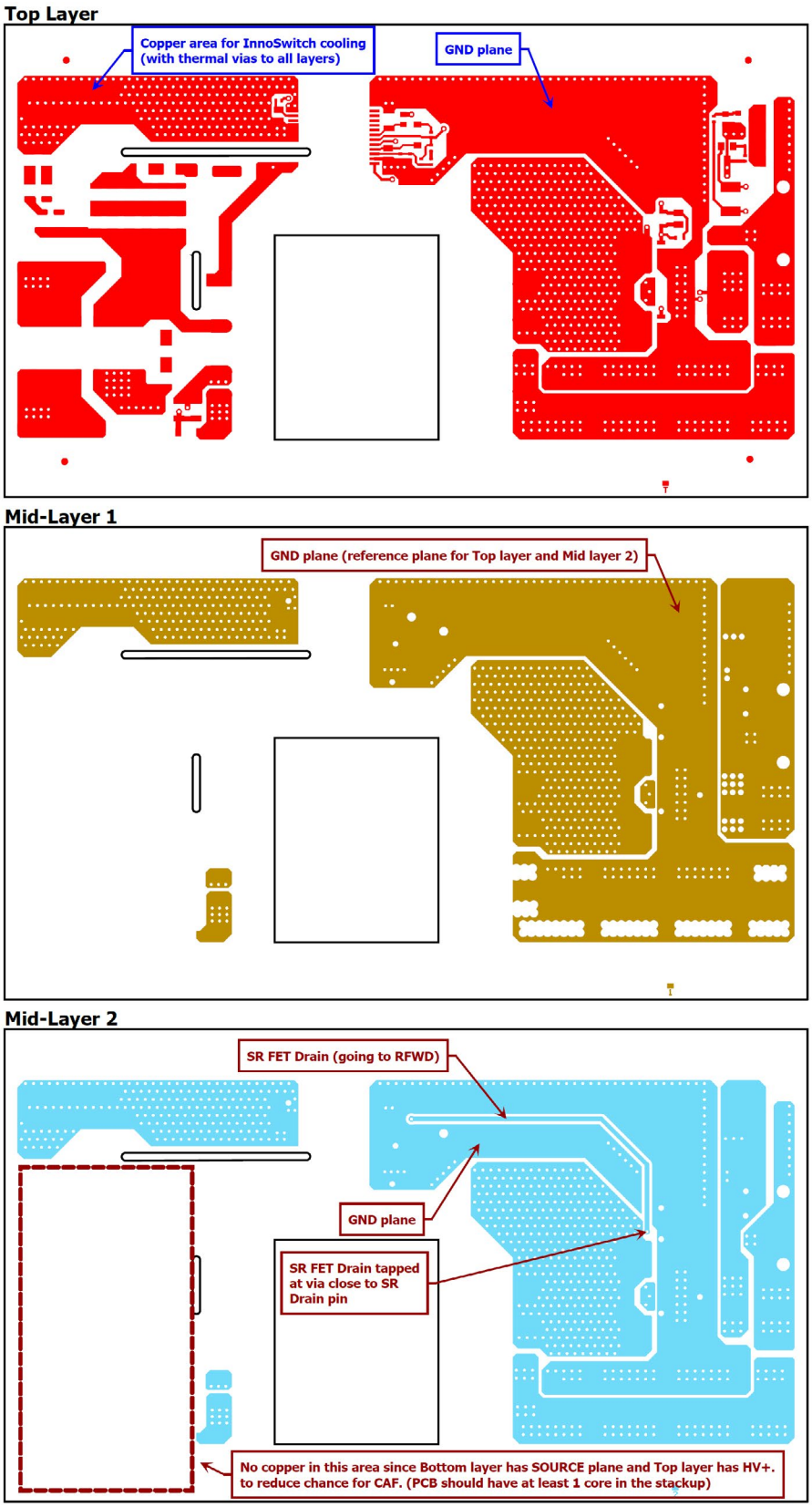


Figure 58. DER-948Q Copper Layers (Top to Mid layer 2).

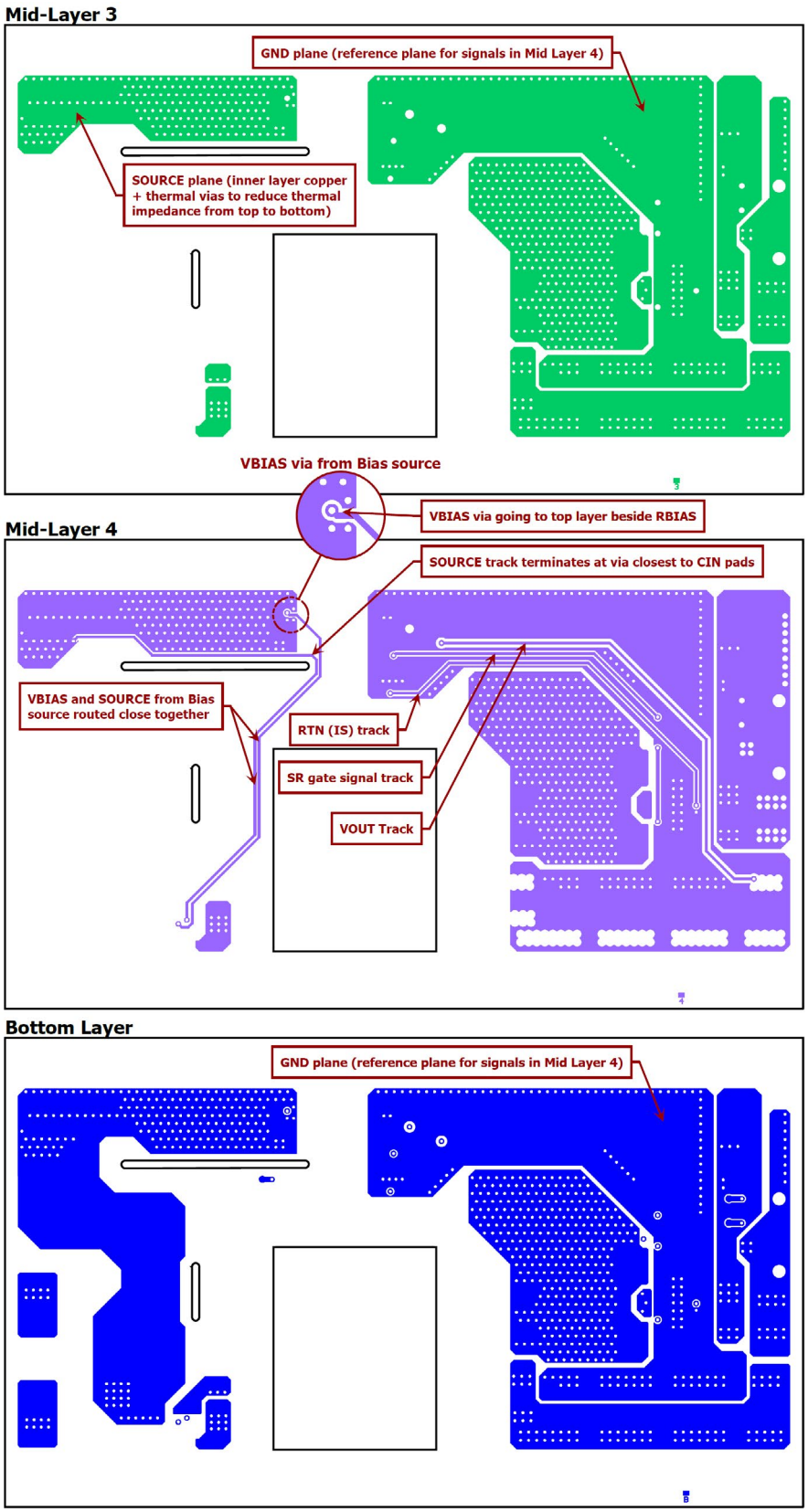


Figure 59. DER-948Q Copper Layers (Mid layer 3 to Bottom).

13 Design Verification Checklist

13.1 Design Stage

1. Check to ensure PIXIs shows no warnings. Use PIXIs to perform set-point analysis and confirm values are within the expected range (e.g., for high V_{IN} designs, verify switching frequency is below 30 kHz at V_{IN} = 1000 V, full load if clearance/creepage is only based on IEC 60664-1)
2. Draw the schematic and apply component selection and derating rules. Maximum voltage, current, and power stresses should be calculated across all temperatures and component tolerances. This will prevent either undersized components (leading to failures) or oversized ones (unnecessary cost) from being used.
3. Build a prototype transformer and measure the leakage inductance to verify the snubber components calculated. If necessary, build multiple prototype transformers to ensure values are repeatable. Re-calculate snubber components and adjust the schematic as necessary.
4. Generate PCB layout following the guidelines listed in Section 10 of this document. It is recommended that all rules, such as clearance/creepage, component distance, track widths, etc., be encoded in the PCB layout software and periodically checked to ensure no violations.

13.2 Prototype Stage

1. Once a prototype unit is built, verify electrical stresses across critical components to confirm stresses are within limits. Testing should be done across all line, load, and temperature conditions. It is recommended that the following signals be monitored during testing to ensure the unit is operating as expected.
    a. InnoSwitch3-AQ V_{DS} and I_{DS}
    b. SR FET V_{DS} and I_{DS}
    c. FWD pin voltage (if SR FET V_{DS} contains spikes >150 V)
    d. V_{BIAS} to check acceptable cross-regulation and correct OVP voltage level if primary-sensed OVP is used.
    e. BPP voltage to check if the bias supply provides enough current to turn off the internal tap of the IC.

Stresses should also be measured at start-up and during special conditions such as short circuit events.

2. Verify that performance parameters are within specifications. Critical parameters to test that might need adjustment during this stage are:
    a. Output voltage regulation and ripple
    b. Efficiency
    c. Thermals
    d. Transient response

3. Verify that protection features are working, including but not limited to:
    a. Primary and secondary OVP
    b. Over-current protection
    c. Over-temperature protection
    d. Short-circuit protection

14 Troubleshooting Guide

Troubleshooting Guide					
Issue Observed		**Possible Cause/Unsatisfied Requirement**		**Recommendation**	**Page**
Auto-Restart		Incorrect BPS capacitor or BPS capacitor is damaged or disconnected		BPS capacitor needs to be at least 2.2 uF, 0805, 25 V, X7R/C0G. Check if BPS is ok and properly connected to the IC	30
		Incorrect transformer design		Confirm with transformer design in PIXIs (i.e., L_P, F_{SW}, $T_{ON(MIN)}$	13-15
				Confirm transformer construction (i.e., reversed polarity winding termination)	-
				Confirm if there are any external shorts on all windings	-
		Damaged SR FET		Check if SR FET D-S is shorted or G-S is open	-
		False secondary overvoltage fault		Confirm the values of the feedback resistors	17
				Confirm the values of the secondary OVP Resistor and Zener diode breakdown voltage	45
Auto-Restart at Certain Loading Condition		False overload fault	Noisy IS pin	Add / increase capacitance value across IS pin	5
				Add a series resistor to the IS pin for RC filtering	5
			Noisy IS pin due to R_{SENSE} placement	Placing the R_{SENSE} after the output LC filter (if used in the design)	55
				Keep R_{SENSE} far from noisy elements such as the secondary snubber circuit	55
			During high-temperature testing	Increase the number of parallel resistors or use a lower tolerance resistor series	-
Output Voltage is Out of Regulation	During standalone operation	Incorrect feedback resistor values		Confirm the values of the feedback resistors with PIXIs	17
		Tight regulation requirements which IC internal control is unable to handle		Consider using an external Precision Voltage Regulation Supplementary Circuit	48
		InnoSwitch pulse bunching	Input oscillation from CMC and CIN resonance	Add damping resistors in parallel with CMC windings for dampening	38
			Due to oscillation from the secondary winding leakage and CSR Resonance	Modify the transformer to reduce secondary leakage inductance or decrease C_{SR}	-
	During inverter operation	Incorrect secondary RTN loop		Ensure proper return loops on the secondary domain, especially when chassis ground is present	-
		Noise in the FB pin		Place feedback resistors and capacitor network as close as possible to the FB and GND pins	55
		Magnetic field coupling into the InnoSwitch, especially when placed near the DC Link Capacitor		Use copper shielding over InnoSwitch connected to HV-	-

Issue Observed		Possible Cause/Unsatisfied Requirement		Recommendation	Page
Output Voltage Ripple is out of Specification		Tight output dynamic and static voltage ripple requirement		Add a feed-forward network across the feedback network with starting value of 10 k and 10 nF, then adjust as needed	-
				Add an output LC filter	-
				Increase output capacitance for better dynamic output voltage ripple	-
				Check probing technique for voltage ripple measurements (i.e., short loop probe, 1 µF parallel capacitor)	-
		High ESR of output capacitor		Consider using polymer type capacitor with lower ESR value	34
Overheating Components	InnoSwitch	During normal operation	High switching losses, especially at high input voltage	Consider lowering F_{SW} operation and confirm with PIXIs	13
			Insufficient current flowing into BPP pin	Check if the value of R_{BIAS} is enough to supply the required BPP current	29
		During start-up and InnoSwitch is disabled	Continuous high current drain tap operation during disabled state	Use supplementary Disable Circuit Resolved internally with new chip version	47
	Snubber Resistors	Insufficient heat sinking or package power capacity		Ensure enough are for heat sinking and using larger resistor package such as MELF type	28
	Primary Snubber Diode	Slow diode reverse recovery time (t_{RR})		Use fast recovery diode, ideally t_{RR} ≤ 75 ns	28
High Component Stresses	InnoSwitch	Insufficient voltage limiting of the snubber circuit		Increase snubber capacitance while also increasing the power capacity of the snubber resistor	28
		High V_{OR} value		Decrease V_{OR} value but taking into account the 150 V maximum voltage rating of the FWD pin	14
		Slow diode reverse recovery time (t_{RR}) of snubber diode		Use fast recovery diode, ideally t_{RR} ≤ 75 ns	28
		Inverted transformer windings		Confirm transformer construction	-
	SR FET	Insufficient voltage limiting of the snubber circuit		Increase snubber capacitance while also increasing the power capacity of the snubber resistor	32
	Input capacitor during start-up	Excessive inrush current during start-up due to high dv/dt		Add limiting resistor with high pulse power capacity in series between DC-Link capacitor and input capacitor	-

Issue Observed	Possible Cause/Unsatisfied Requirement	Recommendation	Page
Unable to start-up with slow ramp input voltage under 30 V	InnoSwitch primary control latches off due to internal logic	Use supplementary start-up circuit	47
Input UV/OV is needed as a requirement	Accurate cut-in/off voltage requirements which IC internal control is unable to handle	Use supplementary UV/OV circuit	47
Oscillations seen on gate driver signals during inverter operation (for GDU using InnoSwitch-AQ IC as power supply)	InnoSwitch3-AQ IC is powered through the module's auxiliary pin	Connect InnoSwitch3-AQ IC input directly to the DC-Link capacitor or include a differential and common mode choke before the input capacitor	37
Output power requirements cannot be met at lower voltages	Transformer design may be optimized for high voltage input and will be limited by t_{OFFMIN})	Confirm with PIXls transformer design. V_{OR} may be decreased to meet the requirements	15
Unusual oscillation and peaking on the InnoSwitch-AQ IC Drain-Source voltage during relaxation ring	InnoSwitch3-AQ IC enters drain-tap operation to power the primary-side controls via the input drain pin	Confirm if the value of R_{BIAS} is enough to supply the required BPP current	29

Revision	Notes	Date
A	Initial release.	09/23
B	Layouts, figures and equation updates.	01/24
C		03/24

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