Application Note AN-112
TinySwitch-5 Family

Design Guide

Introduction

TinySwitch™-5 family of ICs are highly integrated monolithic off-line switcher devices for power supplies in the range of 10 W to approximately 190 W output. Devices within the TinySwitch-5 family can deliver 120 W for universal input voltage range (85 VAC – 265 VAC), 175 W for high-line input (230 VAC), and 190 W when operating from a PFC input delivering 400 VDC. TinySwitch-5 parts are available with 3 high power IC packages - eSOP-12B, eDIP-12B, eSIP-7C. Applications include auxiliary, standby and bias power supplies for appliances and consumer products. TinySwitch-5 ICs can also be used in utility meter, smart grid, and industrial power supplies and for power tools.

TinySwitch-5 devices combine a high-voltage (725 V) power MOSFET switch with a controller that provides a variable frequency, variable peak-current control scheme which ensures very high conversion efficiency across the load range. TinySwitch-5 based designs can seamlessly transition between DCM and CCM operating modes. Jitter is added to the switching frequency to reduce EMI. Start-up current is drawn internally from the DRAIN pin, eliminating the need for external start-up components. An integrated soft-start minimizes component stress when power is applied. The primary current limit is selectable (without extra components which increases design flexibility. Input protection includes Line undervoltage (UV) detection which prevents output glitches during power-up plus line overvoltage (OV)shutdown which increases protection from line surge and mis-wire. In addition the auto-restart limits output power to < 3% during overload and output short-circuit events. Over-temperature protection interrupts switching during thermal overload. The high thermal shutdown threshold is ideal for applications where the ambient temperature is high while the large hysteresis protects the PCB and surrounding components from the effects of excessive average temperatures during fault conditions.

The TinySwitch-5 IC family is ideal for applications requiring high average power efficiency. Power Integrations' EcoSmart™ technology used in TinySwitch-5 enables designs that provide more than 210 mW output power for 300 mW input power (230 VAC) during standby and consumer less than 30 mW during no-load operation. This makes the family ideal for applications that must meet energy efficiency standards such as the United States Department of Energy DoE 6, California Energy Commission (CEC) requirements and the European Code of Conduct.

The design of flyback power supplies is a highly iterative process with multiple variables that must be reviewed and adjusted to optimize the design. The design methodology described in this document consists of a quick start guide which utilizes the Power Integrations design software (PI Expert™), a simplified step-by-step design procedure describes key application design considerations and recommendations, lays out a quick design checklist, and provides application examples. The quick start, with which the engineer may opt to rapidly design and select a transformer. The step-by-step design procedure guides the engineer from a set of given system requirements all the way to the completion of the power supply using the most appropriate TinySwitch-5 device. This also includes lookup tables and utilizes the powerful PIXls design tool that is part of the PI Expert software suite. The section on design considerations and recommendations provides engineers with critical design optimization ideas and guidance. The quick design checklist provide a list of recommend tests to perform before proceeding to full circuit evaluation. Finally, the section on application examples describes an actual reference design using a TinySwitch-5 device analyzing operation and sharing performance data.

Features	TinySwitch-III	TinySwitch-4	TinySwitch-5
BVDSS, Breakdown Voltage	700 V	725 V	725 V
Full Load Switching Frequency	132 kHz	132 kHz	30 kHz to 150 kHz
Soft Start	N/A	N/A	Yes
Line Undervoltage Protection	Yes	Yes	Yes
Line Overvoltage Protection	N/A	N/A	Yes
Line Compensated OCP	N/A	Yes	N/A
Surface Mount	Yes	Yes	Yes
Thru Hole Mount	N/A	N/A	Yes
Packages	DIP-8C SO-8C	DIP-8C SO-8C eSOP-12B	eSIP-7C eDIP-12B eSOP-12B
Universal Input Max Output Power	28.5 W	28.5 W	120 W

Table 1. Feature Comparison of TinySwitch Family of Devices.

Basic Circuit Configuration

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach, and can use the following information to quickly design the transformer and select components for a first prototype.

For this approach, only the information described below needs to be entered into the PIXls spreadsheet, other parameters will be automatically selected based on a typical design. References to spreadsheet line numbers are provided in square brackets [line reference]

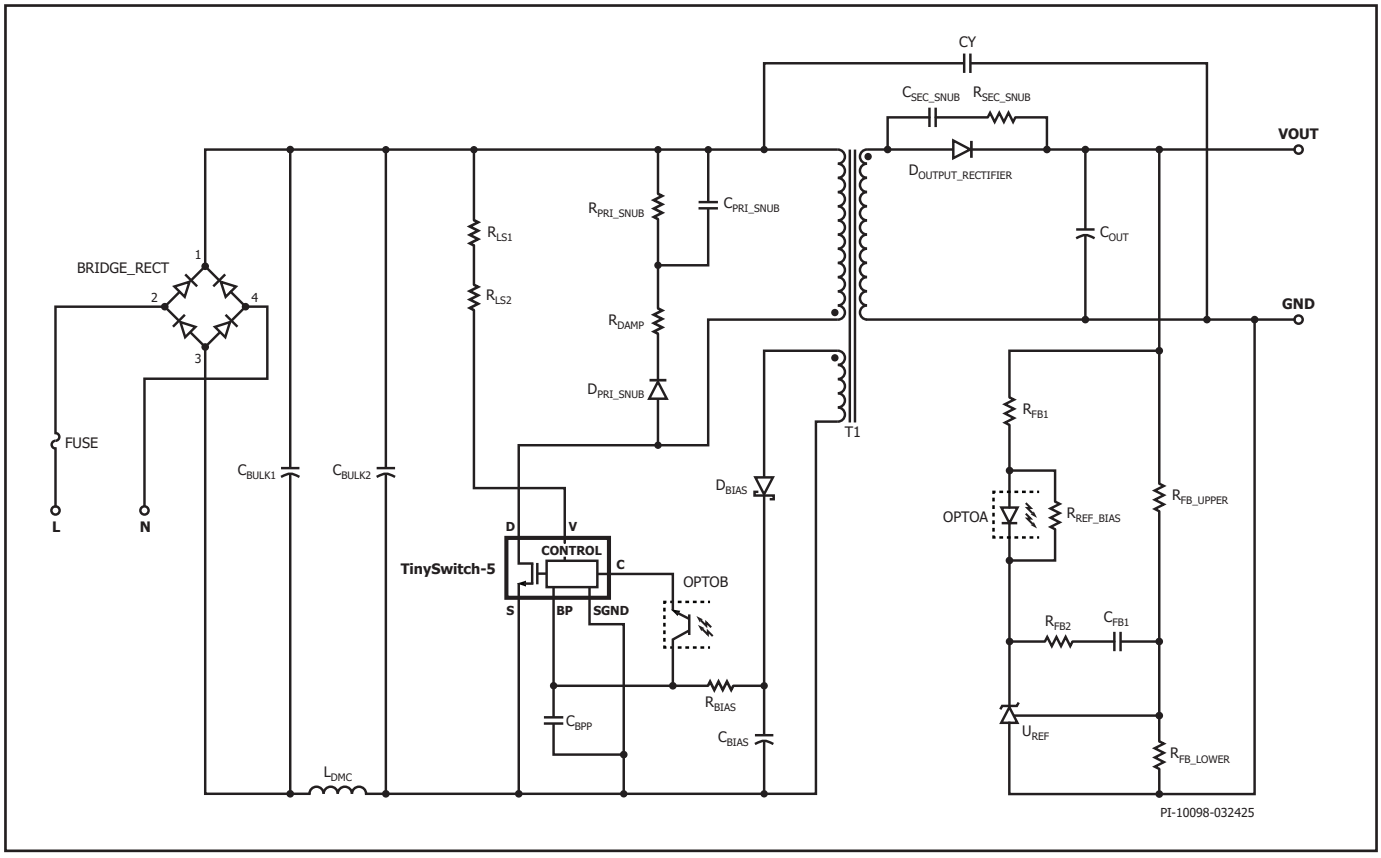


Figure 1. Typical Power Supply Schematic using a TinySwitch-5 device with Line Undervoltage Lockout and Line Overvoltage Shutdown.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply or charger using the TinySwitch-5 family of devices. It provides guidance which enables an engineer to quickly select key components and complete a suitable transformer design. To help simplify the task, this application note refers directly to the PIXls design spreadsheet that is part of the PI Expert design software suite available online (free download from https://piexpertonline.power.com/site/login). The basic configuration used in TinySwitch-5 IC-based flyback power supplies is shown in Figure 1, which also serves as the reference circuit for component identification that is used in descriptions throughout this application note.

In addition to this application note, there is the TinySwitch-5 Design Examples Reference (DER) and Reference Design Kit (RDK) containing an engineering prototype board as well as device samples that provides an example of a working power supply. Further details on downloading PI Expert, obtaining an RDK and updates to this document can be found at www.power.com.

- Enter INPUT_TYPE [B3]. Select if input is AC or DC
- Enter AC/DC input voltage range and line frequency, VIN_MIN [B4],
- VIN_MAX [B5], LINEFREQ [B7]
- Enter input capacitance, CAP_INPUT [B8]
  - 2-3 μF / W for universal (85-265 VAC) or single (100/115 VAC) line. Higher input capacitance is recommended for higher efficiency provided that increased cost and capacitor dimensions are acceptable. A more aggressive value of 2 μF / W can be used for designs that do not need to meet a hold-up-time requirement.
  - Use 1 μF/W for 230 VAC (185-265 VAC) line.
  - If this cell is blank, the input capacitance will be 2 times the output power for low-line and universal input and 1 times the output power for high-line input in microfarads.
- Enter nominal output voltage, VOUT [B9]
- Enter continuous output current, IOUT [B10]
- Enter efficiency estimate, EFFICIENCY [B12]
  - 0.87 for universal input voltage (85-265 VAC) or low-line input 100/115 VAC (85-132 VAC) and 0.89 for a high-line input 230 VAC (185-265 VAC) design. Adjust the number accordingly after measuring the efficiency of the first prototype-board at maximum load and VIN_MIN.

- Select power supply enclosure, ENCLOSURE [B14]
- Select device package options, PACKAGE_DEVICE [B19]
- Select the TinySwitch-5 device from the drop-down list or enter directly [B21]
  - Select the device from Table 1 according to output power and input voltage.
- Enter desired maximum switching frequency (30 kHz to 130 kHz) at full load, FSWITCHING_MAX [B35]
- Enter core type (if desired), from drop down menu CORE [B63]
  - Suggested core size will be selected automatically if none is entered [B63]
  - For custom core, enter CORE CODE [B64], and core parameters from [B65] to [B72]
- Enter secondary number of turns [B88]

If any warnings are generated, make changes to the design by following instructions in spreadsheet column D.

- Build transformer as suggested in "Transformer Construction" tab
- Select other components.
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were initially used (e.g. efficiency, V_{MIN}). Note that the efficiency estimate provided by the tool for the first prototype is very conservative.

Output Power Table[1]

Product[3]	PCB Copper Area[1]			Product[3]	Metal Heatsink[1]		
	400 VDC	230 VAC ±15%	85-265 VAC		400 VDC	230 VAC ±15%	85-265 VAC
	Peak or Open Frame[2,3]	**Peak or Open Frame[2,3]**	**Peak or Open Frame[2,3]**		**Peak or Open Frame[2,3]**	**Peak or Open Frame[2,3]**	**Peak or Open Frame[2,3]**
TNY5071K	25 W	22 W	15 W				
TNY5071V	25 W	22 W	15 W				
TNY5072K	35 W	32 W	20 W				
TNY5072V	35 W	32 W	20 W				
TNY5073K	50 W	45 W	30 W				
TNY5073V	50 W	45 W	25 W				
TNY5074K	60 W	55 W	35 W				
TNY5074V	60 W	55 W	30 W				
TNY5075K	75 W	70 W	45 W				
TNY5075V	75 W	70 W	40 W	**TNY5075E**	120 W	105 W	70 W
				TNY5076E	170 W	155 W	105 W
				TNY5077E	190 W	175 W	120 W

Table 2. Output Power Tables of TinySwitch-5

Notes:

1. The Table 1 represents maximum practical continuous output power based on the following assumptions:
   a. 12 V output.
   b. Schottky or high-efficiency output diode.
   c. 130 V reflected voltage (VOR) and 85% efficiency.
   d. A 100 VDC minimum DC bus voltage for 85-265 VAC and 300 VDC bus voltage for 230 VAC.
   e. Sufficient heatsinking to keep device temperature ≤110 °C.
   f. Power levels shown in the power table for the V package device assume 19.4 cm^2 of 610 g/m^2 copper heatsink area.
   g. Maximum continuous power for an open frame design operating in a +50 °C ambient.
2. Minimum peak power capability.
3. Packages: E: eSIP-7C, V: eDIP-12B, K: eSOP-12B.

Step-by-Step Design Procedure

This design procedure uses the PI Expert design software (available as a free download from Power Integrations), which automatically performs the key calculations required for TinySwitch-5 IC-based flyback power supply design. PI Expert allows designers to circumvent the typical highly iterative power supply design process. Look-up tables and empirical design guidelines are provided where appropriate in this procedure to simplify the design task.

Adjust the design to eliminate warnings. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right-hand column. Once all warnings have been cleared, the output transformer design parameters and manufacturing information provided by PI Expert can be used to create a prototype transformer.

Step 1 – Application Variables

Enter: INPUT_TYPE, VIN_MIN, VIN_MAX, LINEFREQ, CAP_INPUT, VOUT, IOUT, EFFICIENCY, FACTOR_Z, and ENCLOSURE

INPUT TYPE
Select AC for application using AC input voltage and DC for application with PFC input.

Minimum and Maximum Input Voltage, V_{MIN}, V_{MAX} (VAC or VDC)
Determine the input voltage range from Table 4 for a particular regional requirement.

Line Frequency, f_L
60 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate design margin. For absolute worst-case operating conditions or to match a power supply specification reduce these numbers by 6% (47 Hz or 56 Hz).

Total Input Capacitance, C_{AP_INPUT} (µF)
Enter total input capacitance using Table 3 for guidance. The capacitance is used to calculate the minimum DC voltage across the bulk capacitor. It is recommended to use at least 2 µF/W to maintain the DC bus voltage above 90 V, though 3 µF/W provides a more typical margin. The ripple on the DC bus should be measured to confirm the suitability of the transformer primary-winding inductance selected.

Nominal AC Input Voltage (VAC)	Total Input Capacitance per Watt Output Power (µF/W)
100 / 115	>2
Universal	>2
230	>1

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

2	APPLICATION VARIABLES	INPUT	INFO	OUTPUT	UNITS	Design Title
3	INPUT_TYPE	AC	AC	AC		Input Type
4	VIN_MIN	85	85	85	V	Minimum AC input voltage
5	VIN_MAX	265	265	265	V	Maximum AC input voltage
6	VIN_RANGE		85-265 VAC	85-265 VAC		Range of AC input voltage
7	LINEFREQ		60	60	Hz	AC Input voltage frequency
8	CAP_INPUT	82.0	82.0	82.0	µF	Input capacitor
9	VOUT	12.00	12.00	12.00	V	Output voltage at the board
10	IOUT	3.000	3.000	3.000	A	Output current
11	POUT		36.00	36.00	W	Output power
12	EFFICIENCY	0.86	0.86	0.86		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z		0.50	0.50		Z-factor estimate

Figure 2. Application Variable Section of TinySwitch-5 Design Spreadsheet. Note the Gray Override Cells which Allow the User to Specify Values.

Region	Nominal Input Voltage (VAC)	Minimum Input Voltage (VAC)	Maximum Input Voltage (VAC)	Nominal Line Frequency (Hz)
Japan	110, 230	85	265	50 / 60
United States, Canada	110, 230	90	265	60
Australia, China, European Union Countries, India, Korea, Malaysia, Russia	230	90	265	50
Rest of Europe, Asia, Africa, Americas and rest of the world	115, 120, 127 220, 230 240	90 185 185	155 265 265	50 / 60 50 / 60 50

Table 4. Guide to Typical line Voltage Conditions Encountered in Different Geographic Regions.

Nominal Output Voltage, V_{OUT} (V)
Enter the nominal Output voltage of the main output at full load. Usually for a multi output power supply, the main output is the output from which feedback is derived.

Power Supply Output Current, I_{OUT} (A)
This is the maximum continuous load current of the power supply. If the power supply has multiple outputs, enter the output current which allows the product of VOUT and IOUT will match the intended total output power.

Output Power, P_{OUT} (W)
This is a calculated value and will be automatically adjusted.

Power Supply Efficiency, (η)
Enter the estimated efficiency of the complete power supply measured between the input and output terminals under peak load conditions and worst-case line (lowest input voltage). Use a value of 0.86 if no other data is available. Once a prototype has been constructed the measured efficiency should be entered, and further transformer iteration(s) can be performed if necessary.

Power Supply Loss Allocation Factor, FACTOR_ Z
This factor describes the apportioning of losses between the primary and the secondary sides of the power supply. Z factor is used together with the efficiency to determine the actual power that must be delivered by the power stage. This is required because losses in the input stage (EMI filter, rectification etc.) are not processed by the power stage (transferred through the transformer) and so although they reduce efficiency the transformer design is not affected.

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

For designs that do not have a peak power requirement, a value of 0.5 is recommended. For designs with a peak power requirement enter 0.65. The higher number indicates the increased secondary-side losses typically seen with peak-power designs.

Step 2 – Primary Controller Selection

Enter: Generic Device Code, DEVICE_GENERIC

18	PRIMARY CONTROLLER SELECTION	INPUT	INFO	OUTPUT	UNITS	Design Title
19	DEVICE_SERIES	AC		TNY5075		Generic device code
20	PACKAGE_DEVICE	265		eSOP	V	Device Package
21	DEVICE_CODE			TNY5075K		Actual device code
22	POUT_MAX			45	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			3.10	Ω	Primary switch on time drain resistance at 100 ºC
24	ILIMIT_MIN			1.104	A	Minimum current limit of the primary switch
25	ILIMIT_TYP			1.200	A	Typical current limit of the primary switch
26	ILIMIT_MAX			1.296	A	Maximum current limit of the primary switch
27	VDRAIN_BREAK			725	V	Device breakdown voltage
28	VDRAIN_ON_PRSW			1.37	V	Primary switch on-time drain voltage
29	VDRAIN_OFF_PRSW			523.4	V	Peak drain voltage on the primary switch during turn-off. A 50 V leakage spike voltage is assumed

Figure 3. Primary Controller Selection in the TinySwitch-5 Family Design Spreadsheet.

Generic Device Code, DEVICE_SERIES
The default option is automatically selected based on input type, input voltage range, and maximum output power.

For manual selection of device size, refer to the TinySwitch-5 power table from Table 2 and select a device based on the input type and output power. If the continuous power exceeds the value given in the power table (Table 2), then the next larger device should be selected. If the continuous power is close to the maximum power given in the power table, it may be necessary to switch to a larger device based on the actual measured thermal performance of the prototype.

IC Package, PACKAGE_DEVICE
The designer can select preferred IC package either eSOP, eDIP, or eSIP. TinySwitch-5 provides options for either reflow (eSOP) or wave (eDIP or eSIP) soldering processes. For higher power, eSIP is recommended as it supports a simpler option for heatsink mounting.

On-Time Drain Voltage, VDRAIN_ON_PRSW (V)
This parameter is calculated based on RDSON_100DEG and primary RMS current.

Drain Peak Voltage, $V_{DRAIN\_OFF\_PRSW}$ (V)
This parameter is the assumed Drain voltage seen by the device during off-time. A warning will be shown if this parameter exceeds 650 V (90% voltage derating). The calculation assumes a 50 V leakage spike.

$$V_{DRAIN} < (VIN\_MAX \times 1.414) + VOR + VLK_{PRI}$$

$V_{(LK-PRI)}$ is the voltage induced by the leakage inductance of thetransformer when MOSFET turns-off.

Other data sheet electrical parameters are displayed **POUT_MAX, RDSON_100DEG, ILIMIT_MIN, ILIMIT_TYP, ILIMIT_MAX, VDRAIN_BREAKDOWN.**

Step 3 – Worst-Case Electrical Parameters

Enter: FSWITCHING_MAX, VOR and LPRIMARY_TOL, or VMIN

34	WORST CASE ELECTRICAL PARAMETERS	INPUT	INFO	OUTPUT	UNITS	Design Title
35	FSWITCHING_MAX	86100		86100	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage.
36	VOR	120.0		120.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			89.19	V	Valley of the minimum input AC voltage at full load
38	KP			0.58		Measure of continuous / discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.577		Primary switch duty cycle
41	TIME_ON			12.31	µs	Primary switch on-time
42	TIME_OFF			4.91	µs	Primary switch off-time at 85 VAC, 36 W, and 86100 Hz.
43	LPRIMARY_MIN			921.5	µH	Minimum primary inductance
44	LPRIMARY_TYP			970.0	µH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			1018.5	µH	Maximum primary inductance
47						
48	PRIMARY CURRENT					
49	IPEAK_PRIMARY			1.218	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.457	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.443	A	Primary switch average current
52	IRIPPLE_PRIMARY			0.900	A	Primary switch ripple current
53	IRMS_PRIMARY			0.616	A	Primary switch RMS current
54						
55	SECONDARY CURRENT					
56	IPEAK_SECONDARY			12.177	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			4.573	A	Secondary winding current pedestal
58	IRMS_SECONDARY			5.269	A	Secondary winding RMS current

Figure 4. Worst-Case Electrical Parameters Section of TinySwitch-5 Design Spreadsheet with Gray Override Cells.

Switching Frequency, FSWITCHING_MAX (Hz)
This parameter is the switching frequency at full load and minimum input voltage. The maximum switching frequency for TinySwitch-5 devices 150 kHz. In normal operation, the switching frequency at full load should be below the data sheet maximum switching frequency.

The programmable switching frequency range is 30 kHz to 142 kHz. Pushing frequency higher to reduce transformer size is possible but the designer will need to consider the primary inductance, peak current, and parts tolerances to deliver the required energy at the minimum rectified AC input voltage. We recommend a maximum operating frequency of 142 kHz to ensure margin for part tolerances and ensure effective jitter function.

Reflected Output Voltage, VOR (V)
This parameter is the secondary winding voltage during the diode conduction-time reflected back to the primary through the turns ratio of the transformer. The default value is 120 V. VOR can be adjusted to achieve a design that does not violate design rules.

For design optimization purposes, the following factors should be considered,

- Higher VOR allows increased power delivery at VMIN, which minimizes the value of the input capacitor and maximizes power delivery.
- Higher VOR reduces the voltage stress on the output diode(s), which in some cases may allow a lower voltage rated device to be used, typically increasing efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases peak and RMS current on the secondary-side which may increase secondary-side copper, and diode losses thereby reducing efficiency.

It should be noted that there are exceptions to this guidance especially for very high output currents where the VOR should be reduced to obtain highest efficiency. Higher output voltages (above 15 V) should employ a higher VOR to maintain an acceptable peak inverse voltage (PIV) across the output diode.

Optimal selection of VOR depends on the specific application and is based on a compromise between the factors mentioned above.

Minimum Rectified Input Voltage, VMIN
Valley of the rectified minimum AC input voltage at full power is calculated based on input capacitance **(CAP_INPUT)**.

Mode of Operation, KP

KP is a measure of how discontinuous or continuous the mode of switching is. KP > 1 is described as discontinuous operation (DCM), while KP < 1 denotes continuous operation (CCM).

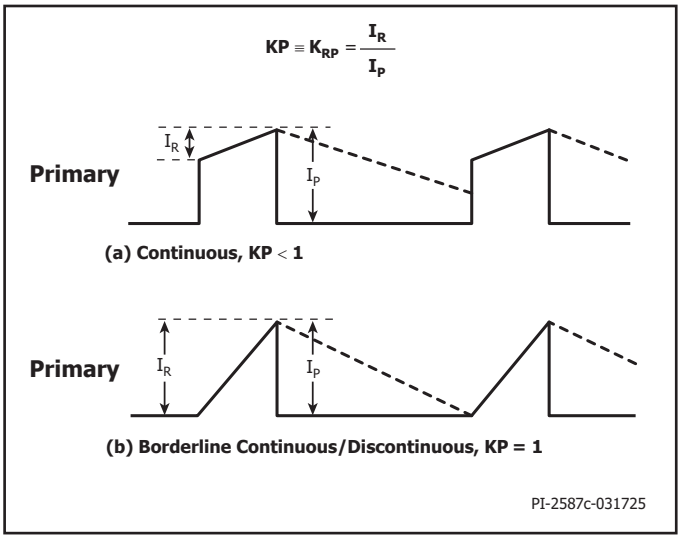


Figure 5. Continuous Mode Current Waveform, KP ≤ 1.

Ripple to Peak Current Ratio, KP

KP is the ratio of ripple current to peak primary current (Figure 5).

$$KP = K_{RP} = I_R / I_P$$

KP value > 1. In this case, KP is the ratio of primary switch off-time to secondary diode conduction time.

$$K \equiv K_{DP} = \frac{(1 - D) \times T}{t}$$

$$= \frac{VOR \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

The value of KP should be greater than 0.4. Guidance is given in the comments cell if the value of KP drops below 0.4.

Experience has shown that a KP value between 0.8 and 1.0 will result in the higher efficiency by ensuring DCM or critical mode operation (CRM) which is desirable for most designs.

The spreadsheet will calculate the values of peak primary current, primary RMS current, primary ripple current, primary average current, and maximum duty cycle for the design based on the design parameters chosen.

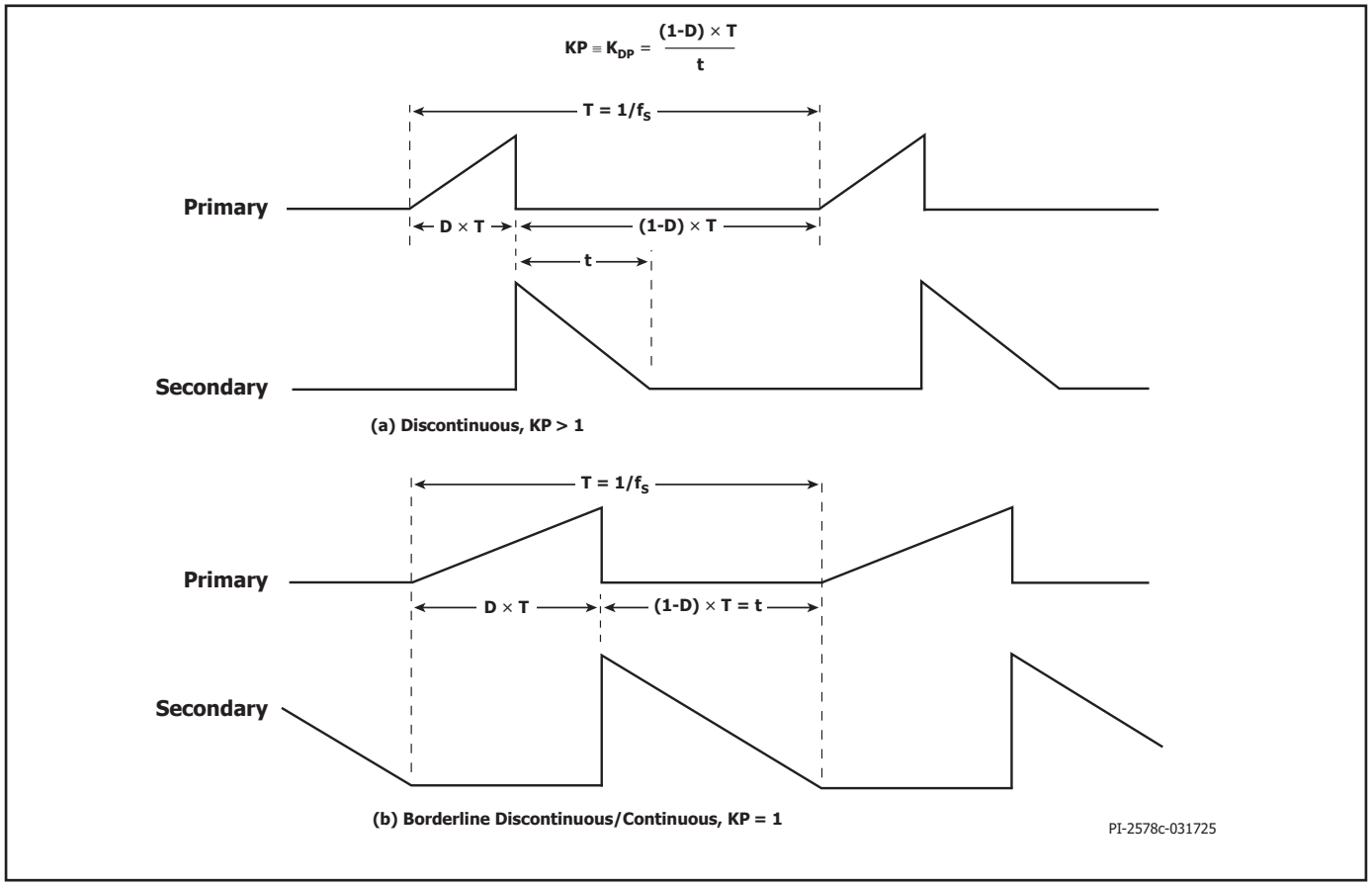


Figure 6. Discontinuous Mode Current Waveform, KP ≥ 1.

Typical Primary Inductance, LPRIMARY_TYP (µH)
This is the typical transformer primary inductance target value.

Primary Inductance Tolerance, LPRIMARY_TOL (%)
This parameter is the assumed primary inductance tolerance. A value of 10% is used by default, however if specific information is provided by the transformer vendor, then this value may be entered in the grey override cell. LPRIMARY_MIN and LPRIMARY_MAX will be calculated based on LPRIMARY_TOL.

Minimum Primary Inductance, LPRIMARY_MIN (µH)
Minimum possible primary inductance. LPRIMARY_MIN is calculated based on LPRIMARY_TOL.

Maximum Primary Inductance, LPRIMARY_MAX (µH)
Maximum possible primary inductance. LPRIMARY_MAX is calculated based on LPRIMARY_TOL.

PRIMARY CURRENT
IPEAK_PRIMARY – Peak primary current
IPEDESTAL_PRIMARY – Primary MOSFET current pedestal in CCM mode IAVG_PRIMARY – Primary MOSFET average current IRIPPLE_ PRIMARY – Primary MOSFET ripple current
IRMS_PRIMARY – Primary MOSFET RMS current

SECONDARY CURRENT
IPEAK_SECONDARY – Peak secondary current IPEDESTAL_ SECONDARY – Secondary winding current pedestal IRMS_ SECONDARY – Secondary winding RMS current

Step 4 – Transformer Construction Parameters

Enter: CORE, AE, LE, AL, VE, BOBBIN, AW, BW, MARGIN
Choose core and bobbin based on maximum output power.

61	TRANSFORMER CONTRUCTION PARAMETERS	INPUT	INFO	OUTPUT	UNITS	Design Title
62	CORE SELECTION					
63	CORE SELECTION					
64	CORE	EF25		EF25		Core code
65	CORE CODE			PC40EF25-Z		Core cross sectional area
66	AE			51.80	mm^2	Core magnetic path length
67	LE			57.80	mm	Ungapped core effective inductance
68	AL			2000	nH/turns^2	Core volume
69	VE			2990.0	mm^3	Bobbin
70	BOBBIN			EF25 - 1 (P5-S5)		Window area of the bobbin
71	AW			61.00	mm^2	Bobbin width
72	BW			15.60	mm	Primary inductance tolerance
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
74						
75	PRIMARY WINDING					
76	NPRIMARY			70		Primary turns
77	BPEAK			3796	Gauss	Peak flux density
78	BMAX			3380	Gauss	Maximum flux density
79	BAC			1224	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			198	nH/turns^2	Typical gapped core effective inductance
81	LG			0.296	mm	Core gap length
82						
83	PRIMARY BIAS WINDING					
84	NBIAS_PRIMARY			8	turns	Primary bias winding number of turns
85						
86	SECONDARY WINDING					
87	NSECONDARY			7	turns	Secondary winding number of turns
88						
89	SECONDARY BIAS WINDING					
90	NBIAS_SECONDARY			NA	turns	Secondary bias winding number of turns

Figure 7. Transformer Core and Construction Variables Section of the TinySwitch-5 family PIXLs Spreadsheet.

Core Type, CORE
The designer must select the core to use. Different core types and sizes from the drop-down list are available. If a user-preferred core is not available, the grey override cells (AE, LE, AL, VE, AW, Bobbin & BW) can be used to enter the core and bobbin parameters directly from the manufacturer's data sheet.

Output Power at 130 kHz Universal Inputs	Core	Code	AE	LE	AL	VE
			(mm2)	(mm)	(nH/T2)	(mm3)
0 W – 10 W	EE10	EE10	11.9	27	1000	321
0 W – 10 W	EE13	PC47EE13-Z	17.1	30.2	1130	517
0 W – 10 W	EE16	PC47EE16-Z	19.0	34.5	1140	656
10 W – 20 W	EE19	PC47EE19-Z	23.0	39.4	1250	906
10 W – 20 W	EE22	PC47EE22-Z	41.0	39.6	2180	1620
20 W – 30 W	EE25	PC47EE25/19-Z	40.0	48.7	2316	1950
20 W – 30 W	EI22	PC47EI22-Z	42	39.3	2400	1650
30 W – 45 W	EF25	PC47EF25-Z	51.8	57.8	2000	2990
30 W – 45 W	EPC30	PC47EPC30-Z	55.6	75.3	1570	4190
45 W – 60 W	EFD25	EFD25/13/9-3C94	58	57	2200	3300
45 W – 60 W	E30	E30/15/7-3C94	60	67	1900	4000
60 W – 75 W	EFD30	EFD30/15/9-3C94	69	68	2100	4700
60 W – 75 W	ETD29	PC47ETD29-Z	73.6	70.6	2500	5200
75 W – 90 W	EFD30	EFD30/15/9-3C94	69	68	2100	4700
75 W – 90 W	ETD29	PC47ETD29-Z	73.6	70.6	2500	5200
90 W – 105 W	EQ25	EQ25-3C94	100	41.4	4800	4145
90 W – 105 W	EQ30	EQ30-3C94	108	46	5400	4970
105 W – 120 W	EE30	PC47EE30-Z	109	57.7	4690	6290
105 W – 120 W	PQ26	PC47PQ26/25Z-12	118	55.5	5250	6530

Table 5. Commonly Available Cores and Power Levels at Which These Cores Can be used for Typical Designs.

Safety Margin, MARGIN (mm)
For designs that require safety isolation between primary and secondary, but that are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically for universal (85 – 265 VAC) input designs a total margin of 6.2 mm is required, and a value of 3.1 mm should be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical; however if a total margin of 6.2 mm is required then 3.1 mm would still be entered even if the physical margin is only present on one side of the bobbin. For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet required safety creepage distances. Typically several bobbins exist for each core size and each will offer different mechanical spacing. Refer to the bobbin data sheet and applicable standards to determine what specific margin is required.

Margin reduces the available area for the windings so marginated construction may not be suitable for small core sizes. If after entering the margin more than 3 primary layers are required, it is suggested that either a larger core be selected or that the design is switched to a zero margin approach using triple insulated wire.

Primary Layers, L
Primary layers should be in the range of 1 to 3, with the lowest number that meets the primary current density limit (CMA) being preferred. A value of ≥200 Circular-mils/Amp can be used as a starting point for most designs, though higher values may be required due to thermal constraints. Designs with more than three layers are possible, but increased leakage inductance and the physical fit of the windings should be considered.

A split primary construction may be beneficial for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. However, this arrangement can be disadvantageous for low power designs as it typically increases common mode noise and adds cost to the input filtering.

Primary Turns, NPRIMARY
This is the number of turns for the main winding of the transformer calculated based on VOR and Secondary Turns.

Peak Flux Density, BPEAK (Gauss)
A maximum value of 3800 gauss is recommended to limit the peak flux density at maximum current limit and 150 kHz operation. Under an output-short condition, the output voltage is low and little reset of the transformer occurs during the MOSFET off-time. This allows the transformer flux density to "staircase" beyond the normal operating level. A value of 3800 gauss at the maximum current limit of the selected device together with the built in protection features of TinySwitch-5 devices provides sufficient margin to prevent core saturation under output short-circuit conditions.

Maximum Flux Density, BMAX (Gauss)
Light load operation can generate audible noise from the transformer, especially if a long core is used. To limit audible noise, the transformer should be designed such that the maximum core flux density is below 3000 gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

AC Flux Density, BAC (Gauss)
The BAC value can be used for calculating core loss.

Gapped Core Effective Inductance, ALG: (nH/N^2)
Used to determine the CORE GAP [LG].

Primary Bias Winding Turns, NBIAS_PRIMARY
Calculated integer number determined based on the desired secondary number of turns NSECONDARY and the primary bias winding voltage VBIAS_PRIMARY.

Secondary Winding Turns, NSECONDARY
By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the peak operating flux density BPEAK is kept below the recommended maximum of 3800 gauss (380 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired.

Secondary Bias Winding Turns, NBIAS_PRIMARY
Calculated integer number based on the desired secondary number of turns NSECONDARY and the secondary bias winding voltage VBIAS_SECONDARY.

Step 5 – Primary Components Selection

Enter: BROWN-IN VOLTAGE, VBIAS, VF_BIAS

Required Line Undervoltage Brown-in, BROWN-IN REQUIRED
This is the input AC/DC voltage at which the power supply will turn on (once the brown-in threshold (I_{UV+}) is exceeded). The typical value is 20% below minimum AC input voltage (VIN_MIN). The brown-in voltage can be changed to a specific voltage [C96].

Line Undervoltage / Overvoltage Sense Resistor, RLS
The spreadsheet will calculate the resistance value based on the brown-in voltage. Shown as R_{LS1} + R_{LS2} on Figure 1, they are typically connected at the bulk capacitor. Typical total value for R_{LS1} and R_{LS2} is 4.02 MΩ. Resulting to a total resistance (RLS) of 8.04 MΩ RLS is approximately equal to $[(V_{BROWN-IN} \times 1.414) - 2.5] / I_{UV+}$ for AC input and $[V_{BROWN-IN} - 2.5] / I_{UV+}$ for DC input.

BROWN-IN ACTUAL
Calculated brown-in input AC or DC input voltage based on the calculated RLS resistance and I_{UV+}.

BROWN-OUT ACTUAL
Calculated brown-out input AC or DC input voltage based on the calculated RLS resistance and I_{UV-}.

Line Overvoltage, OVERVOLTAGE_LINE
This is the input AC or DC input voltage at which the power supply will immediately stop switching once the overvoltage threshold current (I_{OV+}) is exceeded. Switching will be when switching the line overvoltage recovery threshold (I_{OV-}) is reached. Line OV voltage is approximately equal to:

$[(I_{OV+} \times RLS) + 2.5] / 1.414$ for AC Input

$[(I_{OV+} \times RLS) + 2.5]$ for DC Input

Primary Bias Voltage, VBIAS_PRIMARY
This is the bias voltage when the main output is at full load. A default value of 12 V is assumed. The voltage may be set to different values (for example for applications when the bias winding output is also used as a non-isolated primary-side auxiliary output). Higher voltages typically increase no-load input power. Values below 10 V are not recommended since at light load there may be insufficient voltage to supply current to the BYPASS pin which will increase no-load input power.

Bias Diode Forward Drop, VF_BIAS_PRIMARY
A default value of 0.7 V is used though this can be changed to match the type of diode used for rectifying the bias winding (D_{BIAS}).

Reverse Voltage Primary Bias, VREVERSE_BIASDIODE_PRIMARY
Calculated reverse voltage across the primary bias diode. Parasitic voltage ring is not included.

Bias Supply Capacitor, CBIAS_PRIMARY
A 47 µF, 25 V low ESR electrolytic capacitor is recommended for the bias winding rectification filter capacitor, C_{BIAS}. This will also improve no-load and standby input power.

BP Pin Capacitor, CBP
Although, electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they can be placed very close to the IC. A ceramic capacitor X7R (or better), rated to ≥ 10 V, and 0805 size or larger is recommended.

99	PRIMARY COMPONENT SELECTION	INPUT	INFO	OUTPUT	UNITS	Design Title
100	Line undervoltage					
96	BROWN-IN REQURED	76.00		76.00	V	Required AC RMS/DC line voltage brown-in threshold
97	RLS			8.04	V	Connect two 4.02 MΩ resistors to the V pin for the required UV/OV threshold
98	BROWN-IN ACTUAL			62.2 V - 77.2 V		Actual AC RMS/DC brown-in range
99	BROWN-OUT ACTUAL			53.7 V - 66.6 V	W	Actual AC RMS/DC brown-out range
100					Ω	
101	LINE OVERVOLTAGE				A	
102	OVERVOLTAGE_LINE			284.1 V - 353.9 V	A	Actual AC RMS/DC line overvoltage range
103					A	
104	PRIMARY BIAS DIODE				V	
105	VBIAS_PRIMARY	12.0		12.0	V	Rectified primary bias voltage
106	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
107	VREVERSE_BIASDIODE_ PRIMARY			56.38		Bias diode reverse voltage (not accounting parasitic voltage ring)
108	CBIAS_PRIMARY			47		Bias winding rectification capacitor
109	CBP			0.47		BP pin capacitor

Figure 8. Primary Components Section of TinySwitch-5 PIXIs Spreadsheet.

Step 6 – Secondary Components

113	PRIMARY COMPONENTS	INPUT	INFO	OUTPUT	UNITS	Design Title
114	VREF_REG	2.50		2.50	V	Reference voltage of the feedback
115	RFB_UPPER			38.30	kΩ	Upper feedback resistor (connected to the first output voltage)
116	RFB_LOWER			10.00	kΩ	Lower feedback resistor
117						
118	SECONDARY BIAS DIODE					
119	USE_SECONDARY_BIAS	NO		NO		Use secondary bias winding for the design
120	VBIAS_SECONDARY			NA	V	Rectified secondary bias voltage
121	VF_BIAS_SECONDARY			NA	V	Bias winding diode forward drop
122	VREVERSE_BIASDIODE_ SECONDARY			NA	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
123	CBIAS_SECONDARY			NA	µF	Bias winding rectification capacitor

Figure 9. Secondary Component Section of TinySwitch-5 family PIXLs Spreadsheet.

Enter: VREF_REG and RFB_UPPER

Feedback Reference Voltage, VREF_REG
This is the reference voltage for the feedback circuit. VREF_REG issued to calculate the upper and lower feedback resistor values.

Upper Feedback Resistor, RFB_UPPER
The RFB_UPPER resistor is calculated based on VOUT and feedback reference voltage (VREF_REG). The value will change if a specified value is used for the RFB_LOWER resistor.

Lower Feedback Resistor, RFB_LOWER
The RFB_LOWER resistor value is a user define parameter. A default value of 10 kΩ will be used if left blank.

Enable Secondary Bias, USE_SECONDARY_BIAS
Secondary bias supply is needed when the output voltage is too high to bias the secondary feedback circuit directly. If a secondary bias supply is required, select "Yes" from the drop-down list. Default setting in this field is "No".

Secondary Bias Voltage, VBIAS_SECONDARY
This is the secondary bias voltage when the main output is at full load. A default value of 12 V is assumed. The voltage may be set to a different value.

Secondary Bias Diode Forward Drop, VF_BIAS_SECONDARY
A default value of 0.7 V is used though this can be changed to match the type of diode used for rectifying the secondary bias winding.

Reverse Voltage Secondary Bias, VREVERSE_BIASDIODE_ SECONDARY
Calculated reverse voltage across the secondary bias diode. Parasitic voltage ring is not considered.

Secondary Bias Supply Capacitor, CBIAS_SECONDARY
A 47 µF low ESR electrolytic capacitor is recommended for the bias winding rectification filter capacitor, CBIAS_SECONDARY.

126	MULTIPLE OUTPUT PARAMETERS	INPUT	INFO	OUTPUT	UNITS	Design Title
127	OUTPUT 1					Output 1 voltage
128	VOUT1			12.00	V	Output 1 current
129	IOUT1			3.00	A	Output 1 power
130	POUT1			36.00	W	Forward voltage drop of diode for output 1
131	VD1			0.70	V	Number of turns for output 1
132	NS1			7.00	turns	Instantaneous peak value of the secondary current for output 1
133	ISPEAK1			12.18	A	Root-mean-squared value of the secondary current for output 1
134	ISRMS1			5.269	A	Current ripple on the secondary waveform for output 1
135	ISRIPPLE1			4.331	A	Computed peak inverse voltage stress on the diode for output 1
136	PIV1_CALCULATED			59.04	V	Recommended diode for output 1.
137	OUTPUT_RECTIFIER1	AUTO		MBR1060		Peak inverse voltage rating on the diode for output 1
138	PIV1_RATING			60.00	V	Reverse recovery time of the diode for output 1
139	TRR1			0.00	ns	Maximum forward continuous current of the diode for output 1
140	IFM1			10.00	A	Maximum diode power loss for output 1
141	PLOSS_DIODE1			2.23	W	

Figure 10. Secondary Components Section of TinySwitch-5 Spreadsheet.

Step 7 – Multiple_Output Parameters

This section allows the user to design up to three secondary outputs (excluding bias supply) and choose suitable secondary rectifier diode. The spreadsheet will provide a warning should the total power of the multiple outputs exceed the power described in the **POUT** cell.

For single output design, cells **VOUT1**, **IOUT1** and **POUT1** will be the main output parameters entered in section 1.

Each output provides a selection of typical diode types for the secondary rectifier in drop-down menu. Based on the secondary rectifier diode chosen, diode forward voltage drop **VD1 (V)**, rated diode reverse voltage **PIV1_RATING (V)**, diode reverse recovery time **TRR1 (ns)**, and diode maximum forward continuous current **IFM1 (A)** will be displayed in the spreadsheet.

The spreadsheet also calculates the critical electrical parameters for each secondary output:

Number of Turns for Output1, NS1
Calculated turns for each output.

Instantaneous Secondary Peak Current, IPEAK1 (A)
Used to select the secondary rectifier diode.

RMS Current of the Secondary Output, ISRM1 (A)
Used to set the diameter of the secondary winding wire.

Current Ripple on Secondary, IRIPPLE1 (A)
Used to select the output filter capacitor.

Calculated Diode Reverse Voltage , PIV1 (V)
Calculated diode reverse voltage stress for selection of the secondary rectifier diode.

Calculated Secondary Rectifier Diode Power Loss, PLOSS_DIODE1 (W)
Calculated secondary rectifier diode power loss for device selection and temperature management.

143	OUTPUT 2	INPUT	INFO	OUTPUT	UNITS	Design Title
144	VOUT2			0.00	V	Output 2 voltage
145	IOUT2			0.000	A	Output 2 current
146	POUT2			0.00	W	Output 2 power
147	VD2			N/A	V	Forward voltage drop of diode for output 2
148	NS2			N/A	turns	Number of turns for output 2
149	ISPEAK2			N/A	A	Instantaneous peak value of the secondary current for output 1
150	ISRMS2			N/A	A	Root mean squared value of the secondary current for output 2
151	ISRIPPLE2			N/A	A	Current ripple on the secondary waveform for output 2
152	PIV2			N/A	ς	Computed peak inverse voltage stress on the diode for output 2
153	OUTPUT_RECTIFIER2	AUTO		N/A		Recommended diode for output 2.
154	PIV2_RATING			N/A	V	Peak inverse voltage rating on the diode for output 2
155	TRR2			N/A	ns	Reverse recovery time of the diode for output 2
156	IFM2			N/A	A	Maximum forward continuous current of the diode for output 2
157	PLOSS_DIODE2			N/A	W	Maximum diode power loss for output 2
158						
159	OUTPUT 3					
160	VOUT3			0.00	V	Output 3 voltage
161	IOUT3			0.000	A	Output 3 current
162	POUT3			0.00	W	Output 3 power
163	VD3			N/A	V	Forward voltage drop of diode for output 3
164	NS3			N/A	turns	Number of turns for output 3
165	ISPEAK3			N/A	A	Instantaneous peak value of the secondary current for output 1
166	ISRMS3			N/A	A	Root mean squared value of the secondary current for output 3
167	ISRIPPLE3			N/A	A	Current ripple on the secondary waveform for output 3
168	PIV3			N/A	V	Computed peak inverse voltage stress on the diode for output 3
169	OUTPUT_RECTIFIER3	AUTO		N/A		Recommended diode for output 3.
170	PIV3_RATING			N/A	V	Peak inverse voltage rating on the diode for output 3
171	TRR3			N/A	ns	Reverse recovery time of the diode for output 3
172	IFM3			N/A	A	Maximum forward continuous current of the diode for output 3
173	PLOSS_DIODE3			N/A	W	Maximum diode power loss for output 2
174						
175	PO_TOTAL			36.00	W	Total power of all outputs
176	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Figure 11. Multiple Output Parameters Section of TinySwitch-5 PIXIs Spreadsheet.

Step 8 – Critical External Component Selection

The schematic in Figure 12 shows the key external components required for a practical single output TinySwitch-5 IC based design. Component selection criteria is as follows:

Bypass Pin Capacitor (C_{BP})
A capacitor connected from the BYPASS pin (BP) of the TinySwitch-5 IC to SG provides decoupling for the primary controller and selects the current limit. A 0.47 µF or 4.7 µF capacitor may be used. While electrolytic capacitors are an option, surface mount multi-layer ceramic capacitors are often preferred for double-sided boards as they can be placed close to the IC. Their small size also makes them ideal for compact power supplies. X5R or X7R dielectric capacitors are recommended to ensure minimum capacitance requirements are met. Note that ceramic capacitor type designations, such as X7R and X5R, can vary in voltage coefficients between manufacturers and product families. It is advisable to review the capacitor data sheets to ensure the selected capacitor does not experience more than a 20% drop in capacitance at 5 V. Avoid using Y5U or Z5U / 0603 rated MLCCs, as they have poor voltage and temperature coefficients.

Line Sense Resistors (R_{LS1} and R_{LS2})
Resistors connected from the V pin to the DC bus enable input voltage sensing for line undervoltage and overvoltage protection. For a typical universal input application, a total resistor value of 8.04 MΩ is recommended. For high-line input, it is advisable to use two 0.25-Watt SMD 1206 resistors or leaded resistors in series, each with a value of 4.02 MΩ.

Connecting the V pin to SOURCE disables the line sensing function. It is not recommended to leave the V pin floating.

General Formula:

$I_{UV+} = (V_{IN} + V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$
$I_{UV-} = (V_{IN} + V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$
$I_{OV+} = (V_{IN} + V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$
$I_{OV-} = (V_{IN} + V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$

Where:

I_{UV+}: V Pin Brown-In Threshold
I_{UV-}: V Pin Brown-Out Threshold
I_{OV+}: V Pin Line Overvoltage Threshold
I_{OV-}: V Pin Line Overvoltage Recovery Threshold
$V_{PIN\_Voltage}$: V pin voltage = 2.5 V
$R_{LS1} + R_{LS2}$: Line sense resistors
V_{IN}: For DC input, V_{IN} = VDC_INPUT
For AC input, V_{IN} = VAC x 1.414

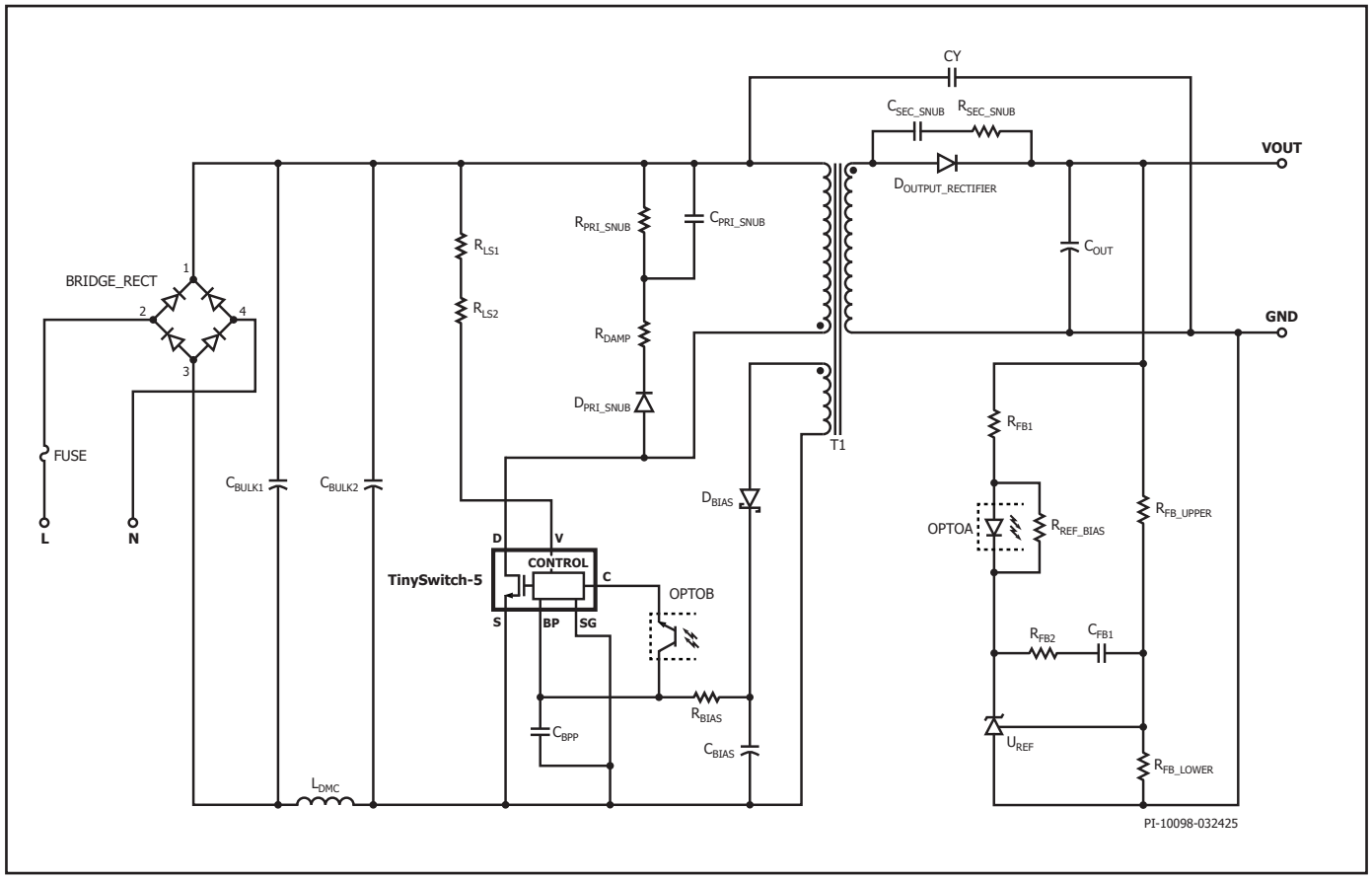


Figure 12. Typical TinySwitch-5 Flyback Power Supply.

Primary Clamp Network Across Primary Winding

(D_{PRI_SNUB}, R_{DAMP}, R_{PRI_SNUB}, C_{PRI_SNUB})

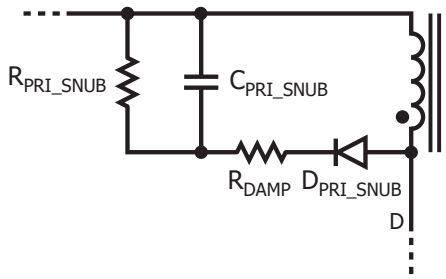
An R2CD clamp is the most commonly used clamp in low power flyback power supplies. For higher power designs, a Zener clamp or the R2CD + Zener clamp can be used to increase efficiency. It is advisable to limit the peak drain voltage to 90% of BVDSS (depending on derating requirements) under worst-case conditions (maximum input voltage, maximum overload power or output short- circuit). In Figure 12, the clamp diode, D_{PRI_SNUB} must be a standard recovery glass-passivated type, or a fast recovery diode with a reverse recovery time of less than 500 ns. The use of a standard recovery] glass passivated diode allows recovery of some of the clamp energy in each switching cycle and helps improve average efficiency. The diode conducts momentarily each time the MOSFET inside the TinySwitch-5 IC turns off and energy from the leakage reactance is transferred to the clamp capacitor C_{PRI_SNUB}. Resistor R_{DAMP}, which is in the series path, offers damping-preventing excessive ringing due to resonance between the leakage inductance and the MOSFET switch and output capacitance C_{OSS}. Resistor R_{PRI_SNUB} bleeds-off energy stored in capacitor C_{PRI_SNUB}. Power supplies using different TinySwitch-5 ICs and each will have its own peak primary current and leakage inductance and therefore leakage energy. Capacitor C_{PRI_SNUB} and resistor R_{PRI_SNUB} and R_{DAMP} must be optimized for each design. As general rule it is advisable to minimize the value of capacitor C_{PRI_SNUB} and maximize the value for R_{PRI_SNUB} and R_{DAMP}, while still meeting the 90% BVDSS limit under worst case conditions. The value of R_{DAMP} should be large enough to reduce the ringing in the required time but not so large as to cause the drain voltage to exceed 90% (or other specified limit) of BV_{DSS}. A ceramic capacitor that uses a dieletric such as Z5U if used in clamp circuit for C_{PRI_SNUB} may generate audible noise, so polyester film type or a ceramic capacitors with X7R as a dielectric, 1 kV rating, 1206 size are recommended.

Key Design Points Primary Clamp Circuit Optimization

- Assuming that Leakage inductance (L_{LK}) is less than 3% of primary inductance (L_p) is a good starting point for the calculation of primary clamp parameters. The Recommended next step is to measure the actual value of leakage inductance in a prototype transformer and modify the clamp and or magnetics design if appropriate.
- Resistor R_{DAMP} must be large enough to prevent excessive ringing caused by the leakage inductance and the MOSFET switch output capacitance (COSS).
- Reduce the value of the snubber resistor R_{DAMP} to reduce power losses while monitoring the following:
  1. EMI performance
  2. Voltage margin on the power MOSFET in the TinySwitch IC
- Minimize leakage inductance by completely filling each winding layer.
- Further reduce clamp losses by optimizing the reflected voltage (VOR).
- Minimizing inter-winding capacitance - add layers of tape between each primary winding if appropriate.
- Optimizing layout and transformer construction to ensure a tightly coupled loop between the primary snubber and the primary winding.

Common Primary Clamp Configurations

R2CD



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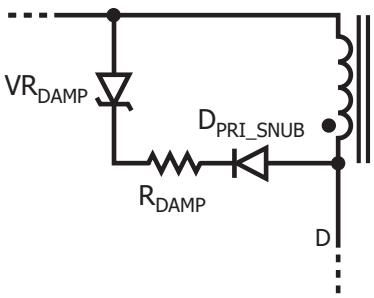
Zener



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R2CD + Zener

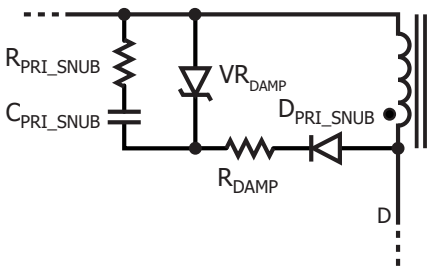

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Figure 13. Recommended Primary Clamp Configurations.

Primay Clamp Circuit			
Benefits	**R2CD**	**Zener**	**R2CD + Zener**
Component Cost	Low	Medium	High
No-Load Input Power	High	Low	Medium
Light-Load Efficiency	Low	High	Medium
EMI Suppression	High	Low	Medium

Table 6. Respective Benefits of Different Primary Clamp Circuits.

Bias Winding and External Bias Supply Circuit

(D_{BIAS}, C_{BIAS}, R_{BIAS})

To achieve start-up, the internal primary bypass regulator connected from the DRAIN pin of the switch to the BYPASS pin of the TinySwitch-5 IC charges the capacitor C_{BP}. A bias supply comprising a bias winding on the transformer feeding a suitable rectifier, limit resistor and filter capacitor should be provided (shown in Figure 12 as D_{BIAS}, R_{BIAS}, C_{BIAS} respectively). This must be able to supply ≥ 1.5 mA to the BYPASS and C pins.

A bias voltage of 12 V is the recommended bias voltage at full load. A higher bias voltage will increase no-load input power. To reduce no-load consumption and improve standby efficiency, and ultrafast or Schottky diode is recommended for D_{BIAS}. The turns ratio for the bias winding should be selected such that 10 V is developed across the bias winding at the lowest rated output voltage under the lowest load condition. If the voltage is lower than this, no-load input power will increase.

The bias current from the external circuit should be set to > I_{S1} of 258 µA to achieve the lowest no-load power consumption when operating the power supply at 230 VAC input. This can be achieved by adjusting the value of R_{BIAS} resistor. To reduce the amplitude of high frequency radiated EMI, we recommend the use of a glass passivated standard recovery rectifier diode with low junction capacitance to avoid the snappy recovery typically seen with fast or ultrafast diodes.

For the bias capacitor C_{BIAS}, a 47 µF aluminum electrolytic capacitor with low ESR and a 25 V rating will help reduce no-load input power and increase standby efficiency. The use of ceramic surface mount capacitors in this position is not recommended, as they can cause audible noise due to a piezoelectric effect on their mechanical structure.

To achieve minimum no-load input power and high full load power efficiency, the resistor R_{BIAS} should be selected such that the current through this resistor is higher than the required BYPASS pin current.

The BYPASS pin supply current at normal operating frequency can be calculated as shown below:

$$I_{SSW} = \frac{F_{SW}}{150\,kHz} \times (I_{S2} - I_{S1}) + I_{S1}$$

Where,

I_{SSW}: BYPASS pin supply current at operating switching frequency

F_{SW}: Operating switching frequency (kHz)

I_{S1}: BYPASS pin supply current at no switching (refer to data sheet)

I_{S2}: BYPASS pin supply current at 132 kHz (refer to data sheet)

The BP voltage is internally clamped to 5.3 V when bias current is higher than BYPASS pin supply current. If BP voltage is ~ 5.0 V, then this indicates that the current through R_{BIAS} is less than the BYPASS pin supply current and charge is being drawn from the DRAIN pin to keep the BYPASS pin above 5.0 V except during start-up.

To determine maximum value of R_{BIAS}:

$$R_{BIAS} = [V_{BIAS(NO-LOAD)} - V_{BP}]/I_{SSW};$$
$$V_{BP} = 5.3\ V$$

Secondary Rectifier Diode ($D_{OUTPUT\_RECTIFIER}$)

The output diode is selected based on peak inverse voltage, output current, and thermal conditions in the application. The high (725 V) primary switch voltage rating in TinySwitch-5 devices combined with an appropriate transformer turns ratio, allows the use of an 80 V Schottky diode for high efficiency at output voltages up to 15 V. Considerations for selecting an output rectifier diode:

3. Ensure the reverse voltage rating for the diode (V_R) is at least 1.25 times the peak inverse voltage (PIV).
4. Select a diode with a current rating (I_D) that is at least twice the output current (I_{OUT}).

Output Filter Capacitance (C_{OUT})

A low ESR electrolytic capacitor is a key parameter in limiting the output voltage ripple. Other parameters to be considered capacitor selection are the RMS ripple current rating and DC working voltage. The actual capacitance value is of secondary importance.

Considerations for Selection of Output Capacitor:

1. Ensure that the capacitor ripple rating specified at 105 ºC, 100 kHz is larger than the expected ripple current (ISRIPPLE).
2. Use a low ESR (Equivalent Series Resistance) electrolytic capacitor to minimize output ripple voltage.
3. Capacitor VRIPPLE = ISRIPPLE x EER rating ≥ 1.25 times the output voltage (VOUT).

Output Post Filter Components (L_{PF} and C_{PF}):

A post filter (L_{PF} and C_{PF}) can be added to reduce high frequency switching noise and ripple.

Considerations for adding a post filter:

1. The inductor (L_{PF}) should have an inductance value in the range of 1 µH to 3.3 µH and a current rating that exceeds the peak output current.
2. The capacitor (C_{PF}) should have a capacitance value in the range of 100 µF to 330 µF and a voltage rating that is at least 1.25 times the output voltage (VOUT).
3. If a post filter is used, ensure that the output voltage sense resistor and optocoupler are connected before the post filter inductor. See Figure 14.

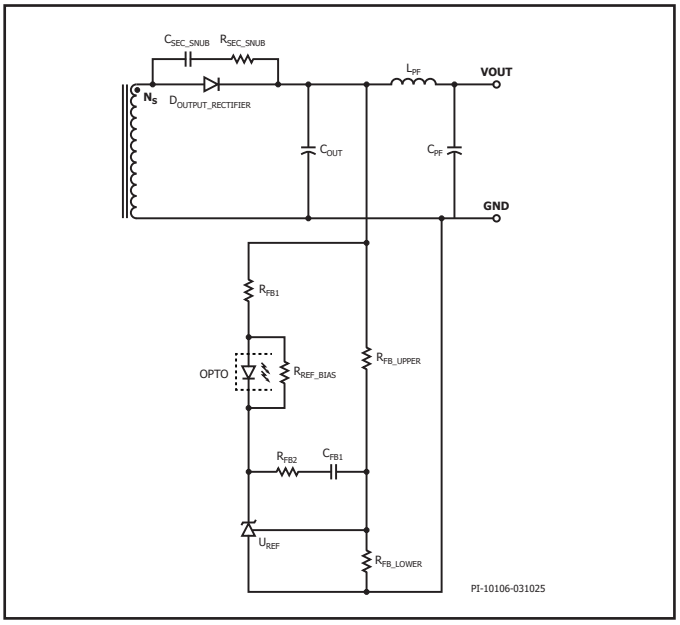

Figure 14. Secondary Output with Post Filter (L_{PF} and C_{PF}).

FEEDBACK Pin Divider Network (R_{FB_UPPER}, R_{FB_LOWER})
A suitable resistive voltage divider should be connected from the output of the power supply to the feedback circuit. The voltage across R_{FB_LOWER} will be made equal to the reference voltage of the feedback circuit.

Feedback Circuit
The reference IC (UREF) - typically a TL431 is used to set the output voltage programmed via the resistor divider R_{FB_UPPER} and R_{FB_LOWER}. Resistor R_{REF_BIAS} provides the minimum cathode current for regulation which is nominally 1 mA for a TL431CDBZR. Each reference IC type will have a different minimum cathode current for regulation, so it is recommended that the designer confirm minimum current requirements from the appropriate manufacturers data sheet. An improvement to no load input power and light load efficiency will be seen if an IC with low minimum cathode current is used. R_{FB1}, sets the DC gain and limits the feedback current during output load transients. Capacitor R_{FB2} and C_{FB1} adjusts the role off of the high frequency gain of U_{REF} so that it ignores output ripple voltage. AC feedback is provided directly through the optocoupler. Use of and optocoupler with high CTR is recommended for improved no load input and standby efficiency.

Key Applications Design Considerations

Output Power Table

The output power table (Table 2) represents the maximum practical continuous output power that can be obtained under the following conditions:

1. Minimum DC input voltage is 100 V or higher for 85 VAC input, and 300 V or higher for 230 VAC input.
2. Efficiency assumptions depend on input voltage range. Universal input voltage or low-line input assumes efficiency >85% increasing to >89% for a high-line input. The assumed efficiency is based on the lowest voltage of the input range.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (VOR) is set to maintain KP > 0.4 at a minimum input voltage to provide the maximum power. At high-line nominal, it recommended to design KP between 1 and 1.1 to increase efficiency.
5. Low forward voltage drop (V_F) Schottky O/P diode
6. The part is board-mounted with SOURCE pins soldered to a sufficient area of copper and/or a heatsink to maintain the device temperature at or below 110 °C at the required highest ambient temperature.
7. An ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.
8. A unique feature of TinySwitch-5 is that a designer can set the full-load switching frequency, between 25 kHz to 142 kHz depending on the transformer design. An effective way to lower device temperature is to design the transformer to operate at a low switching frequency, with a good starting point being 66 kHz. If a smaller size transformer is needed, the operating switching frequency can be increased up to 130 kHz.

Primary-Side Overvoltage Protection
The output overvoltage protection provided by TinySwitch-5 uses an internal latch triggered by a threshold current (I_{SD}) of approximately 8.7 mA into the BYPASS pin. In addition to an internal filter, the BYPASS pin capacitor adds an external filter to help prevent false triggering. To ensure the bypass capacitor is effective as a highfrequency filter, it should be placed as close as possible to the SG and BYPASS pins of the device.

A primary sensed OVP function can be realized by connecting a series combination of a Zener diode (V_{ZOVP}), a resistor (R_{OVP}), and a blocking diode (D_{OVP}) from the rectified and filtered bias winding voltage supply to the BYPASS pin (as shown if Figure 15). The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding which results in a ring on the bias winding voltage waveform. It is therefore recommended to measure the rectified bias winding voltage, ideally at the lowest input voltage and with the highest load on the output. This measured voltage should be used to select the components required to achieve the appropriate trigger point.

A Zener diode should be selected with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered. A forward voltage drop of 1 V can be assumed for the blocking diode (D_{OVP}). A small signal standard recovery diode is recommended for this role. The blocking diode prevents reverse current from discharging the bias capacitor during start-up. Finally, the value of the series resistor should be calculated to ensure that a current higher than I_{SD} flows into the PRIMARY BYPASS pin during an output overvoltage event.

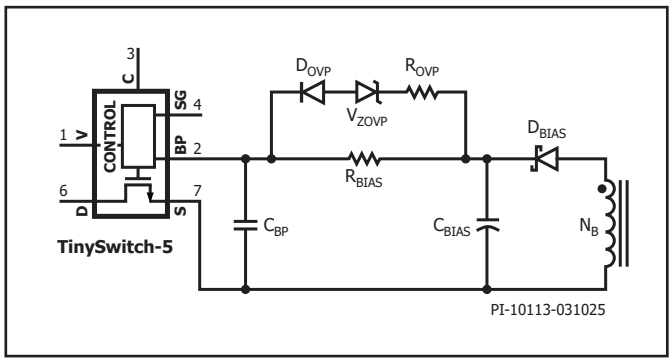

Figure 15. Primary-Side Secondary OVP Which Directs Current into the BP pin via V_{ZOVP}.

Reducing No-load Consumption.
The TinySwitch-5 IC starts in self-powered mode, drawing energy from the BYPASS pin capacitor, which is charged from the internal current source in the TinySwitch-5 IC (connected to the drain tab). Once the TinySwitch-5 IC begins switching, a bias winding is required to provide supply current to the BYPASS pin. This bias winding supply ensures low no-load power consumption. The value of resistor R_{BIAS} should be adjusted to achieve the lowest no-load input power.

Additional techniques to further reduce no-load consumption include:

1. Using a low capacitance primary clamp capacitor (C_{PRI_SNUB}).
2. Employing a Schottky or ultrafast diode for the bias supply rectifier (D_{BIAS}).
3. Use of a high Current Transfer Ratio optocoupler with a CTR of 300-600% (OPTO).
4. Selecting a low ESR capacitor for the bias supply filter capacitor (C_{BIAS}).
5. Selecting a low ESR for input bulk capacitor ($C_{\_BULK}$) and output filter capacitor ($C_{\_OUT}$).
6. Use of a low value RC snubber capacitor (C_{SEC_SNUB}) for the secondary rectifier.
7. Apply tape between primary winding layers and multi-layer tapes between primary and secondary windings to reduce inter-winding capacitance.

Recommendations for Circuit Board Layout

For this section refer to Figures 16 to 20.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. The C_{BIAS} ground should have a dedicated trace that is star-connected to the input filter capacitor ground pin.

Bypass Capacitors and Ferrite Bead
The BYPASS pin decoupling capacitor (C_{BP}) and ferrite bead (L_{FB}) must be located directly adjacent to the BYPASS and SOURCE pins. Ensure that the connections are routed via short traces.

Critical Loop Area
Circuits with high dv/dt or di/dt should be kept as small as possible. Minimize the area of the primary loop that connects the input filter capacitor, transformer primary, and IC. Similarly, reduce the area of the loop connecting the secondary winding, output rectifier diode, and output filter capacitor. (Figure 16 and 17 loops 1 to 4)

To minimize crosstalk between circuits ensure that no loop area is placed inside another loop.

Drain Node
The drain switching node is the dominant noise generator. Therefore, components connected to the drain node should be placed close to the IC and away from sensitive primary control circuits. The clamp circuit components should be located away from the BYPASS pin. Trace widths and lengths in this circuit should be minimized.

Power Trace Routing
Current will flow through the path of least resistance. Even if the trace is connected to the capacitors, there is a possibility that the current may bypass them, rendering the capacitors ineffective. For best filtering and noise immunity, it is recommended that power signal traces be star-connected the bulk capacitor connection pads.

Primary Clamp Circuit
A clamp is used to limit the peak voltage on the DRAIN pin during turn-off. This can be achieved by using an R2CD or R2CDZ clamp across the primary winding. To reduce EMI, minimize the loop area between the clamp components, the transformer, and the IC.

Y Capacitor
The Y capacitor should be placed directly from the positive terminal of the primary input filter capacitor to the output positive or return terminal of the transformer secondary. This placement will route high-magnitude common mode surge currents away from the IC. If an input pi EMI filter (C_{BULK1}, L_{DMC}, C_{BULK2}) is used, the inductor should be placed between the negative terminals of the input filter capacitors.

ESD Immunity
Sufficient clearance should be maintained between the primary-side and secondary-side circuits to ensure compliance with ESD and hi-pot isolation requirements. A spark gap should be placed between the output return and/or positive terminals and one of the AC inputs (after the fuse). In this configuration, a 6.4 mm spark gap (5.5 mm maybe acceptable, depending on customer requirements) is sufficient to meet the creepage and clearance requirements of most safety standards applicable to a universal input power supply. For effective ESD immunity, the spark gap spacing should provide the shortest distance between the primary and secondary sections.

A spark gap across the common-mode choke provides a low impedance path for high-energy discharges due to ESD or common-mode surges.

Secondary Rectifier Diode
For optimal performance, the loop area connecting the secondary winding, secondary rectifier diode, and output filter capacitor should be minimized. When using SM diodes, ensure sufficient copper area at the terminals of the secondary rectifier diode for heat dissipation. A heatsink will be required for a non-SM secondary diode.

Thermal Protection
The SOURCE pin is internally connected to the IC lead frame and serves as the main path for heat removal in V and K packages. The SOURCE pin should be connected to a copper area underneath the IC, functioning as both a single-point ground and a heat sink. Since this area is connected to the quiet source node, it can be maximized for effective heat dissipation without causing EMI issues. K packages feature an exposed pad on the bottom of the IC, which should be soldered to the SOURCE connected copper heatsink to further reduce temperature.

For E packages, the exposed Source pad on the back of the IC is necessary to ensure that the IC operates safely below the absolute maximum junction temperature limit when connected to an appropriate heatsink.

Sufficient copper area or a heatsink should be provided to maintain the IC temperature below absolute maximum limits. It is recommended that the cooling method be sufficient to keep the IC temperature below 110 °C when operating the power supply at the condition of full rated load, the lowest rated input supply voltage, and maximum ambient temperature.

TinySwitch-5 is typically the only component that will have over-temperature protection. Designing cooling such that other components in the circuit will have lower temperatures than the TinySwitch IC will ensure that it protects the whole circuit from thermal damage in the event that excess ambient temperatures are encountered. This will ensure that the TinySwitch-5 part will protect the other devices when ambient temperature increases.

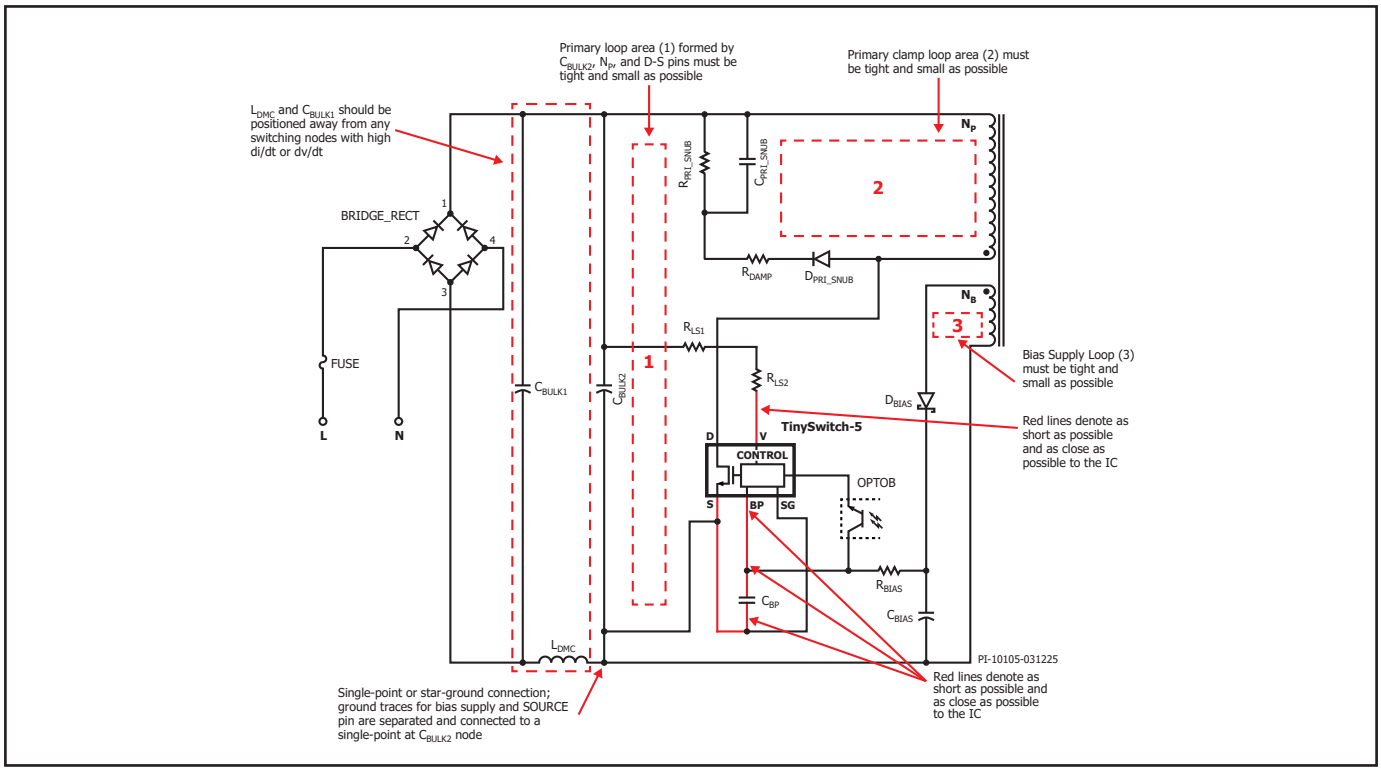

Figure 16. Typical Schematic of TinySwitch-5 Primary-Side Showing Critical Loops Areas, Critical Component Traces, and Single-Point or Star Grounding.

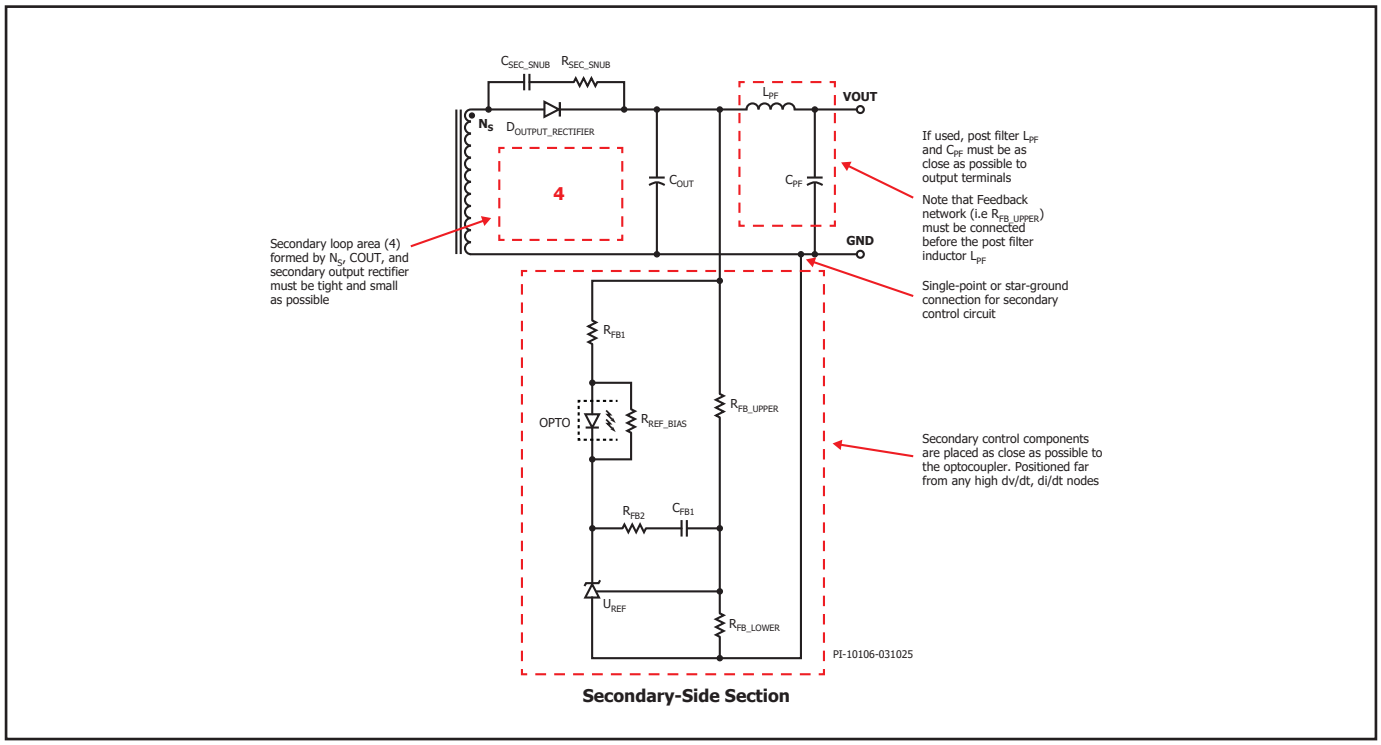

Figure 17. Typical Schematic of TinySwitch-5 Secondary-Side Showing Critical Loops Areas, Critical Component Traces and Single-Point or Star Grounding. Optional LC Post Filter Included.

Layout Example

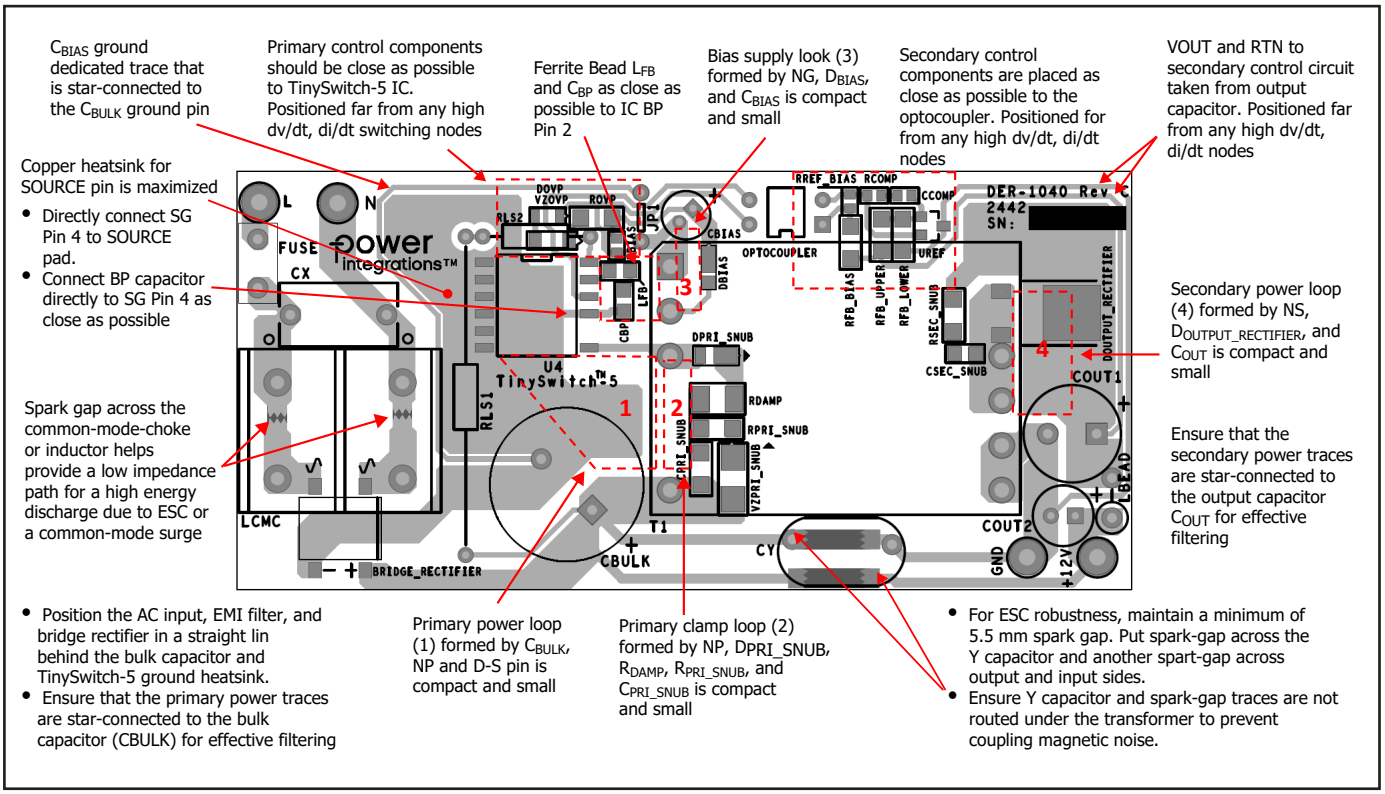

Figure 18. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TinySwitch-5 K-package.

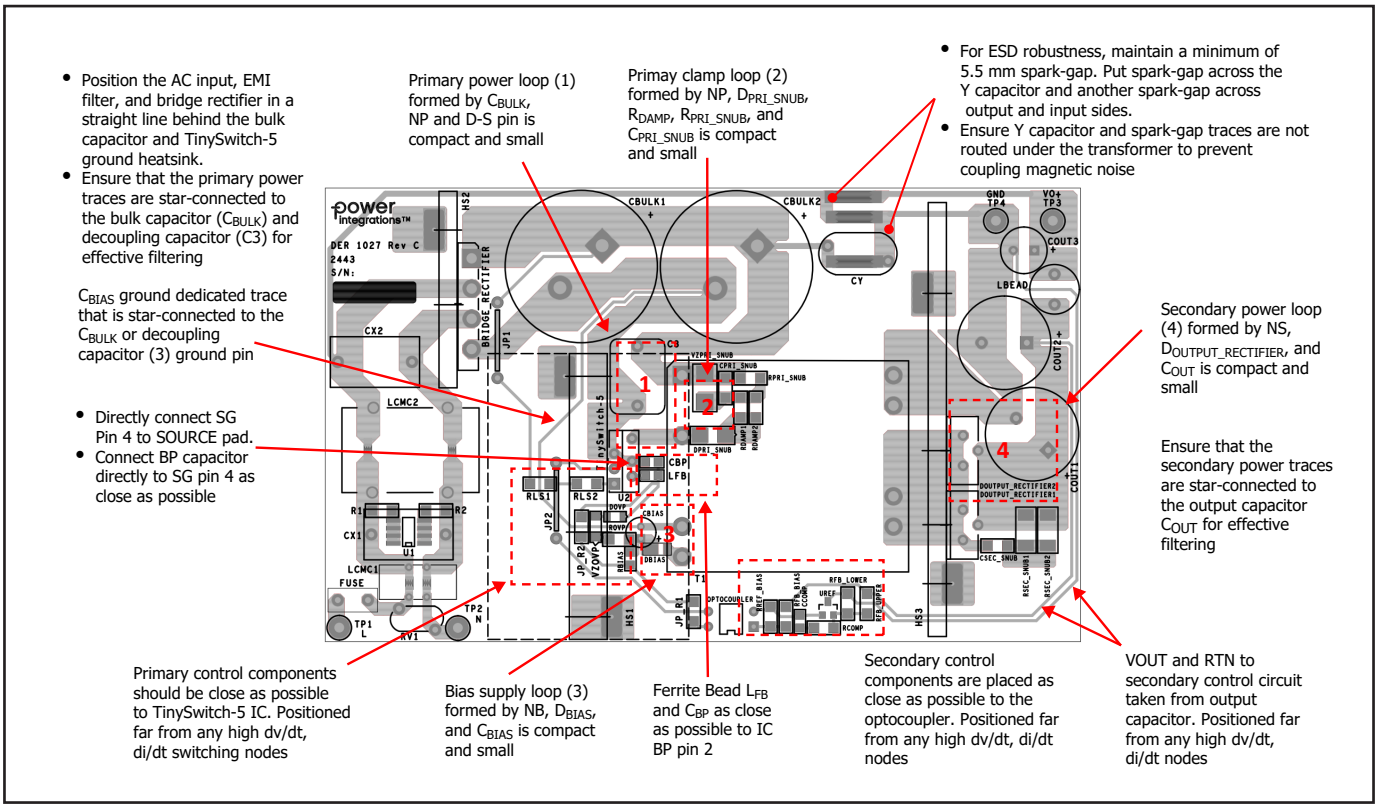

Figure 19. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TinySwitch-5 E-package.

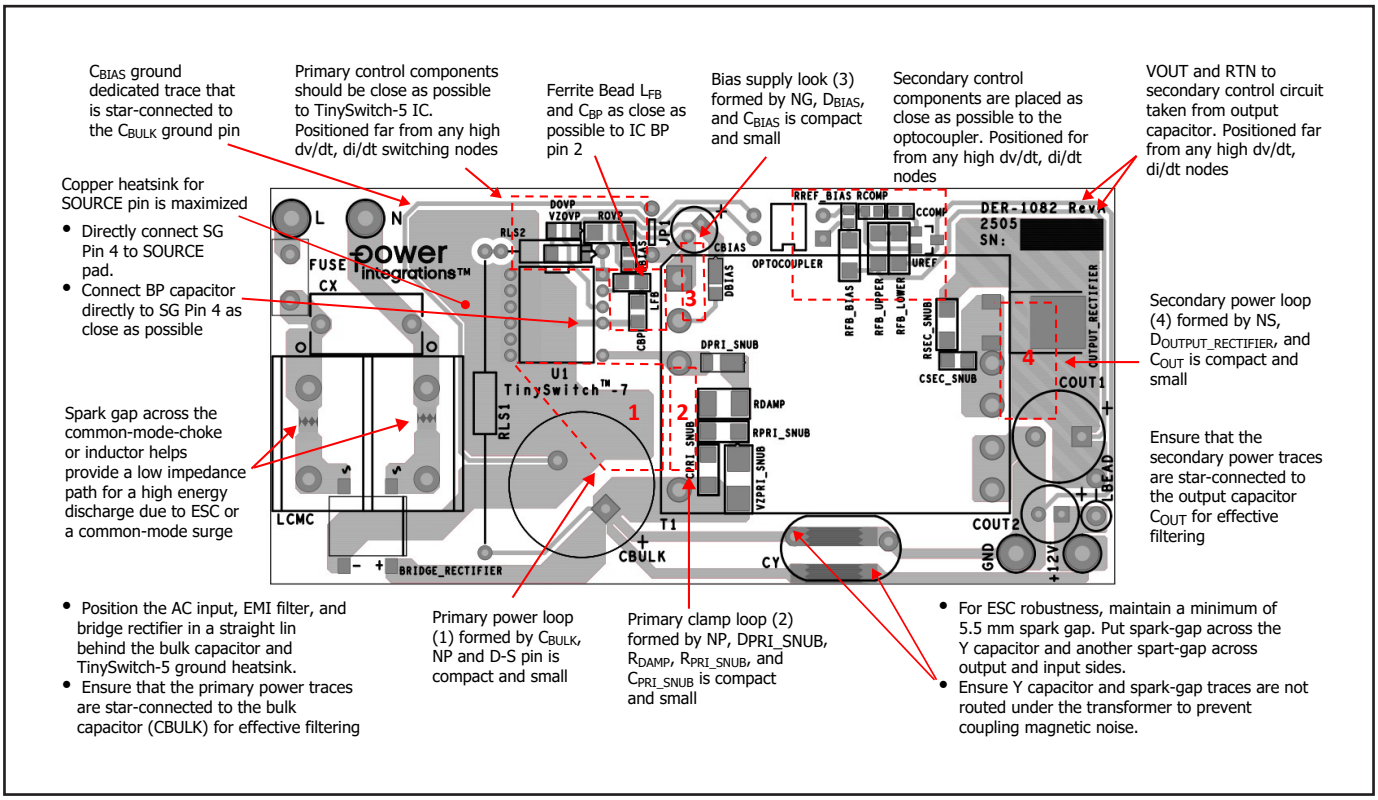

Figure 20. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TinySwitch-5 V-Package.

Recommendation for EMI Reduction

1. Ensure appropriate component placement and minimize loop areas for the primary and secondary power circuits to reduce radiated and conducted EMI. Aim for a compact loop area.
2. Adding a small capacitor in parallel with the clamp diode on the primary side can help reduce radiated EMI.
3. A resistor in series with the bias winding can help reduce radiated EMI.
4. Common mode chokes (CMC) are typically required at the power supply input to attenuate common mode noise. Alternatively, shield windings on the transformer can achieve similar performance. Shield windings can also be used with common mode filter inductors at the input to improve conducted and radiated EMI margins.
5. Adjusting RC snubber component values for the secondary rectifier diode can help reduce high frequency radiated and conducted EMI.
6. Use a pi-filter comprising differential inductors and capacitors in the input rectifier circuit to reduce low-frequency differential EMI.
7. Connecting a 1 μF ceramic capacitor at the power supply output helps reduce radiated EMI.

Quick Design Checklist

As with any power supply, the operation of all TinySwitch-5 part based designs should be verified on-the-bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

Maximum Drain Voltage
Verify that V_{DS} of TinySwitch-5 IC and reverse voltage of the secondary rectifier diode does not exceed 90% of their respective breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.

Maximum Drain Current
At maximum ambient temperature, maximum input voltage and peak output (overload) power, review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading-edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB\ (MIN)}$. Under all conditions, the maximum drain current for the primary MOSFET should be below the specified absolute maximum rating.

Thermal Check
At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for the TinySwitch-5 IC, transformer, bridge rectifier, secondary rectifier diode, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation. At low-line, maximum power, a maximum TinySwitch-5 IC temperature of 110 °C is recommended to allow for $R_{DS(ON)}$ variation.

Design Support

Up-to-date information on design support can be found at the Power Integrations website: www.power.com

Application Examples

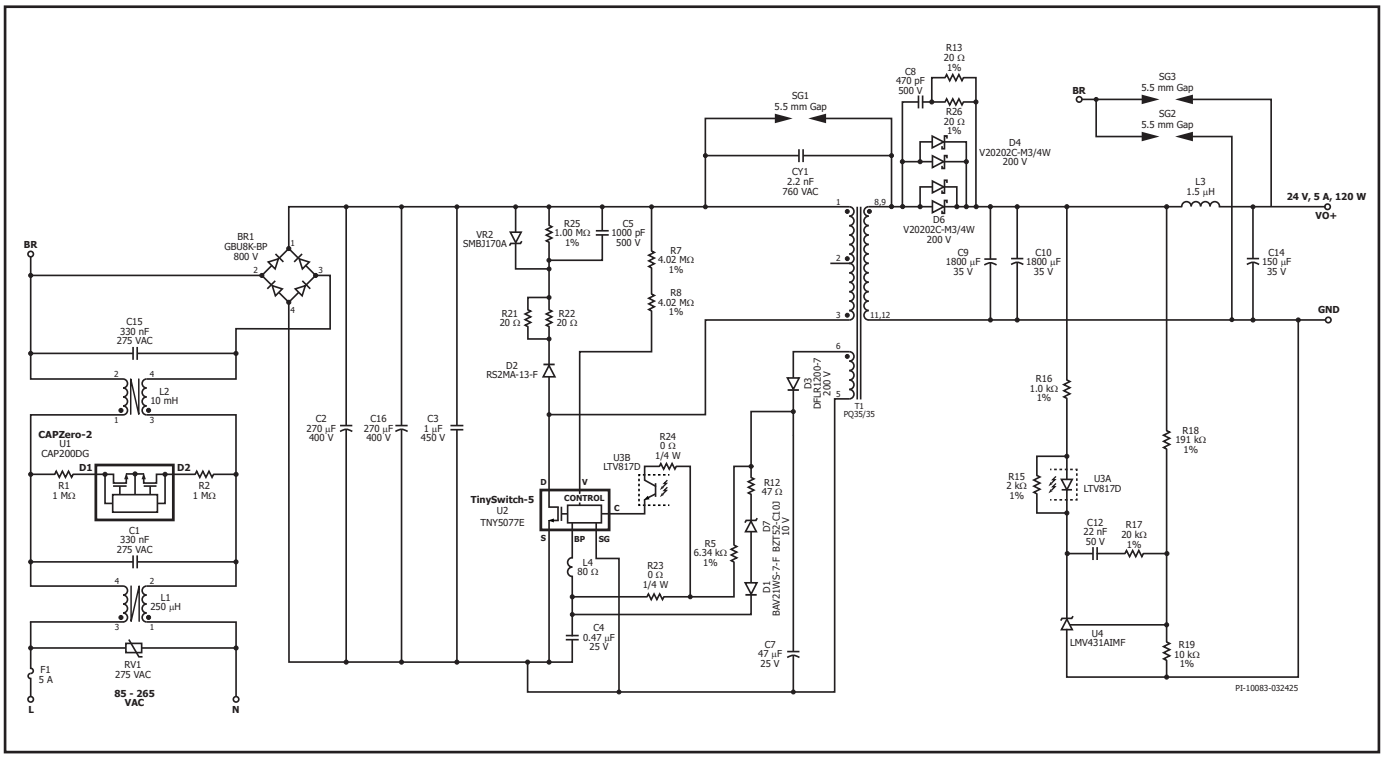

Figure 21. Schematic of DER-1027 120 W, 24 V Power Supply using TNY5077E.

A High-Efficiency, 120 W Output Power Supply (TinySwitch-5)

The circuit shown in Figure 21 is a 120 W output high-efficiency flyback power supply designed for 24 V, 5 A output from universal input using the TNY5077E.

The supply features line undervoltage lockout, line overvoltage protection, primary sensed output overvoltage, output short-circuit protection, high full load efficiency (>90%), high average efficiency (>90%) and low no-load input power consumption (<80 mW at 265 VAC). Output regulation is accomplished using optocoupler and a shunt regulator (LMV431) .

Fuse F1 isolates the circuit and provides protection from component failure. Common mode choke L1 and L2 with X capacitor C1 and C15 attenuate for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitors C2 and C16. Capacitor CY1 is used to mitigate common mode EMI. Additionally, TinySwitch-5 frequency jitter improves EMI performance.

The bleeding resistors, R1 and R2 together with a CAPZero™ IC are used to discharge the stored energy in the input X capacitor C1 and C15 to meet safety discharge requirements.

Line undervoltage and overvoltage is determined by the current supplied to the V pin by resistors R7 and R8.

The input capacitors C2 and C16 are sufficient to maintain full output power delivery at 85 VAC input. The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U2. A RCDZ clamp formed by D2, R22, R21, R25, C5, and VR2 limits the peak drain voltage, limiting the leakage inductance turn-off voltage spike on the DRAIN pin to a safe value.

As the TinySwitch-5 devices are completely self-powered, there is no requirement for an auxiliary or bias winding on the transformer. However by adding a bias winding, power consumption will be reduced. A bias winding is used to supply the TinySwitch-5 device. Resistor R5 feeds current into the BP pin, inhibiting the internal high-voltage current source that would otherwise maintain the BP pin capacitor (C4) voltage during the internal MOSFET off-time. This reduces no-load consumption <80 mW at 265 VAC. Ferrite bead (L4) was used to increase noise immunity.

Output overvoltage protection of the (resistor R12, Zener D7, and blocking diode D1) load against open loop faults is achieved using the bias circuit. When an overvoltage condition occurs, the bias voltage exceeds the sum of Zener D7, D1 and the BP pin voltage, and current begins to flow into the BP pin. When this current exceeds ISD, TinySwitch-5 will stop switching. Auto-restart will occur and continue until the output returns to regulation.

Schottky diodes D4 and D6 rectify the 24 V output T1. Resistors R13, R26, and capacitor C8 snub the voltage spike caused by the commutation of D4 and D6. The output voltage is filtered by C9, C10, L3, and C14. Low ESR capacitor C9 and C10 minimize output voltage ripple, while the post filter (L3) and (C14) further attenuates noise and ripple.

The output voltage is sensed via resistor divider R18 and R19. Output voltage is regulated to achieve a voltage of 1.24 V on the LMV431 REF pin. As the cathode voltage changes, the current through the optocoupler LED and transistor within U2 changes. R12, R14 and C15 provide stable operation while resistor R16 ensures minimum bias to U3.

Output regulation is achieved by modulation of off-time (switching frequency) and primary ILIM which are adjusted by input from U2 as output load changes. At high load, low switch off-time ensures high switching frequency while increased ILIM increases the amount of energy transferred per cycle. As load is reduced, off time increases reducing switching frequency and ILIM - allowing shorter on time per switch cycle and less energy transfer.

A metal heatsink is required to keep the TinySwitch-5, bridge rectifier, and secondary rectifier diode device below 110 °C when operating under full load, low-line, while at maximum ambient temperature.

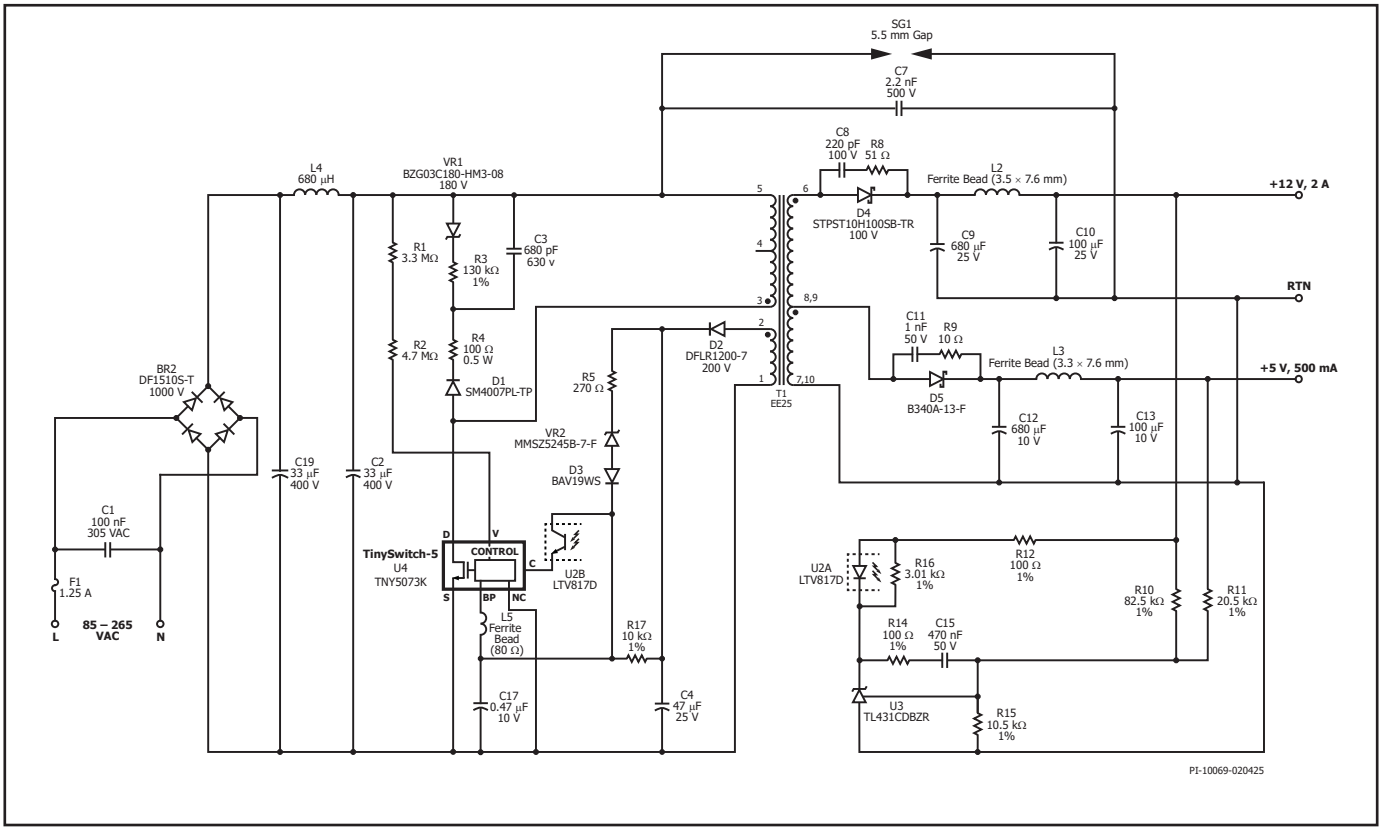

Figure 22. Schematic of RDR-1016 26.5 W, Dual Output Power Supply, 12 V / 2 A and 5 V / 500 mA using TNY5073K.

A High-Efficiency, 27 W Dual Output Power Supply (TinySwitch-5)

The circuit shown in Figure 22 delivers 27 W (12 V at 2 A and 5V a 500 mA) from 85 VAC to 265 VAC input using TNY5073K.

The supply features line undervoltage lockout, line overvoltage protection, primary sensed output overvoltage, output short-circuit protection, high 115 VAC full load efficiency (>86%), high 230 VAC full load efficiency (>87%), high average efficiency (>85.5%) and low no-load input power consumption (<50 mW at 230 VAC). Output regulation is accomplished using an optocoupler and a shunt regulator (TL431) feedback.

The input fuse F1 provides protection against excess input current resulting from catastrophic failure of any components in the power supply. The bridge rectifier BR2 rectifies the AC input supply. Capacitors C2 and C19 filter the rectified AC input, and together with inductor L4, form a pi-filter to attenuate differential mode EMI. The X capacitor C1 also helps to reduce differential mode EMI. The Y capacitor C7, connected between the power supply output and input, helps reduce common mode EMI. Additionally, the TinySwitch-5 frequency jitter feature significantly reduces EMI. One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the TinySwitch-5 IC (U4).

Line undervoltage and overvoltage is determined by the current supplied by Resistors R1 and R2 to the V pin.

An RCDZ clamp, consisting of diode D1, resistors R3 and R4, capacitor C3, and Zener VR1, limits the peak drain voltage of U4 at the moment the switch inside U4 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The TinySwitch-5 IC is self-starting, using an internal high-voltage current source to charge the primary BYPASS pin capacitor (C17) when AC is first applied. An optional ferrite bead (L5) was used to increase noise immunity. During normal operation, the IC primary controller is powered from a bias winding on the transformer T1. Output of this bias winding is rectified by diode D2 and filtered by capacitor C4. Resistor R17 limits the current being supplied to the BYPASS pin of TinySwitch-5 IC (U4). Resistor R17 feeds current into the BP pin, inhibiting the internal high-voltage current source that would otherwise maintain the BP pin capacitor voltage (C17) during the internal MOSFET off-time. This design reduces no-load consumption to less than 50 mW at 230 VAC.

Primary sensed OVP can be achieved by connecting a series combination of a Zener diode (VR2), a current limiting resistor (R5), and a blocking diode D3 from the bias voltage supply to the BYPASS pin. In the event of overvoltage on any output, the increased voltage across the bias winding causes the Zener diode (VR2) to conduct allowing current to flow into the BP pin. Once the current exceeds the current threshold (I_{SD}), the TinySwitch-5 will stop switching, and begin auto-restart which will continue to cycle until the output voltage drops back into regulation.

Output rectification for the 12 V output is provided by the secondary rectifier diode D4, while 5 V output rectification is accomplished by secondary rectifier diode D5. An RC snubber network, consisting of R8 and C8 for D4 and R9 and C11 for D5, damps high frequency ringing across the secondary rectifier diodes, which is induced by leakage inductance in the transformer windings and the secondary trace.

Very low capacitors, C9 and C12, provide filtering for their respective outputs. Ferrite beads L2 and L3, along with output capacitors C10 and C13, form low-pass filters that help reduce output ripple for both 12 V and 5 V outputs.

In the feedback circuit, the output voltages are sensed via the resistor divider R10, R11, and R15. These voltages are regulated to achieve 2.495 V on the TL431 REF pin. The feedback current ratio between the 12 V and 5 V outputs is approximately 1:1, ensuring good output and cross-regulation. As the cathode voltage changes, the current through the optocoupler LED and transistor within U2 changes. R12, R14 and C15 provide stable operation, while resistor R16 ensures minimum bias to U3. The bias winding voltage was tuned to approximately 10 V at no-load and high-line to further reduce no-load input power.

Typically, the feedback current into the CONTROL pin at high line is around 3 mA. This current is sourced from both the bias winding (voltage across C4) and directly from the output, providing load on the power supply output. To minimize dissipation from the bias winding under no-load conditions, the number of bias winding turns and the value of C4 were adjusted to achieve a minimum voltage of approximately 10 V across C4. This is the minimum required to keep the optocoupler biased and the output in regulation.

To further minimize dissipation in the secondary-side feedback circuit, a high CTR (300% – 600%) optocoupler was used. This reduced the secondary-side opto-LED current from around 3 mA to less than 1 mA, thereby reducing the effective load on the output. Additionally, the standard 2.5 V TL431 voltage reference could be replaced with the 1.24 V LMV431, reducing the supply current requirement of this component from 1 mA to 100 µA.

A heat spreader in the form of a PCB copper plane was added to keep the TinySwitch-5 and secondary rectifier diode device below 110 °C when operating.

Revision	Notes	Date
A	Introduction release.	03/25
B	Update ISSW formula in page 20 from (IS1 - IS2) to (IS2 - IS1)	09/25
C	Removed all ILIM selection as per PCN-25481.	12/25

For the latest updates, visit our website: www.power.com

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