Design Example Report

Title	**100 W Isolated Flyback Power Supply Using InnoSwitch™4-QR PowiGaN™ INN4277C-H185**
Specification	90 VAC – 265 VAC Input; 12 V / 8.34 A Output
Application	Appliance Application
Author	Applications Engineering Department
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Revision	A

Summary and Features

- Off-line CV/CC QR flyback integrated switcher IC with 750 V PowiGaN™ and synchronous rectification for higher efficiency
- <40 mW no-load input power at 230 VAC input
- Very high average efficiency
  - 92.4% at 115 VAC and >93% at 230 VAC
- Very high full-load efficiency
  - 91.4% at 115 VAC and 93.2% at 230 VAC
- Secondary-side control provides accurate output regulation via FluxLink™ communication
  - Better than +/- 1% voltage regulation across load and line
  - Eliminates conventional optocoupler feedback – increases reliability
- Input voltage monitor with accurate brown-in/brown-out protection
- Meets EN550022 and CISPR-22 Class B conducted EMI

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 12 V / 8.34 A power supply using the InnoSwitch4-QR INN4277C-H185 IC. This design shows the high-power density and efficiency that is possible due to the high level of integration that combines the InnoSwitch4-QR controller and FluxLink communication with a primary-side PowiGaN power switch.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

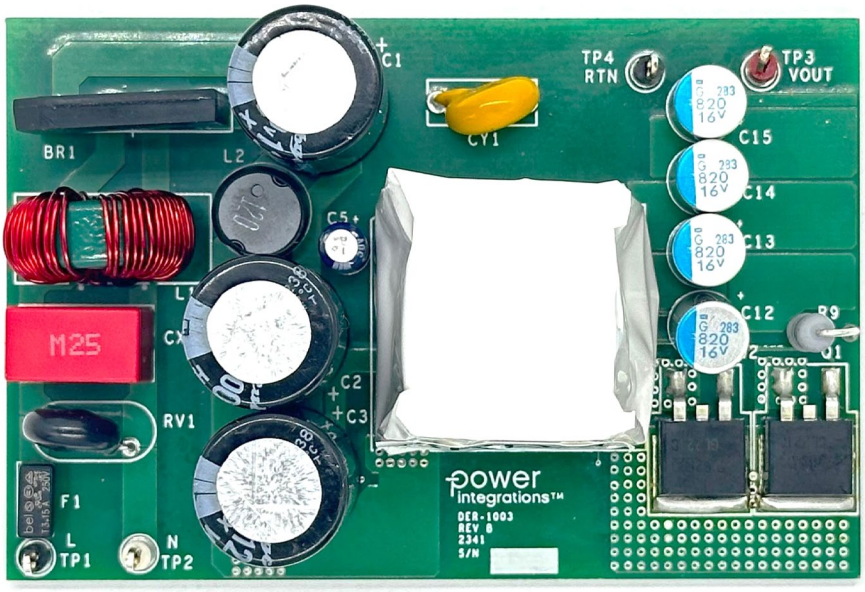


Figure 1 – Populated Circuit Board, Top.

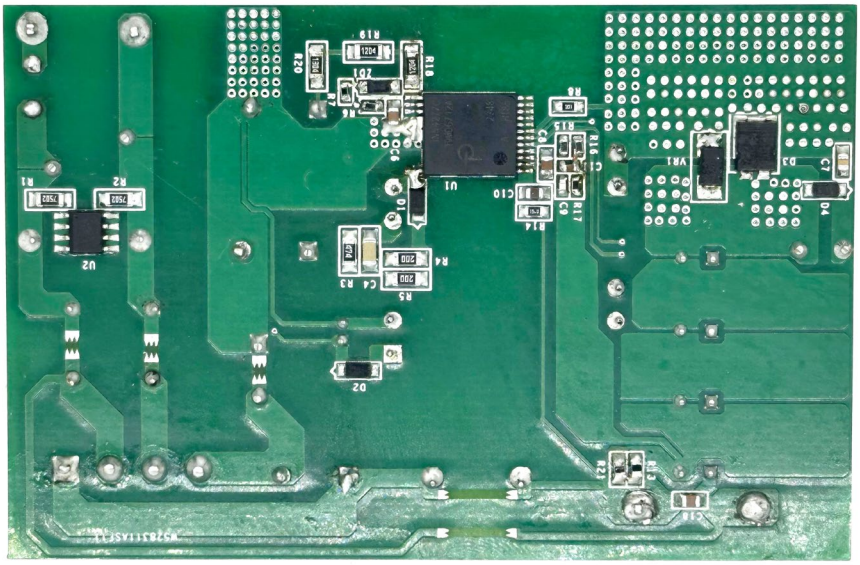


Figure 2 – Populated Circuit Board, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min	Nom	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115/230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				40	mW	
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz Bandwidth, at 25 °C Ambient
Output Current	I_{OUT}		8.34		A	
Total Output Power						
Continuous Output Power	P_{OUT}		100		W	
Efficiency						
	η		91.4		%	Full Load @ 115 VAC
			93.2			Full Load @ 230 VAC
			92.4			Average @ 115 VAC
			93			Average @ 230 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				2	kV	1.2/50 μs Surge, IEC 61000-4-5, Impedance: 2 Ω Class A
Combination Wave Surge Test				6	kV	
EFT				4	kV	IEC 61000-4-4
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

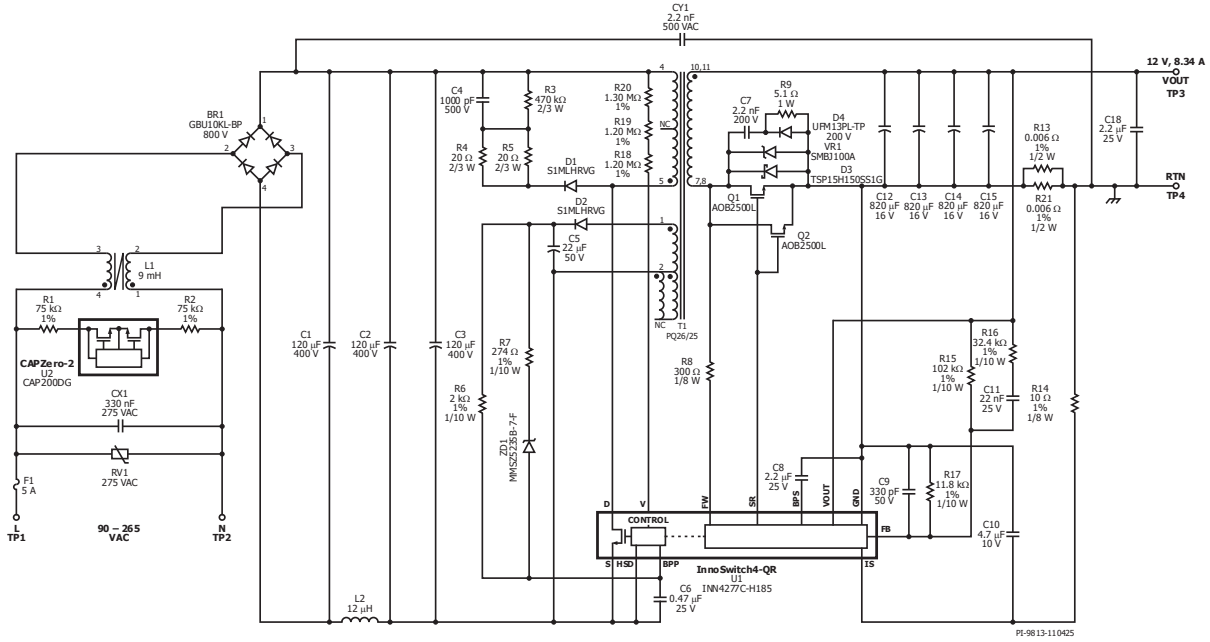


Figure 3 – Power Stage Schematic.

4 Circuit Description

The InnoSwitch4-QR IC combines primary, secondary and feedback circuits in a single surface-mount off-line flyback switcher IC. The IC incorporates a PowiGaN primary switch, primary-side controller, secondary-side controller and synchronous rectification driver and FluxLink technology provides accurate secondary-side sensing while eliminating the optocoupler found in conventional circuits. The InnoSwitch4-QR IC operates in quasi-resonant mode to increase efficiency.

4.1 Input EMI Filtering

Fuse F1 isolates the circuit and provides protection from component failure. Varistor RV1 clamps input voltage spikes that may be experienced during an input surge. X capacitor CX1 and common mode choke L1 form a filter to attenuate common mode noise. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitors C1, C2 and C3. Capacitors C1, C2 and C3 along with L2 form a pi-filter which attenuates both common and differential mode noise. The CAPZero™-2 IC (U2) with bleed resistors, R1 and R2, is used to discharge the stored energy in CX1 when AC is removed to meet safety requirements while ensuring very low no-load input power during normal operation. Capacitor CY1 is used to reduce common mode noise.

4.2 InnoSwitch4-QR IC Primary

One end of the transformer (T1) primary is connected to the rectified DC bus while the other is connected to the drain terminal of the power switch inside the InnoSwitch4-QR IC (U1). Resistors R18, R19 and R20 provide input voltage sensing for undervoltage and overvoltage protection.

A simple RCD clamp formed by diode D1, resistors R3, R4, R5 and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off the primary power switch. The clamp helps to dissipate the energy stored in the leakage inductance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R6 limits the current being supplied to the BPP pin of the InnoSwitch4-QR (U1).

Zener diode ZD1 along with resistor R7 provides primary sensed output overvoltage protection. In a flyback converter, the output of the auxiliary winding tracks the output voltage of the converter. In the event that an overvoltage condition appears on the output of the converter, the auxiliary winding voltage increases and causes breakdown of ZD1 which then causes a current to flow into the BPP pin of InnoSwitch4-QR IC U1.

If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-QR IC will enter auto-restart and protect the circuit and load from damage.

4.3 InnoSwitch4-QR IC Secondary

The InnoSwitch4-QR IC provides output voltage control, output current sensing and drive to the SR FETs providing synchronous rectification. The secondary of the transformer is rectified by SR FETs Q1, Q2 and diode D3, and filtered by output capacitors C12, C13, C14 and C15. High frequency ringing that occurs during switching transients is reduced via an RCD snubber R9, C7 and D4 along with TVS diode VR1. Diode D4 was used to minimize the dissipation in resistor R9.

The gates of Q1 and Q2 are turned on by the secondary-side controller inside IC U1. Timing for SR operation is derived from the winding voltage sensed via resistor R8 and fed into the FWD pin of the IC.

In continuous conduction mode, the SR MOSFET is turned off just prior to the secondary side requesting a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below a threshold of $V_{SR(TH)}$.

The FWD pin is also used to supply the secondary side of IC U1 when the V_{OUT} pin is below its threshold value. Capacitor C8 connected to the BPS pin of InnoSwitch4-QR IC U1 and provides decoupling for the internal circuitry.

Output current is sensed by monitoring the voltage drop across resistors R13 and R21 connected between the IS and GND pins. A low threshold of 35 mV is used to reduce losses. Capacitor C10 provides filtering on the IS pin.

The device operates in constant voltage mode before reaching the current limit set by resistor R13 and R21. During constant voltage mode operation, output voltage regulation is achieved by sensing the output voltage via resistors R15 and R17 which form a potential divider. The voltage across R17 is fed into the FB pin which has an internal voltage threshold of 1.265 V. Output voltage is adjusted to achieve a voltage of 1.265 V on the FB pin. Capacitor C9 provides noise filtering of the signal at the FB pin.

The capacitors C12, C13, C14, C15 and C18 are used to reduce high frequency output voltage ripple.

5 PCB Layout

PCB copper thickness is 2.0 oz.
PCB Material Thickness is 1.6 mm.
PCB Material is FR4.

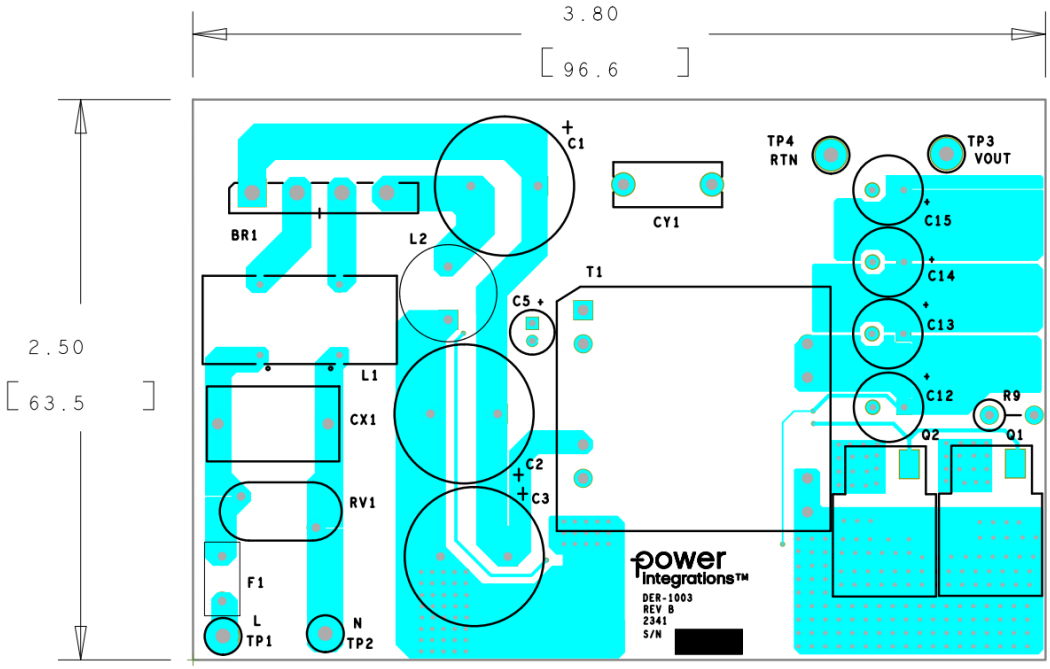


Figure 4 – Printed Circuit Layout, Top.

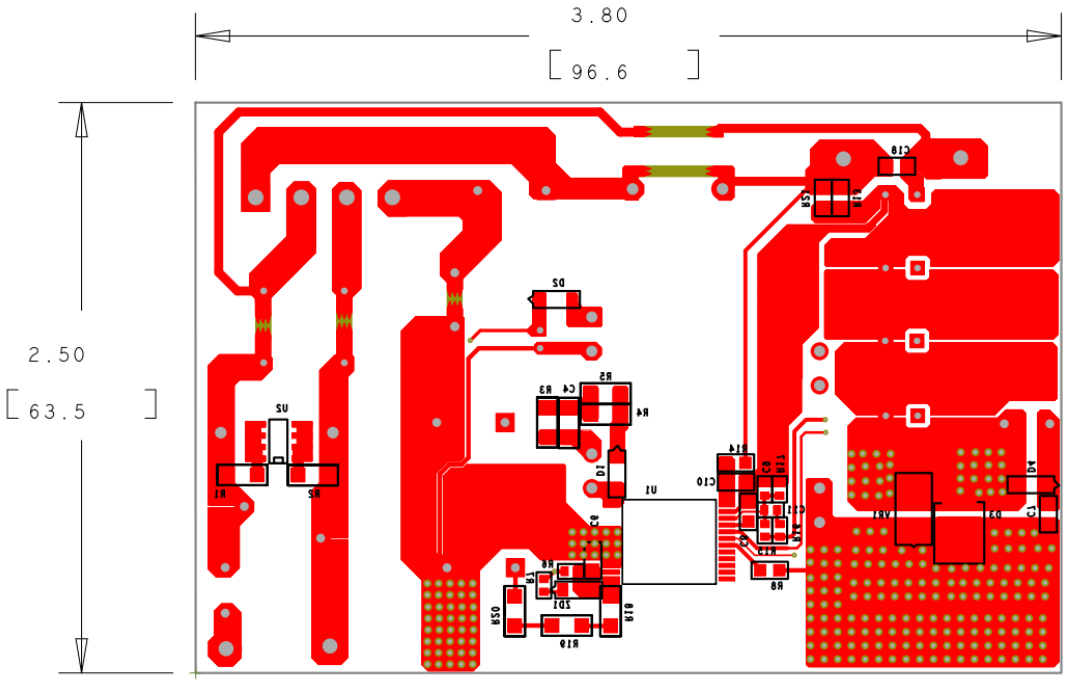


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 Bill of Material: Electrical Components

Item	Qty.	Ref Des.	Description	Mfr. Part Number	Manufacturer
1	1	BR1	BRIDGE RECTIFIER, Single Phase, Standard, 800 V, Through Hole GBU	GBU10KL-BP	Micro Commercial Co
2	3	C1 C2 C3	CAP, 120 µF, ±20%, 400 V Aluminum Electrolytic, Radial (16 x 32)	400HXW120MEFR16X30	Rubycon
3	1	C4	CAP, 1000 pF, ±10%, 500 V, Ceramic, X7R, 1206 (3216 Metric)	CC1206KKX7RBBB102	Yageo
4	1	C5	CAP, 22 µF, 50 V, Aluminum Electrolytic, Radial (5 x 11)	UPW1H220MDD	Nichicon
5	1	C6	CAP, 0.47 µF, ±10%, 25 V, Ceramic, X7R, 0805 (2012 Metric)	CGA4J2X7R1E474K125AA	TDK Corporation
6	1	C7	CAP, 2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX Corp
7	1	C8	CAP, 2.2 µF, ±10%, 25 V, Ceramic, X7R, 0805	C2012X7R1E225K125AB	TDK Corporation
8	1	C9	CAP, 330 pF, ±5%, 50 V, Ceramic, C0G, NP0, 0603	C0603C331J5GACAUTO	KEMET
9	1	C10	CAP, 4.7 µF, ±10%, 10 V, Ceramic, X7R 0805	LMK212B7475KGHT	Taiyo Yuden
10	1	C11	CAP, 0.022 µF, ±5%, 25 V, Ceramic, X7R, 0603	C0603C223J3RAC7867	KEMET
11	4	C12 C13 C14 C15	CAP, 820 µF, ±20%, 16 V, Al Organic Polymer, Radial (8 x 17.50)	APSG160ELL821MH16S	United Chemi-con
12	1	C18	CAP, 2.2 µF, ±10%, 25 V, Ceramic, X7R, 0805	CL21B225KAFVPNE	Samsung Electro-Mechanics America, Inc.
13	1	CX1	CAP, 330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth Electronics Inc.
14	1	CY1	CAP, 2200 pF, ±20%, Class Y1 - 500 VAC, Class X1 – 760 VAC, Ceramic, Y5U Radial, Disc	AY1222M47Y5UC63L0	Vishay/ BC Components
15	2	D1 D2	DIODE, Standard, 1000 V, 1 A, Surface Mount, Sub SMA	S1MLHRVG	TAIWAN SEMICONDUCTOR
16	1	D3	DIODE, Schottky, Trench, 150 V, 15 A, Surface Mount, TO-277A (SMPC)	TSP15H150S S1G	Taiwan Semiconductor Corporation
17	1	D4	DIODE, Gen Purp, 200 V, 1 A, SOD-123F, SOD123FL	UFM13PL-TP	Micro Commercial Co.
18	1	F1	FUSE, 5 A, 250 V, Long Time Lag, RST	RST 5-BULK	Belfuse
19	1	L1	INDUCTOR, 9 mH, Toroidal Common Mode Choke, Input CMC (LCM) #23 AWG Wirewound on Toroid Core: PI #30-00398-00 (JLW T18*10*7C-JL15 or equivalent.)	32-00455-00	Power Integrations
20	1	L2	INDUCTOR, 12 µH @100 KHz, ±10%, 5.1 A, 0.035 ohm, AEC-Q200, Unshielded, Ferrite, Radial, -40 °C ~ 85 °C, 11 x 11.5 mm	RFB1010-120L	Coilcraft
21	2	Q1 Q2	MOSFET, N-Channel 150 V 11.5 A (Ta), 152 A (Tc), 2.1 W (Ta), 375 W (Tc), Surface Mount, TO-263 (D2Pak)	AOB2500L	Alpha & Omega Semiconductor Inc.
22	2	R1 R2	RES, 75.0 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7502V	Panasonic
23	1	R3	RES, 470 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J474V	Panasonic
24	2	R4 R5	RES, 20 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J200V	Panasonic
25	1	R6	RES, 2 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2001V	Panasonic
26	1	R7	RES, 274 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2740V	Panasonic
27	1	R8	RES, 300 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ301V	Panasonic
28	1	R9	RES, 5.1 R, 5%, 1 W, Metal Oxide	RSF100JB-5R1	Yageo
29	2	R13 R21	RES, Current Sense, 0.006 Ohm, ±1%, 1/2 W, Thick Film, 0805	ERJ-6LWFR006V	Panasonic Electronic Components
30	1	R14	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic

31	1	R15	RES, 102 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1023V	Panasonic
32	1	R16	RES, 32.4 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
33	1	R17	RES, 11.8 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1182V	Panasonic
34	2	R18 R19	RES, 1.20 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1204V	Panasonic
35	1	R20	RES, 1.30 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1304V	Panasonic
36	1	RV1	VARISTOR, 275 VAC, 80 J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
37	1	T1	BOBBIN, PQ26/25, Vertical, 12 pins	PQ26X25	Pin Shine
38	1	U1	InnoSwitch4-QR, INN4277C-H185, InSOP-24D	INN4277C-H185	Power Integrations
39	1	U2	CAPZero-2, CAP200DG, SO-8C	CAP200DG	Power Integrations
40	1	VR1	DIODE, TVS, 162 V Clamp, 3.7 A Ipp, Unidirectional, Surface Mount DO-214AA (SMBJ)	SMBJ100A	Littelfuse
41	1	ZD1	DIODE, Zener, 6.8 V, 500 mW, SOD123	MMSZ5235B-7-F	Diodes, Inc

6.2 Bill of Material: Mechanical Components

Item	Qty.	Ref Des.	Description	Manufacturer	Mfr. Part Number
1	2	TP1 TP4	Test Point, BLK, THRU-HOLE MOUNT	Keystone	5011
2	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	Keystone	5012
3	1	TP3	Test Point, RED, THRU-HOLE MOUNT	Keystone	5010

7 Transformer Specification

7.1 Electrical Diagram

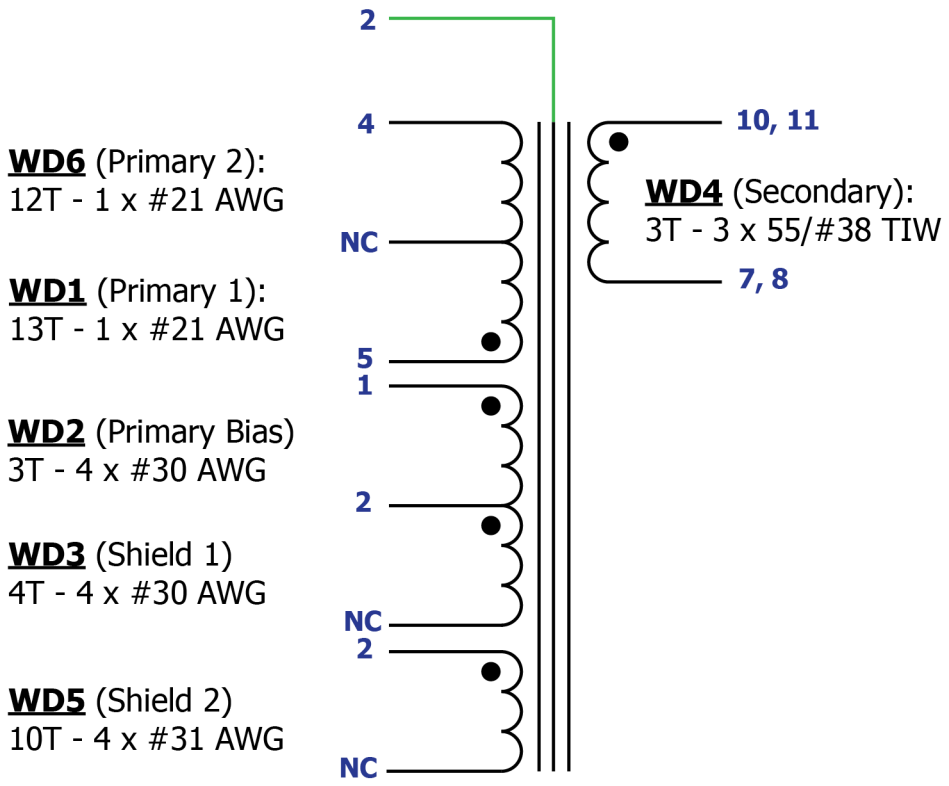


Figure 6 – Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between pin 4 and 5, with all other Windings open.	283 µH ±5.0%
Resonant Frequency	Measured between Pin 4 and Pin 5	2500 kHz (Nominal)
Primary Leakage Inductance	Measured between Pin 4 and 5, with all other Windings shorted.	3.2 µH (Max).

7.3 Materials List

Item	Description
[1]	Core: TDK-PQ26/25.
[2]	Bobbin: PQ26/25, 25-00055-00
[3]	Magnet wire: #21 AWG, double coated.
[4]	Magnet wire: #30 AWG, double coated.
[5]	Magnet wire: #31 AWG, double coated.
[6]	Magnet wire: 55/#38 AWG, Triple Insulated Litz wire
[7]	Bus wire: #28 AWG, Alpha wire, tinned copper.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 13.5 mm width.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 21.0 mm width.
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 16.0 mm width.
[11]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 33.0 mm width.
[12]	Varnish

7.4 Transformer Build Diagram

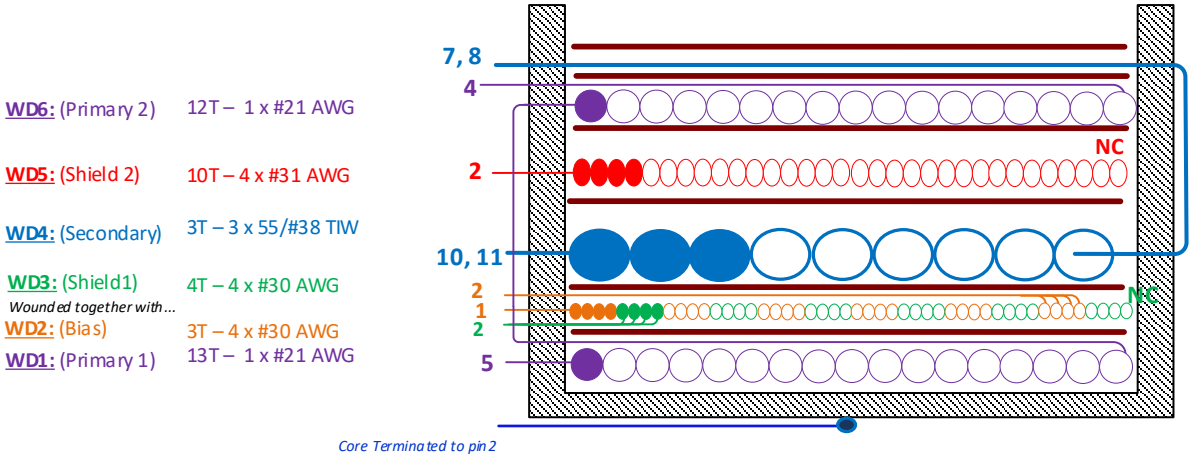


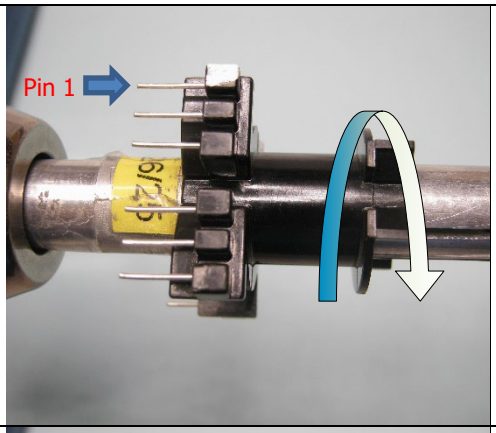
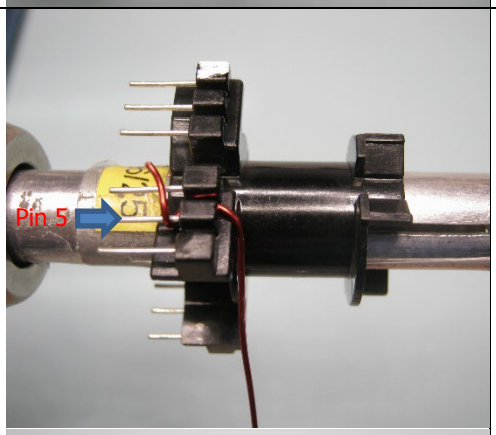
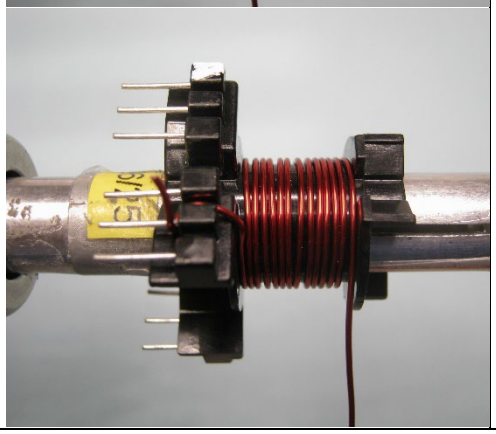
Figure 7 – Transformer Build Diagram.

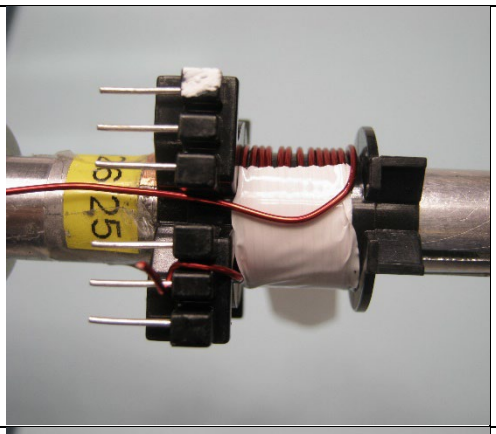
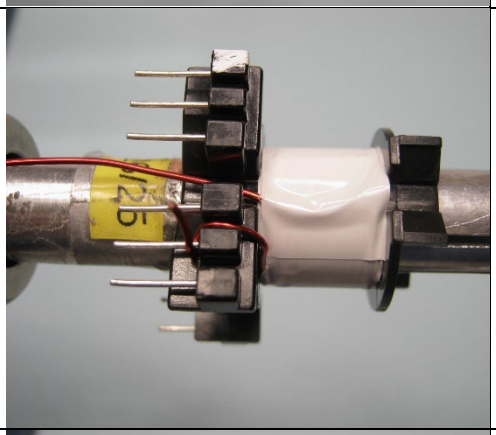
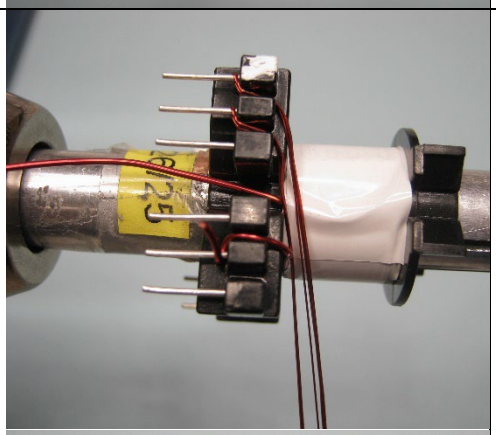
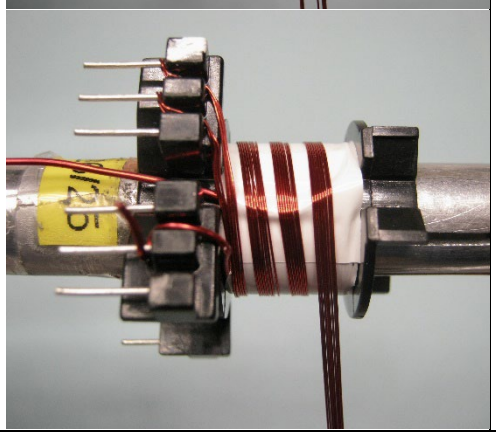
7.5 Transformer Instruction

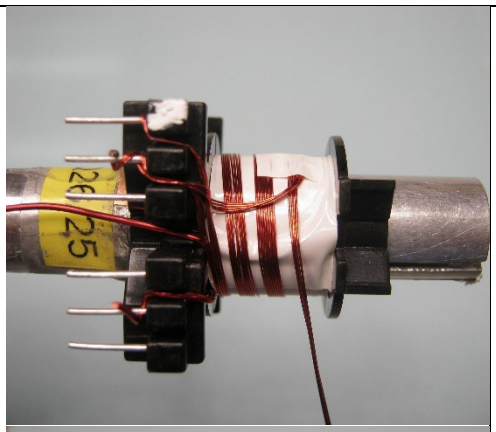
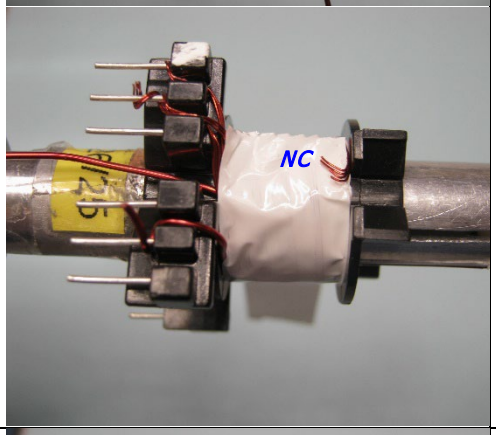
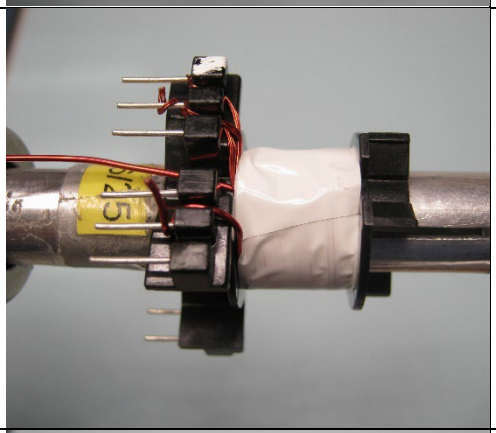
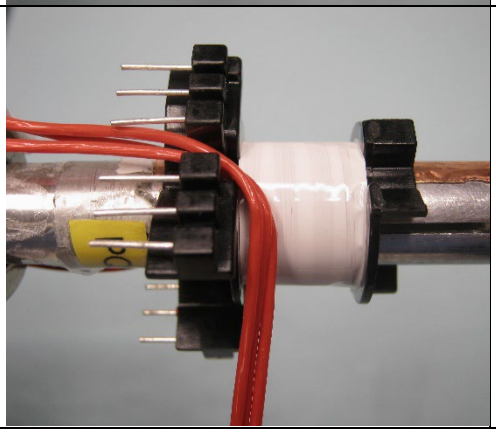
Winding preparation	Position the bobbin item [2] on the mandrel such that the primary pins side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 1st Primary	Start at pin 5, wind 13 turns of wire item [3] in 1 layer from left to right, spread the wire evenly across the bobbin width. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2nd Primary.
Insulation	1 layer of tape item [8].
WD2: Bias & WD3: Shield1	Use 4 wires item [4] start at pin 1 for Bias winding, also use 4 wires same item [4] start at pin 2 for Shield1 winding. Wind all 8 wires in parallel, at the 3rd turn bring 4 wires of Bias winding to the left and terminate at pin 2. Continue winding 1 more turn for Shield1 Winding and cut short as No-Connect.
Insulation	1 layer of tape item [8].

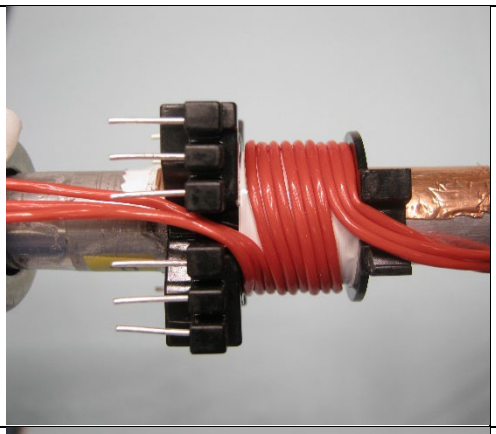
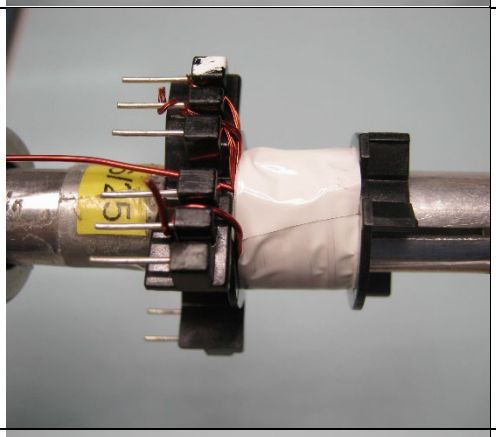
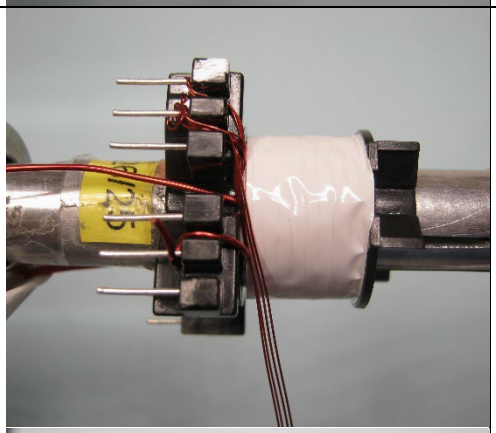
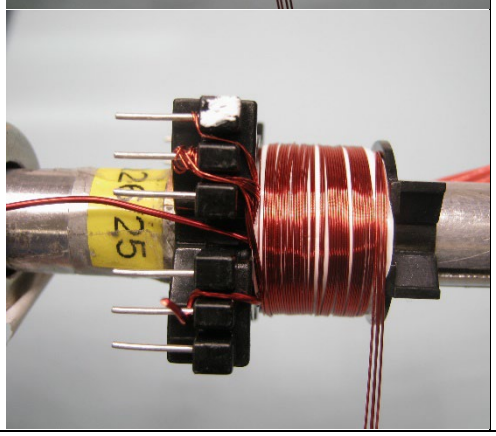
WD4 Secondary	Start from left slot at secondary pins side of bobbin with wire item [6] (will terminate at pins 10 & 11), wind 3 tri-filar turns from left to right. At the last turn exit at right slot and leave ~ 25 mm of wires floating (will terminate at pins 7 & 8).
Insulation	1 layer of tape item [8].
WD5 Shield2	Start at pin 2, wind 10 quad-filar turns of wire item [5], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape item [8].
WD6 2nd Primary	Use floating wire from WD1-1st Primary, wind 12 turns from left to right. At the last turn, bring the wire back to left and finish at pin 4.
Insulation	1 layer of tape item [8].
Finish	Bring 4 wires floating on the right of secondary winding to the left and secure 2 layers of tape item [8]. Solder start leads of secondary winding to pins 10 & 11, and end leads to pins 7 & 8. Gap core halves to get 283 μH. Use tape item [10] to cover one side of core only for bottom secondary side. Solder pin 2 with bus-wire item [7] then lean along core halves and secure with tape item [9]. Varnish with item [12]. Use tape item [11] to wrap around the transformer (see pictures below).

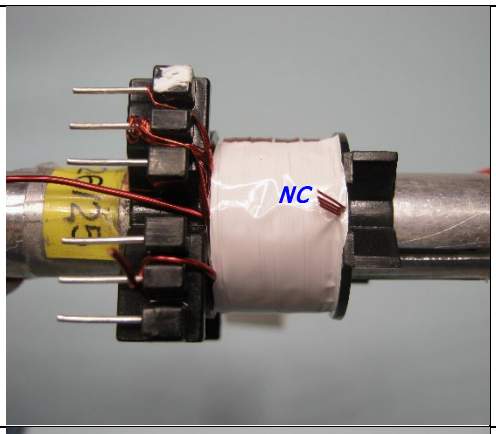
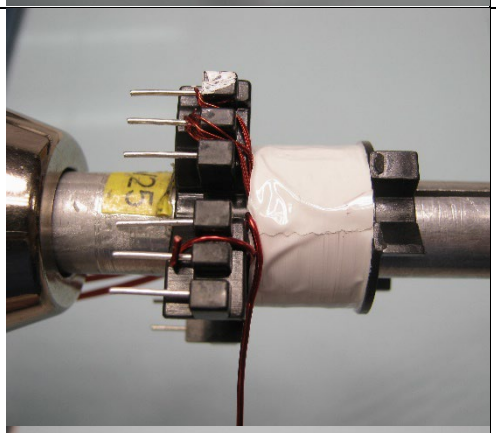
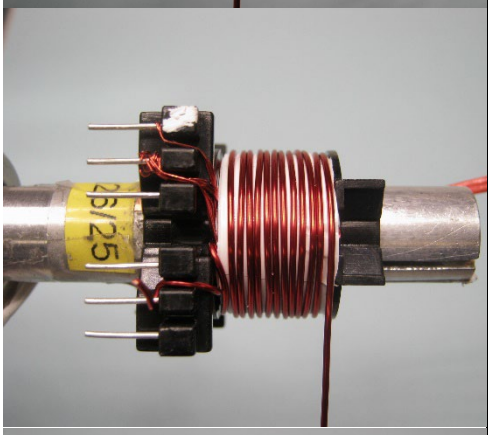
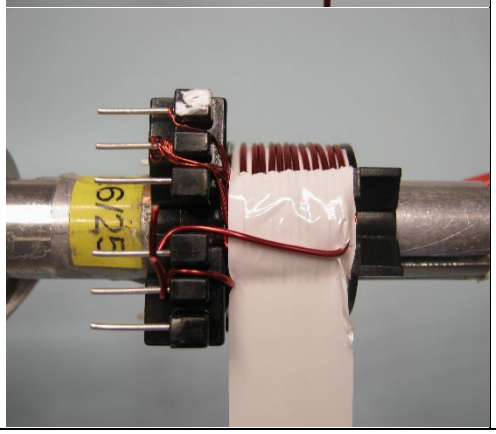
7.6 Winding Illustrations

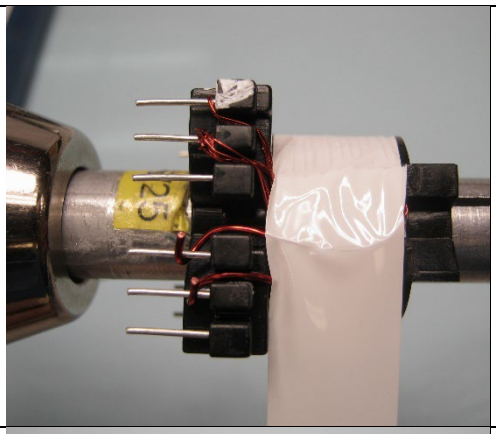
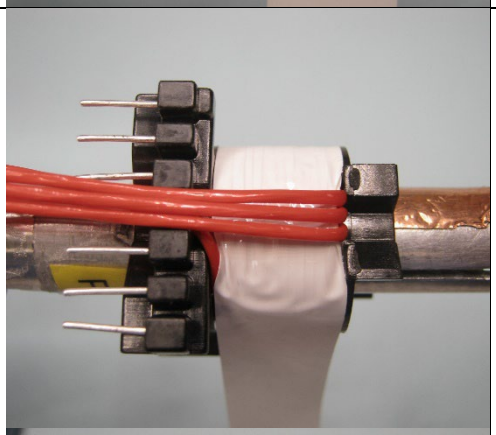
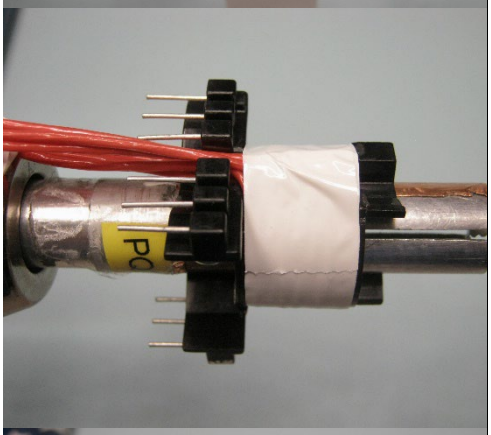
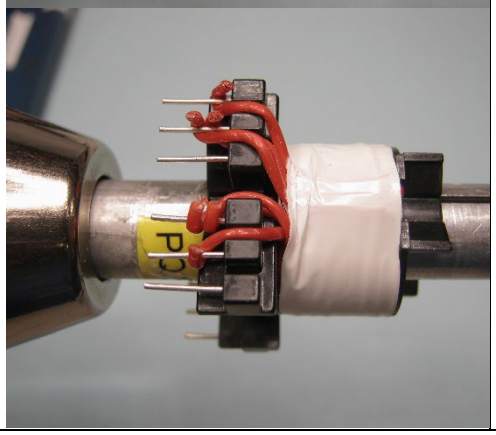
Winding preparation		Position the bobbin item [2] on the mandrel such that the primary pins side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **1st Primary**		Start at pin 5, wind 13 turns of wire item [3] in 1 layer from left to right, spread the wire evenly across the bobbin width.
		At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2nd Primary.

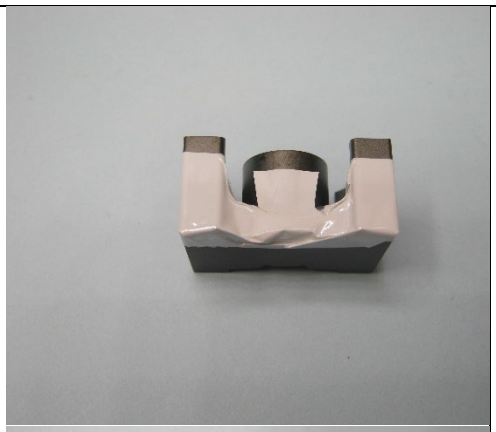
		
Insulation		1 layer of tape item [8].
WD2: Bias **&** **WD3: Shield1**	 	Use 4 wires item [4], start at pin 1 for Bias winding, also use 4 wires same item [4] start at pin 2 for Shield1 winding. Wind all 8 wires in parallel, at the 3rd turn bring 4 wires of Bias winding to the left and terminate at pin 2. Continue winding 1 more turn for Shield1 Winding and cut short as No-Connect.

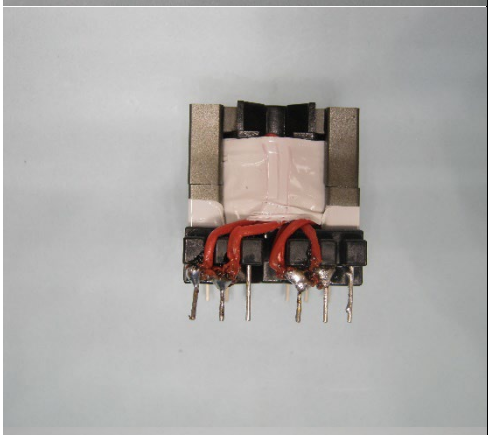
	 	
Insulation		1 layer of tape item [8].
WD4 **Secondary**		Start from left slot at secondary pins side of bobbin (will terminate at pins 10 & 11), wind 3 tri-filar turns of wire item [6] from left to right. At the last turn exit at right slot and leave ~25 mm of wires floating (will terminate at pins 7 & 8).

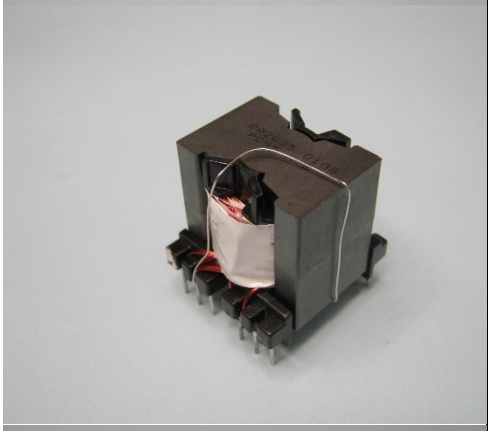
		
Insulation		1 layer of tape item [8].
WD5 **Shield2**	 	Start at pin 2, wind 10 quad-filar turns of wire item [5], from left to right. At the last turn, cut short to leave as No-Connect, and 1 layer of tape item [8].

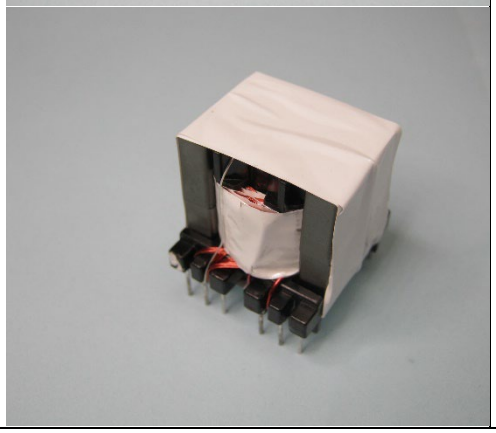
		
WD6 **2nd Primary**	  	Use floating wire from WD1-1st Primary, wind 12 turns from left to right. At the last turn, bring the wire back to left and finish at pin 4.

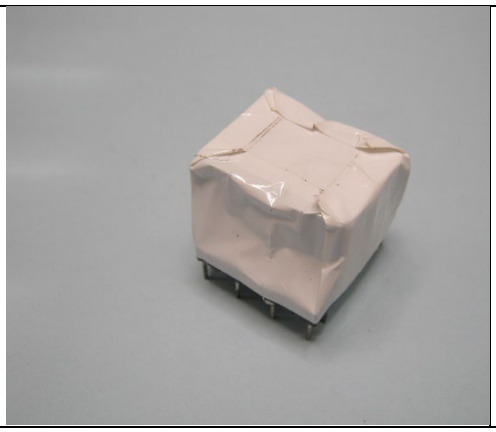
Insulation		1 layer of tape item [8].
Finish	  	Bring 4 wires floating on the right of secondary winding to the left and secure 2 layers of tape item [8]. Solder start leads of secondary winding to pins 10 & 11, and end leads to pins 7 & 8. Gap core halves to get 283 μH. Use tape item [10] to cover one side of core only for bottom secondary side. Solder pin 2 with bus-wire item [7] then lean along core halves and secure with tape item [9]. Varnish with item [12]. Use tape item [11] to wrap around the transformer, (see pictures beside).











8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch4-QR_Flyback_050823; Rev.0.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4 QR Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN			90	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	360.0		360.0	µF	Input capacitor
9	VOUT	12.00		12.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	8.340		8.340	A	Output current
12	POUT			100.08	W	Output power
13	EFFICIENCY	0.90		0.90		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
16	**PRIMARY CONTROLLER SELECTION**					
17	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
18	DEVICE_GENERIC	INN4277		INN4277		Generic device code
19	DEVICE_CODE			INN4277C		Actual device code
20	POUT_MAX			135	W	Power capability of the device based on thermal performance
21	RDSON_100DEG			0.29	Ω	Primary switch on time drain resistance at 100 °C
22	ILIMIT_MIN			3.162	A	Minimum current limit of the primary switch
23	ILIMIT_TYP			3.400	A	Typical current limit of the primary switch
24	ILIMIT_MAX			3.638	A	Maximum current limit of the primary switch
25	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
26	VDRAIN_ON_PRSW			0.28	V	Primary switch on time drain voltage
27	VDRAIN_OFF_PRSW			503.4	V	Peak drain voltage on the primary switch during turn-off
28	**WORST CASE ELECTRICAL PARAMETERS**					
29	FSWITCHING_MAX	90000		90000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
30	VOR	100.0		100.0	V	Secondary voltage reflected to the primary when the primary switch turns off
31	VMIN			109.22	V	Valley of the minimum input AC voltage at full load
32	KP			0.68		Measure of continuous/discontinuous mode of operation
33	MODE_OPERATION			CCM		Mode of operation
34	DUTYCYCLE			0.479		Primary switch duty cycle

35	TIME_ON			8.82	µs	Primary switch on-time is greater than 10.5 µs: Increase the controller switching frequency or increase the VOR NOTE: Actual operation limits TIME_ON to ton(max) and FSWITCHING will increase. Measured maximum FSW on board is around 80 kHz less than fOVL.
36	TIME_OFF			5.79	µs	Primary switch off-time
37	LPRIMARY_MIN			267.7	µH	Minimum primary inductance
38	LPRIMARY_TYP			281.8	µH	Typical primary inductance
39	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
40	LPRIMARY_MAX			295.9	µH	Maximum primary inductance
41	**PRIMARY CURRENT**					
42	IPEAK_PRIMARY			3.476	A	Primary switch peak current
43	IPEDESTAL_PRIMARY			0.992	A	Primary switch current pedestal
44	IAVG_PRIMARY			0.980	A	Primary switch average current
45	IRIPPLE_PRIMARY			2.858	A	Primary switch ripple current
46	IRMS_PRIMARY			1.527	A	Primary switch RMS current
47	**SECONDARY CURRENT**					
48	IPEAK_SECONDARY			28.971	A	Secondary winding peak current
49	IPEDESTAL_SECONDARY			8.265	A	Secondary winding current pedestal
50	IRMS_SECONDARY			13.283	A	Secondary winding RMS current
51	**TRANSFORMER CONSTRUCTION PARAMETERS**					
52	**CORE SELECTION**					
53	CORE	PQ26/25		PQ26/25		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
54	CORE CODE			B65877A0000R095		Core code
55	AE			122.00	mm^2	Core cross sectional area
56	LE			53.60	mm	Core magnetic path length
57	AL			5700	nH/turns^2	Ungapped core effective inductance
58	VE			6530.0	mm^3	Core volume
59	BOBBIN			B65878E1012D001		Bobbin
60	AW			47.00	mm^2	Window area of the bobbin
61	BW			12.70	mm	Bobbin width
62	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
63	**PRIMARY WINDING**					
64	NPRIMARY			25		Primary turns
65	BPEAK			3681	Gauss	Peak flux density
66	BMAX			3335	Gauss	Maximum flux density
67	BAC			1349	Gauss	AC flux density (0.5 x Peak to Peak)
68	ALG			451	nH/turns^2	Typical gapped core effective inductance
69	LG			0.313	mm	Core gap length
70	**PRIMARY BIAS WINDING**					
71	NBIAS_PRIMARY			3		Primary bias winding number of turns
72	**SECONDARY WINDING**					
73	NSECONDARY	3		3		Secondary winding number of turns
74	**SECONDARY BIAS WINDING**					

75	NBIAS_SECONDARY			NA		Secondary bias winding number of turns
76	**PRIMARY COMPONENTS SELECTION**					
77	**LINE UNDERVOLTAGE**					
78	BROWN-IN REQURED	72.30		72.30	V	Required AC RMS/DC line voltage brown-in threshold
79	RLS			3.74	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
80	BROWN-IN ACTUAL			61.9 V - 74.9 V	V	Actual AC RMS/DC brown-in range
81	BROWN-OUT ACTUAL			55.1 V - 68.2 V	V	Actual AC RMS/DC brown-out range
82	**LINE OVERVOLTAGE**					
83	OVERVOLTAGE_LINE			279 V - 316.6 V	V	Actual AC RMS/DC line over-voltage range
84	**PRIMARY BIAS DIODE**					
85	VBIAS_PRIMARY	10.0		10.0	V	Rectified primary bias voltage
86	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
87	VREVERSE_BIASDIODE_PRIMARY			56.80	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
88	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
89	CBPP			0.47	µF	BPP pin capacitor
90	**SECONDARY COMPONENTS**					
91	RFB_UPPER	102.00		102.00	kΩ	Upper feedback resistor (connected to the first output voltage)
92	RFB_LOWER			12.10	kΩ	Lower feedback resistor
93	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
94	**SECONDARY BIAS DIODE**					
95	USE_SECONDARY_BIAS	NO		NO		Use secondary bias winding for the design
96	VBIAS_SECONDARY			NA	V	Rectified secondary bias voltage
97	VF_BIAS_SECONDARY			NA	V	Bias winding diode forward drop
98	VREVERSE_BIASDIODE_SECONDARY			NA	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
99	CBIAS_SECONDARY			NA	µF	Bias winding rectification capacitor
100	CBPS			NA	µF	BPP pin capacitor
101	**MULTIPLE OUTPUT PARAMETERS**					
102	OUTPUT 1					
103	VOUT1			12.00	V	Output 1 voltage
104	IOUT1			8.34	A	Output 1 current
105	POUT1			100.08	W	Output 1 power
106	IRMS_SECONDARY1			13.283	A	Root mean squared value of the secondary current for output 1
107	IRIPPLE_CAP_OUTPUT1			10.338	A	Current ripple on the secondary waveform for output 1
108	NSECONDARY1			3		Number of turns for output 1
109	VREVERSE_RECTIFIER1			56.80	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
110	SRFET1	AOB2500L		AOB2500L		Secondary rectifier (Logic MOSFET) for output 1
111	VF_SRFET1			0.054	V	SRFET on-time drain voltage for output 1
112	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
113	RDSON_SRFET1			5.1	mΩ	SRFET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1

114	**OUTPUT 2**					
115	VOUT2			0.00	V	Output 2 voltage
116	IOUT2			0.000	A	Output 2 current
117	POUT2			0.00	W	Output 2 power
118	IRMS_SECONDARY2			0.000	A	Root mean squared value of the secondary current for output 2
119	IRIPPLE_CAP_OUTPUT2			0.000	A	Current ripple on the secondary waveform for output 2
120	NSECONDARY2			0		Number of turns for output 2
121	VREVERSE_RECTIFIER2			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
122	SRFET2	Auto		NA		Secondary rectifier (Logic MOSFET) for output 2
123	VF_SRFET2			NA	V	SRFET on-time drain voltage for output 2
124	VBREAKDOWN_SRFET2			NA	V	SRFET breakdown voltage for output 2
125	RDSON_SRFET2			NA	mΩ	SRFET on-time drain resistance at 25 °C and VGS = 4.4 V for output 2
126	**OUTPUT 3**					
127	VOUT3			0.00	V	Output 3 voltage
128	IOUT3			0.000	A	Output 3 current
129	POUT3			0.00	W	Output 3 power
130	IRMS_SECONDARY3			0.000	A	Root mean squared value of the secondary current for output 3
131	IRIPPLE_CAP_OUTPUT3			0.000	A	Current ripple on the secondary waveform for output 3
132	NSECONDARY3			0		Number of turns for output 3
133	VREVERSE_RECTIFIER3			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 3
134	SRFET3	Auto		NA		Secondary rectifier (Logic MOSFET) for output 3
135	VF_SRFET3			NA	V	SRFET on-time drain voltage for output 3
136	VBREAKDOWN_SRFET3			NA	V	SRFET breakdown voltage for output 3
137	RDSON_SRFET3			NA	mΩ	SRFET on-time drain resistance at 25 °C and VGS = 4.4 V for output 3
138	PO_TOTAL			120.00	W	Total power of all outputs
139	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

9 Common Mode Choke (L1) Specification

9.1 Electrical Diagram

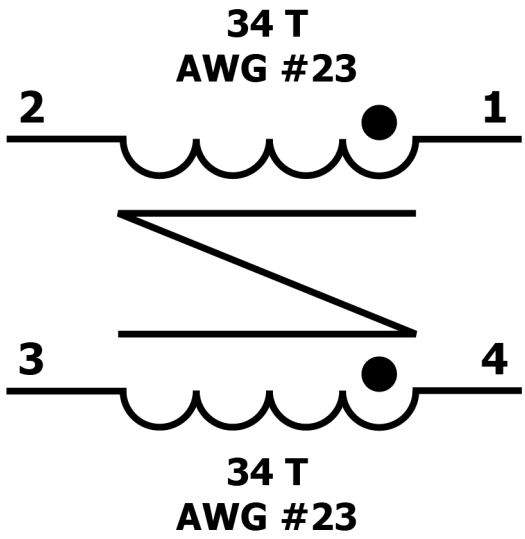


Figure 8 - CMC Electrical Diagram.

9.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and pin 3 or pin 2 and pin 4 with all other windings open.	9 mH
Tolerance	Tolerance of Primary Inductance.	±20%

9.3 Materials

Item	Description
[1]	Toroid Core: 30-00398-00 (Green)
[2]	Magnet Wire: #23 AWG

9.4 Assembled Picture

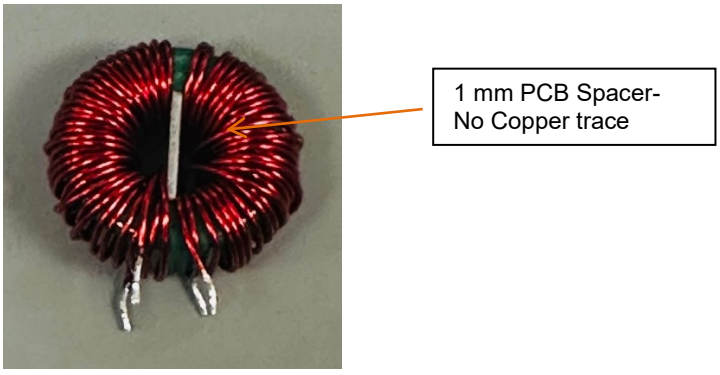


Figure 9 - CMC Assembled Photo.

Diameter: 22 mm
Width: 10 mm

9.5 Inductor Build Diagram

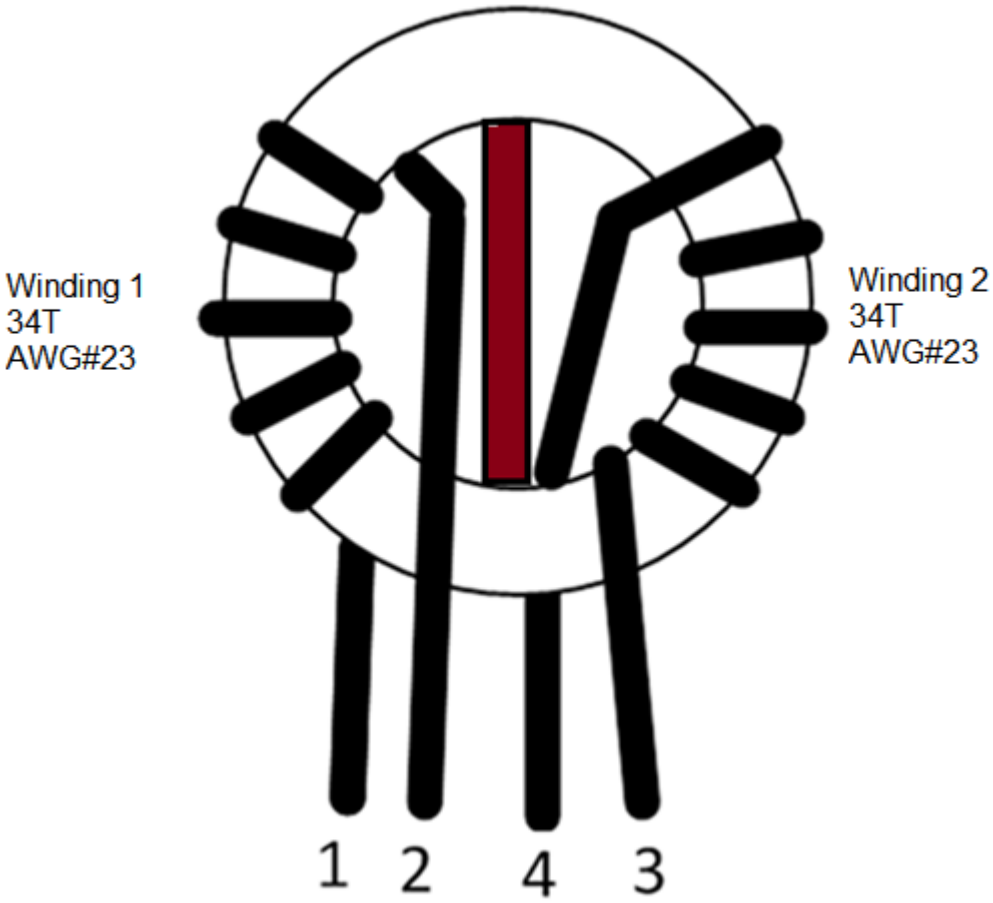


Figure 10 – Inductor Build Diagram.

9.6 Inductor Construction

1. Winding 1 - Wind 34 turns.
2. Winding 2 - Wind 34 turns.

10 Performance Data

All performance data has been taken on the board unless otherwise mentioned.

10.1 Power Meter Setting for Output Load > 5 W

For output power > 5 W the effect of voltage drop due to input cable impedance is noticeable particularly at low input line. The input power meter arrangement shown in figure 11 is recommended for accurate input power measurement.

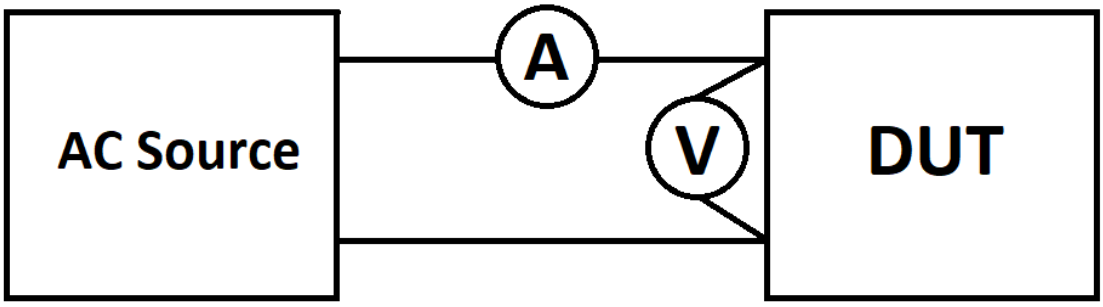


Figure 11 – Input Power meter setting for output load > 5 W.

10.2 Power Meter Setting for Output Load < 5 W

For output power < 5 W the effect of leakage current drawn by the voltmeter is noticeable especially at high line. The input power meter arrangement shown in figure 12 is recommended for accurate input power measurement at light- or no-load.

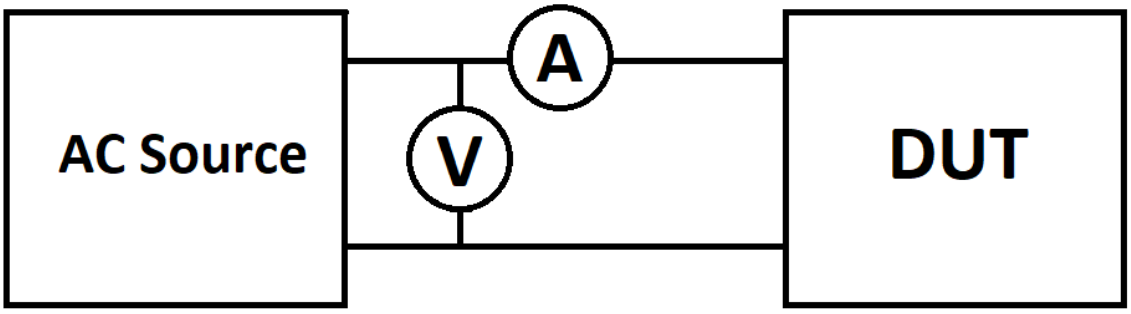


Figure 12 – Input Power meter setting for output load < 5 W.

10.3 Full-load Efficiency vs. Line

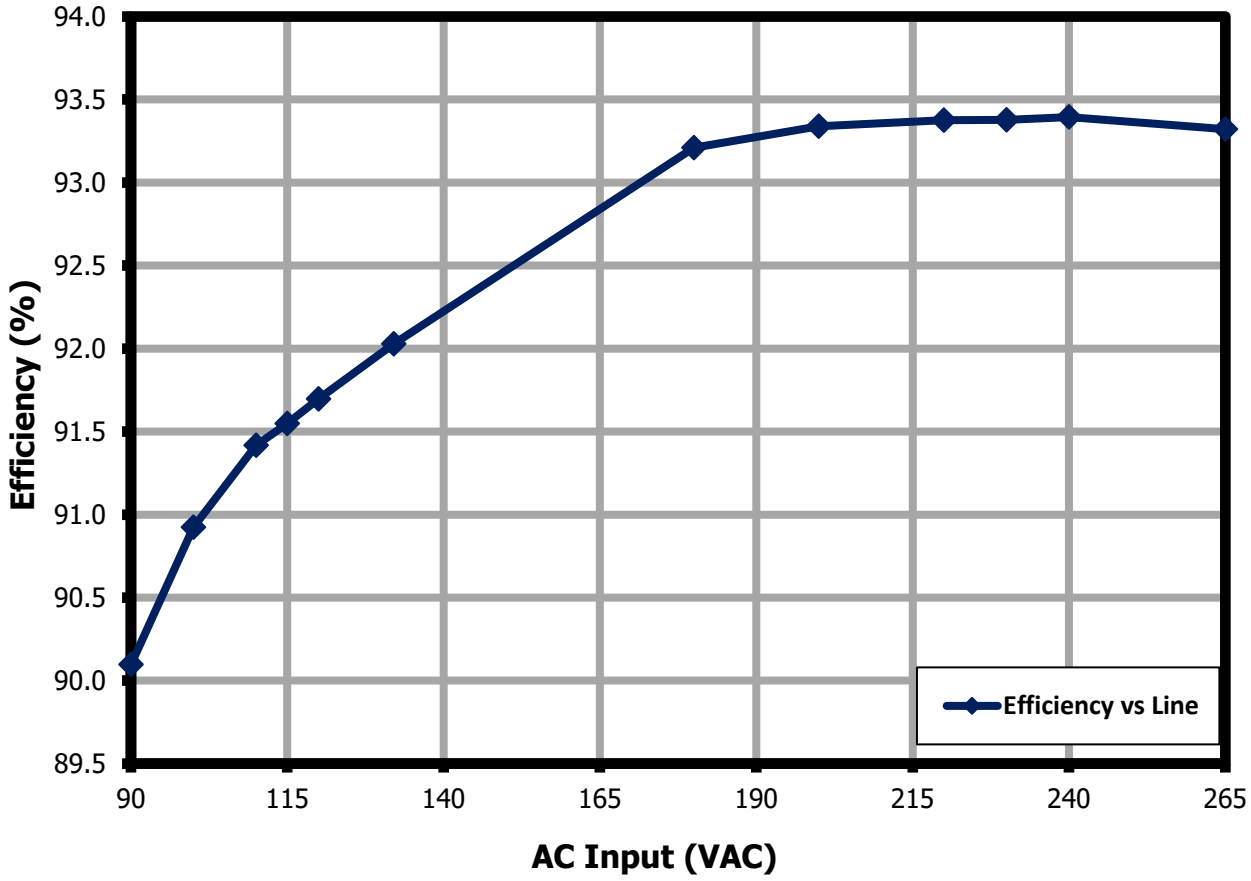


Figure 13 – Full-load Efficiency vs. Line, Room Ambient.

10.4 Efficiency vs. Line at Different Load Conditions

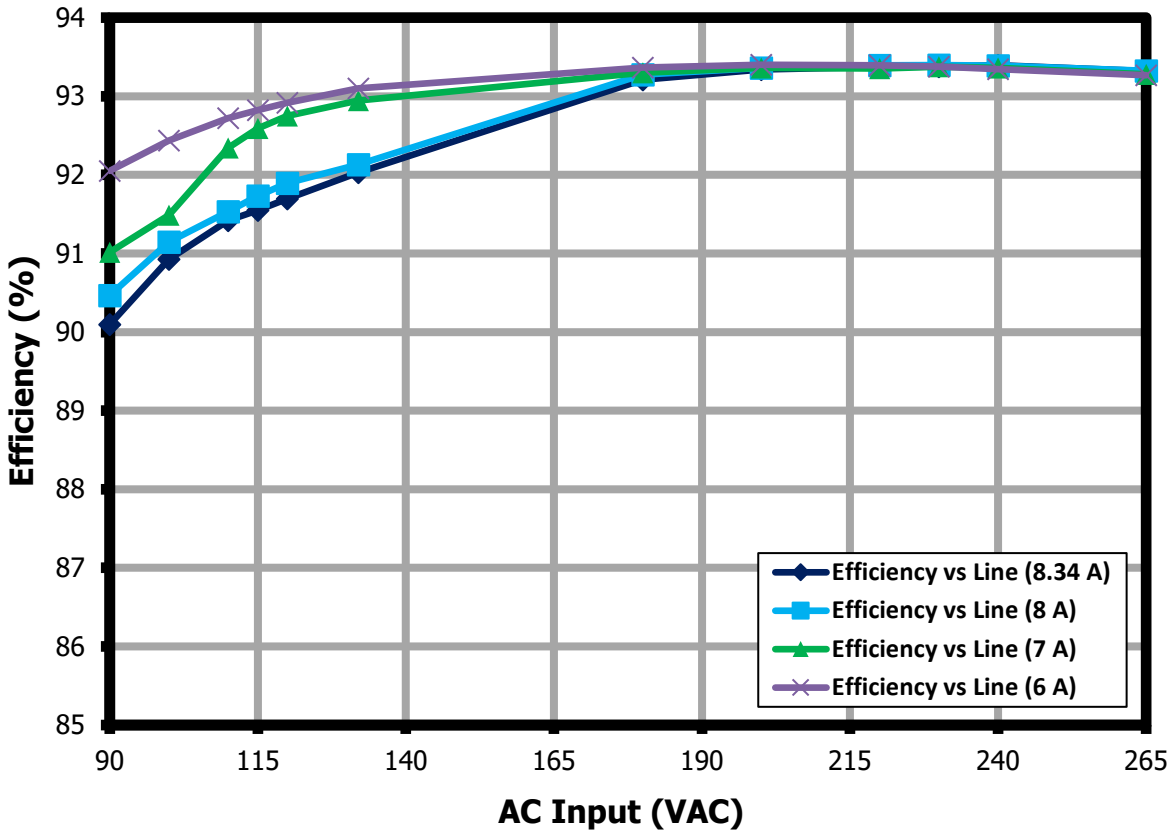


Figure 14 – Efficiency vs. Line, Room Ambient.

10.5 Efficiency vs. Load at Different Line Conditions

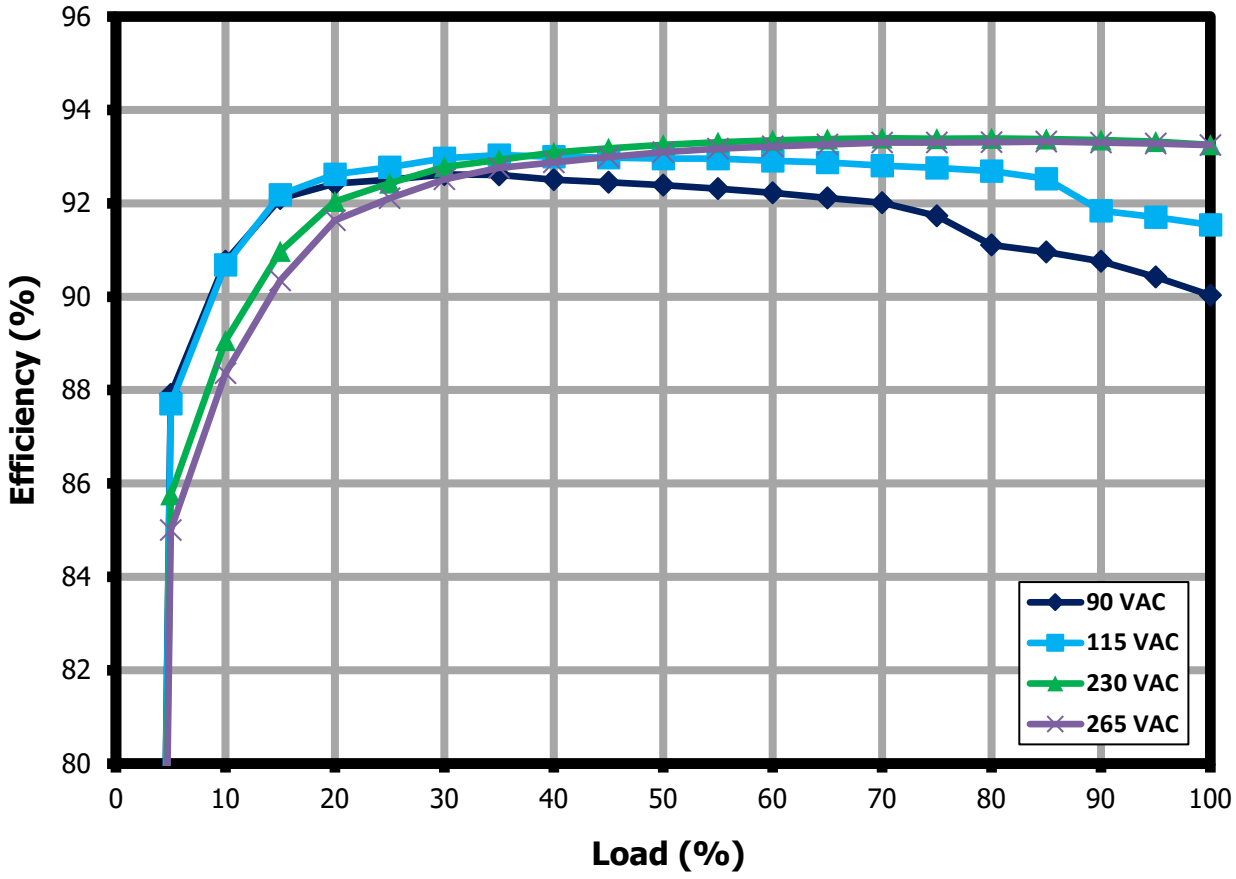


Figure 15 – Efficiency vs. Load, Room Ambient.

10.6 Agency test Limits for Average Efficiency

	Test	Average	Average	10% Load
Output Voltage (V)	Power [W]	DOE6 Limit (%)	CoC v5 Tier 2 (%)	CoC v5 Tier 2 (%)
12	100	88.0	89.0	79.0

10.7 Average and 10% Efficiency at 90 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	111	100	90.1	91.6
75	82.4	75.5	91.6	
50	54.7	50.5	92.3	
25	27.4	25.3	92.3	
10	11.1	10	90.1	

10.8 Average and 10% Efficiency at 115 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	110	101	91.8	92.5
75	81.6	75.6	92.6	
50	54.4	50.6	93	
25	27.3	25.3	92.7	
10	11.1	10	90.1	

10.9 Average and 10% Efficiency at 230 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	108	101	93.5	93.1
75	81.2	75.8	93.3	
50	54.3	50.6	93.2	
25	27.4	25.3	92.3	
10	11.3	10	88.5	

10.10 Average and 10% Efficiency at 265 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	108	101	93.5	92.9
75	81.3	75.8	93.2	
50	54.4	50.6	93	
25	27.5	25.3	92	
10	11.4	10	87.7	

10.11 No-Load Input Power

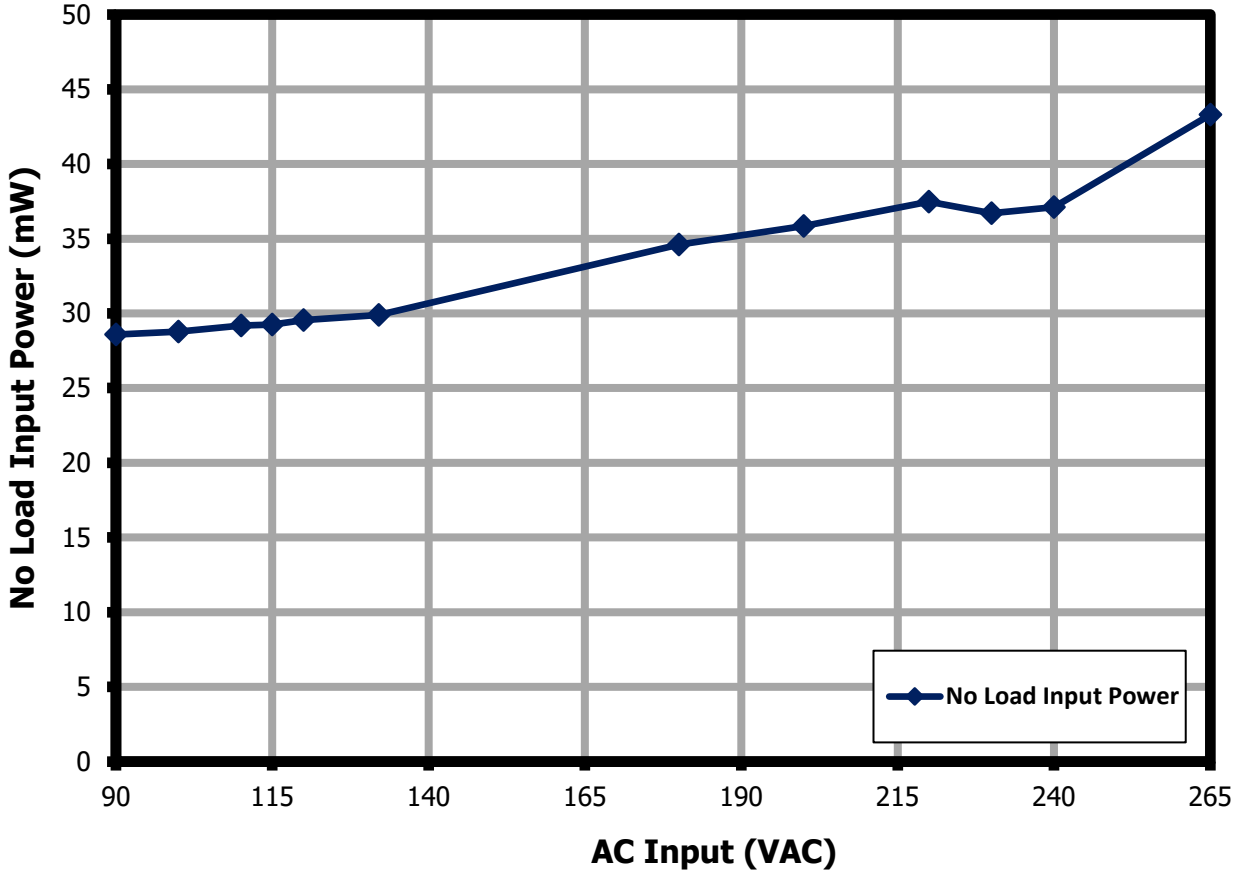


Figure 16 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.12 Line Regulation

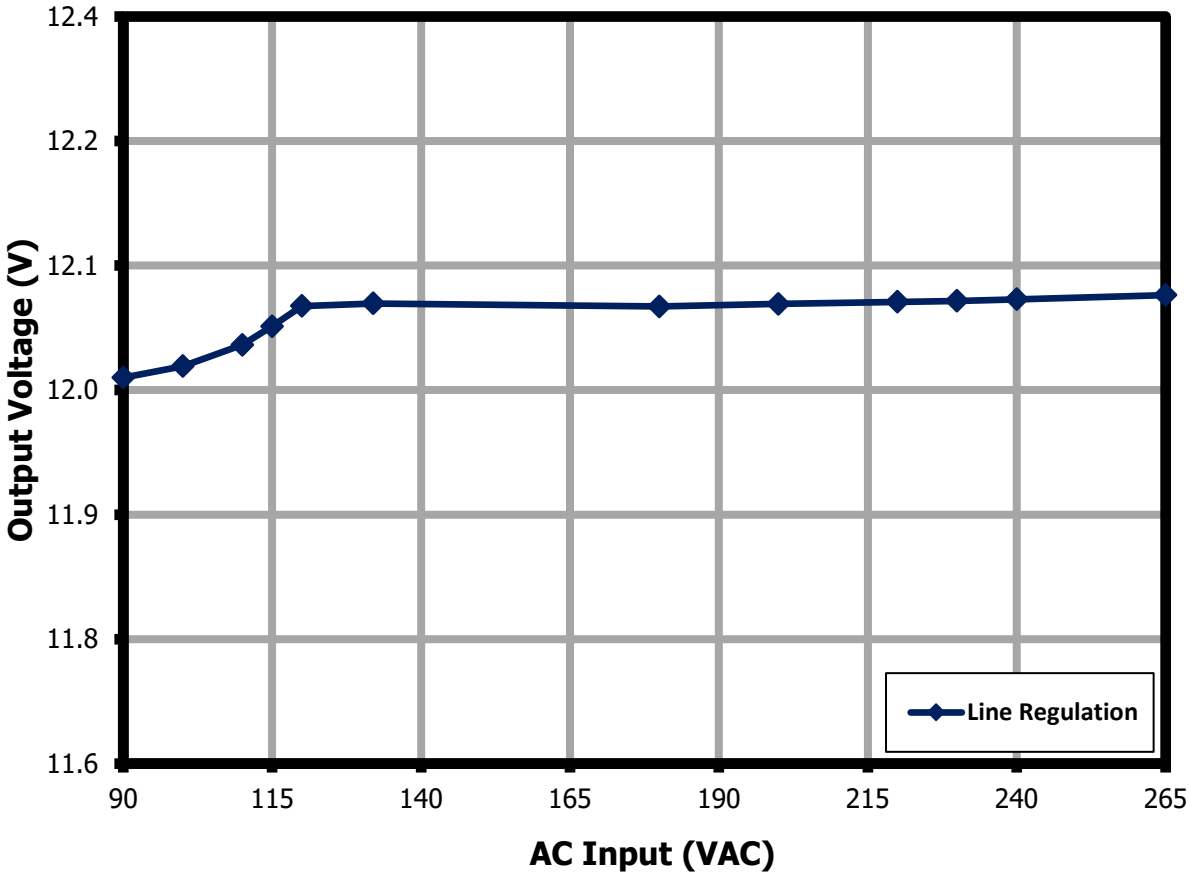


Figure 17 – Line Regulation.

10.13 Load Regulation

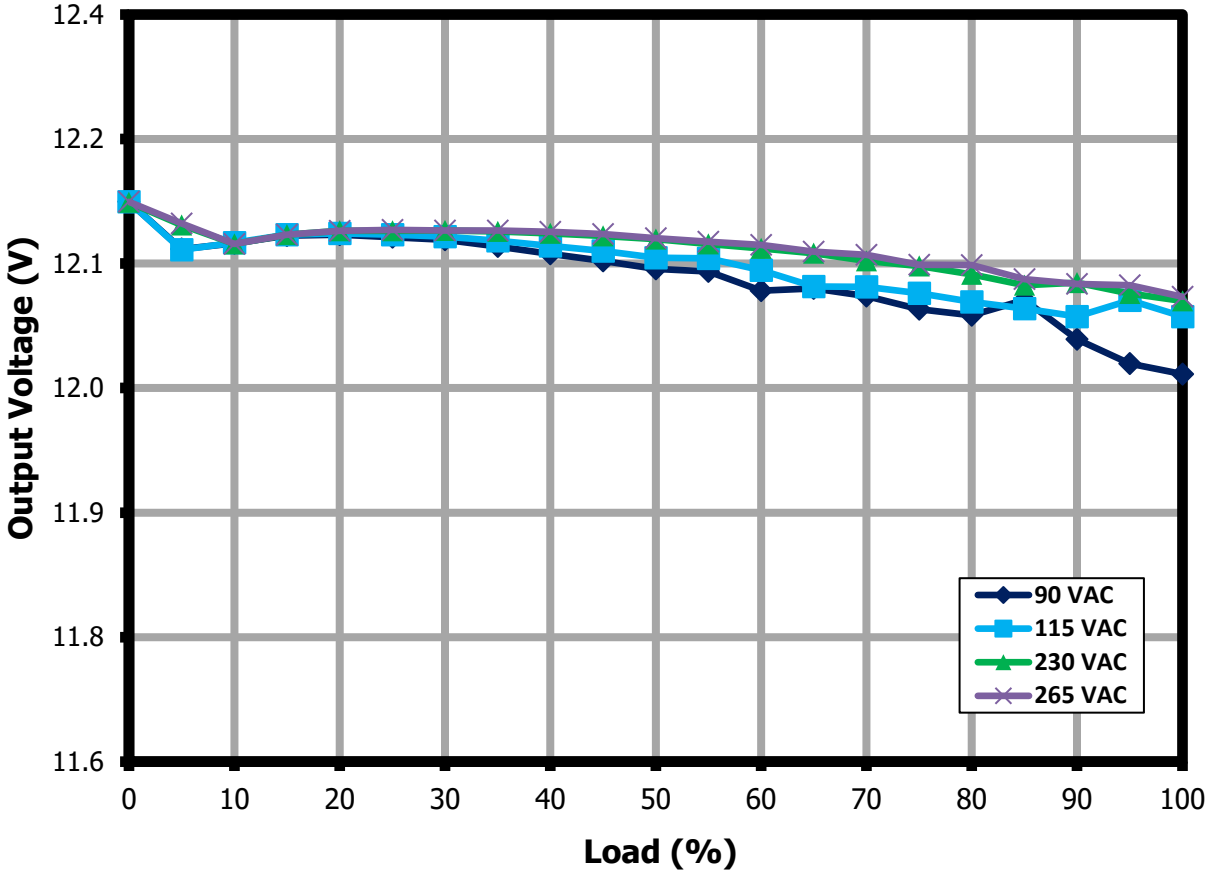


Figure 18 – Load Regulation.

10.14 Standby Efficiency

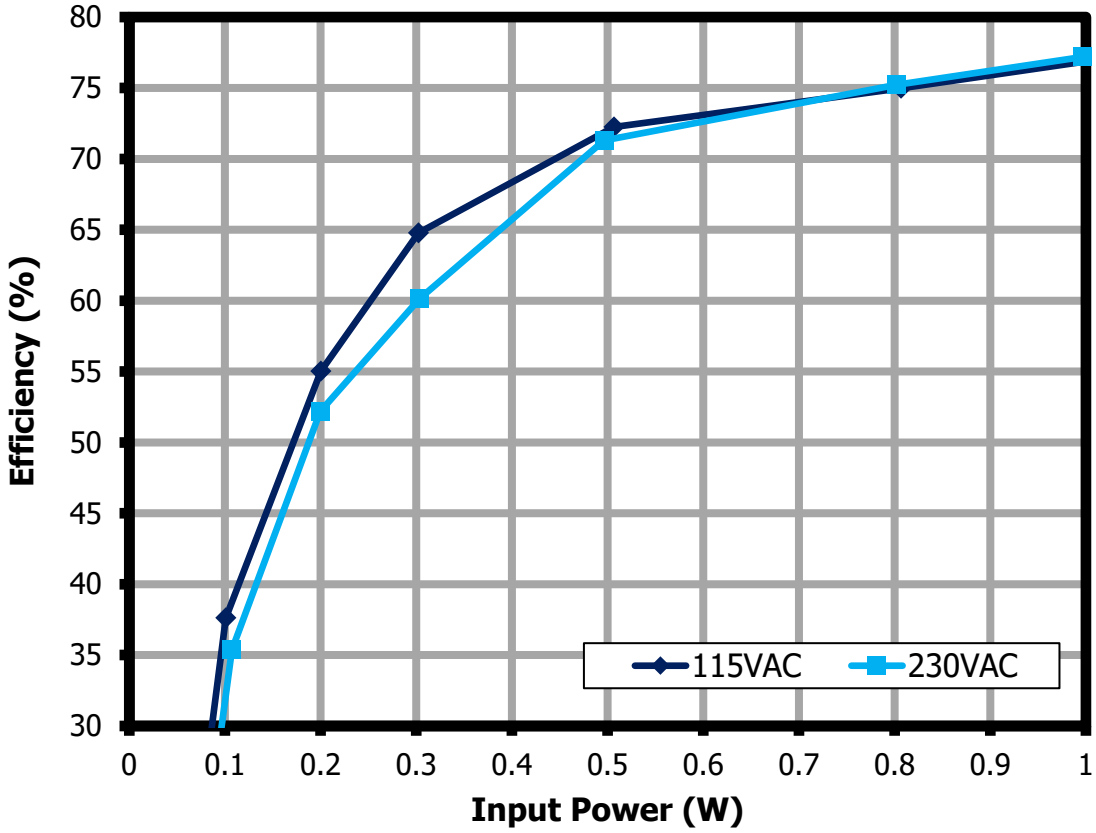


Figure 19 – Efficiency vs. Input Power.

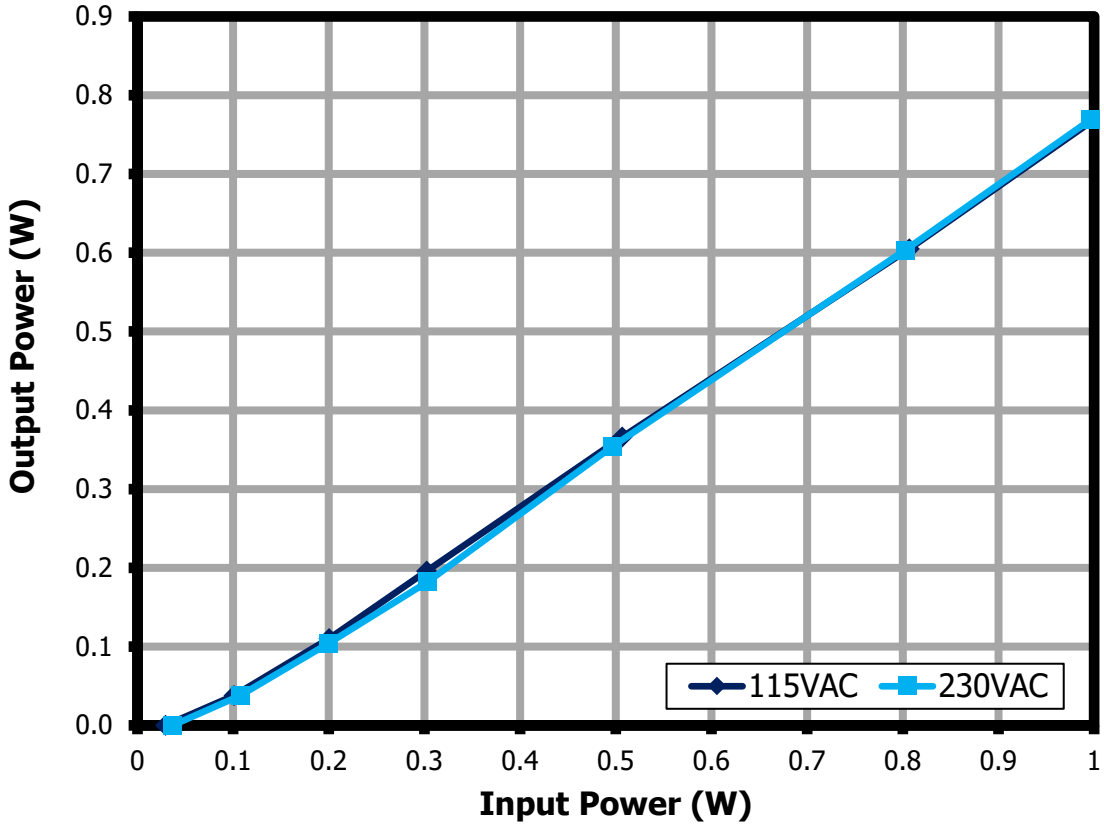


Figure 20 – Output Power vs. Input Power.

11 Thermal Performance

Thermal performance was measured using an IR camera with the unit inside an acrylic box. The unit was soaked for one hour at full load prior to measurements being made.

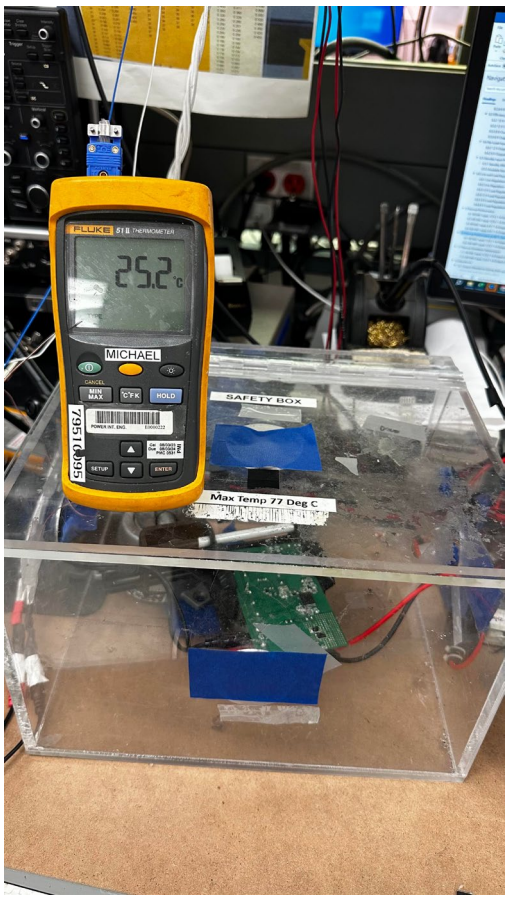


Figure 21 - Test Set-up.

11.1 90 VAC, 100 W at Room Temperature

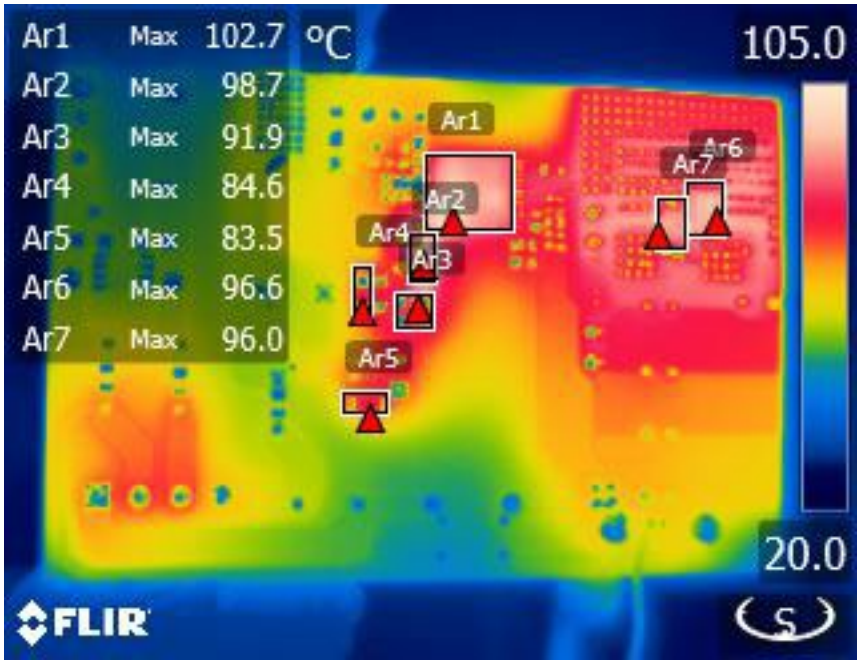


Figure 22 – Thermal Performance at 90 VAC Input (BOTTOM).

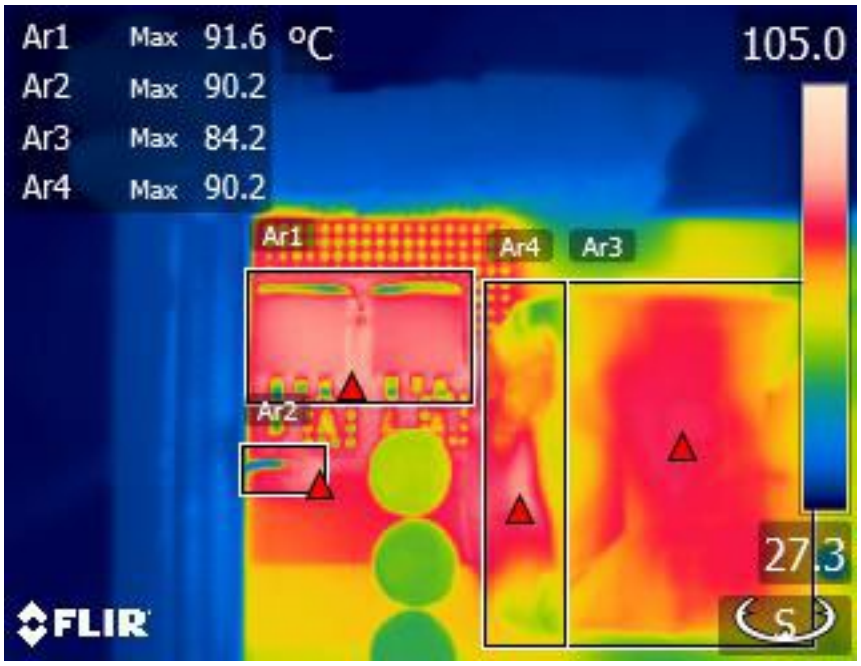


Figure 23 – Thermal Performance at 90 VAC Input (SR FET).

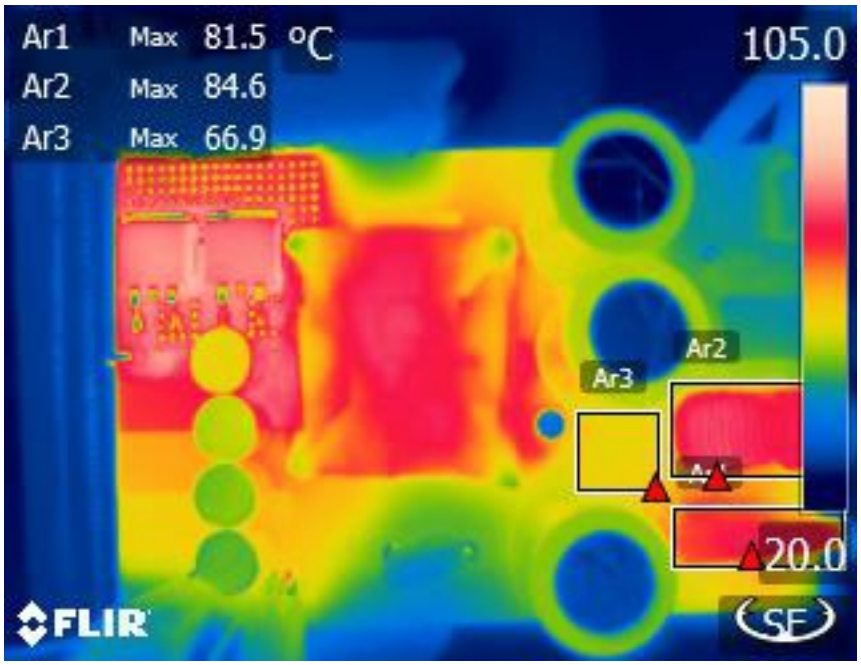


Figure 24 – Thermal Performance at 90 VAC Input (TOP).

Component	Actual Temperature (°C)	Temperature - Normalized to 25 °C Ambient (°C)
Ambient	32.9	25
INN4277C (U1)	103	95.1
Primary Snubber Diode (D1)	98.7	90.8
Primary Snubber Series Resistor (R4, R5)	91.9	84
Primary Snubber Resistor (R3)	84.6	76.7
Bias Diode (D2)	83.5	75.6
Schottky Diode (D3)	96.6	88.7
TVS Diode (VR1)	96	88.1
SRFET (Q1, Q2)	91.6	83.7
Secondary Snubber Resistor (R9)	90.2	82.3
TF Core (T1)	84.2	76.3
TF Winding (T1)	90.2	82.3
Bridge (BR1)	81.5	73.6
Common Mode Choke (L1)	84.6	76.7
Differential Inductor (L2)	66.9	59

11.2 265 VAC, 100 W at Room Temperature

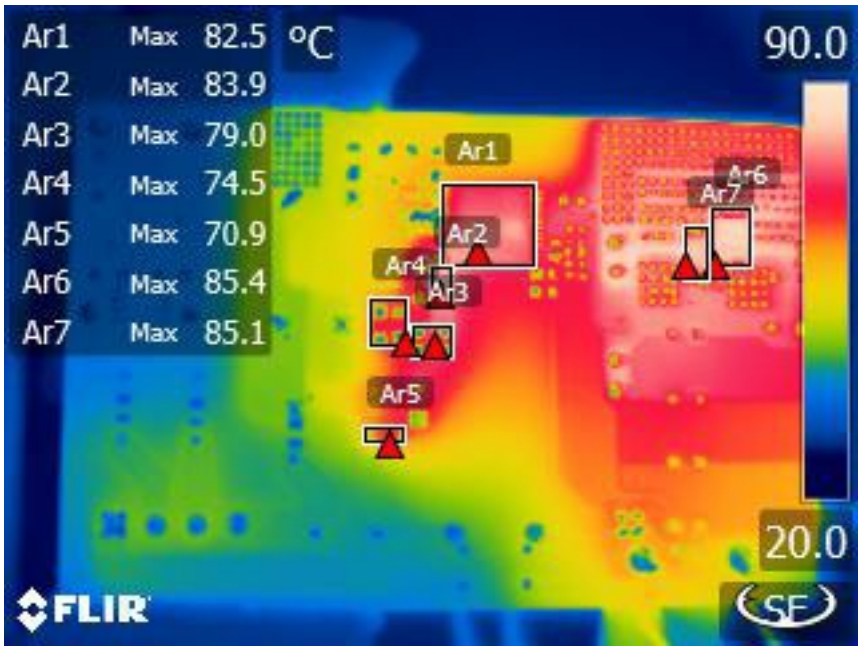


Figure 25 – Thermal Performance at 265 VAC Input (BOTTOM).

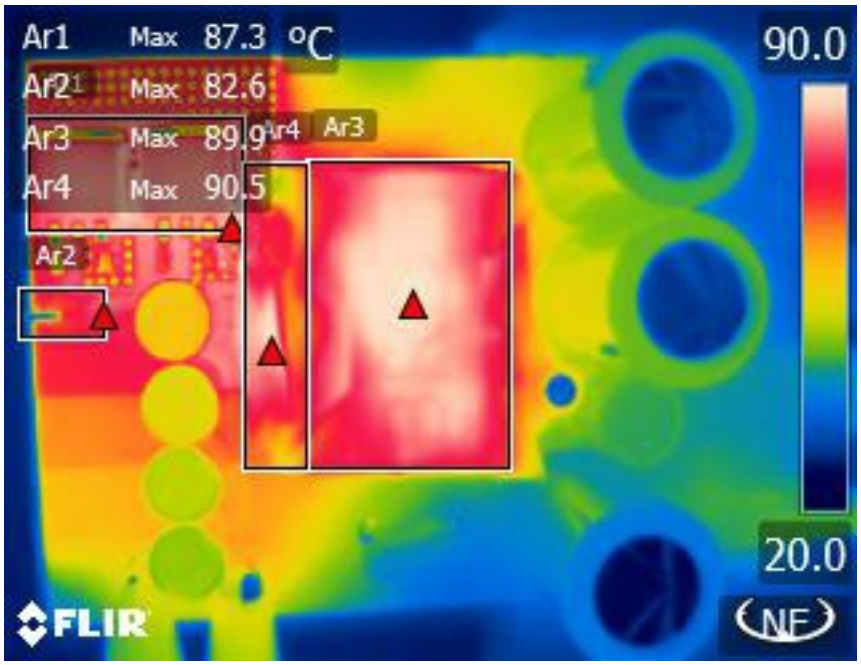


Figure 26 – Thermal Performance at 265 VAC Input (SR FET).

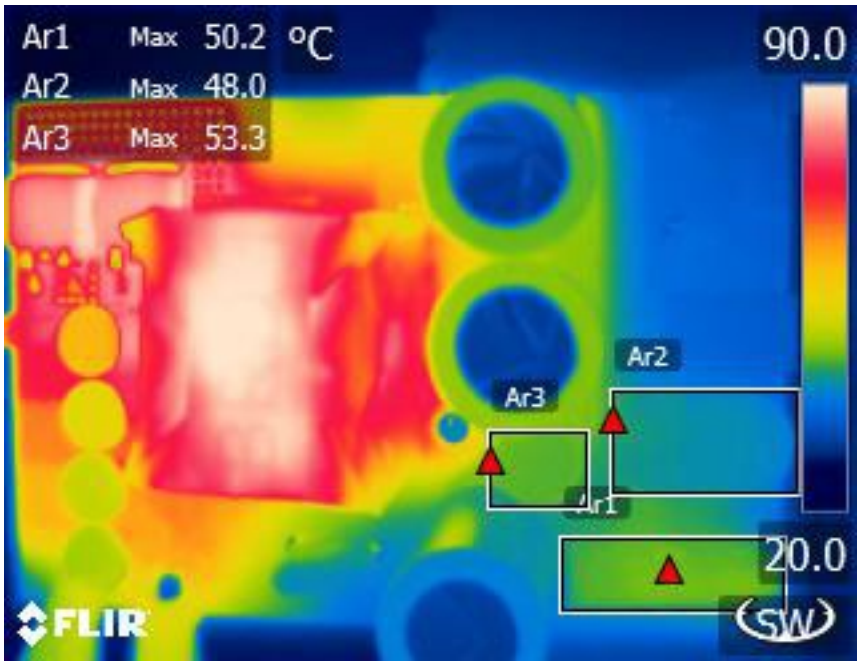


Figure 27 – Thermal Performance at 265 VAC Input (TOP).

Component	Actual Temperature (°C)	Temperature - Normalized to 25 °C Ambient (°C)
Ambient	30.1	25
INN4277C (U1)	82.5	77.4
Primary Snubber Diode (D1)	83.9	78.8
Primary Snubber Series Resistor (R4, R5)	79.0	73.9
Primary Snubber Resistor (R3)	74.5	69.4
Bias Diode (D2)	70.9	65.8
Schottky Diode (D3)	85.4	80.3
TVS Diode (VR1)	85.1	80
SRFET (Q1, Q2)	87.3	82.2
Secondary Snubber Resistor (R9)	82.6	77.5
TF Core (T1)	89.9	84.8
TF Winding (T1)	90.5	85.4
Bridge (BR1)	50.2	45.1
Common Mode Choke (L1)	48	42.9
Differential Inductor (L2)	53.3	48.2

12 Thermal Performance at 40 °C Ambient

Note: A thermal chamber was used to increase the ambient temperature to 40 °C. Unit is placed inside a box to prevent air flow and soaked at full load for one hour prior to measurements being made.

Figure 28 – Thermal Chamber Test Set-up.

12.1 90 VAC, 100 W, 40 °C Ambient

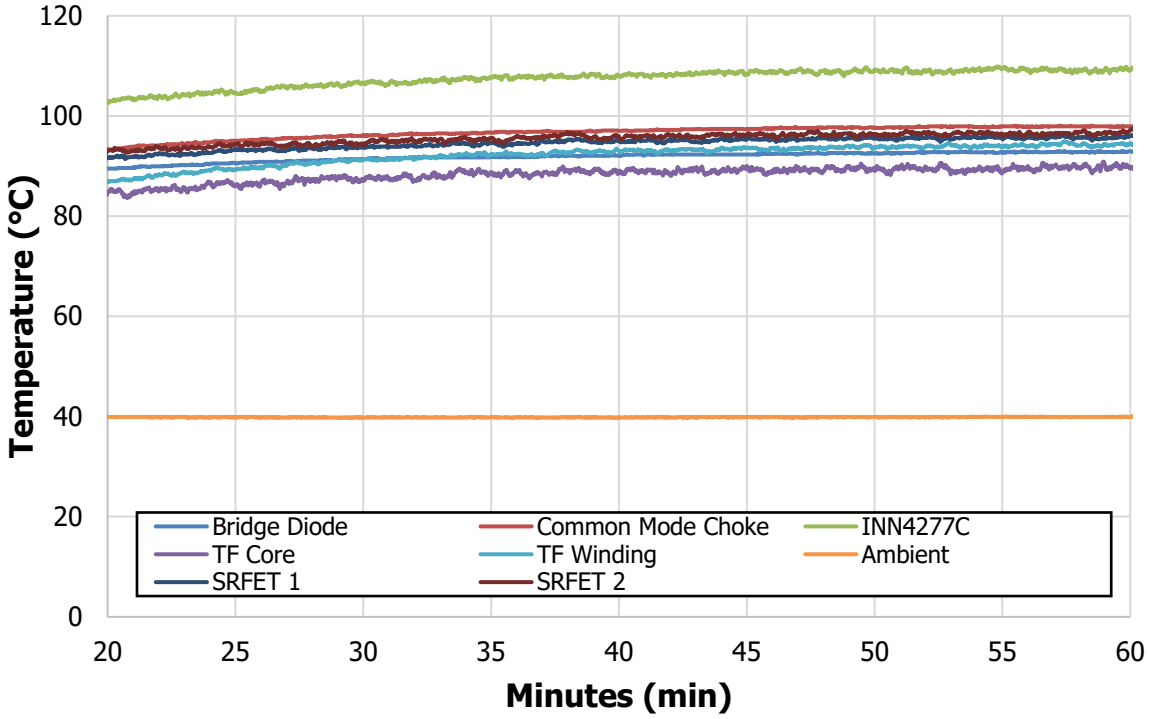


Figure 29 – Thermal Performance at 90 VAC Input.

Component	Max Temperature (°C)
INN4277C (U1)	110
Bridge Diode (BR1)	93
Common Mode Choke (L1)	98.1
Transformer Core (T1)	90.9
Transformer Winding (T1)	94.9
SRFET 1 (Q1)	96.3
SRFET 2 (Q2)	97.7
Ambient	40.4

12.2 265 VAC Input, 100 W, 40 °C Ambient

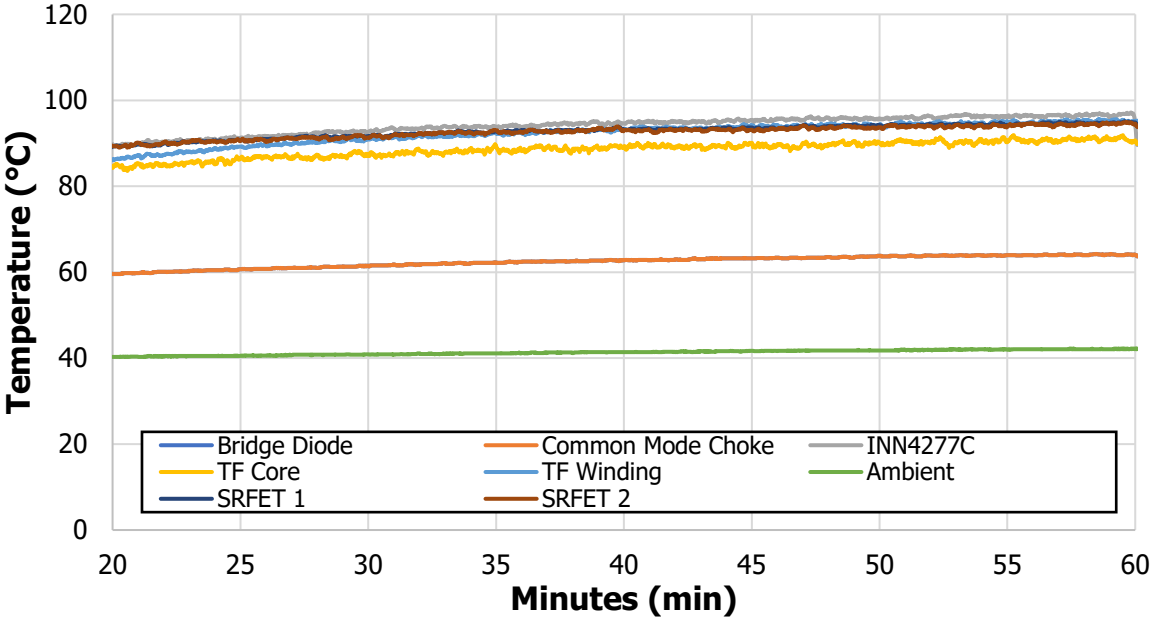


Figure 30 – Thermal Performance at 265 VAC Input.

Component	Max Temperature (°C)
INN4277C (U1)	97.2
Bridge Diode (BR1)	64.3
Common Mode Choke (L1)	61.9
Transformer Core (T1)	91.9
Transformer Winding (T1)	95.7
SRFET 1 (Q1)	95.2
SRFET 2 (Q2)	94.9
Ambient	42.2

13 Waveforms

13.1 Output Voltage Start-up Waveforms at Room Temperature

13.1.1 CC Load

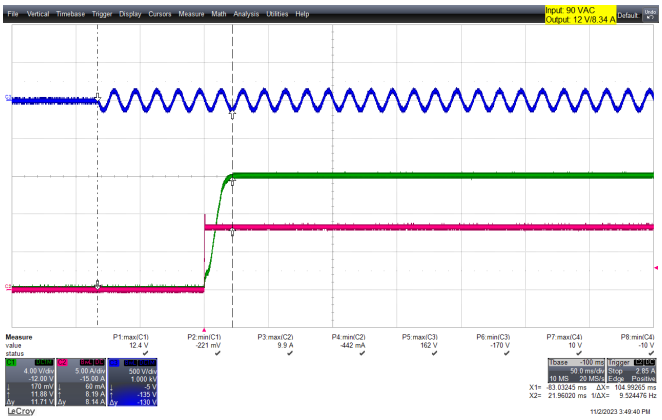


Figure 31 – 90 VAC 60 Hz, I_{OUT} = 8.34 A (Full-Load, CC)
CH1: Output Voltage: 4 V / div, 50 ms / div.
CH2: Output Current: 5 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Start-up Time = 105 ms.

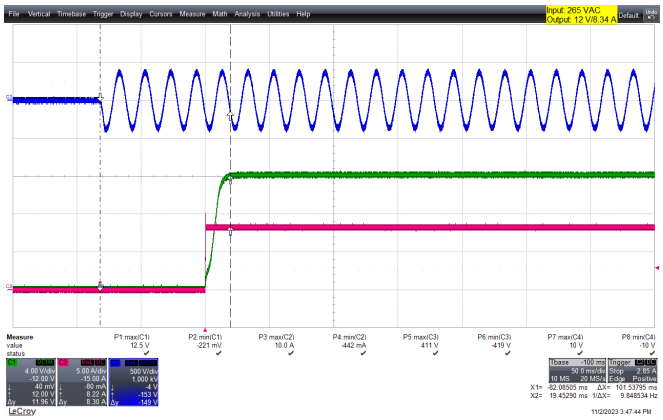


Figure 32 – 265 VAC 50 Hz, I_{OUT} = 8.34 A (Full-Load, CC)
CH1: Output Voltage: 4 V / div, 50 ms / div.
CH2: Output Current: 5 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Start-up Time = 102 ms.

13.1.2 CR Load

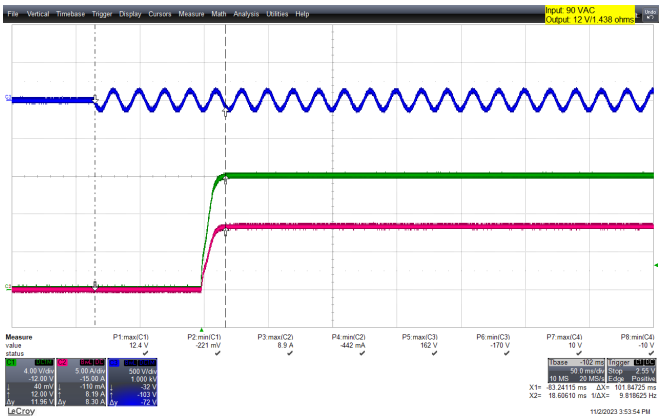


Figure 33 – 90 VAC 60 Hz, R_{load} = 1.44 Ω (Full-Load, CR).
CH1: Output Voltage: 4 V / div, 50 ms / div.
CH2: Output Current: 5 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Start-up Time = 102 ms.

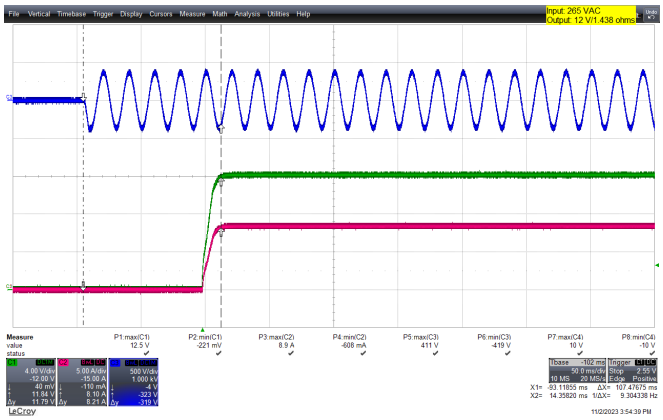


Figure 34 – 265 VAC 50 Hz, R_{load} = 1.44 Ω (Full-Load, CR).
CH1: Output Voltage: 4 V / div, 50 ms / div.
CH2: Output Current: 5 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Start-up Time = 107 ms.

13.1.3 No-Load

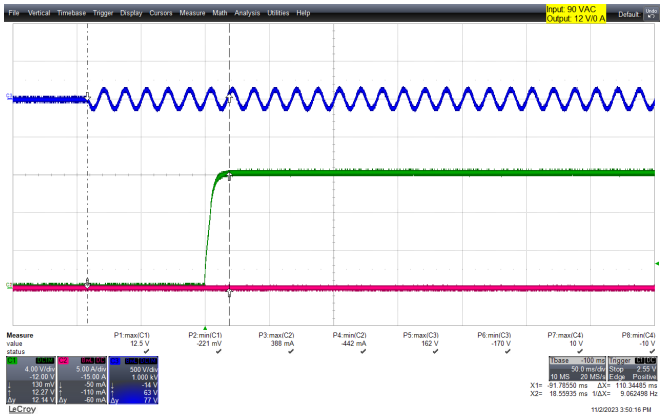


Figure 35 – 90 VAC 60 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 4 V / div, 50 ms / div.
CH2: Output Current: 5 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Start-up Time = 110 ms.

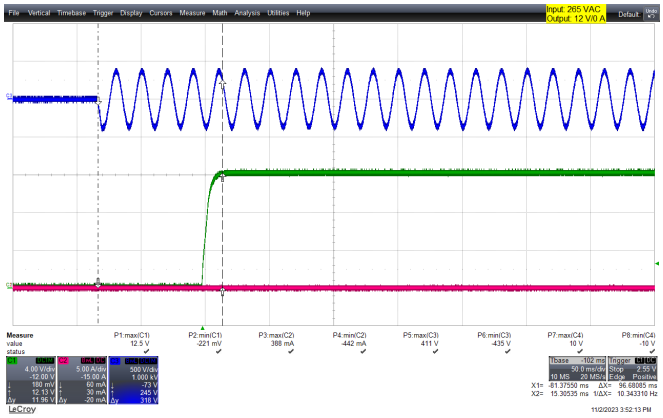


Figure 36 – 265 VAC 50 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 4 V / div, 50 ms / div.
CH2: Output Current: 5 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Start-up Time = 97 ms.

13.2 Output Voltage Start-up Waveforms at 40 °C Ambient

13.2.1 CC Load

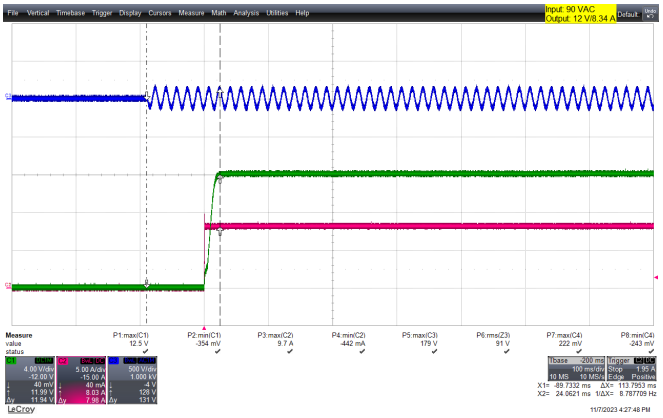


Figure 37 – 90 VAC 60 Hz, I_{OUT} = 8.34 A (Full-Load, CC)
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 114 ms.

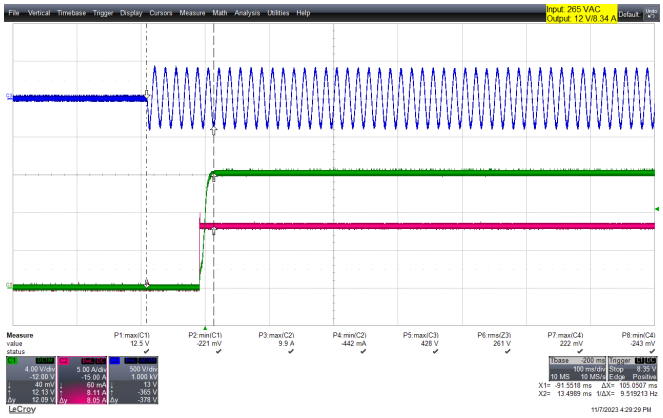


Figure 38 – 265 VAC 50 Hz, I_{OUT} = 8.34 A (Full-Load, CC)
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 105 ms.

13.2.2 CR Load

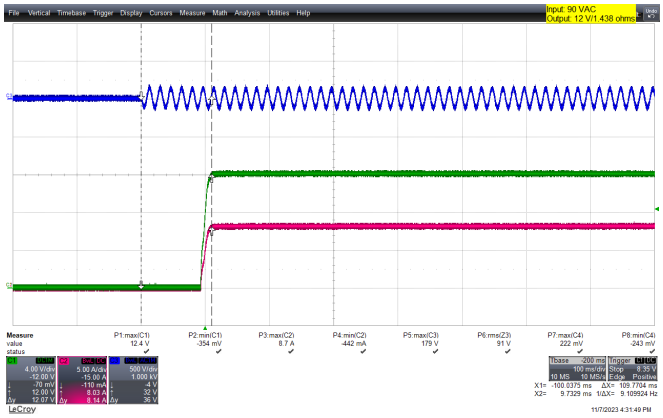


Figure 39 – 90 VAC 60 Hz, R_{load} = 1.44 Ω (Full-Load, CR).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 110 ms.

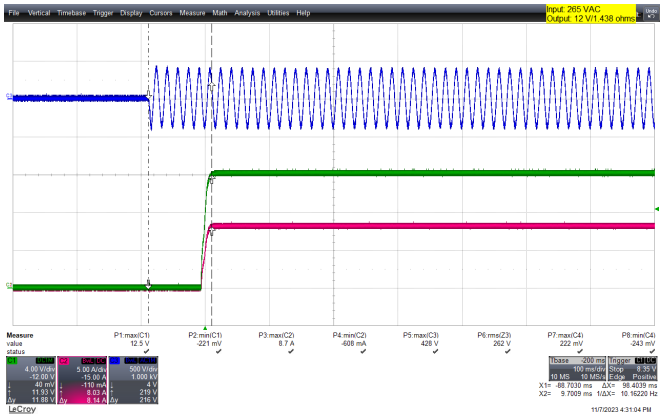


Figure 40 – 265 VAC 50 Hz, R_{load} = 1.44 Ω (Full-Load, CR).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 98 ms.

13.2.3 No-Load

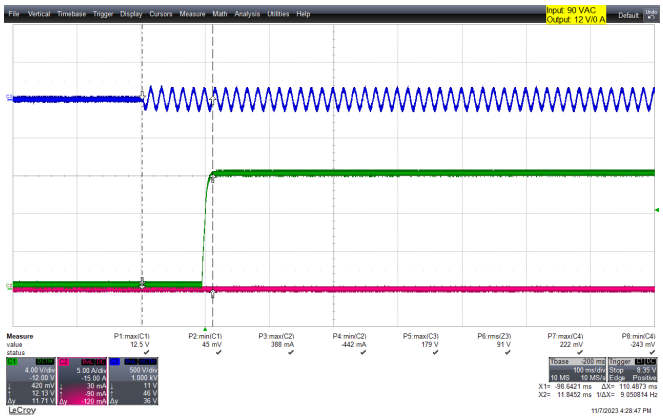


Figure 41 – 90 VAC 60 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 110 ms.

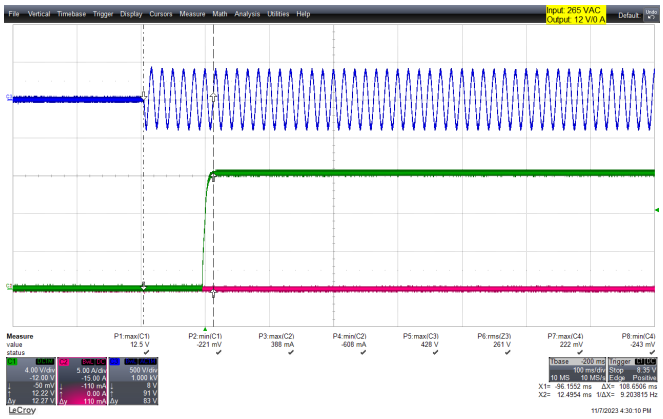


Figure 42 – 265 VAC 50 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 109 ms.

13.3 Output Voltage Start-up Waveforms at 0 °C Ambient

13.3.1 CC Load

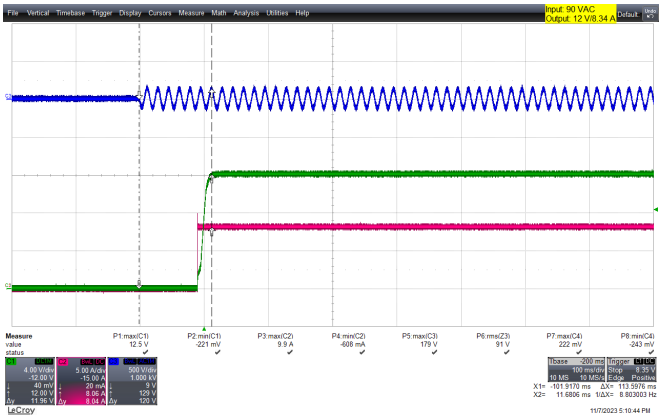


Figure 43 – 90 VAC 60 Hz, I_{OUT} = 8.34 A (Full-Load, CC)
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 114 ms.

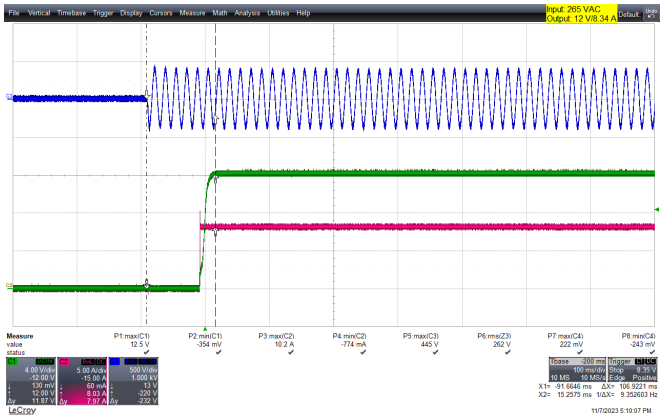


Figure 44 – 265 VAC 50 Hz, I_{OUT} = 8.34 A (Full-Load, CC)
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 107 ms.

13.3.2 CR Load

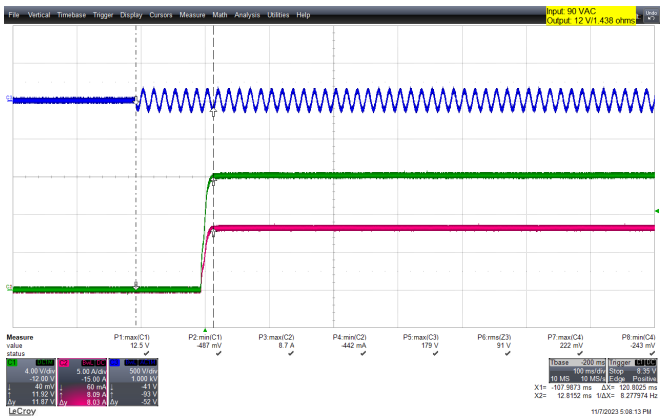


Figure 45 – 90 VAC 60 Hz, R_{load} = 1.44 Ω (Full-Load, CR).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 121 ms.

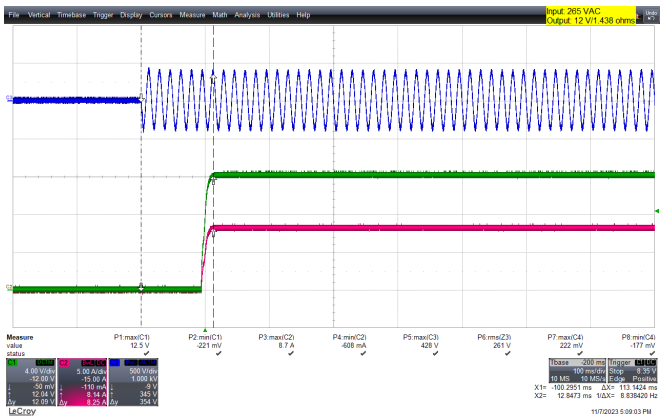


Figure 46 – 265 VAC 50 Hz, R_{load} = 1.44 Ω (Full-Load, CR).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 113 ms.

13.3.3 No-Load

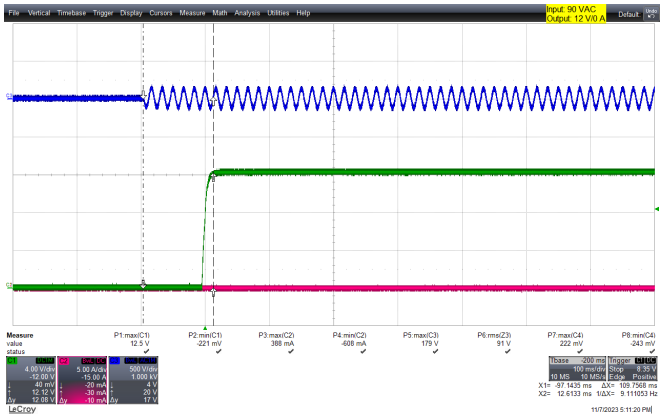


Figure 47 – 90 VAC 60 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 110 ms.

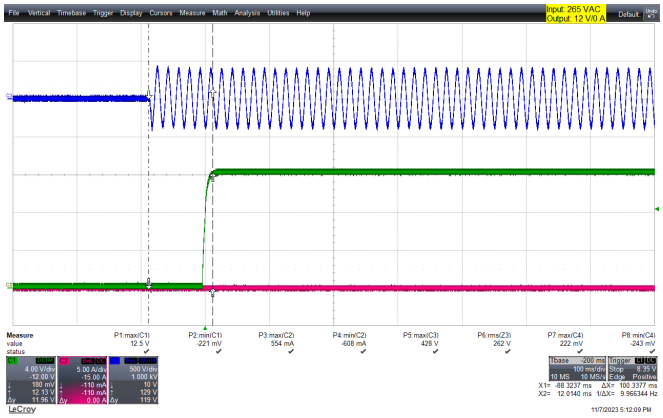


Figure 48 – 265 VAC 50 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 4 V / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
CH3: Input Voltage: 500 V / div, 100 ms / div.
Start-up Time = 100 ms.

13.4 Load Transient Response (Measured on the Board)

13.4.1 0 – 100% Load Step

Set-up: Dynamic load using Chroma 63103A. Dynamic load was set at 8.34 A for 100 ms and 0 A for 100 ms. Load current slew rate was 2.5 A / µs.

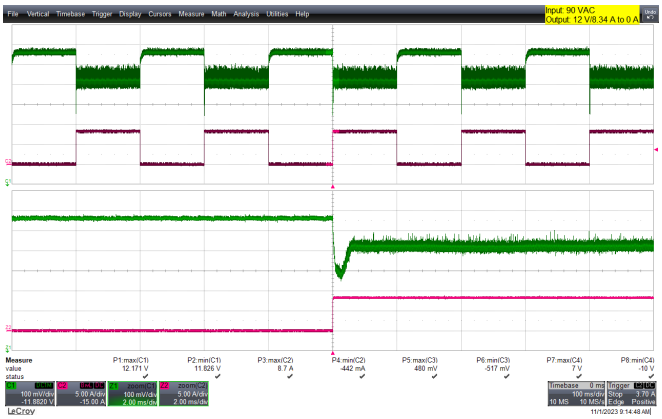


Figure 49 – 90 VAC 60 Hz. I_{OUT} = 0 A – 8.34 A (0 - 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.2 V.
V_{OUT_MIN}: 11.8 V.

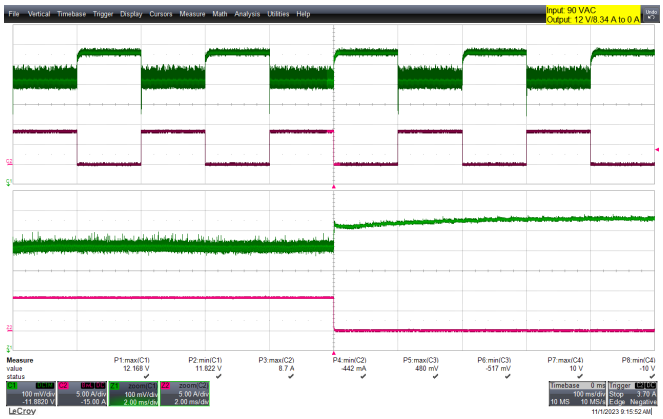


Figure 50 – 90 VAC 60 Hz. I_{OUT} = 8.34 A – 0 A (100 - 0%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.2 V.
V_{OUT_MIN}: 11.8 V.

Figure 51 – 265 VAC 50 Hz. I_{OUT} = 0 A – 8.34 A (0 - 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.2 V.
V_{OUT_MIN}: 11.8 V.

Figure 52 – 265 VAC 50 Hz. I_{OUT} = 8.34 A – 0 A (100 - 0%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.2 V.
V_{OUT_MIN}: 11.8 V.

13.4.2 50 – 100% Load Step

Set-up: Dynamic load using Chroma 63103A. Dynamic load was set at 8.34 A for 100 ms and 4.17 A for 100 ms. Load current slew rate was 2.5 A / µs.

Figure 53 – 90 VAC 60 Hz. I_{OUT} = 4.17 A – 8.34 A (50 - 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.1 V.
V_{OUT_MIN}: 11.9 V.

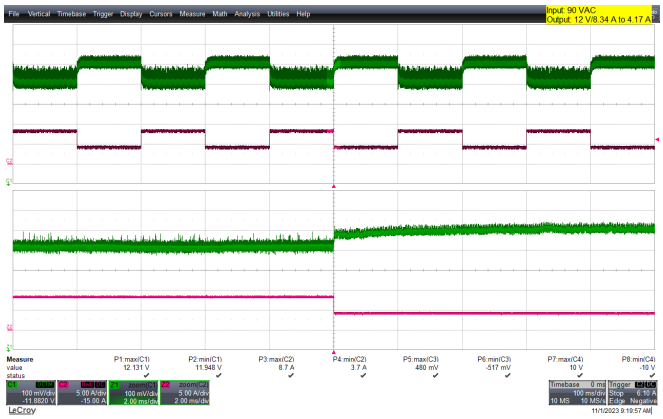


Figure 54 – 90 VAC 60 Hz. I_{OUT} = 8.34 A – 4.17 A (100 - 50%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.1 V.
V_{OUT_MIN}: 11.9 V.

Figure 55 – 265 VAC 50 Hz. I_{OUT} = 4.17 A – 8.34 A (50 - 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.2 V.
V_{OUT_MIN}: 12 V.

Figure 56 – 265 VAC 50 Hz. I_{OUT} = 8.34 A – 4.17 A (100 - 50%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 2 ms / div.
V_{OUT_MAX}: 12.1 V.
V_{OUT_MIN}: 12 V.

13.5 Switching Waveforms

13.5.1 Drain Voltage and Current at Start-up Operation

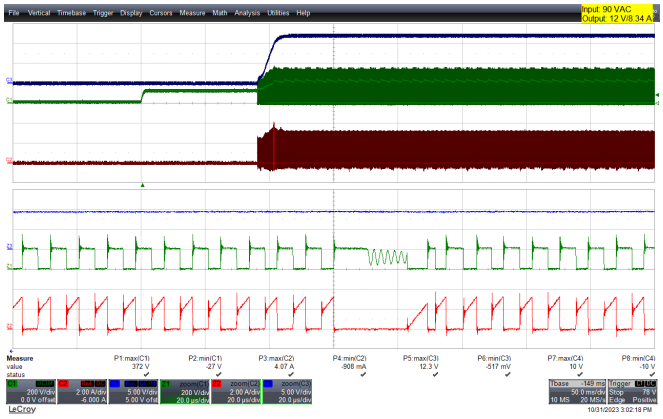


Figure 57 – 90 VAC, I_{OUT} = 8.34 A (Full-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 5 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 372 V.
Drain current, Max. = 4.07 A.

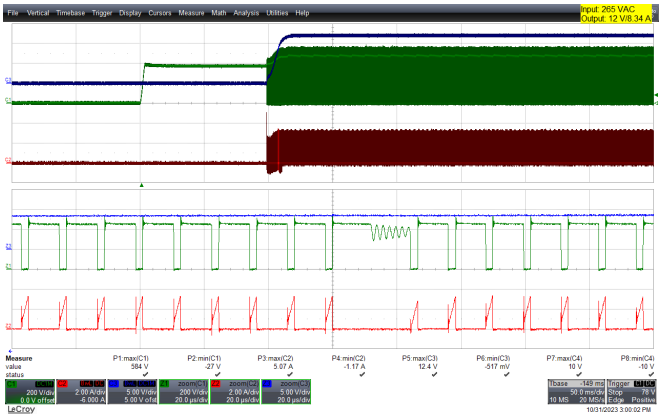


Figure 58 – 265 VAC, I_{OUT} = 8.34 A (Full-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 5 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 584 V.
Drain current, Max. = 5.07 A.

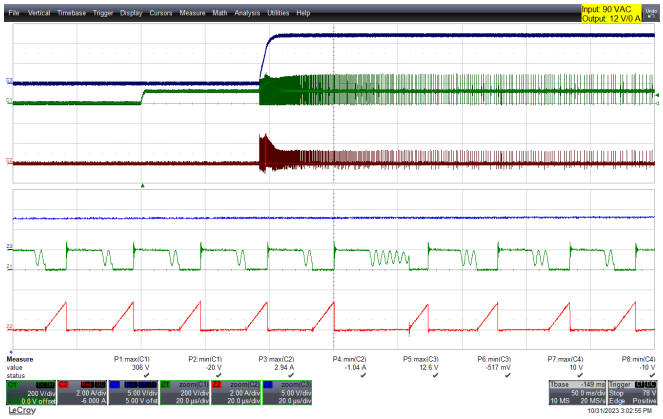


Figure 59 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 5 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 306 V.
Drain current, Max. = 2.94 A.

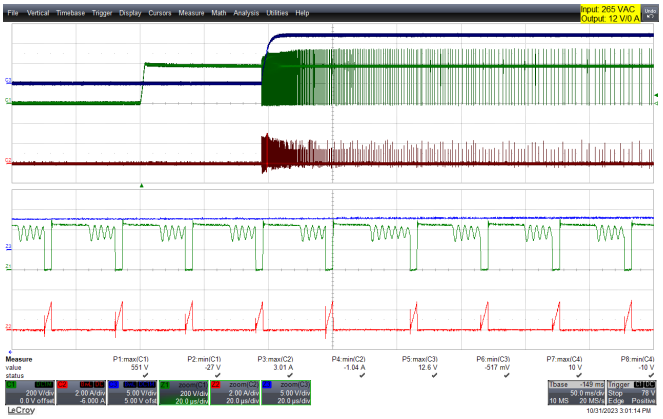


Figure 60 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 5 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 551 V.
Drain current, Max. = 3.01 A.

13.5.2 Drain Voltage and Current at Normal Operation

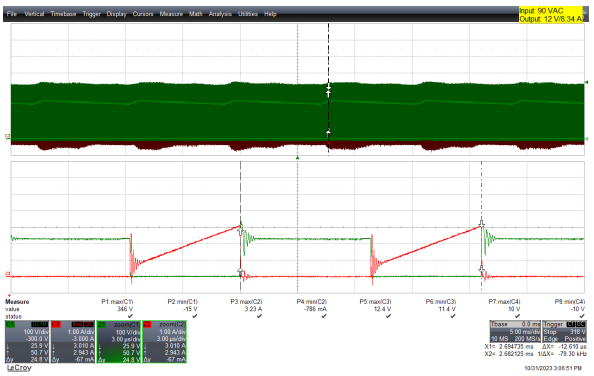


Figure 61 – 90 VAC, I_{OUT} = 8.34 A (Full-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 3 µs / div.
Drain voltage, Max. = 346 V.
Drain current, Max. = 3.23 A.

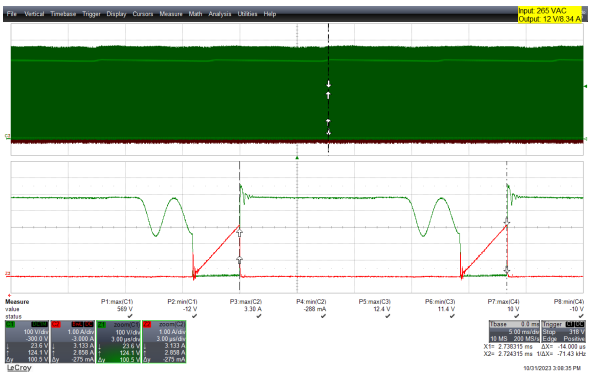


Figure 62 – 265 VAC, I_{OUT} = 8.34 A (Full-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 3 µs / div.
Drain voltage, Max. = 569 V.
Drain current, Max. = 3.3 A.

Figure 63 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 3 µs / div.
Drain voltage, Max. = 287 V.
Drain current, Max. = 1.27 A.

Figure 64 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 3 µs / div.
Drain voltage, Max. = 546 V.
Drain current, Max. = 2.27 A.

13.5.3 Drain Voltage and Current at Output Short Condition

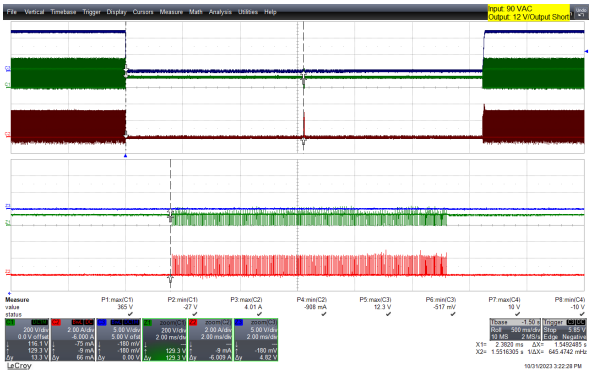


Figure 65 – 90 VAC, I_{OUT} = Output Shorted.
CH1: Drain Voltage: 200 V / div, 500 ms / div.
CH2: Drain Current: 2 A / div, 500 ms / div.
Zoom: 2 ms / div.
Drain voltage, Max. = 365 V.
Drain current, Max. = 4.01 A.

Figure 66 – 265 VAC, I_{OUT} = Output Shorted.
CH1: Drain Voltage: 200 V / div, 500 ms / div.
CH2: Drain Current: 2 A / div, 500 ms / div.
Zoom: 2 ms / div.
Drain voltage, Max. = 578 V.
Drain current, Max. = 5.00 A.

13.5.4 SR FET Voltage at Start-up

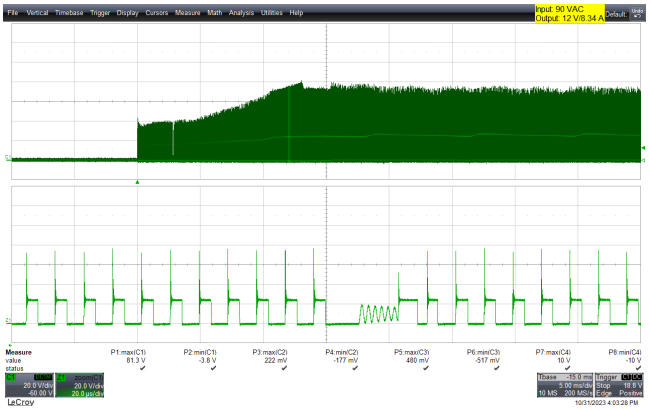


Figure 67 – 90 VAC, I_{OUT} = 8.34 A (Full-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 20 µs.
SR FET Drain Voltage, Max. = 81.3 V.

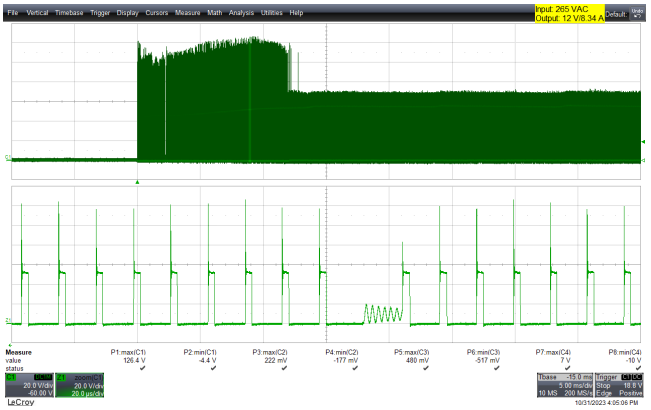


Figure 68 – 265 VAC, I_{OUT} = 8.34 A (Full-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 20 µs.
SR FET Drain Voltage, Max. = 126 V.

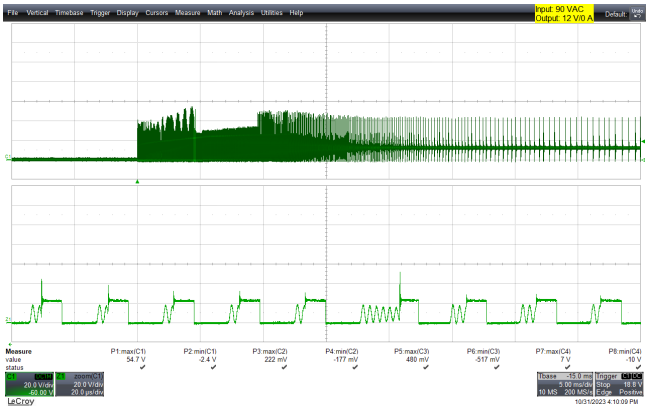


Figure 69 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 20 µs.
SR FET Drain Voltage, Max. = 54.7 V.

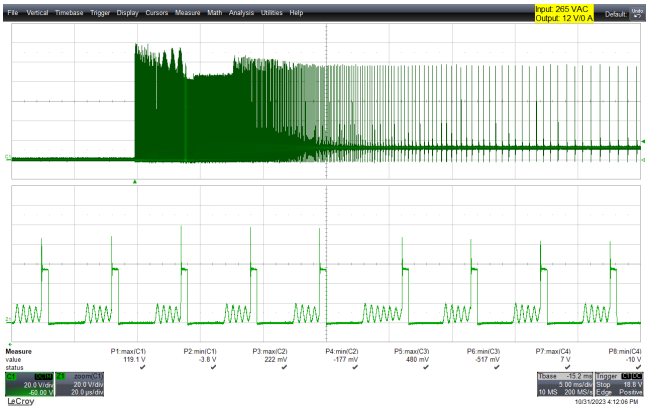


Figure 70 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 20 µs.
SR FET Drain Voltage, Max. = 119 V.

13.5.5 SR FET Voltage at Normal Operation

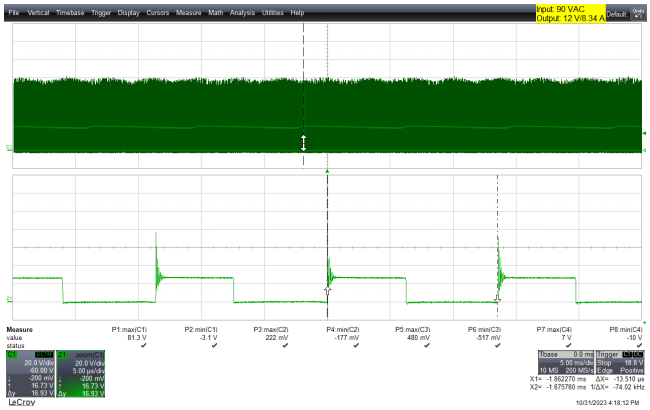


Figure 71 – 90 VAC, I_{OUT} = 8.34 A (Full-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 5 µs.
SR FET Drain Voltage, Max. = 81.3 V.

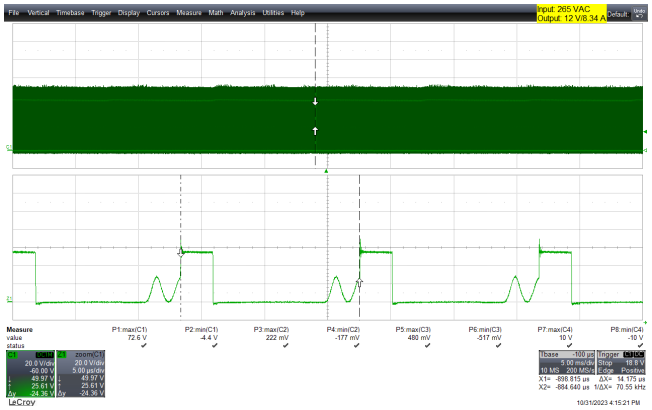


Figure 72 – 265 VAC, I_{OUT} = 8.34 A (Full-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 5 µs.
SR FET Drain Voltage, Max. = 72.6 V.

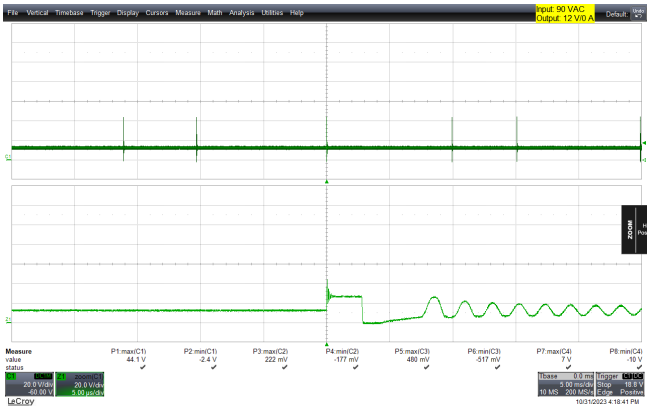


Figure 73 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 5 µs.
SR FET Drain Voltage, Max. = 44.1 V.

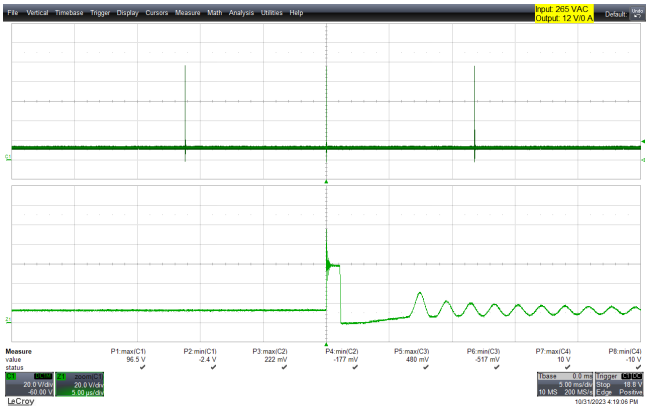


Figure 74 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 5 µs.
SR FET Drain Voltage, Max. = 96.5 V.

13.5.6 SR FET Voltage at Output Short Condition

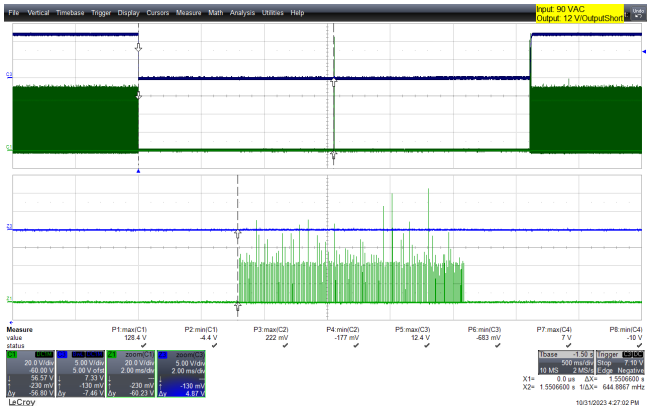


Figure 75 – 90 VAC, I_{OUT} = Output Shorted.
CH2: SR FET Drain Voltage: 20 V / div, 500 ms / div.
CH3: Output Voltage: 5 V / div, 500 ms /div.
Zoom: 2 ms.
AR_OFF: 1.55 s

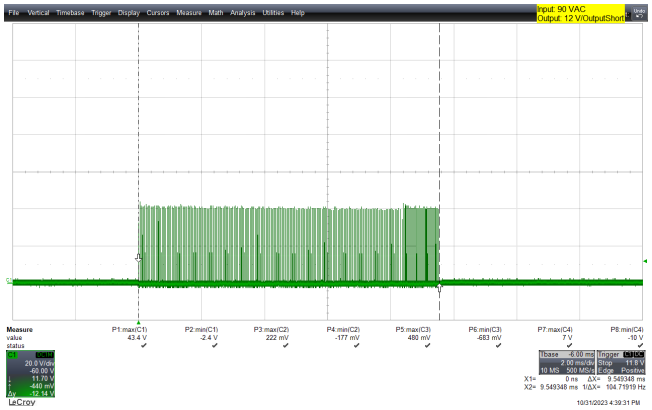


Figure 76 – 90 VAC, I_{OUT} = Output Shorted (Zoomed).
CH2: SR FET Drain Voltage: 20 V / div, 2 ms / div.
SR FET Drain Voltage, Max. = 43.4 V.

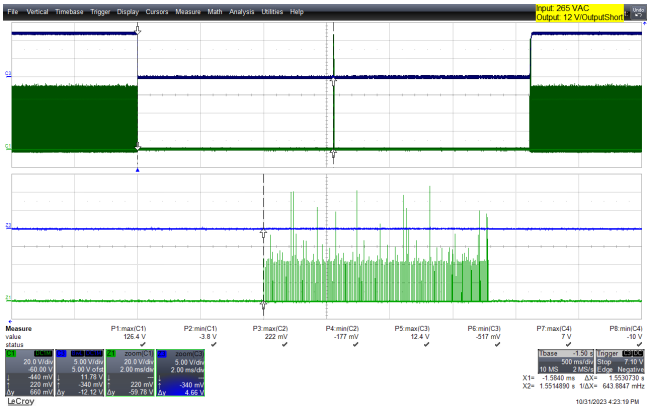


Figure 77 – 90 VAC, I_{OUT} = Output Shorted.
CH2: SR FET Drain Voltage: 20 V / div, 500 ms / div.
CH3: Output Voltage: 5 V / div, 500 ms /div.
Zoom: 2 ms.
AR_OFF: 1.55 s

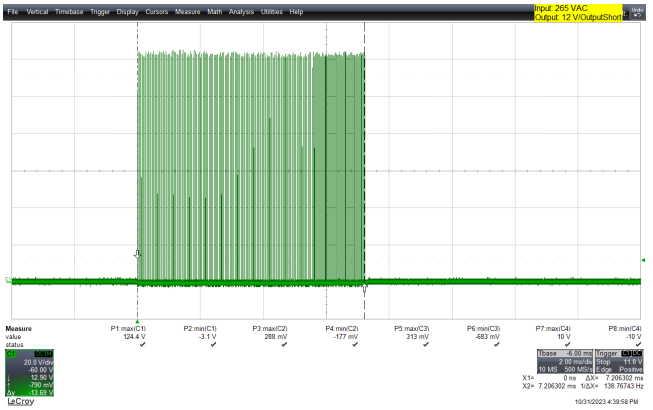


Figure 78 – 265 VAC, I_{OUT} = Output Shorted (Zoomed).
CH 2: SR FET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 5 µs.
SR FET Drain Voltage, Max. = 124 V.

13.6 Output Ripple Measurements

13.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in figure 88 and 89.

The PP026 probe adapter was modified by having two capacitors connected in parallel mounted across the probe tip. The capacitors were a 0.1 μF/50 V ceramic type and a 47 μF/50 V aluminum electrolytic type. The aluminum electrolytic capacitor is polarized, so proper polarity across DC outputs must be maintained as shown in figure 88 and 89.

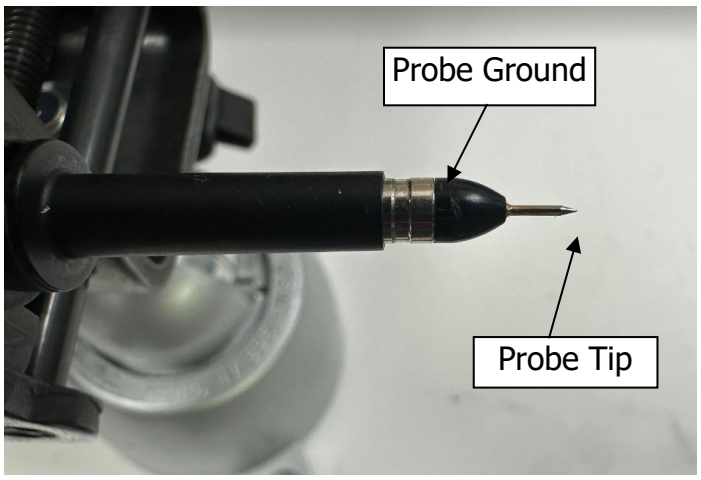


Figure 79 – Oscilloscope Probe Prepared for Ripple Measurement.

(End Cap and Ground Lead Removed)

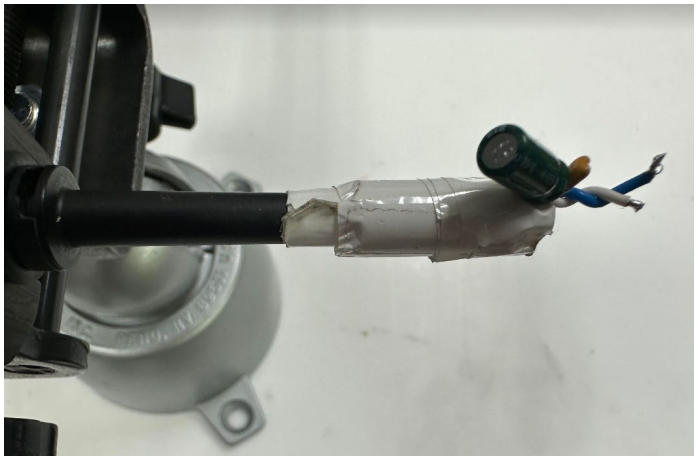


Figure 80 – Oscilloscope Probe with BNC Adapter.

(https://www.teledynelecroy.com/probes/passive-probes/pp026-1)

13.6.2 Ripple Waveforms (Measured on Board)

13.6.2.1 100% Load

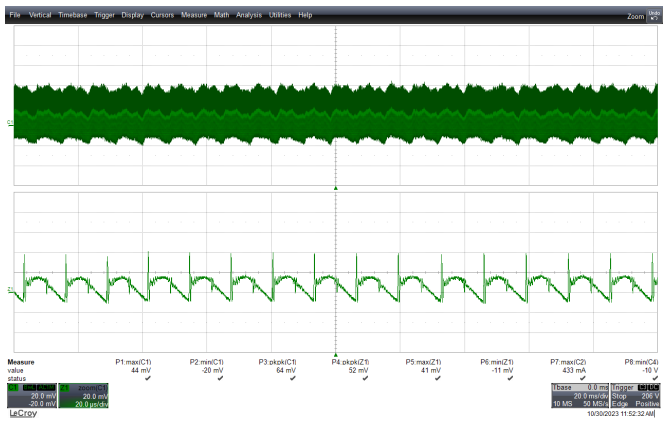


Figure 81 – Output Ripple. (PK-PK – 64 mV).
90 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

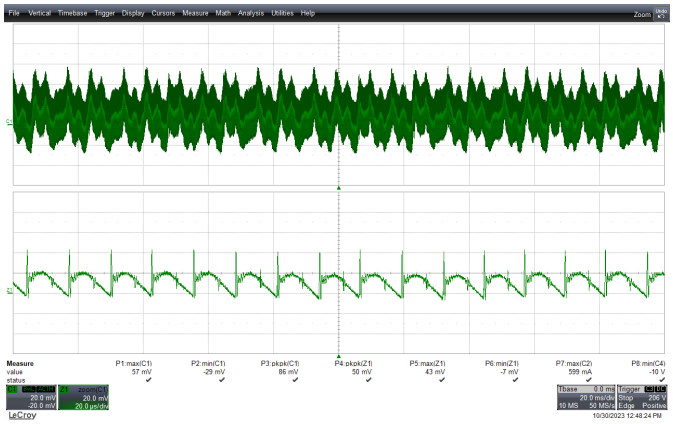


Figure 82 – Output Ripple. (PK-PK – 86 mV).
115 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

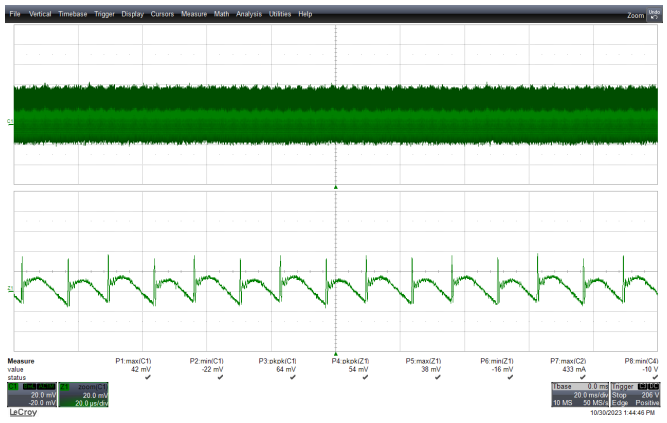


Figure 83 – Output Ripple. (PK-PK – 64 mV).
230 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

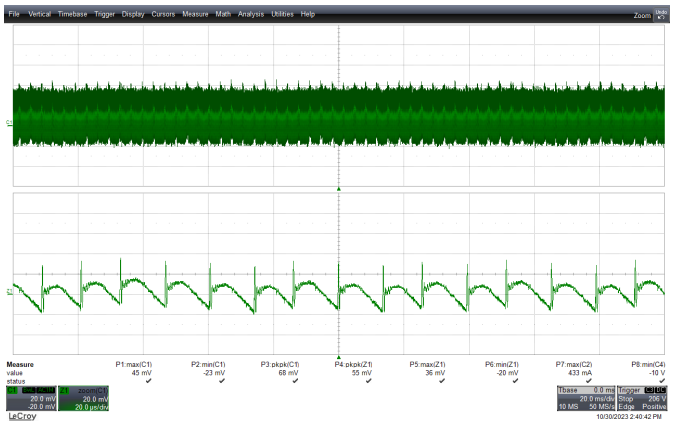


Figure 84 – Output Ripple. (PK-PK – 68 mV).
265 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

13.6.2.2 75% Load

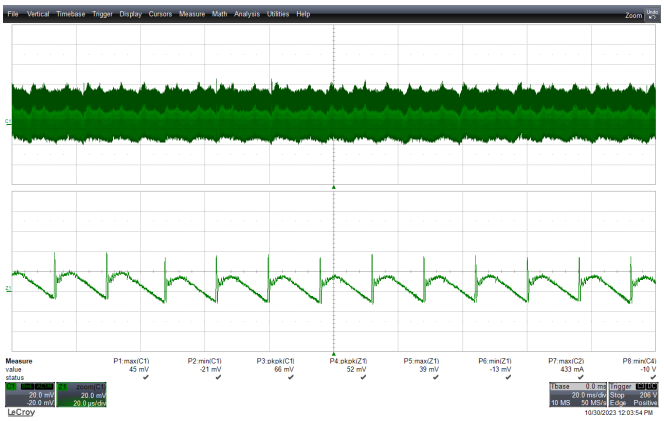


Figure 85 – Output Ripple. (PK-PK – 66 mV).
90 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

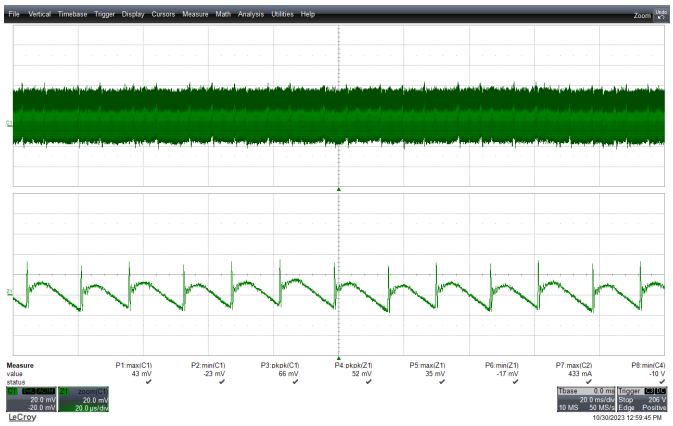


Figure 86 – Output Ripple. (PK-PK – 66 mV).
115 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

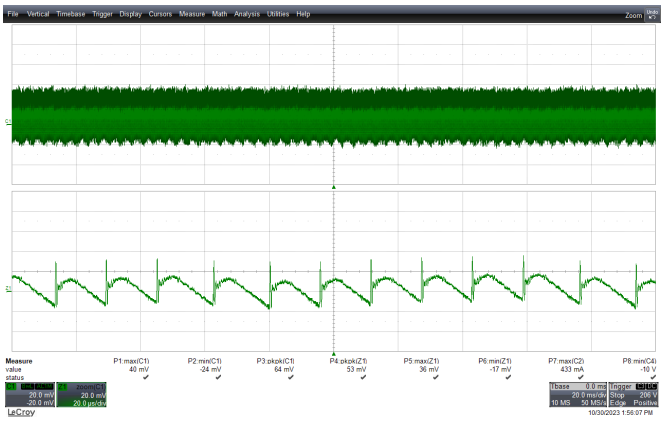


Figure 87 – Output Ripple. (PK-PK – 64 mV).
230 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

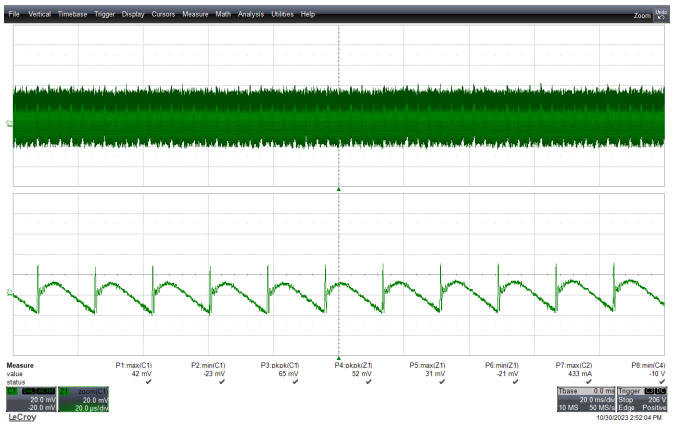


Figure 88 – Output Ripple. (PK-PK – 65 mV).
265 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

13.6.2.3 50% Load

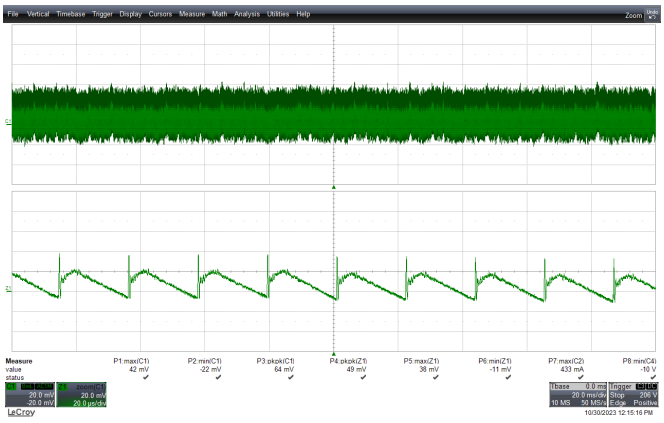


Figure 89 – Output Ripple. (PK-PK – 64 mV).
90 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

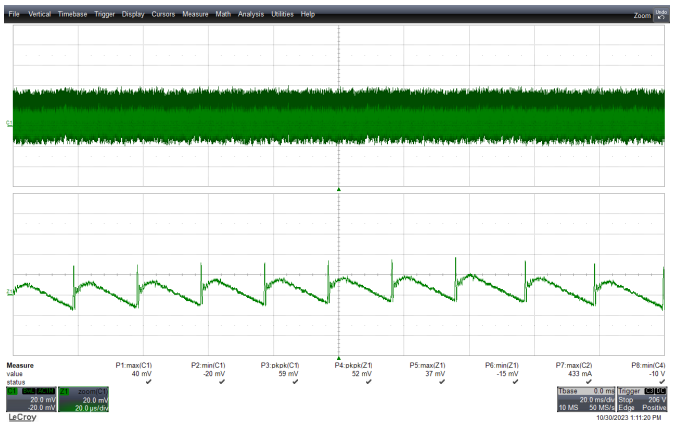


Figure 90 – Output Ripple. (PK-PK – 59 mV).
115 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

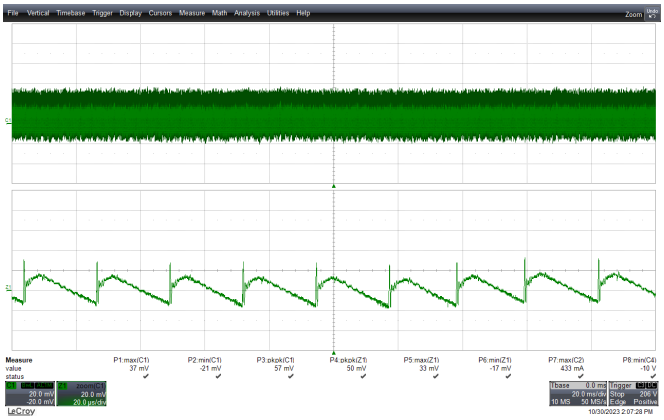


Figure 91 – Output Ripple. (PK-PK – 57 mV).
230 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

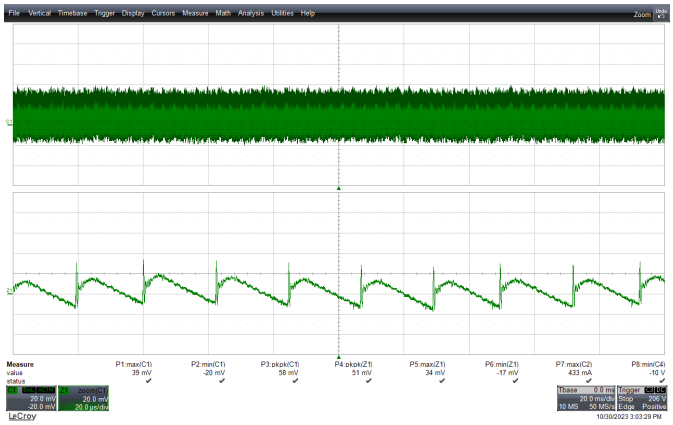


Figure 92 – Output Ripple. (PK-PK – 58 mV).
265 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

13.6.2.4 25% Load

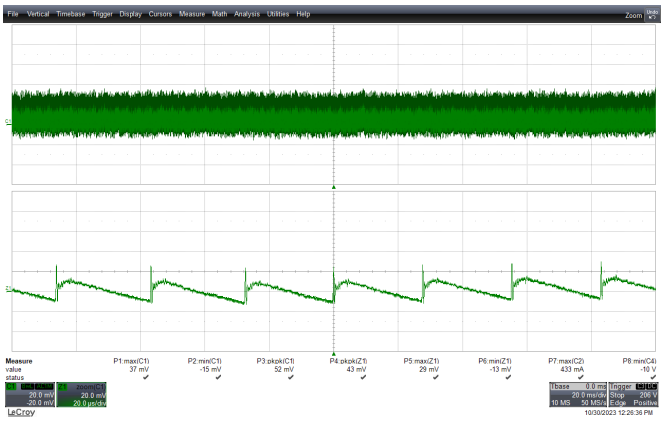


Figure 93 – Output Ripple. (PK-PK – 52 mV).
90 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

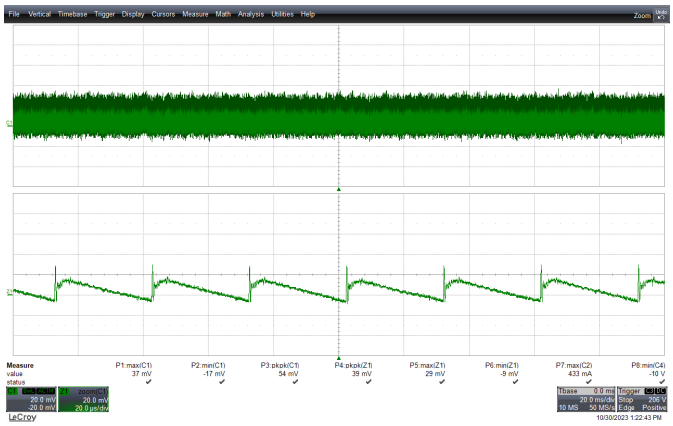


Figure 94 – Output Ripple. (PK-PK – 54 mV).
115 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

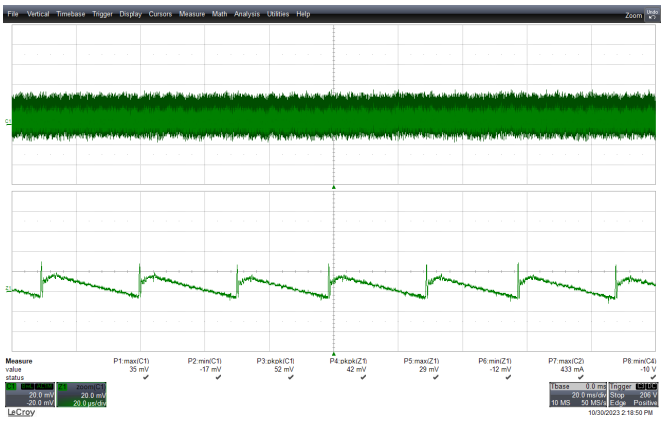


Figure 95 – Output Ripple. (PK-PK – 52 mV).
230 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

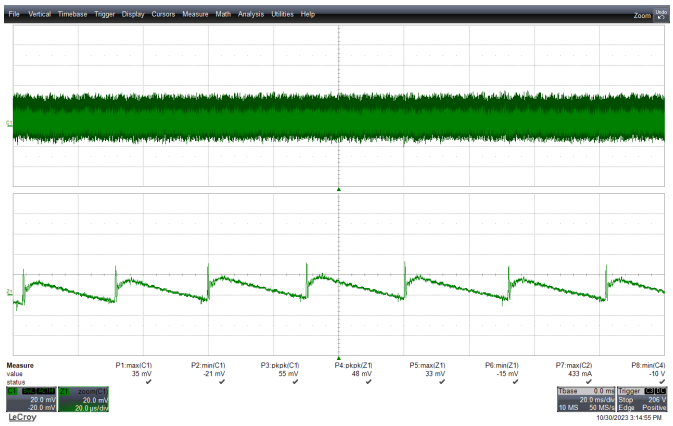


Figure 96 – Output Ripple. (PK-PK – 55 mV).
265 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

13.6.2.5 10% Load

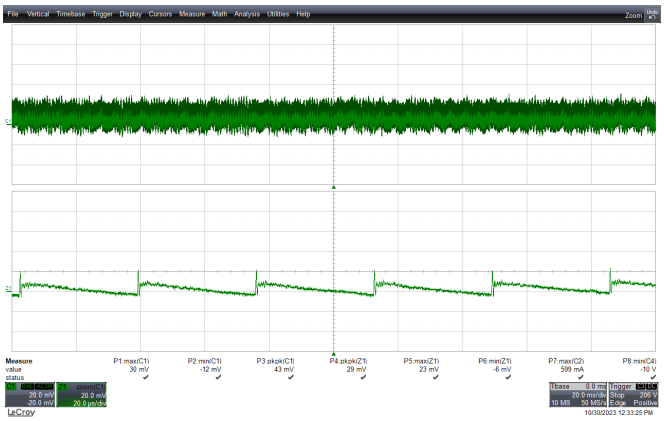


Figure 97 – Output Ripple. (PK-PK – 43 mV).
90 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

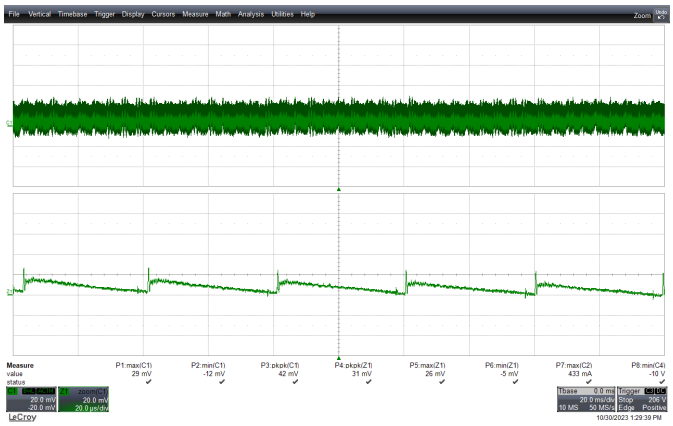


Figure 98 – Output Ripple. (PK-PK – 42 mV).
115 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

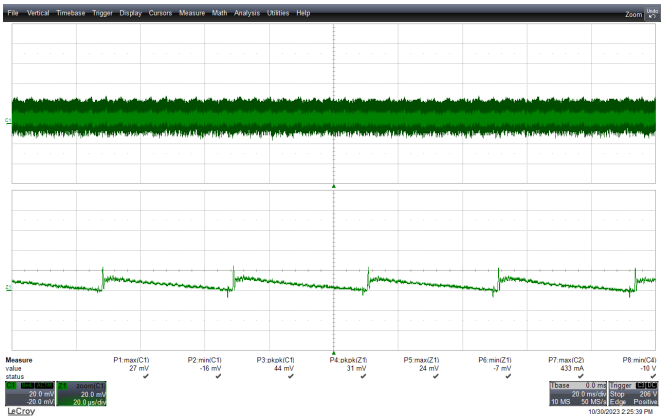


Figure 99 – Output Ripple. (PK-PK – 44 mV).
230 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

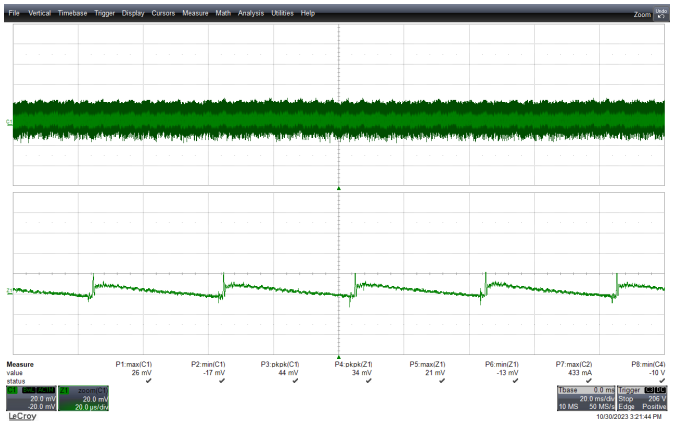


Figure 100 – Output Ripple. (PK-PK – 44 mV).
265 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

13.6.2.6 0% Load

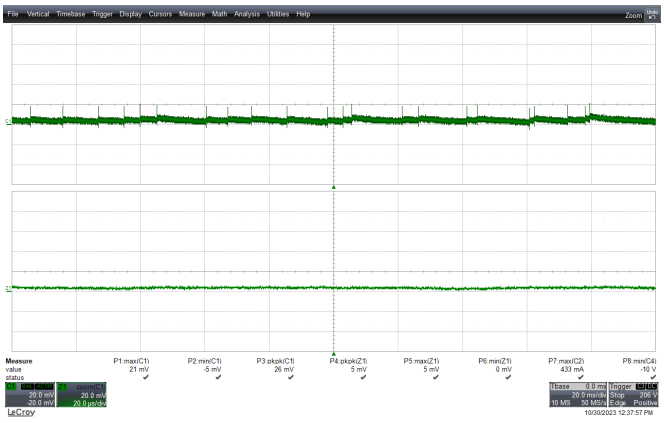


Figure 101 – Output Ripple. (PK-PK – 26 mV).
90 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

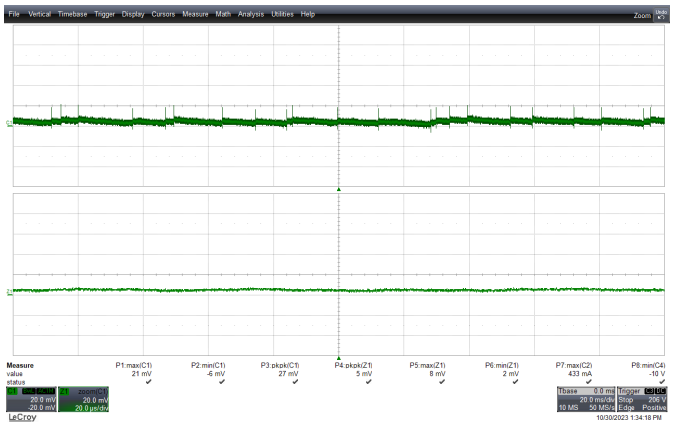


Figure 102 – Output Ripple. (PK-PK – 27 mV).
115 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

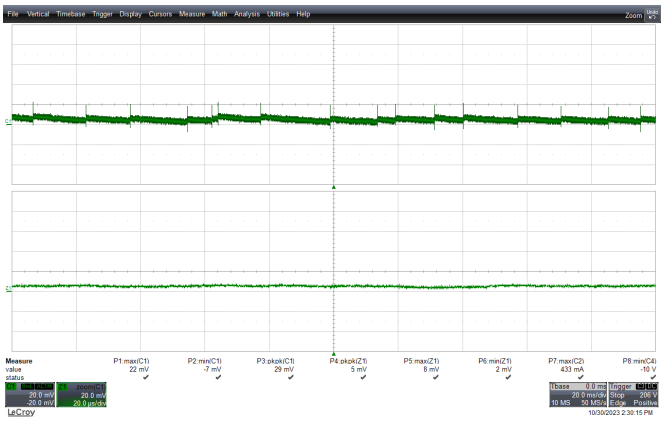


Figure 103 – Output Ripple. (PK-PK – 29 mV).
230 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

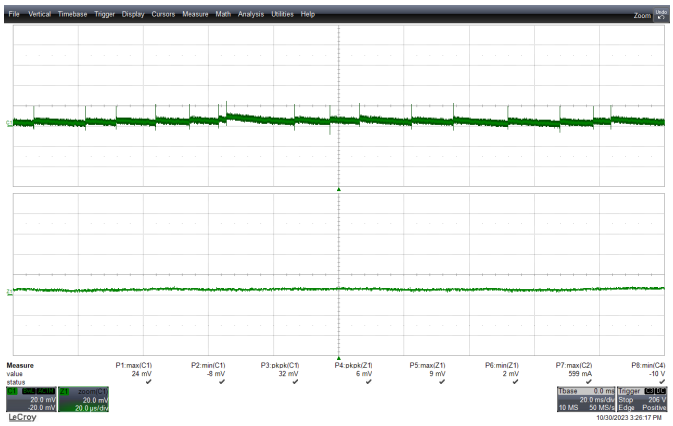


Figure 104 – Output Ripple. (PK-PK – 32 mV).
265 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 20 mV / div, 20 ms / div.
Zoom: 20 μs.

13.6.3 Output Voltage Ripple

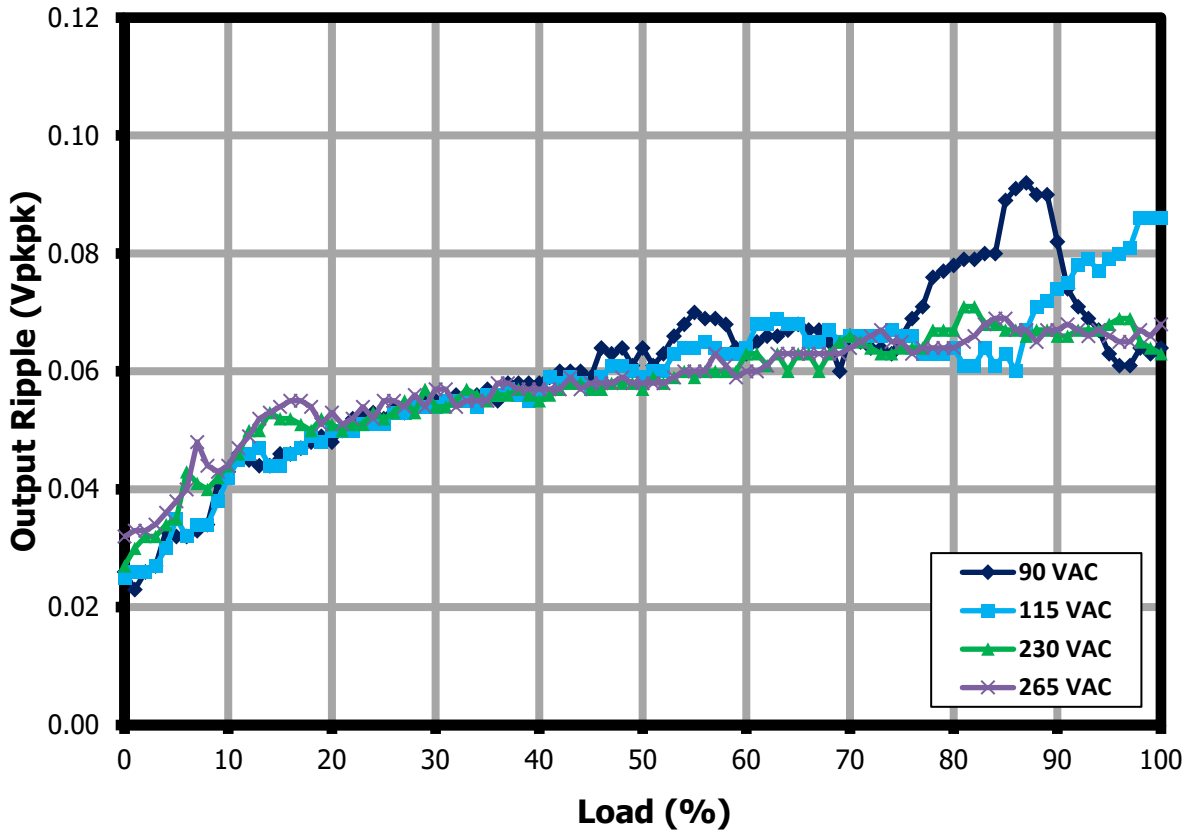


Figure 105 – Output Ripple.

13.7 Brown-In and Brown-Out

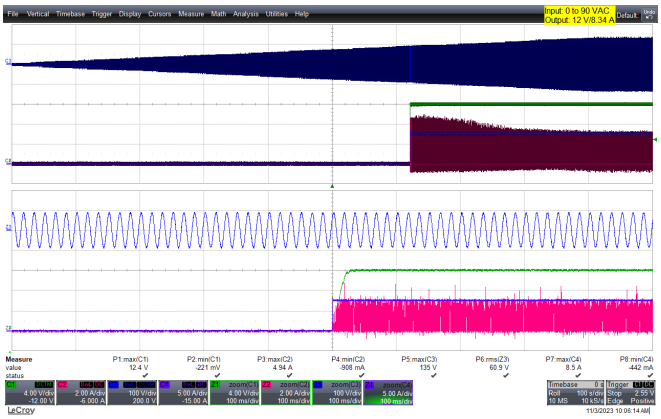


Figure 106 – 0-90 VAC Brown-In (0.1 V / s) R_{LOAD} = 1.44 Ω (Full-Load, CR).
CH 1: Output Voltage: 4 V / div, 100 s / div.
CH 2: Drain Current: 2 A / div, 100 s / div.
CH 3: Input Voltage: 100 V / div, 100 s / div.
CH 4: Output Current: 5 A / div., 100 s / div.
Brown-In Voltage, RMS = 60.9 V.

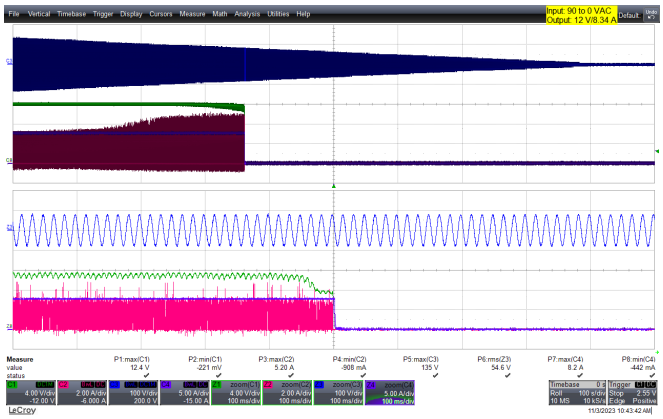


Figure 107 – 90-0 VAC Brown-Out (0.1 V / s) R_{LOAD} = 1.44 Ω (Full-Load, CR).
CH 1: Output Voltage: 4 V / div, 100 s / div.
CH 2: Drain Current: 2 A / div, 100 s / div.
CH 3: Input Voltage: 100 V / div, 100 s / div.
CH 4: Output Current: 5 A / div., 100 s / div.
Brown-Out Voltage, RMS = 54.6 V.

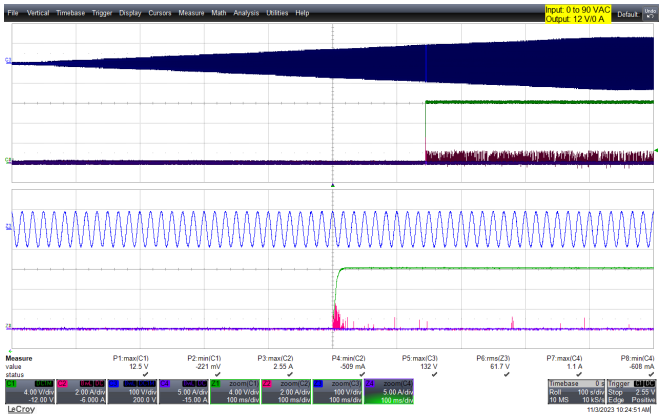


Figure 108 – 0-90 VAC brown-in (0.1 V / s) No-Load.
CH 1: Output Voltage: 4 V / div, 100 s / div.
CH 2: Drain Current: 2 A / div, 100 s / div.
CH 3: Input Voltage: 100 V / div, 100 s / div.
CH 4: Output Current: 5 A / div., 100 s / div.
Brown-In Voltage, RMS = 61.7 V.

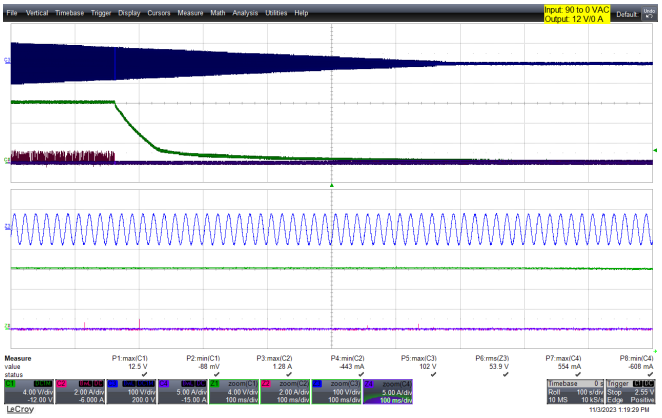


Figure 109 – 90-0 VAC brown-out (0.1 V / s) No-Load.
CH 1: Output Voltage: 4 V / div, 100 s / div.
CH 2: Drain Current: 2 A / div, 100 s / div.
CH 3: Input Voltage: 100 V / div, 100 s / div.
CH 4: Output Current: 5 A / div., 100 s / div.
Brown-Out Voltage, RMS = 53.9 V.

13.8 Overvoltage Protection

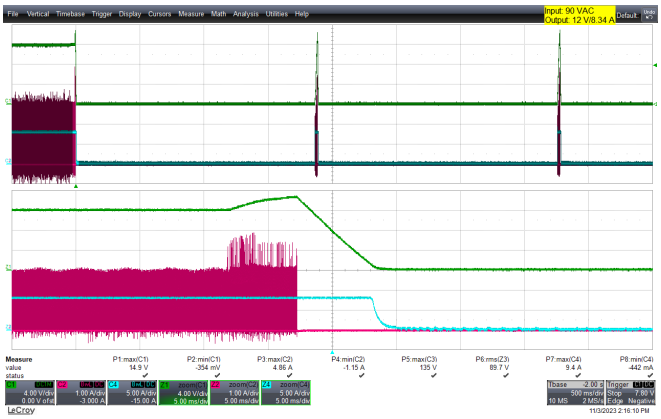


Figure 110 – 90 VAC, I_{OUT} = 8.34 A (Full-Load).
OVP Running Short.
CH 1: Output Voltage: 4 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 14.9 V

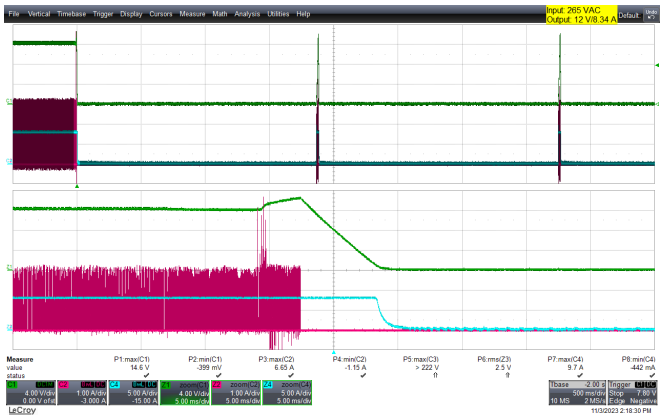


Figure 111 – 265 VAC, I_{OUT} = 8.34 A (Full-Load).
OVP Running Short
CH 1: Output Voltage: 4 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 14.6 V

Figure 112 – 90 VAC, I_{OUT} = 0 A (No-Load).
OVP Running Short.
CH 1: Output Voltage: 4 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 14.6 V

Figure 113 – 265 VAC, I_{OUT} = 0 A (No-Load).
OVP Running Short
CH 1: Output Voltage: 4 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 14.6 V

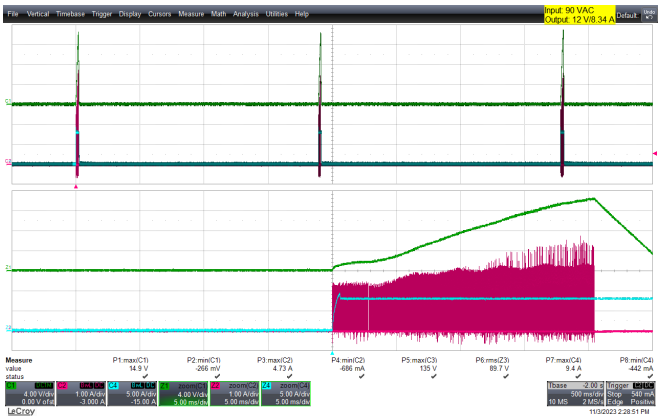


Figure 114 – 90 VAC, I_{OUT} = 8.34 A (Full-Load).
OVP Startup.
CH 1: Output Voltage: 4 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 14.9 V

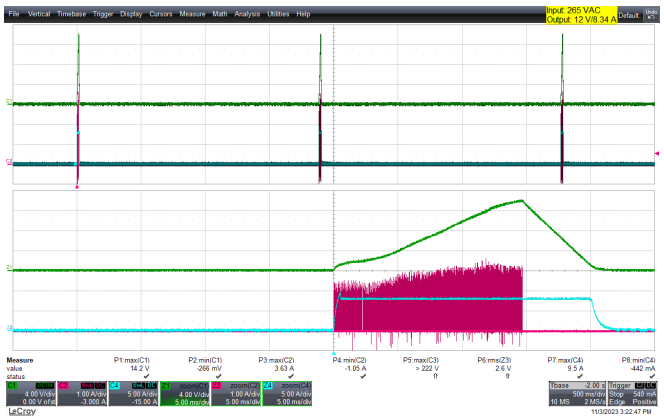


Figure 115 – 265 VAC, I_{OUT} = 8.34 A (Full-Load).
OVP Startup.
CH 1: Output Voltage: 4 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 14.2 V

14 Conducted EMI

14.1 Floating Output

14.1.1 Line

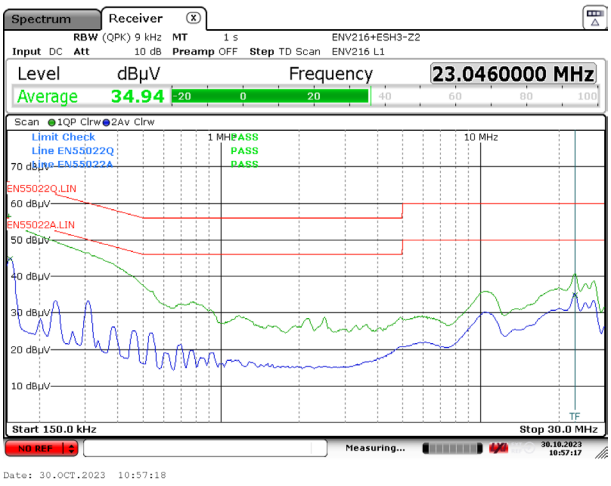


Figure 116 – Floating Output EMI, 12 V / 100% Load for 115 VAC.

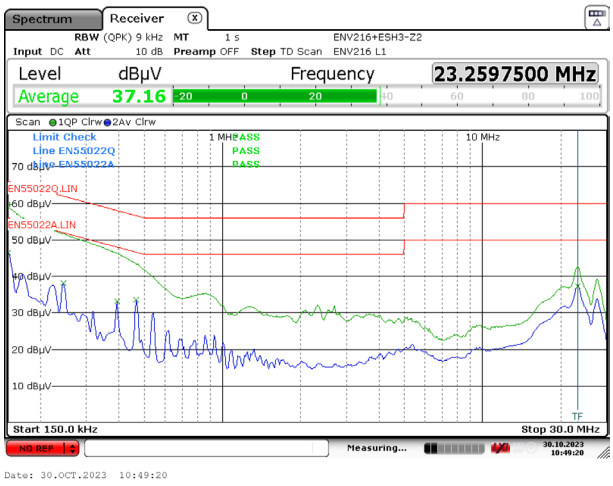


Figure 117 – Floating Output EMI, 12 V / 100% Load for 230 VAC.

14.1.2 Neutral

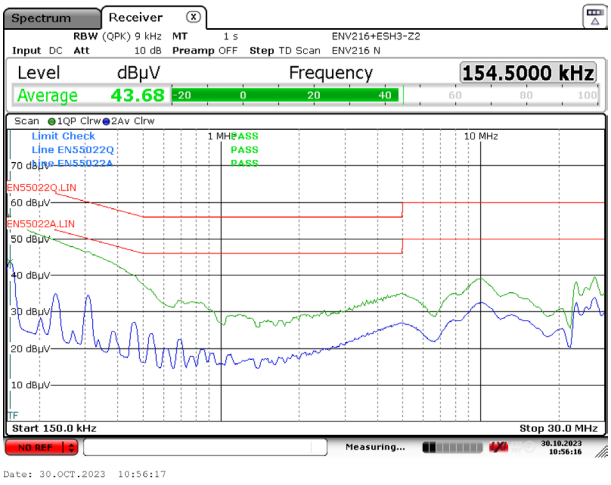


Figure 118 – Floating Output EMI, 12 V / 100% Load for 115 VAC.

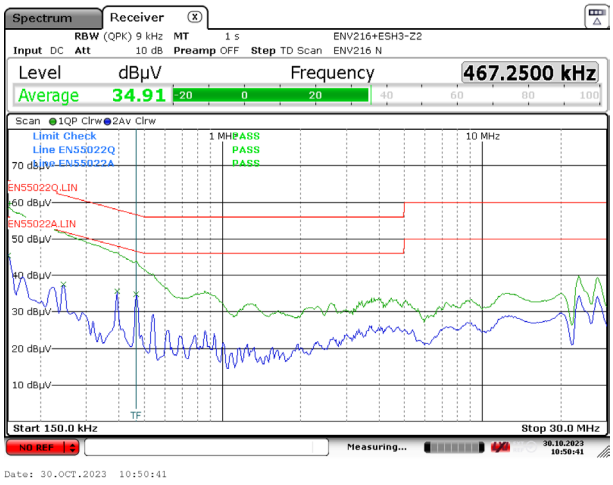


Figure 119 – Floating Output EMI, 12 V / 100% Load for 230 VAC.

14.2 Artificial Hand Output

14.2.1 Line

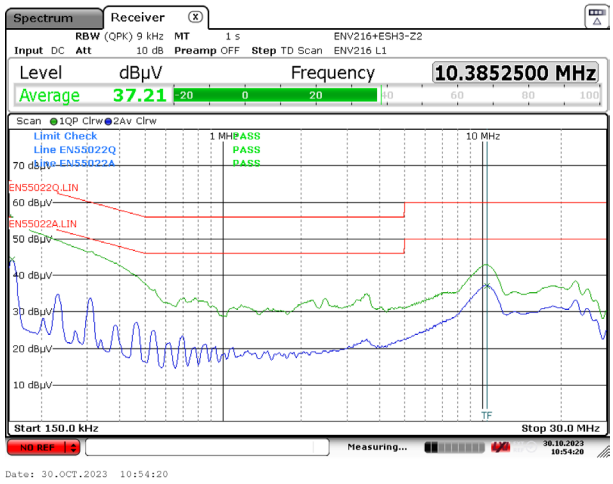


Figure 120 – Artificial hand Output EMI, 12 V / 100% Load for 115 VAC.

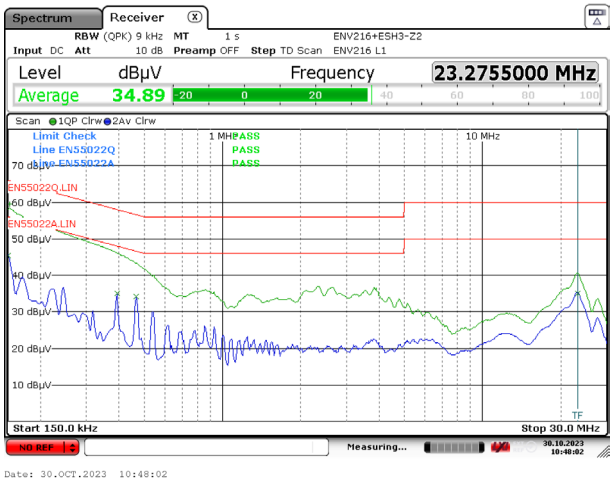


Figure 121 – Artificial hand Output EMI, 12 V / 100% Load for 230 VAC.

14.2.2 Neutral

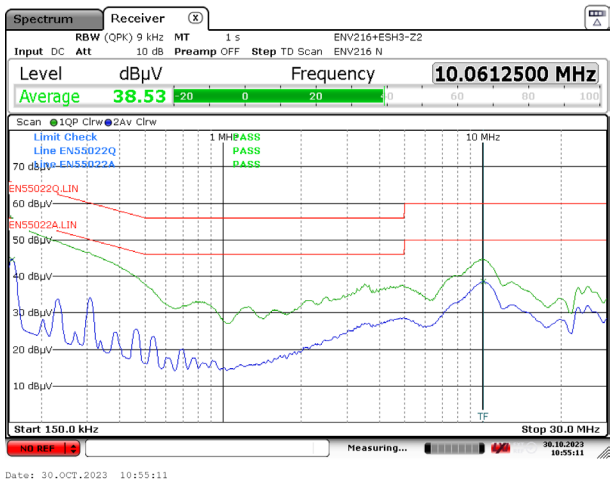


Figure 122 – Artificial hand Output EMI, 12 V / 100% Load for 115 VAC.

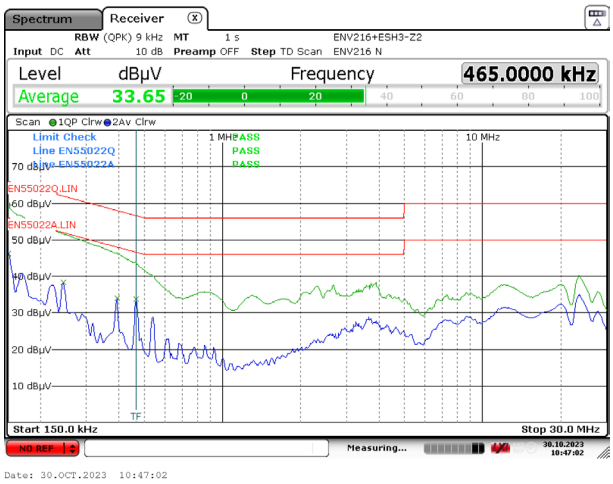


Figure 123 – Artificial Hand Output EMI, 12 V / 100% Load for 230 VAC.

14.3 Grounded Output

14.3.1 Line

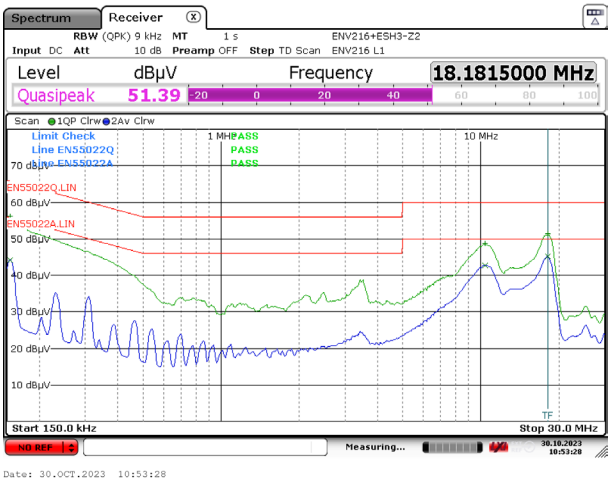


Figure 124 – Grounded Output EMI, 12 V / 100% Load for 115 VAC.

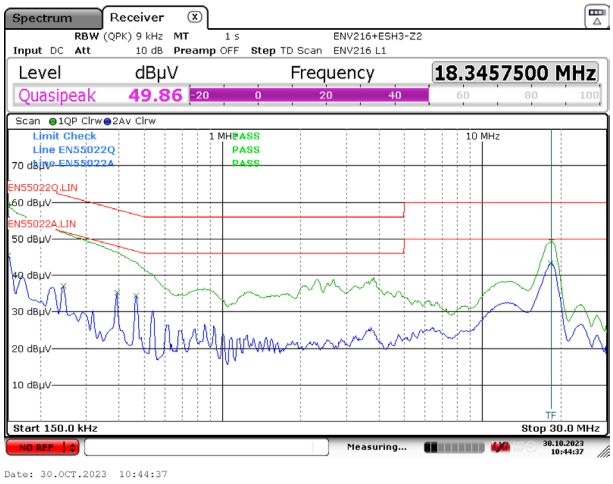


Figure 125 – Grounded Output EMI, 12 V / 100% Load for 230 VAC.

14.3.2 Neutral

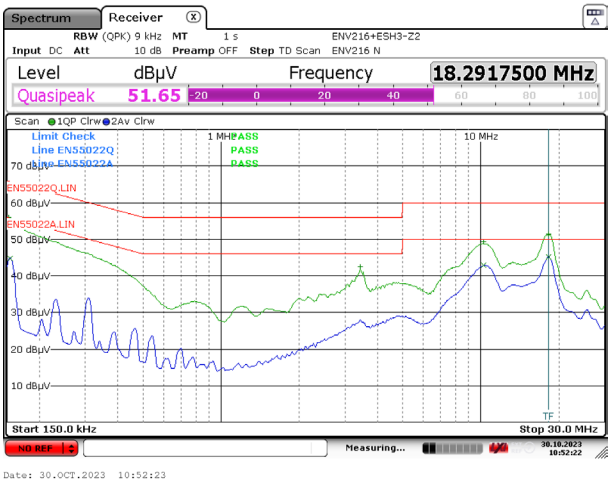


Figure 126 – Grounded Output EMI, 12 V / 100% Load for 115 VAC.

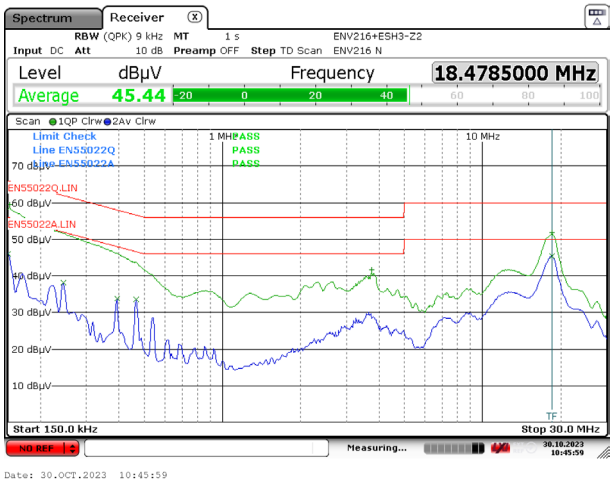


Figure 127 – Grounded Output EMI, 12 V / 100% Load for 230 VAC.

15 Line Surge

15.1 Differential Mode Test

15.1.1 230 VAC Input

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1000	0	L, N	2	10	Pass – No AR
–1000	0	L, N	2	10	Pass – No AR
+1000	90	L, N	2	10	Pass – No AR
–1000	90	L, N	2	10	Pass – No AR
+1000	180	L, N	2	10	Pass – No AR
–1000	180	L, N	2	10	Pass – No AR
+1000	270	L, N	2	10	Pass – No AR
–1000	270	L, N	2	10	Pass – No AR
+2000	0	L, N	2	10	Pass – No AR
–2000	0	L, N	2	10	Pass – No AR
+2000	90	L, N	2	10	Pass – No AR
–2000	90	L, N	2	10	Pass – No AR
+2000	180	L, N	2	10	Pass – No AR
–2000	180	L, N	2	10	Pass – No AR
+2000	270	L, N	2	10	Pass – No AR
–2000	270	L, N	2	10	Pass – No AR

15.2 Ring Wave Surge

15.2.1 230 VAC Input

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	0	L, N → PE	12	10	Pass – No AR
–6000	0	L, N → PE	12	10	Pass – No AR
+6000	90	L, N → PE	12	10	Pass – No AR
–6000	90	L, N → PE	12	10	Pass – No AR
+6000	180	L, N → PE	12	10	Pass – No AR
–6000	180	L, N → PE	12	10	Pass – No AR
+6000	270	L, N → PE	12	10	Pass – No AR
–6000	270	L, N → PE	12	10	Pass – No AR

16 EFT

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Frequency (kHz)	Burst Time	Reception Time (ms)	Step Duration (s)	Result
+4000	0	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	0	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	90	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	90	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	180	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	180	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	270	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	270	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	0	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	0	L, N - PE	100	750 µs	300	120	Pass – No AR
+4000	90	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	90	L, N - PE	100	750 µs	300	120	Pass – No AR
+4000	180	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	180	L, N - PE	100	750 µs	300	120	Pass – No AR
+4000	270	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	270	L, N - PE	100	750 µs	300	120	Pass – No AR

17 ESD

Passed ±16.5 kV air discharge and ±8.8 kV contact discharge at both output positive and negative terminals, under full load condition for 230 VAC input.

Contact Discharge

No.	Test Voltage	No. of Strikes	Discharge Location	Remarks	Pass/Fail
1	+2	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
2		10	- Output Terminal End of Cable	No Damage / No AR	Pass
3	-2	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
4		10	- Output Terminal End of Cable	No Damage / No AR	Pass
5	+4	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
6		10	- Output Terminal End of Cable	No Damage / No AR	Pass
7	-4	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
8		10	- Output Terminal End of Cable	No Damage / No AR	Pass
9	+6	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
10		10	- Output Terminal End of Cable	No Damage / No AR	Pass
11	-6	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
12		10	- Output Terminal End of Cable	No Damage / No AR	Pass
13	+8.8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
14		10	- Output Terminal End of Cable	No Damage / No AR	Pass
15	-8.8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
16		10	- Output Terminal End of Cable	No Damage / No AR	Pass

Air Discharge

No.	Test Voltage	No. of Strikes	Discharge Location	Remarks	Pass/Fail
1	+8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
2		10	- Output Terminal End of Cable	No Damage / No AR	Pass
3	-8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
4		10	- Output Terminal End of Cable	No Damage / No AR	Pass
5	+10	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
6		10	- Output Terminal End of Cable	No Damage / No AR	Pass
7	-10	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
8		10	- Output Terminal End of Cable	No Damage / No AR	Pass
9	+12	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
10		10	- Output Terminal End of Cable	No Damage / No AR	Pass
11	-12	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
12		10	- Output Terminal End of Cable	No Damage / No AR	Pass
13	+14	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
14		10	- Output Terminal End of Cable	No Damage / No AR	Pass
15	-14	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
16		10	- Output Terminal End of Cable	No Damage / No AR	Pass
17	+16.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
18		10	- Output Terminal End of Cable	No Damage / No AR	Pass
19	-16.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
20		10	- Output Terminal End of Cable	No Damage / No AR	Pass

18 Revision History

Date	Author	Revision	Description & Changes
6-Nov-25	MA	A	First Release

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.

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