Design Example Report

Title	**120 W Isolated Flyback Power Supply with 150 W Peak Power Using InnoSwitch™4-QR INN4277C-H185**
Specification	90 VAC – 265 VAC Input; 24 V / 5 A Nominal Output; 24 V / 6.25 A Short-Term Peak Power
Application	Appliance Application
Author	Applications Engineering Department
Document Number	DER-1032
Date	November 21, 2025
Revision	A

Summary and Features

- Very high average efficiency
  - >93.9% at 115 VAC and >94.9% at 230 VAC
- Very high full-load efficiency
  - 92.5% at 115 VAC and 95.4% at 230 VAC
- <110 mW no-load input power at 230 VAC input
- No optocoupler increases reliability
- Meets EN550022 and CISPR-22 Class B conducted EMI

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 24 V / 5 A power supply using the InnoSwitch™4-QR INN4277C-H185 IC. This design shows a high-power density and efficiency that is possible due to the high level of integration of the InnoSwitch4-QR controller, driving the integrated PowiGaN™ switch while employing quasi-resonant switching.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

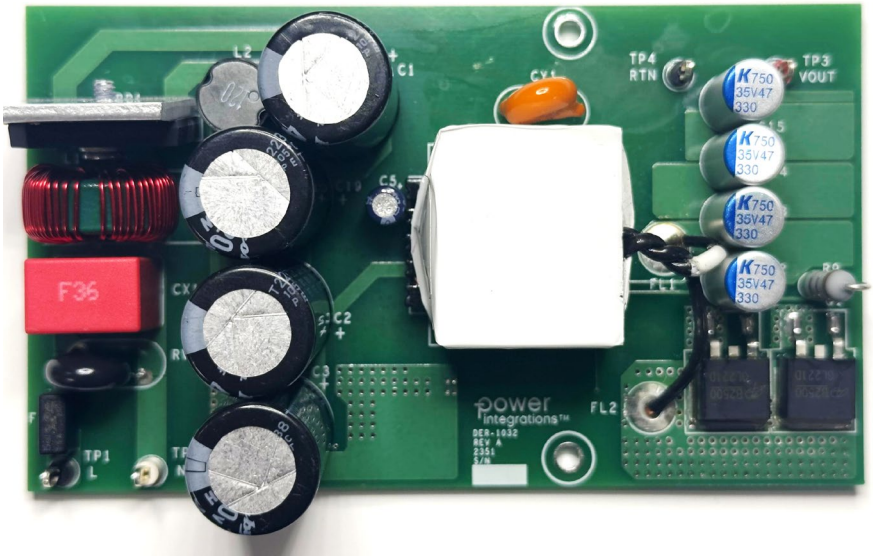


Figure 1 – Populated Circuit Board, Top.

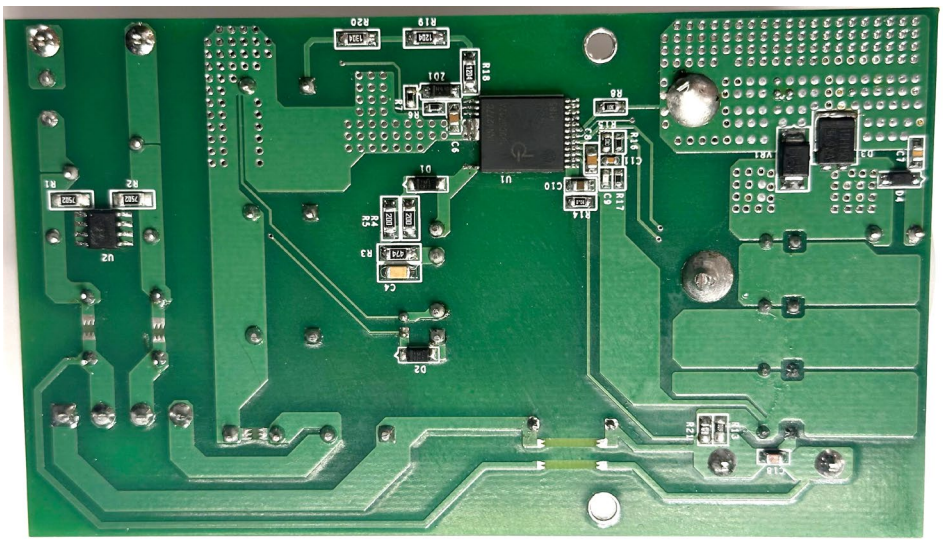


Figure 2 – Populated Circuit Board, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min	Nom	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115/230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				120	mW	
Output						
Output Voltage	V_{OUT}	22.8	24	25.2	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			240	mV	20 MHz Bandwidth, at 25 °C Ambient
Output Current	I_{OUT}		5		A	
Total Output Power						
Continuous Output Power	P_{OUT}		120		W	
Efficiency						
	η		92.5		%	Full Load @ 115 VAC
			95.5			Full Load @ 230 VAC
			93.9			Average @ 115 VAC
			95			Average @ 230 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				2	kV	1.2/50 μs Surge, IEC 61000-4-5, Impedance: 2 Ω Class A
Combination Wave Surge Test				6	kV	
EFT				4	kV	IEC 61000-4-4
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

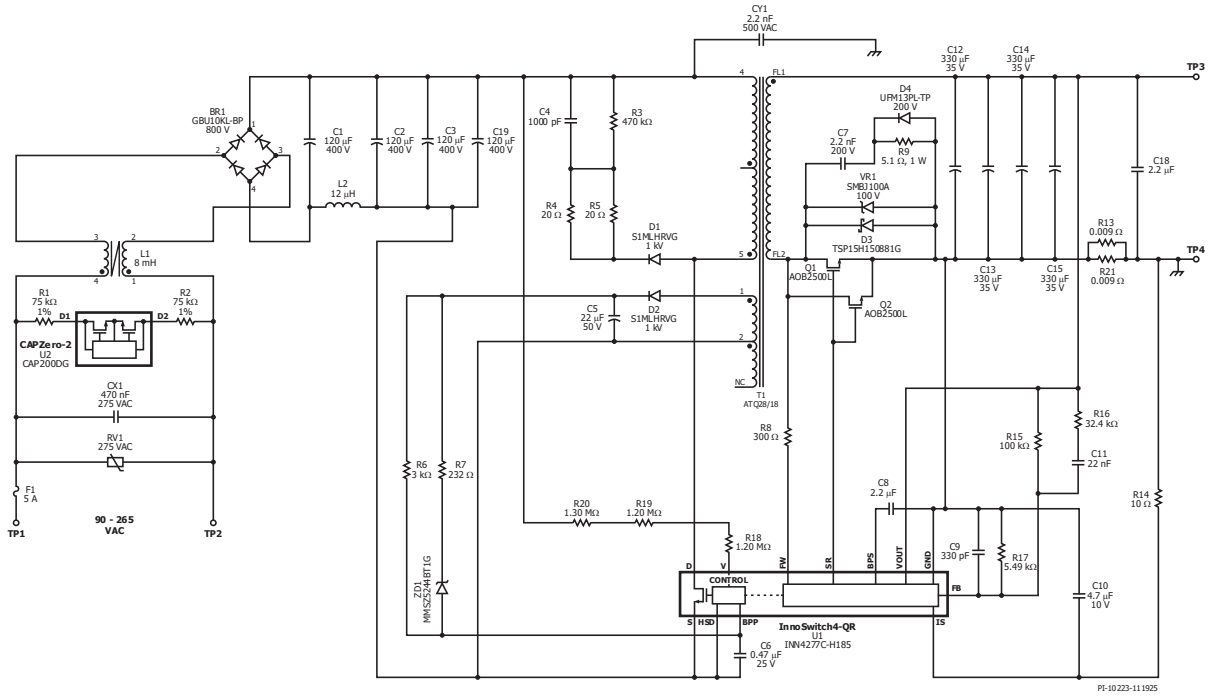


Figure 3 – Power Stage Schematic.

4 Circuit Description

The InnoSwitch4-QR IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates a PowiGaN primary power switch, primary-side controller, secondary-side controller for synchronous rectification and Fluxlink™ technology which provides safety isolated secondary-side feedback without the need for an optocoupler. InnoSwitch4-QR operates in quasi-resonant mode to achieve high efficiency.

4.1 Input EMI Filtering

Fuse F1 isolates the circuit and provides protection from component failure. Varistor RV1 clamps input voltage spike from input surge voltage. X capacitor CX1 and common mode choke L1 forms a filter to attenuate common mode noise. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitors. Filter capacitors C1, C2, C3 and C19 along with L2 form a pi filter. The pi filter attenuates both common and differential mode noise. The CAPZero™-2 IC (U2) with bleed resistors, R1 & R2, discharges the stored energy in CX1 when AC line is disconnected to meet safety requirement while ensuring very low no load input power. Capacitor CY1 is used to reduce common mode EMI.

4.2 InnoSwitch4-QR IC Primary

One end of the transformer (T1) primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4-QR IC (U1). Resistors R18, R19 and R20 provide input voltage sense for protection from line undervoltage and overvoltage.

A simple RCD clamp formed by diode D1, resistors R3, R4, R5 and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off the switch inside U1. The clamp helps dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R6 limits the current being supplied to the BPP pin of the InnoSwitch4-QR (U1).

Zener diode ZD1 along with resistor R7 provides primary sensed output overvoltage protection. In a flyback converter, the output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage on the output of the converter, the auxiliary winding voltage increases and causes breakdown of ZD1 which then causes a current to flow into the BPP pin of the InnoSwitch4-QR IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-QR controller will enter auto-restart and protect the converter (and load) from damage.

4.3 InnoSwitch4-QR IC Secondary

The secondary-side of the InnoSwitch4-QR IC provides output voltage and current sensing and drives to the synchronous rectification (SR) FET. The secondary of the transformer is rectified by SR FETs Q1, Q2 and diode D3, and filtered by output capacitors C12, C13, C14 and C15. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber R9, C7 and D4 along with TVS diode VR1. Diode D4 minimizes the dissipation in resistor R9.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C8 connected to the BPS pin of InnoSwitch4-QR IC U1 provides decoupling for the internal circuitry.

The gates of Q1 and Q2 are turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R8 and fed into the FWD pin of the IC. The FWD pin is also used to supply the secondary side of IC U1 when V_{OUT} pin is below the threshold value.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary side requesting a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drops across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$.

Output current is sensed by monitoring the voltage drop across resistors R13 & R21 which are connected between the IS and GND pins. A low threshold of approximately 35 mV is used to reduce losses. Capacitor C10 provides filtering to protect the IS pin from external noise.

The device operates in constant voltage mode before reaching the current limit set by resistors R13 & R21. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via the potential divider formed by resistors R15 and R17. The voltage across R17 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. Output voltage is regulated to achieve a voltage of 1.265 V on the FB pin. Capacitor C9 provides noise filtering for the FB pin.

The capacitors C12, C13, C14, C15 and C18 are used to reduce high frequency output voltage ripple.

5 PCB Layout

PCB copper thickness is 2.0 oz.
PCB Material Thickness is 1.6 mm.
PCB Material is FR4.

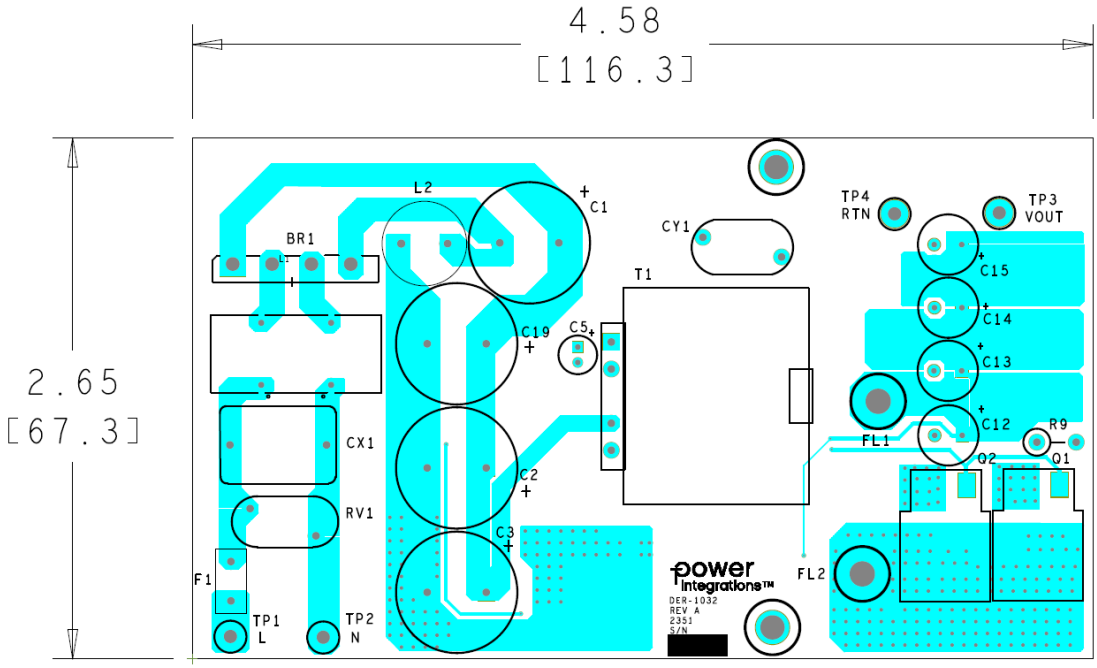


Figure 4 – Printed Circuit Layout, Top.

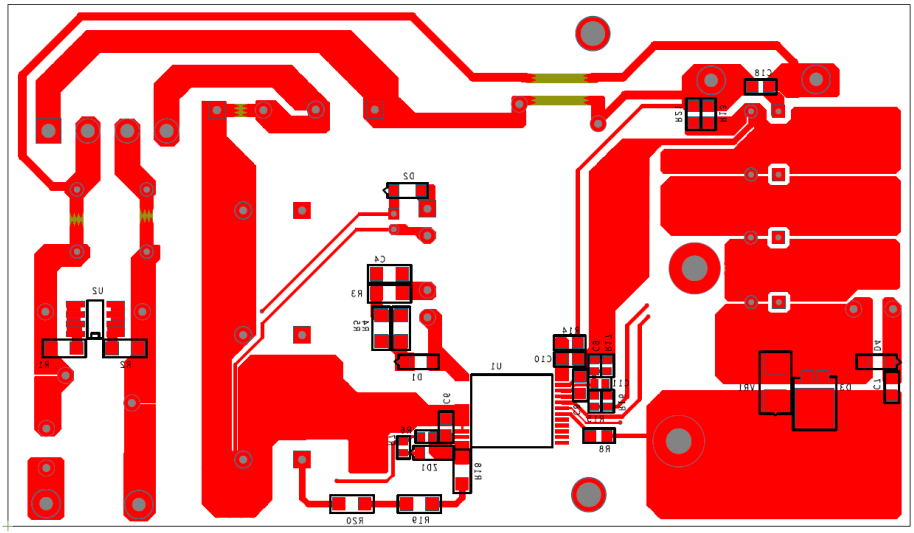


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 Bill of Material: Electrical Components

Item	Qty.	Ref Des.	Description	Mfr. Part Number	Manufacturer
1	1	BR1	BRIDGE Rectifier, Single Phase, Standard, 800 V, Through Hole GBU	GBU10KL-BP	Micro Commercial Co
2	4	C1 C2 C3 C19	CAP, 120 µF, ±20%, 400 V Aluminum Electrolytic, Radial (16 x 32)	400HXW120MEFR16X30	Rubycon
3	1	C4	CAP, 1000 pF, ±10%, 500 V, Ceramic, X7R, 1206 (3216 Metric)	CC1206KKX7RBBB102	Yageo
4	1	C5	CAP, 22 µF, 50 V, Aluminum Electrolytic, Radial (5 x 11)	UPW1H220MDD	Nichicon
5	1	C6	CAP, 0.47 µF, ±10%, 25 V, Ceramic, X7R, 0805 (2012 Metric)	CGA4J2X7R1E474K125AA	TDK Corporation
6	1	C7	CAP, 2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX Corp
7	1	C8	CAP, 2.2 µF, ±10%, 10 V, Ceramic, X7R, 0805	C0805C225M8RACTU	Kemet
8	1	C9	CAP, 330 pF, ±5%, 50 V, Ceramic, C0G, NP0, 0603 (1608 Metric)	C0603C331J5GACAUTO	KEMET
9	1	C10	CAP, 4.7 µF, ±10% 10 V, Ceramic, X7R, 0805 (2012 Metric)	LMK212B7475KGHT	Taiyo Yuden
10	1	C11	CAP, 0.022 µF, ±5%, 25 V, Ceramic, X7R, 0603 (1608 Metric)	C0603C223J3RAC7867	KEMET
11	4	C12 C13 C14 C15	CAP, 330 µF, ±20%, 35 V, Al Polymer, Radial (8 x 16)	A750KW337M1VAAE020	KEMET
12	1	C18	CAP, 2.2 µF, ±10%, 50 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	CGA4J3X7R1H225K125AE	TDK
13	1	CX1	CAP, 470 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 10.00 mm	890324024005	Würth Elektronik
14	1	CY1	CAP, 2200 pF, ±20%, Class Y1 - 500 VAC Class X1 – 760 VAC, Ceramic, Y5U, Radial, Disc	440LD22-R	Vishay
15	2	D1 D2	DIODE, Standard, 1000 V, 1 A, Surface Mount, Sub SMA	S1MLHRVG	TAIWAN SEMICONDUCTOR
16	1	D3	DIODE, Schottky, Trench, 150 V, 15 A, Surface Mount, TO-277A (SMPC)	TSP15H150S S1G	Taiwan Semiconductor Corporation
17	1	D4	DIODE, Gen Purp, 200 V, 1 A, SOD-123F, SOD123FL	UFM13PL-TP	Micro Commercial Co.
18	1	F1	FUSE, 5 A, 250 V, Slow, Long Time Lag, RST	RST 5	Belfuse
19	1	L1	INDUCTOR, 8 mH, Toroidal Common Mode Choke, Input CMC (LCM) L1, 32 T #22 AWG Wirewound on Toroid Core: PI #30-00398-00 (JLW T18*10*7C-JL15 or equivalent.)	32-00462-00	Power Integrations
20	1	L2	INDUCTOR, 12 µH @ 100 KHz, ±10%, 5.1 A, 0.035 ohm, AEC-Q200, Unshielded, Ferrite, Radial, -40 °C ~ 85 °C, 11 x 11.5 mm	RFB1010-120L	Coilcraft
21	2	Q1 Q2	MOSFET, N-Channel 150 V 11.5 A (Ta), 152 A (Tc), 2.1 W (Ta), 375 W (Tc), Surface Mount, TO-263 (D2Pak)	AOB2500L	Alpha & Omega Semiconductor Inc.
22	2	R1 R2	RES, 75.0 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7502V	Panasonic
23	1	R3	RES, 470 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J474V	Panasonic
24	2	R4 R5	RES, 20 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J200V	Panasonic
25	1	R6	RES, 3 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3001V	Panasonic
26	1	R7	RES, 232 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2320V	Panasonic
27	1	R8	RES, 300 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ301V	Panasonic
28	1	R9	RES, 5.1 R, 5%, 1 W, Metal Oxide	RSF100JB-5R1	Yageo

29	2	R13 R21	RES, Current Sense, 0.009 R, ±1%, 0.5 W, 0805 (2012 Metric), Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
30	1	R14	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
31	1	R15	RES, 100 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
32	1	R16	RES, 32.4 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
33	1	R17	RES, 5.49 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5491V	Panasonic
34	2	R18 R19	RES, 1.20 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1204V	Panasonic
35	1	R20	RES, 1.30 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1304V	Panasonic
36	1	RV1	VARISTOR, 275 VAC, 80 J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
37	1	T1	BOBBIN, ATQ28/18, Vertical, 5 pins.	ATQ28/18	
38	1	U1	InnoSwitch4-QR, INN4277C-H185, InSOP-24D	INN4277C-H185	Power Integrations
39	1	U2	CAPZero-2, CAP200DG, SO-8C	CAP200DG	Power Integrations
40	1	VR1	DIODE, TVS, 162 V Clamp, 3.7 A Ipp, Unidirectional, Surface Mount DO-214AA (SMBJ)	SMBJ100A	Littelfuse
41	1	ZD1	DIODE ZENER, 14 V, 500 MW, SOD123	MMSZ5244BT1G	ON Semiconductor

6.2 Bill of Material: Mechanical Components

Item	Qty.	Ref Des.	Description	Manufacturer	Mfr. Part Number
19	2	FL1 FL2	FLYING LEAD, Hole size 130 mils	N/A	N/A
20	2	HS_CONN_1 HS_CONN_2	FLYING LEAD, Hole size 125 mils	N/A	N/A
1	2	TP1 TP4	TEST POINT, BLK, THRU-HOLE MOUNT	Keystone	5011
2	1	TP2	TEST POINT, WHT, THRU-HOLE MOUNT	Keystone	5012
3	1	TP3	TEST POINT, RED, THRU-HOLE MOUNT	Keystone	5010

7 Heat Sinks

7.1 Heat Spreader

7.1.1 Heat Spreader Sheet Metal Drawing

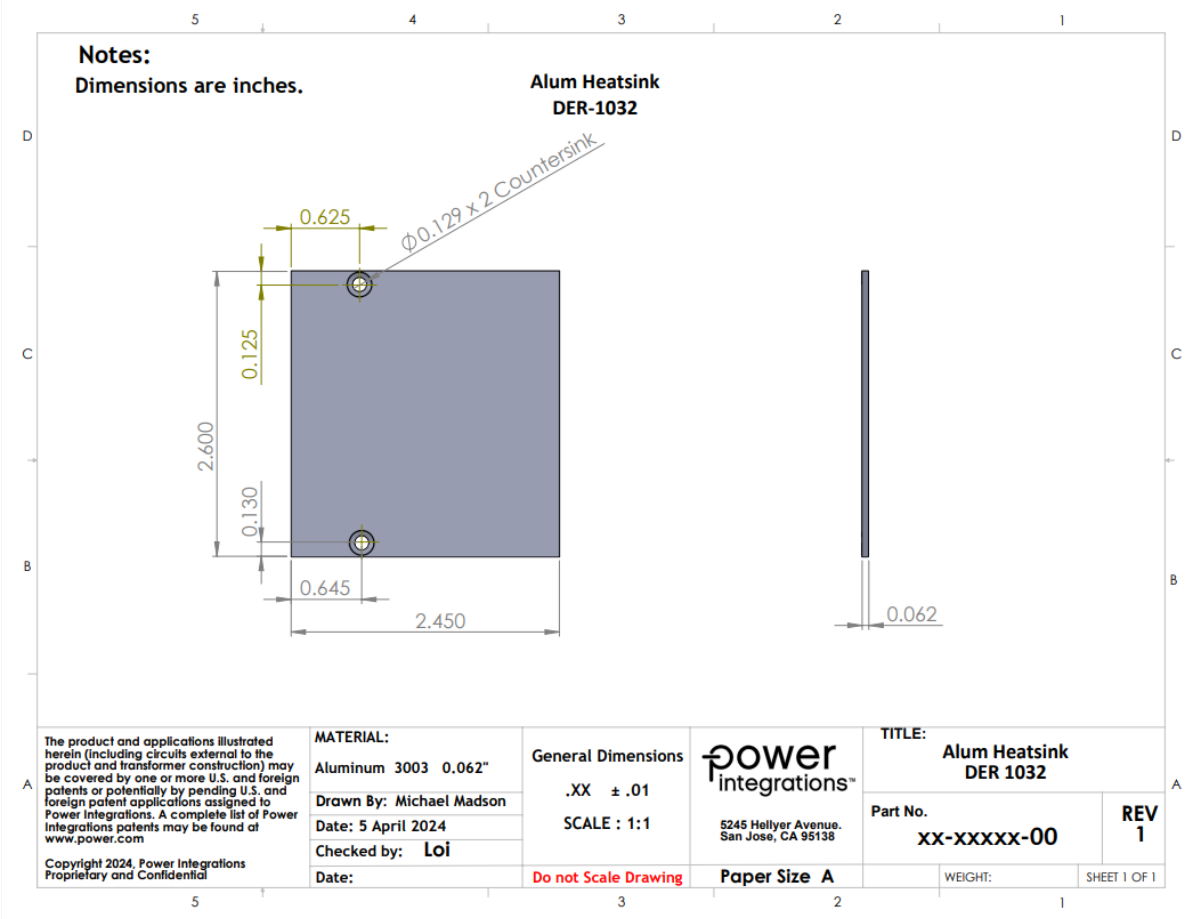


Figure 6 – DER-1032 Heat Spreader Sheet Metal Drawing.

7.1.2 Heat Spreader Assembly

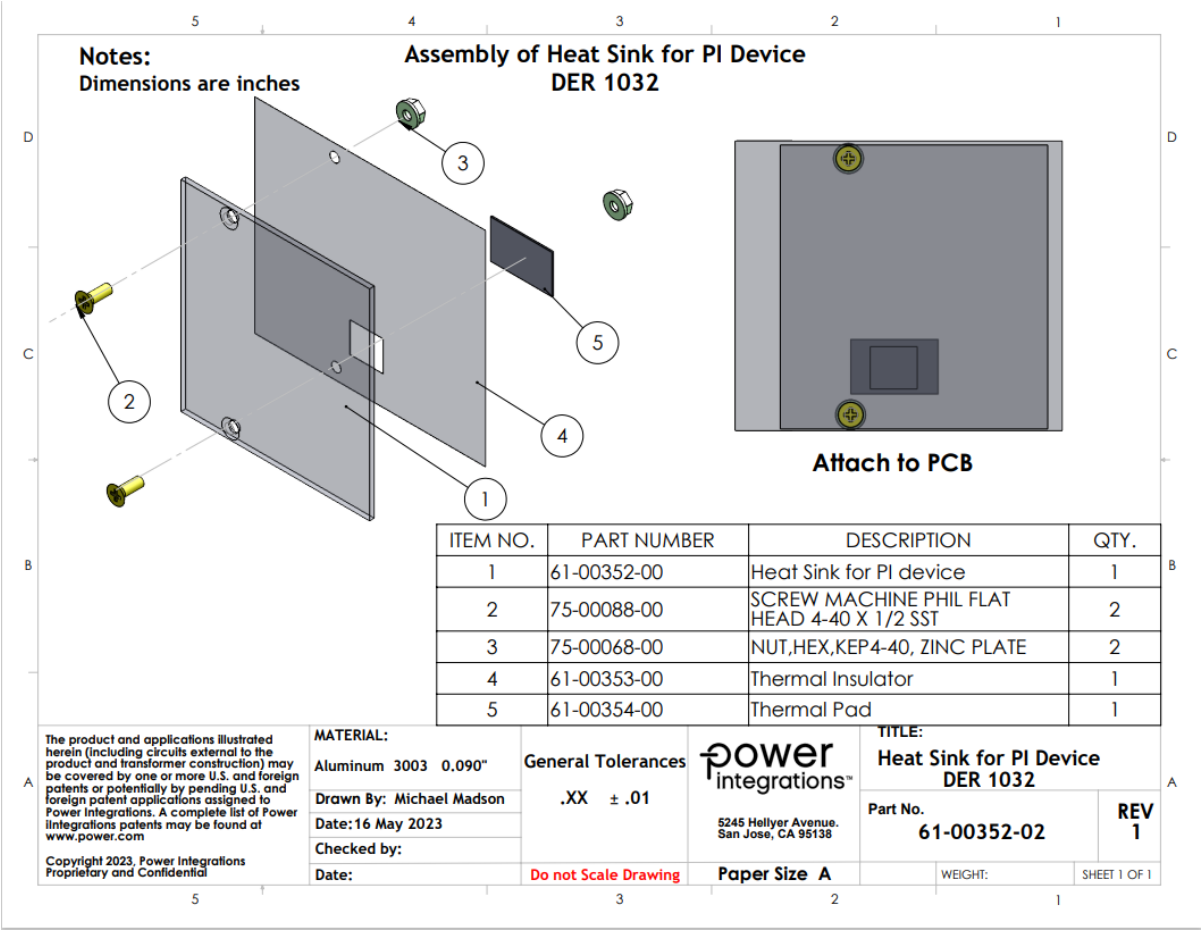
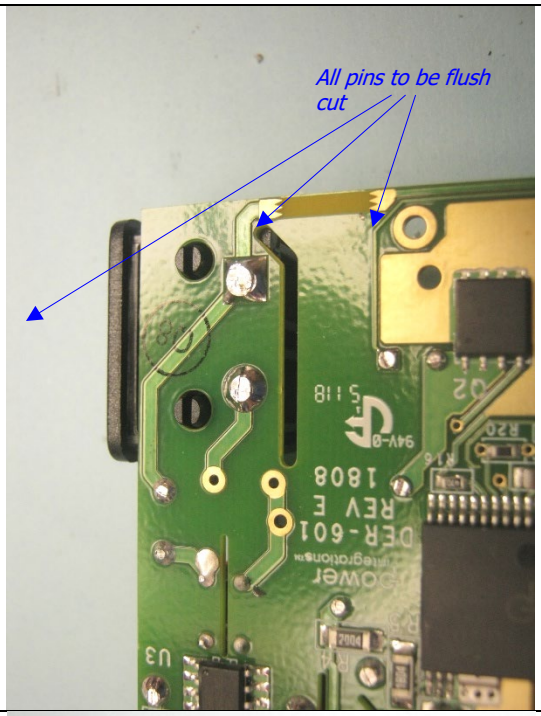
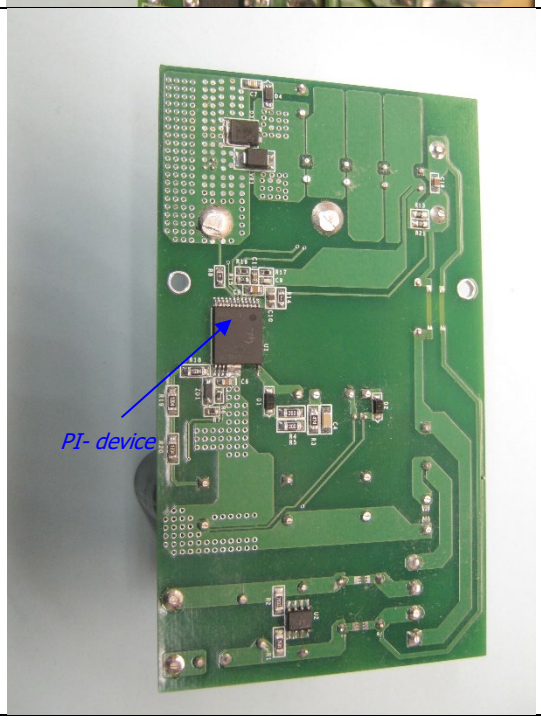


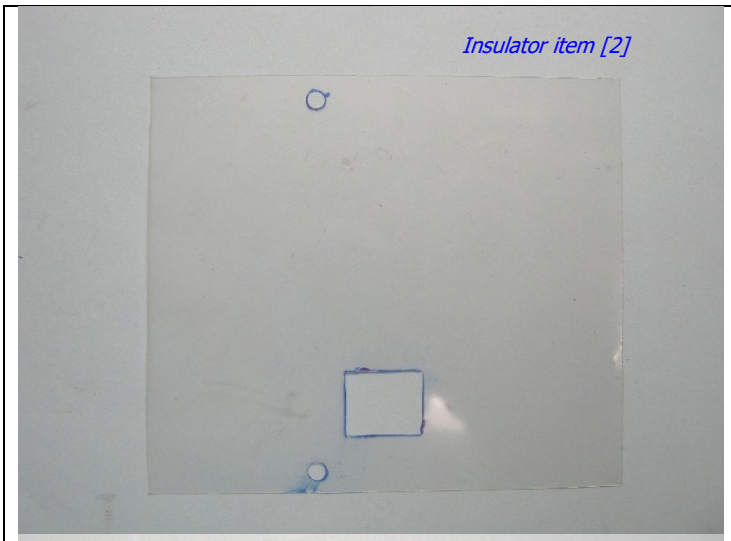
Figure 7 – DER-1032 Heat Spreader Assembly.

7.1.3 Materials

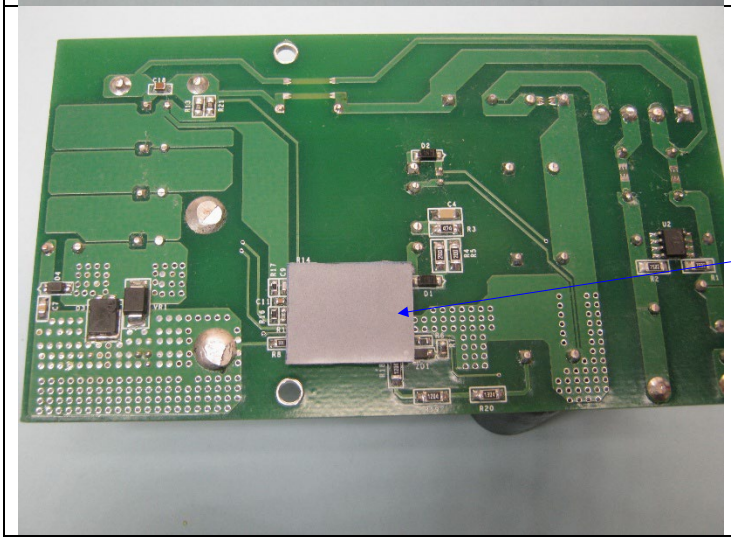
Item	Description
[1]	Heat spreader; Aluminum, 63 mil thick, PI#: 61-00352-00.
[2]	Clear, Mylar Teijin, 3 mil thick, (use material: 66-00230-0); PI#: 61-00353-00.
[3]	Thermal pad for PI device, 3M, 0.5 mm thick (use material: 66-00083-00); PI#: 61-00354-00.
[4]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 8.0 mm width; or equivalent.
[5]	Screw: 4-40, 5/16”, flat head, PI#: 75-00088-00.
[6]	Nut: Kepnut, 4-40, PI#: 75-00068-00.

7.1.4 Assembly Instructions

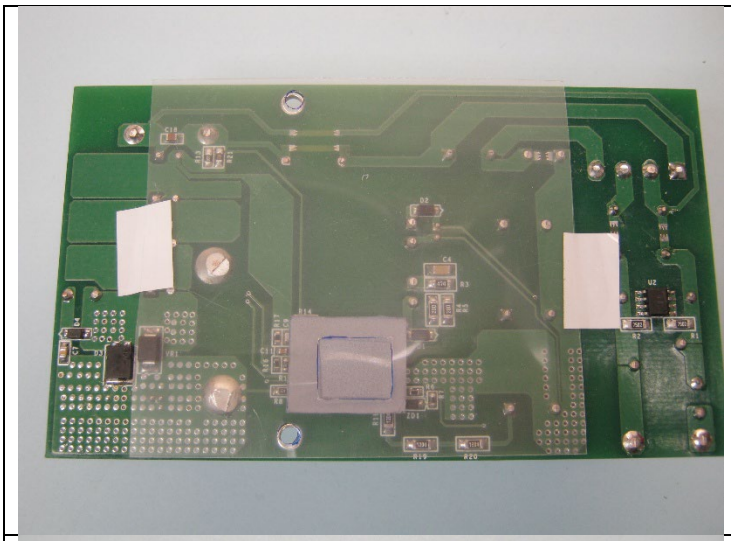
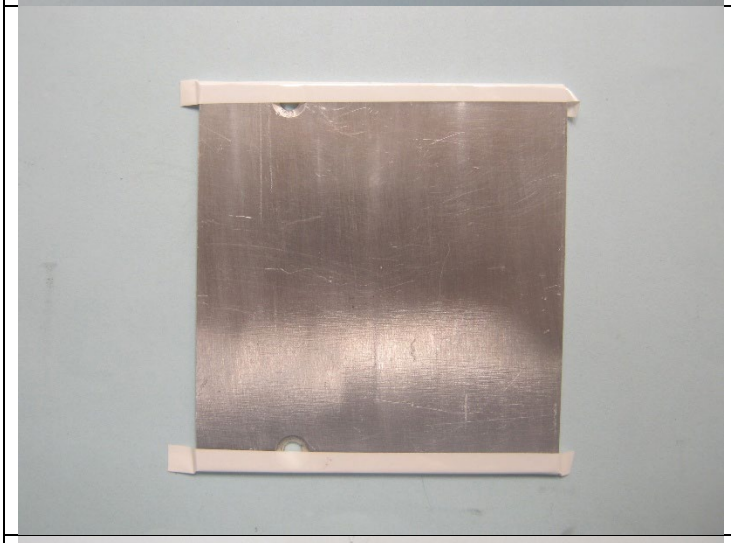
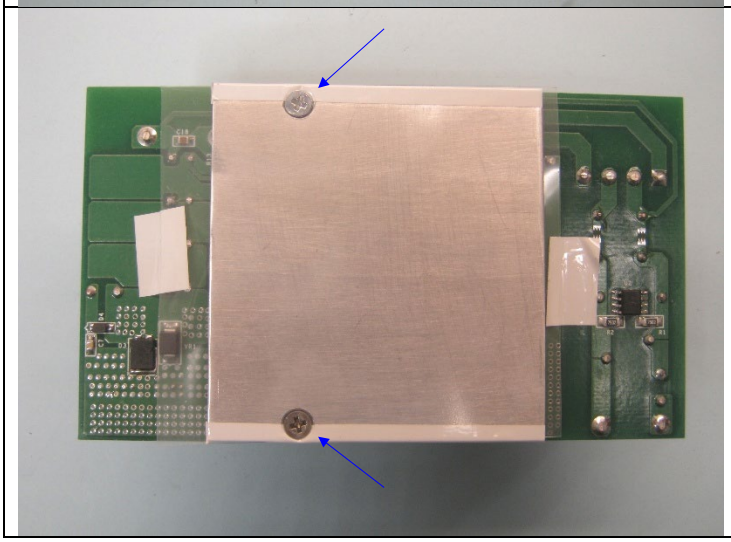
		Use proper flush cutters to have all pins of PCB to be flush cut to avoid any pins poking into the thermal pads. (see illustration beside for reference).
		Bottom of board.

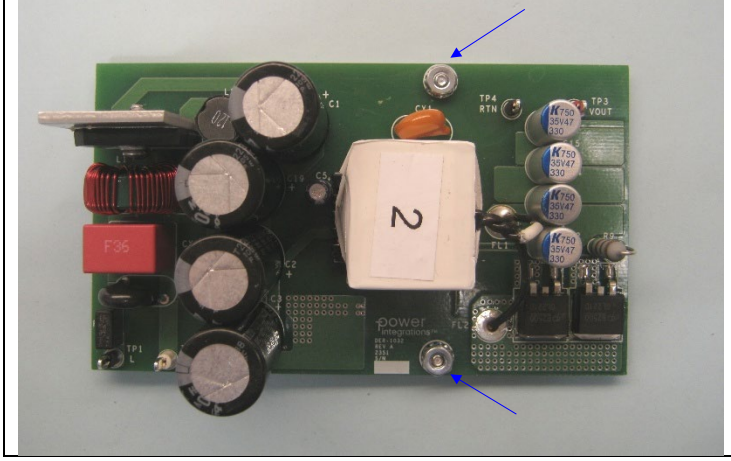


Prepare insulator Item [2] and thermal pads Item [3].



Place thermal pad Item [4] on PI – device (device should be center of thermal pad).

	Place insulator Item [2] on bottom of board. Note the use of tape to keep it correctly aligned in place.
	Prepare heat spreader Item [1], and wrap around on 2 sides with tape Item [4], (see picture beside).
	Secure with screws Item [5] and nuts Item [6].



7.2 Bridge Diode Heatsink

7.2.1 Bridge Diode Heatsink Sheet Metal Drawing

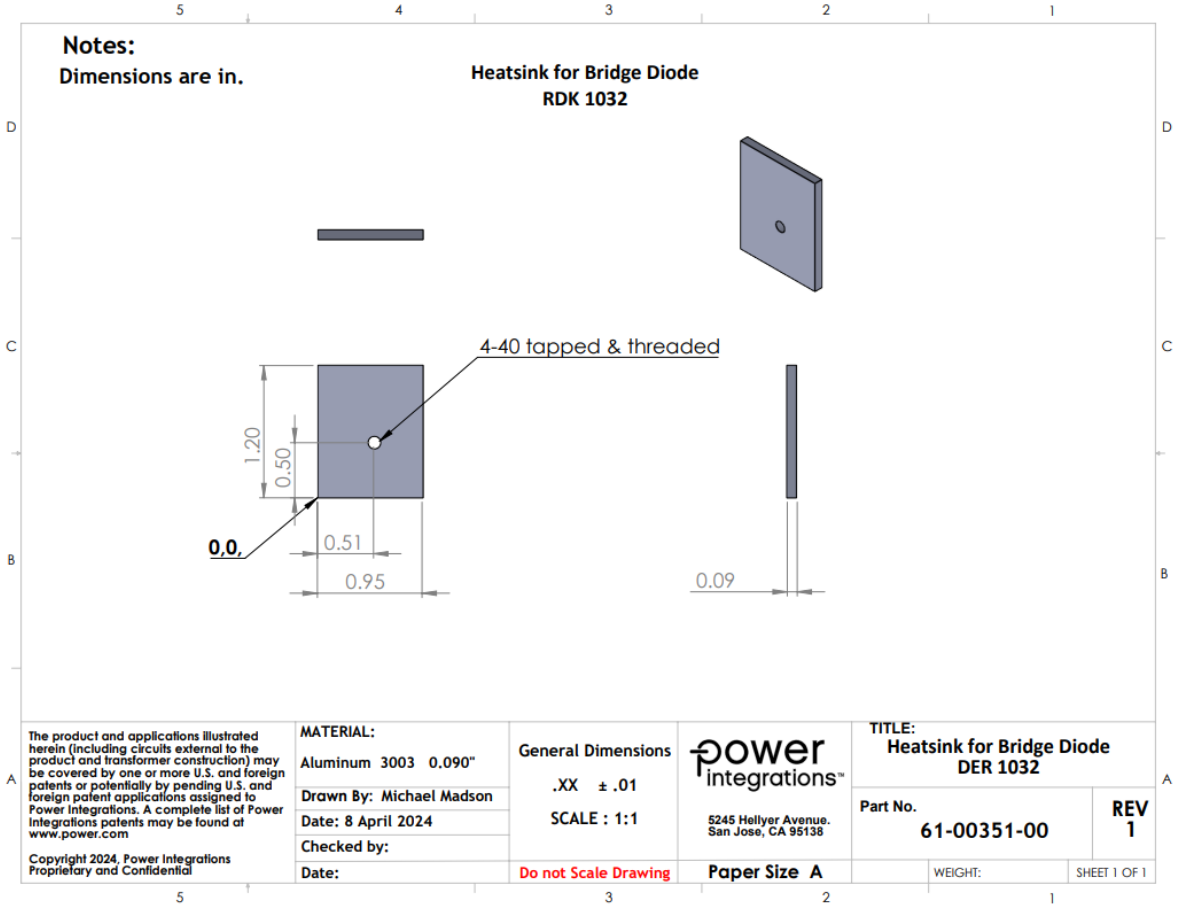
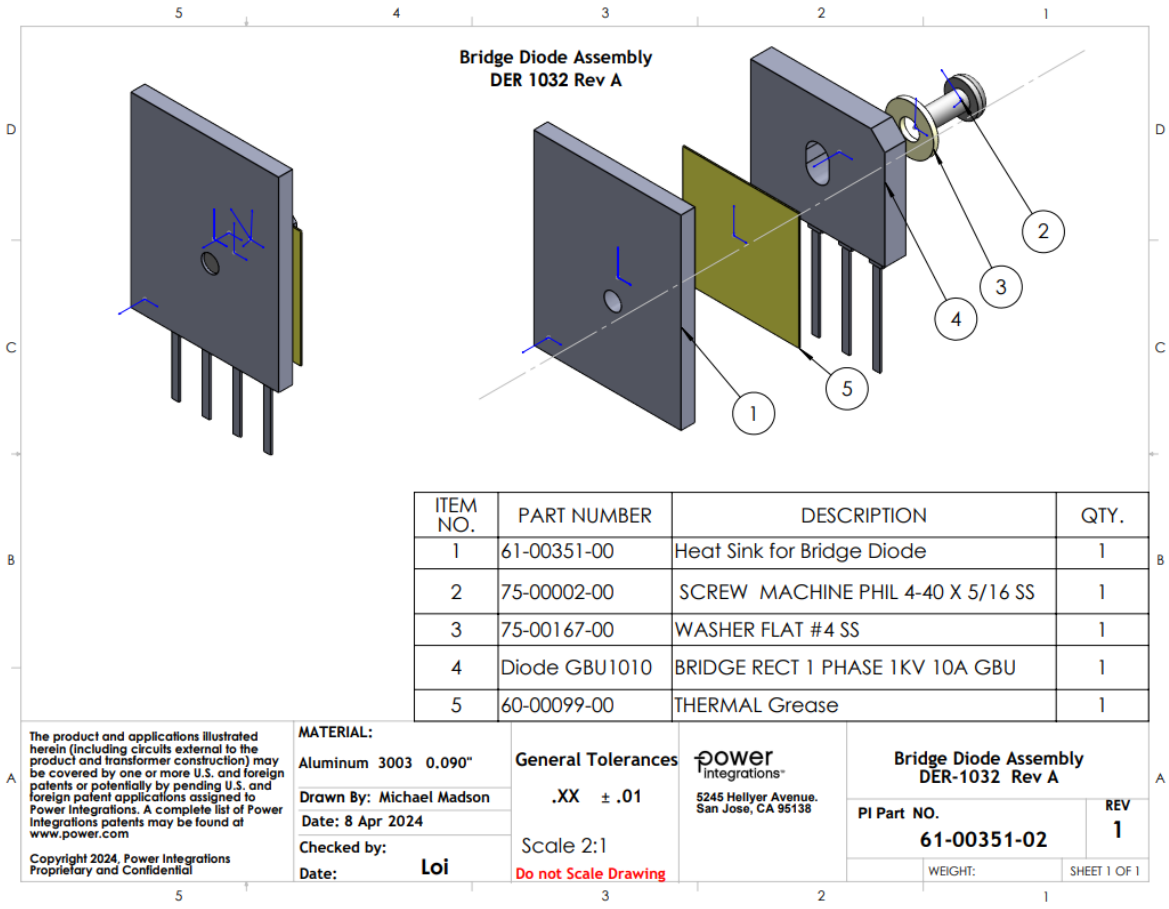


Figure 8 – DER-1032 Bridge Diode Heatsink Sheet Metal Drawing.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00351-00	Heat Sink for Bridge Diode	1
2	75-00002-00	SCREW MACHINE PHIL 4-40 X 5/16 SS	1
3	75-00167-00	WASHER FLAT #4 SS	1
4	Diode GBU1010	BRIDGE RECT 1 PHASE 1KV 10A GBU	1
5	60-00099-00	THERMAL Grease	1

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com

Copyright 2024, Power Integrations Proprietary and Confidential

MATERIAL: Aluminum 3003 0.090"

Drawn By: Michael Madson

Date: 8 Apr 2024

Checked by:

Date: Loi

General Tolerances .XX ± .01

Scale 2:1

Do not Scale Drawing

power integrations

5245 Hellyer Avenue. San Jose, CA 95138

Bridge Diode Assembly DER-1032 Rev A

PI Part NO. 61-00351-02

REV 1

WEIGHT:

SHEET 1 OF 1

Figure 9 – DER-1032 Bridge Diode Heatsink Assembly.

8 Transformer Specification

8.1 Electrical Diagram

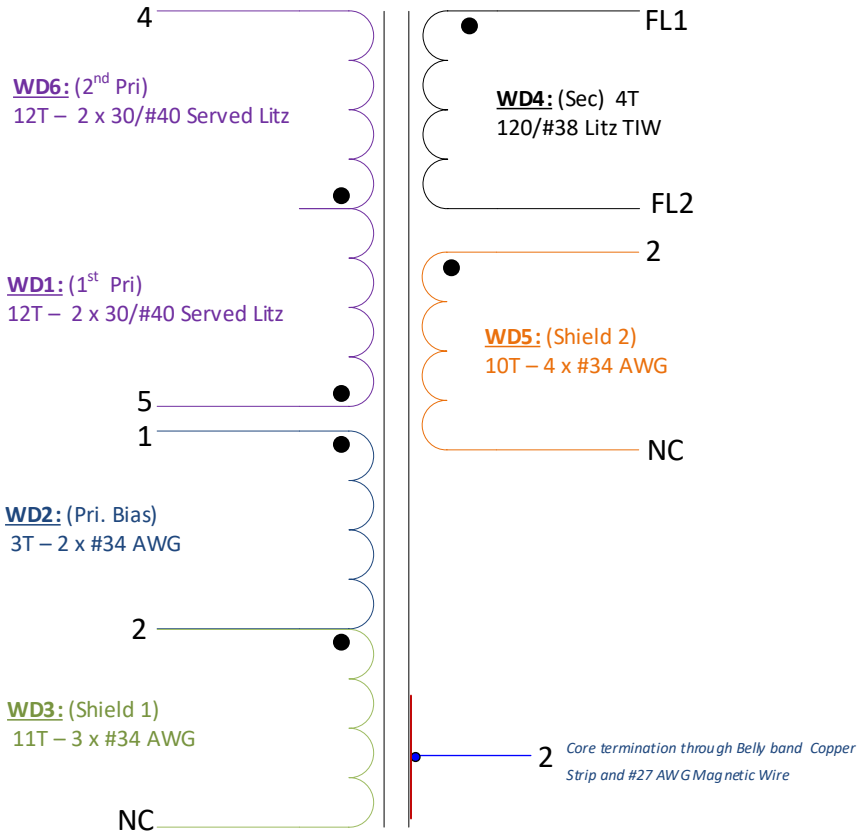


Figure 10 – Electrical Diagram.

8.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between Pin 4 and Pin 5, with all other windings open.	335 µH ± 5%
Resonant Frequency	Measured between Pin 4 and Pin 5, other windings open.	1500 kHz (Nominal)
Primary Leakage Inductance	Measured between Pin 4 and Pin 5, with all other windings shorted.	4 µH ± 10% (Max).

8.3 Materials List

Item	Description
[1]	Core: ATQ28/18 PI#: 99-00071-00.
[2]	Bobbin: Bobbin, ATQ28/18, Vertical, 5pins (5/0), PI#: 25-01170-00.
[3]	Magnet wire: 30/#40 Served Litz.
[4]	Magnet wire: #34 AWG, double coated.
[5]	Magnet wire: #27 AWG, double coated.
[6]	Magnet wire: 120/#38 Litz Triple Insulated Wire.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 8.6 mm width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 12.0 mm width.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 65 mm x 33 mm.
[10]	Copper Foil tape: 2 mil thick, 9.5 mm (3/8”).
[11]	Varnish: Dolph BC-359.

8.4 Transformer Build Diagram

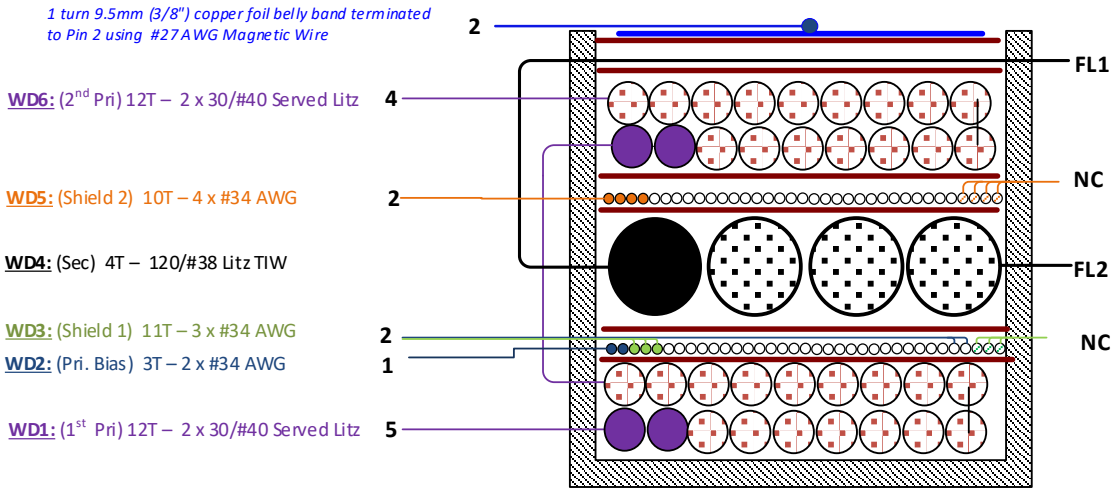
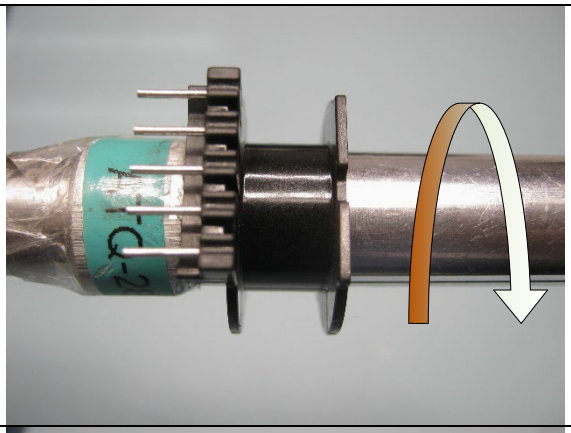
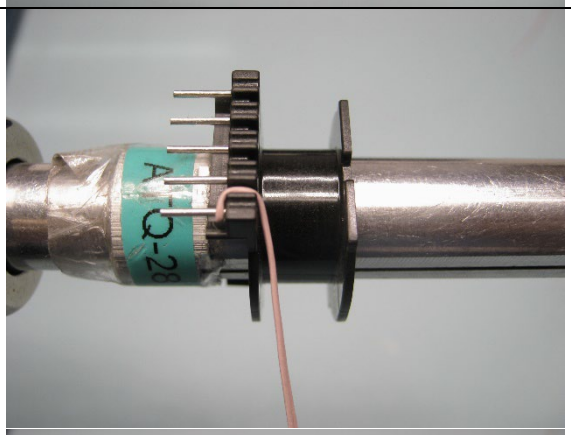
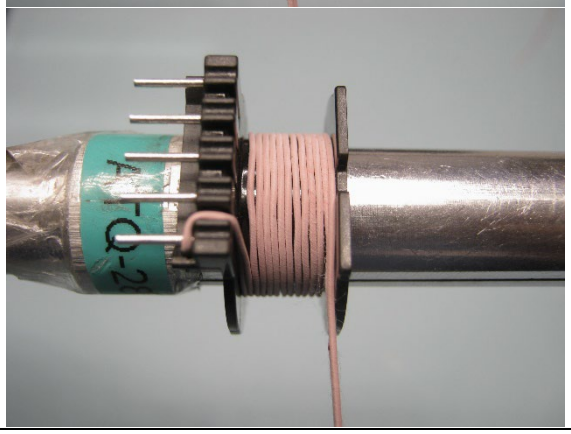


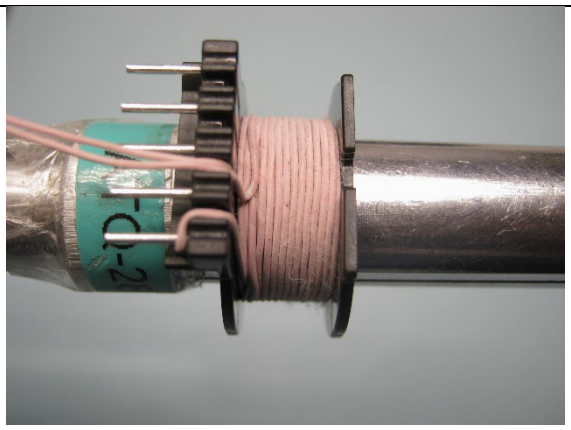
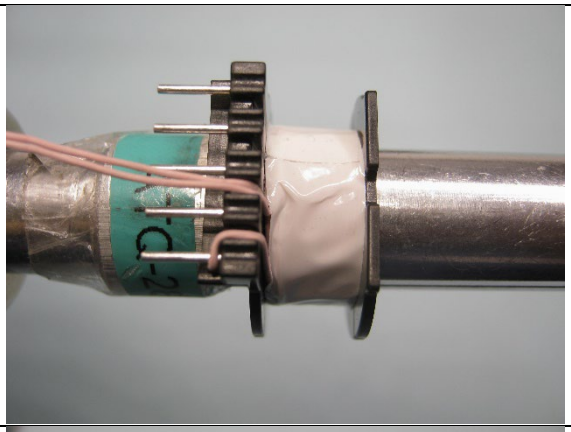
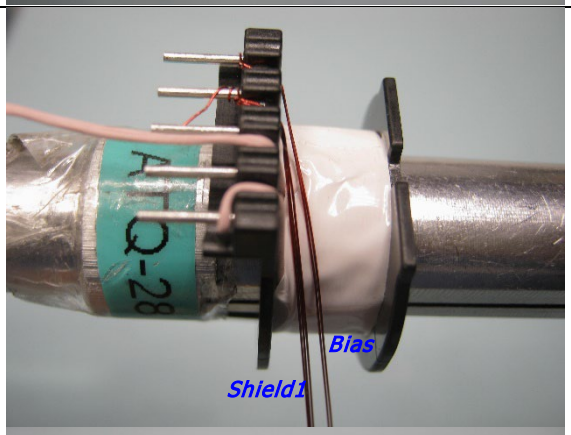
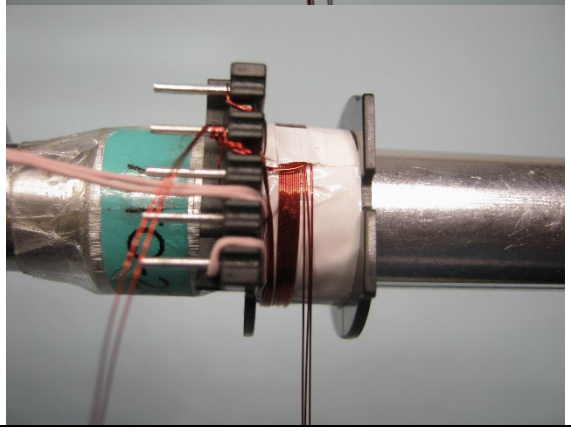
Figure 11 – Transformer Build Diagram.

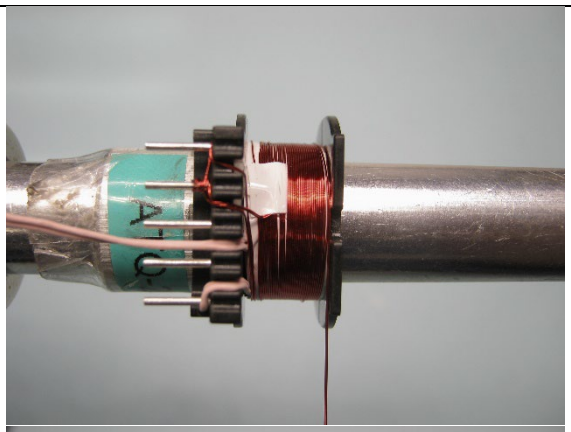
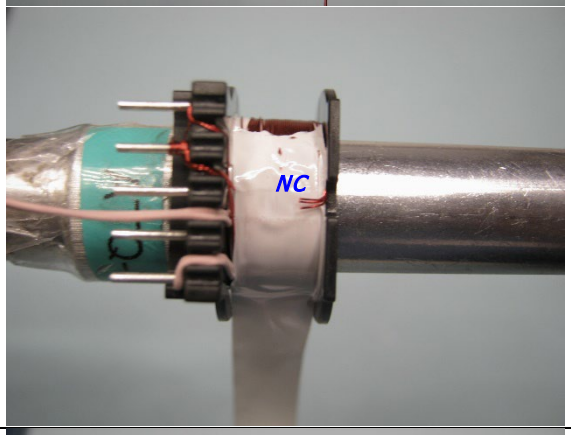
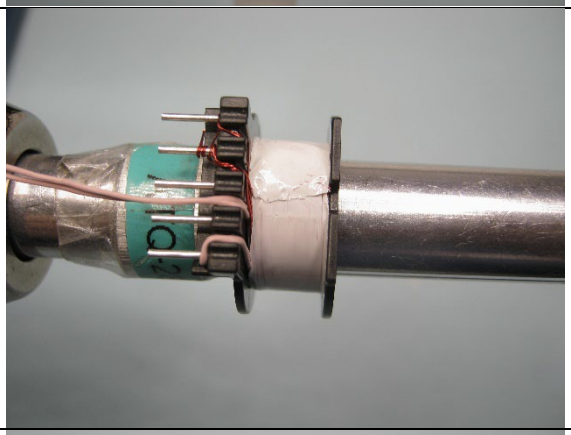
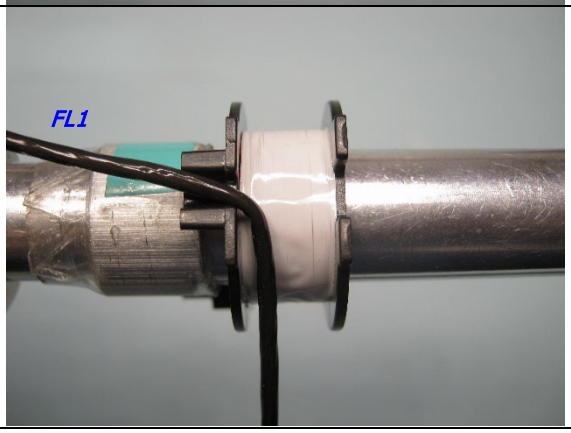
8.5 Transformer Instruction

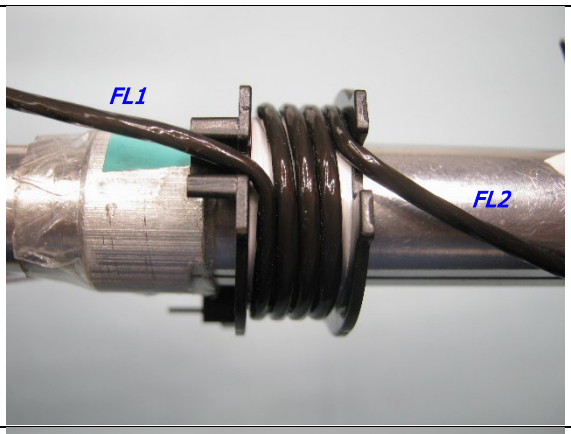
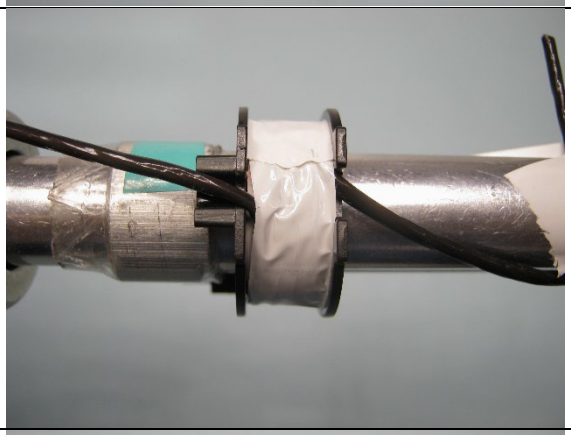
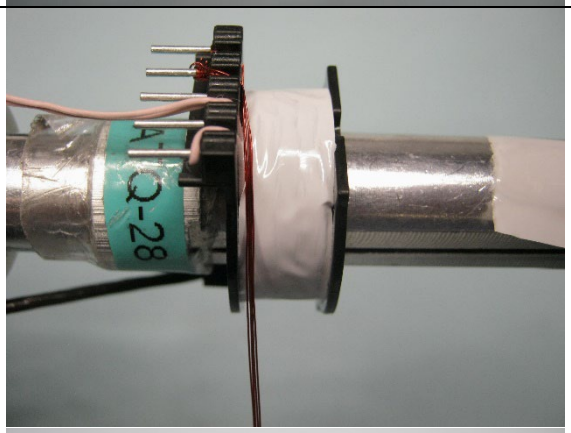
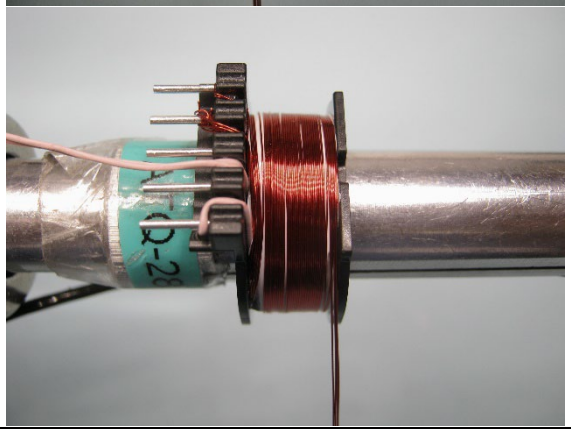
Winding preparation	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1: 1st Primary	Start at pin 5, wind 12 bifilar turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2nd Primary.
Insulation	1 layer of tape Item [7].
WD2: Primary Bias & WD3: Shield1	Use 2 wires Item [4] start at pin 1 for Bias winding, also use 3 wires same Item [4] start at pin 2 for Shield1 winding. Wind all 5 wires in parallel, at the 3rd turn: - bring 2 wires for Primary Bias winding to the left and terminate at pin 2, - continue winding 8 more turns and cut short 3 wires as no connect for Shield1 winding.
Insulation	1 layer of tape Item [7].
WD4: Secondary	Start at left slot of secondary side, use wire Item [6], leaving ~ 40 mm floating, and mark as FL1. Wind 4 turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 32 mm floating, and mark FL2.
Insulation	1 layer of tape Item [7].
WD5: Shield2	Start at pin 2, wind 10 quad-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape Item [7].
WD6: 2nd Primary	Use floating wire from WD1-1st Primary, wind 12 bi-filar turns in 2 layers, from right to left and left to right. At the last turn, finish at pin 4.
Insulation	Secure WD6 2nd Primary with 1 layer of tape Item [7]. Bring floating wire marked as FL1 from Secondary winding to the left and secure with 1 layer of tape Item [7].
Finish	Gap core halves to get 335 μH and secure with tape Item [8]. Wrap around transformer 1 layer of copper foil Item [10], solder at joint to make a closed loop, and solder pin 2 with wire Item [5] to copper foil. Varnish with Item [11]. Place 2 layers of tape Item [9] at the bottom and top then wrap up to the transformer body, and tape around 1 layer of tape Item [8]. Remove Pin 3.

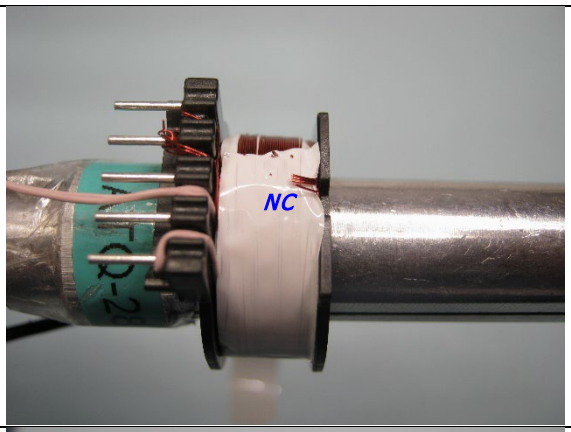
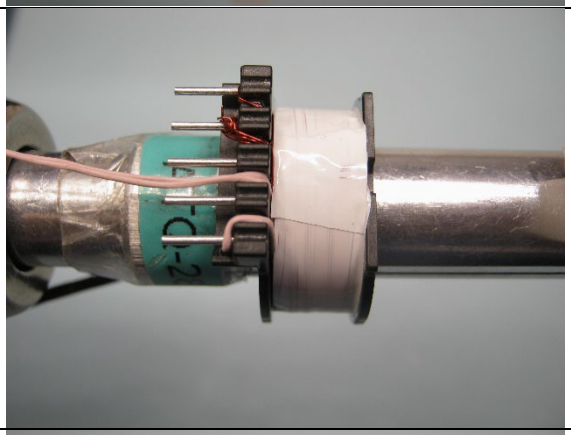
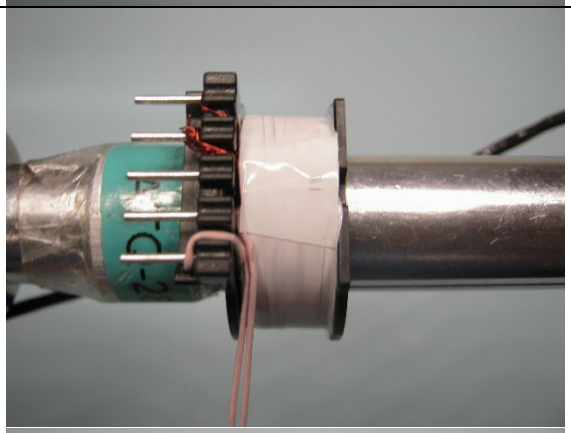
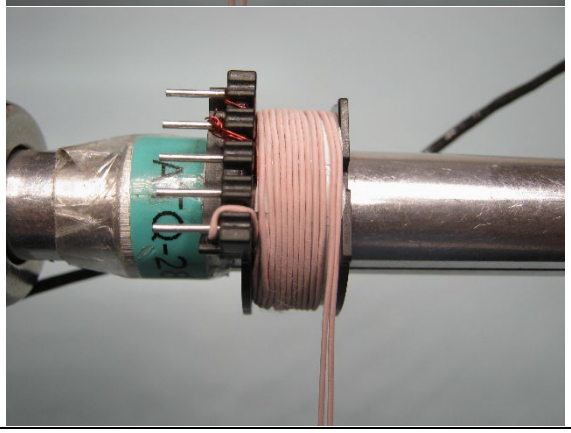
8.6 Winding Illustrations

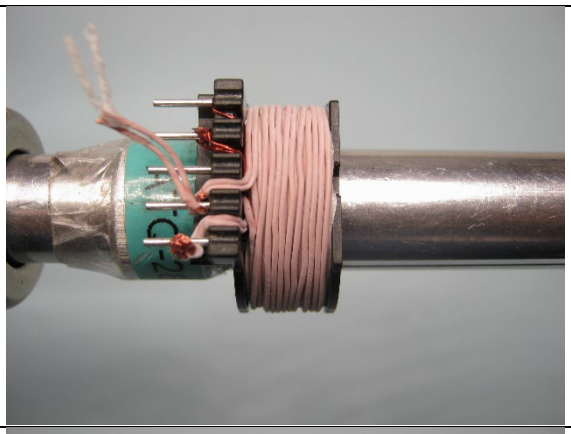
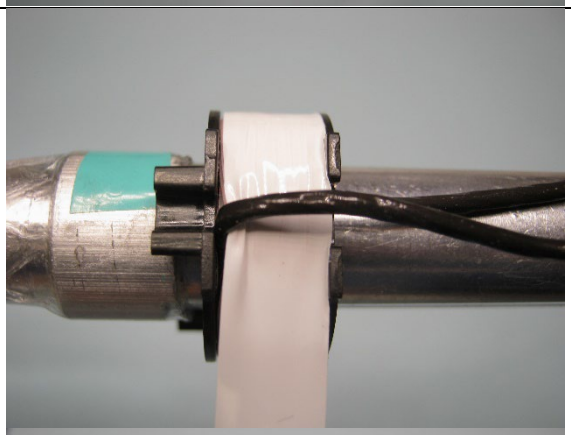
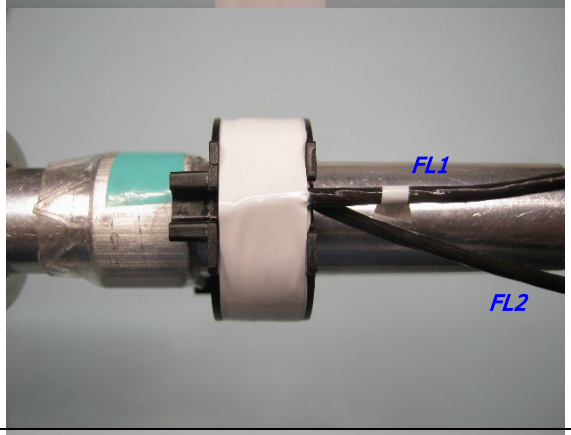
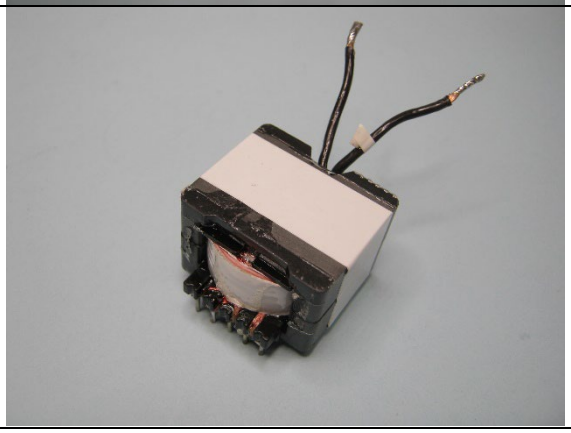
Winding preparation		Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1: **1st Primary**	 	Start at pin 5, wind 12 bifilar turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2nd Primary.

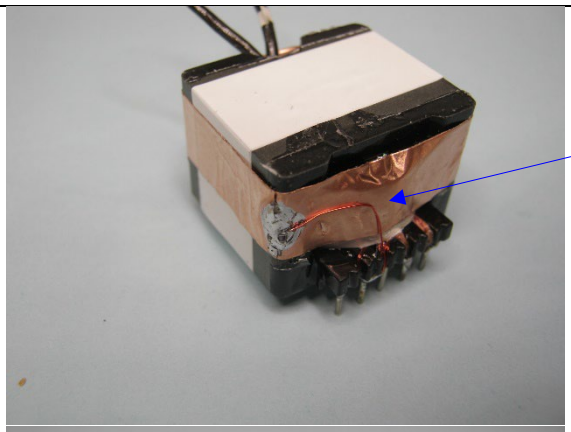
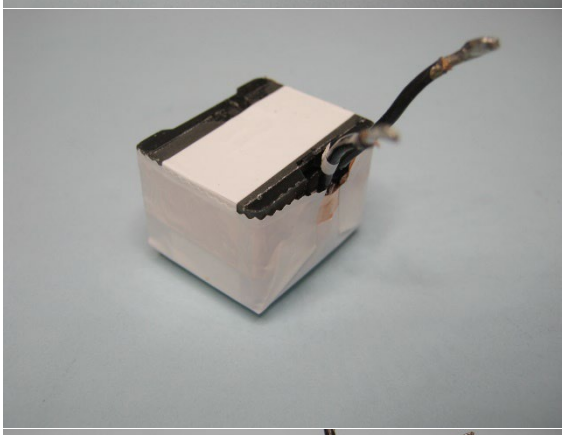
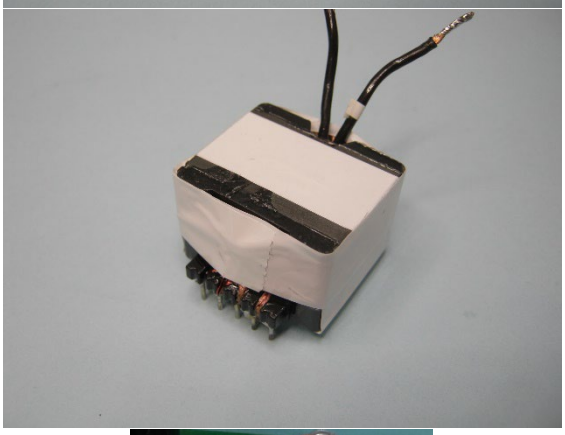
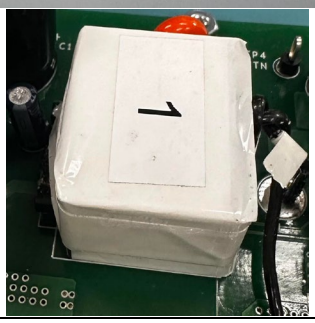
		
Insulation		1 layer of tape Item [7].
WD2: Primary Bias **&** **WD3: Shield1**	 	Use 2 wires Item [4] start at pin 1 for Bias winding, also use 3 wires same Item [4] start at pin 2 for Shield1 winding. Wind all 5 wires in parallel, at the 3rd turn: - bring 2 wires for Primary Bias winding to the left and terminate at pin 2, - continue winding 8 more turns and cut short 3 wires as no connect for Shield1 winding.

	 	
Insulation		1 layer of tape Item [7].
WD4: Secondary		Start at left slot of secondary side, use wire Item [6], leaving ~ 40 mm floating, and mark as FL1. Wind 4 turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 32 mm floating, and mark FL2.

		
Insulation		1 layer of tape Item [7].
WD5: Shield2	 	Start at pin 2, wind 10 quad-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.

		
Insulation		1 layer of tape Item [7].
WD6: **2nd Primary**	 	Use floating wire from WD1-1st Primary, wind 12 bi-filar turns in 2 layers, from right to left and left to right. At the last turn, finish at pin 4.

		
Insulation	 	Secure WD6 2nd Primary with 1 layer of tape Item [7]. Bring floating wire marked as FL1 from Secondary winding to the left and secure with 1 layer of tape Item [7].
Finish		Gap core halves to get 335 μH and secure with tape Item [8]. Wrap around transformer 1 layer of copper foil Item [10], solder at joint to make a closed loop, and solder pin 2 with wire item [5] to copper foil. Varnish with Item [11].

	   	Place 2 layers of tape Item [9] at the bottom and top then wrap up to the transformer body, and tape around 1 layer of tape Item [8]. Remove Pin 3. (See pictures beside).

9 Transformer Design Spreadsheet – 120 W

1	ACDC_InnoSwitch4-QR_Flyback_050823; Rev.0.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4 QR Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN			90	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	480.0		480.0	µF	Input capacitor
9	VOUT	24.00		24.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	5.000		5.000	A	Output current
12	POUT			120.00	W	Output power
13	EFFICIENCY	0.94		0.94		AC-DC efficiency estimates at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
16	**PRIMARY CONTROLLER SELECTION**					
17	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
18	DEVICE_GENERIC	INN4277		INN4277		Generic device code
19	DEVICE_CODE			INN4277C		Actual device code
20	POUT_MAX			135	W	Power capability of the device based on thermal performance
21	RDSON_100DEG			0.29	Ω	Primary switch on time drain resistance at 100 °C
22	ILIMIT_MIN			3.162	A	Minimum current limit of the primary switch
23	ILIMIT_TYP			3.400	A	Typical current limit of the primary switch
24	ILIMIT_MAX			3.638	A	Maximum current limit of the primary switch
25	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
26	VDRAIN_ON_PRSW			0.32	V	Primary switch on time drain voltage
27	VDRAIN_OFF_PRSW			547.4	V	Peak drain voltage on the primary switch during turn-off
28	**WORST CASE ELECTRICAL PARAMETERS**					
29	FSWITCHING_MAX	87000		87000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
30	VOR	144.0		144.0	V	Secondary voltage reflected to the primary when the primary switch turns off
31	VMIN			111.57	V	Valley of the minimum input AC voltage at full load
32	KP			0.72		Measure of continuous/discontinuous mode of operation
33	MODE_OPERATION			CCM		Mode of operation
34	DUTYCYCLE			0.564		Primary switch duty cycle
35	TIME_ON			10.37	µs	Primary switch on-time is greater than 10.5 µs: Increase the controller switching frequency or

						increase the VOR NOTE: Actual operation limits TIME_ON to ton (max) and FSWITCHING will increase. Measured maximum FSW on board is around 80 kHz less than fOVL.
36	TIME_OFF			5.01	µs	Primary switch off-time
37	LPRIMARY_MIN			318.5	µH	Minimum primary inductance
38	LPRIMARY_TYP			335.2	µH	Typical primary inductance
39	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
40	LPRIMARY_MAX			352.0	µH	Maximum primary inductance
41	**PRIMARY CURRENT**					
42	IPEAK_PRIMARY			3.465	A	Primary switch peak current
43	IPEDESTAL_PRIMARY			0.880	A	Primary switch current pedestal
44	IAVG_PRIMARY			1.120	A	Primary switch average current
45	IRIPPLE_PRIMARY			2.959	A	Primary switch ripple current
46	IRMS_PRIMARY			1.623	A	Primary switch RMS current
47	**SECONDARY CURRENT**					
48	IPEAK_SECONDARY			20.788	A	Secondary winding peak current
49	IPEDESTAL_SECONDARY			5.280	A	Secondary winding current pedestal
50	IRMS_SECONDARY			8.561	A	Secondary winding RMS current
51	**TRANSFORMER CONSTRUCTION PARAMETERS**					
52	**CORE SELECTION**					
53	CORE	ATQ28/18.1B		ATQ28/18.1B		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
54	CORE CODE			ATQ28/18.1B		Core code
55	AE			153.00	mm^2	Core cross sectional area
56	LE			47.70	mm	Core magnetic path length
57	AL			9800	nH/turns^2	Ungapped core effective inductance
58	VE			7298.0	mm^3	Core volume
59	BOBBIN			TBI-238-07271.17XX		Bobbin
60	AW			37.40	mm^2	Window area of the bobbin
61	BW			8.50	mm	Bobbin width
62	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
63	**PRIMARY WINDING**					
64	NPRIMARY			24		Primary turns
65	BPEAK			3637	Gauss	Peak flux density
66	BMAX			3283	Gauss	Maximum flux density
67	BAC			1380	Gauss	AC flux density (0.5 x Peak to Peak)
68	ALG			582	nH/turns^2	Typical gapped core effective inductance
69	LG			0.311	mm	Core gap length
70	**PRIMARY BIAS WINDING**					
71	NBIAS_PRIMARY			3		Primary bias winding number of turns
72	**SECONDARY WINDING**					
73	NSECONDARY	4		4		Secondary winding number of turns
74	**SECONDARY BIAS WINDING**					
75	NBIAS_SECONDARY			NA		Secondary bias winding number of turns
76	**PRIMARY COMPONENTS SELECTION**					
77	**LINE UNDERVOLTAGE**					

78	BROWN-IN REQURED	72.30		72.30	V	Required AC RMS/DC line voltage brown-in threshold
79	RLS			3.74	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
80	BROWN-IN ACTUAL			61.9 V - 74.9 V	V	Actual AC RMS/DC brown-in range
81	BROWN-OUT ACTUAL			55.1 V - 68.2 V	V	Actual AC RMS/DC brown-out range
82	**LINE OVERVOLTAGE**					
83	OVERVOLTAGE_LINE			279 V - 316.6 V	V	Actual AC RMS/DC line over-voltage range
84	**PRIMARY BIAS DIODE**					
85	VBIAS_PRIMARY			12.0	V	Rectified primary bias voltage
86	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
87	VREVERSE_BIASDIODE_PRIMARY			64.67	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
88	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
89	CBPP			0.47	µF	BPP pin capacitor
90	**SECONDARY COMPONENTS**					
91	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
92	RFB_LOWER			5.62	kΩ	Lower feedback resistor
93	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
94	**SECONDARY BIAS DIODE**					
95	USE_SECONDARY_BIAS	NO		NO		Use secondary bias winding for the design
96	VBIAS_SECONDARY			NA	V	Rectified secondary bias voltage
97	VF_BIAS_SECONDARY			NA	V	Bias winding diode forward drop
98	VREVERSE_BIASDIODE_SECONDARY			NA	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
99	CBIAS_SECONDARY			NA	µF	Bias winding rectification capacitor
100	CBPS			NA	µF	BPP pin capacitor
101	**MULTIPLE OUTPUT PARAMETERS**					
102	OUTPUT 1					
103	VOUT1			24.00	V	Output 1 voltage
104	IOUT1			5.00	A	Output 1 current
105	POUT1			120.00	W	Output 1 power
106	IRMS_SECONDARY1			8.561	A	Root mean squared value of the secondary current for output 1
107	IRIPPLE_CAP_OUTPUT1			6.949	A	Current ripple on the secondary waveform for output 1
108	NSECONDARY1			4		Number of turns for output 1
109	VREVERSE_RECTIFIER1			86.23	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 1
110	SRFET1	AOB2500L		AOB2500L		Secondary rectifier (Logic MOSFET) for output 1
111	VF_SRFET1			0.054	V	SR FET on-time drain voltage for output 1
112	VBREAKDOWN_SRFET1			150	V	SR FET breakdown voltage for output 1
113	RDSON_SRFET1			5.1	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1
114	**OUTPUT 2**					
115	VOUT2			0.00	V	Output 2 voltage
116	IOUT2			0.000	A	Output 2 current

117	POUT2			0.00	W	Output 2 power
118	IRMS_SECONDARY2			0.000	A	Root mean squared value of the secondary current for output 2
119	IRIPPLE_CAP_OUTPUT2			0.000	A	Current ripple on the secondary waveform for output 2
120	NSECONDARY2			0		Number of turns for output 2
121	VREVERSE_RECTIFIER2			0.00	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 2
122	SRFET2	Auto		NA		Secondary rectifier (Logic MOSFET) for output 2
123	VF_SRFET2			NA	V	SR FET on-time drain voltage for output 2
124	VBREAKDOWN_SRFET2			NA	V	SR FET breakdown voltage for output 2
125	RDSON_SRFET2			NA	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 2
126	**OUTPUT 3**					
127	VOUT3			0.00	V	Output 3 voltage
128	IOUT3			0.000	A	Output 3 current
129	POUT3			0.00	W	Output 3 power
130	IRMS_SECONDARY3			0.000	A	Root mean squared value of the secondary current for output 3
131	IRIPPLE_CAP_OUTPUT3			0.000	A	Current ripple on the secondary waveform for output 3
132	NSECONDARY3			0		Number of turns for output 3
133	VREVERSE_RECTIFIER3			0.00	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 3
134	SRFET3	Auto		NA		Secondary rectifier (Logic MOSFET) for output 3
135	VF_SRFET3			NA	V	SR FET on-time drain voltage for output 3
136	VBREAKDOWN_SRFET3			NA	V	SR FET breakdown voltage for output 3
137	RDSON_SRFET3			NA	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 3
138	PO_TOTAL			120.00	W	Total power of all outputs
139	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 has negative output, select 2

10 Transformer Design Spreadsheet – 150 W Peak

1	ACDC_InnoSwitch4-QR_Flyback_050823; Rev.0.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4 QR Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN			90	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	480.0		480.0	µF	Input capacitor
9	VOUT	24.00		24.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	6.250		6.250	A	Output current
12	POUT			150.00	W	Output power
13	EFFICIENCY	0.94		0.94		AC-DC efficiency estimates at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
16	**PRIMARY CONTROLLER SELECTION**					
17	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
18	DEVICE_GENERIC	INN4277		INN4277		Generic device code
19	DEVICE_CODE			INN4277C		Actual device code
20	POUT_MAX			135	W	Power capability of the device based on thermal performance
21	RDSON_100DEG			0.29	Ω	Primary switch on time drain resistance at 100 °C
22	ILIMIT_MIN			3.162	A	Minimum current limit of the primary switch
23	ILIMIT_TYP			3.400	A	Typical current limit of the primary switch
24	ILIMIT_MAX			3.638	A	Maximum current limit of the primary switch
25	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
26	VDRAIN_ON_PRSW			0.42	V	Primary switch on time drain voltage
27	VDRAIN_OFF_PRSW			547.4	V	Peak drain voltage on the primary switch during turn-off
28	**WORST CASE ELECTRICAL PARAMETERS**					
29	FSWITCHING_MAX	136000		136000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
30	VOR	144.0		144.0	V	Secondary voltage reflected to the primary when the primary switch turns off
31	VMIN			107.93	V	Valley of the minimum input AC voltage at full load
32	KP			0.43		Measure of continuous/discontinuous mode of operation
33	MODE_OPERATION			CCM		Mode of operation
34	DUTYCYCLE			0.573		Primary switch duty cycle
35	TIME_ON			10.34	µs	Primary switch on-time is greater than 10.5 µs: Increase the controller switching frequency or

						increase the VOR NOTE: Actual operation limits TIME_ON to ton(max) and FSWITCHING will increase. Measured maximum FSW on board is around 80 kHz less than fOVL.
36	TIME_OFF			3.14	µs	Primary switch off-time
37	LPRIMARY_MIN			317.4	µH	Minimum primary inductance
38	LPRIMARY_TYP			334.1	µH	Typical primary inductance
39	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
40	LPRIMARY_MAX			350.9	µH	Maximum primary inductance
41	**PRIMARY CURRENT**					
42	IPEAK_PRIMARY			3.602	A	Primary switch peak current
43	IPEDESTAL_PRIMARY			1.835	A	Primary switch current pedestal
44	IAVG_PRIMARY			1.449	A	Primary switch average current
45	IRIPPLE_PRIMARY			2.144	A	Primary switch ripple current
46	IRMS_PRIMARY			1.971	A	Primary switch RMS current
47	**SECONDARY CURRENT**					
48	IPEAK_SECONDARY			21.614	A	Secondary winding peak current
49	IPEDESTAL_SECONDARY			11.008	A	Secondary winding current pedestal
50	IRMS_SECONDARY			10.218	A	Secondary winding RMS current
51	**TRANSFORMER CONSTRUCTION PARAMETERS**					
52	**CORE SELECTION**					
53	CORE	ATQ28/18.1B		ATQ28/18.1B		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
54	CORE CODE			ATQ28/18.1B		Core code
55	AE			153.00	mm^2	Core cross sectional area
56	LE			47.70	mm	Core magnetic path length
57	AL			9800	nH/turns^2	Ungapped core effective inductance
58	VE			7298.0	mm^3	Core volume
59	BOBBIN			TBI-238-07271.17XX		Bobbin
60	AW			37.40	mm^2	Window area of the bobbin
61	BW			8.50	mm	Bobbin width
62	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
63	**PRIMARY WINDING**					
64	NPRIMARY			24		Primary turns
65	BPEAK			3625	Gauss	Peak flux density
66	BMAX			3414	Gauss	Maximum flux density
67	BAC			997	Gauss	AC flux density (0.5 x Peak to Peak)
68	ALG			580	nH/turns^2	Typical gapped core effective inductance
69	LG			0.312	mm	Core gap length
70	**PRIMARY BIAS WINDING**					
71	NBIAS_PRIMARY			3		Primary bias winding number of turns
72	**SECONDARY WINDING**					
73	NSECONDARY	4		4		Secondary winding number of turns
74	**SECONDARY BIAS WINDING**					
75	NBIAS_SECONDARY			NA		Secondary bias winding number of turns
76	**PRIMARY COMPONENTS SELECTION**					
77	**LINE UNDERVOLTAGE**					

78	BROWN-IN REQURED	72.30		72.30	V	Required AC RMS/DC line voltage brown-in threshold
79	RLS			3.74	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
80	BROWN-IN ACTUAL			61.9 V - 74.9 V	V	Actual AC RMS/DC brown-in range
81	BROWN-OUT ACTUAL			55.1 V - 68.2 V	V	Actual AC RMS/DC brown-out range
82	**LINE OVERVOLTAGE**					
83	OVERVOLTAGE_LINE			279 V - 316.6 V	V	Actual AC RMS/DC line over-voltage range
84	**PRIMARY BIAS DIODE**					
85	VBIAS_PRIMARY			12.0	V	Rectified primary bias voltage
86	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
87	VREVERSE_BIASDIODE_PRIMARY			64.67	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
88	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
89	CBPP			0.47	µF	BPP pin capacitor
90	**SECONDARY COMPONENTS**					
91	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
92	RFB_LOWER			5.62	kΩ	Lower feedback resistor
93	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
94	**SECONDARY BIAS DIODE**					
95	USE_SECONDARY_BIAS	NO		NO		Use secondary bias winding for the design
96	VBIAS_SECONDARY			NA	V	Rectified secondary bias voltage
97	VF_BIAS_SECONDARY			NA	V	Bias winding diode forward drop
98	VREVERSE_BIASDIODE_SECONDARY			NA	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
99	CBIAS_SECONDARY			NA	µF	Bias winding rectification capacitor
100	CBPS			NA	µF	BPP pin capacitor
101	**MULTIPLE OUTPUT PARAMETERS**					
102	OUTPUT 1					
103	VOUT1			24.00	V	Output 1 voltage
104	IOUT1			6.25	A	Output 1 current
105	POUT1			150.00	W	Output 1 power
106	IRMS_SECONDARY1			10.218	A	Root mean squared value of the secondary current for output 1
107	IRIPPLE_CAP_OUTPUT1			8.084	A	Current ripple on the secondary waveform for output 1
108	NSECONDARY1			4		Number of turns for output 1
109	VREVERSE_RECTIFIER1			86.23	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 1
110	SRFET1	AOB2500L		AOB2500L		Secondary rectifier (Logic MOSFET) for output 1
111	VF_SRFET1			0.054	V	SR FET on-time drain voltage for output 1
112	VBREAKDOWN_SRFET1			150	V	SR FET breakdown voltage for output 1
113	RDSON_SRFET1			5.1	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1
114	**OUTPUT 2**					
115	VOUT2			0.00	V	Output 2 voltage
116	IOUT2			0.000	A	Output 2 current

117	POUT2			0.00	W	Output 2 power
118	IRMS_SECONDARY2			0.000	A	Root mean squared value of the secondary current for output 2
119	IRIPPLE_CAP_OUTPUT2			0.000	A	Current ripple on the secondary waveform for output 2
120	NSECONDARY2			0		Number of turns for output 2
121	VREVERSE_RECTIFIER2			0.00	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 2
122	SRFET2	Auto		NA		Secondary rectifier (Logic MOSFET) for output 2
123	VF_SRFET2			NA	V	SR FET on-time drain voltage for output 2
124	VBREAKDOWN_SRFET2			NA	V	SR FET breakdown voltage for output 2
125	RDSON_SRFET2			NA	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 2
126	**OUTPUT 3**					
127	VOUT3			0.00	V	Output 3 voltage
128	IOUT3			0.000	A	Output 3 current
129	POUT3			0.00	W	Output 3 power
130	IRMS_SECONDARY3			0.000	A	Root mean squared value of the secondary current for output 3
131	IRIPPLE_CAP_OUTPUT3			0.000	A	Current ripple on the secondary waveform for output 3
132	NSECONDARY3			0		Number of turns for output 3
133	VREVERSE_RECTIFIER3			0.00	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 3
134	SRFET3	Auto		NA		Secondary rectifier (Logic MOSFET) for output 3
135	VF_SRFET3			NA	V	SR FET on-time drain voltage for output 3
136	VBREAKDOWN_SRFET3			NA	V	SR FET breakdown voltage for output 3
137	RDSON_SRFET3			NA	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 3
138	PO_TOTAL			150.00	W	Total power of all outputs
139	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

11 Common Mode Choke (L1) Specification

11.1 Electrical Diagram

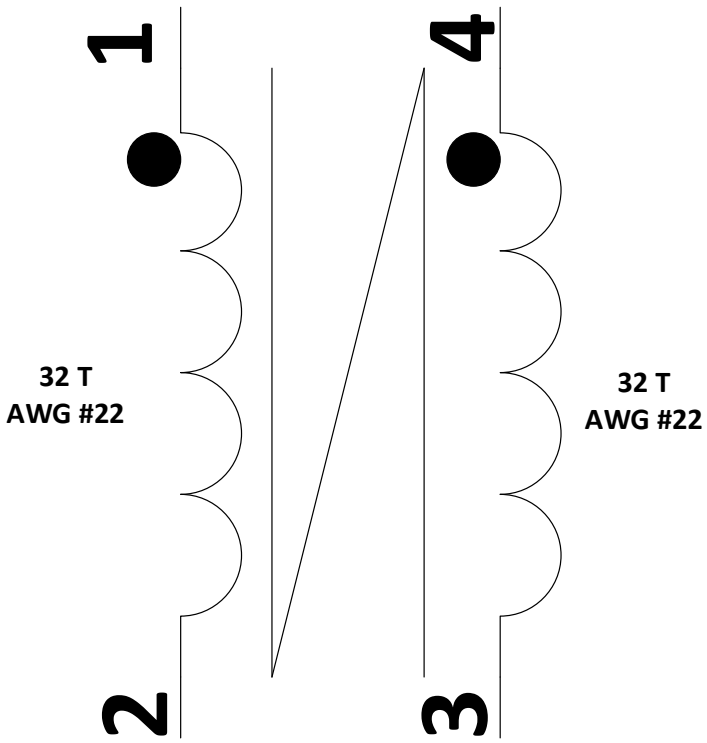


Figure 12 – CMC Electrical Diagram.

11.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and pin 3 or pin 2 and pin 4 with all other windings open.	8 mH
Tolerance	Tolerance of Primary Inductance.	±20%

11.3 Materials

Item	Description
[1]	Toroid Core: 30-00398-00 (Green).
[2]	Magnet Wire: #22 AWG.

11.4 Assembled Picture

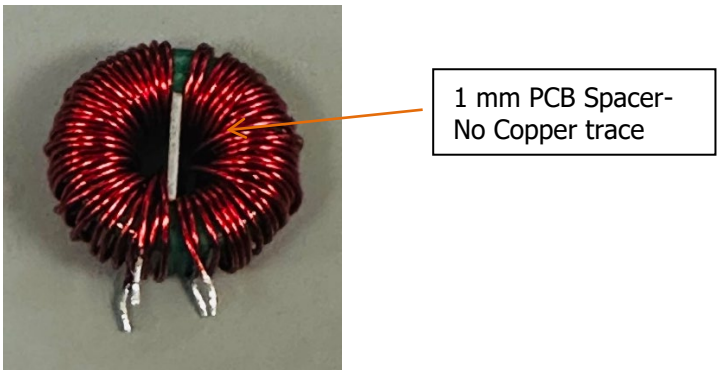


Figure 13 – CMC Assembled Photo.

Diameter: 22 mm
Width: 10 mm

11.5 Inductor Build Diagram

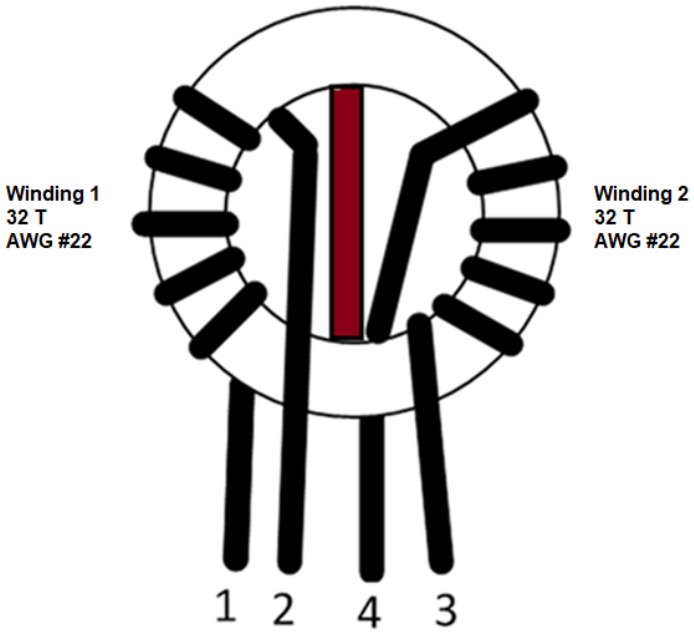


Figure 14 – Inductor Build Diagram.

11.6 Inductor Construction

1. Winding 1 - Wind 32 turns of item 2 as shown in figure 14.
2. Winding 2 - Wind 32 turns of item 2 as shown in figure 14.

12 Performance Data

All the performance data was measured on the board unless otherwise noted.

12.1 Power Meter Setting for Output Load > 5 W

For output power > 5 W the effect of voltage drop along the input cable is significant particularly at low input line. In figure 15 we show the input power meter arrangement recommended for accurate input power measurement.

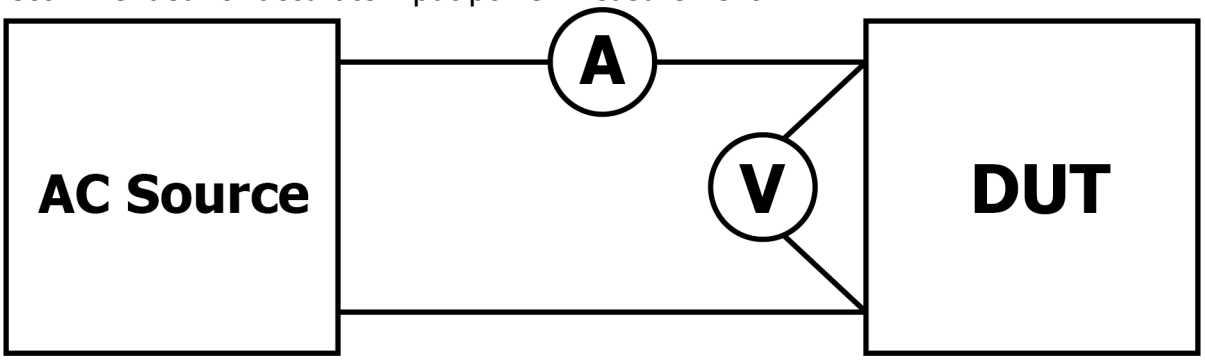


Figure 15 – Input Power meter setting for output load > 5 W.

12.2 Power Meter Setting for Output Load < 5 W

For output power < 5 W the effect of leakage current drawn by the voltmeter is also important, especially at high line. In figure 16 we show the input power meter arrangement recommended for accurate input power measurement.

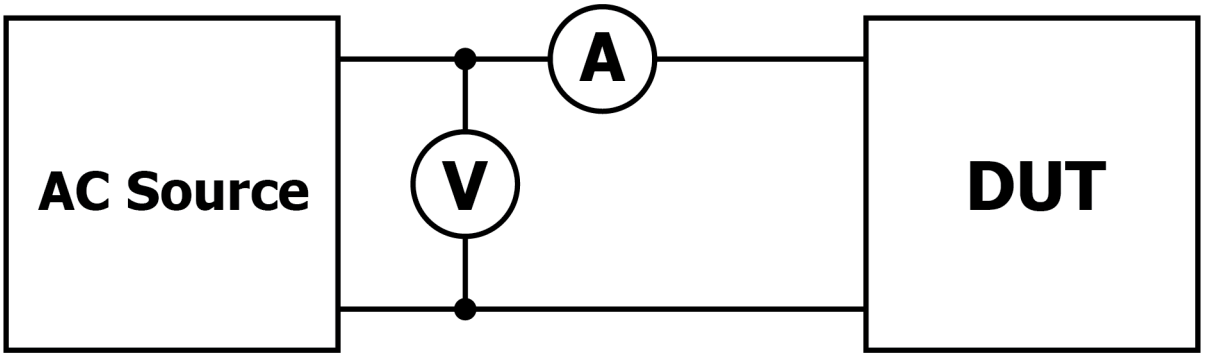


Figure 16 – Input Power meter setting for output load < 5 W.

12.3 Full-load Efficiency vs. Line

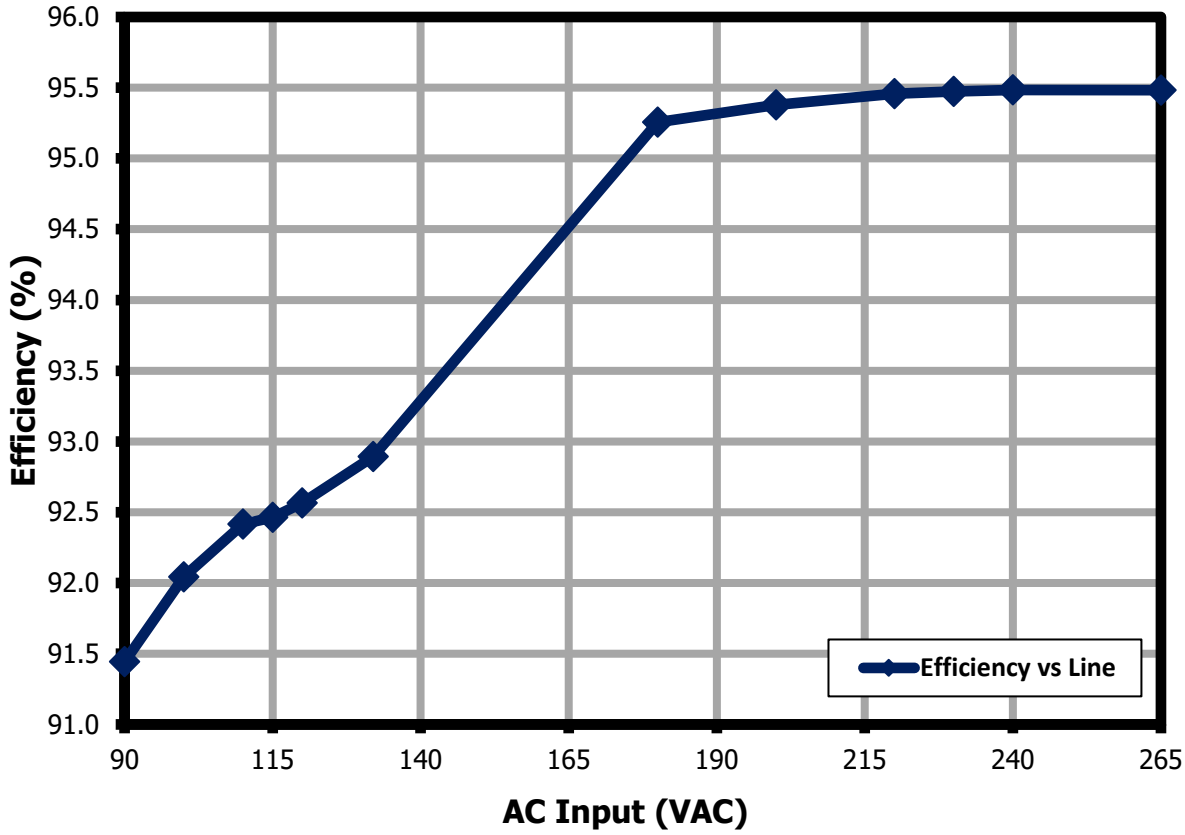


Figure 17 – Full-load Efficiency vs. Line, Room Ambient.

12.4 Efficiency vs. Load

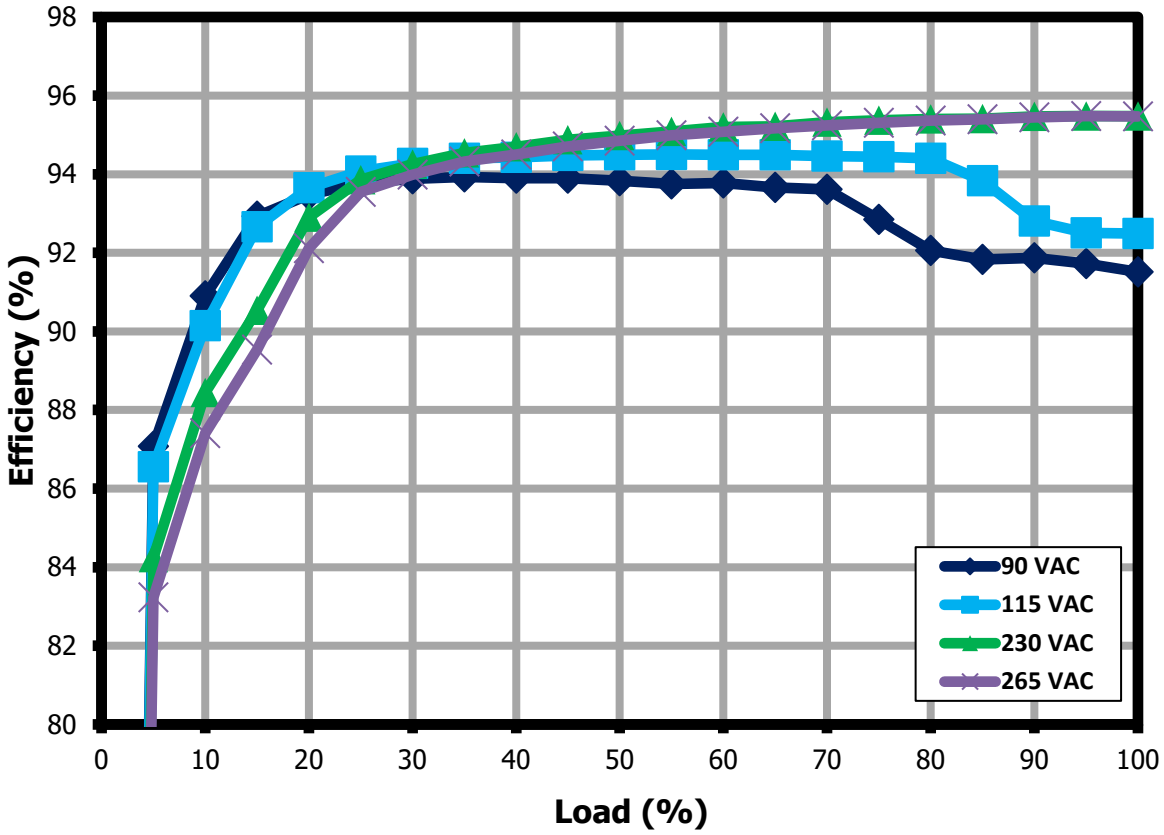


Figure 18 – Efficiency vs. Load, Room Ambient.

12.5 Agency test Limits for Average Efficiency

	Test	Average	Average	10% Load
Output Voltage (V)	Power [W]	DOE6 Limit (%)	CoC v5 Tier 2 (%)	CoC v5 Tier 2 (%)
24	120	88.0	89.0	79.0

12.6 Average and 10% Efficiency at 90 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	132	121	91.7	93.1
75	98	91	92.9	
50	64.6	60.6	93.8	
25	32.4	30.4	93.8	
10	13.3	12.1	91	

12.7 Average and 10% Efficiency at 115 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	131	121	92.4	93.9
75	96.5	91.2	94.5	
50	64.1	60.6	94.5	
25	32.3	30.4	94.1	
10	13.4	12.1	90.3	

12.8 Average and 10% Efficiency at 230 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	127	122	96.1	95.2
75	95.8	91.4	95.4	
50	63.9	60.7	95	
25	32.3	30.4	94.1	
10	13.6	12.1	89	

12.9 Average and 10% Efficiency at 265 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	127	122	96.1	95
75	95.9	91.4	95.3	
50	64.1	60.8	94.9	
25	32.5	30.4	93.5	
10	13.8	12.1	87.7	

12.10 No-Load Input Power

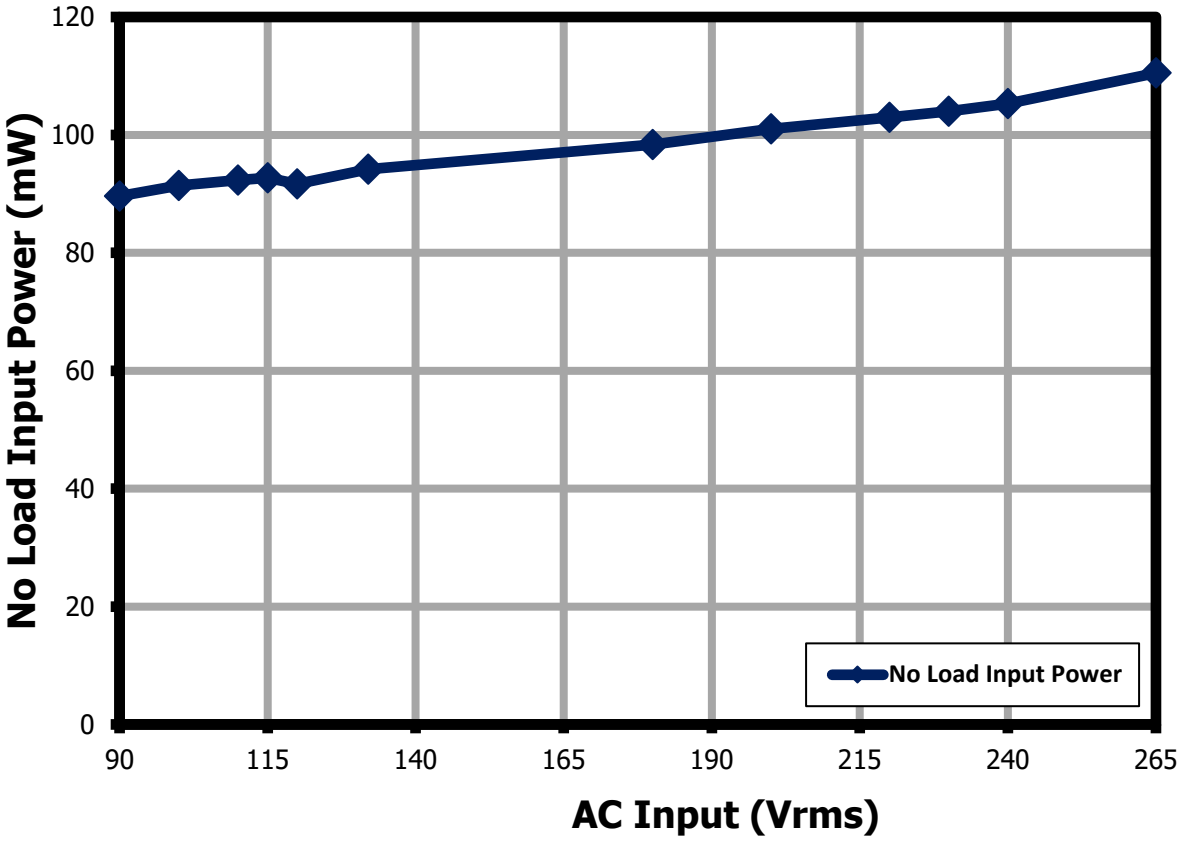


Figure 19 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

12.11 Line Regulation

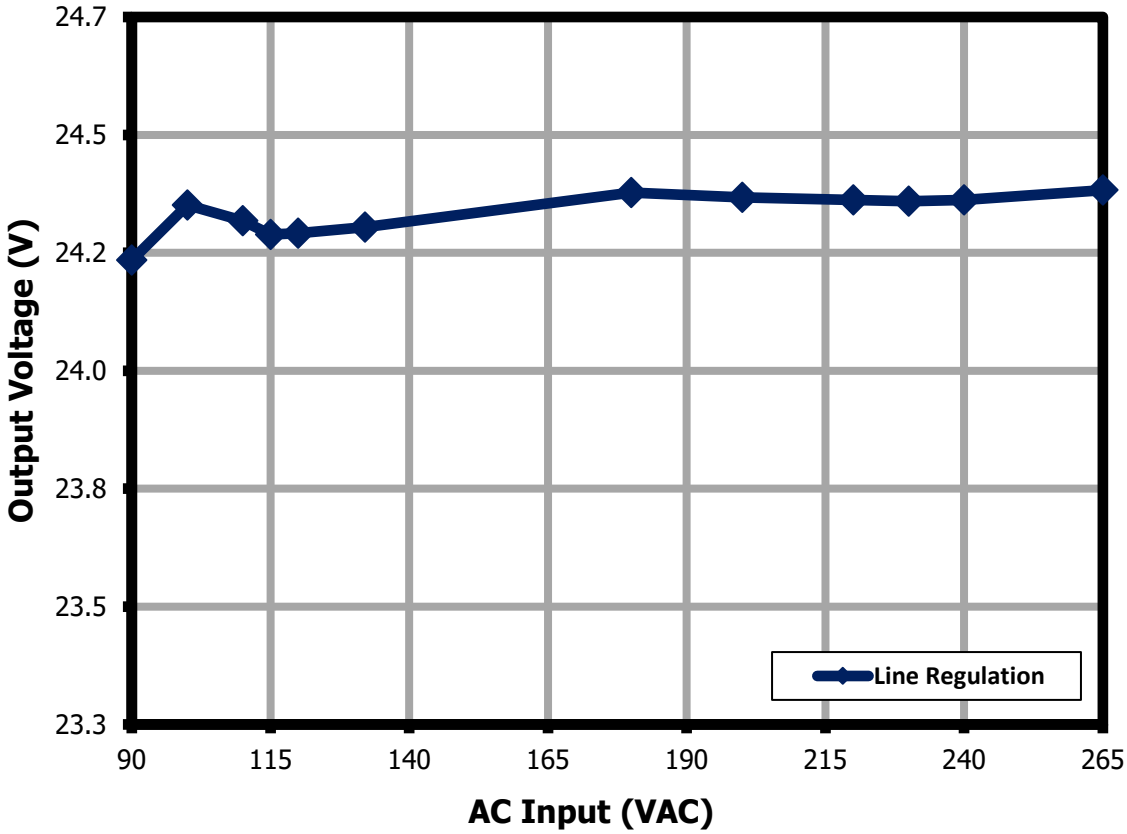


Figure 20 – Line Regulation.

12.12 Load Regulation

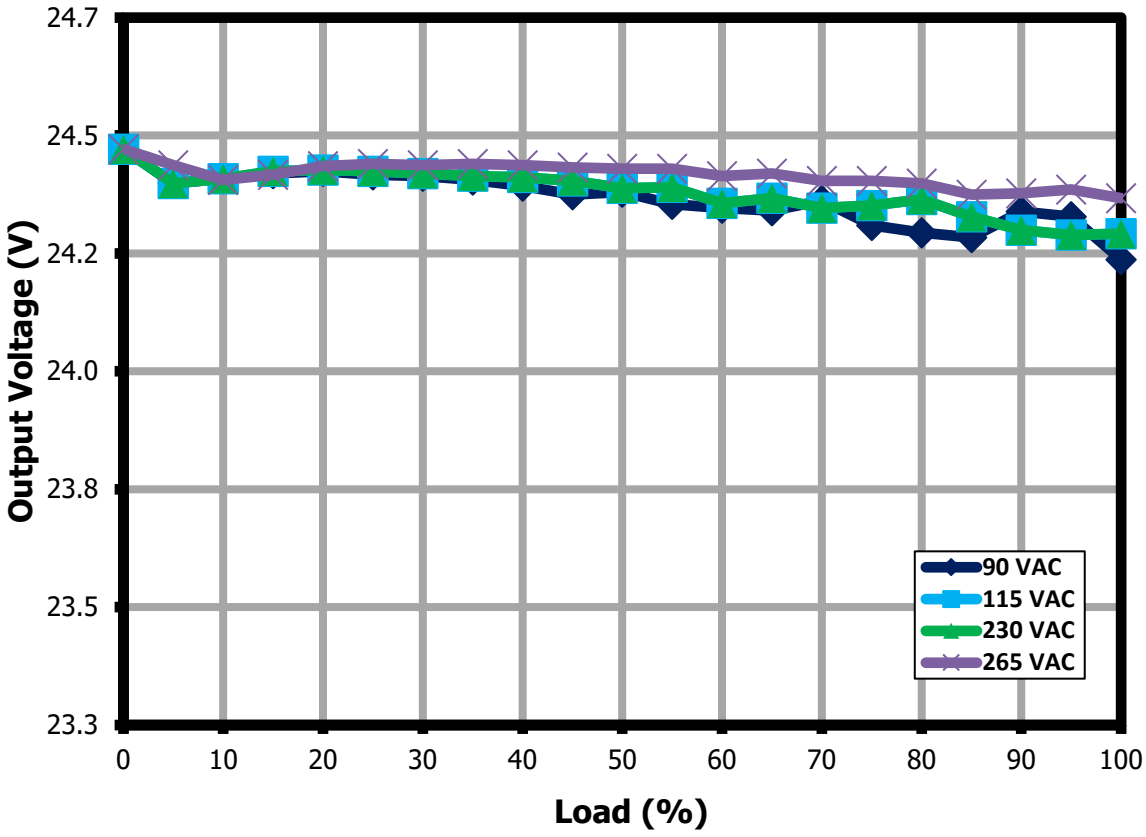


Figure 21 – Load Regulation.

12.13 Standby Efficiency

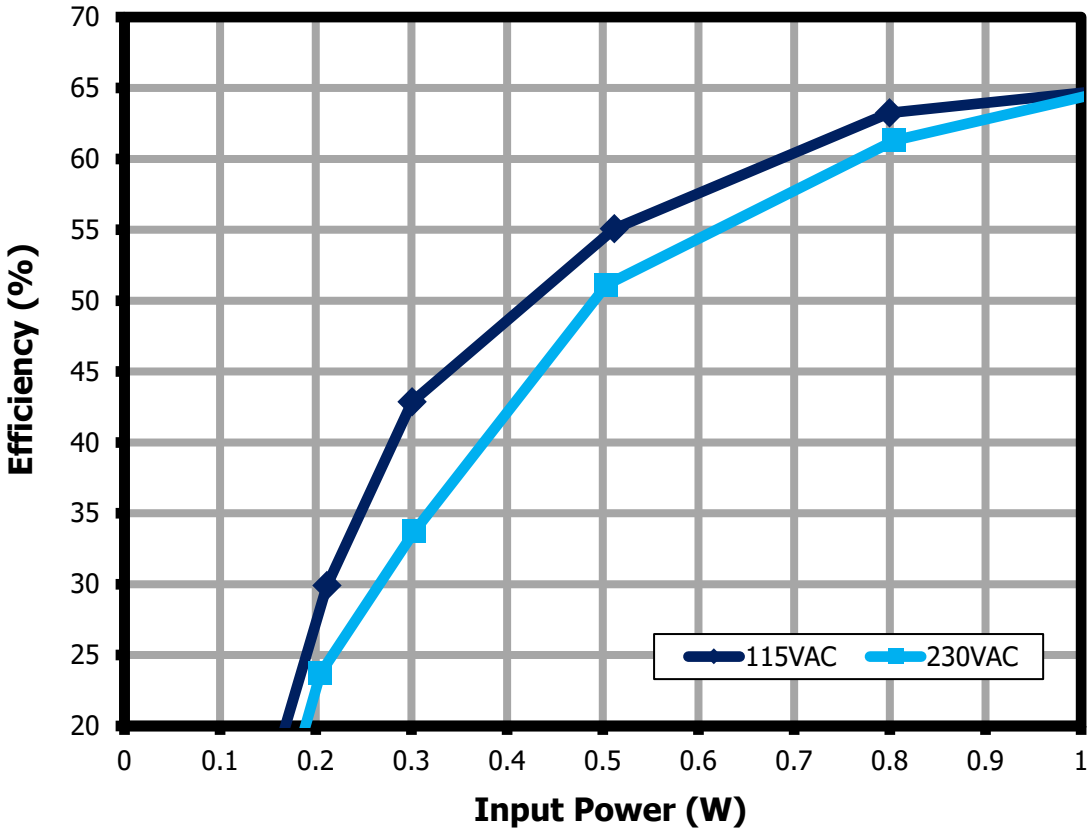


Figure 22 – Efficiency vs. Input Power.

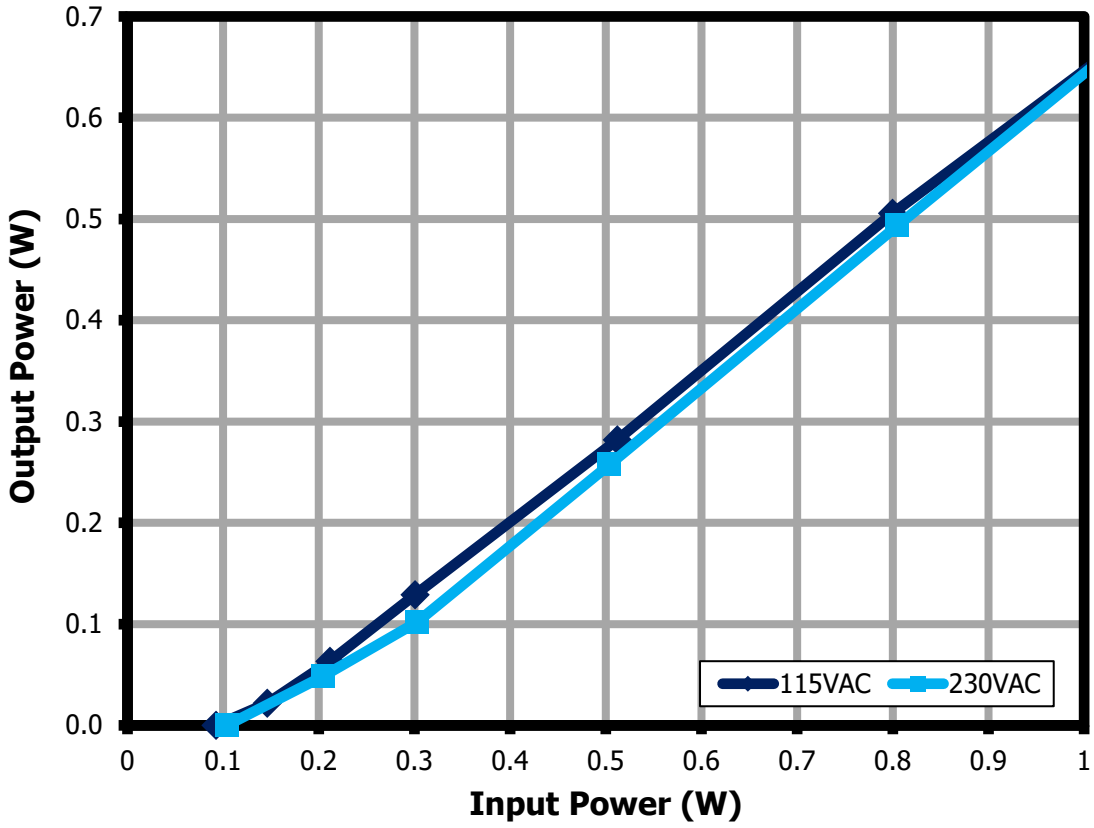


Figure 23 – Output Power vs. Input Power.

13 Thermal Performance

Thermal performance was measured using an IR camera with the unit inside an acrylic box. The unit was soaked and allowed to stabilize for one hour prior to measurements being taken.

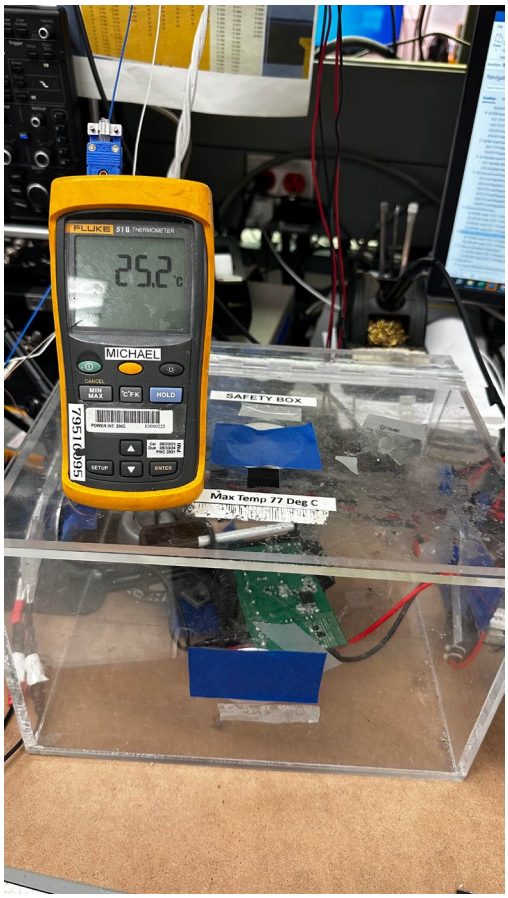


Figure 24 – Test Set-up.

13.1 90 VAC, 120 W at Room Temperature

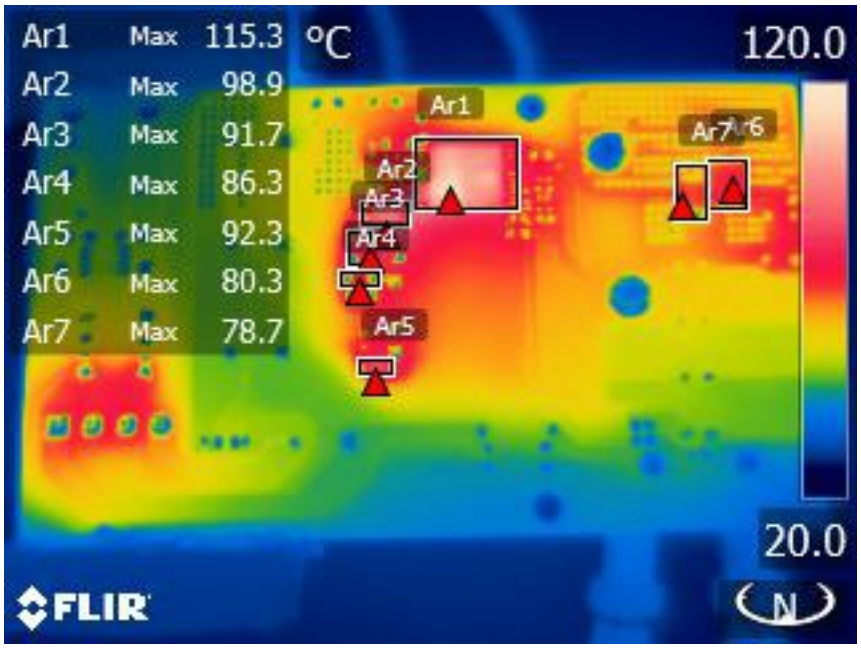


Figure 25 – Thermal Performance at 90 VAC Input (BOTTOM).

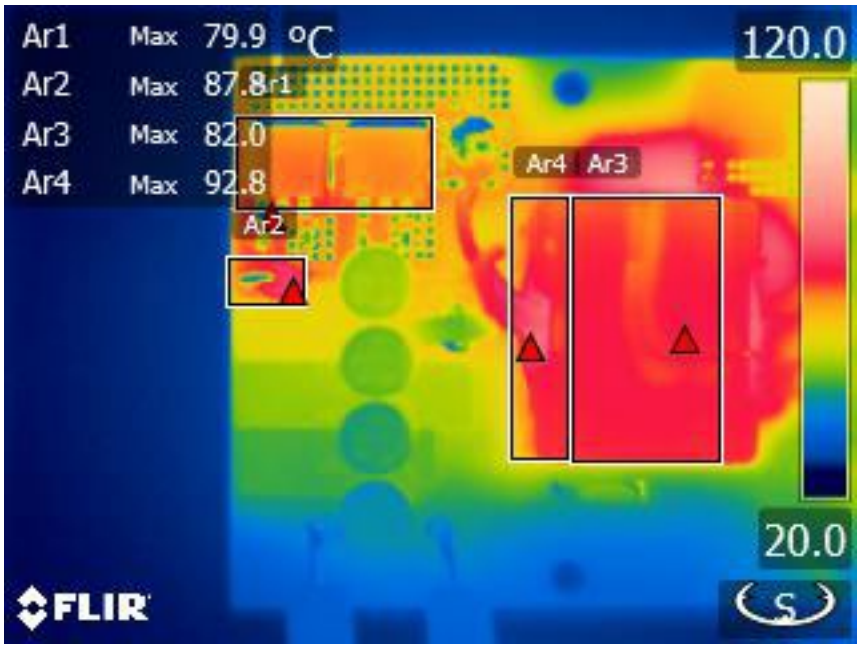


Figure 26 – Thermal Performance at 90 VAC Input (SR FET).

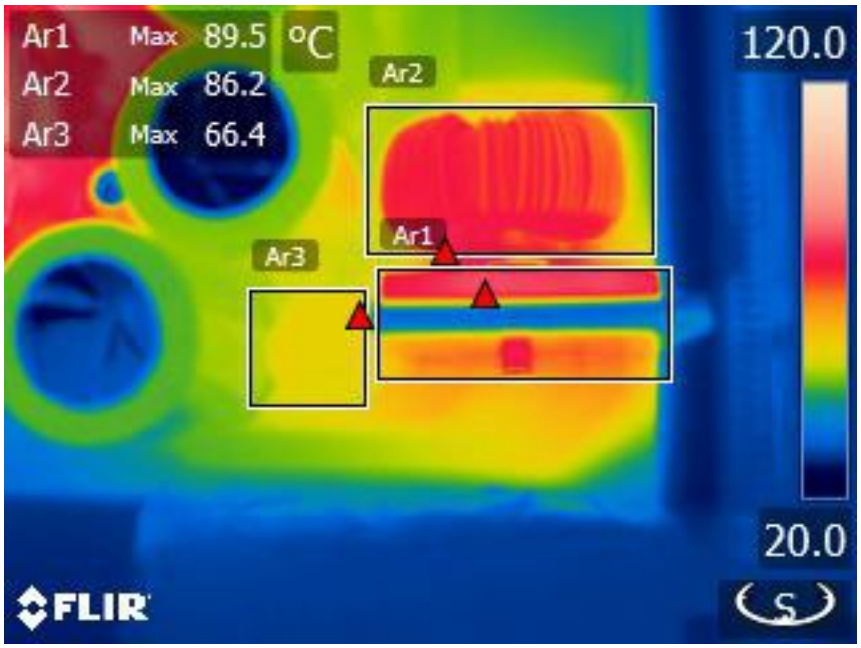


Figure 27 – Thermal Performance at 90 VAC Input (TOP).

Component	Actual Temperature (°C)	Temperature - Normalized to 25 °C Ambient (°C)
Ambient	33.2	25
INN4277C (U1)	115	107
Primary Snubber Diode (D1)	98.9	90.7
Primary Snubber Series Resistor (R4, R5)	91.7	83.5
Primary Snubber Resistor (R3)	86.3	78.1
Bias Diode (D2)	92.3	84.1
Schottky Diode (D3)	80.3	72.1
TVS Diode (VR1)	78.7	70.5
SR FET (Q1, Q2)	79.9	71.7
Secondary Snubber Resistor (R9)	87.8	79.6
TF Core (T1)	82	73.8
TF Winding (T1)	92.8	84.6
Bridge (BR1)	89.5	81.3
Common Mode Choke (L1)	86.2	78
Differential Inductor (L2)	66.4	58.2

13.2 90 VAC, 120 W at Room Temperature with Heat Spreader

Note: For enclosed applications, this design requires use of a metallic heat spreader with suitable thermally conductive insulator pads to ensure low temperature of the InnoSwitch-4 QR IC. The thermal performance data shown below was measured using a thermocouple and heat spreader for cooling.

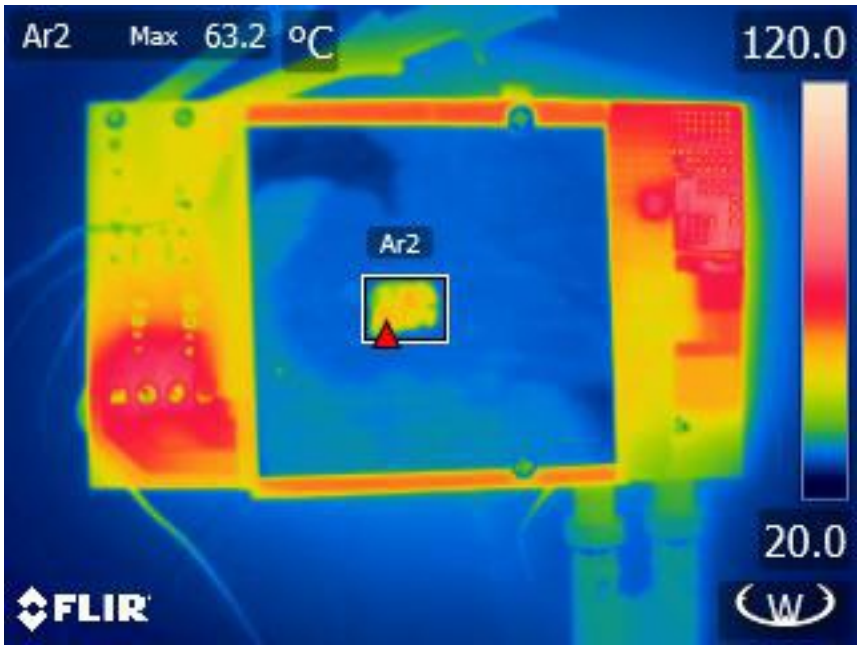


Figure 28 – Thermal Performance at 90 VAC Input with Heat Spreader (BOTTOM).

Component	Actual Temperature (°C)	Temperature - Normalized to 25 °C Ambient (°C)
Ambient	30.9	25
INN4277C (U1)	85	79.1

13.3 265 VAC, 120 W at Room Temperature

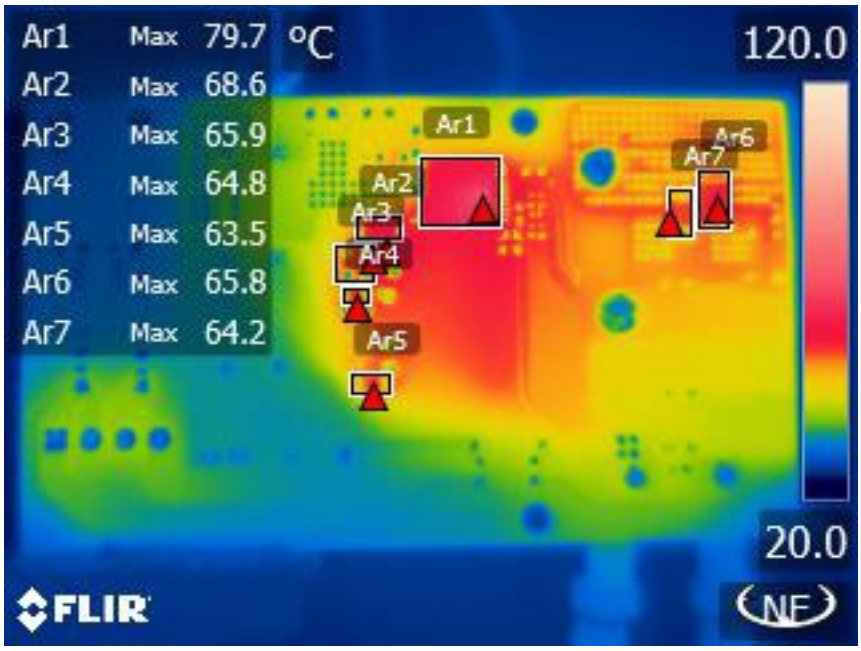


Figure 29 – Thermal Performance at 265 VAC Input (BOTTOM).

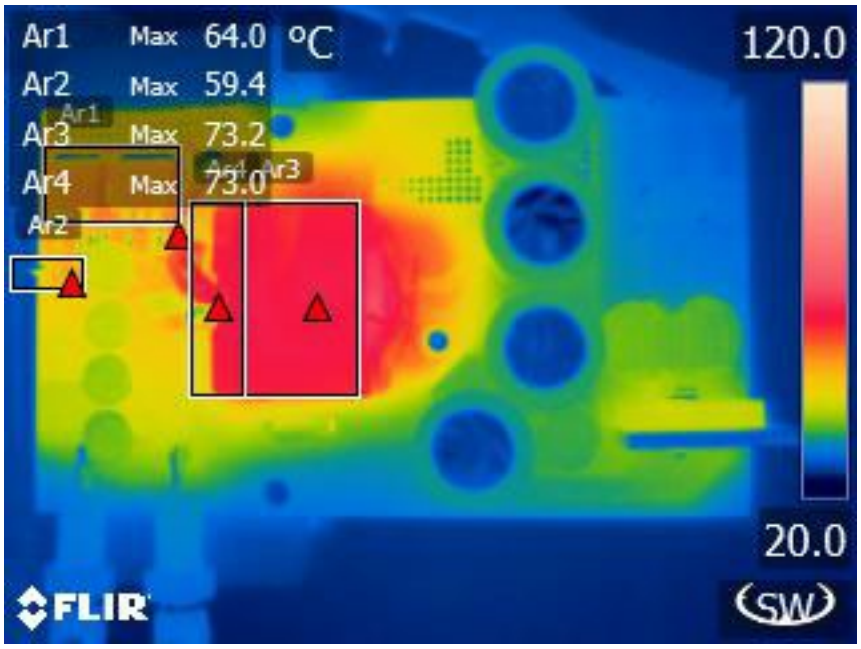


Figure 30 – Thermal Performance at 265 VAC Input (SR FET).

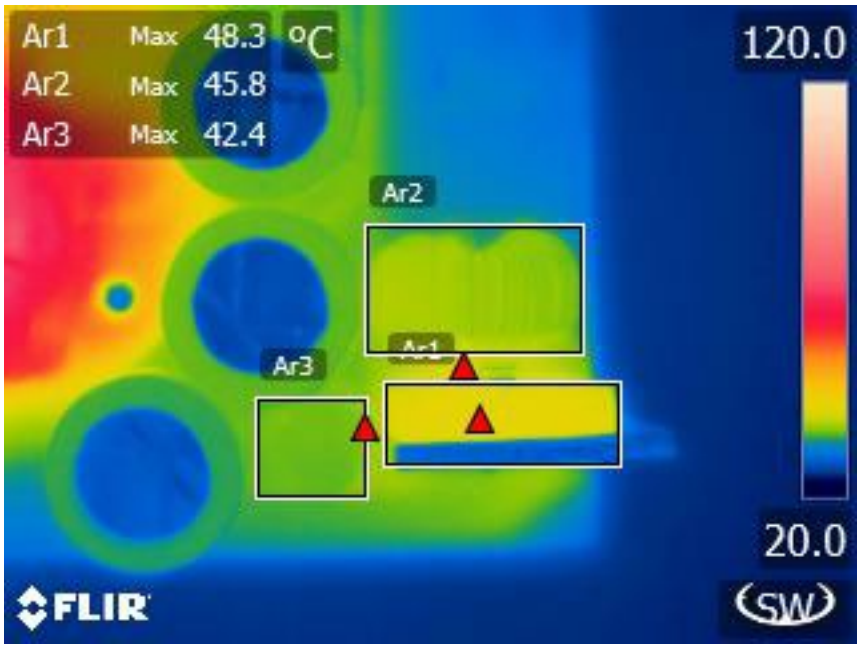


Figure 31 – Thermal Performance at 265 VAC Input (TOP).

Component	Actual Temperature (°C)	Temperature - Normalized to 25 °C Ambient (°C)
Ambient	27.6	25
INN4277C (U1)	79.7	77.1
Primary Snubber Diode (D1)	68.6	66
Primary Snubber Series Resistor (R4, R5)	65.9	63.3
Primary Snubber Resistor (R3)	64.8	62.2
Bias Diode (D2)	63.5	60.9
Schottky Diode (D3)	65.8	63.2
TVS Diode (VR1)	64.2	61.6
SR FET (Q1, Q2)	64.0	61.4
Secondary Snubber Resistor (R9)	59.4	56.8
TF Core (T1)	73.2	70.6
TF Winding (T1)	73.0	70.4
Bridge (BR1)	48.3	45.7
Common Mode Choke (L1)	45.8	43.2
Differential Inductor (L2)	42.4	39.8

14 Thermal Performance at 40 °C Ambient

Note: A thermal chamber was used to increase the ambient temperature to 50 °C. The power supply was placed inside a box to prevent air flow. The unit was soaked at full load and allowed to stabilize for 1 hour before measurements were taken.

Figure 32 – Thermal Chamber Test Set-up.

14.1 90 VAC, 100 W at 40 °C Ambient

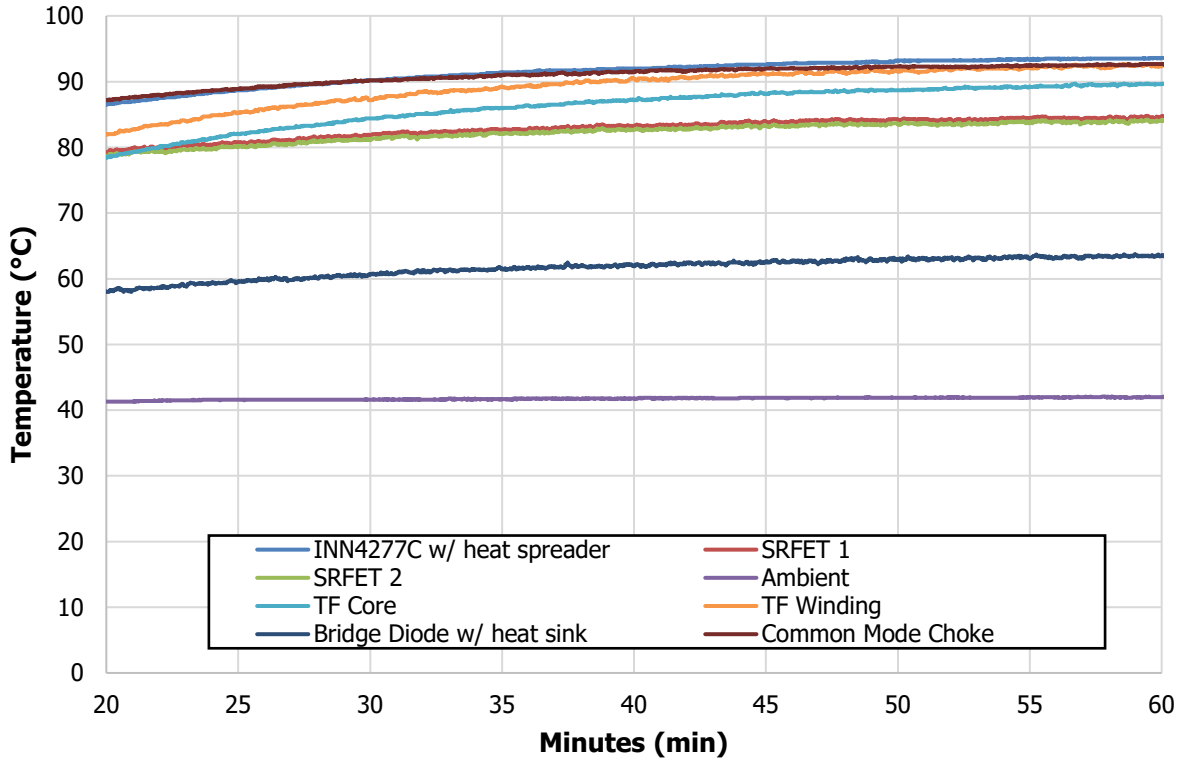


Figure 33 – Thermal Performance at 90 VAC Input.

Component	Max Temperature (°C)
INN4277C (U1)	93.8
Bridge Diode (BR1)	63.8
Common Mode Choke (L1)	92.8
Transformer Core (T1)	89.9
Transformer Winding (T1)	92.8
SR FET 1 (Q1)	84.9
SR FET 2 (Q2)	84.3
Ambient	42.1

14.2 265 VAC Input, 100 W at 40 °C Ambient

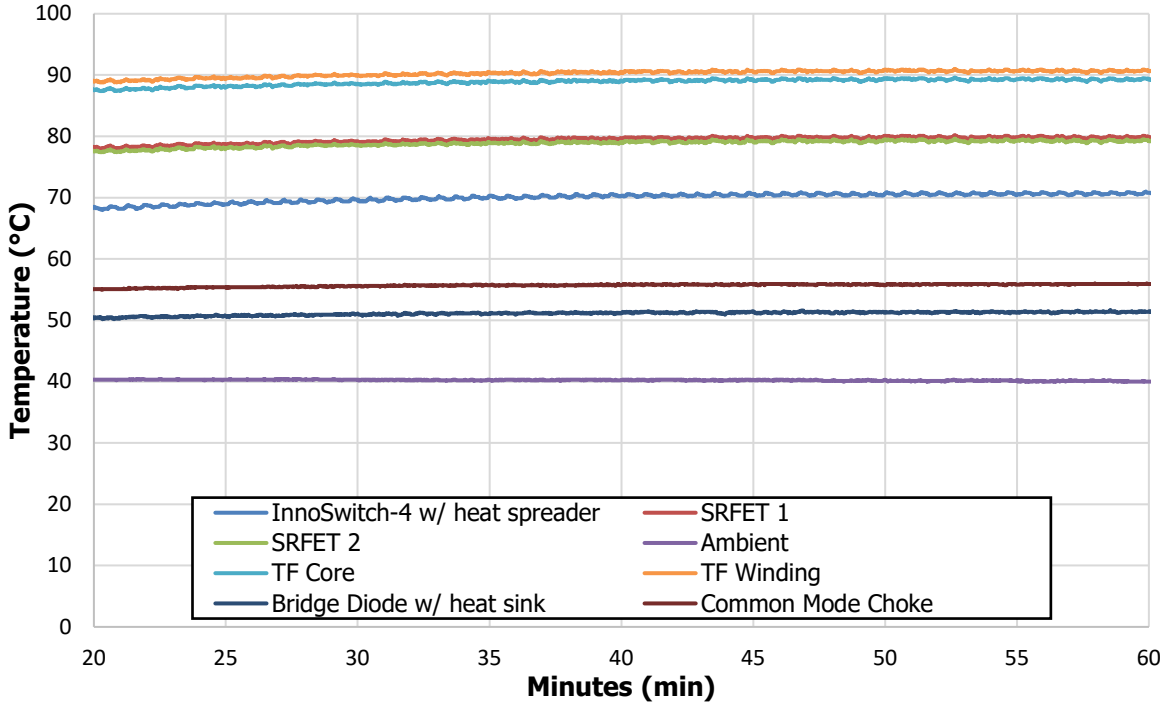


Figure 34 – Thermal Performance at 265 VAC Input.

Component	Max Temperature (°C)
INN4277C (U1)	71
Bridge Diode (BR1)	51.7
Common Mode Choke (L1)	56
Transformer Core (T1)	89.7
Transformer Winding (T1)	91.1
SR FET 1 (Q1)	80.3
SR FET 2 (Q2)	79.7
Ambient	40.6

15 Waveforms

15.1 Output Voltage Start-up Waveforms at Room Temperature

15.1.1 CC Load

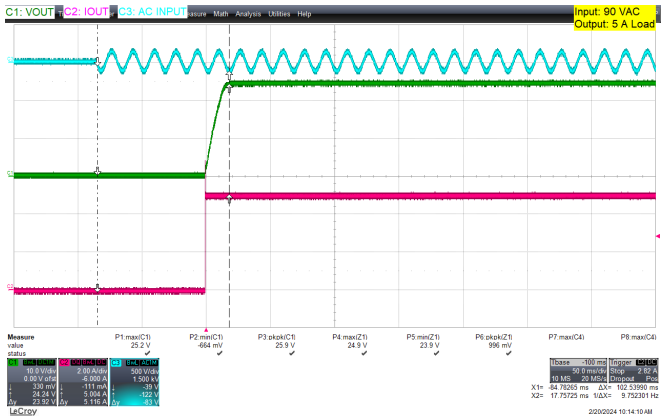


Figure 35 – 90 VAC 60 Hz, I_{OUT} = 5 A (Full-Load, CC)
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.2 V.
Start-up Time = 102 ms.

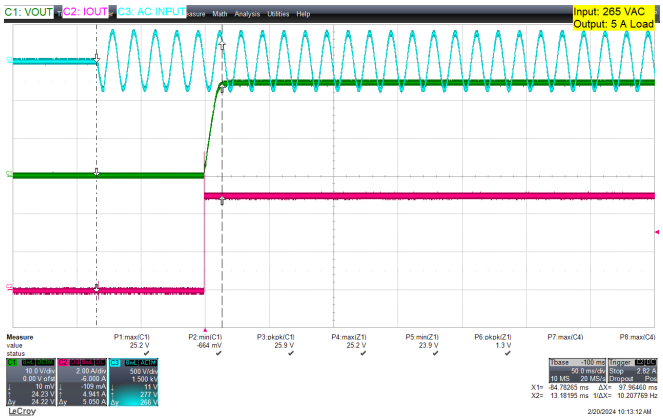


Figure 36 – 265 VAC 50 Hz, I_{OUT} = 5 A (Full-Load, CC)
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max = 25.2 V.
Start-up Time = 98 ms.

15.1.2 CR Load

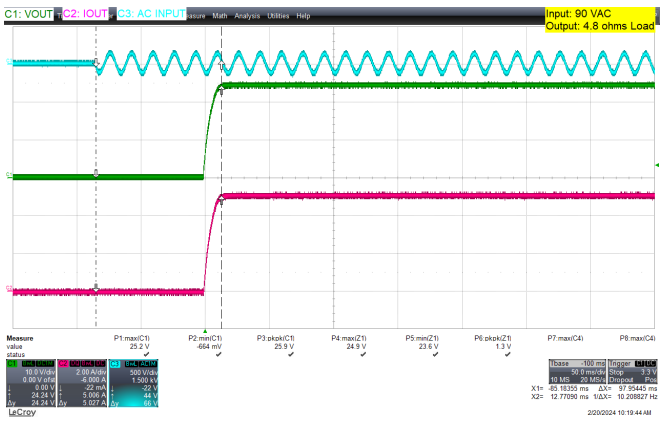


Figure 37 – 90 VAC 60 Hz, R_{load} = 4.8 Ω (Full-Load, CR).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.2 V.
Start-up Time = 97 ms.

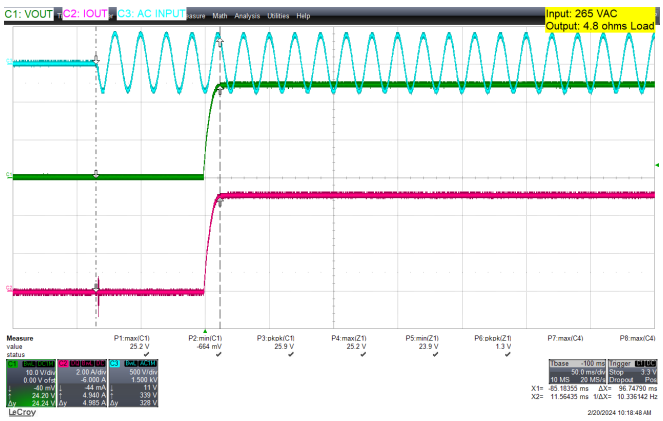


Figure 38 – 265 VAC 50 Hz, R_{load} = 4.8 Ω (Full-Load, CR).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max = 25.2 V.
Start-up Time = 96 ms.

15.1.3 No-Load

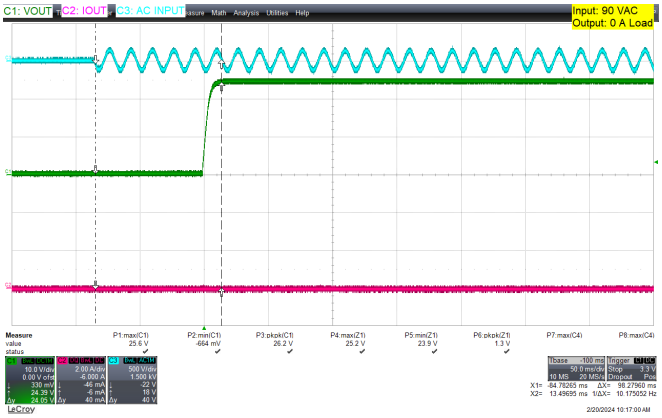


Figure 39 – 90 VAC 60 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.6 V.
Start-up Time = 98 ms.

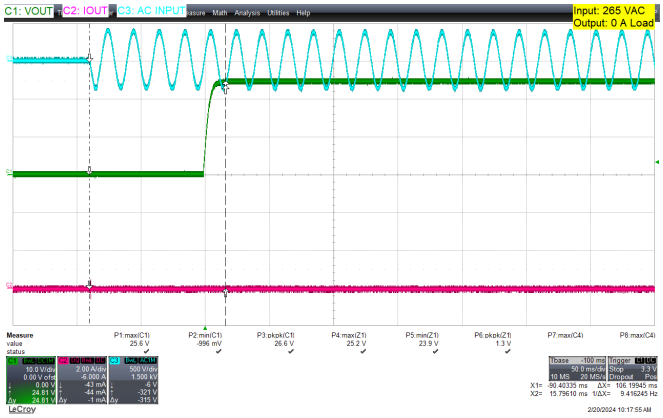


Figure 40 – 265 VAC 50 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.6 V.
Start-up Time = 106 ms.

15.2 Output Voltage Start-up Waveforms at 40 °C

15.2.1 CC Load

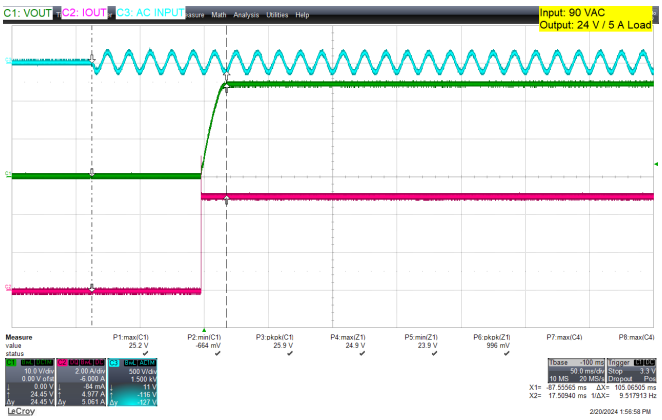


Figure 41 – 90 VAC 60 Hz, I_{OUT} = 5 A (Full-Load, CC)
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.2 V.
Start-up Time = 105 ms.

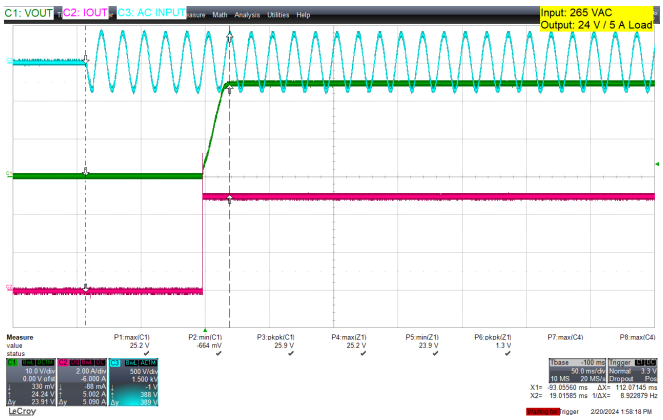


Figure 42 – 265 VAC 50 Hz, I_{OUT} = 5 A (Full-Load, CC)
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max = 25.2 V.
Start-up Time = 112 ms.

15.2.2 CR Load

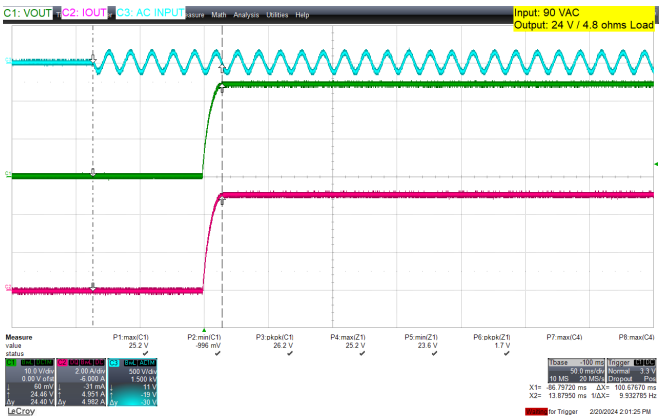


Figure 43 – 90 VAC 60 Hz, R_{load} = 4.8 Ω (Full-Load, CR).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.2 V.
Start-up Time = 100 ms.

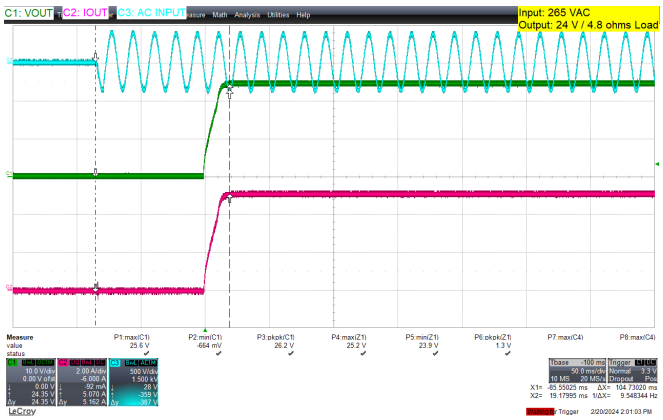


Figure 44 – 265 VAC 50 Hz, R_{load} = 4.8 Ω (Full-Load, CR).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max = 25.6 V.
Start-up Time = 104 ms.

15.2.3 No-Load

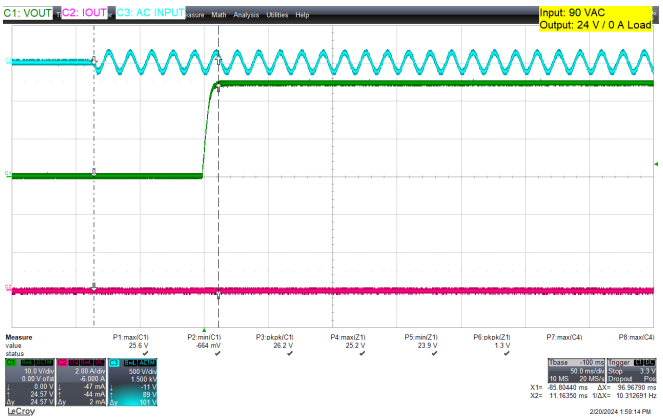


Figure 45 – 90 VAC 60 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.6 V.
Start-up Time = 97 ms.

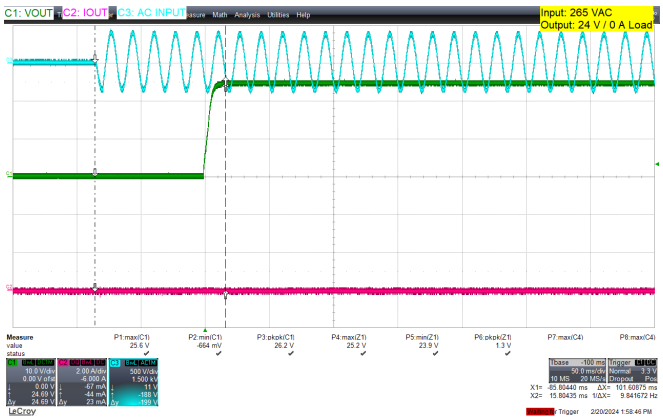


Figure 46 – 265 VAC 50 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.6 V.
Start-up Time = 101 ms.

15.3 Output Voltage Start-up Waveforms at 0 °C

15.3.1 CC Load

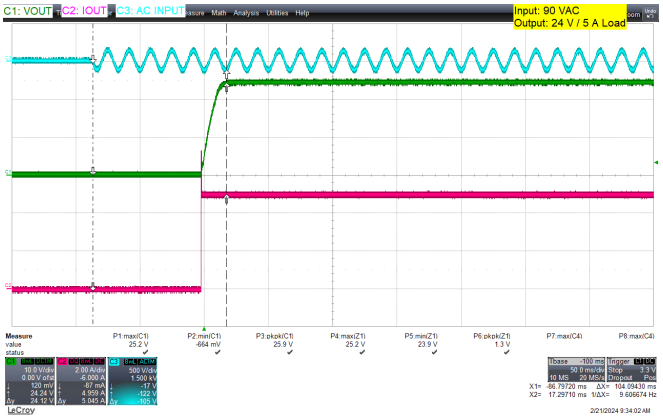


Figure 47 – 90 VAC 60 Hz, I_{OUT} = 5 A (Full-Load, CC)
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.2 V.
Start-up Time = 104 ms.

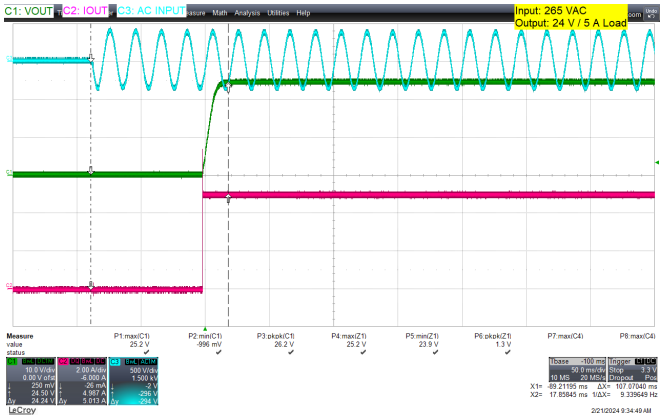


Figure 48 – 265 VAC 50 Hz, I_{OUT} = 5 A (Full-Load, CC)
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max = 25.2 V.
Start-up Time = 107 ms.

15.3.2 CR Load

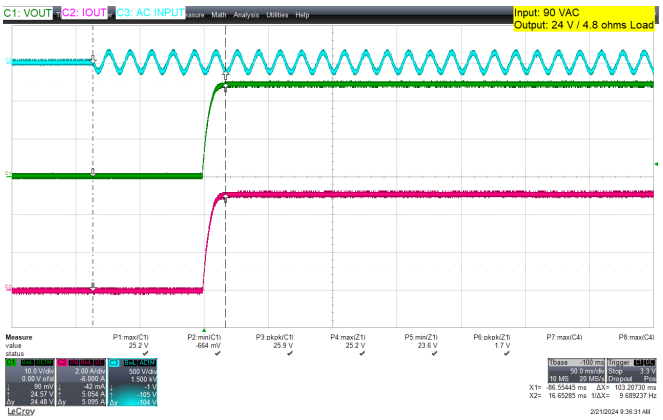


Figure 49 – 90 VAC 60 Hz, R_{load} = 4.8 Ω (Full-Load, CR).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.2 V.
Start-up Time = 103 ms.

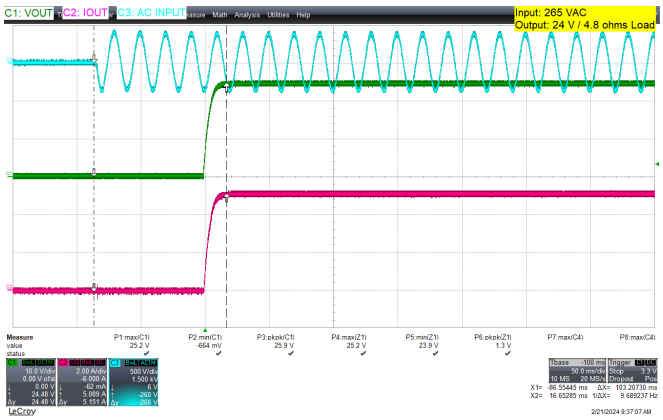


Figure 50 – 265 VAC 50 Hz, R_{load} = 4.8 Ω (Full-Load, CR).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max = 25.2 V.
Start-up Time = 103 ms.

15.3.3 No-Load

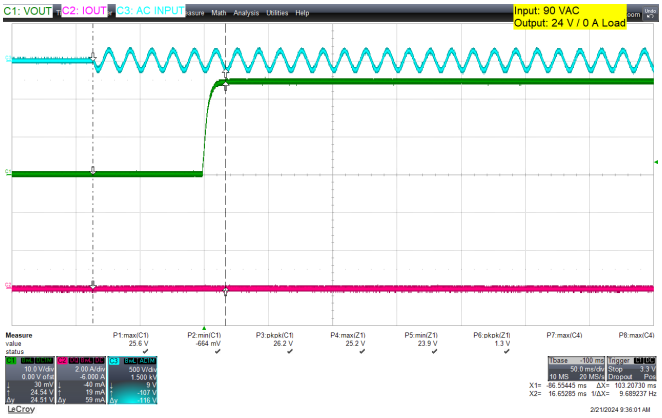


Figure 51 – 90 VAC 60 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.6 V.
Start-up Time = 103 ms.

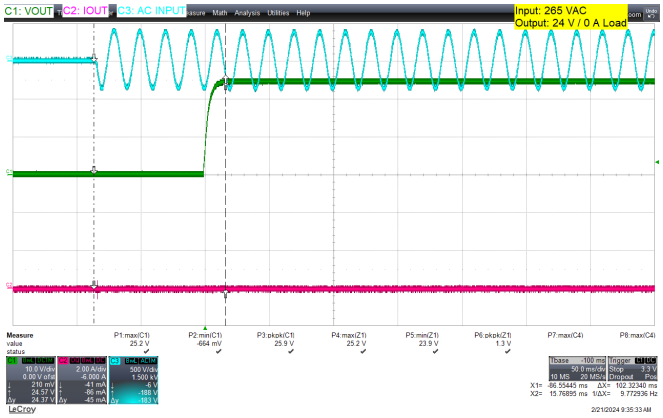


Figure 52 – 265 VAC 50 Hz, I_{OUT} = 0 A (No-Load).
CH1: Output Voltage: 10 V / div, 50 ms / div.
CH2: Output Current: 2 A / div, 50 ms / div.
CH3: Input Voltage: 500 V / div, 50 ms / div.
Output Voltage, Max. = 25.2 V.
Start-up Time = 102 ms.

15.4 Load Transient Response (On Board)

15.4.1 0 – 100% Load Step

Set-up: Dynamic load using Chroma 63103A. Dynamic load is set at 5 A for 100 ms and 0 A for 100 ms time duration. Load current slew rate at 2.5 A / µs.

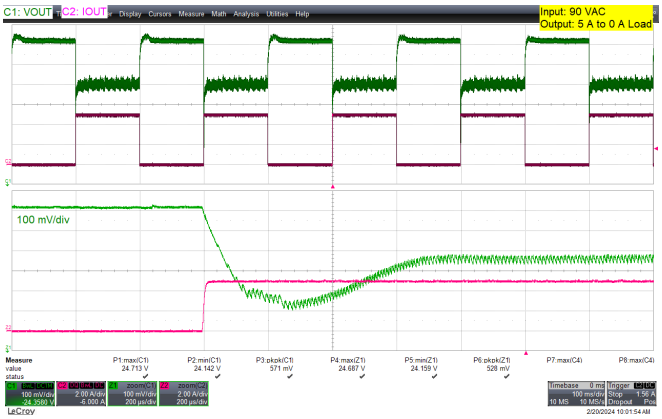


Figure 53 – 90 VAC, 60 Hz, I_{OUT} = 0 A – 5 A (0 – 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 2 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.7 V
V_{OUT_MIN}: 24.1 V

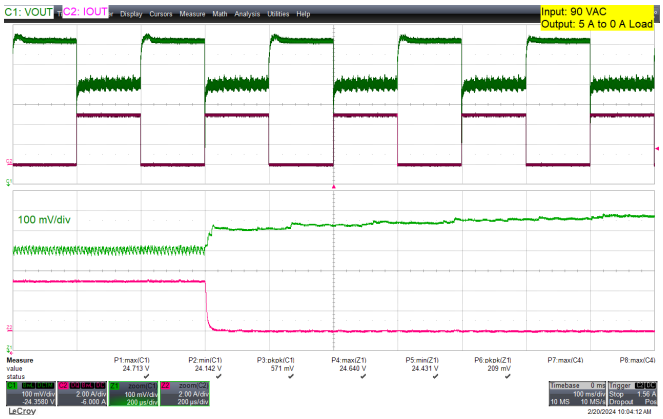


Figure 54 – 90 VAC, 60 Hz, I_{OUT} = 5 A – 0 A (100 – 0%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 2 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.7 V
V_{OUT_MIN}: 24.1 V

Figure 55 – 265 VAC 50 Hz. I_{OUT} = 0 A – 5 A (0 – 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 2 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.7 V.
V_{OUT_MIN}: 24.2 V.

Figure 56 – 265 VAC 50 Hz. I_{OUT} = 5 A – 0 A (100 – 0%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 2 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.7 V.
V_{OUT_MIN}: 24.2 V.

15.4.2 50 – 100% Load Step

Set-up: Dynamic load using Chroma 63103A. Dynamic load is set at 5 A for 100 ms and 2.5 A for 100 ms time duration. Load current slew rate at 2.5 A / µs.

Figure 57 – 90 VAC 60 Hz. I_{OUT} = 2.5 A – 5 A (50 – 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 2 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.6 V.
V_{OUT_MIN}: 24.4 V.

Figure 58 – 90 VAC 60 Hz. I_{OUT} = 5 A – 2.5 A (100 – 50%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.6 V.
V_{OUT_MIN}: 24.4 V.

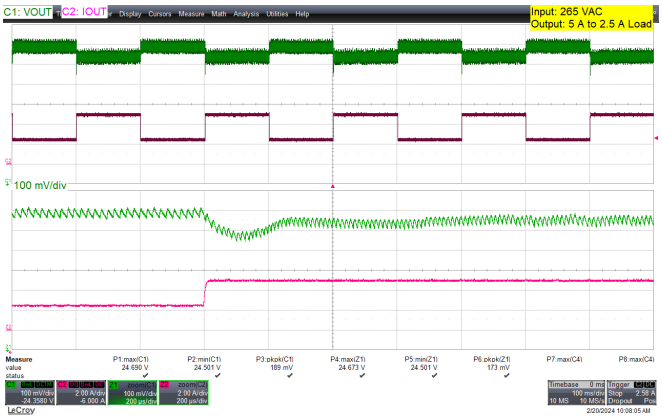


Figure 59 – 265 VAC 50 Hz. I_{OUT} = 2.5 A – 8.34 A (50 – 100%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.7 V.
V_{OUT_MIN}: 24.5 V.

Figure 60 – 265 VAC 50 Hz. I_{OUT} = 8.34 A – 2.5 A (100 – 50%) Load Step.
CH1: Output Voltage: 100 mV / div, 100 ms / div.
CH2: Output Current: 5 A / div, 100 ms / div.
Zoom: 200 µs / div.
V_{OUT_MAX}: 24.7 V.
V_{OUT_MIN}: 24.5 V.

15.5 Peak Load Transient Test

15.5.1 0 – 125% Load Step (0 W for 1000 ms to 150 W for 100 ms)

Set-up: Dynamic load using Chroma 63103A. Dynamic load is set at 6.25 A for 100 ms and 0 A for 1000 ms time duration. Load current slew rate at 2.5 A / μs.

Figure 61 – 90 VAC 60 Hz. I_{OUT} = 0 A (1000 ms) – 6.25 A (100 ms) - (0 – 125%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 μs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

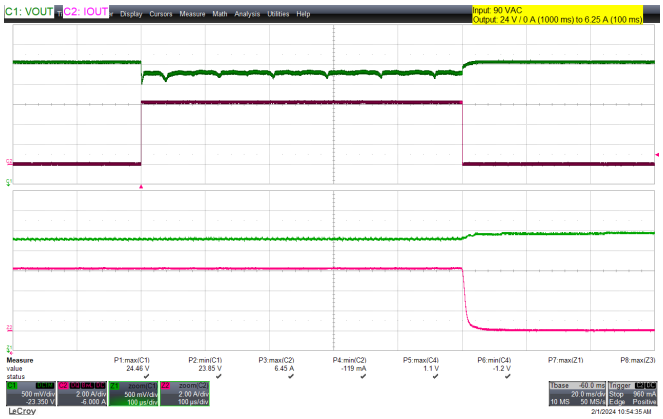


Figure 62 – 90 VAC 60 Hz. I_{OUT} = 6.25 A (100 ms) – 0 A (1000 ms) - (125 – 0%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 μs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

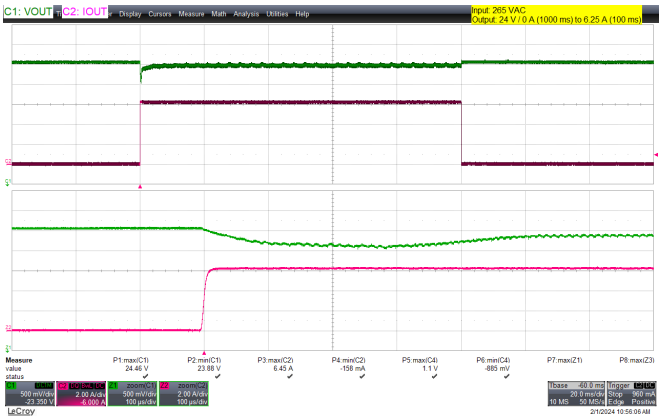


Figure 63 – 265 VAC 50 Hz. I_{OUT} = 0 A (1000 ms) – 6.25 A (100 ms) - (0 – 100%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 μs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

Figure 64 – 265 VAC 50 Hz. I_{OUT} = 6.25 A (100 ms) – 0 A (1000 ms) - (100 – 0%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 μs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

15.5.2 0 – 125% Load Step (0 W for 100 ms to 150 W for 100 ms)

Set-up: Dynamic load using Chroma 63103A. Dynamic load is set at 6.25 A for 100 ms and 0 A for 100 ms time duration. Load current slew rate at 2.5 A / µs.

Figure 65 – 90 VAC 60 Hz. I_{OUT} = 0 A (100ms) – 6.25 A (100 ms) - (0 – 125%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 µs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

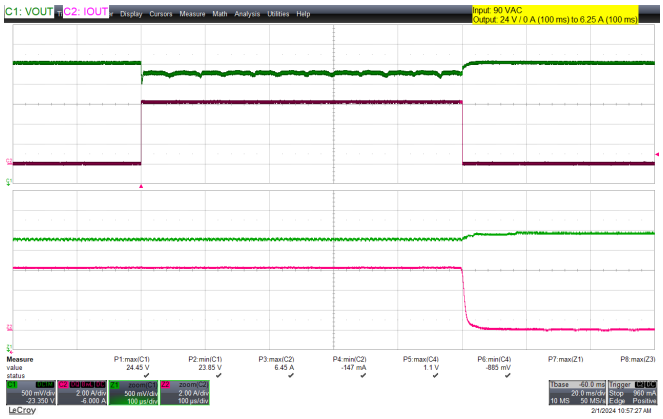


Figure 66 – 90 VAC 60 Hz. I_{OUT} = 6.25 A (100 ms) – 0 A (100 ms) - (125 – 0%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 µs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

Figure 67 – 265 VAC 50 Hz. I_{OUT} = 0 A (100 ms) – 6.25 A (100 ms) - (0 – 100%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 µs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

Figure 68 – 265 VAC 50 Hz. I_{OUT} = 6.25 A (100 ms) – 0 A (1000 ms) - (100 – 0%) Load Step.
CH1: Output Voltage: 500 mV / div, 20 ms / div.
CH2: Output Current: 2 A / div, 20 ms / div.
Zoom: 100 µs / div.
V_{OUT_MAX}: 24.5 V.
V_{OUT_MIN}: 23.9 V.

15.6 Switching Waveforms

15.6.1 Drain Voltage and Current at Start-up Operation

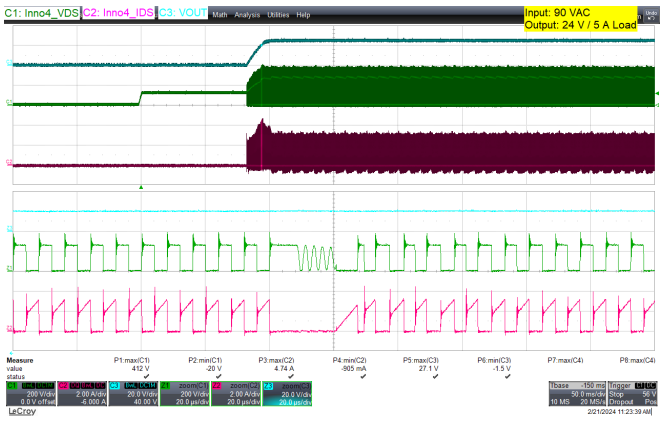


Figure 69 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 20 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 412 V.
Drain current, Max. = 4.74 A.

Figure 70 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 20 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 611 V.
Drain current, Max. = 3.95 A.

Figure 71 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 20 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 352 V.
Drain current, Max. = 2.94 A.

Figure 72 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 200 V / div, 50 ms / div.
CH2: Drain Current: 2 A / div, 50 ms / div.
CH3: Drain Voltage: 20 V / div, 50 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 618 V.
Drain current, Max. = 5.26 A.

15.6.2 Drain Voltage and Current at Normal Operation

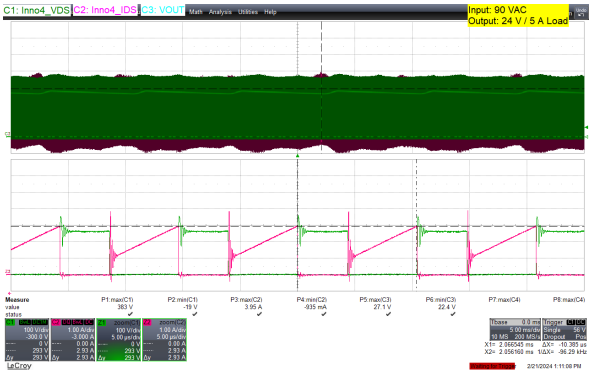


Figure 73 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 5 µs / div.
Drain voltage, Max. = 383 V.
Drain current, Max. = 3.95 A.

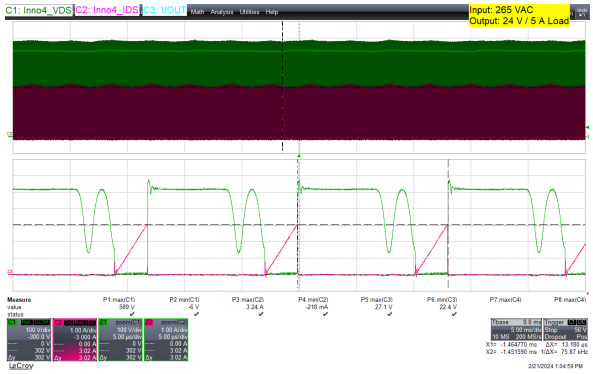


Figure 74 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 5 µs / div.
Drain voltage, Max. = 589 V.
Drain current, Max. = 3.24 A.

Figure 75 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 3 µs / div.
Drain voltage, Max. = 320 V.
Drain current, Max. = 1.18 A.

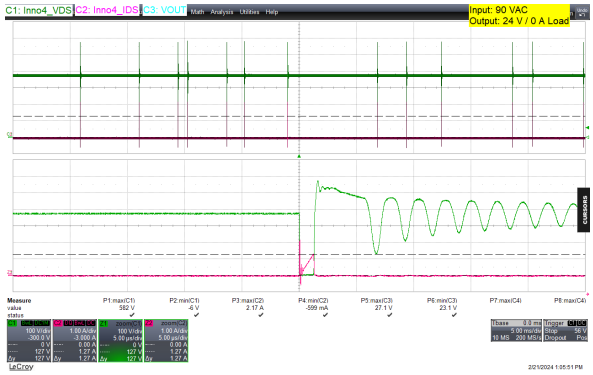


Figure 76 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH1: Drain Voltage: 100 V / div, 5 ms / div.
CH2: Drain Current: 1 A / div, 5 ms / div.
Zoom: 5 µs / div.
Drain voltage, Max. = 582 V.
Drain current, Max. = 2.17 A.

15.6.3 Drain Voltage and Current at Output Short Condition

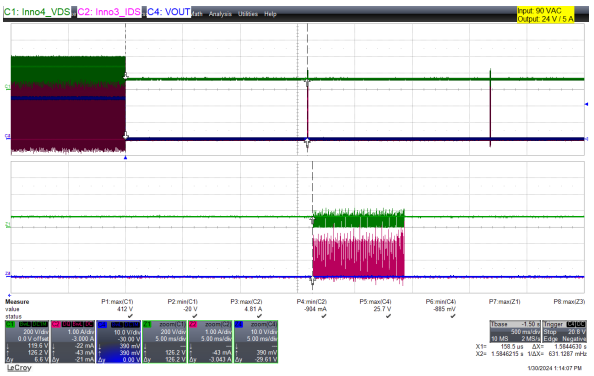


Figure 77 – 90 VAC, I_{OUT} = Output Shorted.
CH1: Drain Voltage: 200 V / div, 500 ms / div.
CH2: Drain Current: 1 A / div, 500 ms / div.
CH4: Output Voltage: 10 V / div, 500 ms / div.
Zoom: 2 ms / div.
Drain voltage, Max. = 412 V.
Drain current, Max. = 4.81 A.

Figure 78 – 265 VAC, I_{OUT} = Output Shorted.
CH1: Drain Voltage: 200 V / div, 500 ms / div.
CH2: Drain Current: 1 A / div, 500 ms / div.
CH4: Output Voltage: 10 V / div, 500 ms / div.
Zoom: 2 ms / div.
Drain voltage, Max. = 618 V.
Drain current, Max. = 6.06 A.

15.6.4 Drain Voltage and Current during Peak Load (0 A – 100 ms, 6.25 A – 1000 ms)

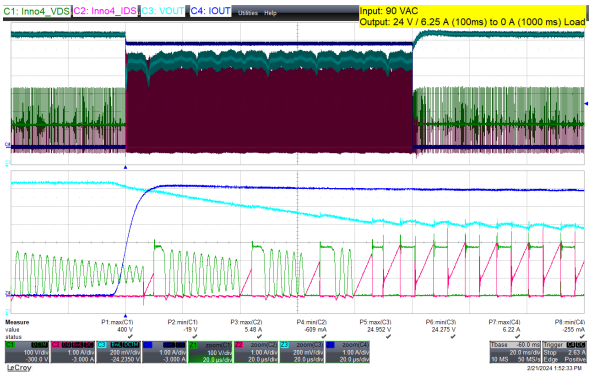


Figure 79 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 400 V.
Drain current, Max. = 5.48 A.

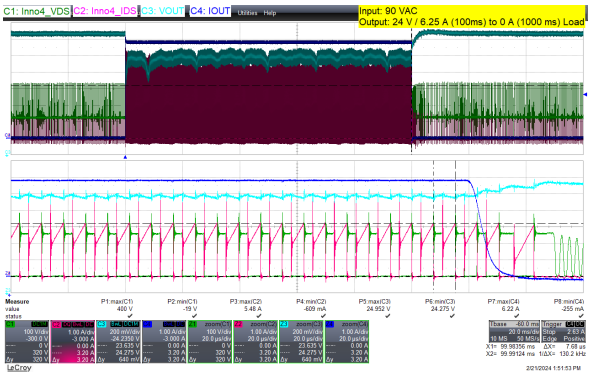


Figure 80 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 400 V.
Drain current, Max. = 5.48 A.
Current Limit @ 6.25 A Load = 3.2 A

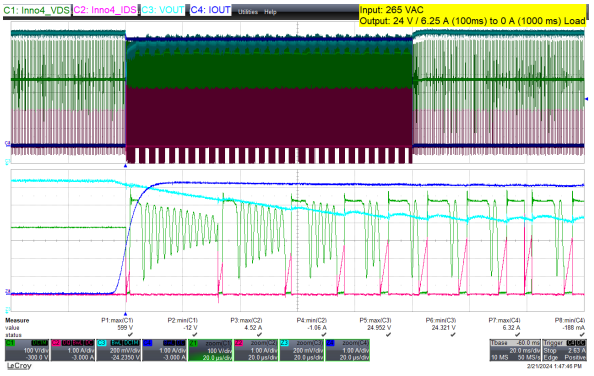


Figure 81 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 599 V.
Drain current, Max. = 4.52 A.

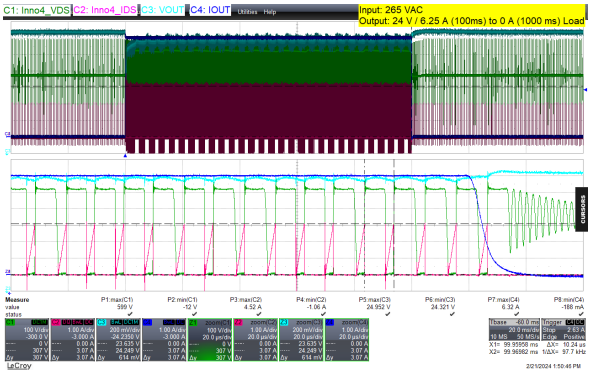


Figure 82 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 599 V.
Drain current, Max. = 4.52 A.
Current Limit @ 6.25 A Load = 3.07 A

15.6.5 Drain Voltage and Current during Peak Load (0 A – 100 ms, 6.25 A – 100 ms)

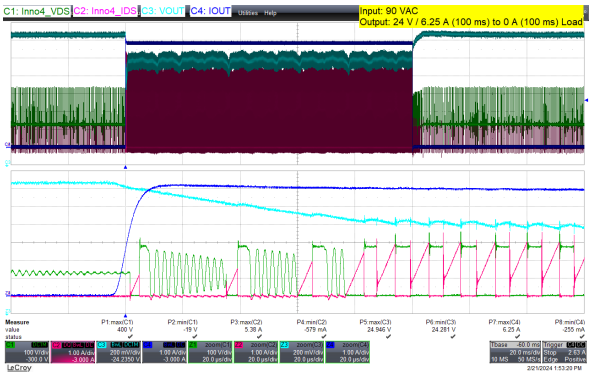


Figure 83 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 400 V.
Drain current, Max. = 5.38 A.

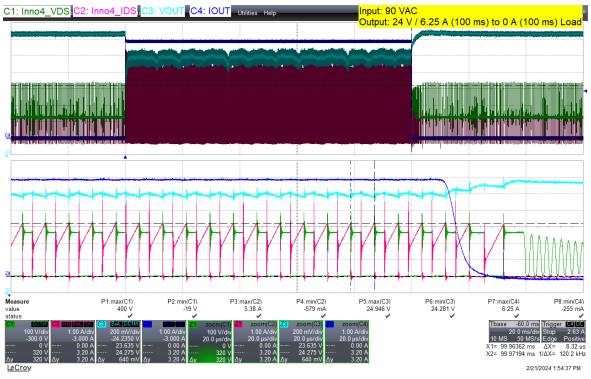


Figure 84 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 400 V.
Drain current, Max. = 5.38 A.
Current Limit @ 6.25 A Load = 3.2 A

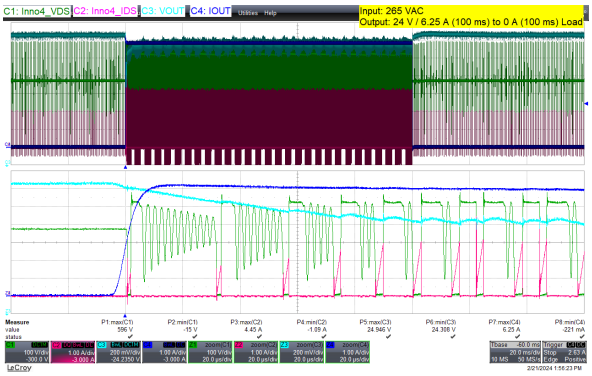


Figure 85 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 596 V.
Drain current, Max. = 4.45 A.

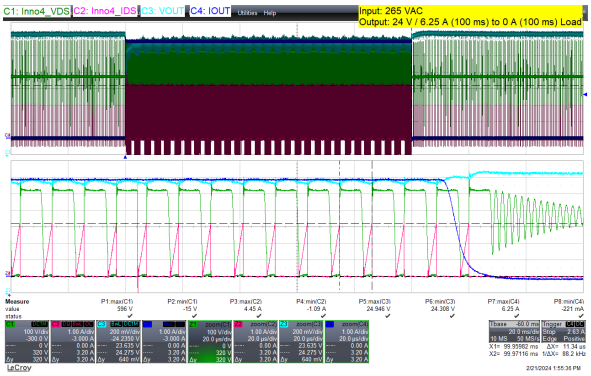


Figure 86 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: Drain Voltage: 100 V / div, 20 ms / div.
CH2: Drain Current: 1 A / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
Drain voltage, Max. = 596 V.
Drain current, Max. = 4.45 A.
Current Limit @ 6.25 A Load = 3.2 A

15.6.6 SR FET Voltage at Start-up

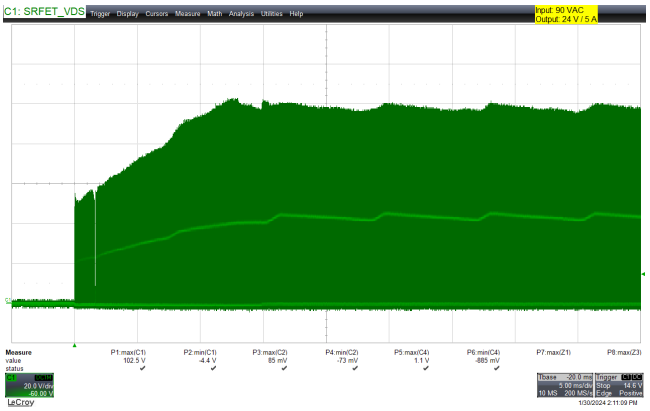


Figure 87 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH2: SRFET Drain Voltage: 20 V / div, 5 ms / div.
SRFET Drain Voltage, Max. = 103 V.

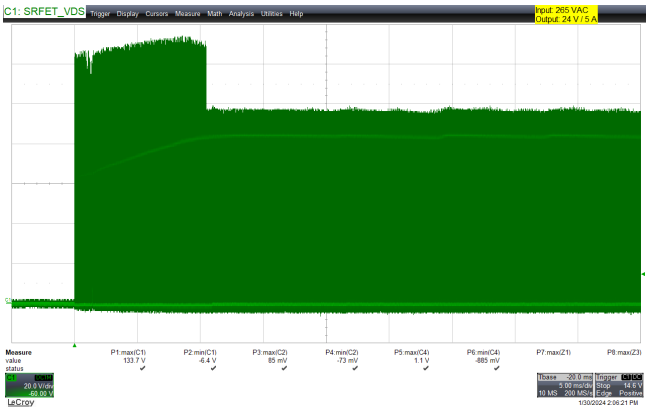


Figure 88 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH2: SRFET Drain Voltage: 20 V / div, 5 ms / div.
SRFET Drain Voltage, Max. = 134 V.

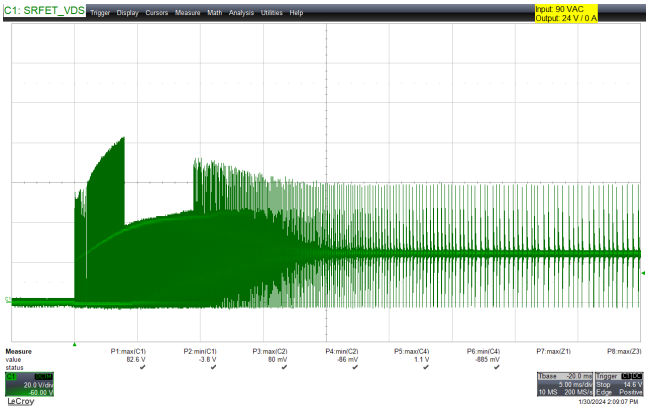


Figure 89 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH2: SRFET Drain Voltage: 20 V / div, 5 ms / div.
SRFET Drain Voltage, Max. = 82.6 V.

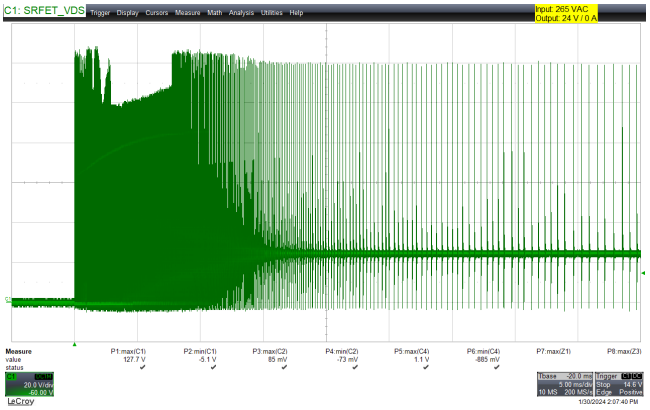


Figure 90 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH2: SRFET Drain Voltage: 20 V / div, 5 ms / div.
SRFET Drain Voltage, Max. = 128 V.

15.6.7 SR FET Voltage at Normal Operation

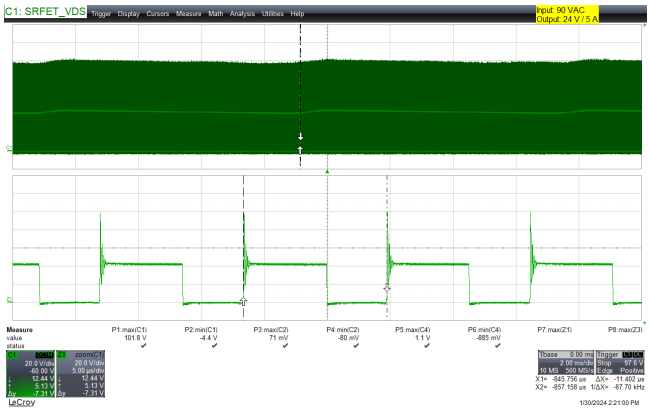


Figure 91 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH2: SRFET Drain Voltage: 20 V / div, 2 ms / div.
Zoom: 5 µs.
SRFET Drain Voltage, Max. = 102 V.

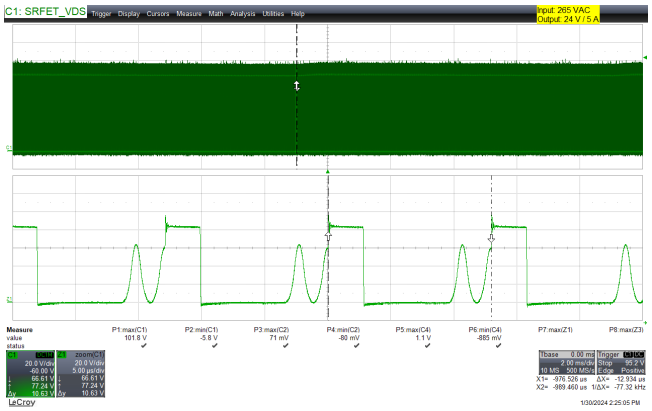


Figure 92 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH2: SRFET Drain Voltage: 20 V / div, 2 ms / div.
Zoom: 5 µs.
SRFET Drain Voltage, Max. = 102 V.

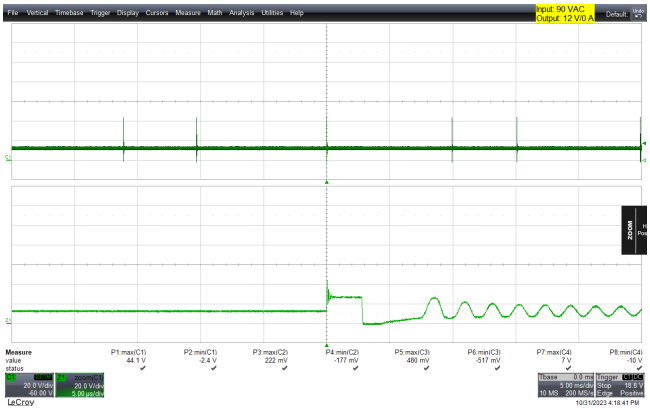


Figure 93 – 90 VAC, I_{OUT} = 0 A (No-Load).
CH2: SRFET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 5 µs.
SRFET Drain Voltage, Max. = 44.1 V.

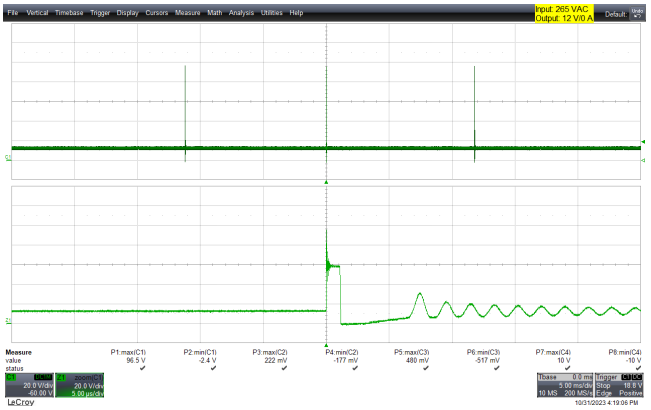


Figure 94 – 265 VAC, I_{OUT} = 0 A (No-Load).
CH2: SRFET Drain Voltage: 20 V / div, 5 ms / div.
Zoom: 5 µs.
SRFET Drain Voltage, Max. = 96.5 V.

15.6.8 SR FET Voltage at Output Short Condition

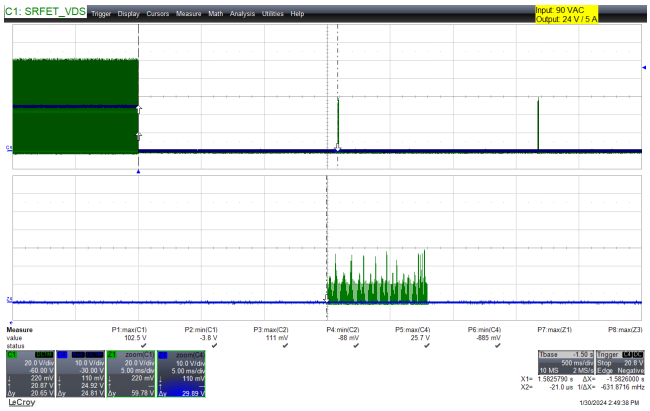


Figure 95 – 90 VAC, I_{OUT} = Output Shorted.
CH2: SRFET Drain Voltage: 20 V / div, 500 ms / div.
CH3: Output Voltage: 10 V / div, 500 ms /div.
Zoom: 5 ms.
AR_OFF: 1.58 s

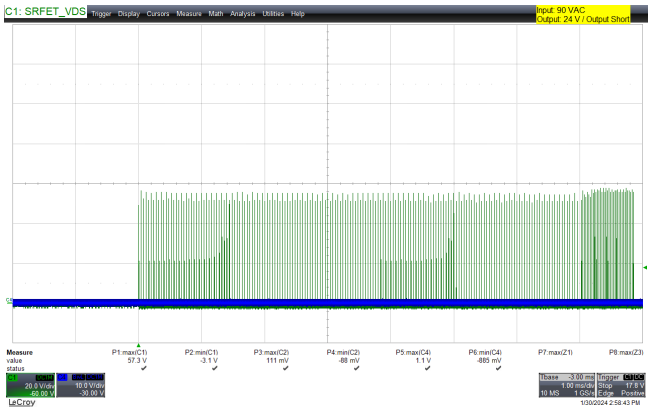


Figure 96 – 90 VAC, I_{OUT} = Output Shorted (Zoomed).
CH2: SRFET Drain Voltage: 20 V / div, 500 ms / div.
CH3: Output Voltage: 10 V / div, 500 ms /div.
Zoom: 5 ms.
SR FET Drain Voltage, Max = 57.3 V

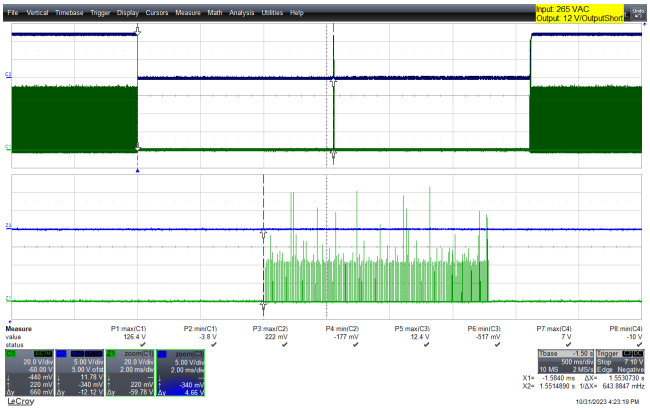


Figure 97 – 90 VAC, I_{OUT} = Output Shorted
CH2: SRFET Drain Voltage: 20 V / div, 500 ms / div.
CH3: Output Voltage: 5 V / div, 500 ms /div.
Zoom: 2 ms.
AR_OFF: 1.55 s

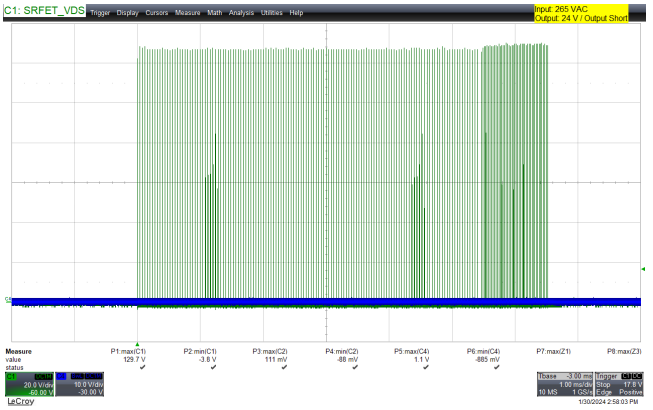


Figure 98 – 265 VAC, I_{OUT} = Output Shorted (Zoomed).
CH2: SRFET Drain Voltage: 20 V / div, 500 ms / div.
CH3: Output Voltage: 10 V / div, 500 ms /div.
Zoom: 5 ms.
SR FET Drain Voltage, Max = 130 V

15.6.9 SR FET Voltage and Current during Peak Load (0 A – 100 ms, 6.25 A – 1000 ms)

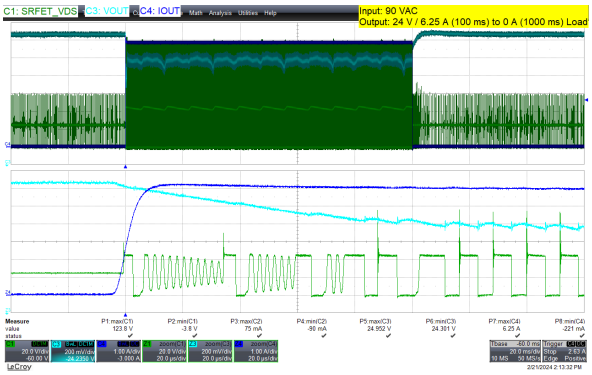


Figure 99 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 124 V.

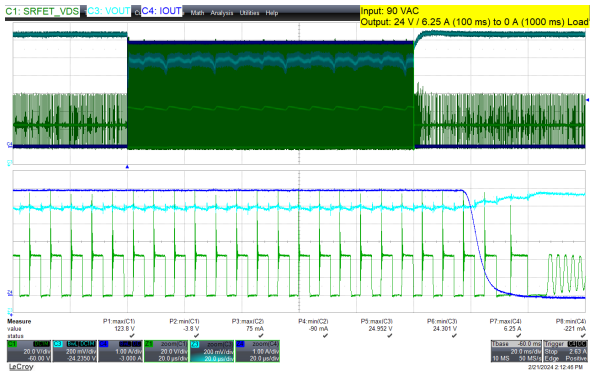


Figure 100 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 124 V.

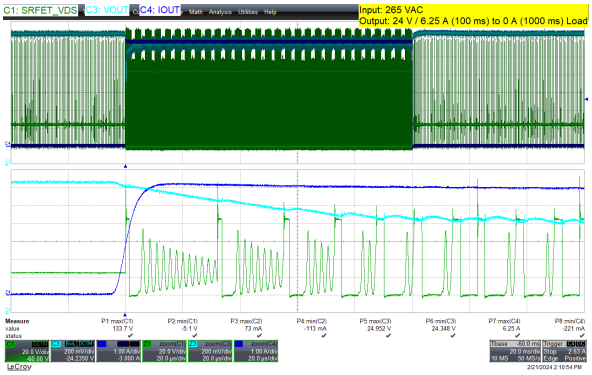


Figure 101 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 134 V.

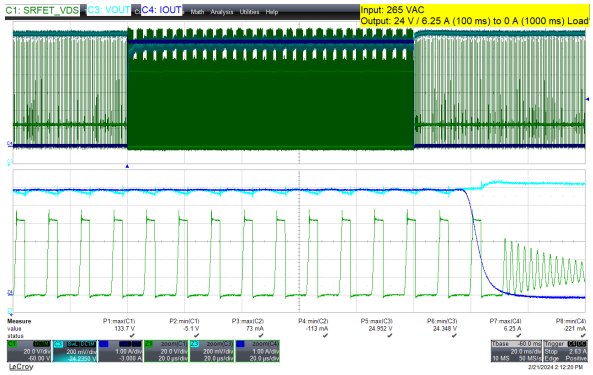


Figure 102 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (1000 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 134 V.

15.6.10 SR FET Voltage and Current during Peak Load (0 A – 100 ms, 6.25 A – 100 ms)

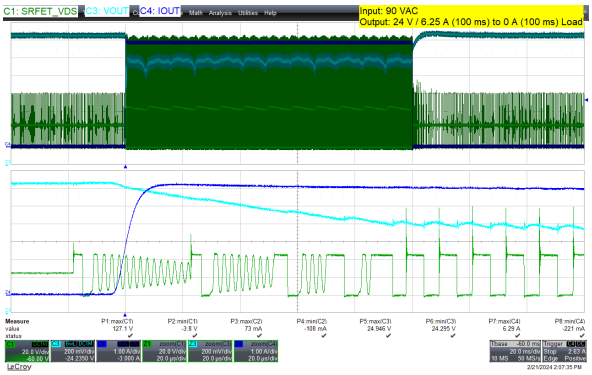


Figure 103 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 127 V.

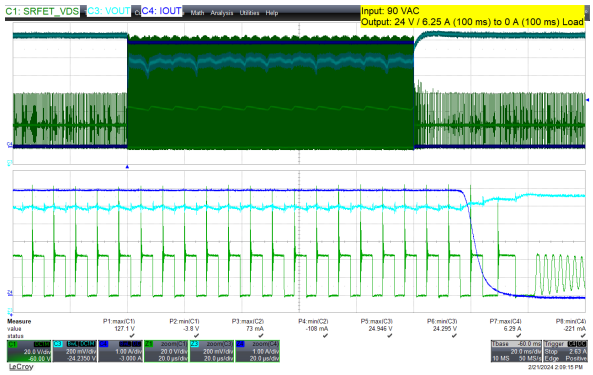


Figure 104 – 90 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 127 V.

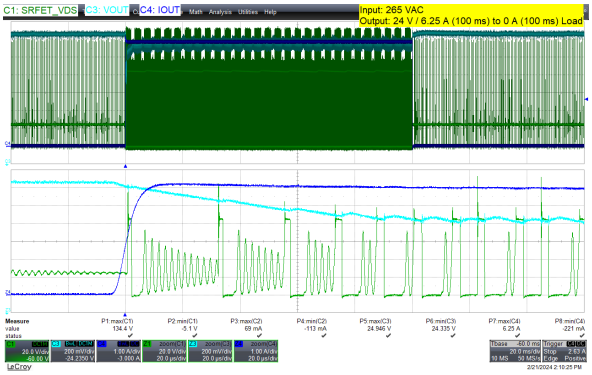


Figure 105 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 134 V.

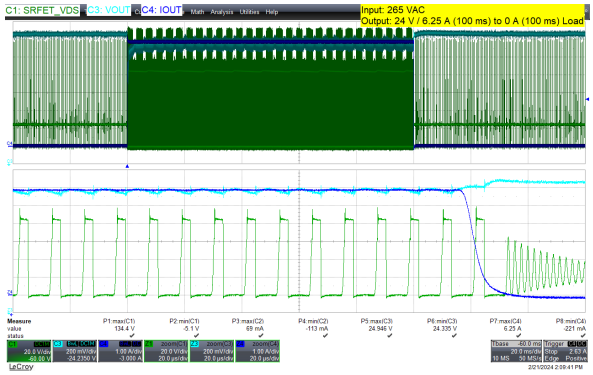


Figure 106 – 265 VAC, I_{OUT} = 0 A (100 ms) to 6.25 A (100 ms).
CH1: SR FET Drain Voltage: 20 V / div, 20 ms / div.
CH3: V_{OUT}: 200 mV / div, 20 ms / div.
CH2: I_{OUT}: 1 A / div, 20 ms / div.
Zoom: 20 µs / div.
SR FET Drain voltage, Max. = 134 V.

15.7 Output Ripple Measurements

15.7.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in figure 107 and 108.

The PP026 probe adapter was modified by having two capacitors tied in parallel across the probe tip. The capacitors included one 0.1 μF/50 V ceramic type and one 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

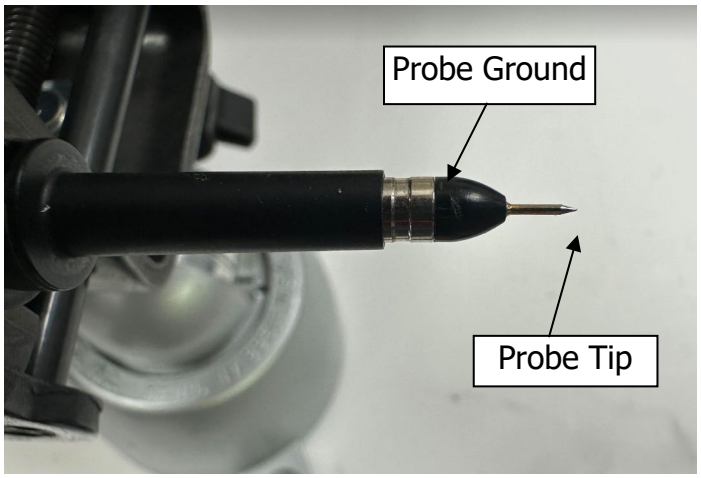


Figure 107 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

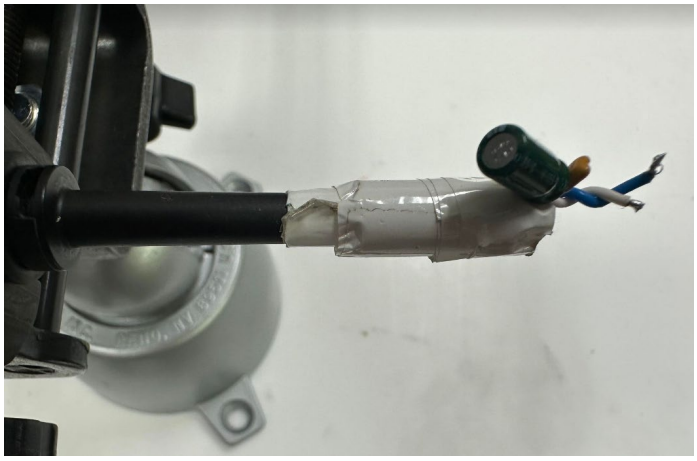


Figure 108 – Oscilloscope Probe with BNC Adapter.

(https://www.teledynelecroy.com/probes/passive-probes/pp026-1)

15.7.2 Ripple Waveforms (Measured on Board)

15.7.2.1 100% Load

Figure 109 – Output Ripple. (PK-PK – 125 mV).
90 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

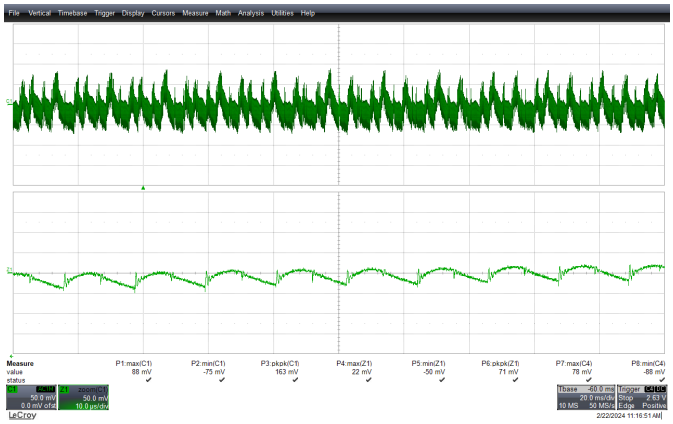


Figure 110 – Output Ripple. (PK-PK – 163 mV).
115 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

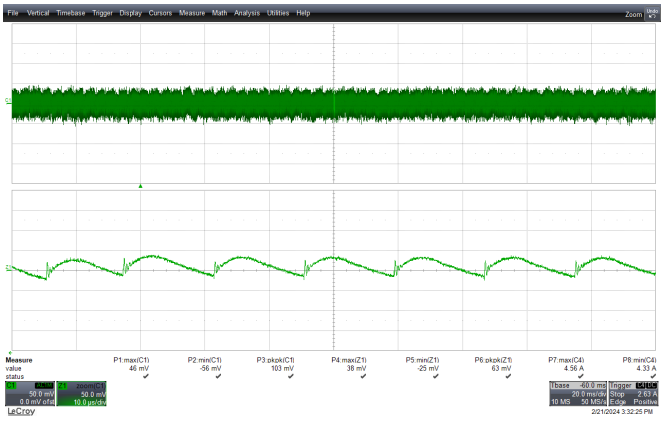


Figure 111 – Output Ripple. (PK-PK – 103 mV).
230 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

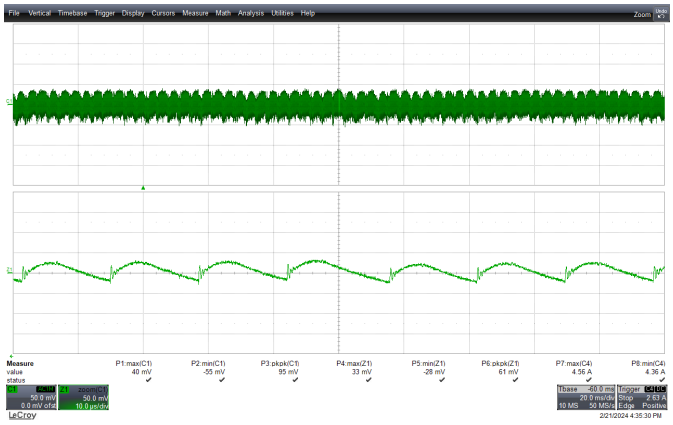


Figure 112 – Output Ripple. (PK-PK – 95 mV).
265 VAC Input, 100% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

15.7.2.2 75% Load

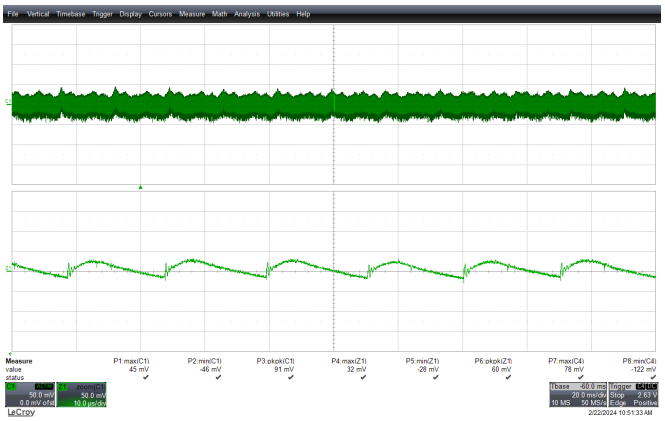


Figure 113 – Output Ripple. (PK-PK – 91 mV).
90 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

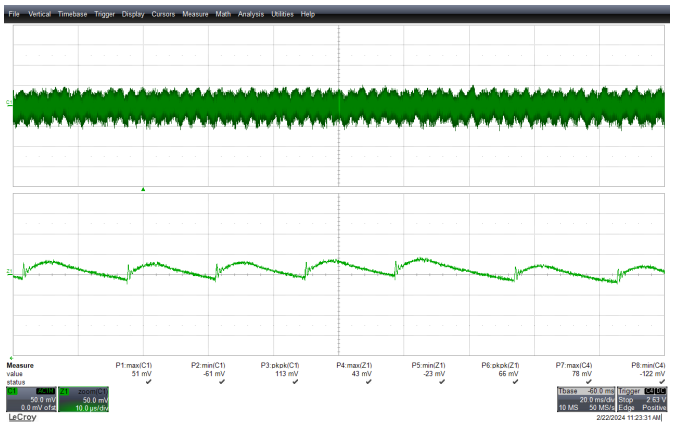


Figure 114 – Output Ripple. (PK-PK – 113 mV).
115 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

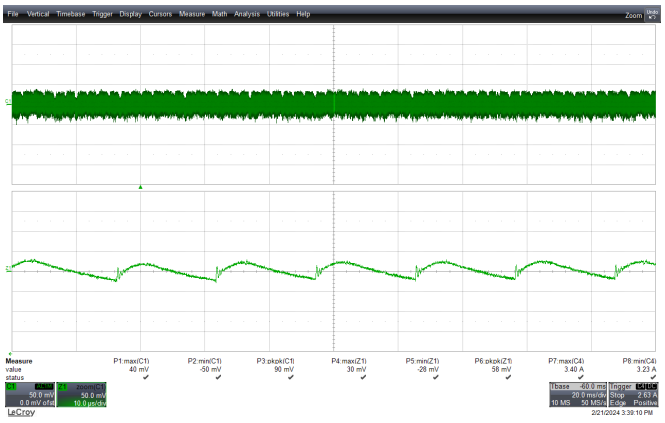


Figure 115 – Output Ripple. (PK-PK – 90 mV).
230 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

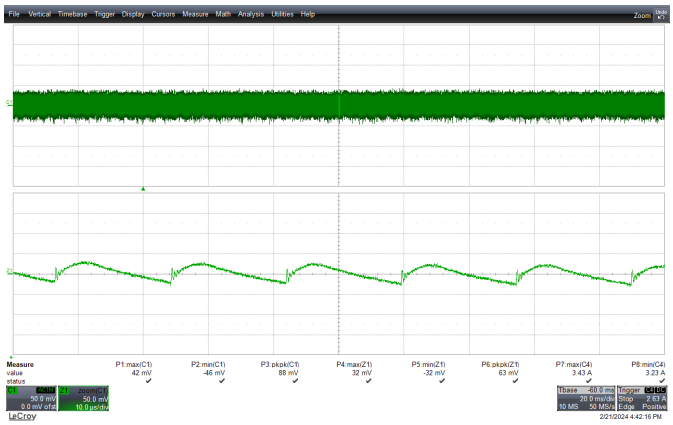


Figure 116 – Output Ripple. (PK-PK – 88 mV).
265 VAC Input, 75% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

15.7.2.3 50% Load

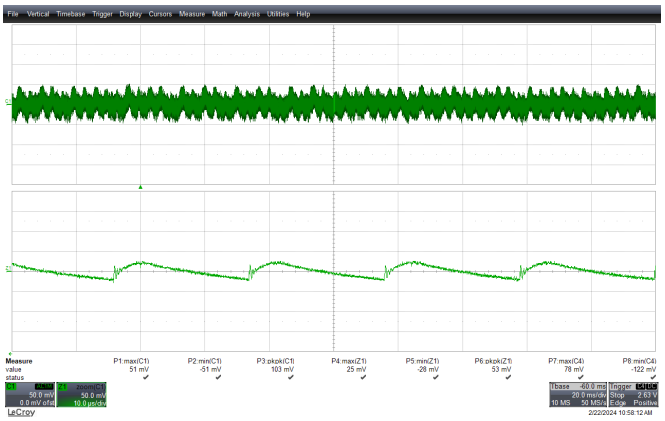


Figure 117 – Output Ripple. (PK-PK – 103 mV).
90 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

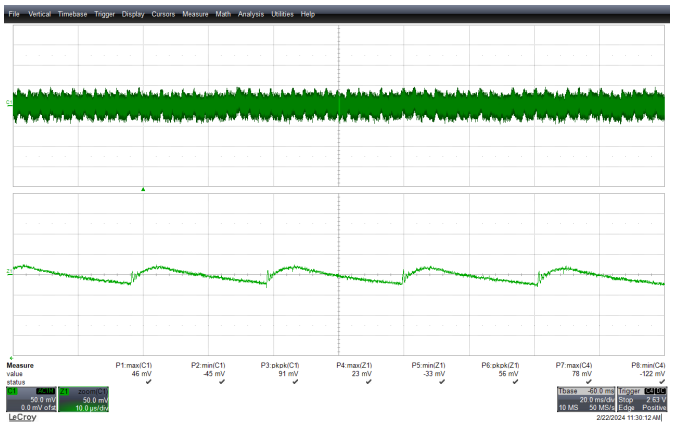


Figure 118 – Output Ripple. (PK-PK – 91 mV).
115 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

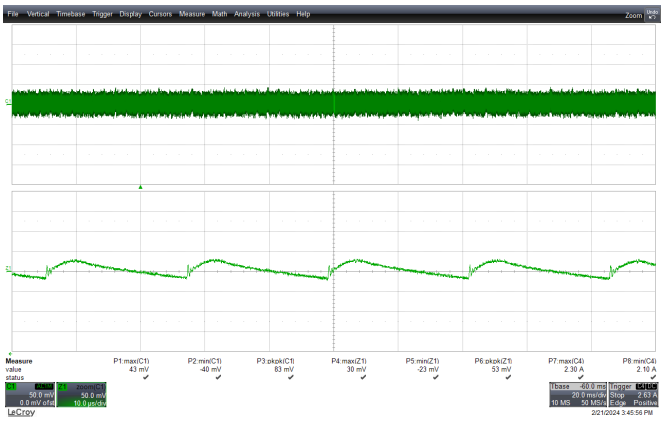


Figure 119 – Output Ripple. (PK-PK – 83 mV).
230 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

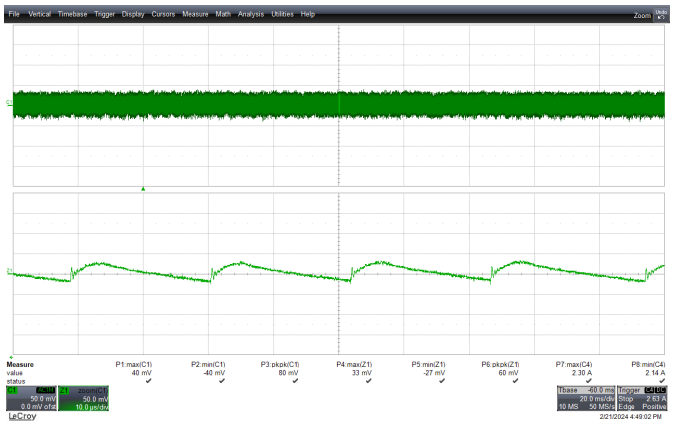


Figure 120 – Output Ripple. (PK-PK – 80 mV).
265 VAC Input, 50% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

15.7.2.4 25% Load

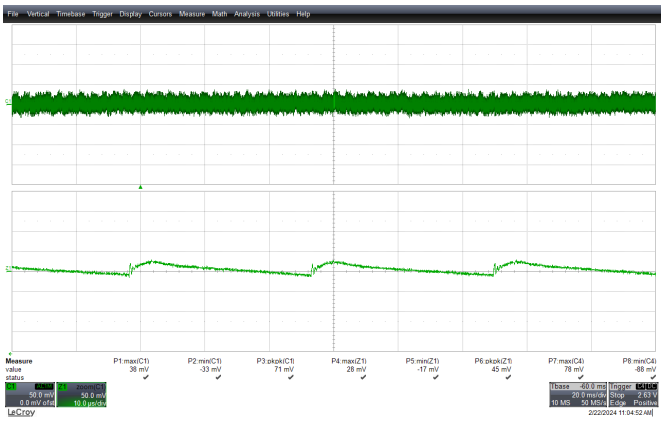


Figure 121 – Output Ripple. (PK-PK – 71 mV).
90 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

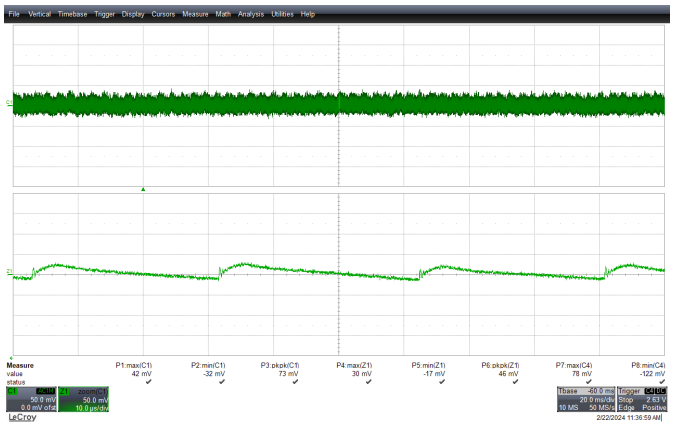


Figure 122 – Output Ripple. (PK-PK – 73 mV).
115 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

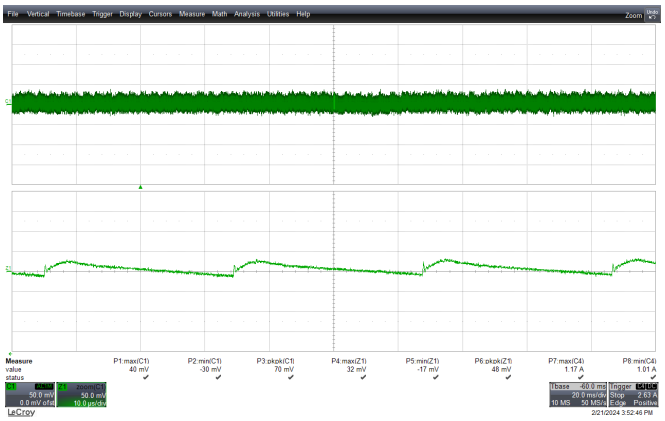


Figure 123 – Output Ripple. (PK-PK – 70 mV).
230 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

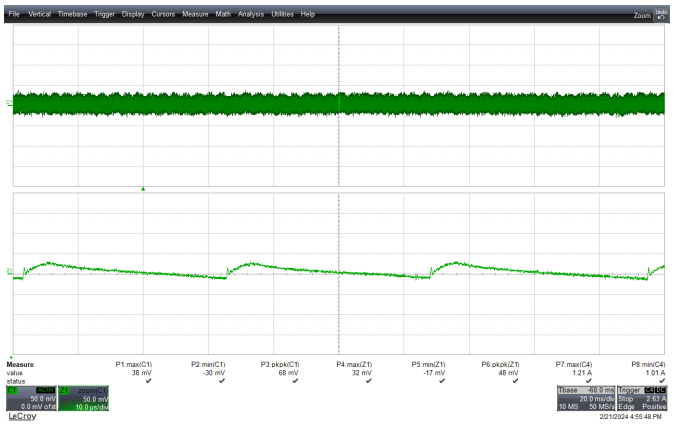


Figure 124 – Output Ripple. (PK-PK – 68 mV).
265 VAC Input, 25% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

15.7.2.5 10% Load

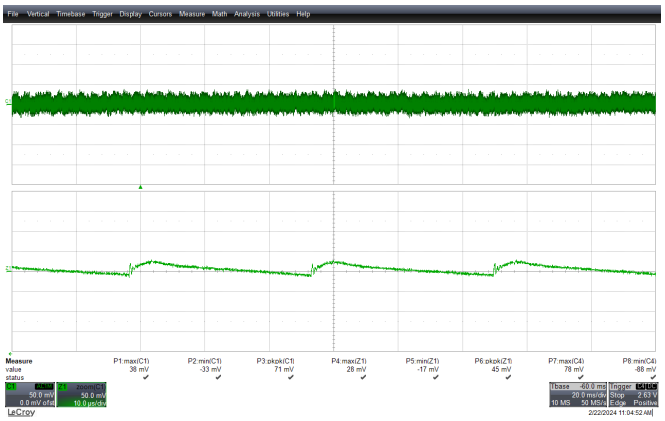


Figure 125 – Output Ripple. (PK-PK – 71 mV).
90 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

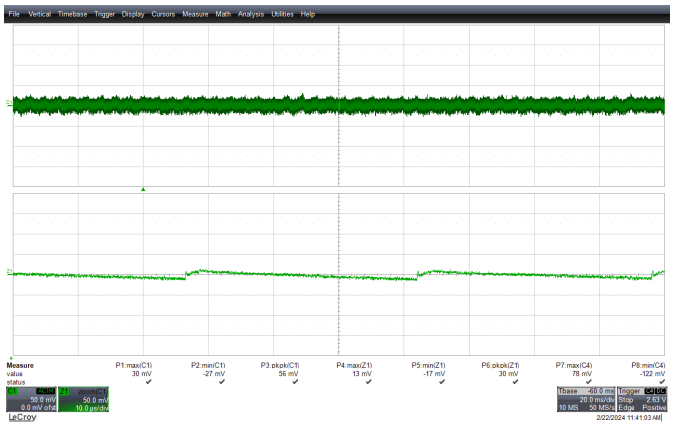


Figure 126 – Output Ripple. (PK-PK – 56 mV).
115 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

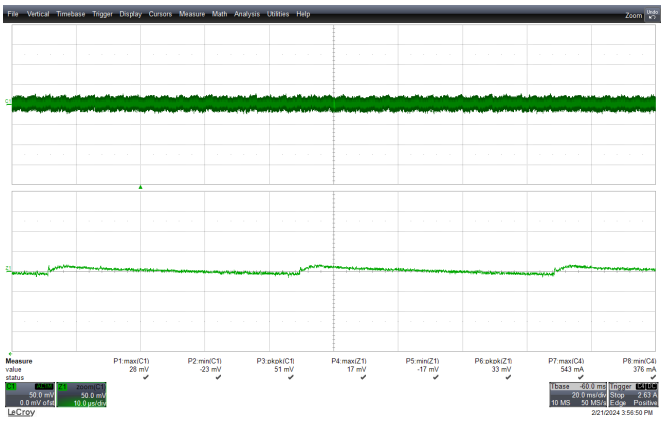


Figure 127 – Output Ripple. (PK-PK – 51 mV).
230 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

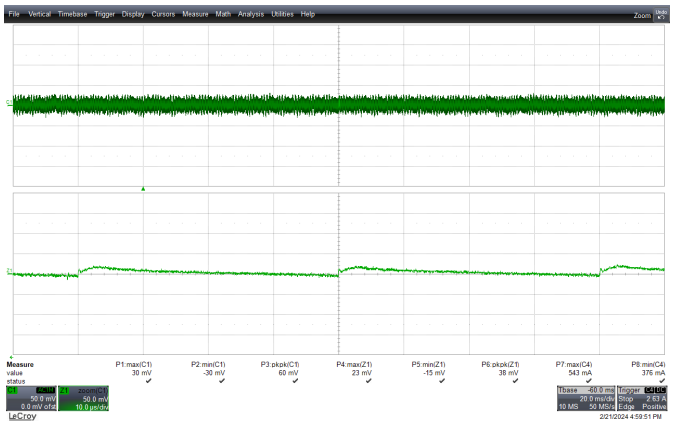


Figure 128 – Output Ripple. (PK-PK – 60 mV).
265 VAC Input, 10% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

15.7.2.6 0% Load

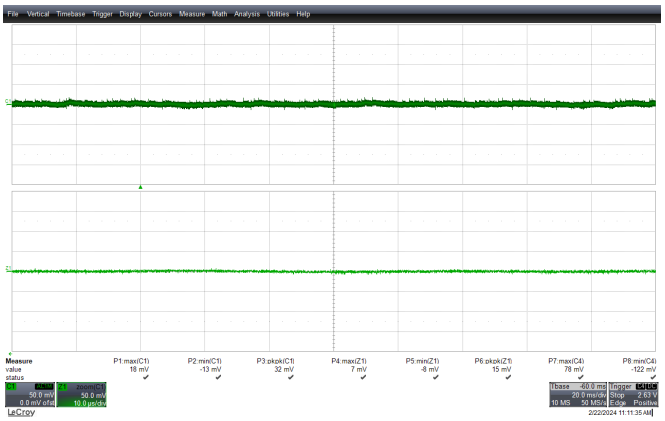


Figure 129 – Output Ripple. (PK-PK – 32 mV).
90 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

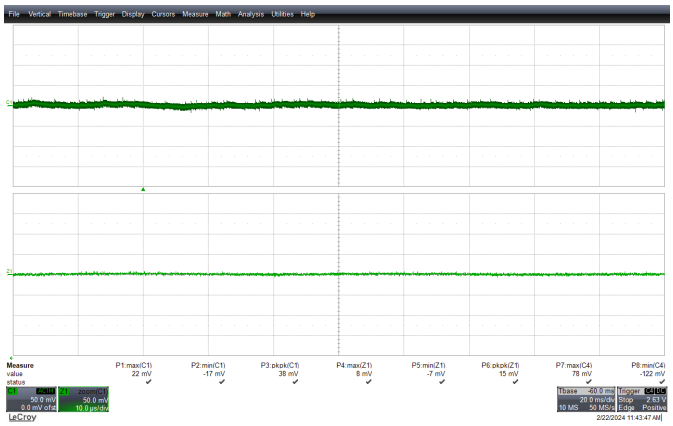


Figure 130 – Output Ripple. (PK-PK – 38 mV).
115 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

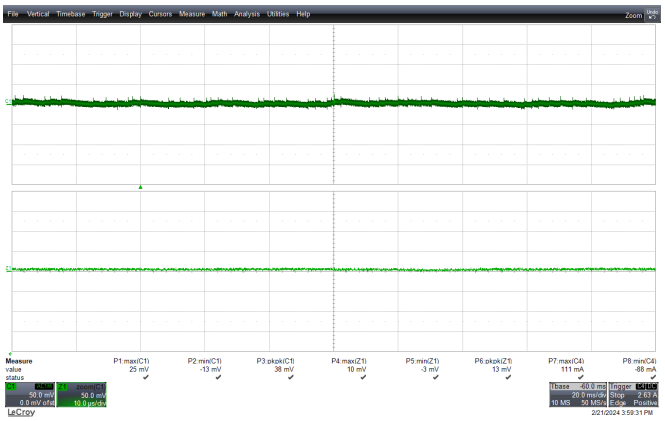


Figure 131 – Output Ripple. (PK-PK – 38 mV).
230 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

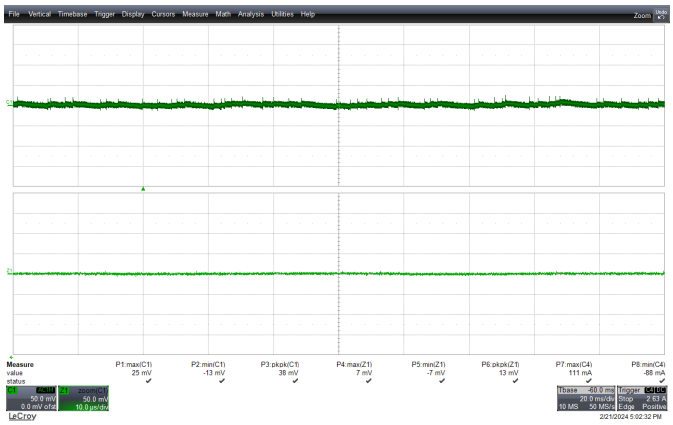


Figure 132 – Output Ripple. (PK-PK – 38 mV).
265 VAC Input, 0% Load.
V_{OUT_RIPPLE}, 50 mV / div, 20 ms / div.
Zoom: 10 μs.

15.7.3 Output Voltage Ripple

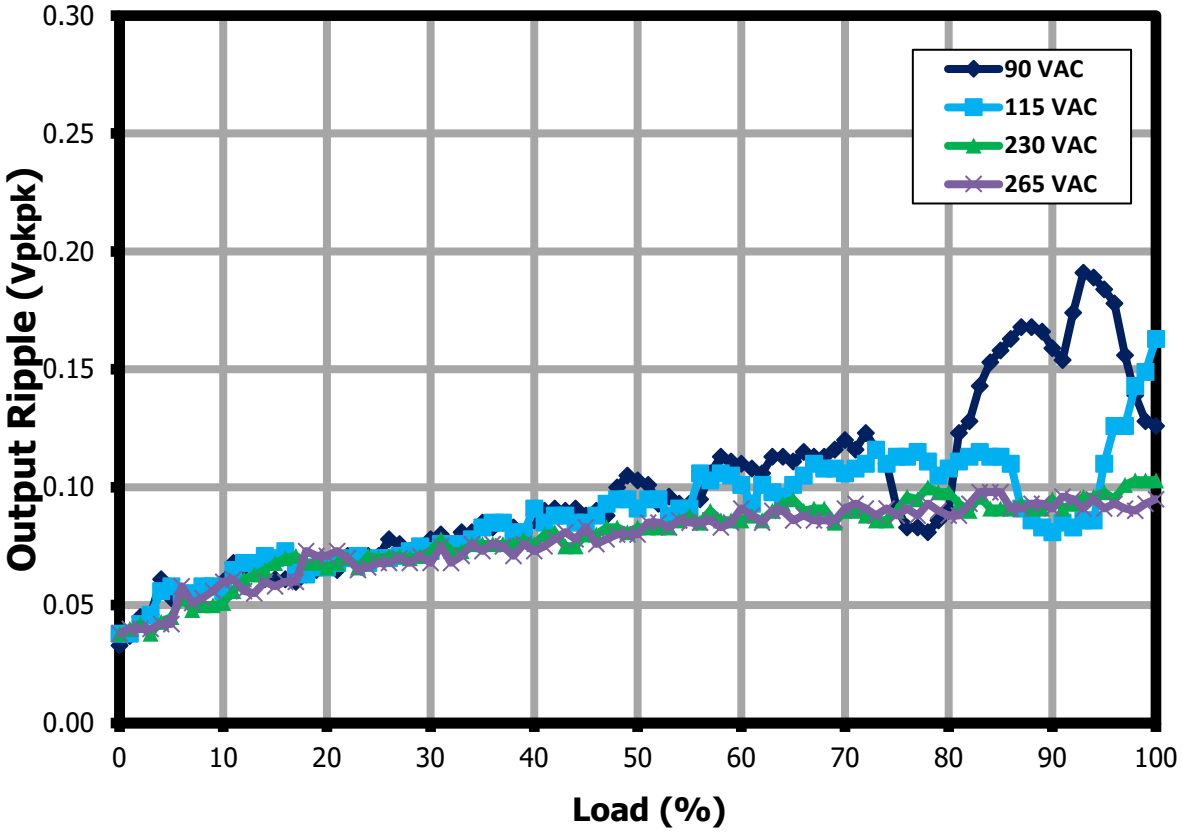


Figure 133 – Output Ripple.

15.8 Overvoltage Protection

Figure 134 – 90 VAC, I_{OUT} = 5 A (Full-Load).
OVP Running Short.
CH 1: Output Voltage: 5 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 29.6 V

Figure 135 – 265 VAC, I_{OUT} = 5 A (Full-Load).
OVP Running Short
CH 1: Output Voltage: 5 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 29.4 V

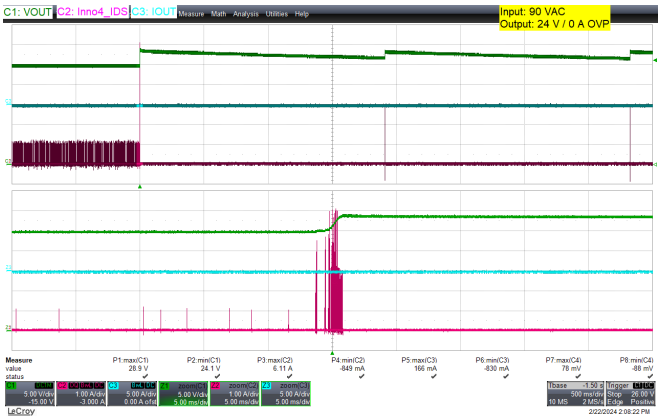


Figure 136 – 90 VAC, I_{OUT} = 0 A (No-Load).
OVP Running Short.
CH 1: Output Voltage: 5 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 28.9 V

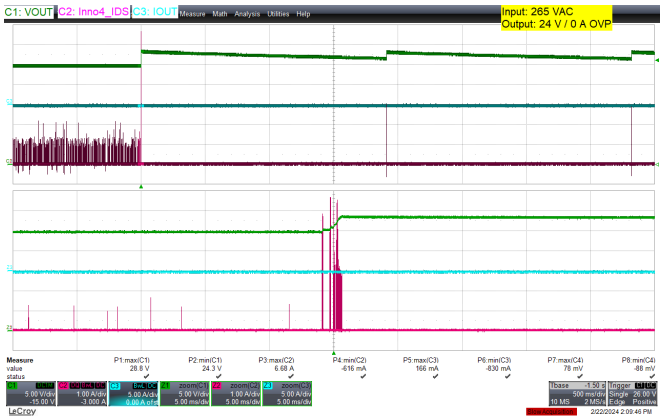


Figure 137 – 265 VAC, I_{OUT} = 0 A (No-Load).
OVP Running Short
CH 1: Output Voltage: 5 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 28.8 V

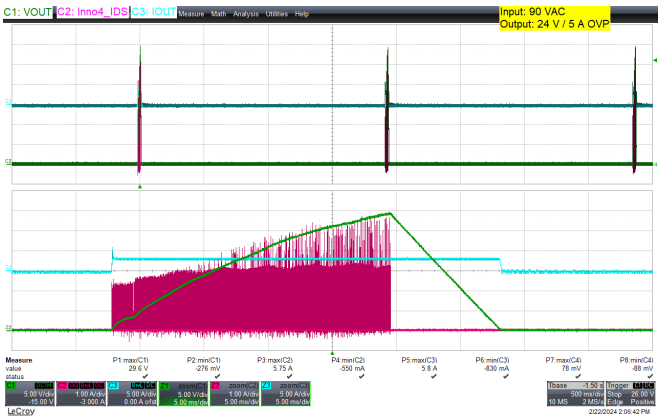


Figure 138 – 90 VAC, I_{OUT} = 5 A (Full-Load).
OVP Startup.
CH 1: Output Voltage: 5 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 29.6 V

Figure 139 – 265 VAC, I_{OUT} = 5 A (Full-Load).
OVP Startup
CH 1: Output Voltage: 4 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 28.8 V

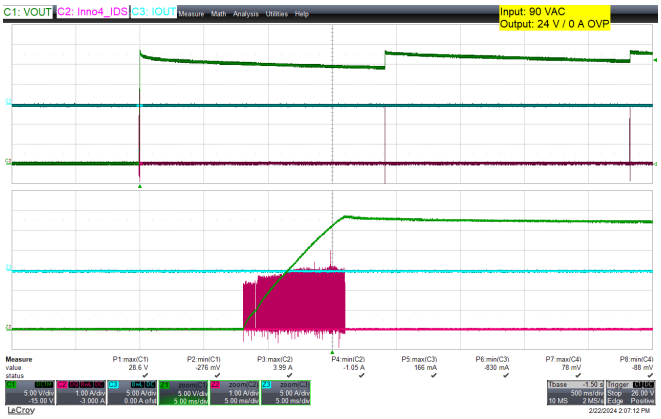


Figure 140 – 90 VAC, I_{OUT} = 0 A (No-Load).
OVP Startup.
CH 1: Output Voltage: 5 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 28.6 V

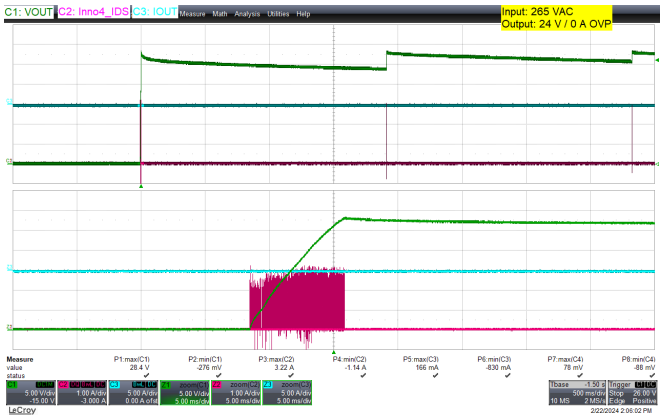


Figure 141 – 265 VAC, I_{OUT} = 0 A (No-Load).
OVP Startup
CH 1: Output Voltage: 5 V / div, 500 ms / div.
CH 2: Drain Current: 1 A / div, 500 ms / div.
CH 4: Output Current: 5 A / div, 500 ms / div.
Max Output Voltage = 28.4 V

16 Conducted EMI

16.1 Floating Output

16.1.1 Line

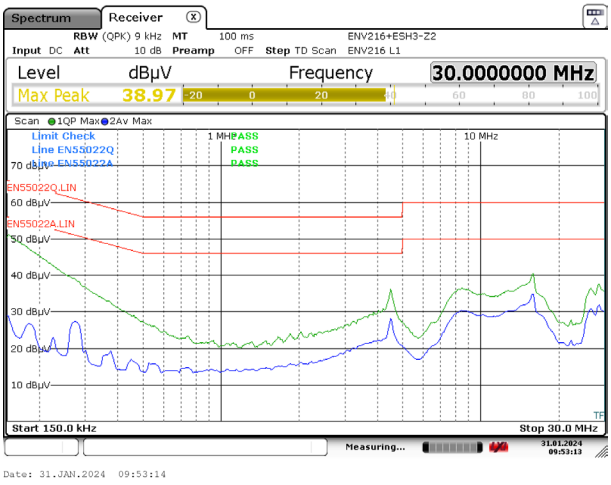


Figure 142 – Floating Output EMI, 24 V / 100% Load for 115 VAC.

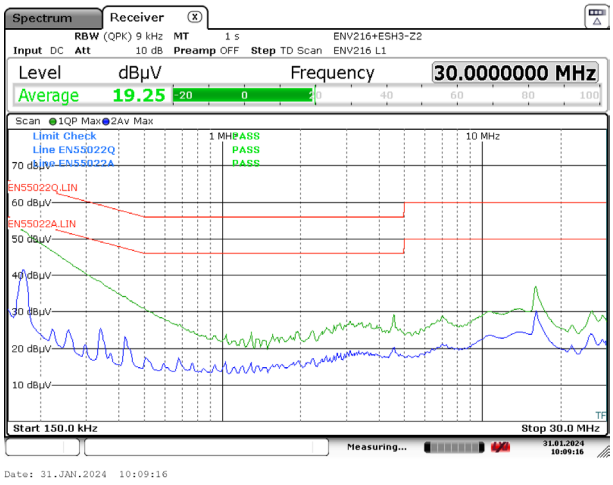


Figure 143 – Floating Output EMI, 24 V / 100% Load for 230 VAC.

16.1.2 Neutral

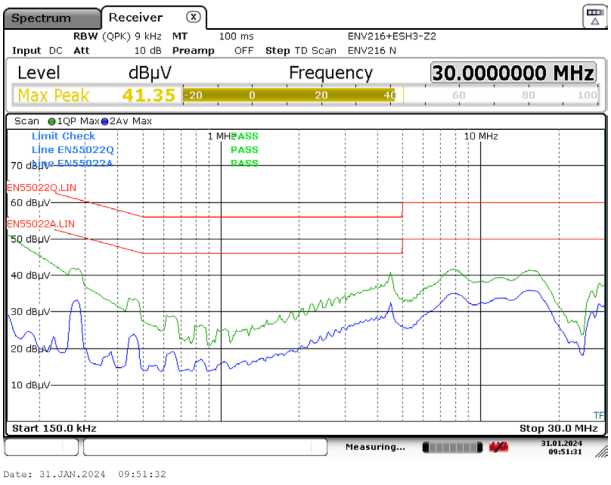


Figure 144 – Floating Output EMI, 24 V / 100% Load for 115 VAC.

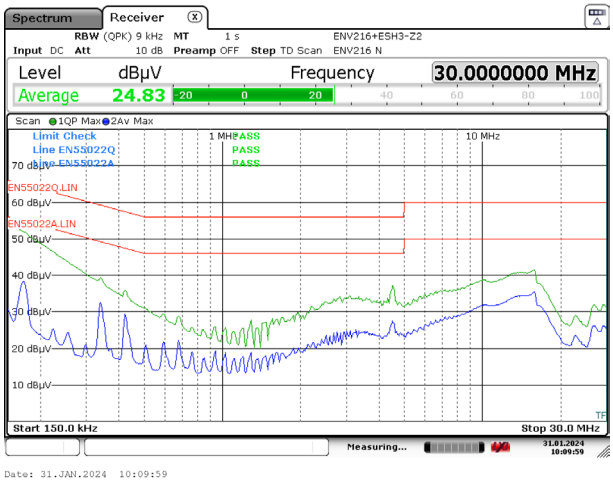


Figure 145 – Floating Output EMI, 24 V / 100% Load for 230 VAC.

16.2 Artificial Hand Output

16.2.1 Line

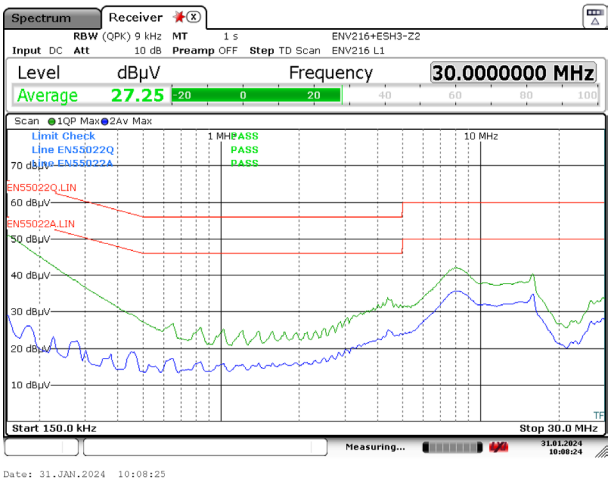


Figure 146 – Artificial hand Output EMI, 24 V / 100% Load for 115 VAC.

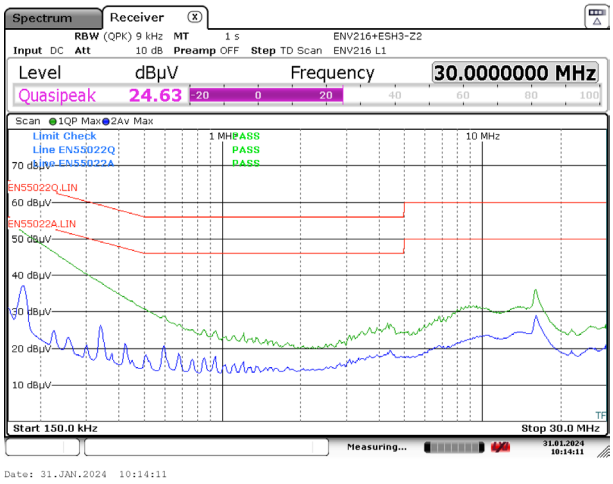


Figure 147 – Artificial hand Output EMI, 24 V / 100% Load for 230 VAC.

16.2.2 Neutral

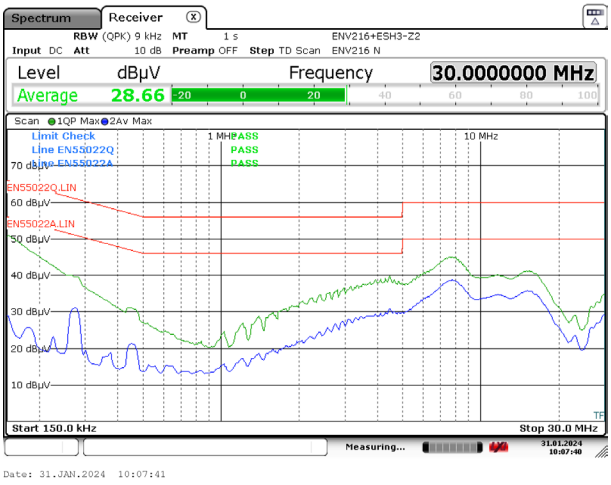


Figure 148 – Artificial hand Output EMI, 24 V / 100% Load for 115 VAC.

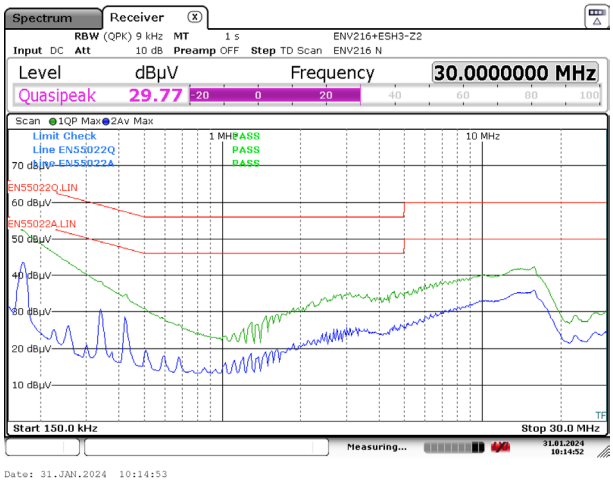


Figure 149 – Artificial Hand Output EMI, 24 V / 100% Load for 230 VAC.

16.3 Grounded Output

16.3.1 Line

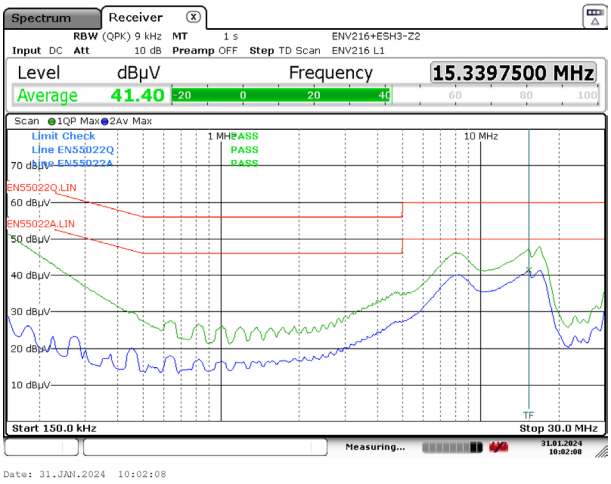


Figure 150 – Grounded Output EMI, 24 V / 100% Load for 115 VAC.

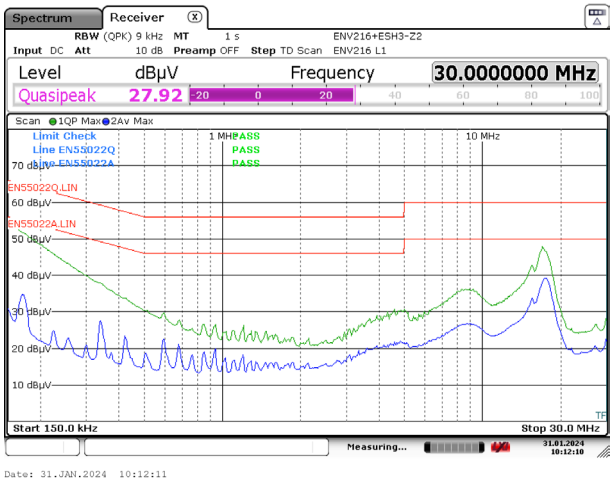


Figure 151 – Grounded Output EMI, 24 V / 100% Load for 230 VAC.

16.3.2 Neutral

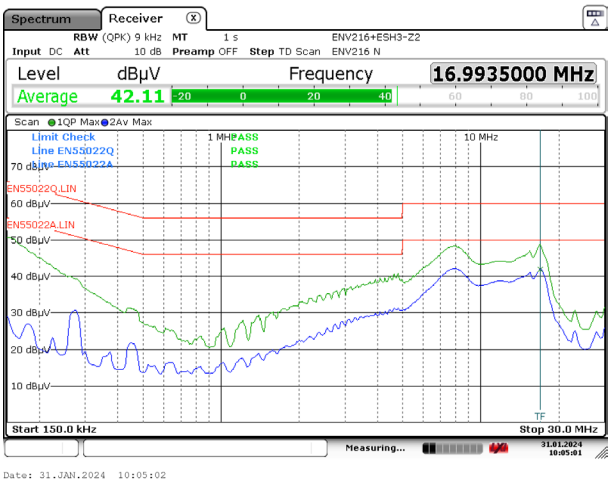


Figure 152 – Grounded Output EMI, 24 V / 100% Load for 115 VAC.

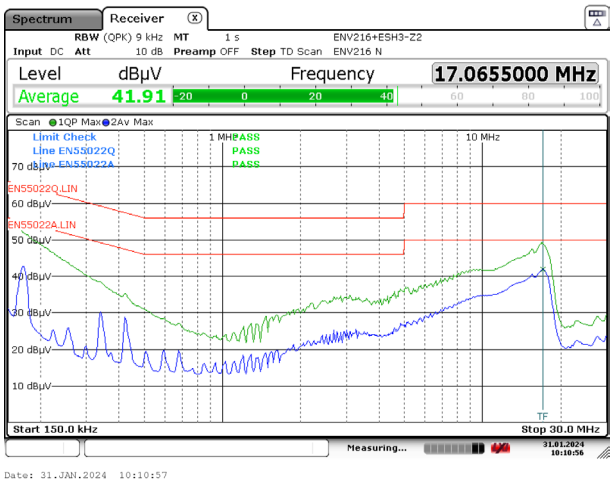


Figure 153 – Grounded Output EMI, 24 V / 100% Load for 230 VAC.

17 Line Surge

17.1 Differential Mode Test

17.1.1 230 VAC Input

Surge Voltage (V)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1000	0	L, N	2	10	Pass – No AR
–1000	0	L, N	2	10	Pass – No AR
+1000	90	L, N	2	10	Pass – No AR
–1000	90	L, N	2	10	Pass – No AR
+1000	180	L, N	2	10	Pass – No AR
–1000	180	L, N	2	10	Pass – No AR
+1000	270	L, N	2	10	Pass – No AR
–1000	270	L, N	2	10	Pass – No AR
+2000	0	L, N	2	10	Pass – No AR
–2000	0	L, N	2	10	Pass – No AR
+2000	90	L, N	2	10	Pass – No AR
–2000	90	L, N	2	10	Pass – No AR
+2000	180	L, N	2	10	Pass – No AR
–2000	180	L, N	2	10	Pass – No AR
+2000	270	L, N	2	10	Pass – No AR
–2000	270	L, N	2	10	Pass – No AR

17.2 Ring Wave Surge

17.2.1 230 VAC Input

Surge Voltage (V)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	0	L, N → PE	12	10	Pass – No AR
–6000	0	L, N → PE	12	10	Pass – No AR
+6000	90	L, N → PE	12	10	Pass – No AR
–6000	90	L, N → PE	12	10	Pass – No AR
+6000	180	L, N → PE	12	10	Pass – No AR
–6000	180	L, N → PE	12	10	Pass – No AR
+6000	270	L, N → PE	12	10	Pass – No AR
–6000	270	L, N → PE	12	10	Pass – No AR

18 EFT

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Frequency (kHz)	Burst Time	Reception Time (ms)	Step Duration (s)	Result
+4000	0	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	0	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	90	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	90	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	180	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	180	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	270	L, N - PE	5	15 ms	300	120	Pass – No AR
–4000	270	L, N - PE	5	15 ms	300	120	Pass – No AR
+4000	0	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	0	L, N - PE	100	750 µs	300	120	Pass – No AR
+4000	90	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	90	L, N - PE	100	750 µs	300	120	Pass – No AR
+4000	180	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	180	L, N - PE	100	750 µs	300	120	Pass – No AR
+4000	270	L, N - PE	100	750 µs	300	120	Pass – No AR
–4000	270	L, N - PE	100	750 µs	300	120	Pass – No AR

19 ESD

Passed ±16.5 kV air discharge and ±8.8 kV contact discharge at both output positive and negative terminals, under full load condition for 230 VAC input.

Contact Discharge

No.	Test Voltage	No. of Strikes	Discharge Location	Remarks	Pass/Fail
1	+2	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
2		10	- Output Terminal End of Cable	No Damage / No AR	Pass
3	-2	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
4		10	- Output Terminal End of Cable	No Damage / No AR	Pass
5	+4	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
6		10	- Output Terminal End of Cable	No Damage / No AR	Pass
7	-4	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
8		10	- Output Terminal End of Cable	No Damage / No AR	Pass
9	+6	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
10		10	- Output Terminal End of Cable	No Damage / No AR	Pass
11	-6	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
12		10	- Output Terminal End of Cable	No Damage / No AR	Pass
13	+8.8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
14		10	- Output Terminal End of Cable	No Damage / No AR	Pass
15	-8.8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
16		10	- Output Terminal End of Cable	No Damage / No AR	Pass

Air Discharge

No.	Test Voltage	No. of Strikes	Discharge Location	Remarks	Pass/Fail
1	+8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
2		10	- Output Terminal End of Cable	No Damage / No AR	Pass
3	-8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
4		10	- Output Terminal End of Cable	No Damage / No AR	Pass
5	+10	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
6		10	- Output Terminal End of Cable	No Damage / No AR	Pass
7	-10	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
8		10	- Output Terminal End of Cable	No Damage / No AR	Pass
9	+12	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
10		10	- Output Terminal End of Cable	No Damage / No AR	Pass
11	-12	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
12		10	- Output Terminal End of Cable	No Damage / No AR	Pass
13	+14	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
14		10	- Output Terminal End of Cable	No Damage / No AR	Pass
15	-14	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
16		10	- Output Terminal End of Cable	No Damage / No AR	Pass
17	+16.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
18		10	- Output Terminal End of Cable	No Damage / No AR	Pass
19	-16.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
20		10	- Output Terminal End of Cable	No Damage / No AR	Pass

20 Revision History

Date	Author	Revision	Description and Changes	Reviewed
21-Nov-25	MA	A	Initial Release	Apps & Mktg.

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.

https://www.power.com/company/sales/sales-offices