Design Example Report

Title	**27 W Automotive Power Supply for 800 V Systems Using InnoSwitch™3-AQ INN3949CQ**
Specification	80 VDC – 1000 VDC Input; 15.0 V / 1.8 A Output; 35 W (15 V 2.33 A) Peak Output Power; 30 VDC Start-up and Operation (7.95 W Output Power)
Application	Traction Inverter Gate-Drive or Emergency Power Supply
Author	Applications Engineering Department
Document Number	DER-1049Q
Date	November 6, 2025
Revision	A

Summary and Features

- Ultra-compact design for 800 VDC automotive BEV applications
- Low component count (only 66 electrical components)[1]
- Wide range start-up and operating voltage from <80 VDC to 1000 VDC[2] input
- Planar transformer[3] with reinforced isolation at 1000 V and complies with partial discharge (PD) and Hi-Pot requirements (IEC-60664-1 and IEC-60664-4)
- ≥85% full load efficiency across input voltage range[4]
- Accurate secondary-side regulation without optocouplers
- Provides continuous 27 W output from -40 ºC to 85 ºC
- 35 W peak power for at least seven minutes at 85 ºC
- Comprehensive fault protection including output current limit and short-circuit
- Uses automotive qualified AEC-Q surface mount (SMD) components[5,6]
- Low profile, only 15 mm height

[1] Excluding input and output ports.
[2] Derated power below 80 VDC input. See Section 14.
[3] Designed with PI Expert Online's Planar Magnetics Designer. See Section 8.2.
[4] 84.5% minimum full load efficiency across input voltage range at -40 °C ambient.
[5] Qualification of AEC-Q200 compliant transformer and common-mode input choke belongs to final design.
[6] Excluding customized transformer and input and output ports

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1 Introduction

This engineering report describes a 27 W single-output automotive power supply. It is intended for use in 800 V battery powered electric vehicles and supports a wide input range of 30 VDC to 1000 VDC. This design uses the 1700 V rated INN3949CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design uses a planar transformer with reinforced isolation between the primary (high-voltage input) and secondary (low-voltage output) sides that complies with partial discharge (PD) and Hi-Pot test requirements described in IEC-60664 parts 1 and 4. The planar transformer provides a low-profile design, ideal for applications with strict height constraints. It also offers low assembly cost and excellent transformer parameter repeatability compared to conventional wire-wound transformers.

This report contains the power supply specification, schematic, printed circuit board (PCB) layout, bill of materials (BOM), specification for the magnetics, and performance data.

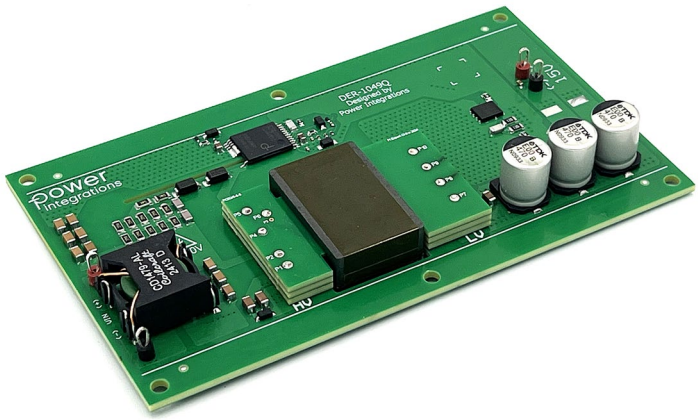


Figure 1 – Populated Circuit Board, Entire Assembly.

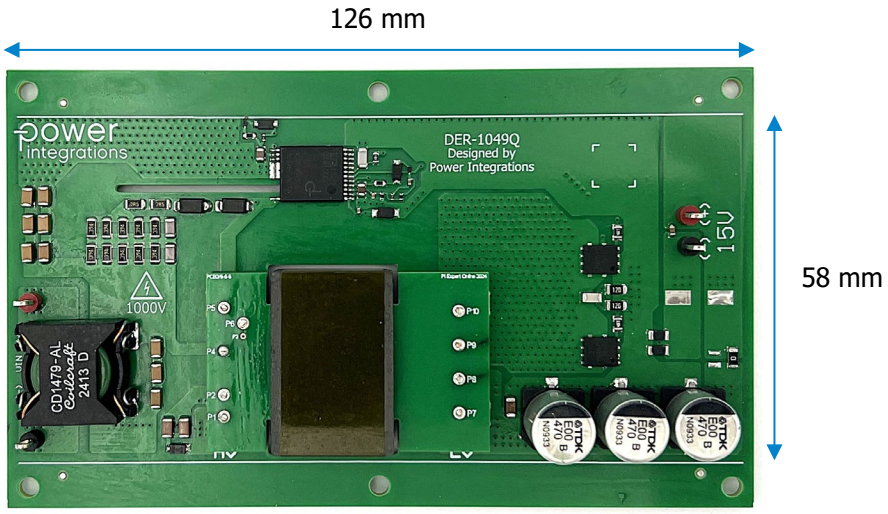


Figure 2 – Populated Circuit Board, Top.

Figure 3 – Populated Circuit Board, Side.

The design can deliver the rated 27 W output power continuously at 85 ºC ambient at an input voltage range of 80 VDC to 1000 VDC input. It is derated to 15 W with 60 V input and 7.5 W with 30 V input in the same 85 ºC ambient. The design can also deliver 35 W peak power for at least 7 minutes at 85 ºC ambient from 80 VDC to 1000 VDC input. The 15 V output is typically configured to provide a redundant power source should the 12 V system supplying the traction inverter fail. This is a typical requirement to meet functional safety by allowing the inverter to provide uninterrupted active short-circuit, active discharge, and reporting functions.

The InnoSwitch3-AQ IC maintains regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink™ magneto-inductive coupling. The secondary-side controller also simplifies the implementation of synchronous rectification improving overall efficiency (compared to diode rectification)—saving cost and space and eliminating the need for heat sinks.

2 Design Specification

The following tables represent the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV**	80	800	1000	VDC
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	V_{OUT}	14.2	15.0	15.8	VDC
Output Voltage Load and Line Regulation	V_{REG}	-5		+5	%
Ripple Voltage Measured on Board	V_{RIPPLE}			500	mV
Output Current Parameters					
Output Current	I_{OUT}		1800	2333[7]	mA
Output Power Parameters[8]					
Continuous Output Power at 80 VDC – 1000 VDC Input	P_{OUT}		27		
Peak Output Power at 80 VDC – 1000 VDC Input				35	
Output Overshoot and Undershoot During Dynamic Load Condition	ΔV_{OUT}	-5		+5	%
Operating Parameters					
Operating Switching Frequency	f_{SW}			55.5	kHz

Table 1 – Electrical Specifications.

[7] Maximum peak output current at peak output power.
[8] From -40 to 85 ºC ambient. For maximum output power capability at V_{IN} less than 80 VDC, see Section 14.

2.2 Isolation

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949CQ	$\mathbf{BV_{DSS}}$			1700	V
System Voltage	$\mathbf{V_{SYSTEM}}$			1360	V
Working Voltage	$\mathbf{V_{WORKING}}$			1000	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175		399	
Rated Impulse Voltage	$\mathbf{V_{IMPULSE}}$			2.5	kV
Altitude Correction Factor for h_a	$\mathbf{C_{ha}}$			1.59	
Technical Cleanliness Requirement				0.0	mm
Basic Clearance Distance Requirement	$\mathbf{CLR_{BASIC}}$	2.4			mm
Reinforced Clearance Distance Requirement	$\mathbf{CLR_{REINFORCED}}$	4.8			mm
Basic Creepage Distance Requirement for PCB	$\mathbf{CPG_{BASIC(PCB)}}$	5.0			mm
Reinforced Creepage Distance Requirement for PCB	$\mathbf{CPG_{REINFORCED(PCB)}}$	10.0			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	$\mathbf{V_{ISO}}$	5000			V_{PK}
Partial Discharge Test Voltage	$\mathbf{V_{PD\_TEST}}$	2100			V_{PK}

Table 2 – Isolation Coordination[9].

2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		85	ºC
Altitude of Operation	ha			5500	m
Relative Humidity	Rh			85	%

Table 3 – Environmental Specifications.

[9] Clearance and creepage distances were derived from IEC 60664-1 and IEC 60664-4.

3 Schematic[10]

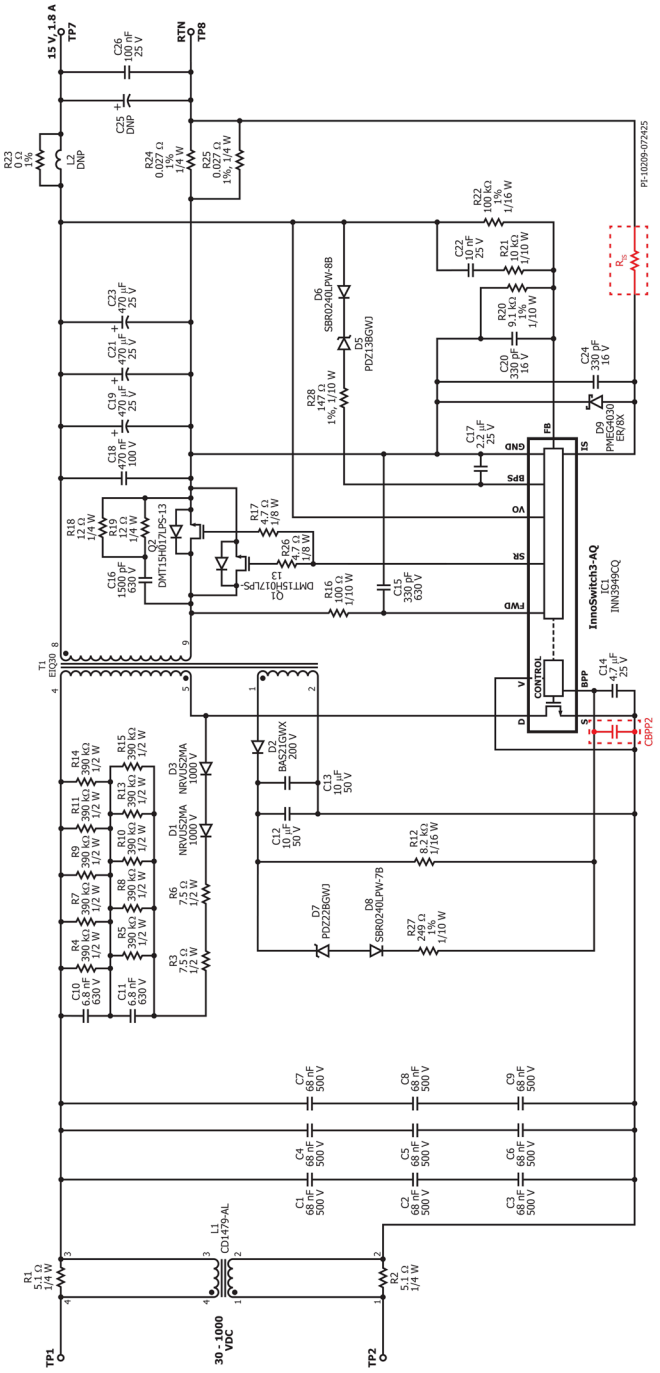


Figure 4 – DER-1049Q Schematic.

[10] The components highlighted in red (enclosed within the dashed box) are not included in DER-1049Q board but are recommended for functional safety. A redundant BPP capacitor C_{BPP2} is recommended for increased robustness, while R_{IS} is recommended for IS pin filtering. For this design example, C_{BPP2} is open while R_{IS} is shorted (no footprint).

4 Circuit Description

4.1 Input Filter

The automotive inverter environment is harsh, characterized by high dv/dt and di/dt from the switching action of the power modules. Large common-mode currents are generated across the isolation barrier of the power supply which can interfere with the operation of the power supply and other inverter blocks and compromise the integrity of signal measurement. The input common-mode choke L1 together with the bypass capacitors C1 to C9 help filter unwanted noise to prevent it from affecting the overall performance of the design.

Common-mode inductor L1 was selected to enable the reference board to withstand the Power Integrations internal Resistance-to-ripple-on-high-voltage-network test. The test injects high frequency ripple onto the high-voltage input to simulate the actual DC-link capacitor ripple seen in a traction inverter. The final value of L1 will depend on the application requirement. Higher noise will require an increased inductance value for L1. Consideration should be given to the DC resistance (DCR) which increases with higher inductance and can impact the overall efficiency of the design.

Bypass capacitors C1 to C9 were selected so as not to exceed 65% of their voltage rating as well as to maintain enough pad separation to meet creepage and clearance requirements. Resistors R1 and R2 provide damping to reduce the imposition of oscillation to the input voltage during each switching cycle.

4.2 High-Voltage Circuit

The power supply is a flyback converter topology that provides an isolated low voltage output from the high-voltage input. The primary winding of flyback transformer T1 is connected between the high-voltage DC input and the drain terminal of the 1700 V SiC power switch which is internal to InnoSwitch3-AQ IC (IC1).

An RCD type snubber circuit is placed across the primary winding, to limit the drain-source voltage peak across the primary switch during turn-off. Two super-fast surface-mount AEC-Q qualified diodes D1 and D3 were placed in series to meet creepage and clearance requirements and ensure that the voltage across the diodes would not exceed 70% of their maximum rating. Capacitors C10 and C11 captures energy from the leakage inductance of transformer T1. The capacitor values were selected to minimize voltage ripple across the snubber resistor network and maintain nearly constant power dissipation through the switching period. Resistors R4, R5, R7, R8, R9, R10, R11, R13, R14 and R15 dissipate the energy stored in the snubber capacitors. The resistor values were selected such that the voltage across each did not exceed 80% of their maximum rating and was below 50% of maximum power rating. The cooling area for the snubber resistors was also considered to ensure that the resistor temperature would be at an acceptable level.

During normal operation, the primary-side block is powered by an auxiliary winding on transformer T1. This minimizes the power derived from the internal high-voltage current source and improves the overall converter efficiency and reduces heating of IC1. The output of the auxiliary winding is rectified, and DC filtered using diode D2 and capacitors C12 and C13. The DC filtered voltage is applied to the BPP pin through resistor R12. The resistor value is chosen to allow sufficient current to ensure operation of IC1 during switching.

IC1 is self-starting, using an internal high-voltage current source to charge the BPP capacitor C14. InnoSwitch3-AQ IC will typically start below the 30 V specification requirement. Diodes D7, D8, and resistor R27 serve as a primary-sensed output overvoltage protection (primary OVP) circuit, which injects current to the BPP pin of InnoSwitch3-AQ IC during output overvoltage events, driving the IC to enter auto-restart (AR) as long as the fault is present.

In this design, the input undervoltage and overvoltage features were disabled by shorting the V pin to the SOURCE pin. This allows the design to operate at inputs as low as 30 VDC. Output voltage regulation at high load may increase at voltages < 80 VDC.[11] If the output voltage fails to reach 90% of nominal value within 60 ms ($t_{SS(RAMP)}$ + $t_{FB(AR)}$) during start-up, an auto-restart fault is triggered which forces a 2 s off time. This will result in an output voltage "hiccup" where the output rises but fails to reach regulation. If this output response is not acceptable, then the undervoltage feature can be implemented. Please refer to the InnoSwitch3-AQ data sheet and design guide for information about the recommended undervoltage-lockout circuit.

4.3 Low-Voltage Circuit

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing and gate drive for the secondary MOSFET providing synchronous rectification (SR). The voltage across the secondary winding of transformer T1 is rectified by the synchronous rectifier MOSFETs Q1 and Q2 then DC filtered by capacitors C18, C19, C21 and C23. High frequency ringing during switching is reduced by the RC snubber formed by resistors R18, R19 and capacitor C16.

Switching of Q1 and Q2 is controlled by the secondary-side controller inside IC1. Control timing is based on the negative edge of the voltage transition detected on the FWD pin via resistor R16. Capacitor C15 and R16 form a low pass filter that reduces the voltage spike seen by the FWD pin and ensures that the maximum rating of 150 V is not exceeded.

In continuous conduction mode operation, the primary-side power switch is turned off just prior to the secondary-side controller requesting a new switching cycle from the primary. In discontinuous conduction mode, the SR MOSFET is turned off when the voltage-drop

[11] Output current is derated at voltages less than 80 V.

across it rises above $V_{SR(TH)}$. The secondary-side control of the primary-side power switch prevents cross conduction ensuring reliable synchronous rectifier operation.

The secondary-side of the InnoSwitch3-AQ IC is self-powered from either the secondary winding forward voltage (thru R16 and the FWD pin) or by the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C17 via an internal regulator.

Diodes D5, D6, and resistor R28 form the secondary-side output overvoltage protection circuit. During output overvoltage events, the diodes turn on, and current is injected into the BPS pin of InnoSwitch3-AQ IC, triggering AR. This network protects for faults on the secondary when the secondary controller is functional. When the secondary controller is not functional, the primary side BPP pin-based output OV function is recommended.

Resistors R20 and R22 form a voltage divider network that provides an analog of the output voltage to the FB pin. The InnoSwitch3-AQ IC has an internal reference of 1.265 V presented on the FB pin. Power supply output voltage is adjusted until the mid-point voltage of the sense network reaches this value. Capacitor C20 provides decoupling of high frequency noise. Capacitor C22 and R21 form a feedforward network to speed up the feedback response and lower output ripple. Resistor R23 is installed by default and is used to short inductor L2 when the output LC filter is not needed. If lower output ripple is required, remove R23 and install the appropriate inductor L2 and capacitor C25.

Output current is measured by monitoring the voltage drop across resistors R24 and R25 which are connected in parallel. The resulting current information is filtered by decoupling capacitor C24 and monitored by the IS pin referenced to the SECONDARY GROUND pin. A low internal current sense threshold of 35 mV is used to reduce losses. Once the threshold is exceeded, secondary request will be inhibited causing output voltage to drop. The IC will enter auto-restart (AR) when the output voltage feedback is below 90% of target and will recover when the load current is reduced below the target threshold. Diode D9 limits the voltage drop across resistors R24 and R25 to protect the IS pin during overload or short-circuit conditions.

5 PCB Layout

5.1 Main Board PCB

Layers: Six (6) (typical for traction inverter control board)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 2 oz

Figure 5 – DER-1049Q PCB Layout.

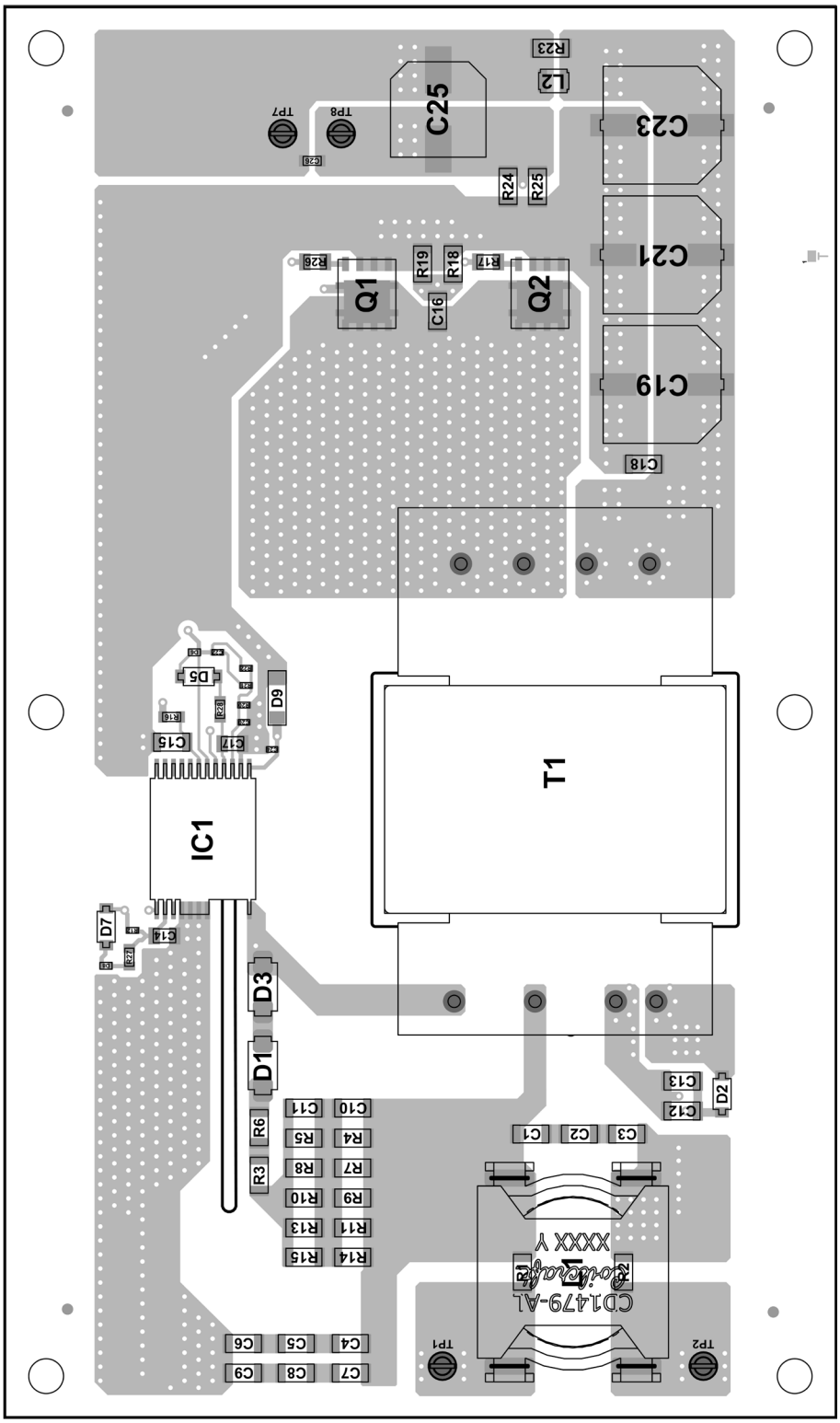


Figure 6 – DER-1049Q PCB Assembly (Top).

5.2 Planar Transformer PCB

Layers: Six (6)
Board Material: FR4
Board Thickness: 1.57 mm (±10%)
Copper Weight: 2 oz

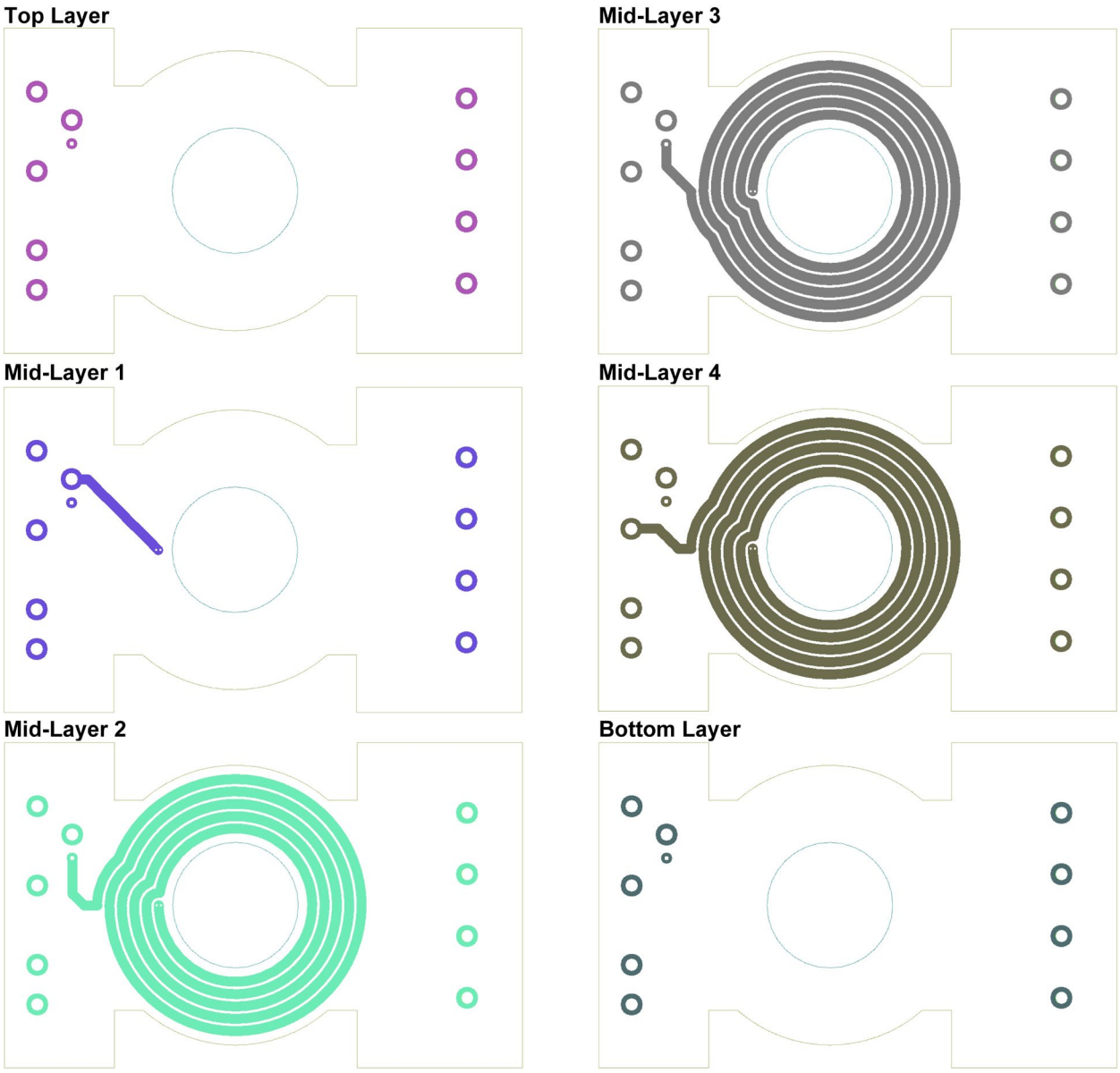


Figure 7 – DER-1049Q Planar Transformer PCB1 Layout.

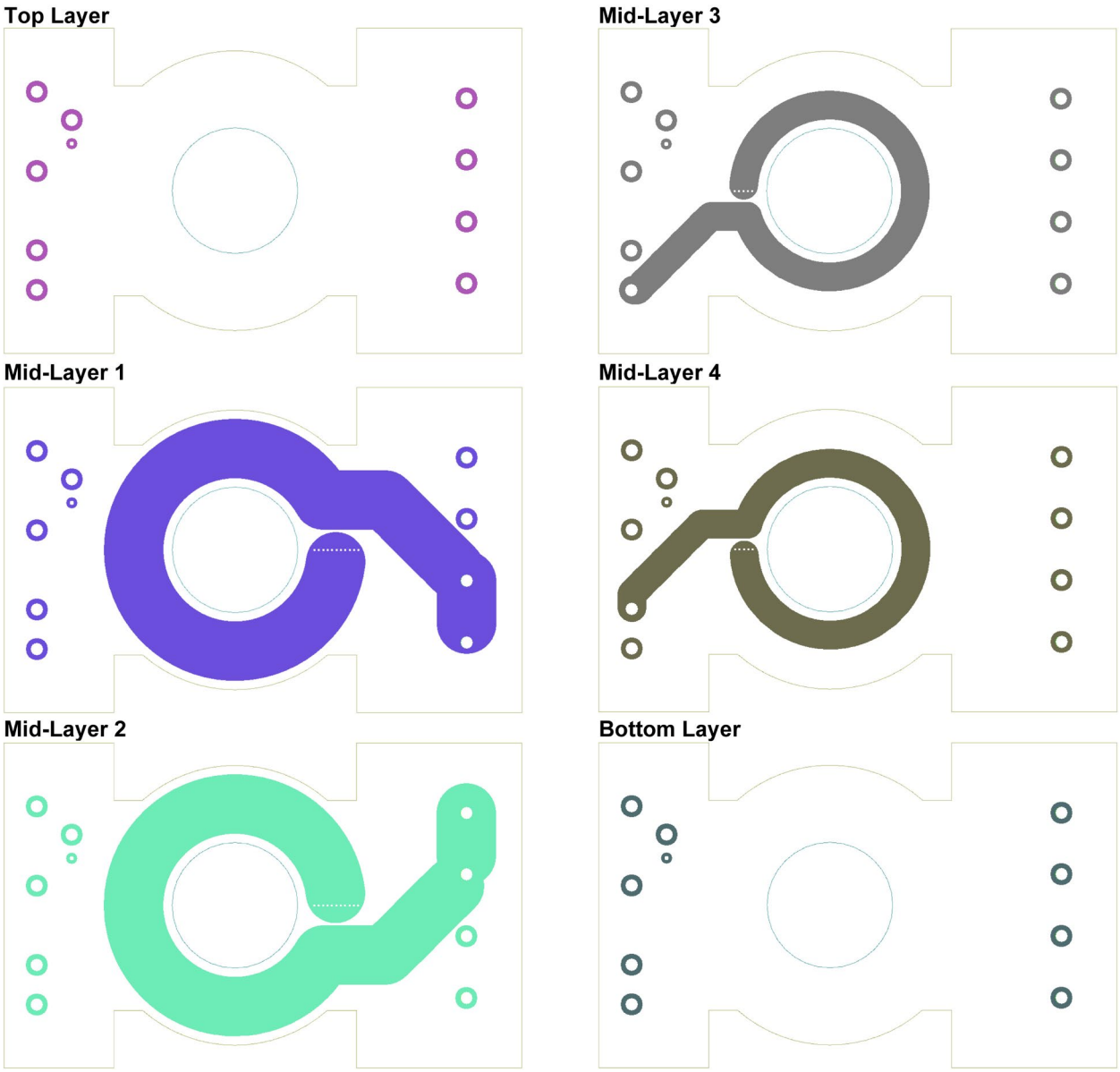


Figure 8 – DER-1049Q Planar Transformer PCB2 Layout.

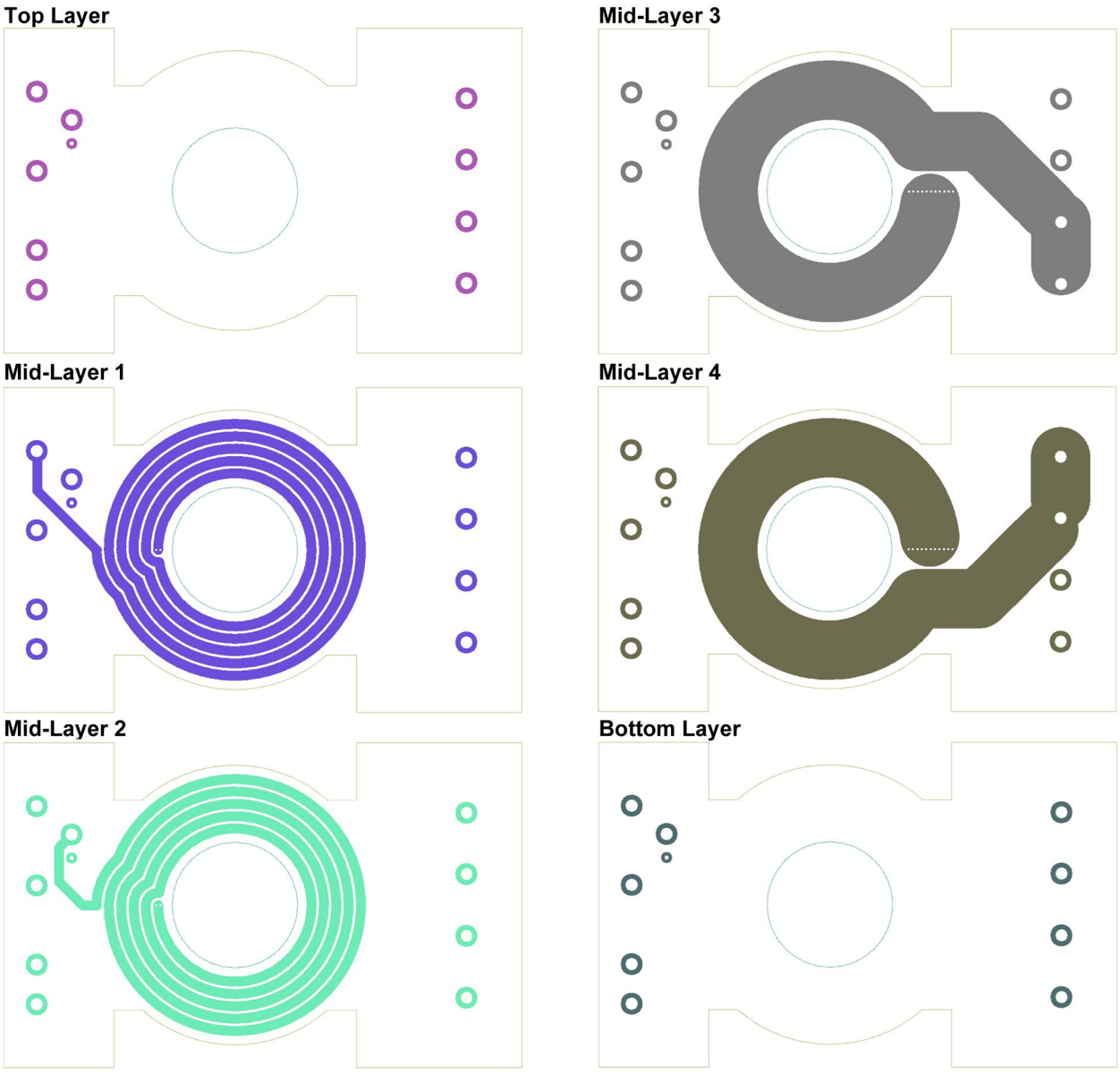


Figure 9 – DER-1049Q Planar Transformer PCB3 Layout.

6 Bill of Materials

Item	Quantity	Designator	Description	Mfr. Part Number	Manufacturer
1	9	C1, C2, C3, C4, C5, C6, C7, C8, C9	Multilayer Ceramic Capacitors MLCC - SMD/SMT 68n X7R 500 V 10%1206 AEC-Q200	C1206C683KCRACAUTO	KEMET
2	2	C10, C11	Multilayer Ceramic Capacitors MLCC - SMD/SMT 6.8n C0G 630 V 5%1206 AEC-Q200	CGA5H4C0G2J682J115AE	TDK
3	2	C12, C13	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10u X7R 50 V 10%1206 AEC-Q200	CGA5L1X7R1H106K160AE	TDK
4	1	C14	Multilayer Ceramic Capacitors MLCC - SMD/SMT 4.7u X7R 25 V 20%805 AEC-Q200	CGA4J1X7R1E475M125AC	TDK
5	1	C15	Multilayer Ceramic Capacitors MLCC - SMD/SMT 330p C0G 630 V 5%1206 AEC-Q200	CGA5C4C0G2J331J060AA	TDK
6	1	C16	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1500p C0G 630 V 5%1206 AEC-Q200	CGA5H4C0G2J152J115AA	TDK
7	1	C17	Multilayer Ceramic Capacitors MLCC - SMD/SMT 2.2u X7R 25V 10%805 AEC-Q200	C0805C225K3RACAUTO	KEMET
8	1	C18	Multilayer Ceramic Capacitors MLCC - SMD/SMT 470n X7R 100 V 10%1206 AEC-Q200	HMK316B7474KLHT	Taiyo Yuden
9	3	C19, C21, C23	Polymer Aluminum Capacitor 470u AL 25V 20%10x12.5mm AEC-Q200	B40900B5477M000	TDK
10	2	C20, C24	Multilayer Ceramic Capacitors MLCC - SMD/SMT 330p X7R 16 V 10%402 AEC-Q200	VJ0402Y331KLJAJ32	Vishay
11	1	C22	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10n X7R 25 V 10%402 AEC-Q200	CGA2B2X7R1E103K050BA	TDK
12	1	C26	Multilayer Ceramic Capacitors MLCC - SMD/SMT 100n X7R 25 V 10%603 AEC-Q200	CGA3E2X7R1E104K080AA	TDK
13	2	D1, D3	Diode Standard 1000 V 1.5A SMT DO-214AC AEC-Q101	NRVUS2MA	onsemi
14	1	D2	Diode Standard 200 V 225mA SMT SOD-123 AEC-Q101	BAS21GWX	Nexperia
15	1	D5	Diode Zener 13 V 365 mW SMT SOD-123 AEC-Q101	PDZ13BGWJ	Nexperia
16	2	D6, D8	Diode Standard 40 V 200mA SMT X1-DFN1006-2 AEC-Q	SBR0240LPW-7B	Diodes, Inc.
17	1	D7	Diode Zener 22 V 365 mW SMT SOD-123 AEC-Q101	PDZ22BGWJ	Nexperia
18	1	D9	Diode Schottky 40 V 3A Surface Mount SOD-123	PMEG4030ER-QX	Nexperia
19	1	IC1	CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3949CQ	Power Integrations
20	1	L1	Input Common Mode Choke	CD1479-AL	Coilcraft
21	2	Q1, Q2	N-Channel MOSFET: 150 V 9.4 A PowerDI5060-8	DMT15H017LPS-13[12]	Diodes, Inc.
22	2	R1, R2	Thick Film Resistors - SMD 5.1 Ohms 250 mW 1206 1% AEC-Q200 Standard Power Version	AC1206FR-075R1L	YAGEO
23	2	R3, R6	Thick Film Resistors - SMD 1206 7.5R 5% 0.5W 200 V AEC-Q200	ESR18EZPJ7R5	ROHM Semi
24	10	R4, R5, R7, R8, R9, R10, R11, R13, R14, R15	Thick Film Resistors - SMD 1206 390K 5% 0.5W 200 V AEC-Q200	ESR18EZPJ394	ROHM Semi

[12] DMT15H017LPS-13 is qualified for AEC-Q101 reliability test only but not fully qualified for all AEC-Q criteria.

25	1	R12	Thick Film Resistors - SMD 0402 8.2K 5% 0.0625W 50 V AEC-Q200	CR0402AJW-822GLF	Bourns
26	1	R16	Thick Film Resistors - SMD 0603 100R 5% 0.1W AEC-Q200	RMCF0603JT100R	Stackpole
27	2	R17, R26	Thick Film Resistors - SMD 0805 4.7R 5% 0.125W 150 V AEC-Q200	AC0805JR-074R7L	YAGEO
28	2	R18, R19	Thick Film Resistors - SMD 1206 12R 5% 0.25W 200 V AEC-Q200	AC1206JR-0712RL	YAGEO
29	1	R20	Thick Film Resistors - SMD 0402 9.1K 1% 0.1W 50 V AEC-Q200	ERJ-2RKF9101X	Panasonic
30	1	R21	Thick Film Resistors - SMD 0402 10K 5% 0.1W 50 V AEC-Q200	ERJ-U02J103X	Panasonic
31	1	R22	Thick Film Resistors - SMD 0402 100K 1% 0.0625W AEC-Q200	RMCF0402FT100K	Stackpole
32	1	R23	Thick Film Resistors - SMD 1206 0R 1% 0.25W 200 V AEC-Q200	AF1206JR-070RL	YAGEO
33	2	R24, R25	Thick Film Resistors - SMD 1206 0.027R 1% 0.25W AEC-Q200	WSL1206R0270FEA	Vishay
34	1	R27	Thick Film Resistors - SMD 0603 249ohms 1% AEC-Q200	ERJ-3EKF2490V	Panasonic
35	1	R28	Thick Film Resistors - SMD 0603 147ohms 1% AEC-Q200	ERJ-3EKF1470V	Panasonic
36	1	T1	35 W Power Transformer		Power Integrations
37	1	T1-Core	3C96 Ferrite Core	EQ30 – 3C96	Ferroxcube
38	1	T1-Core	3C96 Ferrite Core	PLT30/20/3 – 3C96	Ferroxcube
39	2	TP1, TP7	Test Plugs & Test Jacks RED TEST POINT	5010	Keystone
40	2	TP2, TP8	Test Plugs & Test Jacks BLACK TEST POINT	5011	Keystone

Table 4 – DER-1049Q Bill of Materials[13].

[13] All components are AEC-Q qualified except test point connectors and magnetics T1 and L1.

7 Transformer Specification (T1)

7.1 Electrical Diagram

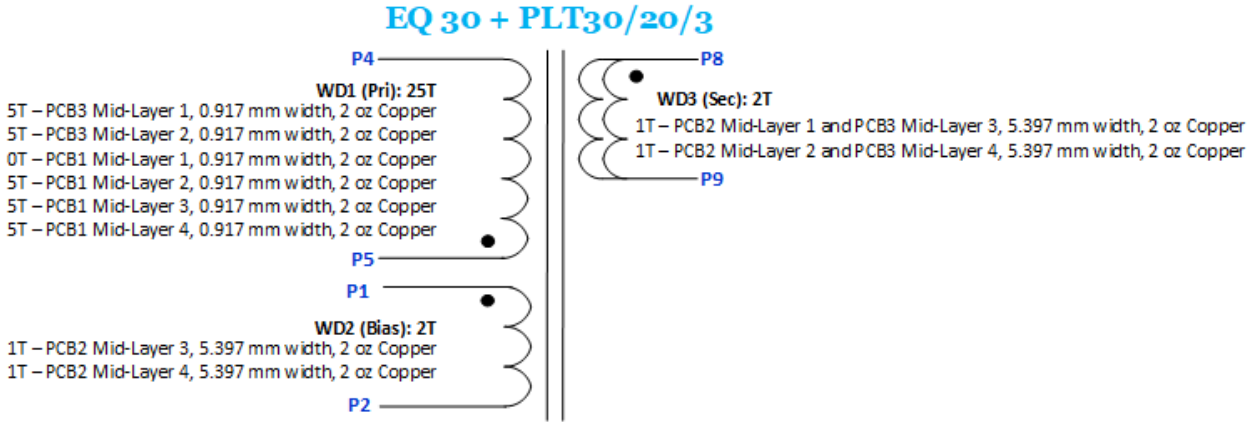


Figure 10 – Transformer Electrical Diagram.

Figure 11 – DER-1049Q Planar Transformer Test Pins.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side.		27	35[14]	W
Input voltage VDC	Flyback topology.	30	800	1000	V
Switching frequency	Flyback topology.			55.5	kHz
Duty cycle	Flyback topology.			52.8	%
Np:Ns			12.5		
Rdc	Primary side.		451		mΩ
Rdc	Secondary side.		3.58		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency, with pins 1-2 shorted, pins P4-P5 shorted and pins P8-P9 shorted at 25 ºC.		53.9		pF

[14] Peak output power for 7 minutes.

Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin P4-P5, with all other windings open at 25 ºC.		422.6		µH
Part to part tolerance	Tolerance of Primary Inductance.	-3.0		3.0	%
Primary leakage inductance	Measured between pin P4 to pin P5, with all other windings shorted.			6.2	µH

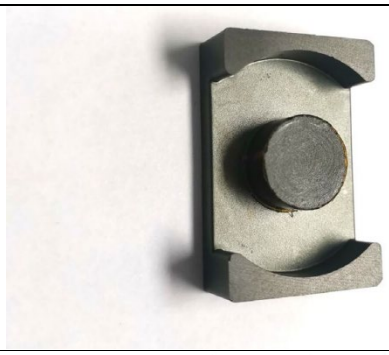
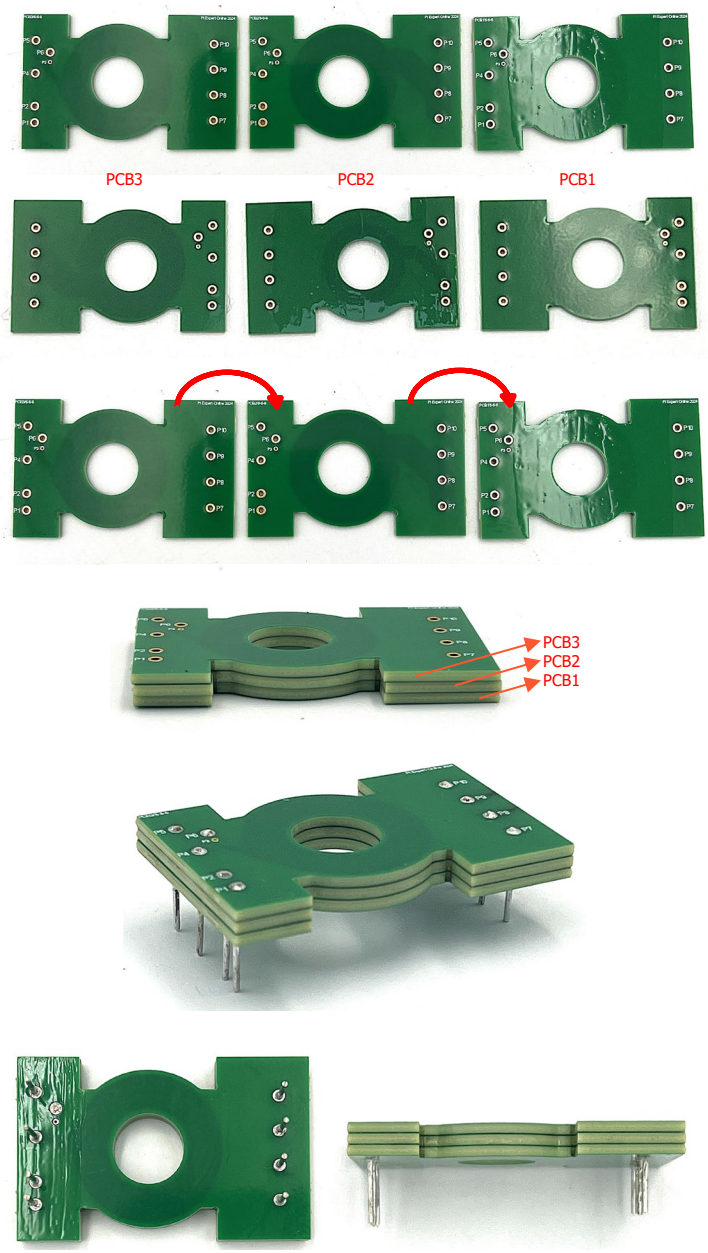
Table 5 – Transformer (T1) Electrical Specifications.

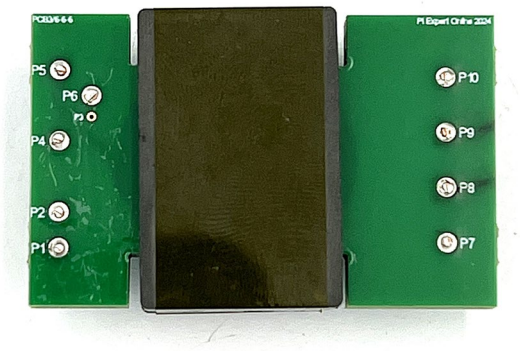
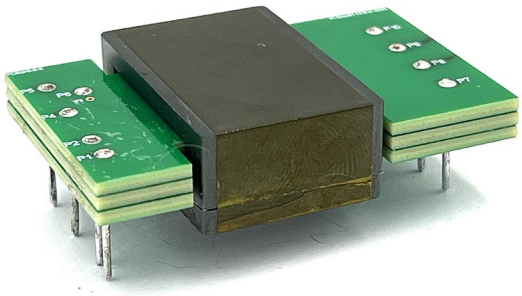
7.3 Material List

Item	Description	Qty	UOM	Material	Manufacturer
[1]	Core: EQ30	1	PC	3C96 (or equivalent)	Ferroxcube
[2]	Core: PLT30/20/3	1	PC	3C96 (or equivalent)	Ferroxcube
[3]	Single Post Terminal Connector Tin S08-46, width: 0.028" (0.70mm) length: 0.591" (15.00mm)	9	PC	Phosphor Bronze (or equivalent)	Harwin Inc.
[4]	3M Polyimide Film Tape 5413, width: 0.625 in (15.9 mm)		mm	3M 5413 0.625" X 36YD (or equivalent)	3M

Table 6 – Transformer (T1) Material List.

7.4 Transformer Assembly Instructions

Core Preparation		Gap EQ core (Item [1]) to get 422.6 µH ± 3% of inductance between pins P4 and P5.
Transformer Assembly		Prepare the three planar boards. Prior to assembly, apply conformal coating on the bottom surface of PCB2, and on the top surface of PCB1. Stack the three planar boards in the following order: PCB3 (Top) – PCB2 – PCB1 (Bottom) Insert pin connectors (Item [3]) on pins P1, P2, P4 – P10 and solder them onto the planar board stack. Remove excess connector lengths on the top side across all pins. Apply conformal coating over the primary-side pins. Remove excess connector length on the bottom side for Pin P6. Apply conformal coating over the primary-side pins.

		Mount the gapped core and fasten with tape or glue. During the evaluation, tape (Item [4]) is used to fasten the cores, as illustrated. For the final application, it is recommended to use glue instead of tape.
Finishing		Fasten the core to the PCB using epoxy. The gapped section of the core should be positioned away from the PCB.

8 Transformer Design

8.1 Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_032525; Rev.4.0; Copyright Power Integrations 2025	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	15.00		15.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	2.333		2.333	A	Output current 1
7	POUT1			35.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	80.00		80.00	V	Input DC voltage 2
13	IOUT2	2.333		2.333	A	Output current 2
14	POUT2			35.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
71	**PRIMARY CONTROLLER SELECTION**					
72	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
73	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
74	DEVICE_GENERIC			INN39X9		Device selection
75	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
76	PDEVICE_MAX			120	W	Device maximum power capability
77	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25ºC
78	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125ºC
79	ILIMIT_MIN			1.981	A	Primary switch minimum current limit
80	ILIMIT_TYP			2.130	A	Primary switch typical current limit
81	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
82	VDRAIN_ON_PRSW			0.53	V	Primary switch on-time voltage drop
83	VDRAIN_OFF_PRSW			1217.5	V	Peak drain voltage on the primary switch during turn-off
91	**WORST CASE ELECTRICAL PARAMETERS**					
92	FSWITCHING_MAX	55500		55500	Hz	Maximum switching frequency at full load and minimum DC input voltage
93	VOR	187.5		187.5	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
94	KP			2.107		Measure of continuous/discontinuous mode of operation
95	MODE_OPERATION			DCM		Mode of operation
96	DUTYCYCLE			0.528		Primary switch duty cycle
97	TIME_ON_MIN			0.75	us	Minimum primary switch on-time
99	TIME_ON_MAX			10.95	us	Maximum primary switch on-time
100	TIME_OFF			8.58	us	Primary switch off-time
101	LPRIMARY_MIN			410.0	uH	Minimum primary magnetizing inductance
102	LPRIMARY_TYP			422.6	uH	Typical primary magnetizing inductance
103	LPRIMARY_TOL	3.0		3.0	%	Primary magnetizing inductance tolerance
104	LPRIMARY_MAX			435.3	uH	Maximum primary magnetizing inductance
105	**PRIMARY CURRENT**					
106	IAVG_PRIMARY			2.019	A	Primary switch average current
107	IPEAK_PRIMARY			2.019	A	Primary switch peak current
108	IPEDESTAL_PRIMARY			0.479	A	Primary switch current pedestal

109	IRIPPLE_PRIMARY			2.019	A	Primary switch ripple current
110	IRMS_PRIMARY			0.803	A	Primary switch RMS current
114	**TRANSFORMER CONSTRUCTION PARAMETERS**					
115	**CORE SELECTION**					
116	CORE	EQ/PLT30		EQ/PLT30		Core selection
117	CORE NAME	PLT30/20/3-3C96		PLT30/20/3-3C96		Core code
118	AE	108.0		108.0	mm^2	Core cross sectional area
119	LE	36.2		36.2	mm	Core magnetic path length
121	AL	6000		6000	nH	Ungapped core effective inductance per turns squared
115	VE	3910		3910	mm^3	Core volume
128	**PRIMARY WINDING**					
129	NPRIMARY			25		Primary winding number of turns
130	BPEAK			3761	Gauss	Peak flux density
131	BMAX			3224	Gauss	Maximum flux density
132	BAC			1612	Gauss	AC flux density (0.5 x Peak to Peak)
133	ALG			676	nH	Typical gapped core effective inductance per turns squared
134	LG			0.178	mm	Core gap length
136	**SECONDARY WINDING**					
137	NSECONDARY	2		2		Secondary winding number of turns
139	**BIAS WINDING**					
140	NBIAS			2		Bias winding number of turns
144	**PRIMARY COMPONENTS SELECTION**					
145	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
146	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
147	**UNDERVOLTAGE PARAMETERS**					
148	BROWN-IN REQUIRED	30.00		30.00	V	Required DC bus brown-in voltage threshold
149	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
150	VZ			9.10	V	Zener diode reverse voltage
151	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
152	ILKG			2.00	uA	Zener diode maximum reverse leakage current
153	ILKG_MIN			0.10	uA	Zener diode minimum reverse leakage current
154	BROWN-IN ACTUAL			21.52 - 29.83	V	Actual brown-in voltage range using standard resistors
155	BROWN-OUT ACTUAL			18.31 - 26.75	V	Actual brown-out voltage range using standard resistors
156	**OVERVOLTAGE PARAMETERS**					
157	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
158	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
159	VF				V	OV diode forward voltage
160	VRRM				V	OV diode reverse voltage
161	PIV				V	OV diode peak inverse voltage
162	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
163	**DC BUS SENSE RESISTORS**					
164	RLS_H			0.83	MΩ	Connect five 140 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
165	RLS_L			127	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
168	**BIAS WINDING**					
169	VBIAS	9.00		9.00	V	Rectified bias voltage
170	VF_BIAS	1.00		1.00	V	Bias winding diode forward drop

171	VREVERSE_BIASDIODE			89.00	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
172	CBIAS			22	uF	Bias winding rectification capacitor
173	CBPP			4.70	uF	BPP pin capacitor
177	**SECONDARY COMPONENTS SELECTION**					
178	**FEEDBACK COMPONENTS**					
179	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
180	RFB_LOWER			9.31	kΩ	Lower feedback resistor
181	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
185	**MULTIPLE OUTPUT PARAMETERS**					
186	**OUTPUT 1**					
187	VOUT1			15.00	V	Output 1 voltage
188	IOUT1			2.333	A	Output 1 current
189	POUT1			35.00	W	Output 1 power
190	IRMS_SECONDARY1			6.536	A	Root mean squared value of the secondary current for output 1
191	IRIPPLE_CAP_OUTPUT1			6.106	A	Current ripple on the secondary waveform for output 1
192	NSECONDARY1			2		Number of turns for output 1
193	VREVERSE_RECTIFIER1			95.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
194	SRFET1	DMT15H017LPS-13		DMT15H017LPS-13		Secondary rectifier (Logic MOSFET) for output 1
195	NUM_SRFET1	2		2		Number of SRFETs in parallel for output 1
196	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
197	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
198	RDSON_SRFET1			37	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
237	PO_TOTAL			35.00	W	Total power of all outputs

Table 7 – DER-1049Q PIXls Spreadsheet.

8.2 Magnetics Designer

The planar transformer was designed exclusively with PI Expert Online's Magnetics Designer tool. Figure 12 below shows a screenshot of the design's final planar transformer design inside the designer tool interface. Section 8.2.1 further discusses the design specification details taken in the designer tool to arrive at the final design.

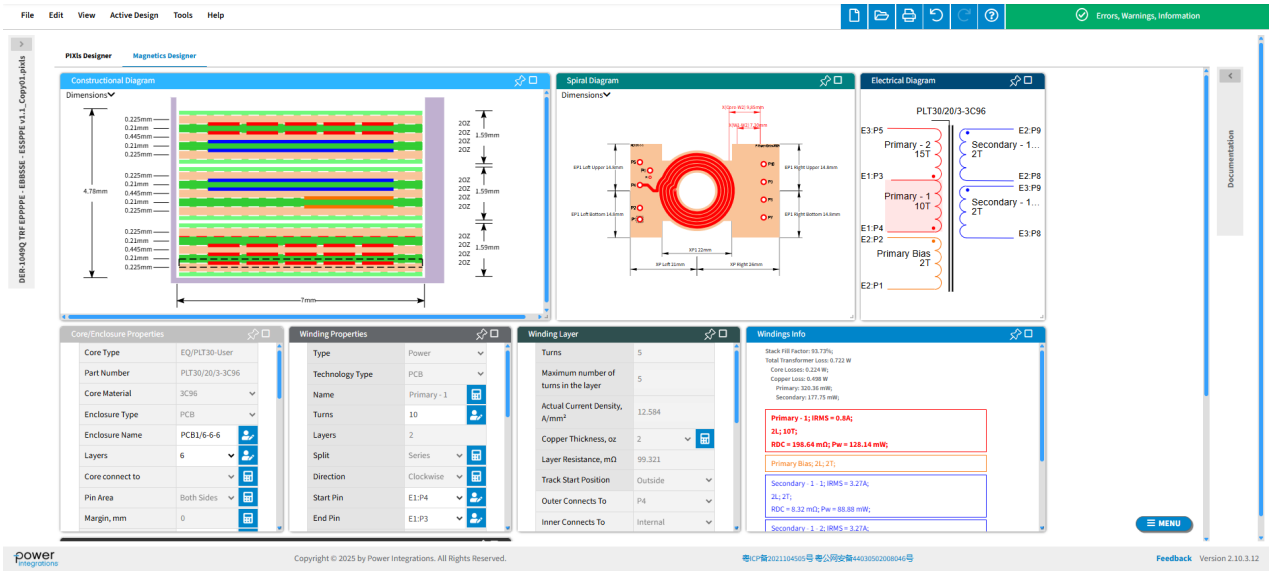
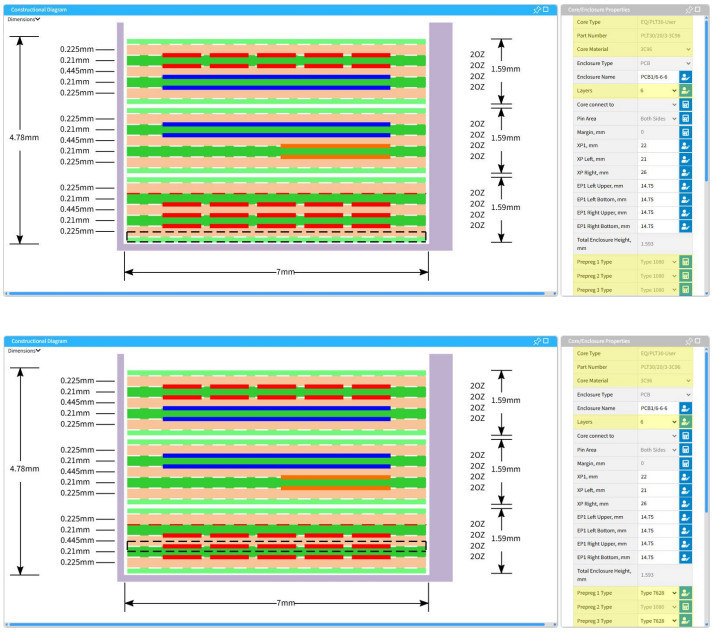
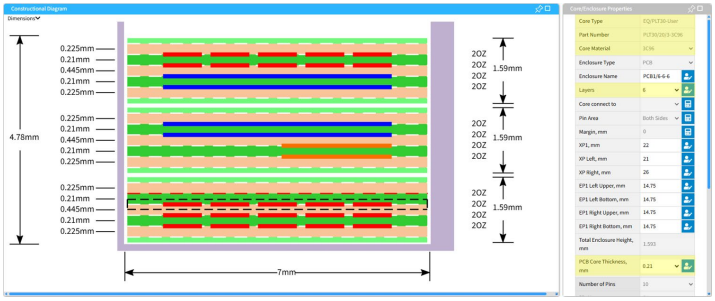
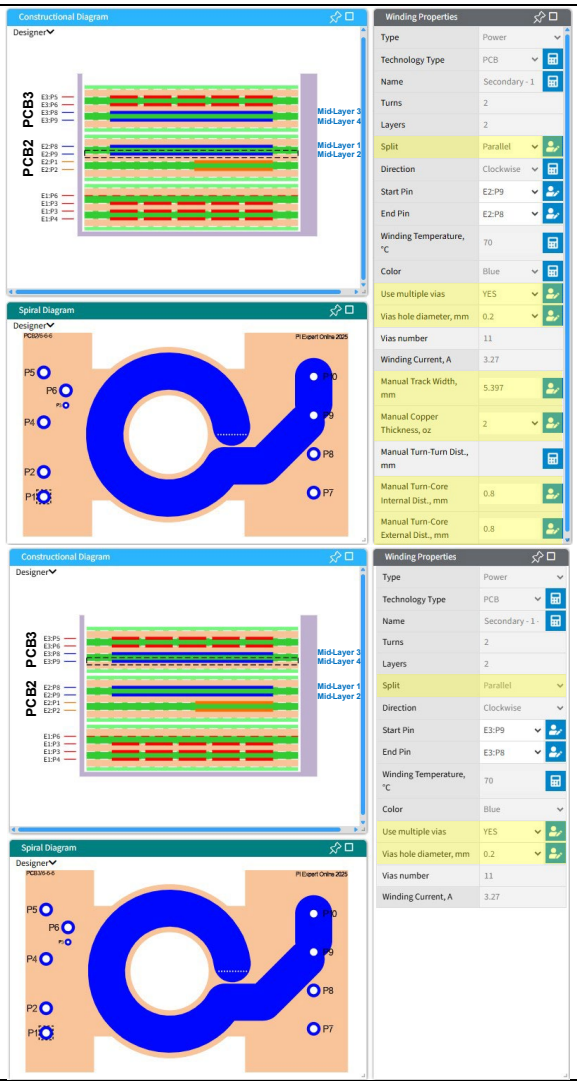
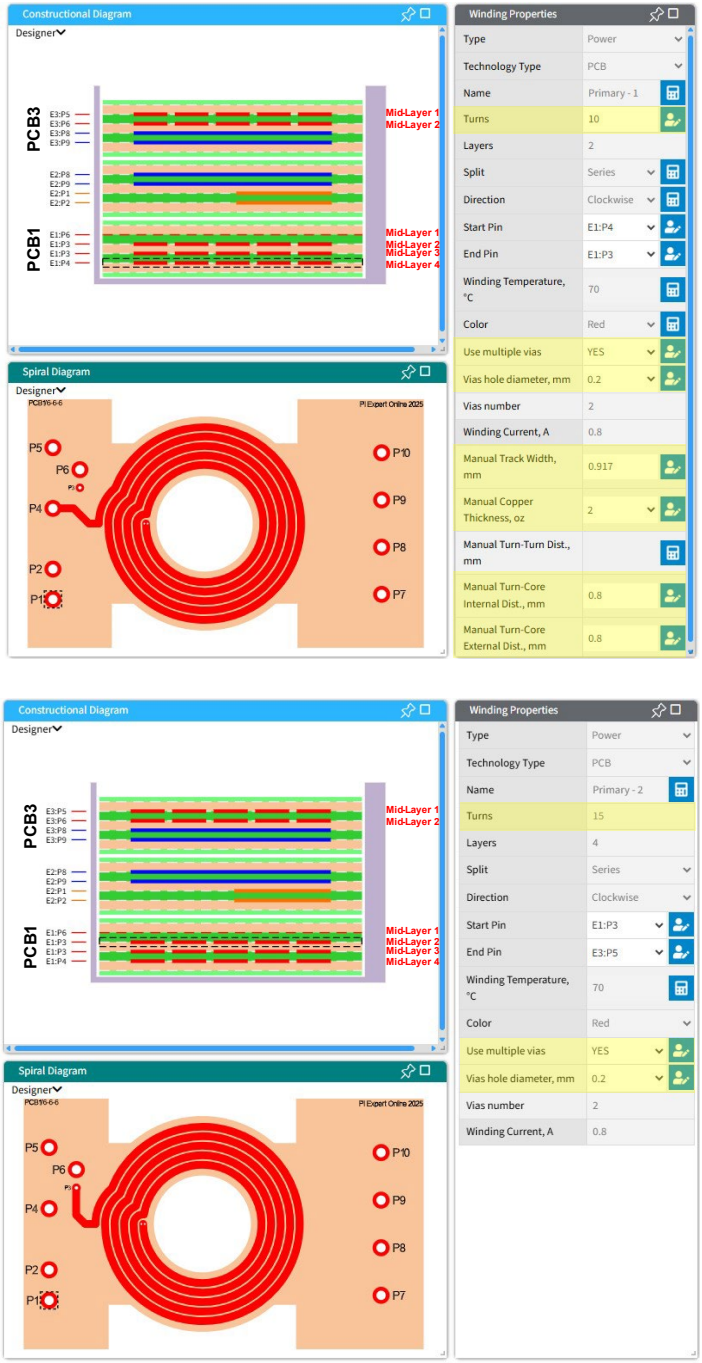


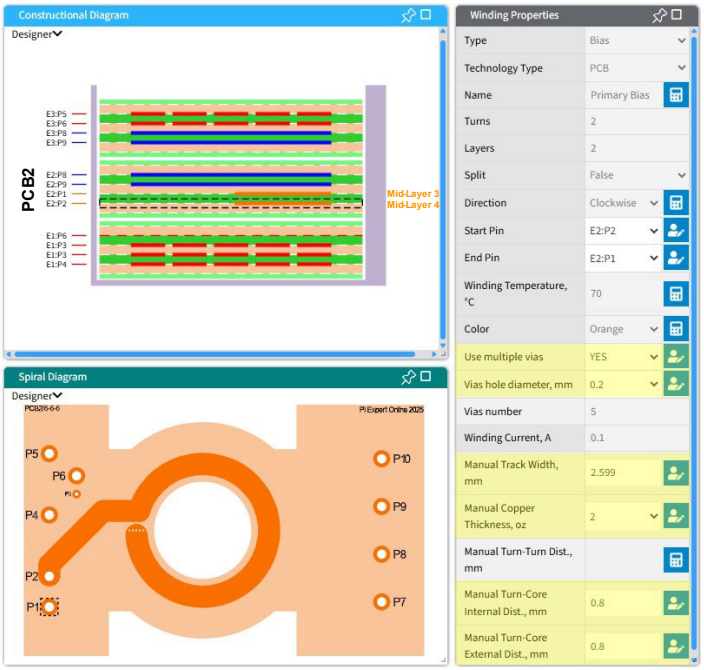
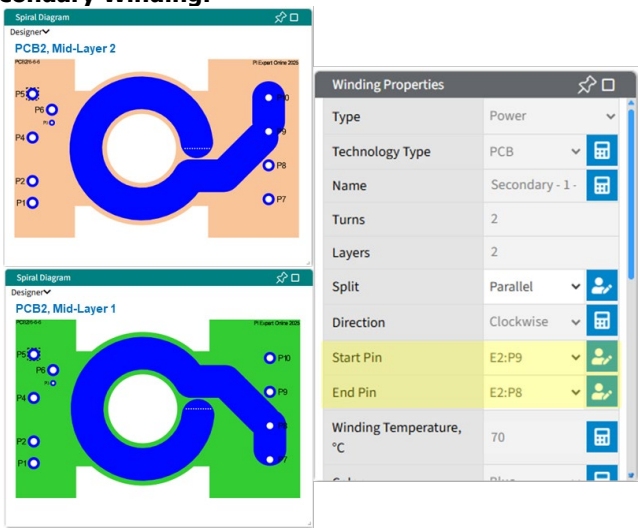
Figure 12 – PI Expert Online Magnetics Designer for Planar Transformer.

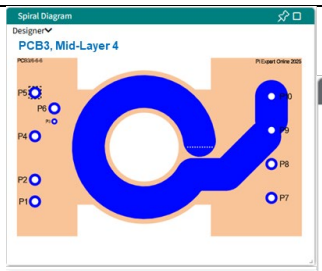
8.2.1 Design Process and Details

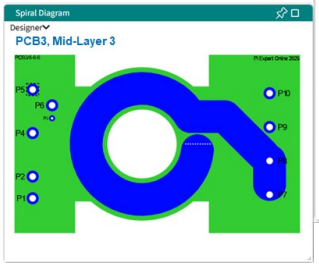
1. PCB Insulation Layer Specifications		The planar design was restricted to using 6-layer boards, as well as exclusively using internal layers for the windings. With this restriction, and maximizing fit factor, three 6-layer boards are used. To ensure sufficient production yield, the board insulation layer thicknesses were adjusted to the following: • Outer pre-preg layers: Type 1080+1080+1080 = 0.225 mm. • Middle pre-preg layer: Type 7628+1080+7628 = 0.445 mm. • PCB core layers: 0.21 mm.

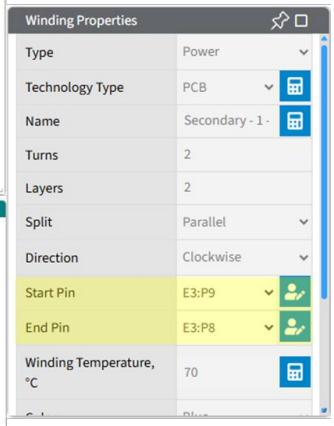
		These properties can be modified through the *Core/Enclosure Properties* window. The same board insulation layer thicknesses were applied across all three boards to allow for board panelization. Note: To ensure sufficient production yield, margins were implemented by using a custom EQ/PLT30 core with increased dimensions in the design, specified from the PIXls spreadsheet. Alternatively, margins can be implemented by specifying it in the *Core/Enclosure Properties* window.
2. Secondary Winding Specifications		For the secondary winding, the following specifications were implemented. These properties can be modified through the *Winding Properties* window: • 2 oz. copper thickness, consistent with all other windings. • Turn-Core internal and external distances of 0.8 mm. Note: safety distance requirements may vary depending on application • Track width of 5.397 mm. • Multiple vias – for improved resistance • 0.2 mm. via hole diameter – fabrication limitation In addition, a parallel split configuration was implemented for improved effective resistance. The first winding split is located on PCB2's (middle) mid-layers 1 and 2, while the other winding split is located on PCB3's (top) mid-layers 3 and 4.

3. Primary Winding Specifications		For the primary winding, the following specifications were implemented. These properties can be modified through the *Winding Properties* window: • 2 oz. copper thickness, consistent with all other windings. • Turn-Core internal and external distances of 0.8 mm. Note: safety distance requirements may vary depending on application • Track width of 0.917 mm. – allows for 5 turns per layer • Multiple vias – for improved resistance • 0.2 mm. via hole diameter – fabrication limitation In addition, a series split configuration was implemented for flexibility in turns distribution across layers. • The first winding split, having 10 turns, is located on PCB1's (bottom) mid-layers 3 and 4. • The second winding split, having 15 turns, is separated into two sections. The first one, having 5 turns, is located on PCB1's (bottom) mid-layers 1 and 2. The other one, having 10 turns, is located on PCB3's (top) mid-layers 1 and 2. • PCB1's primary winding was intentionally split into two sections to have a consistent HDI design as with the other two boards – allowing for board panelization.

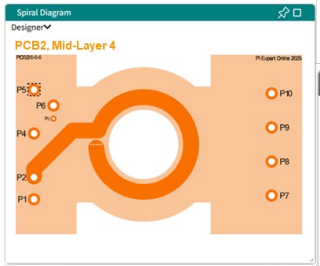
4. Primary Bias Winding Specifications		For the primary bias winding, the following specifications were implemented. These properties can be modified through the *Winding Properties* window: • 2 oz. copper thickness, consistent with all other windings. • Turn-Core internal and external distances of 0.8 mm. Note: safety distance requirements may vary depending on application • Track width of 2.599 mm. – to comply with safety requirements with respect to primary winding pins. Note: safety distance requirements may vary depending on application • Multiple vias – for improved resistance • 0.2 mm. via hole diameter – fabrication limitation The primary bias winding is in PCB2's (middle) mid-layers 3 and 4.
5. Winding Pin Terminations	**Secondary Winding:** 	In the Magnetics Designer tool, the winding pin terminations can be modified through the *Winding Properties* window. For both secondary winding splits (parallel), the windings were specified to start from pin P9, and end at pin P8.

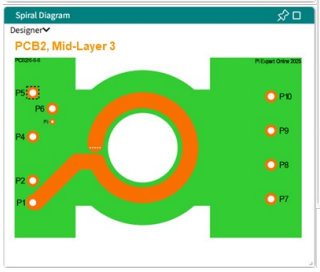


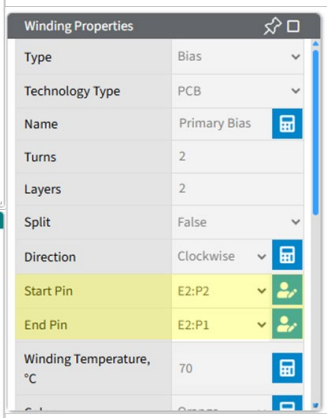




Primary Bias Winding:

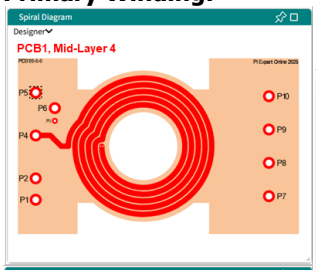


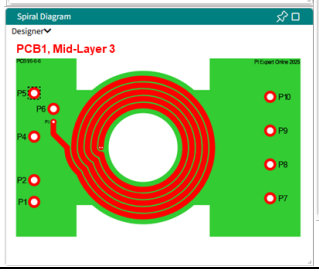


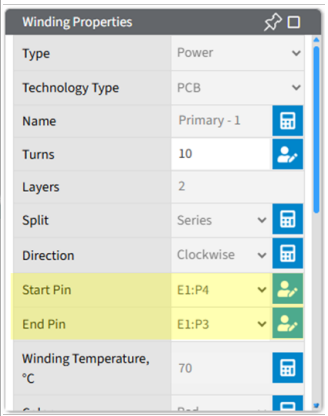


For the primary bias winding, the windings were specified to start from pin P2, and end at pin P1.

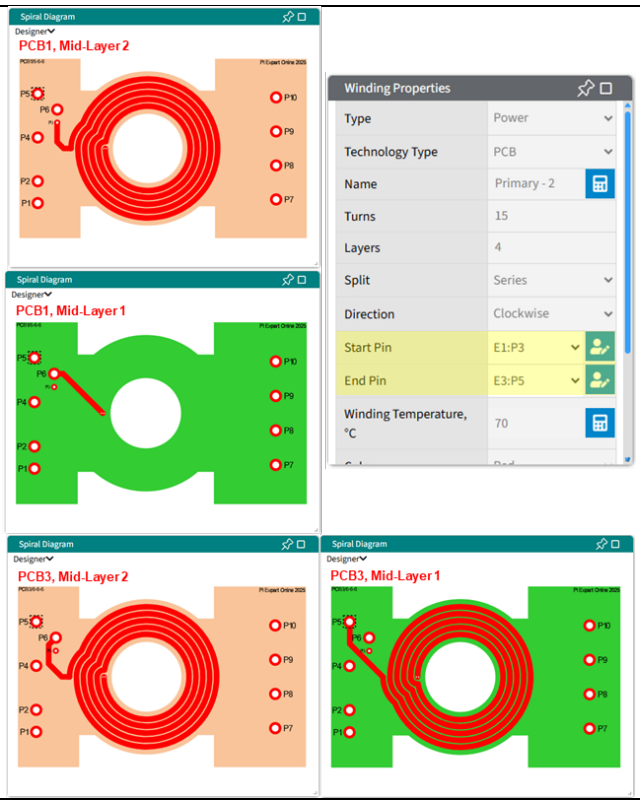
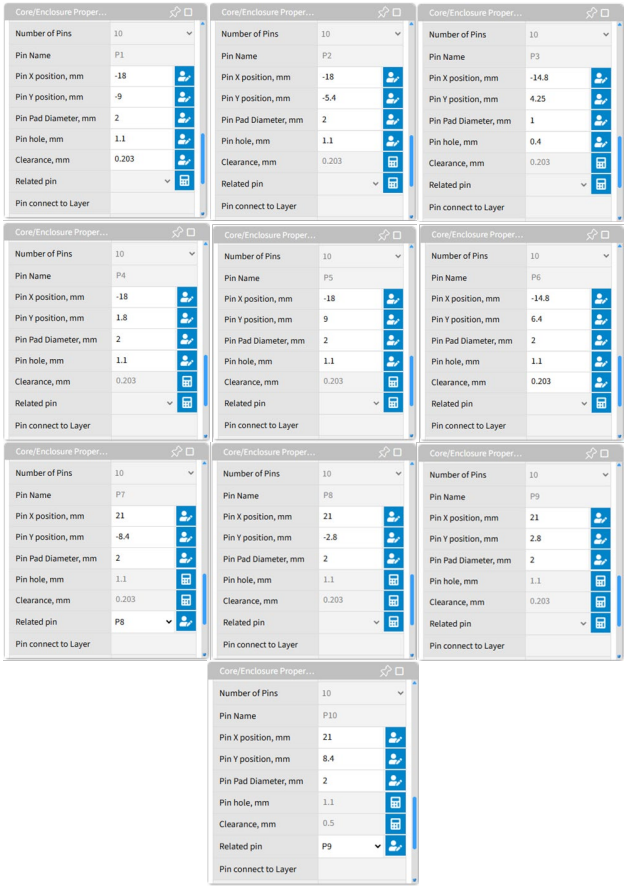
Primary Winding:

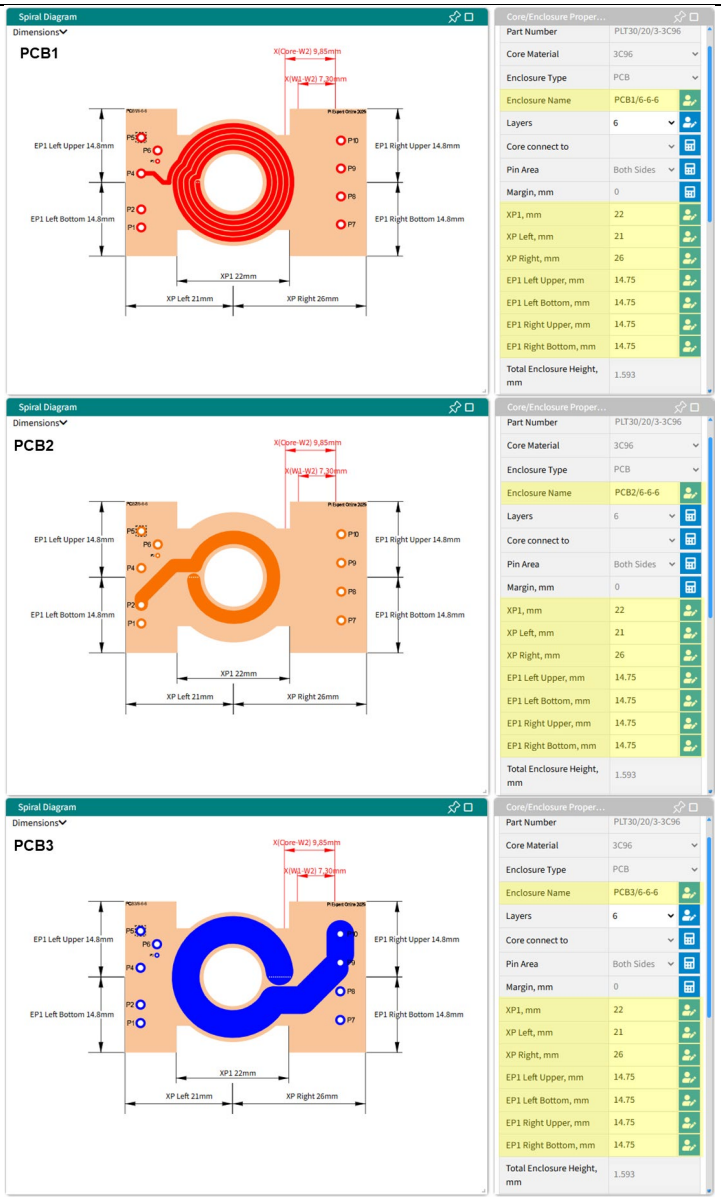


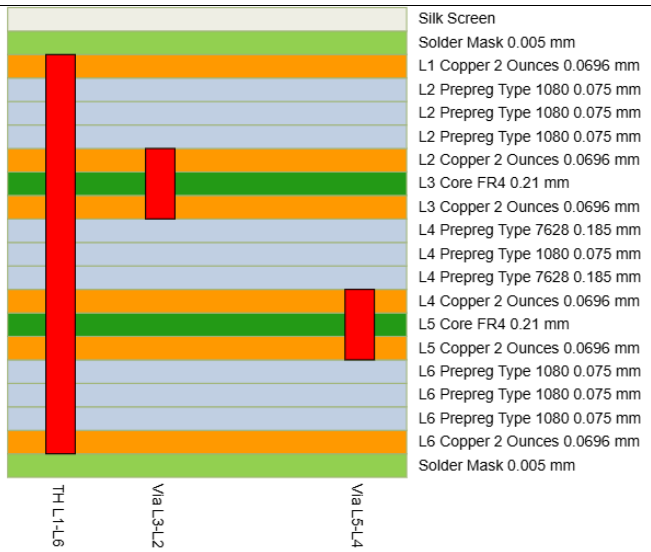




For the first primary winding split (located on PCB1 mid-layers 3 and 4), the windings were specified to start from pin P4, and end at pin P3.

		For the second primary winding split (located on PCB1 mid-layers 1 and 2, and on PCB3 mid-layers 1 and 2), the windings were specified to start from pin P3 (continuing from the first primary split), and end at pin P5. Since the second primary winding split is separated across two boards, an additional pin – pin P6 – was allocated for connection. In effect, the second primary winding split starts in PCB1 from pin P3 and terminates at pin P6. The winding then continues in PCB3 from pin P6 and ends at pin P5.
6. Pin Properties and Positions		The pin properties and positions can be modified through the *Core/Enclosure Properties* window. 10 pins in total are used as terminations for the transformer windings, with the following specifications: For pin P3, • Pin Pad Diameter: 1 mm. • Pin Hole: 0.4 mm. For all other pins, • Pin Pad Diameter: 2 mm. • Pin Hole: 1.1 mm. Pin positions are defined with respect to the x- and y-axes, with the core's center leg referred to as the origin, as seen from the *Spiral Diagram* window. Note: When working on this section of the design, it is recommended to first define the PCB dimensions, particularly XP1, prior to defining the pin properties and positions.

7. PCB Dimensions		Across all three boards, the following PCB dimension specifications were implemented. These properties can be modified through the *Core/Enclosure Properties* window: • XP1: 22 mm. • XP Left: 21 mm. • XP Right: 26 mm. • EP1 Left Upper, Left Bottom, Right: 14.75 mm.

8. Foundry Stack-up		All boards (PCB1, PCB2, and PCB3) can be verified to have a consistent stack-up and HDI design with each other – allowing for panelization in fabrication. This can be viewed through the Foundry view of the *Constructional Diagram* window.

9 Partial Discharge (PD) and Hi-Pot Testing for Transformer

9.1 Partial Discharge (PD)

Partial discharge (PD) is defined by IEC 60270 as localized electrical discharges that partially bridge the insulation between conductors. It appears as small electrical discharges lasting less than 1 µs. Successful PD testing ensures that high-quality materials are used in the design, thus reducing the risk of failure over time.

Figure 13 and Figure 14 shows the test profiles used to evaluate the planar transformer of DER-1049Q. The test profile is based on IEC 60664-1:2020.

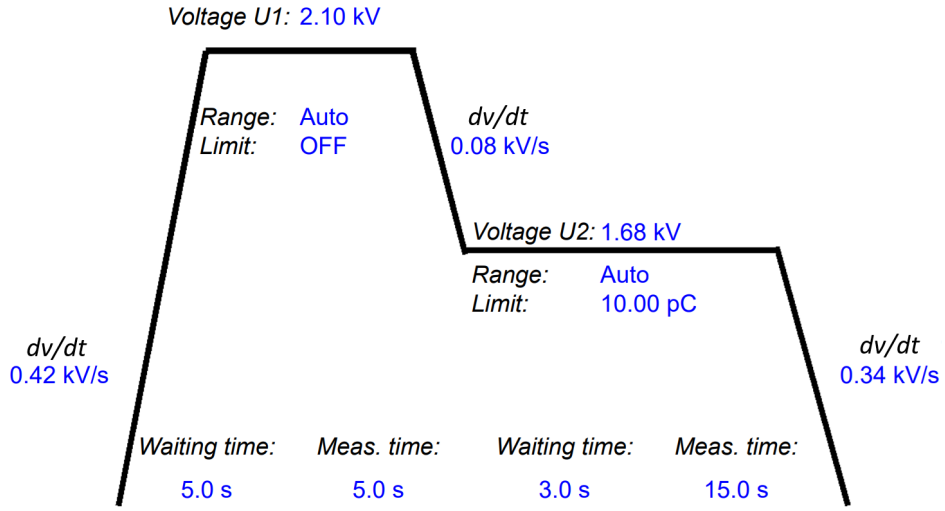


Figure 13 – Basic Insulation PD Test Profile of DER-1049Q.

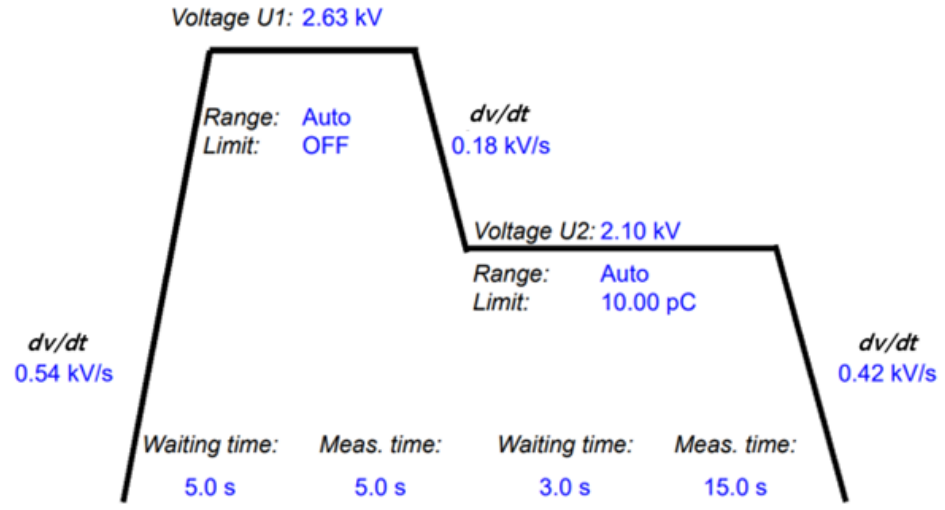


Figure 14 - Reinforced Insulation PD Test Profile of DER-1049Q.

The partial discharge for the basic insulation[15] of the planar transformer was measured between nodes 1 to 5 at 25 °C ambient. Nodes 1-2 and nodes 4-5 are shorted. Refer to section 7.1 for the transformer electrical diagram.

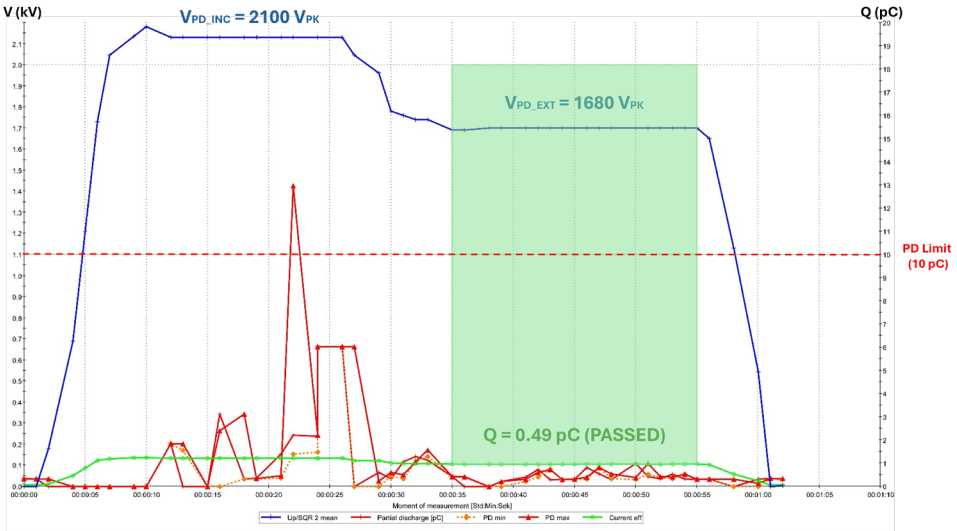


Figure 15 – Basic Insulation PD Test Result of DER-1049Q.

The partial discharge for the reinforced insulation[16] of the planar transformer was measured between nodes 1 to 9 at 25 °C ambient. Nodes 1-5 and nodes 8-9 are shorted. Refer to section 7.1 for the transformer electrical diagram.

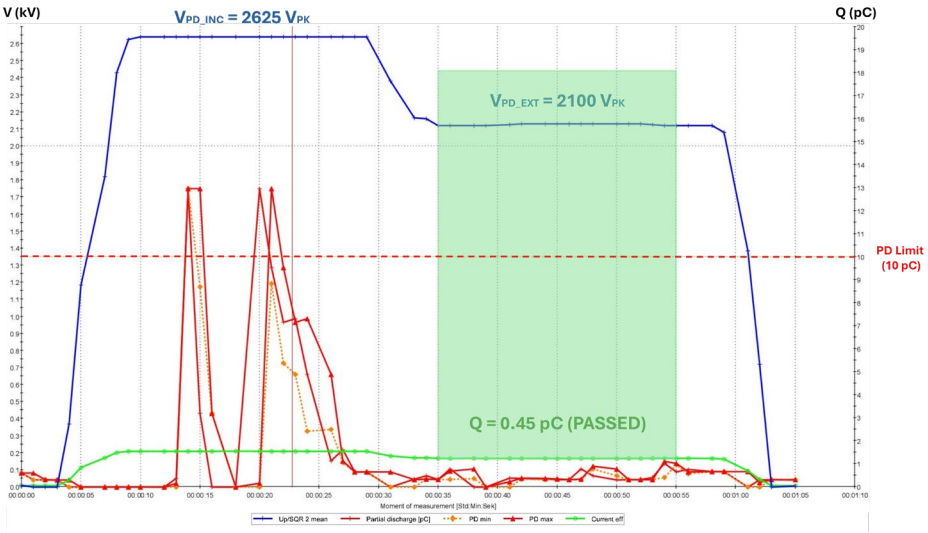


Figure 16 – Reinforced Insulation PD Test Result of DER-1049Q.

[15] Conformal coating is applied to the transformer board before the transformer is assembled to meet the PD requirements. See Section 7.4.
[16] Conformal coating is applied to the transformer board before the transformer is assembled to meet the PD requirements. See Section 7.4.

9.2 Hi-Pot Testing

Hi-Pot testing measures the dielectric breakdown of the primary-to-secondary isolation used in the transformer. This test is done to assess the ability of the insulation to withstand steady state working voltage stresses. Hi-pot testing also checks for the existence of damage in the isolation barrier.

Figure 17 shows the test profile used to evaluate the planar transformer of DER-1049Q.

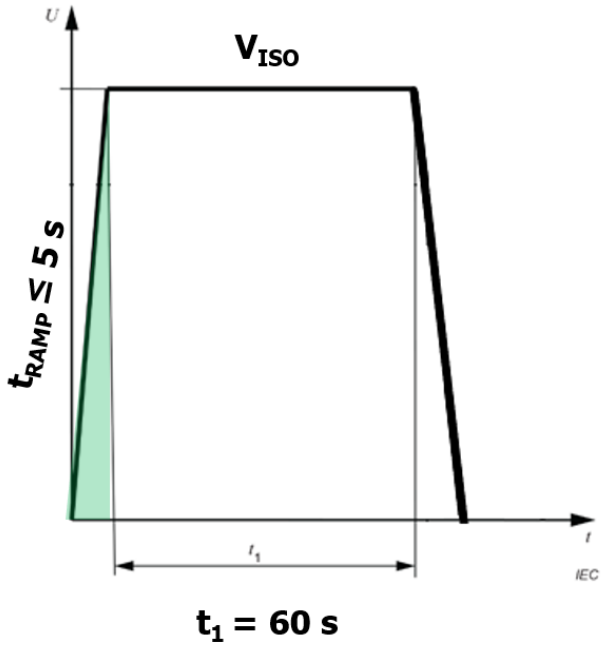


Figure 17 – Hi-Pot Test Profile of DER-1049Q.

The unit under test was tested with an isolation voltage of 4000 V_{RMS} to 6400 V_{RMS} with a 5-second ramp-up and 60-second dwell time. The isolation test was done between nodes 1 to 6 at 25 °C ambient, with nodes 1-4 and 5-6 shorted. Refer to section 7.1 for the transformer electrical diagram.

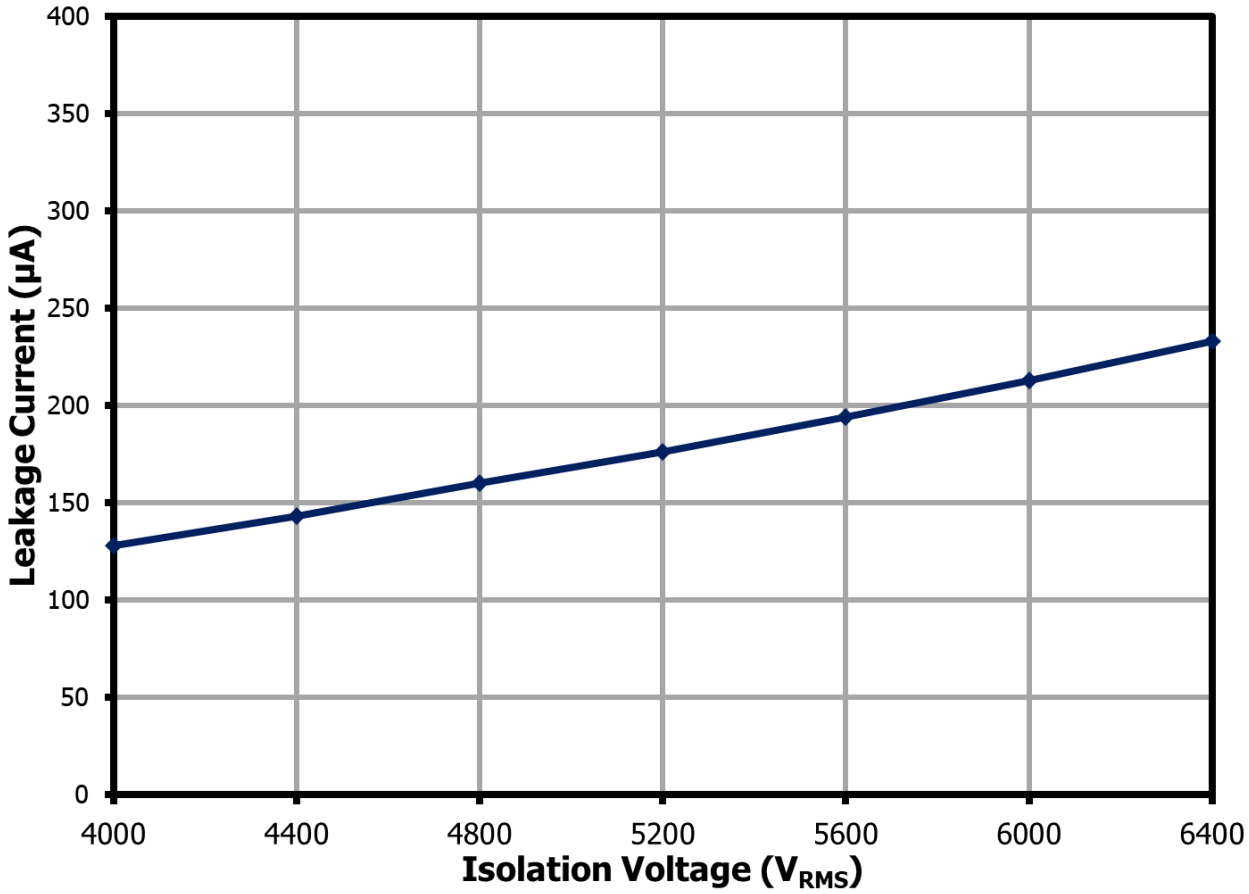


Figure 18 – Isolation Voltage vs. Leakage Current (25 °C Ambient).

Note: The leakage current across the isolation barrier above is due to the primary to secondary coupling capacitance. When the high voltage 60 Hz AC test voltage is applied, current flows through this capacitance (~54 pF). Under DC voltage conditions, this leakage is not present (<3 uA measured).

10 Performance data

Note: 1. Measurements were taken with the unit-under-test positioned inside a thermal chamber.

2. The DER-1049Q board was placed in a box inside the thermal chamber to eliminate the effects of any airflow.

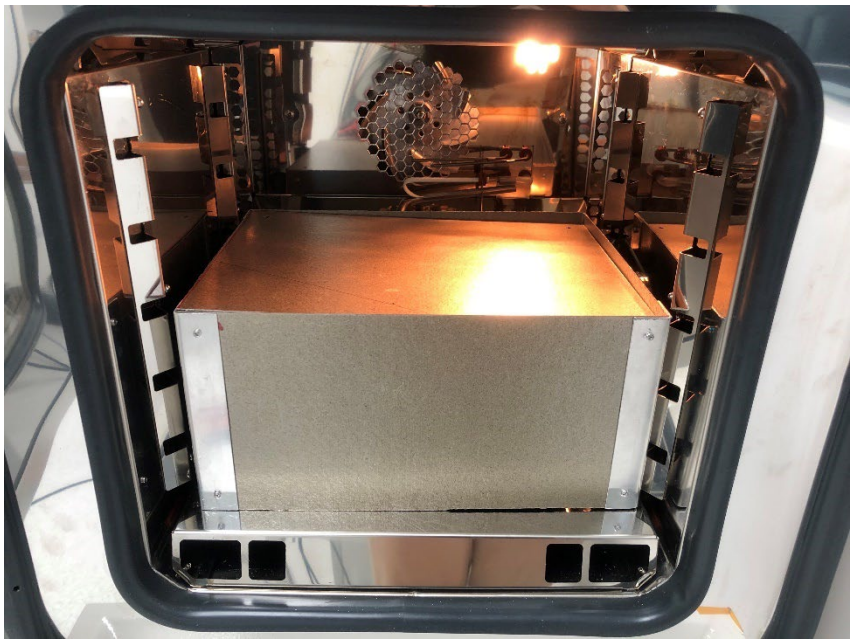


Figure 19 – Unit under test placed inside a box to eliminate the effect of airflow.

3. The unit was soaked for 5 minutes at full load at the start of each test sequence. For each loading condition, the DER-1049Q test board was allowed to stabilize for 1 minute before measurements were taken.

4. List of Equipment Used for Testing

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	HP20 757 152	2 kV/750 mA/1.5 kW DC PSU	Iseg
Power Supply	MR100020	1000 V/20 A/5 kW Programmable DC PSU	BK Precision
Power Supply	SL1000-1.5	1000 V/1.5 A/1.5 kW Programmable DC PSU	Magna Power
Electronic Load	PEL-2020A	80 V/20 A/100 W DC Electronic Load	GW Instek
Electronic Load	63303A	80 V/60 A/300 W DC Electronic Load	Chroma
Electronic Load	63113A	300 V/20 A/300 W DC Electronic Load	Chroma
Power Meter	66205	600 V/30 A Digital Power Meter	Chroma
Power Meter	WT310E	600 V/20 A Digital Power Meter	Yokogawa
High-Voltage Measurement	TT-SI 9010A	70 MHz 7000 V Differential Probe	Testec
High-Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low-Voltage Measurement	PHT 312	400 V Passive Probe Extended Temperature	PMK
Low-Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Current Measurement	701928	100 MHz 30 A_{rms} Current Probe	Yokogawa
Current Measurement	CWTUM/015/B	30 MHz 30 A_{peak} Rogowski Coil	CWT
Current Measurement	CWTUM/06/R	30 MHz 120 A_{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20-Channel Data Logger	Graphtec
Thermal Image	TiX580	1000°C Thermal Imaging Camera	Fluke
Thermal Chamber	SH-242	Temperature & Humidity Chamber	Espec
Thermal Chamber	TUJR	Temperature & Humidity Chamber	SPX
Oscilloscope	DLM5058	2.5GS/s 500 MHz Mixed Signal	Yokogawa
Oscilloscope	DLM5054	2.5GS/s 500 MHz Mixed Signal	Yokogawa

Table 8 – List of Equipment Used for Testing.

10.1 No-Load Input Power

Figure 20 shows the test circuit used for no-load input power measurement. The voltmeter was placed before the ammeter; this was done to prevent the voltmeter bias current from affecting the input current measurement. A Chroma Digital Power Meter 66205 was used to measure both the current and voltage.

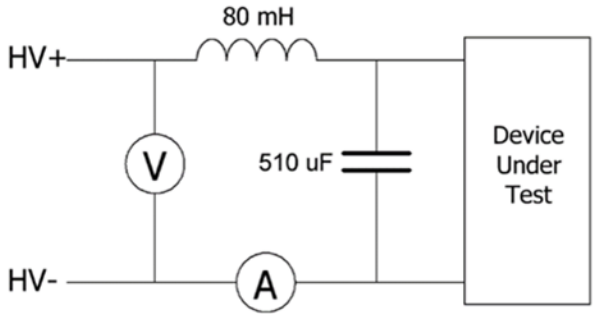


Figure 20 – No-Load Input Power Measurement Circuit Configuration.

The unit was allowed to stabilize for ten minutes for each test before measurements were started. The leakage current through the DC-Link capacitor was also measured before testing and was subtracted from the measured no-load input current. The average voltage across the inductor was assumed to be negligible due to the inductor's very low DCR (40 mΩ) and low input current. AC losses in the inductor were also assumed to be negligible since the input current was DC.

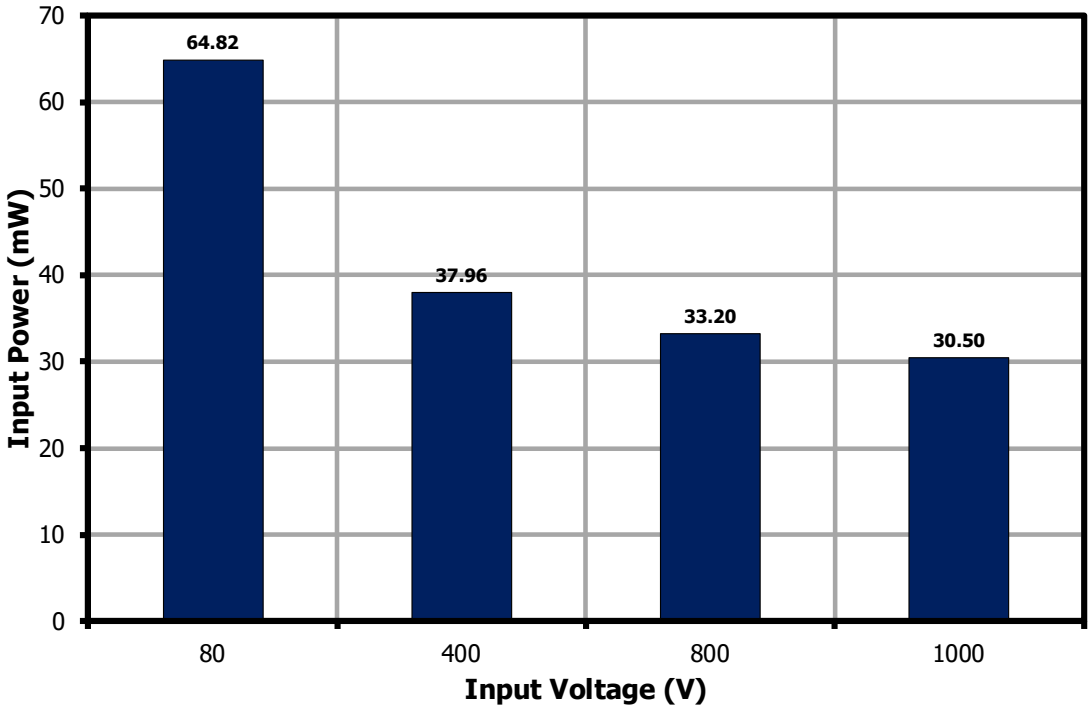


Figure 21 – No-Load Input Power vs. Input Voltage (25 ºC Ambient).

10.2 Efficiency

10.2.1 Efficiency Across Line

Efficiency across line describes how input voltage affects the unit's overall efficiency. The points in the graph were taken at 100% load conditions.

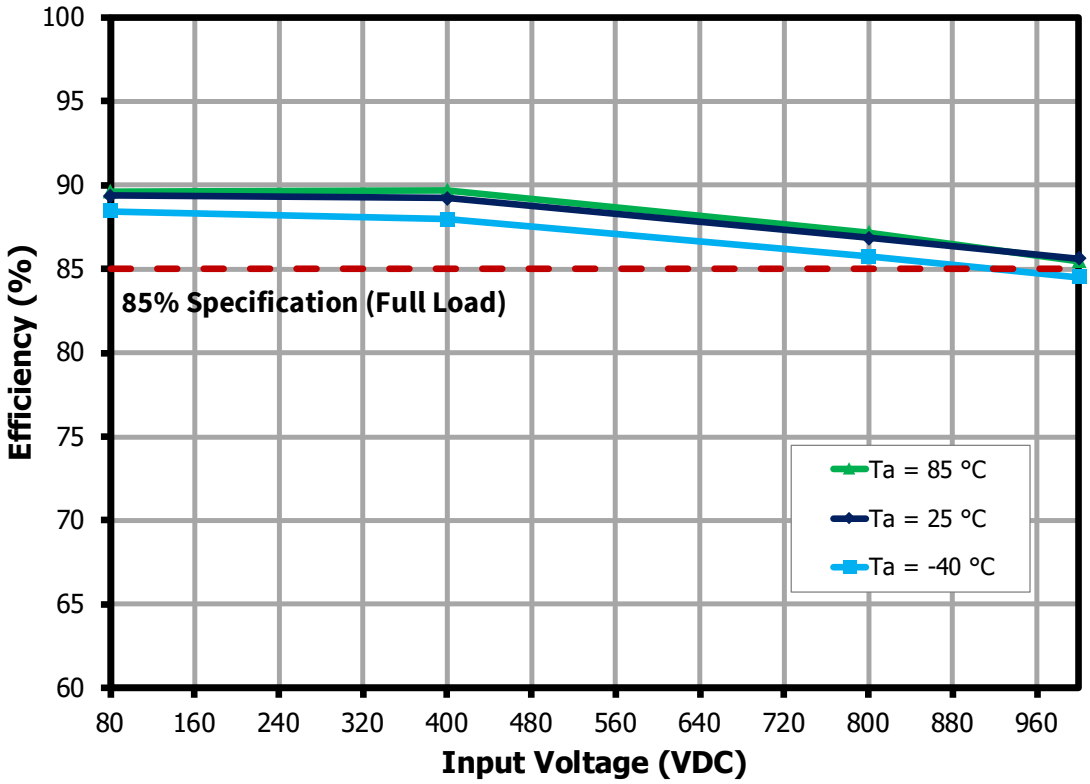


Figure 22 – Full Load Efficiency vs. Input Line Voltage (80 VDC to 1000 VDC).[17]

[17] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

10.2.2 Efficiency Across Load

Efficiency across load describes how output loading affects the overall efficiency of the power supply.

10.2.2.1 Efficiency Across Load at 85 °C Ambient

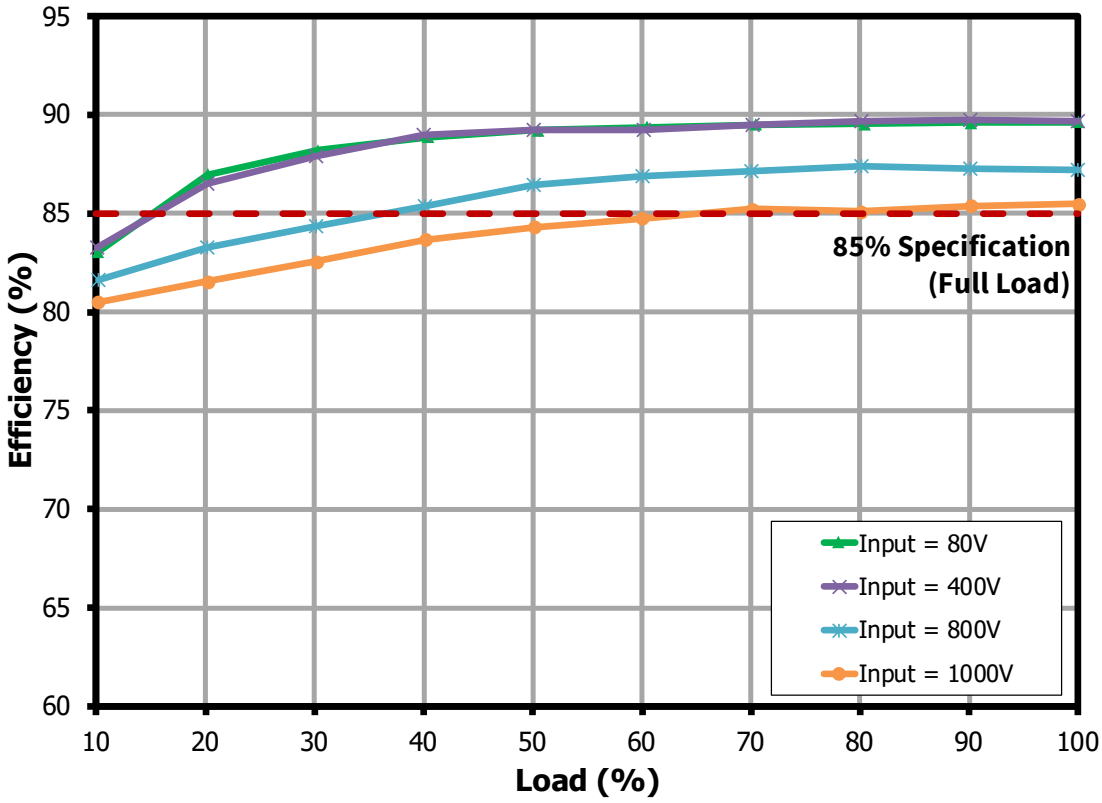


Figure 23 – Efficiency vs. Load at Different Input Voltages (85 ºC Ambient).[18]

[18] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

10.2.2.2 Efficiency Across Load at 25 ºC Ambient

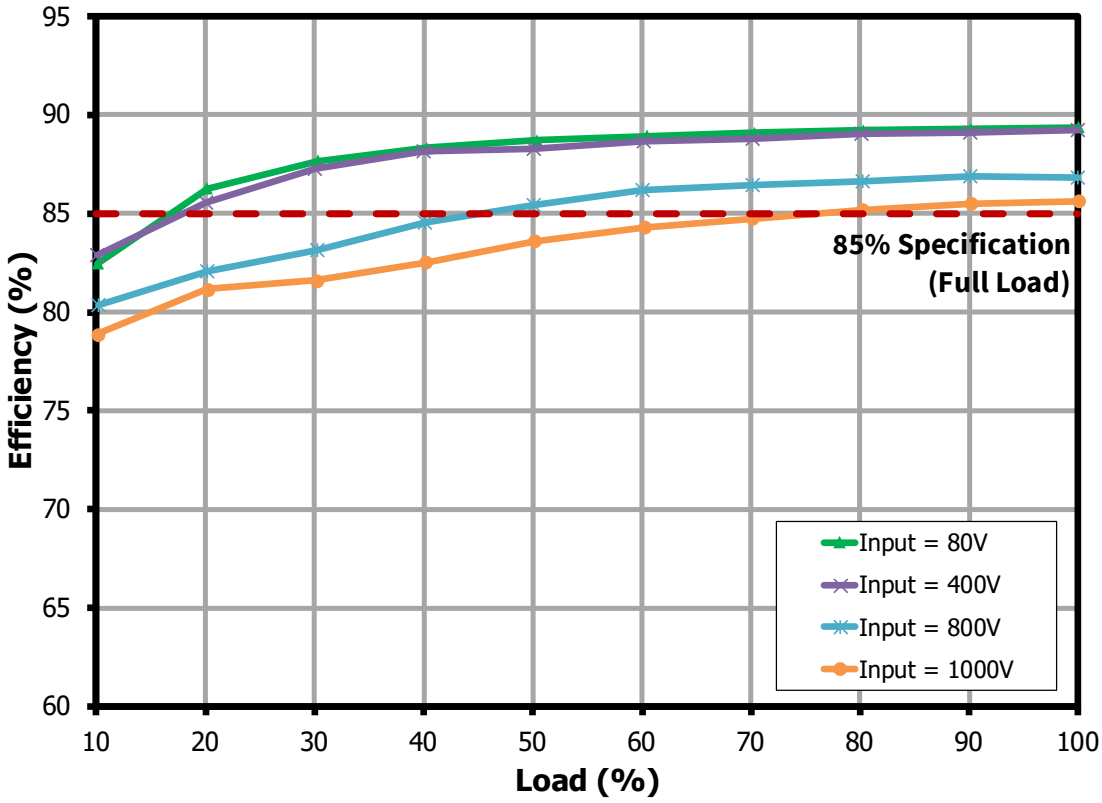


Figure 24 – Efficiency vs. Load at Different Input Voltages (25 ºC Ambient).[19]

[19] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

10.2.2.3 Efficiency Across Load at -40 ºC Ambient

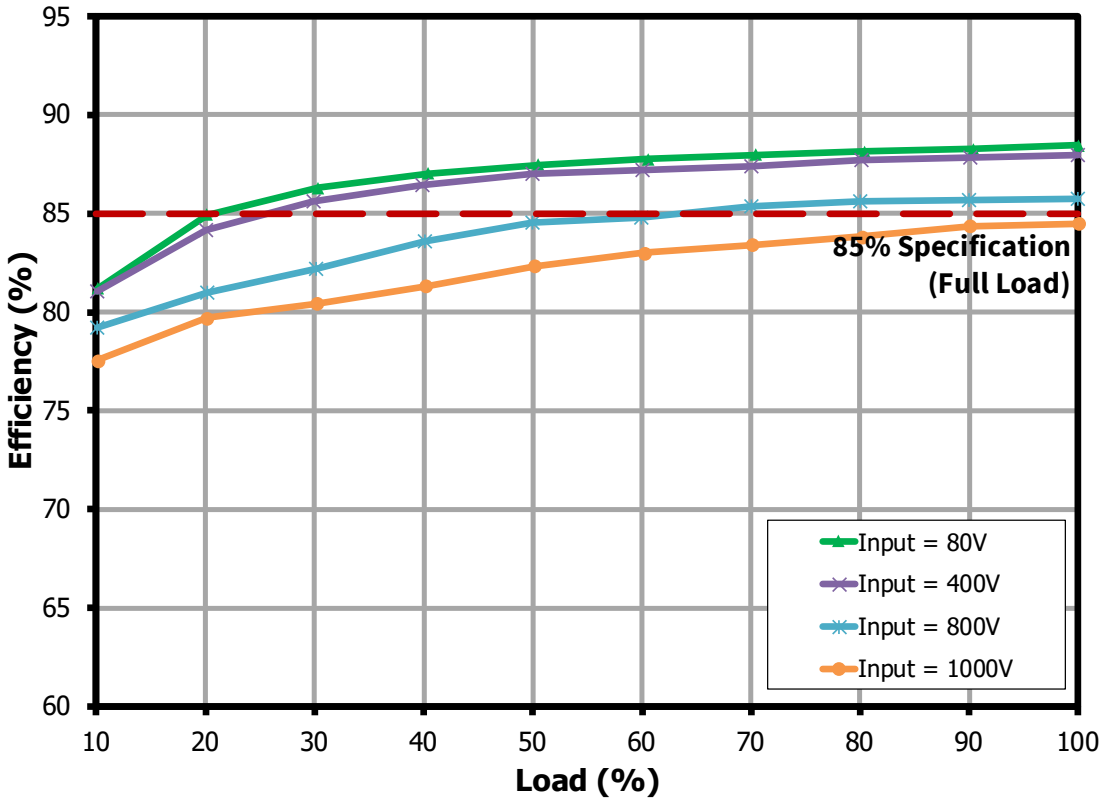


Figure 25 – Efficiency vs. Load at Different Input Voltages (-40 ºC Ambient).[20]

[20] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

10.3 Line and Load Regulation

10.3.1 Load Regulation

Load regulation describes how a change in load affects output voltage.

10.3.1.1 Load Regulation at 85 ºC Ambient

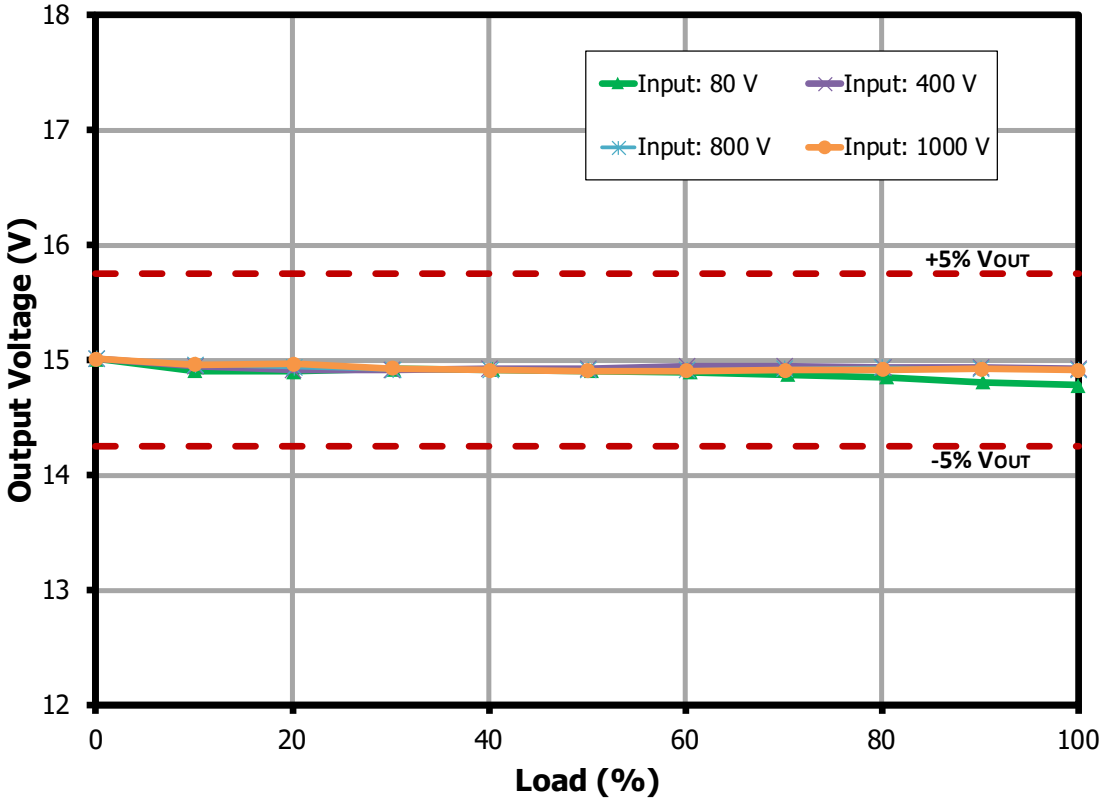


Figure 26 – Output Regulation vs. Load at Different Input Voltages (85 ºC Ambient).[21]

[21] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

10.3.1.2 Load Regulation at 25 ºC Ambient

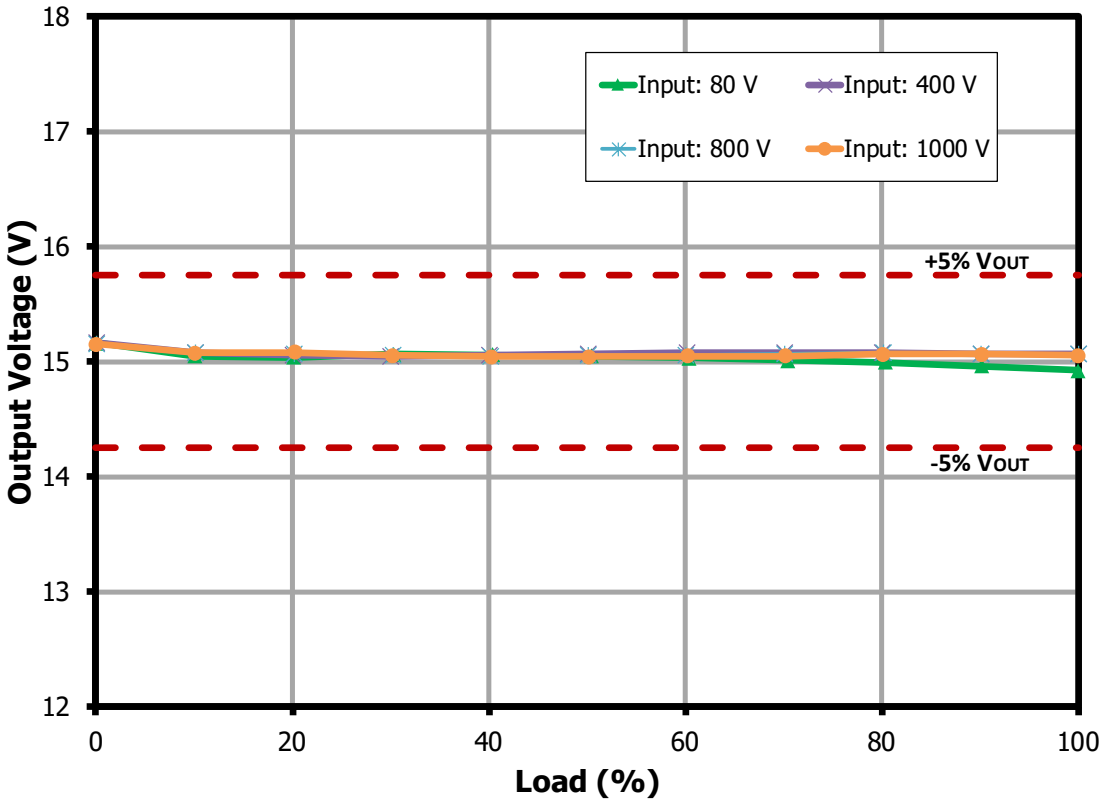


Figure 27 – Output Regulation vs. Load at Different Input Voltages (25 ºC Ambient).[22]

[22] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

10.3.1.3 Load Regulation at -40 ºC Ambient

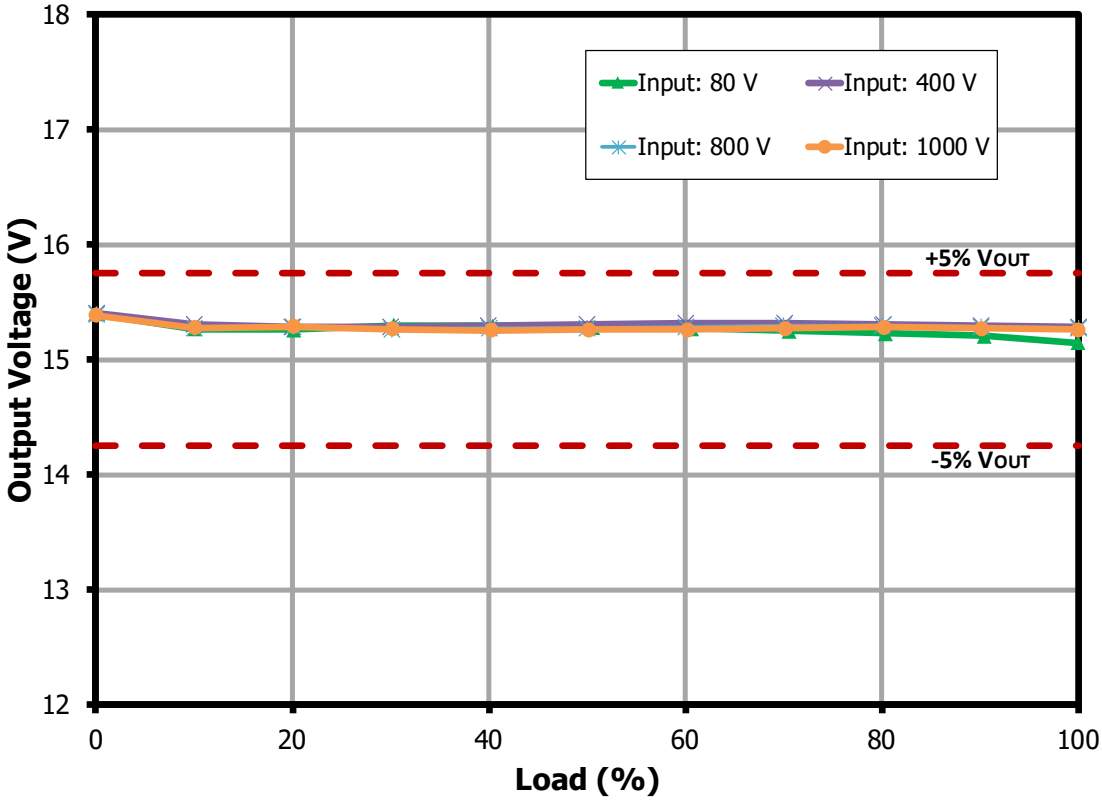


Figure 28 – Output Regulation vs. Load at Different Input Voltages (-40 ºC Ambient).[23]

[23] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

10.3.2 Line Regulation

Line regulation describes how the change in input voltage affects the output voltage.

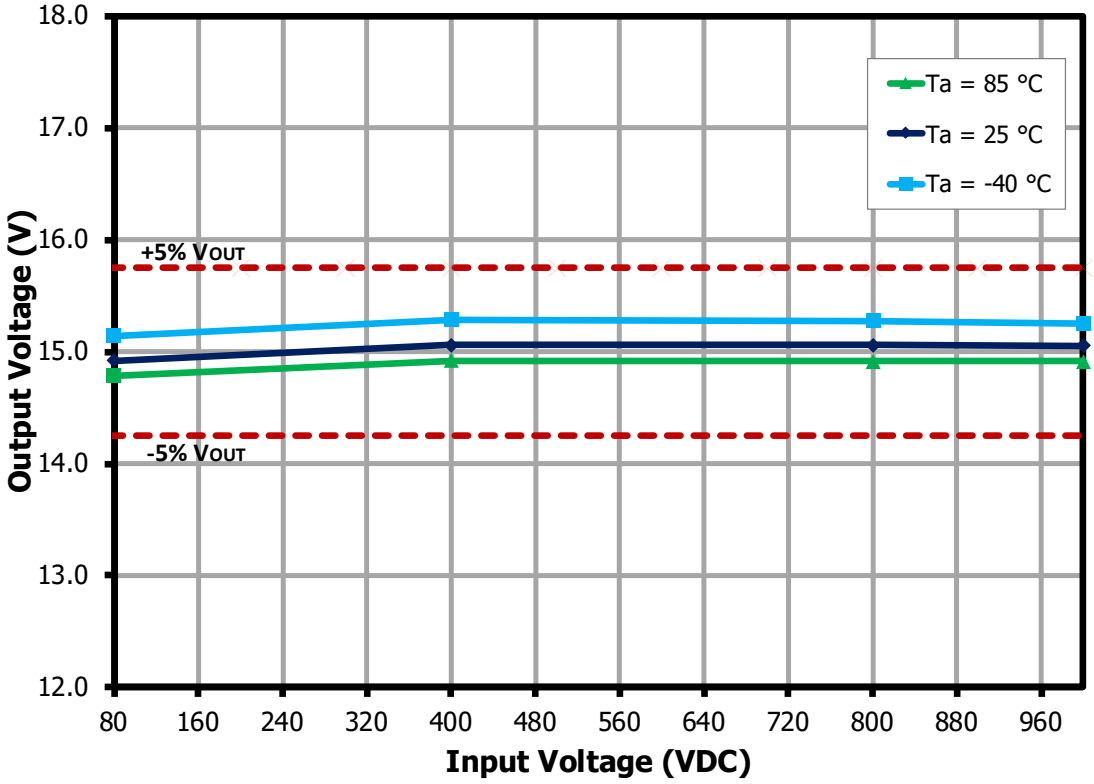


Figure 29 – Output Voltage vs Input Voltage at Full Load (80 VDC to 1000 VDC).[24]

[24] 100% load was defined at 1.8 A output current for 80 VDC to 1000 VDC.

11 Thermal Performance

11.1 Thermal Data at 85 ºC Ambient

11.1.1 27 W Continuous Output Power

The unit was placed inside a thermal chamber and allowed to stabilize for 1 hour. Figure 19 shows the setup for thermal measurements.

Critical Components	Temperature (°C)			
	80 V	400 V	800 V	1000 V
InnoSwitch3-AQ	104.7	102.5	117.7	129.0
Common Mode Choke Core	95.3	94.8	95.2	96.7
Common Mode Choke Winding	96.7	96.9	98.8	101.1
Primary Snubber (R3)	105.3	104.1	108.1	111.4
Primary Snubber (R15)	102.7	102.3	105.3	108.2
Transformer Winding	98.8	99.8	104.5	107.0
Transformer Core	99.1	100.8	106.8	109.9
SR MOSFET (Q1)	94.5	95.5	97.9	97.2
SR MOSFET (Q2)	95.4	96.4	98.4	97.1
Secondary Snubber Resistor (R18)	93.0	94.9	98.6	98.1
Output Capacitor (C19)	91.6	92.2	92.8	90.6

Table 9 – Thermal Data at 85 ºC at Different Input Voltages.

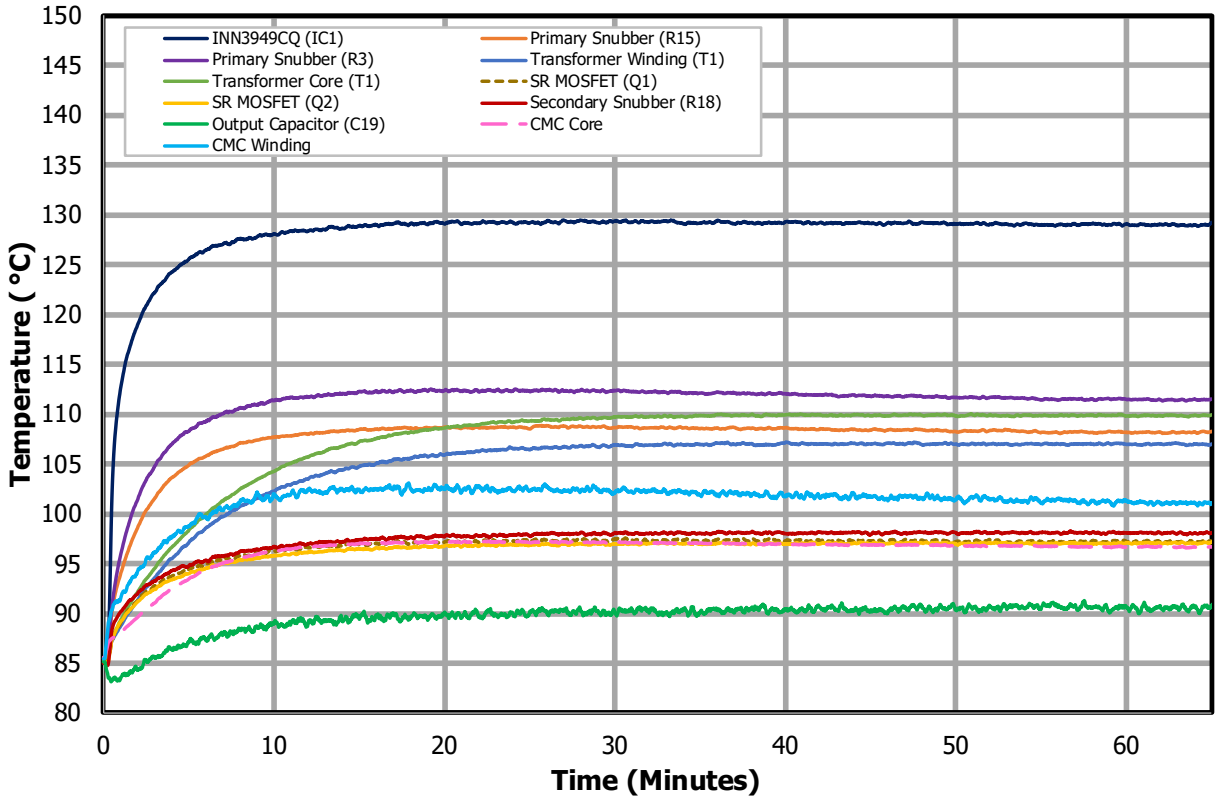


Figure 30 – Component Temperatures at 85 ºC Ambient, 1000 V Input, 1.8 A Load.

11.1.2 Operating Time of Peak Output Power

This test determines the maximum operating time of the peak output power at 85 °C ambient before overtemperature protection (OTP) is triggered. The unit was placed inside a thermal chamber and stabilized for 1 hour at 1000 VDC with no load before applying peak output current. Data was collected until overtemperature protection (OTP) was triggered.

11.1.2.1 35 W Peak Output Power

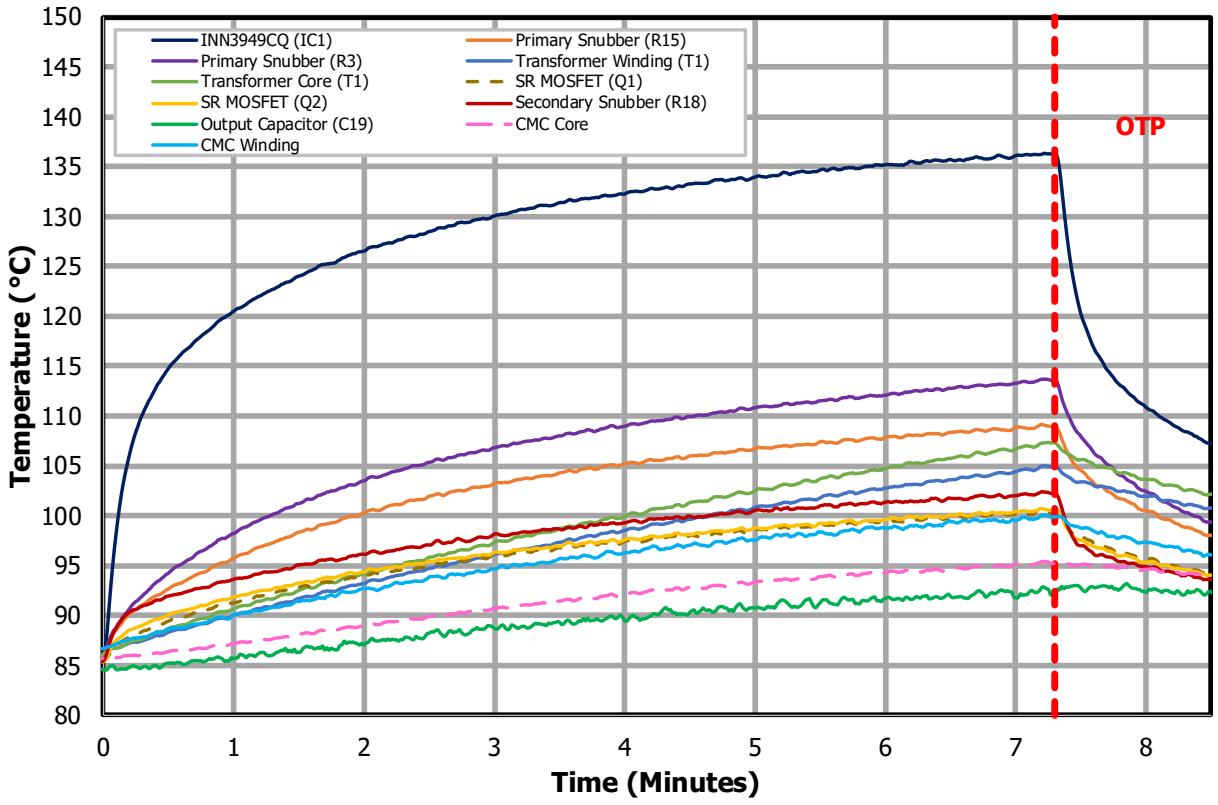


Figure 31 – Component Temperatures at 85 ºC Ambient, 1000 V Input, 2.333 A Load.

11.2 Thermal Image Data at 25 ºC Ambient

11.2.1 27 W Continuous Output Power

The following thermal scans were captured using a Fluke thermal imager after soaking the power supply in an enclosure to minimize the effect of air flow for 1 hour.

Critical Components	Temperature (°C)			
	80 V	400 V	800 V	1000 V
InnoSwitch3-AQ	47.6	48.4	65.7	78.9
Common Mode Choke	46.2	45.7	45.6	47.7
Primary Snubber (R3)	49.7	49.1	50.3	53.2
Primary Snubber (R15)	50.5	50	51.1	53.4
Primary Snubber Diode	48.5	47.5	50.1	54.7
Transformer	46.6	62.3	52.8	56
SR MOSFET (Q1)	38.7	40.5	43	45
SR MOSFET (Q2)	39.5	41.2	43.7	45.6
Secondary Snubber Resistor	38.1	40.1	45.5	47.8
Output Capacitor (C19)	36.7	38	40.2	41.7

Table 10 – Thermal Data at 25 ºC at Different Input Voltages.

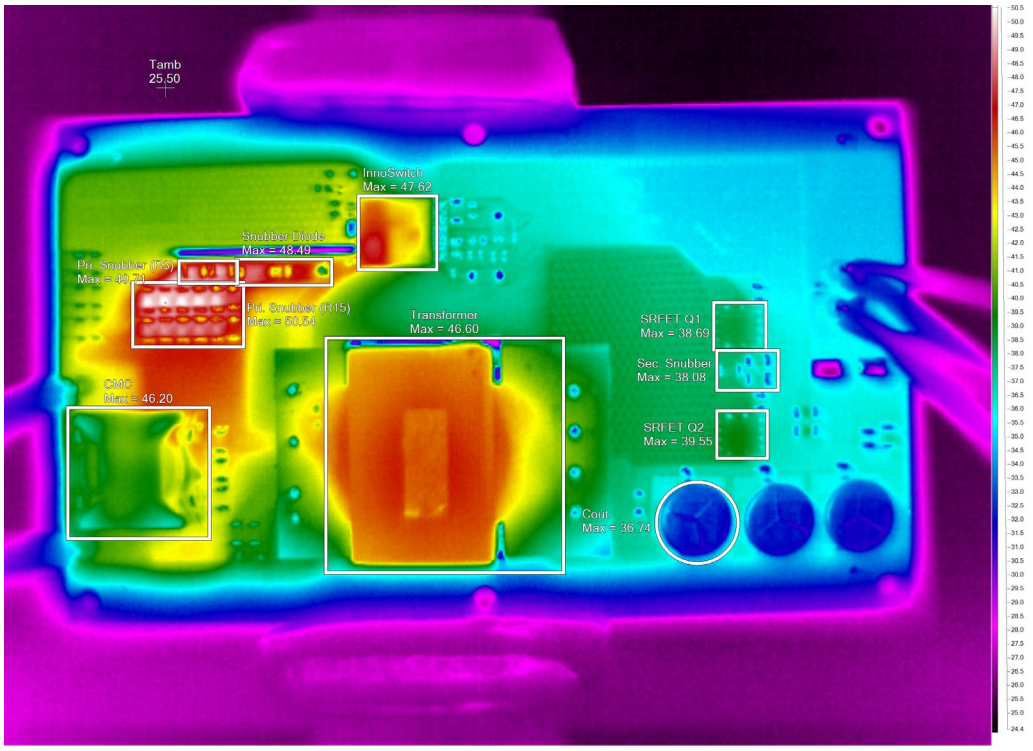


Figure 32 – Thermal Scan of the Top of the PCB at 80 V Input.

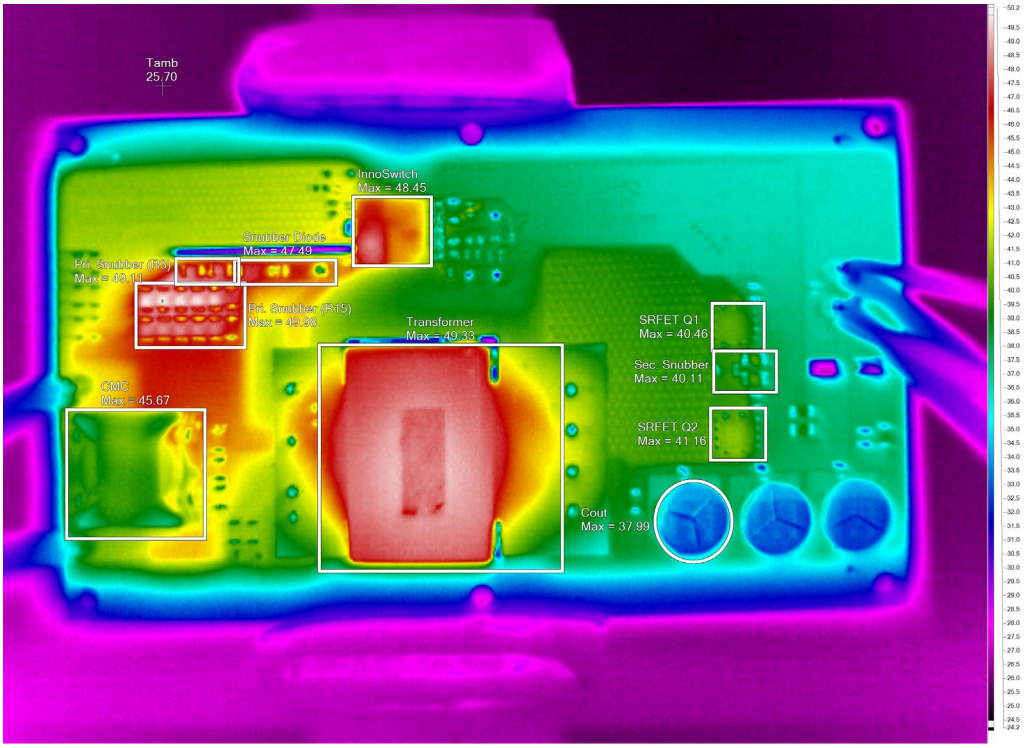


Figure 33 – Thermal Scan of the Top of the PCB at 400 V Input.

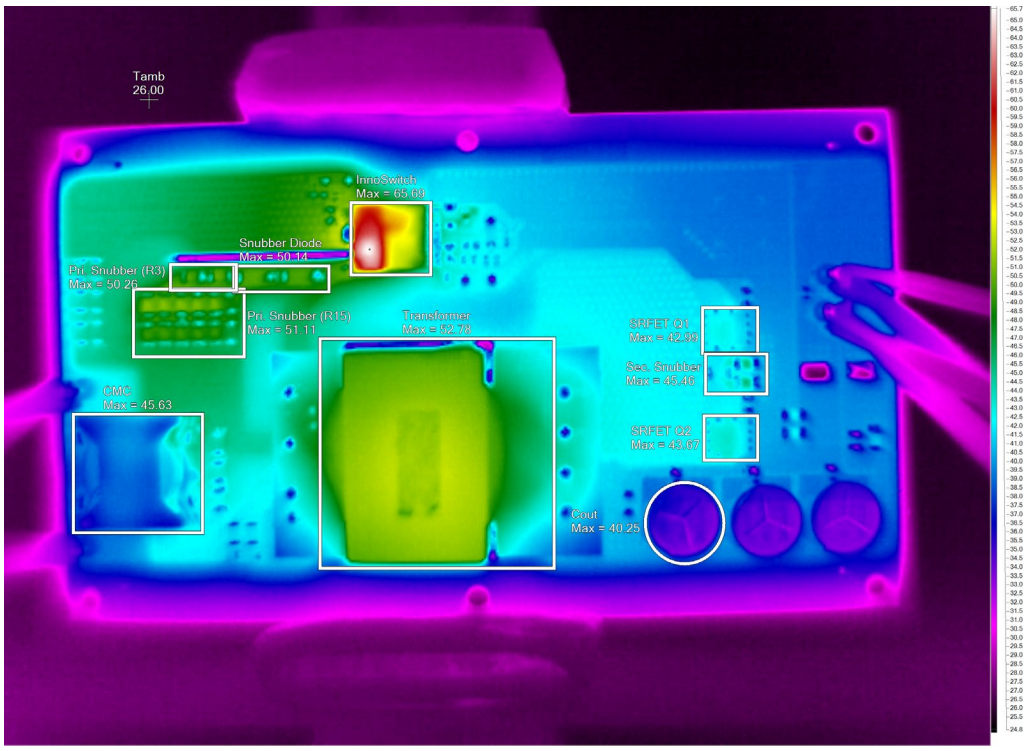


Figure 34 – Thermal Scan of the Top of the PCB at 800 V Input.

Figure 35 – Thermal Scan of the Top of the PCB at 1000 V Input.

12 Waveforms

12.1 Start-Up Waveforms

The following measurements were taken by connecting the unit into a fully charged DC link capacitor[25] at different input voltages. A *constant resistance* load configuration was used for all start up tests.

12.1.1 Output Voltage and Current at 25 ºC Ambient[26,27]

12.1.1.1 No Load

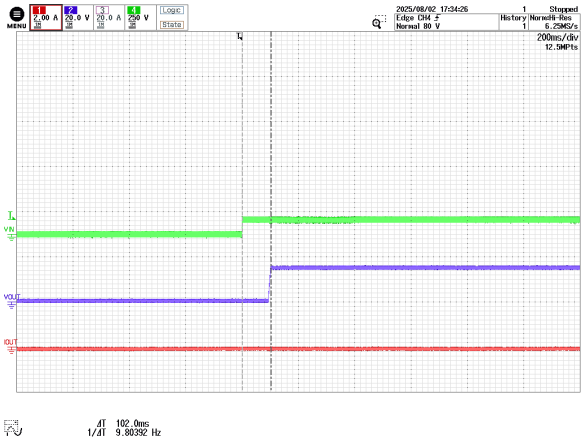


Figure 36 – Output Voltage and Current.
80 VDC, No Load.
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

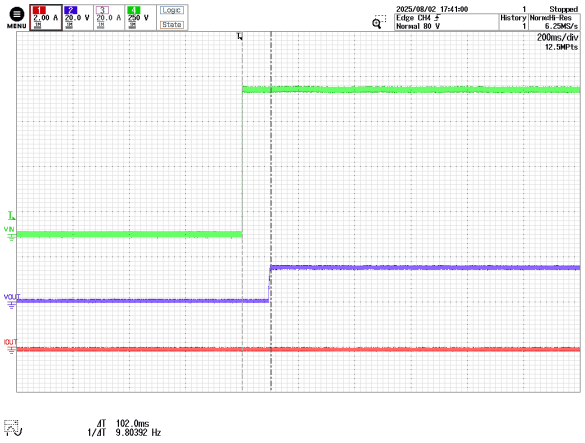


Figure 37 – Output Voltage and Current.
800 VDC, No Load.
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

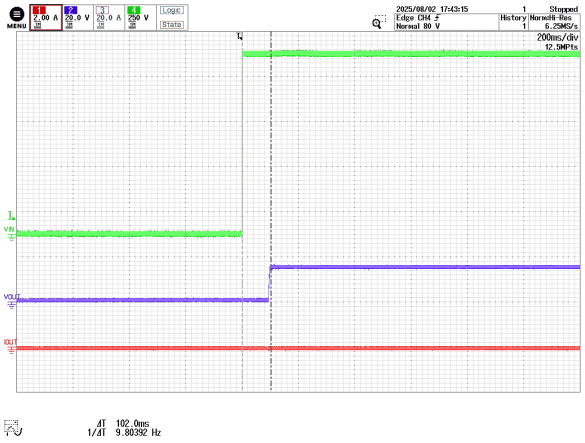


Figure 38 – Output Voltage and Current.
1000 VDC, No Load.
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

[25] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[26] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.
[27] The instance of small step increase seen on the I_{OUT} waveform was due to the Constant Resistance (CR) mode response of the electronic load.

12.1.1.2 27 W Continuous Output Power

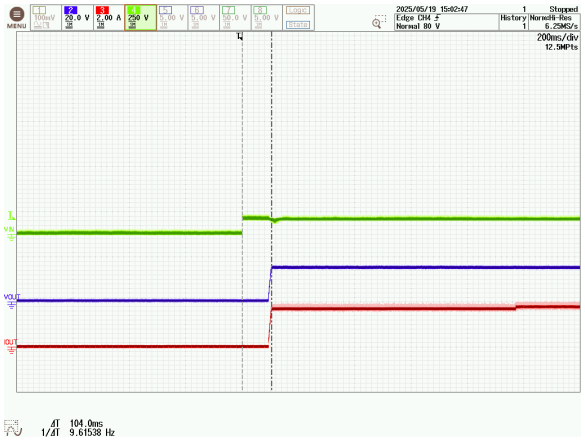


Figure 39 – Output Voltage and Current.
80 VDC, 8.33 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 40 – Output Voltage and Current.
800 VDC, 8.33 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 41 – Output Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

12.1.1.3 35 W Peak Output Power

Figure 42 – Output Voltage and Current.
80 VDC, 6.43 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 43 – Output Voltage and Current.
800 VDC, 6.43 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 44 – Output Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

12.1.2 InnoSwitch3-AQ Drain Voltage and Current at 25 ºC Ambient[28]

12.1.2.1 No Load

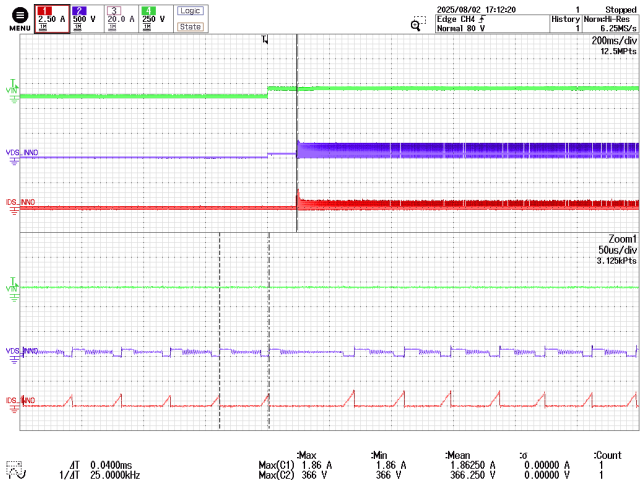


Figure 45 – INN3949CQ Drain Voltage and Current.
80 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

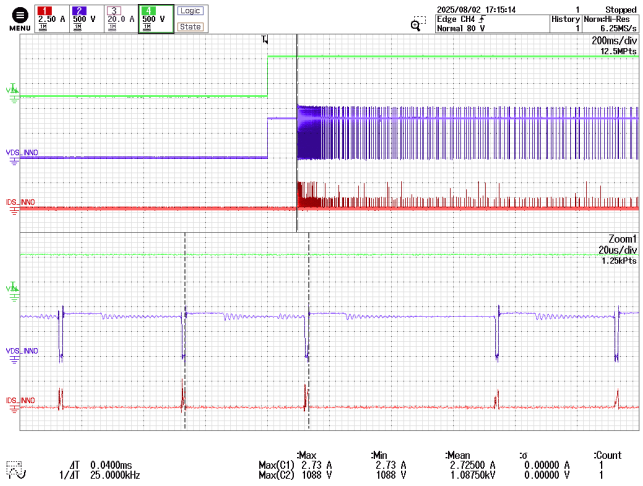


Figure 46 – INN3949CQ Drain Voltage and Current.
800 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

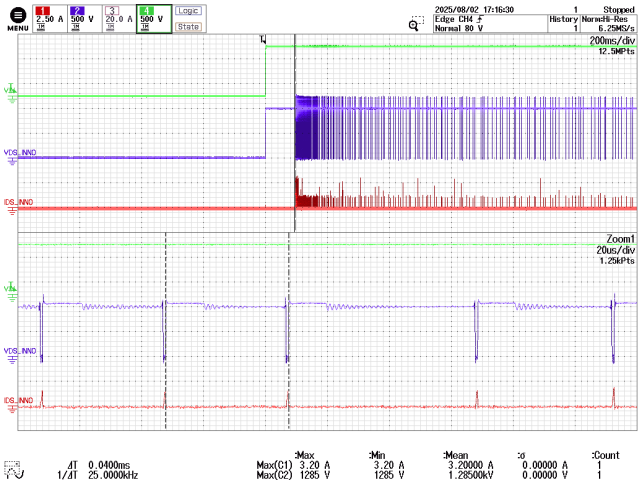


Figure 47 – INN3949CQ Drain Voltage and Current.
1000 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

[28] The time between V_{IN} turn-on and the InnoSwitch3 starting switching was due to the "Wait and Listen" period of the InnoSwitch3 device.

12.1.2.2 27 W Continuous Output Power

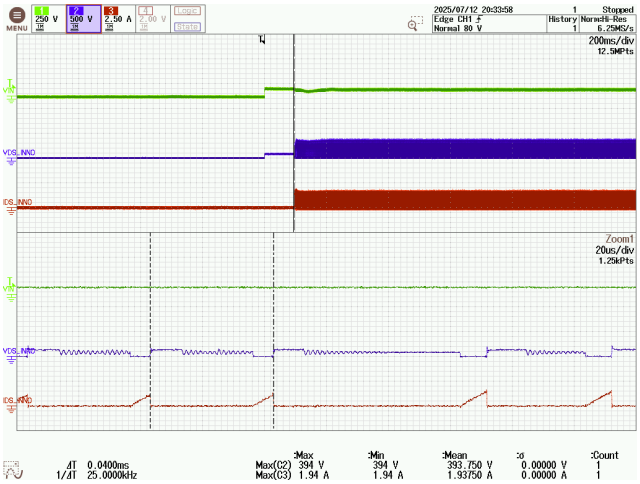


Figure 48 – INN3949CQ Drain Voltage and Current.
80 VDC, 8.33 Ω Load.
CH1: V_{IN}, 250 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

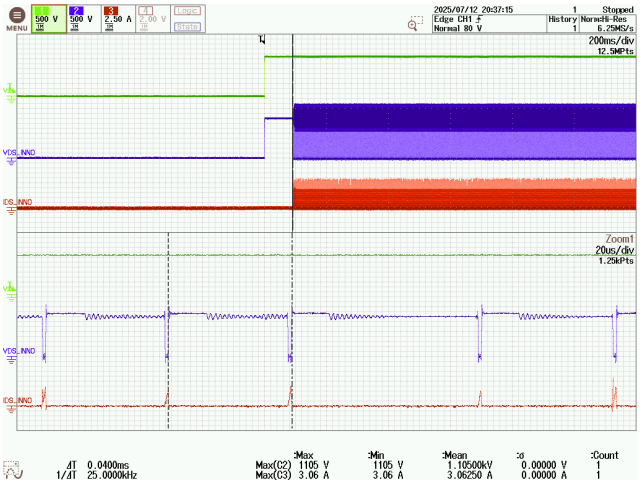


Figure 49 – INN3949CQ Drain Voltage and Current.
800 VDC, 8.33 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

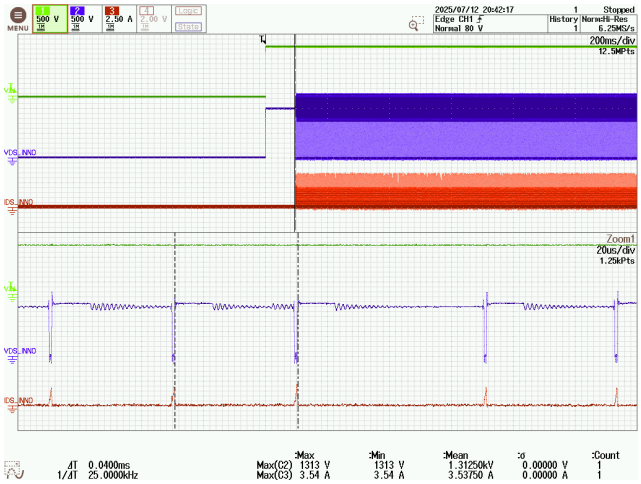


Figure 50 – INN3949CQ Drain Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

12.1.2.3 35 W Peak Output Power

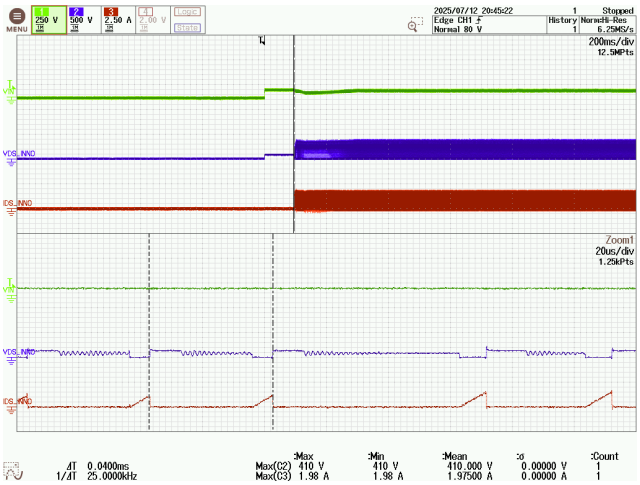


Figure 51 – INN3949CQ Drain Voltage and Current.
80 VDC, 6.43 Ω Load.
CH1: V_{IN}, 250 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

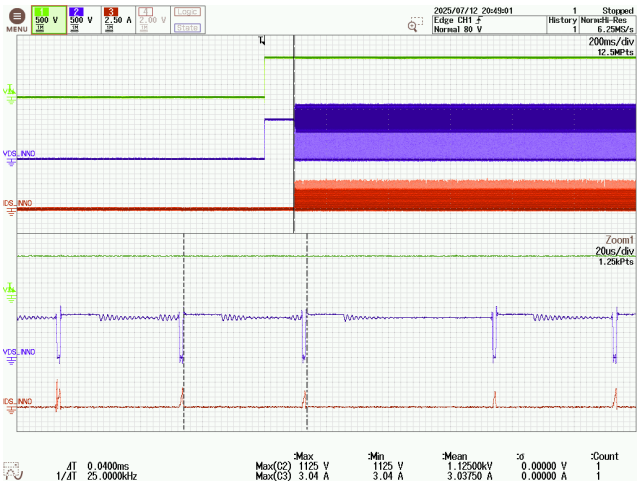


Figure 52 – INN3949CQ Drain Voltage and Current.
800 VDC, 6.43 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

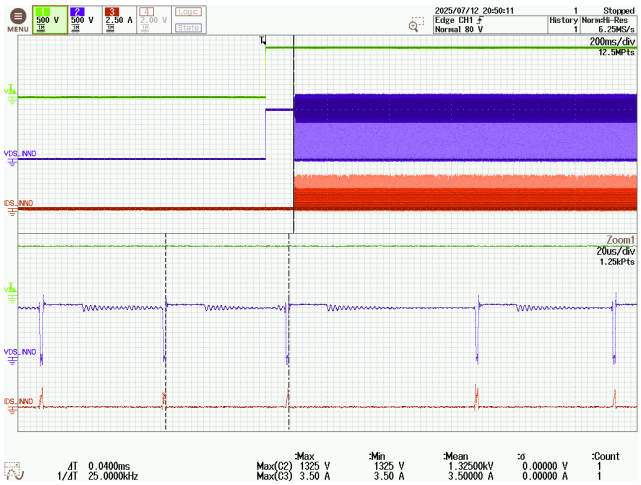


Figure 53 – INN3949CQ Drain Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

12.1.3 SR FET Drain Voltage and Current at 25 ºC Ambient[29,30]

12.1.3.1 No Load

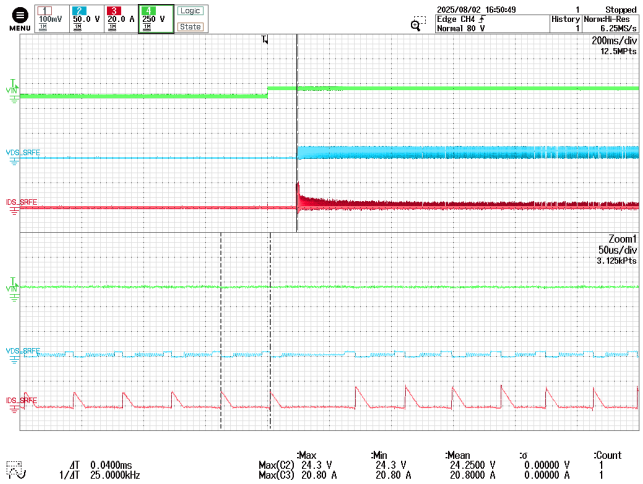


Figure 54 – SR FET Drain Voltage and Current.
80 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

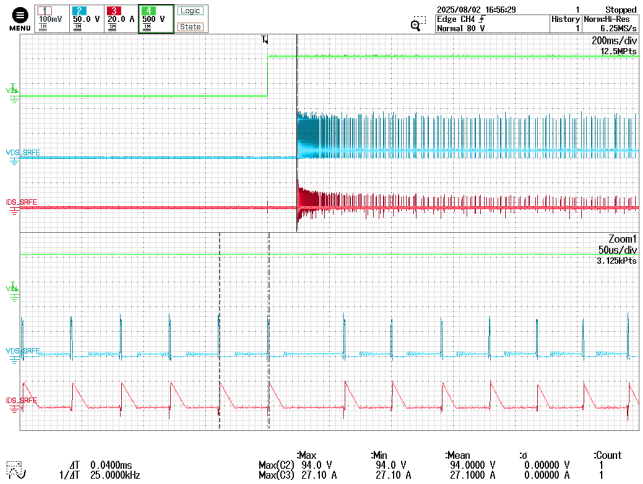


Figure 55 – SR FET Drain Voltage and Current.
800 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

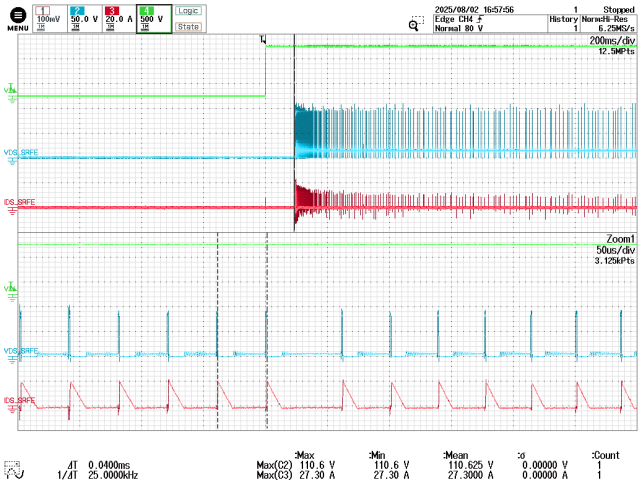


Figure 56 – SR FET Drain Voltage and Current.
1000 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

[29] The time between when V_{IN} turned on and the SR FET starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[30] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.1.3.2 27 W Continuous Output Power

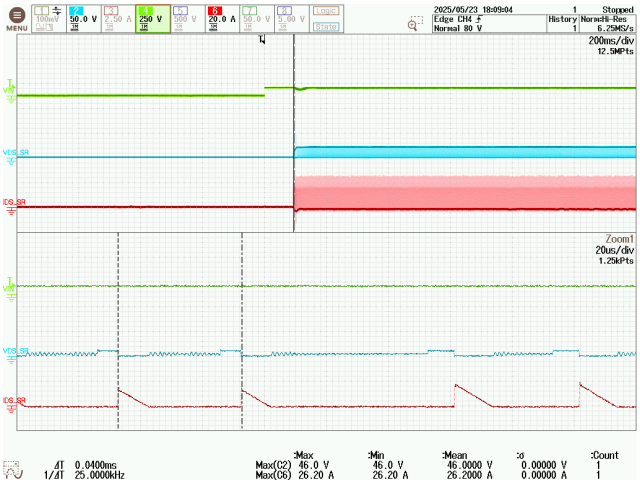


Figure 57 – SR FET Drain Voltage and Current.
80 VDC, 8.33 Ω Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH4: V_{IN}, 250 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 200 ms / div.

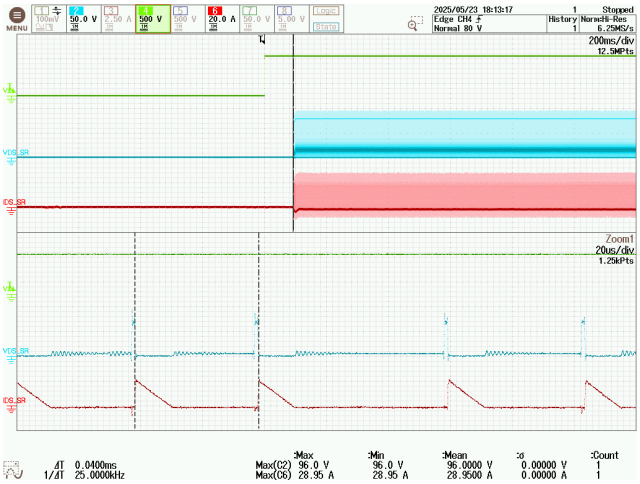


Figure 58 – SR FET Drain Voltage and Current.
800 VDC, 8.33 Ω Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 200 ms / div.

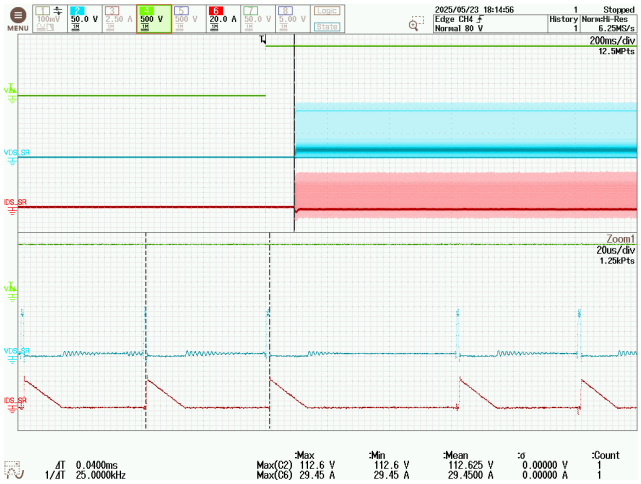


Figure 59 – SR FET Drain Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 200 ms / div.

12.1.3.3 35 W Peak Output Power

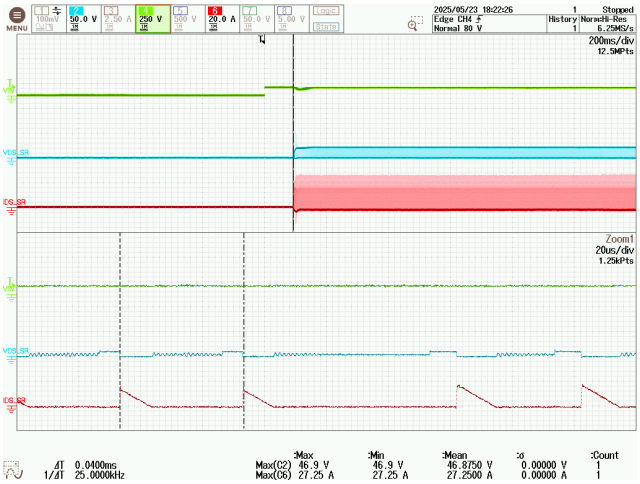


Figure 60 – SR FET Drain Voltage and Current.
80 VDC, 6.43 Ω Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH4: V_{IN}, 250 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 200 ms / div.

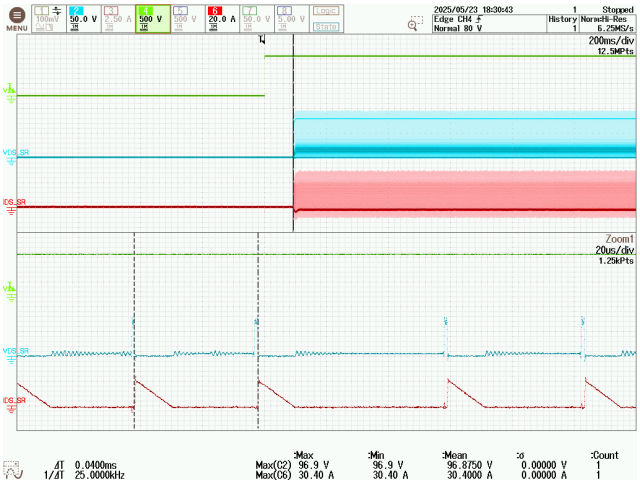


Figure 61 – SR FET Drain Voltage and Current.
800 VDC, 6.43 Ω Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 200 ms / div.

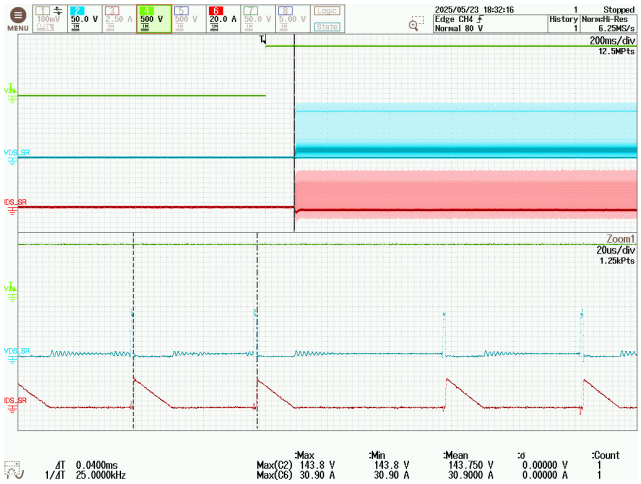


Figure 62 – SR FET Drain Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 200 ms / div.

12.1.4 Output Voltage and Current at -40 ºC Ambient[31,32]

12.1.4.1 No Load

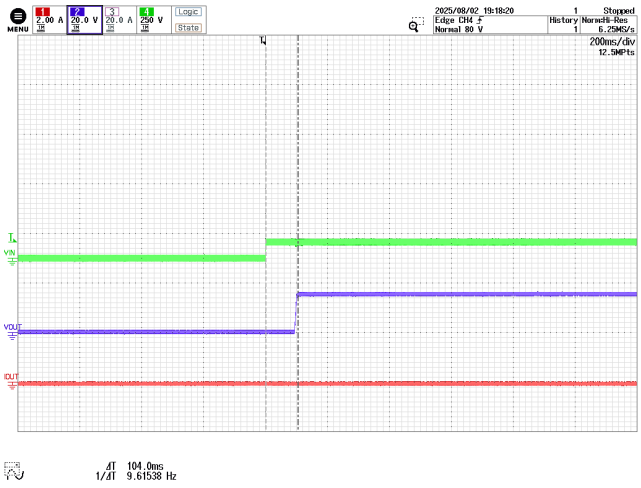


Figure 63 – Output Voltage and Current.
80 VDC, No Load
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

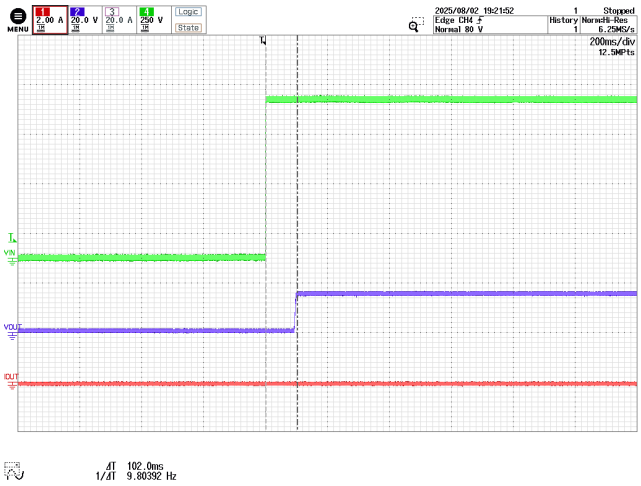


Figure 64 – Output Voltage and Current.
800 VDC, No Load.
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

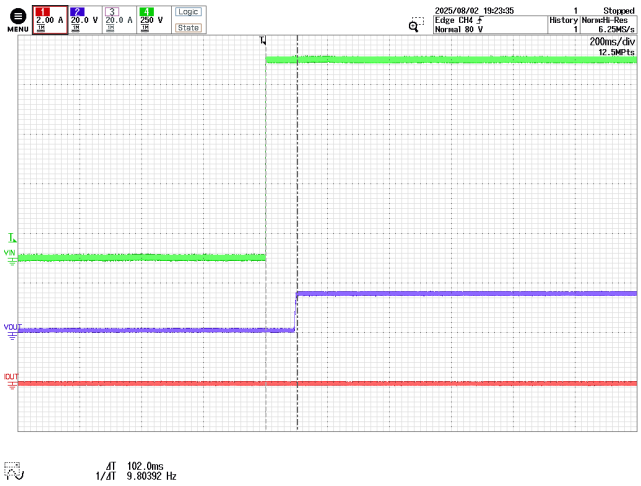


Figure 65 – Output Voltage and Current.
1000 VDC, No Load.
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

[31] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.
[32] The instance of small step increase seen on the I_{OUT} waveform was due to the Constant Resistance (CR) mode response of the electronic load.

12.1.4.2 27 W Continuous Output Power

Figure 66 – Output Voltage and Current.
80 VDC, 8.33 Ω Load
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 67 – Output Voltage and Current.
800 VDC, 8.33 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 68 – Output Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

12.1.4.3 35 W Peak Output Power

Figure 69 – Output Voltage and Current.
80 VDC, 6.43 Ω Load
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 70 – Output Voltage and Current.
800 VDC, 6.43 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 71 – Output Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

12.1.5 InnoSwitch3-AQ Drain Voltage and Current at -40 ºC Ambient[33]

12.1.5.1 No Load

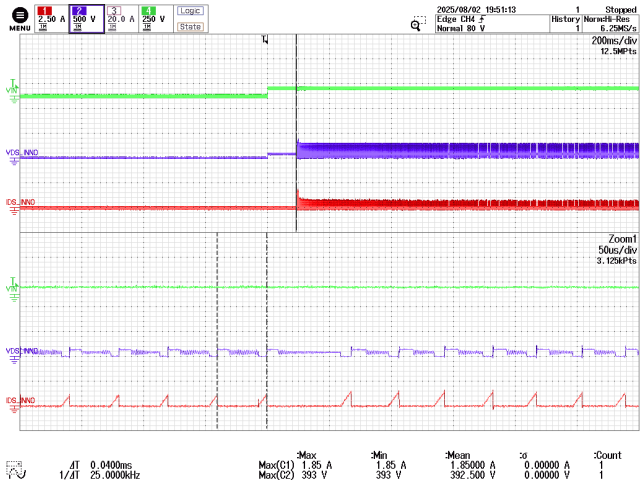


Figure 72 – INN3949CQ Drain Voltage and Current.
80 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

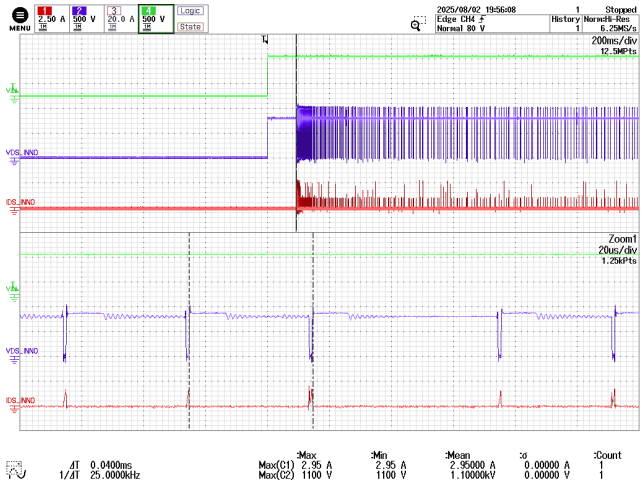


Figure 73 – INN3949CQ Drain Voltage and Current.
800 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

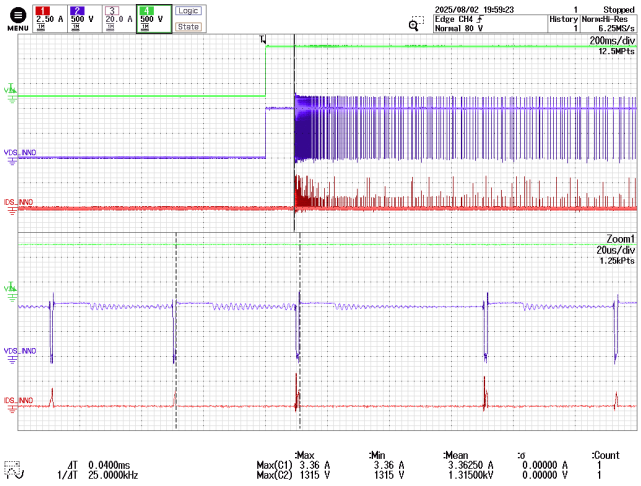


Figure 74 – INN3949CQ Drain Voltage and Current.
1000 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

[33] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.

12.1.5.2 27 W Continuous Output Power

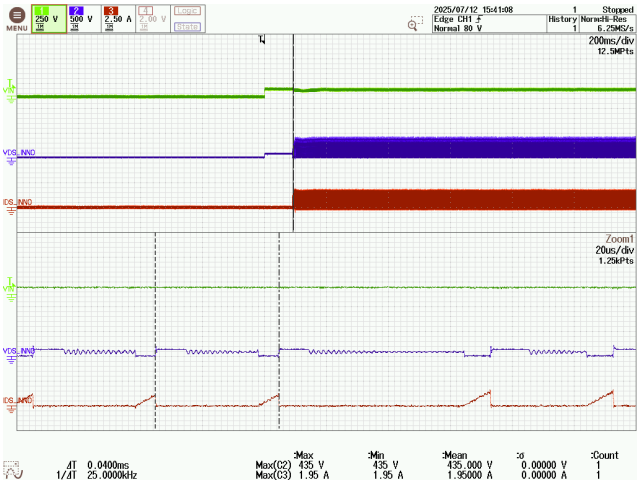


Figure 75 – INN3949CQ Drain Voltage and Current.
80 VDC, 8.33 Ω Load.
CH1: V_{IN}, 250 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

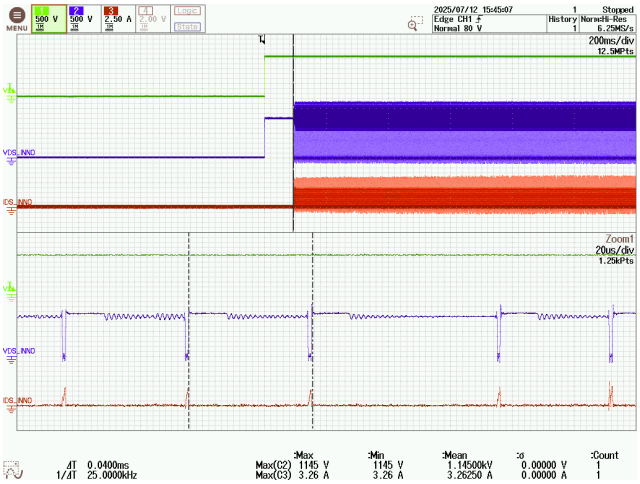


Figure 76 – INN3949CQ Drain Voltage and Current.
800 VDC, 8.33 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

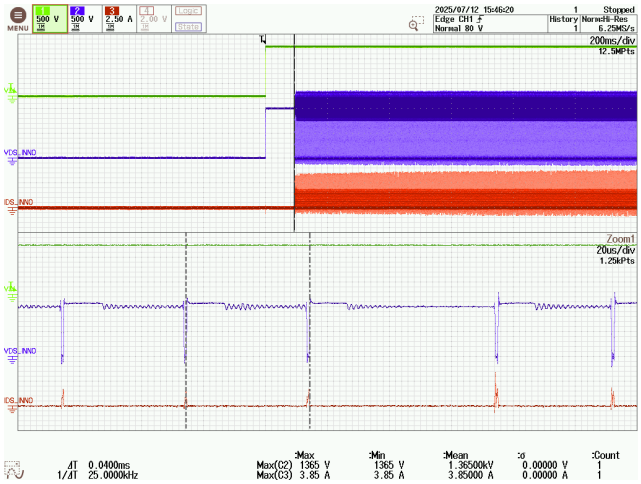


Figure 77 – INN3949CQ Drain Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

12.1.5.3 35 W Peak Output Power

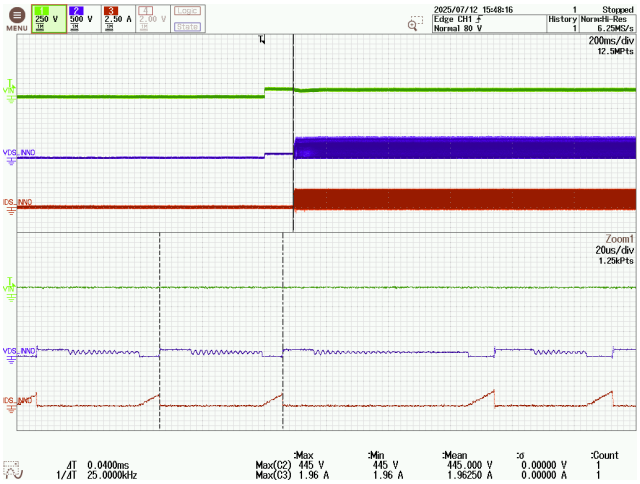


Figure 78 – INN3949CQ Drain Voltage and Current.
80 VDC, 6.43 Ω Load.
CH1: V_{IN}, 250 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

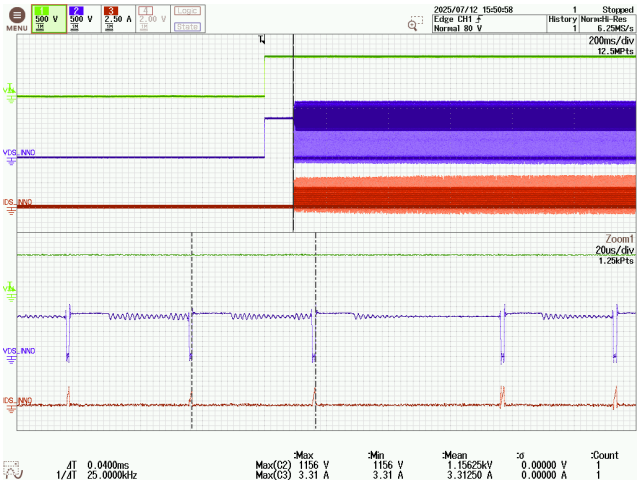


Figure 79 – INN3949CQ Drain Voltage and Current.
800 VDC, 6.43 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

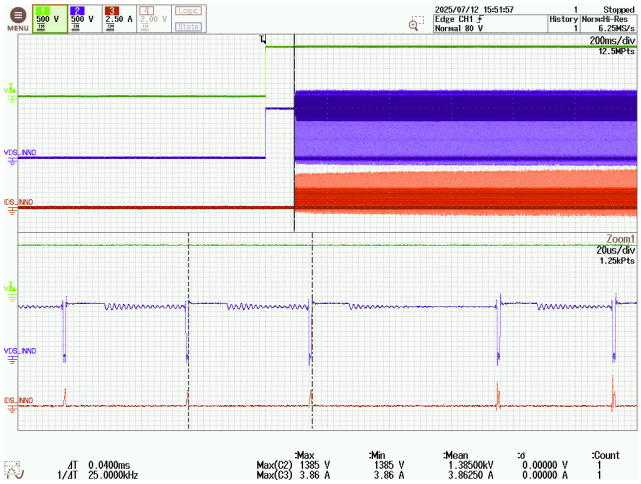


Figure 80 – INN3949CQ Drain Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

12.1.6 SR FET Drain Voltage and Current at -40 ºC Ambient[34, 35]

12.1.6.1 No Load

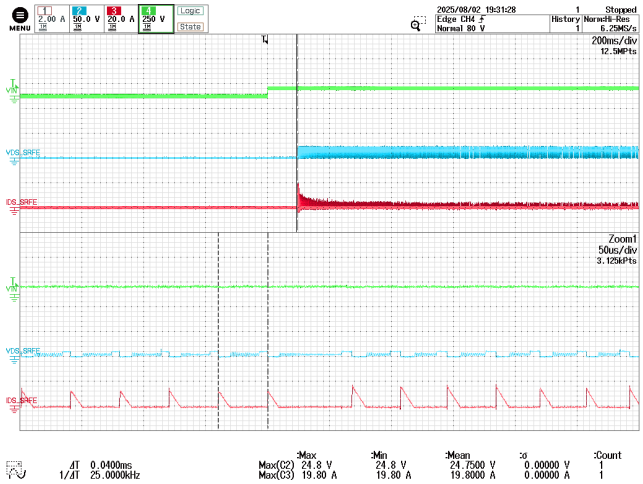


Figure 81 – SR FET Drain Voltage and Current.
80 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

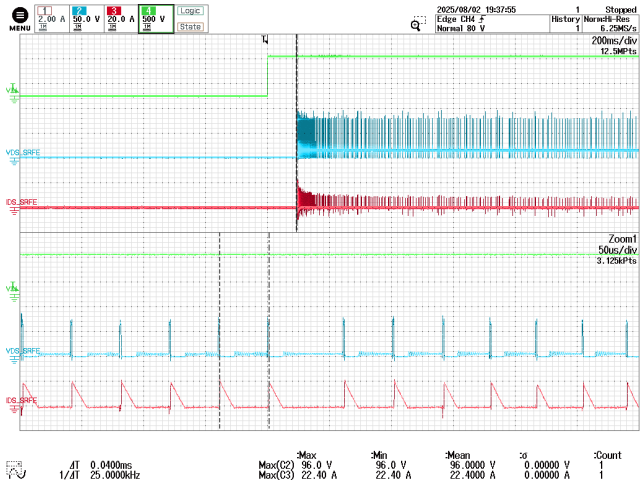


Figure 82 – SR FET Drain Voltage and Current.
800 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

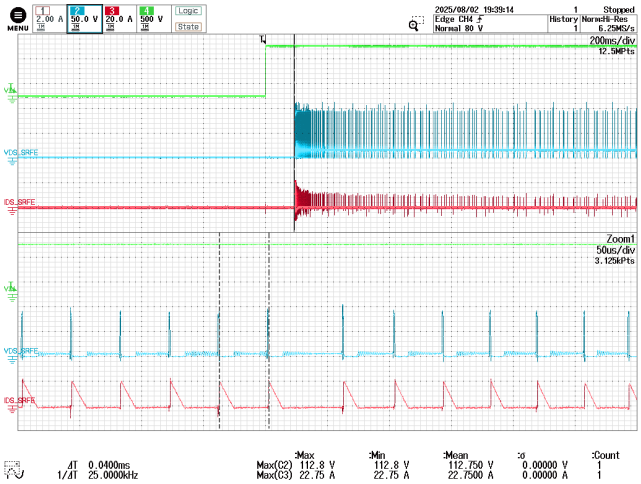


Figure 83 – SR FET Drain Voltage and Current.
1000 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

[34] The time between when V_{IN} turned on and the SR FET starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[35] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.1.6.2 27 W Continuous Output Power

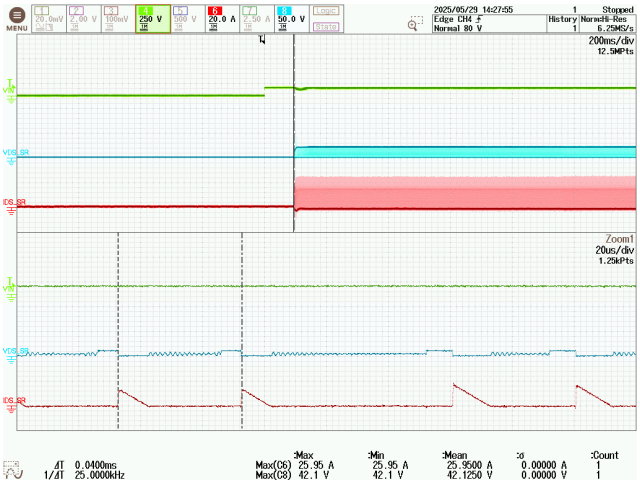


Figure 84 – SR FET Drain Voltage and Current.
80 VDC, 8.33 Ω Load.
CH4: V_{IN}, 250 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

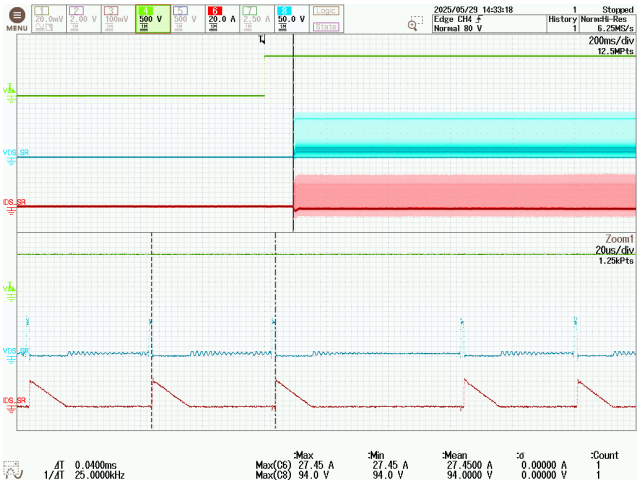


Figure 85 – SR FET Drain Voltage and Current.
800 VDC, 8.33 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

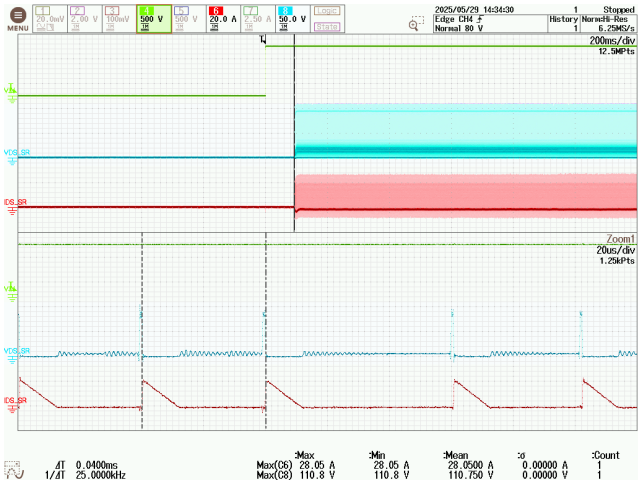


Figure 86 – SR FET Drain Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

12.1.6.3 35 W Peak Output Power

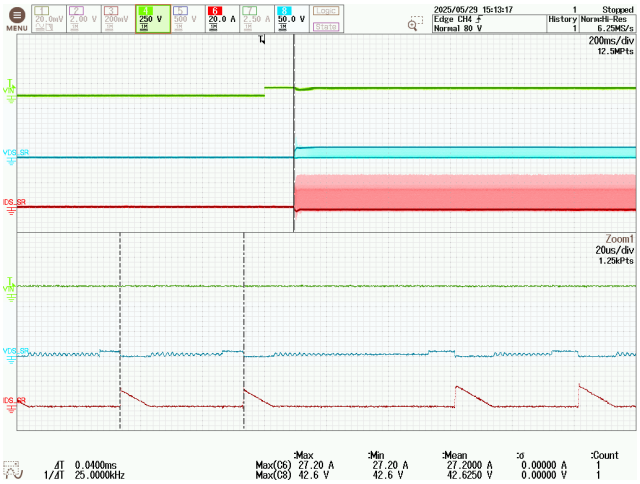


Figure 87 – SR FET Drain Voltage and Current.
80 VDC, 6.43 Ω Load.
CH4: V_{IN}, 250 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

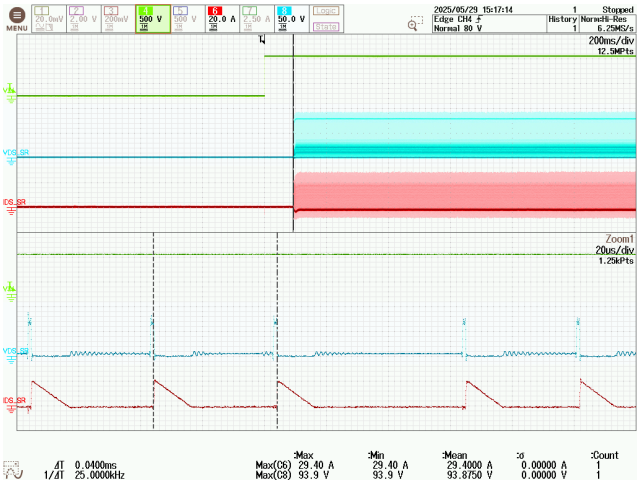


Figure 88 – SR FET Drain Voltage and Current.
800 VDC, 6.43 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

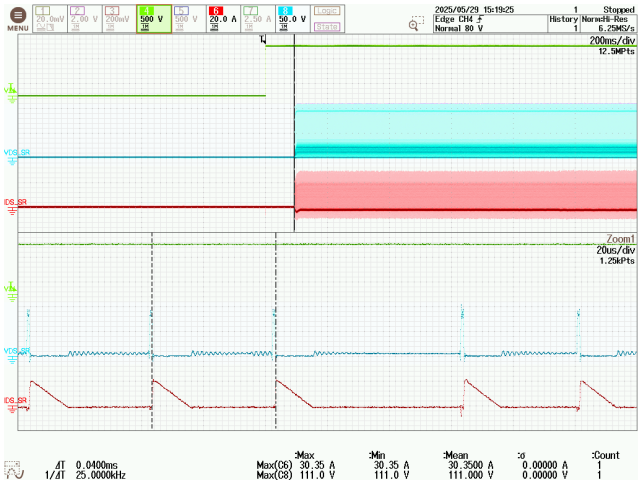


Figure 89 – SR FET Drain Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

12.1.7 Output Voltage and Current at 85 ºC Ambient[36,37]

12.1.7.1 No Load

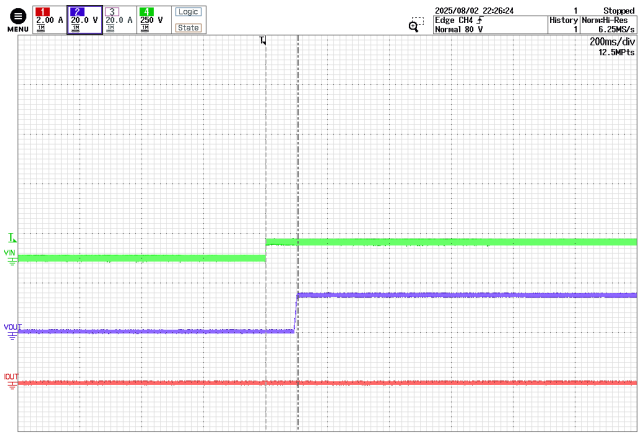


Figure 90 – Output Voltage and Current.
80 VDC, No Load
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

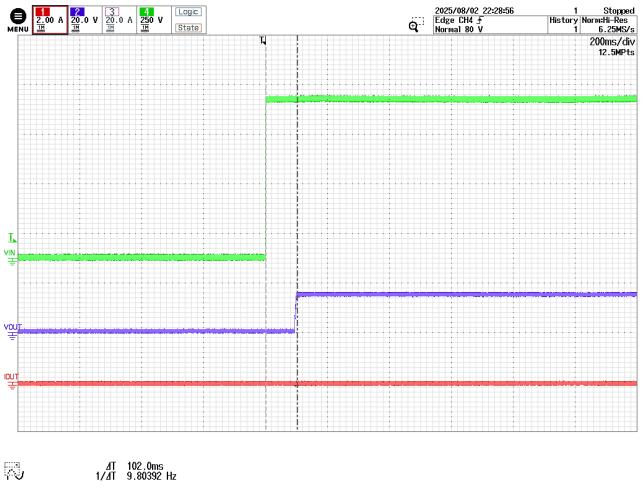


Figure 91 – Output Voltage and Current.
800 VDC, No Load.
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

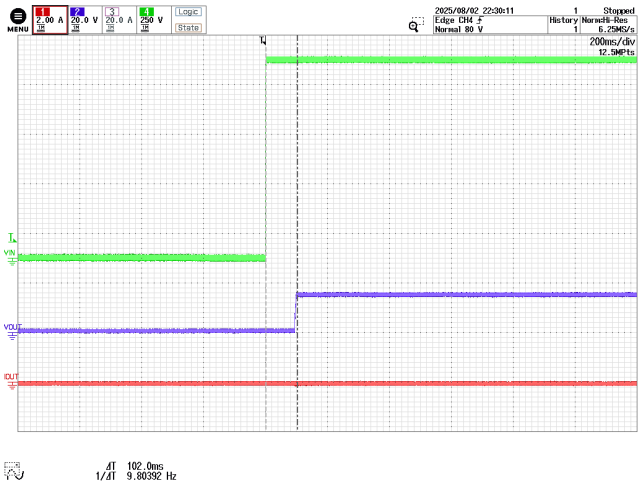


Figure 92 – Output Voltage and Current.
1000 VDC, No Load.
CH1: I_{OUT}, 2 A / div.
CH2: V_{OUT}, 20 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

[36] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.
[37] The instance of small step increase seen on the I_{OUT} waveform was due to the Constant Resistance (CR) mode response of the electronic load.

12.1.7.2 27 W Continuous Output Power

Figure 93 – Output Voltage and Current.
80 VDC, 8.33 Ω Load
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 94 – Output Voltage and Current.
800 VDC, 8.33 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 95 – Output Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

12.1.7.3 35 W Peak Output Power

Figure 96 – Output Voltage and Current.
80 VDC, 6.43 Ω Load
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 97 – Output Voltage and Current.
800 VDC, 6.43 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

Figure 98 – Output Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH2: V_{OUT}, 20 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

12.1.8 InnoSwitch3-AQ Drain Voltage and Current at 85 ºC Ambient[38]

12.1.8.1 No Load

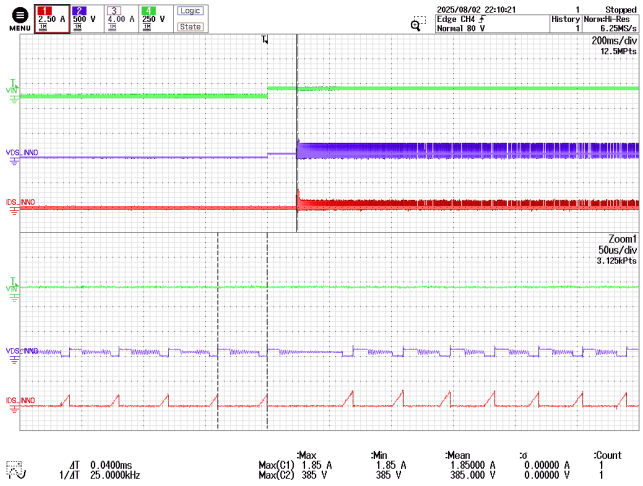


Figure 99 – INN3949CQ Drain Voltage and Current.
80 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

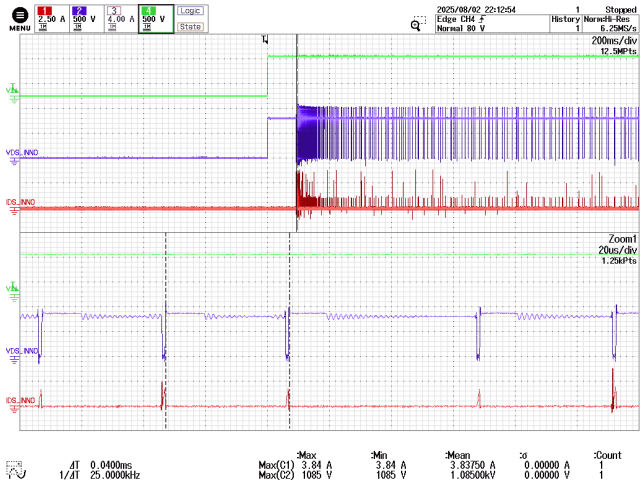


Figure 100 – INN3949CQ Drain Voltage and Current.
800 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

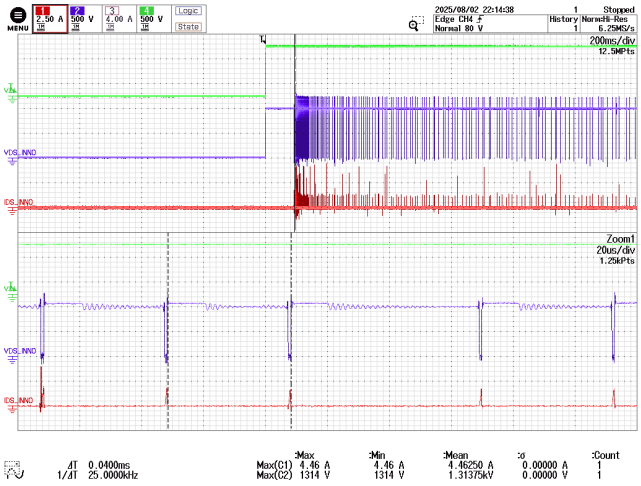


Figure 101 – INN3949CQ Drain Voltage and Current.
1000 VDC, No Load.
CH1: I_D, 2.5 A / div.
CH2: V_{DS}, 500 V / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

[38] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.

12.1.8.2 27 W Continuous Output Power

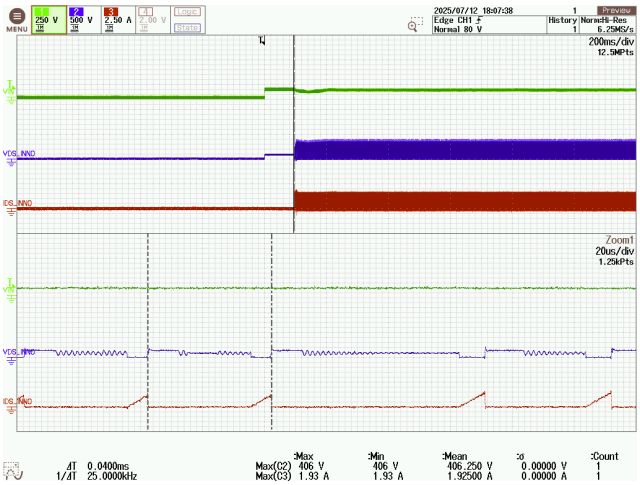


Figure 102 – INN3949CQ Drain Voltage and Current.
80 VDC, 8.33 Ω Load.
CH1: V_{IN}, 250 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

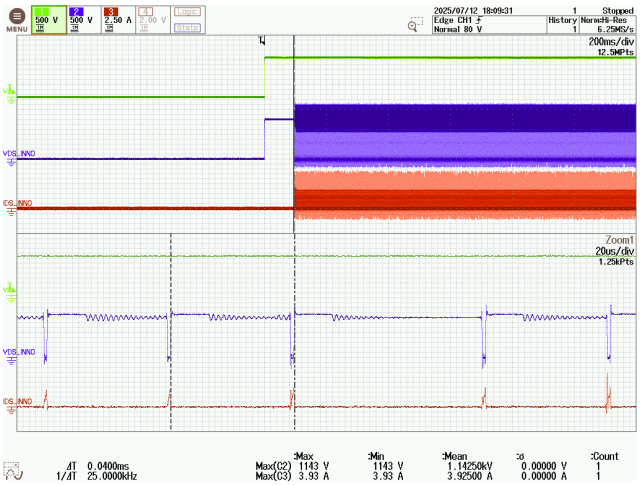


Figure 103 – INN3949CQ Drain Voltage and Current.
800 VDC, 8.33 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

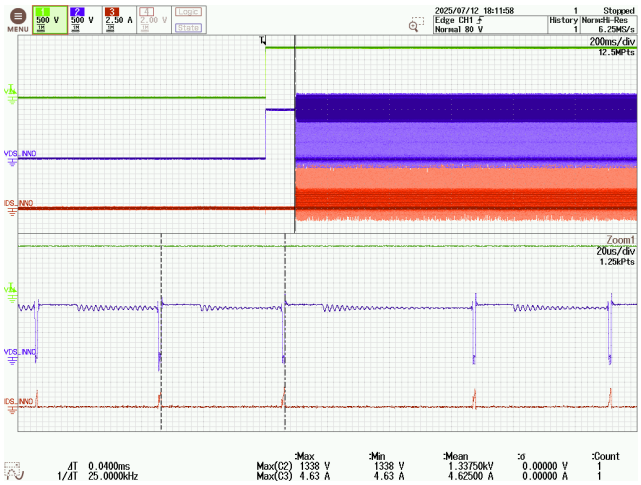


Figure 104 – INN3949CQ Drain Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

12.1.8.3 35 W Peak Output Power

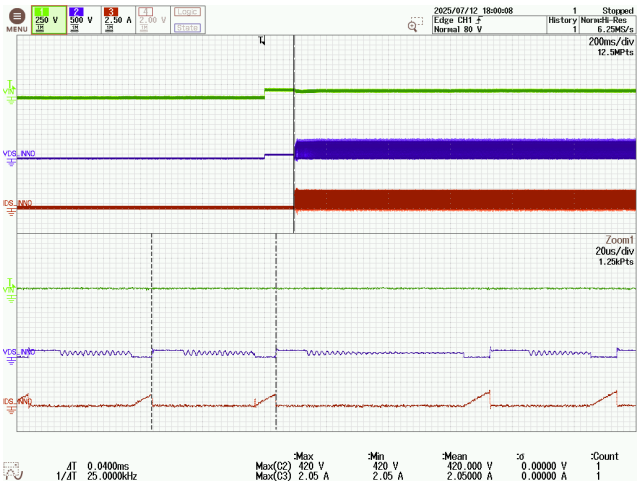


Figure 105 – INN3949CQ Drain Voltage and Current.
80 VDC, 6.43 Ω Load.
CH1: V_{IN}, 250 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

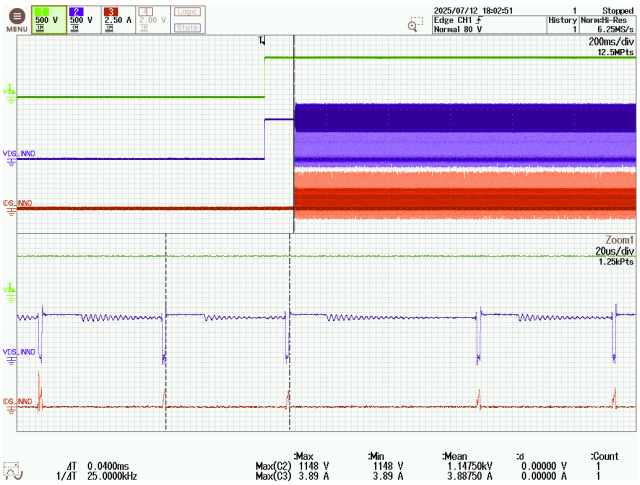


Figure 106 – INN3949CQ Drain Voltage and Current.
800 VDC, 6.43 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

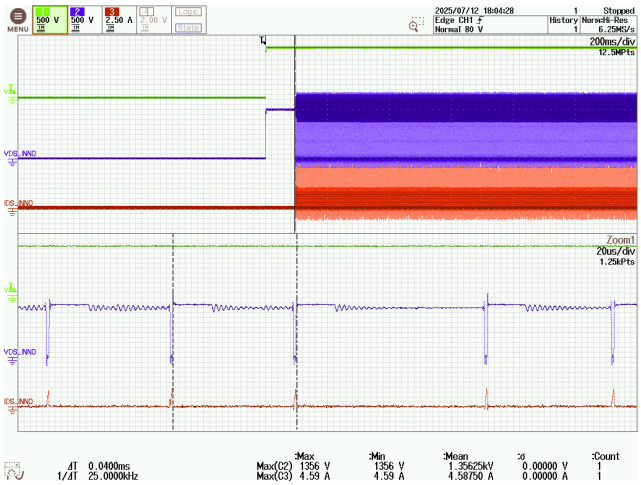


Figure 107 – INN3949CQ Drain Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{DS}, 500 V / div.
CH3: I_D, 2.5 A / div.
Time: 200 ms / div.

12.1.9 SR FET Drain Voltage and Current at 85 ºC Ambient[39,40]

12.1.9.1 No Load

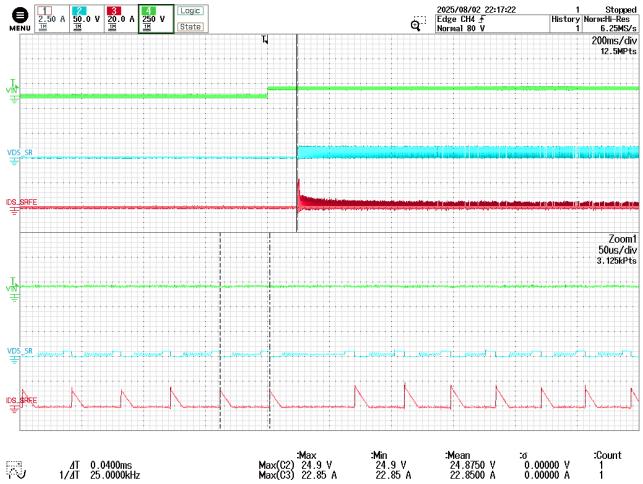


Figure 108 – SR FET Drain Voltage and Current.
80 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 250 V / div.
Time: 200 ms / div.

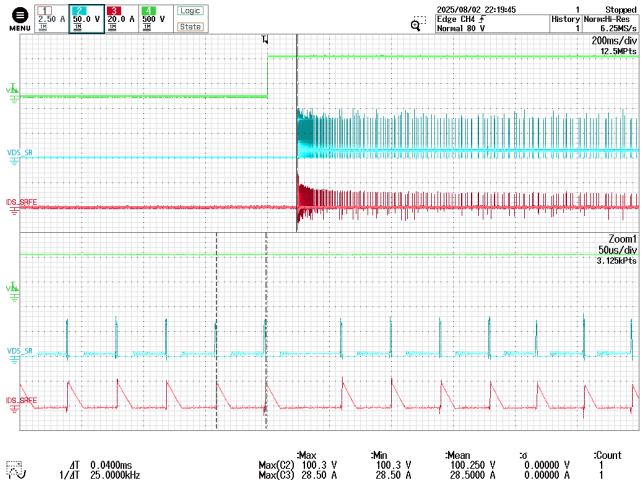


Figure 109 – SR FET Drain Voltage and Current.
800 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

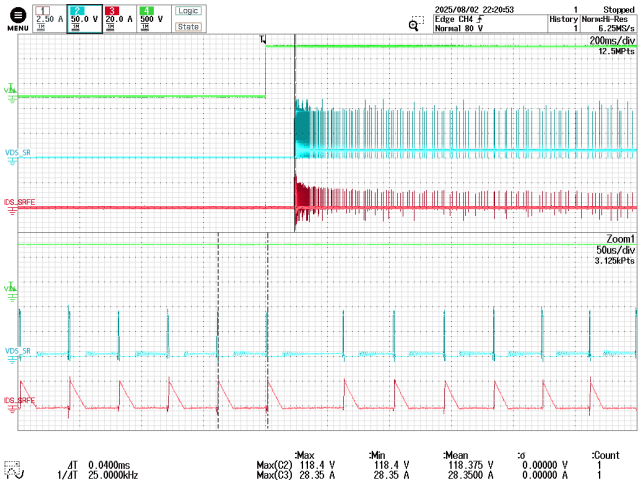


Figure 110 – SR FET Drain Voltage and Current.
1000 VDC, No Load.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 20 A / div.
CH4: V_{IN}, 500 V / div.
Time: 200 ms / div.

[39] The time between when V_{IN} turned on and the SR FET starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[40] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.1.9.2 27 W Continuous Output Power

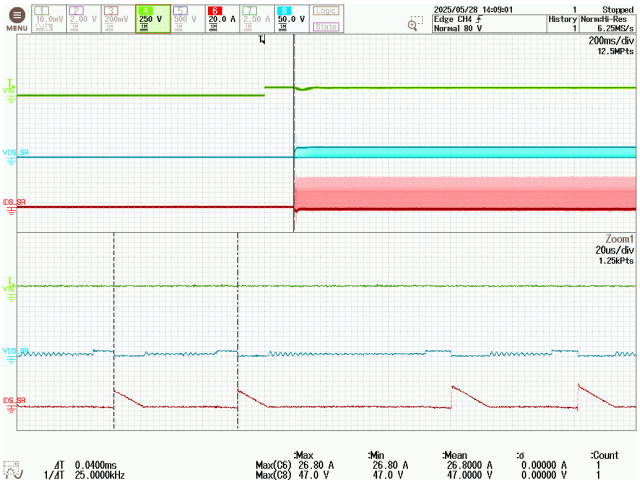


Figure 111 – SR FET Drain Voltage and Current.
80 VDC, 8.33 Ω Load.
CH4: V_{IN}, 250 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

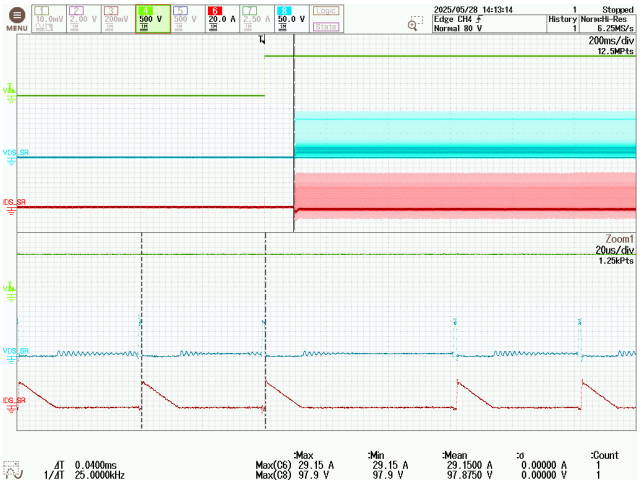


Figure 112 – SR FET Drain Voltage and Current.
800 VDC, 8.33 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

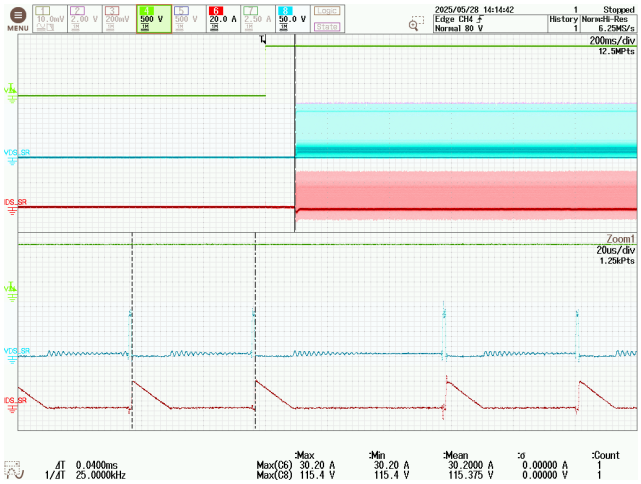


Figure 113 – SR FET Drain Voltage and Current.
1000 VDC, 8.33 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

12.1.9.3 35 W Peak Output Power

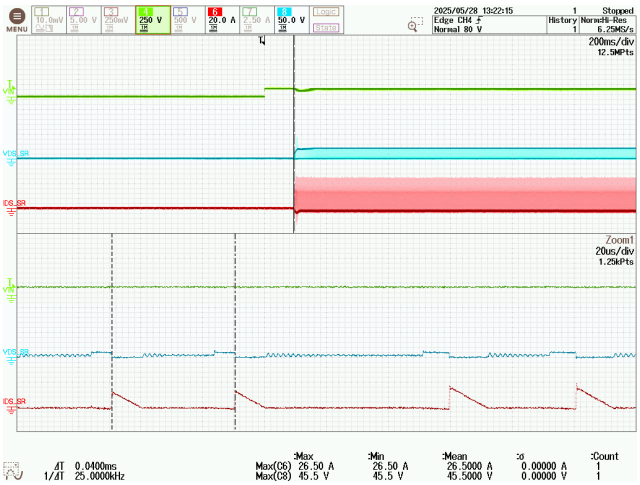


Figure 114 – SR FET Drain Voltage and Current.
80 VDC, 6.43 Ω Load.
CH4: V_{IN}, 250 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

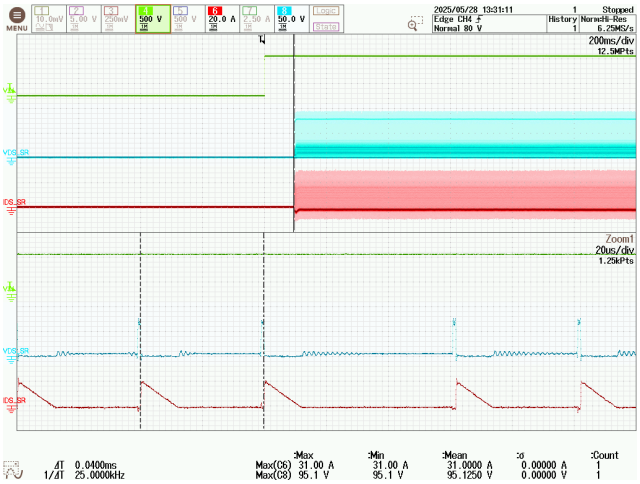


Figure 115 – SR FET Drain Voltage and Current.
800 VDC, 6.43 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

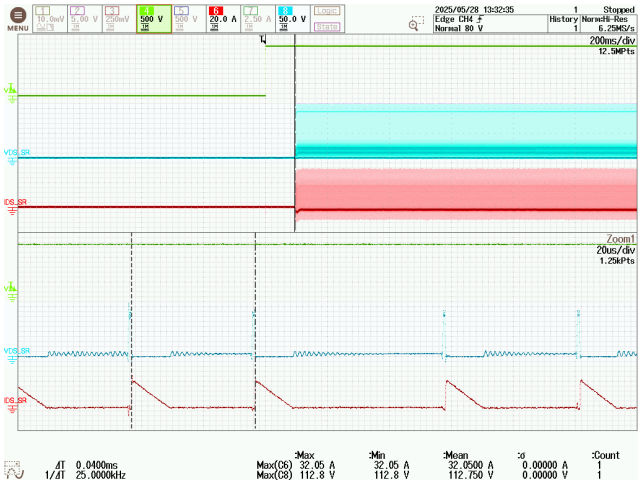


Figure 116 – SR FET Drain Voltage and Current.
1000 VDC, 6.43 Ω Load.
CH4: V_{IN}, 500 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 200 ms / div.

12.2 Steady-State Waveforms

12.2.1 Switching Waveforms at 85 ºC Ambient

12.2.1.1 Normal Operation Component Stress at No Load

	Steady-State Switching Waveforms 85 ºC Ambient, No Load					
Input	**INN3949CQ**			**SR FET**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[41]**	**V_{DS} (V)[42]**	**V_{STRESS} (%)**
80	0.71	303	17.8	4.97	25.6	17.1
400	0.98	626	36.8	8.64	64.6	43.1
800	1.18	1038	61.1	12.4	101	67.3
1000	1.33	1245	73.2	14.1	119	79.2

Table 11 – Summary of Voltage Stress on Critical Component at 85 ºC Ambient.

[41] SR FET current is the sum of Q1 and Q2 currents.
[42] SR FET voltage was taken from Q2.

12.2.1.1.1 InnoSwitch3-AQ Drain Voltage and Current at 85 ºC Ambient

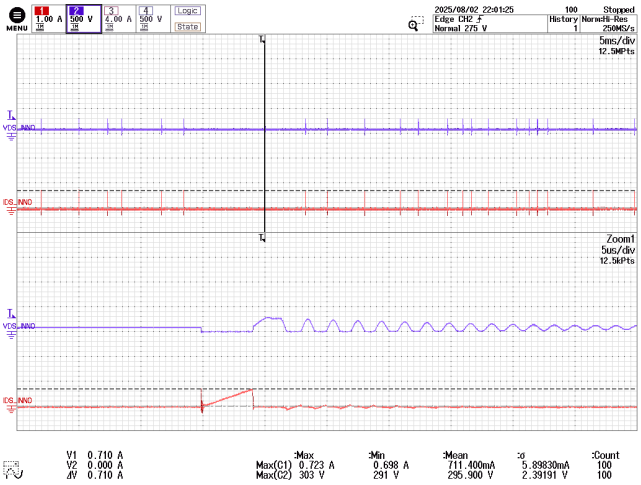


Figure 117 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, No Load, 85 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

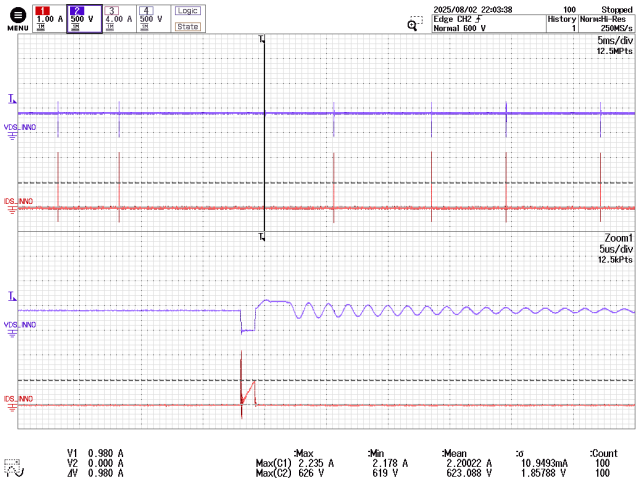


Figure 118 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, No Load, 85 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

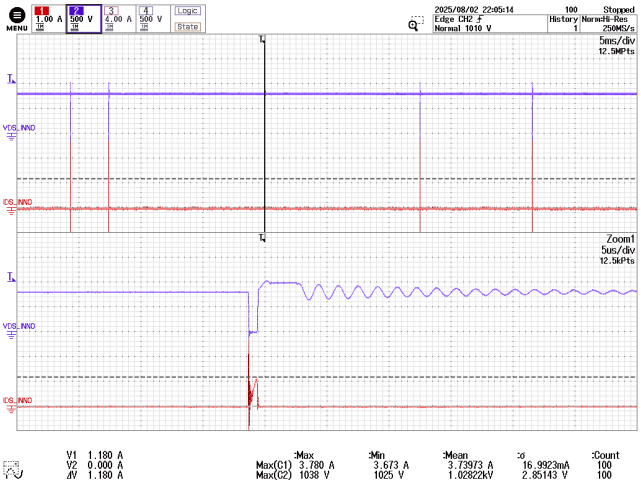


Figure 119 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, No Load, 85 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

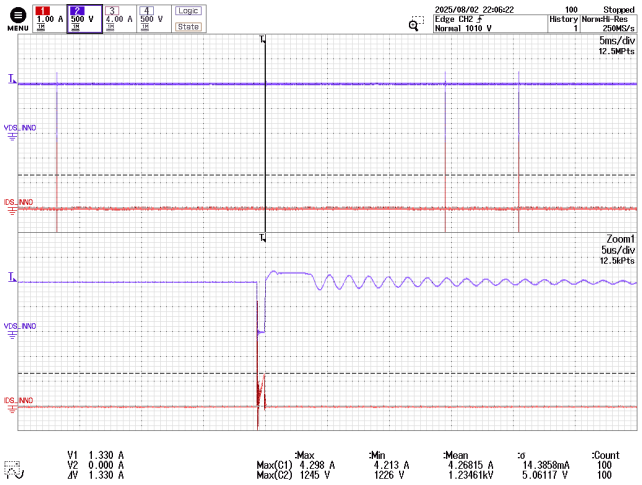


Figure 120 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, No Load, 85 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

12.2.1.1.2 SR FET Drain Voltage and Current at 85 ºC Ambient[43]

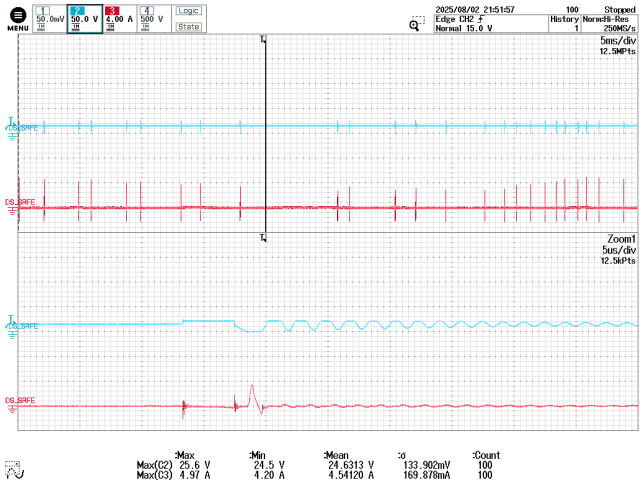


Figure 121 – SR FET Drain Voltage and Current.
80 VDC, No Load, 85 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

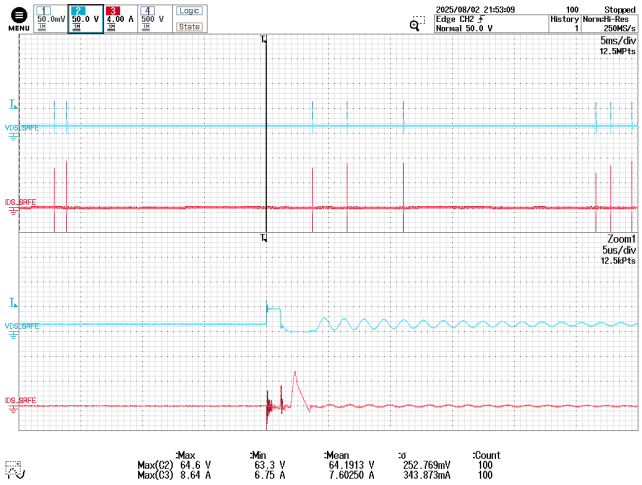


Figure 122 – SR FET Drain Voltage and Current.
400 VDC, No Load, 85 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

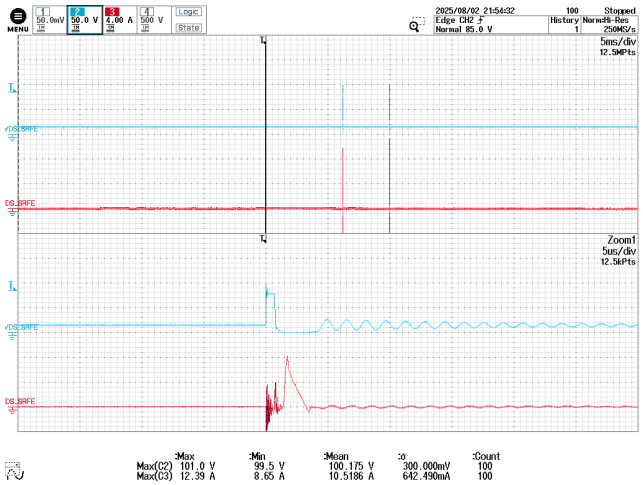


Figure 123 – SR FET Drain Voltage and Current.
800 VDC, No Load, 85 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

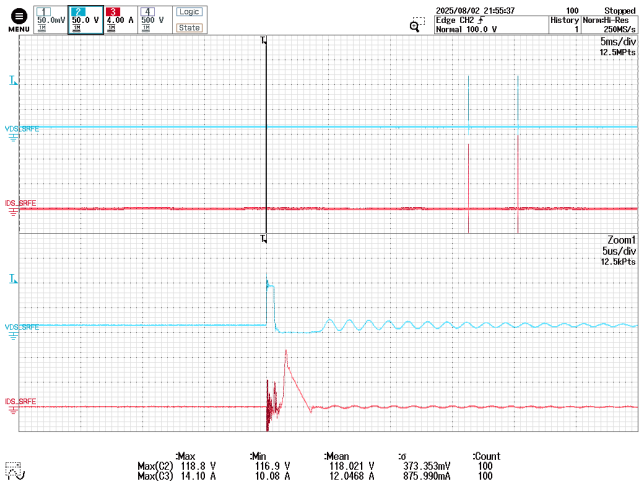


Figure 124 – SR FET Drain Voltage and Current.
1000 VDC, No Load, 85 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

[43] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.1.2 Normal Operation Component Stress at 27 W Continuous Output

	Steady-State Switching Waveforms 85 ºC Ambient, Full Load					
Input	**INN3949CQ**			**SR FET**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[44]**	**V_{DS} (V)[45]**	**V_{STRESS} (%)**
80	1.85	408	24.0	25.8	23.9	15.9
400	1.88	725	42.6	27.7	60.4	40.3
800	2.00	1125	66.2	29.1	95.6	63.7
1000	2.08	1343	79.0	30.4	112	74.7

Table 12 – Summary of Voltage Stress on Critical Component at 85 ºC Ambient.

[44] SR FET current is the sum of Q1 and Q2 currents.
[45] SR FET voltage was taken from Q2.

12.2.1.2.1 InnoSwitch3-AQ Drain Voltage and Current at 85 ºC Ambient

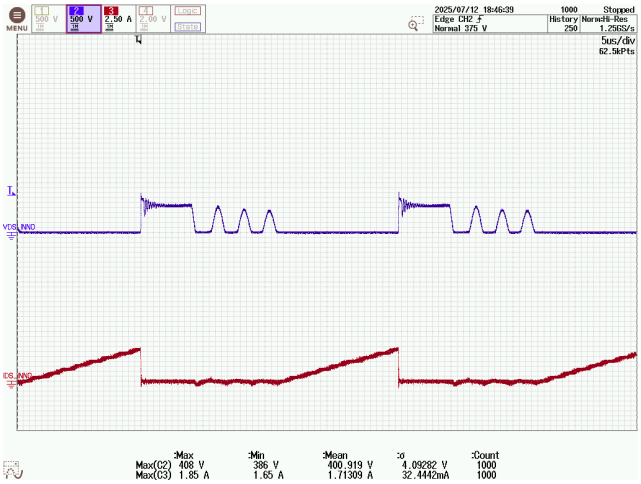


Figure 125 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, 1.8 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

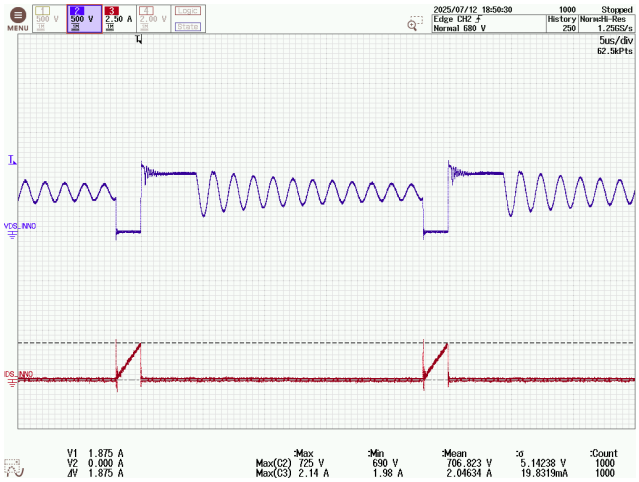


Figure 126 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 1.8 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 127 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, 1.8 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 128 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 1.8 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

12.2.1.2.2 SR FET Drain Voltage and Current at 85 ºC Ambient[46]

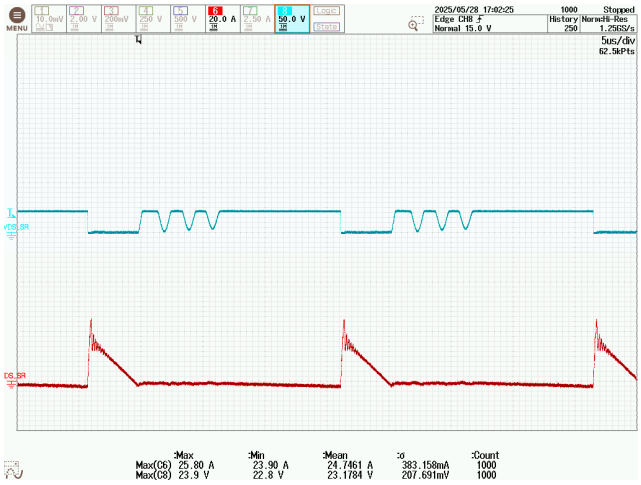


Figure 129 – SR FET Drain Voltage and Current.
80 VDC, 1.8 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

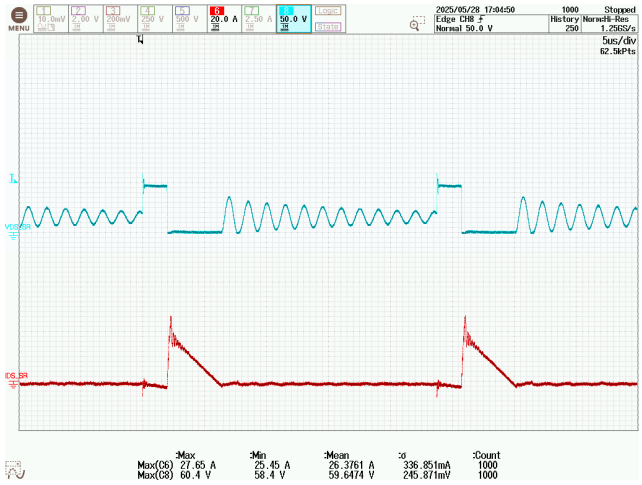


Figure 130 – SR FET Drain Voltage and Current.
400 VDC, 1.8 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

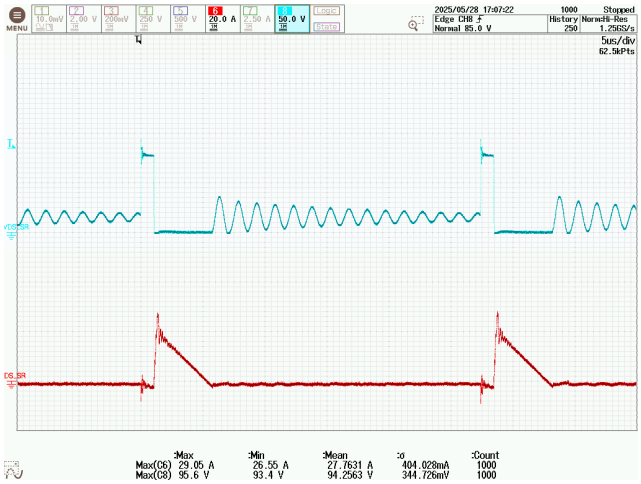


Figure 131 – SR FET Drain Voltage and Current.
800 VDC, 1.8 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

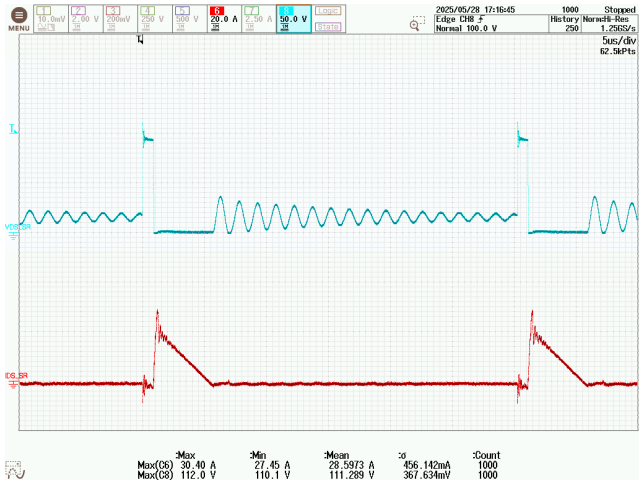


Figure 132 – SR FET Drain Voltage and Current.
1000 VDC, 1.8 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

[46] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.1.3 Normal Operation Component Stress at 35 W Peak Output

	Steady-State Switching Waveforms 85 ºC Ambient, Peak Load					
Input	**INN3949CQ**			**SR FET**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[47]**	**V_{DS} (V)[48]**	**V_{STRESS} (%)**
80	1.90	425	25	26.2	23.5	15.7
400	2.05	740	43.5	28.6	64.5	43
800	2.15	1155	67.9	31.7	95.1	63.4
1000	2.28	1355	79.7	32.6	112	74.5

Table 13 – Summary of Voltage Stress on Critical Component at 85 ºC Ambient.

[47] SR FET current is the sum of Q1 and Q2 currents.
[48] SR FET voltage was taken from Q2.

12.2.1.3.1 InnoSwitch3-AQ Drain Voltage and Current at 85 ºC Ambient

Figure 133 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, 2.33 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

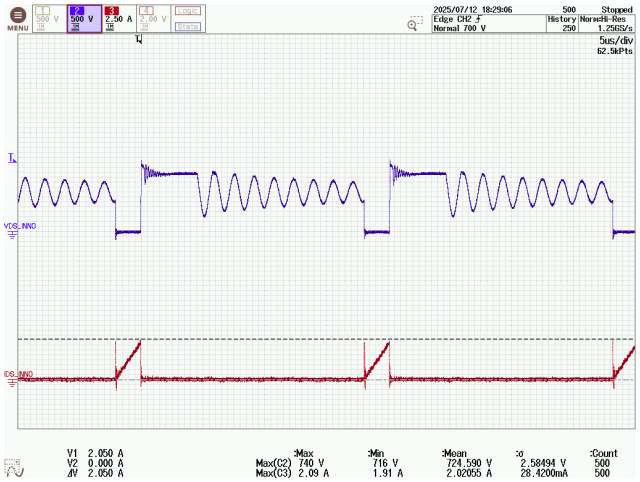


Figure 134 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 2.33 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 135 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, 2.33 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 136 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 2.33 A Load, 85 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

12.2.1.3.2 SR FET Drain Voltage and Current at 85 ºC Ambient[49]

Figure 137 – SR FET Drain Voltage and Current.
80 VDC, 2.33 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

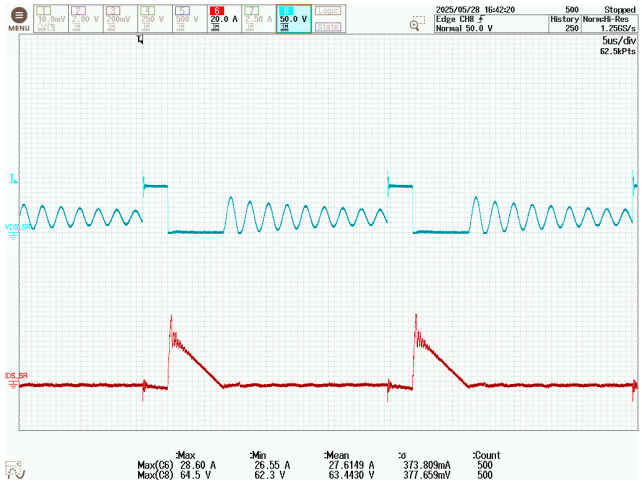


Figure 138 – SR FET Drain Voltage and Current.
400 VDC, 2.33 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

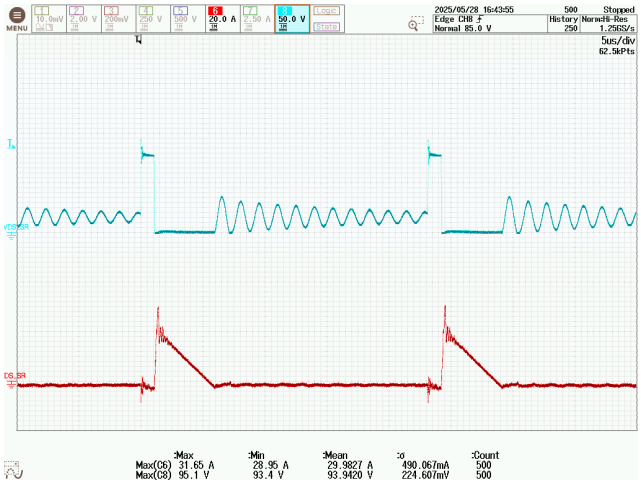


Figure 139 – SR FET Drain Voltage and Current.
800 VDC, 2.33 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

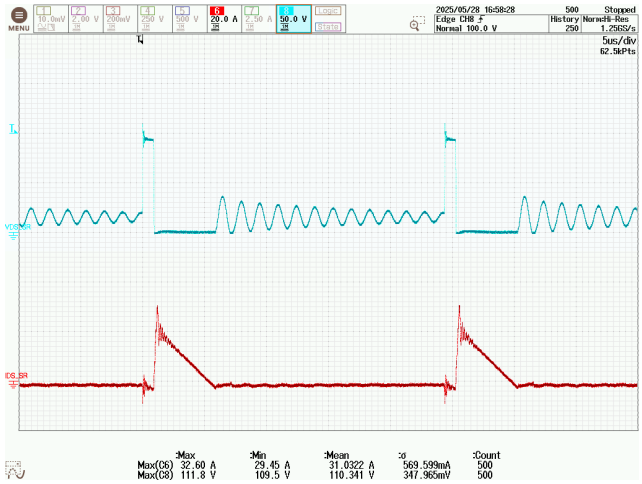


Figure 140 – SR FET Drain Voltage and Current.
1000 VDC, 2.33 A Load, 85 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

[49] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.2 Switching Waveforms at 25 ºC Ambient

12.2.2.1 Normal Operation Component Stress at No Load

	Steady-State Switching Waveforms 25 ºC Ambient, No Load					
Input	**INN3949CQ**			**SR FET**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[50]**	**V_{DS} (V)[51]**	**V_{STRESS} (%)**
80	0.81	306	18	4.63	24.6	16.4
400	1.01	636	37.4	7.51	59.8	39.9
800	1.21	1046	61.5	9.76	93.9	62.6
1000	1.36	1246	73.3	11.3	111	73.9

Table 14 – Summary of Critical Component Voltage Stresses at 25 ºC Ambient.

[50] SR FET current is the sum of Q1 and Q2 currents.
[51] SR FET voltage was taken from Q2.

12.2.2.1.1 InnoSwitch3-AQ Drain Voltage and Current at 25 ºC Ambient

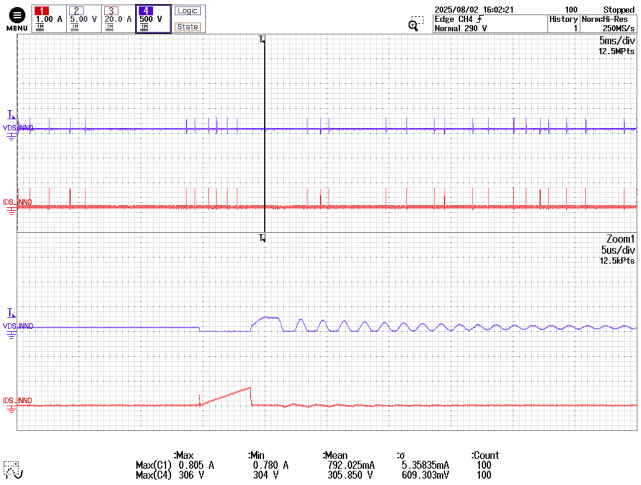


Figure 141 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, No Load, 25 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH4: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

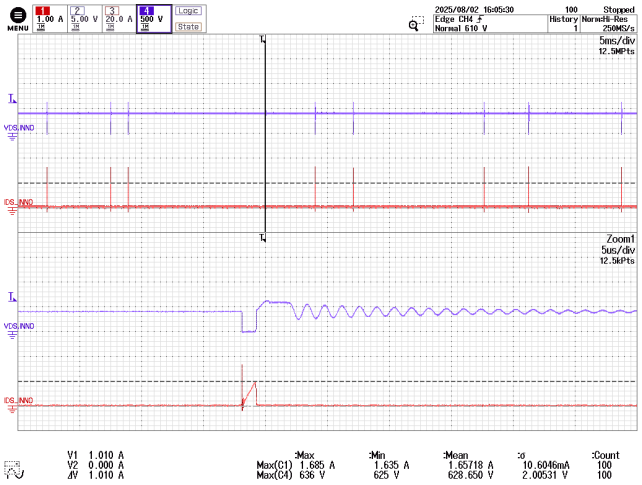


Figure 142 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, No Load, 25 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH4: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

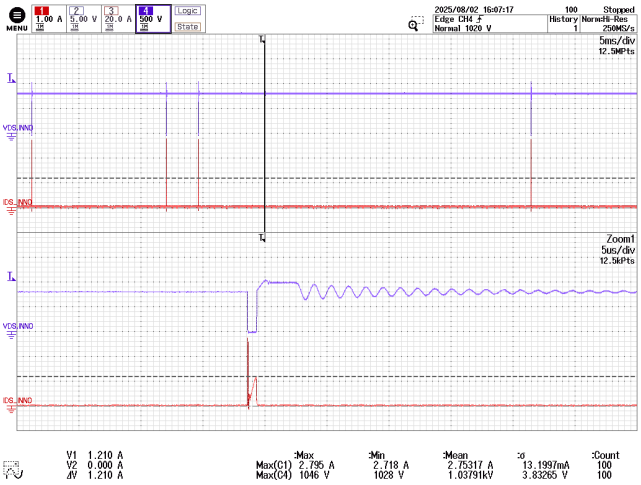


Figure 143 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, No Load, 25 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH4: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

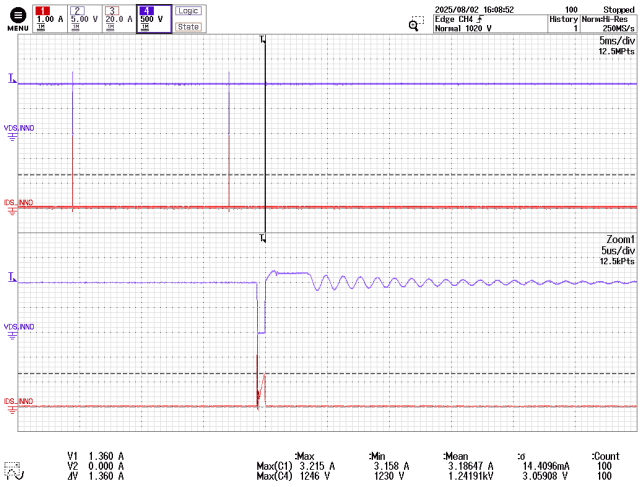


Figure 144 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, No Load, 25 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH4: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

12.2.2.1.2 SR FET Drain Voltage and Current at 25 ºC Ambient[52]

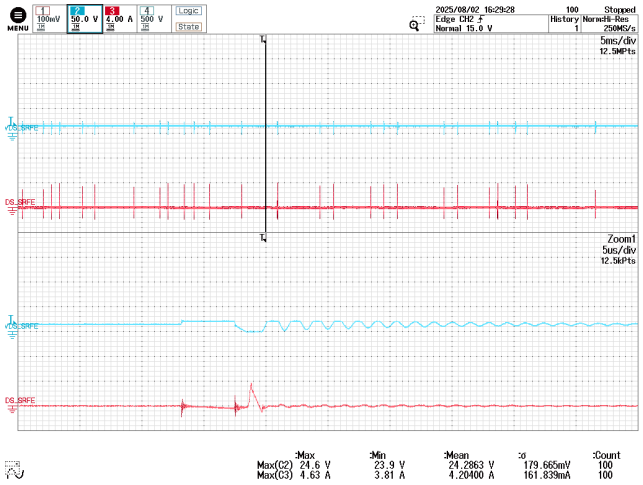


Figure 145 – SR FET Drain Voltage and Current.
80 VDC, No Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

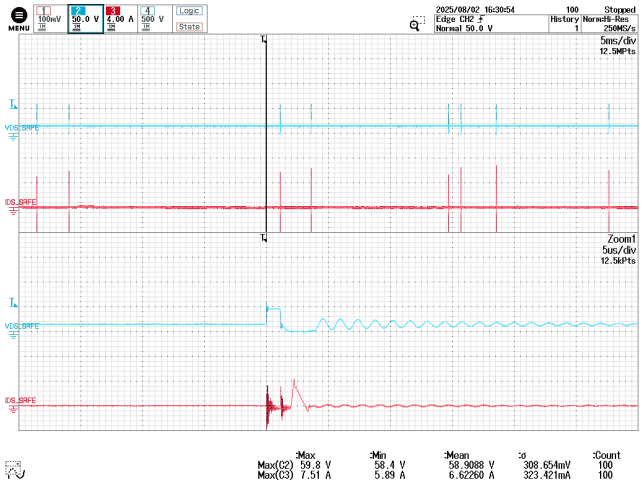


Figure 146 – SR FET Drain Voltage and Current.
400 VDC, No Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

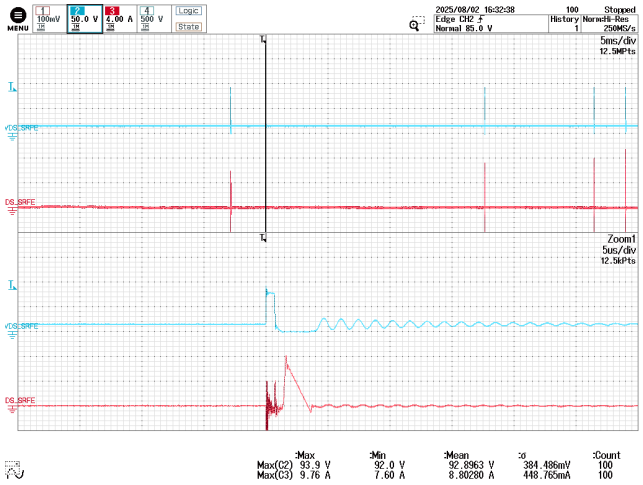


Figure 147 – SR FET Drain Voltage and Current.
800 VDC, No Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

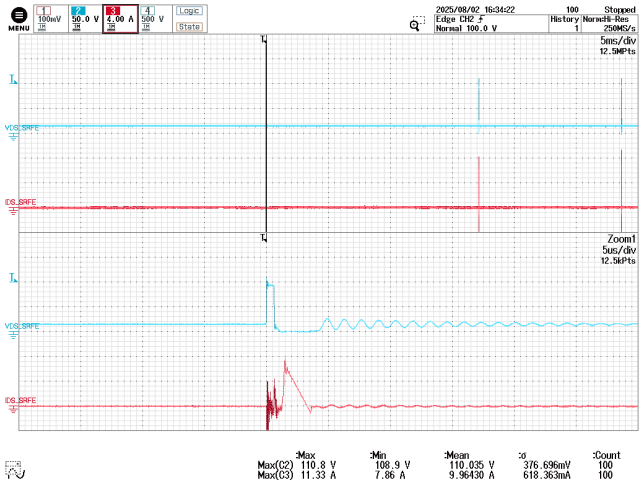


Figure 148 – SR FET Drain Voltage and Current.
1000 VDC, No Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

[52] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.2.2 Normal Operation Component Stress at 27 W Continuous Output

	Steady-State Switching Waveforms 25 ºC Ambient, Full Load					
Input	**INN3949CQ**			**SR FET**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[53]**	**V_{DS} (V)[54]**	**V_{STRESS} (%)**
80	1.86	404	23.8	27.1	24	16
400	1.90	711	41.8	26.9	61.4	40.9
800	2.03	1106	65.1	28.6	96	64
1000	2.13	1311	77.1	30	112	74.7

Table 15 – Summary of Critical Component Voltage Stresses at 25 ºC Ambient.

[53] SR FET current is the sum of Q1 and Q2 currents.
[54] SR FET voltage was taken from Q2.

12.2.2.2.1 InnoSwitch3-AQ Drain Voltage and Current at 25 ºC Ambient

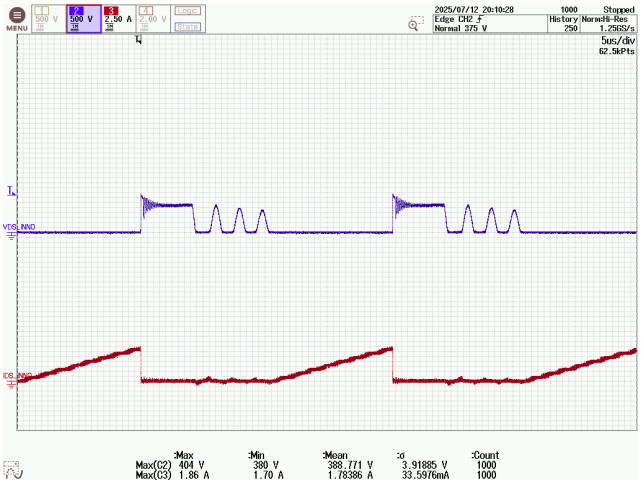


Figure 149 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 150 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 151 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

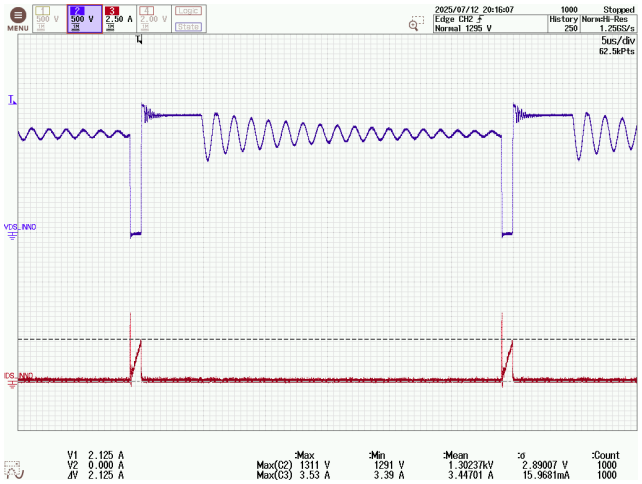


Figure 152 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

12.2.2.2.2 SR FET Drain Voltage and Current at 25 ºC Ambient[55]

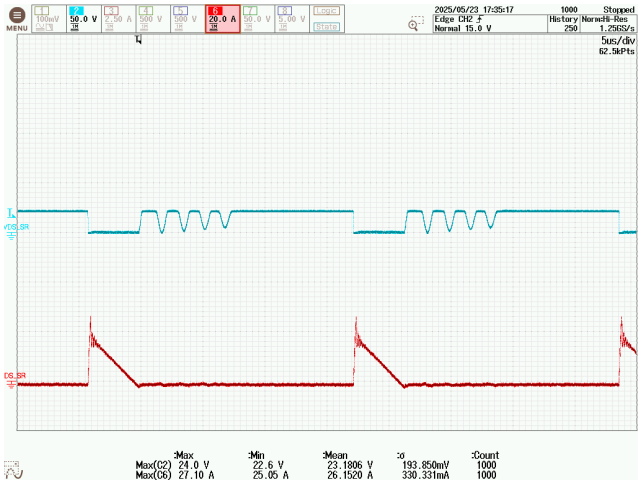


Figure 153 – SR FET Drain Voltage and Current.
80 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

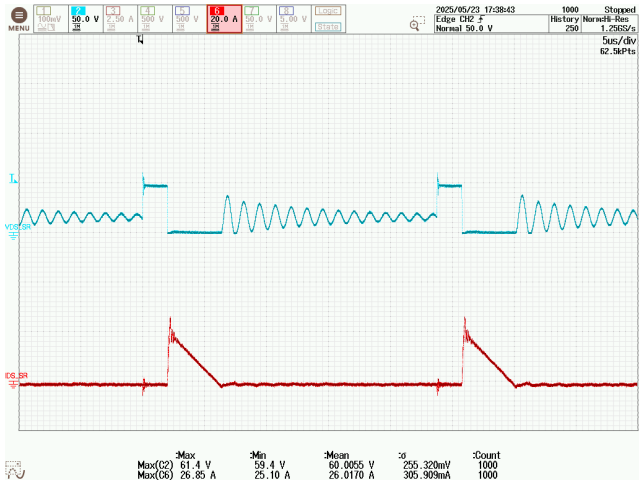


Figure 154 – SR FET Drain Voltage and Current.
400 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

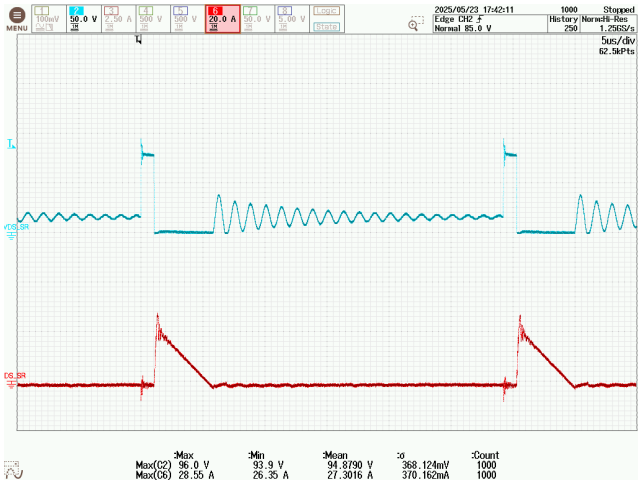


Figure 155 – SR FET Drain Voltage and Current.
800 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

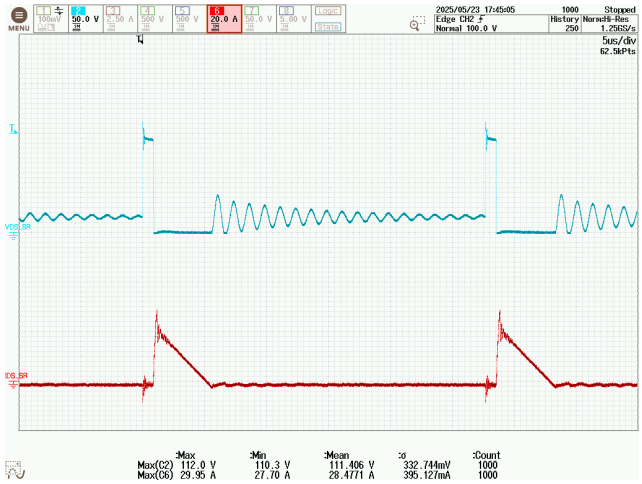


Figure 156 – SR FET Drain Voltage and Current.
1000 VDC, 1.8 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

[55] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.2.2.3 Short-Circuit Response

The unit was tested by applying an output short-circuit during normal working conditions and then removing the short-circuit to determine whether the unit will recover and operate normally. The expected response during short-circuit is for the unit to go to auto-restart (AR) mode and attempt to recover every 1.7 to 2.11 seconds.

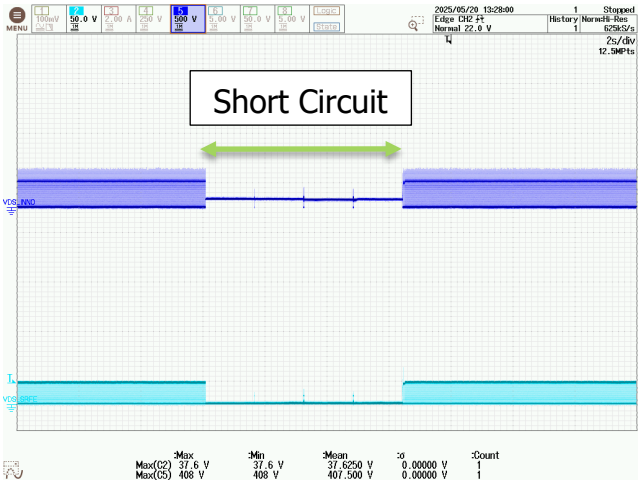


Figure 157 – InnoSwitch3-AQ and SR FET Drain Voltage.
80 VDC, 1.8 A-Short-1.8 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div.
Time: 2 s / div.

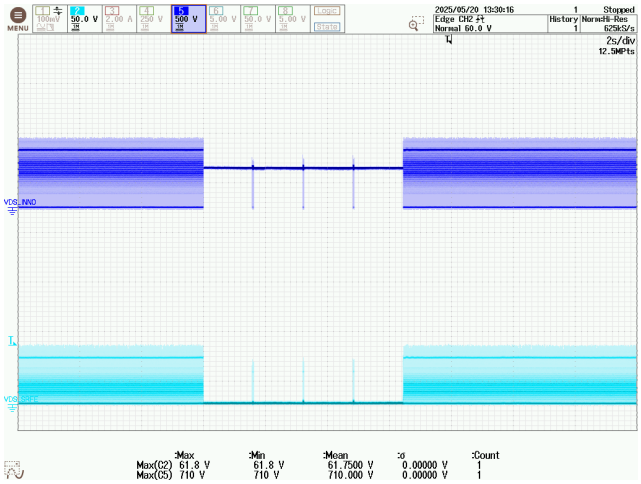


Figure 158 – InnoSwitch3-AQ and SR FET Drain Voltage.
400 VDC, 1.8 A-Short-1.8 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div
Time: 2 s / div.

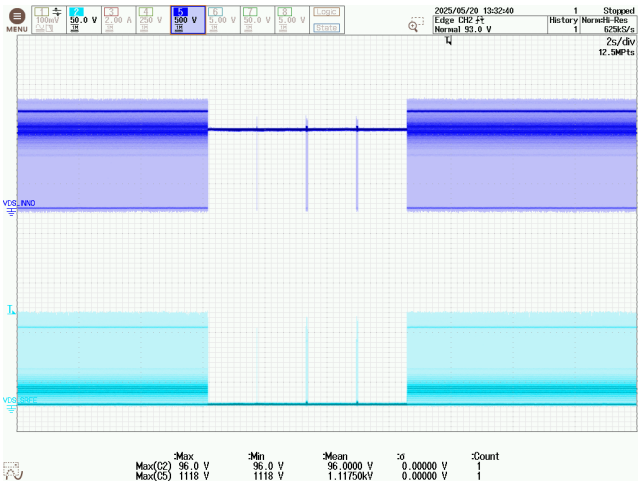


Figure 159 – InnoSwitch3-AQ and SR FET Drain voltage.
800 VDC, 1.8 A-Short-1.8 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div
Time: 2 s / div.

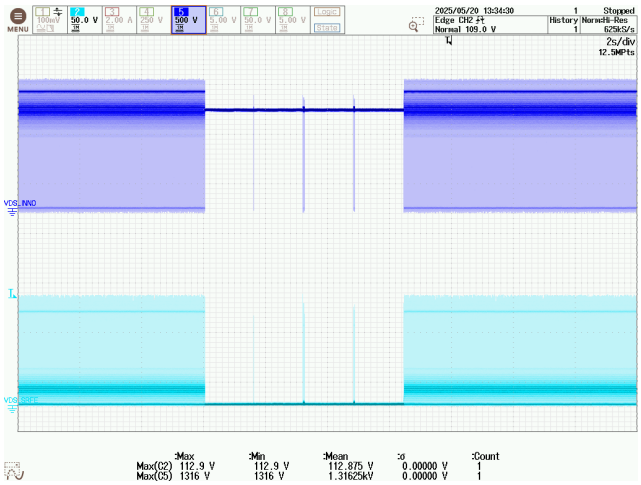


Figure 160 – InnoSwitch3-AQ and SR FET Drain voltage.
1000 VDC, 1.8 A-Short-1.8 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div
Time: 2 s / div.

12.2.2.3 Normal Operation Component Stress at 35 W Peak Output

	Steady-State Switching Waveforms 25 ºC Ambient, Peak Load					
Input	**INN3949CQ**			**SR MOSFETs**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[56]**	**V_{DS} (V)[57]**	**V_{STRESS} (%)**
80	1.93	413	24.3	28	23.5	15.7
400	1.95	726	42.7	28.8	61.5	41
800	2.13	1126	66.2	30.4	95.9	63.9
1000	2.20	1326	78	31.2	112	74.7

Table 16 – Summary of Critical Component Voltage Stresses at 25 ºC Ambient.

[56] SR FET current is the sum of Q1 and Q2 currents.
[57] SR FET voltage was taken from Q2.

12.2.2.3.1 InnoSwitch3-AQ Drain Voltage and Current at 25 ºC Ambient

Figure 161 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 162 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

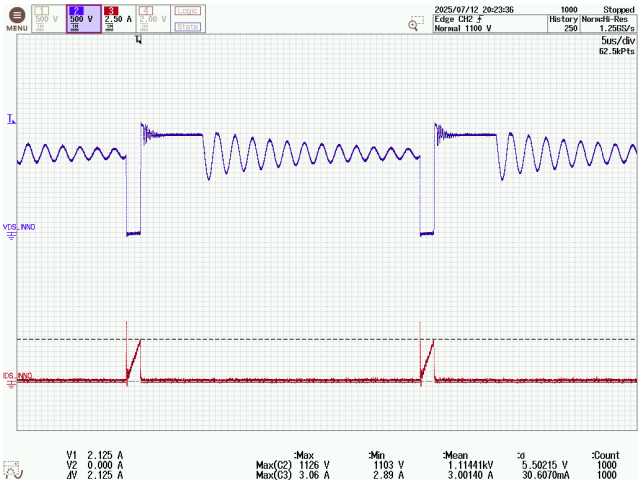


Figure 163 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 164 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

12.2.2.3.2 SR FET Drain Voltage and Current at 25 ºC Ambient[58]

Figure 165 – SR FET Drain Voltage and Current.
80 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

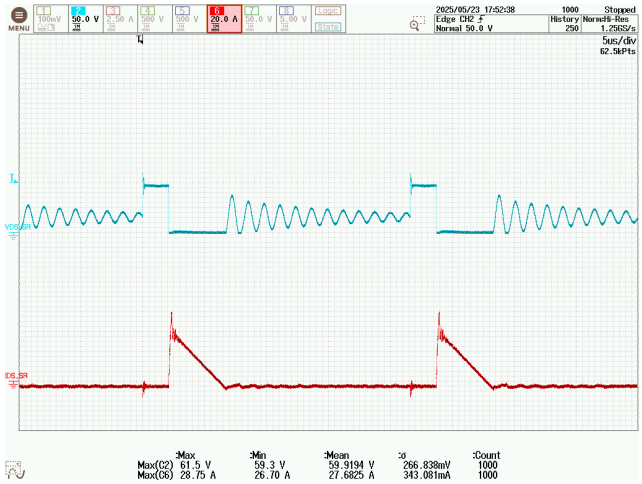


Figure 166 – SR FET Drain Voltage and Current.
400 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

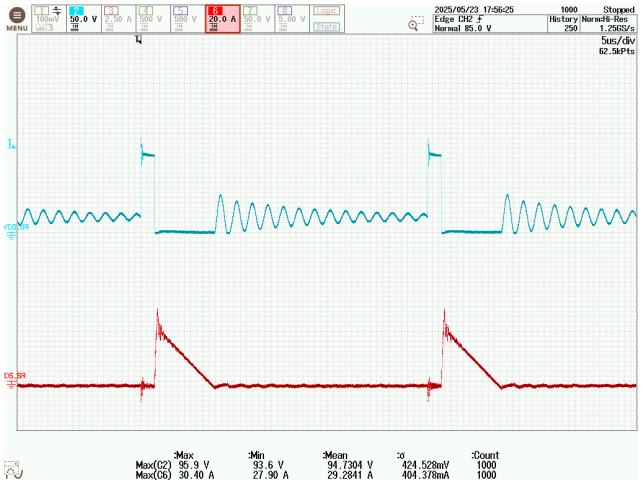


Figure 167 – SR FET Drain Voltage and Current.
800 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

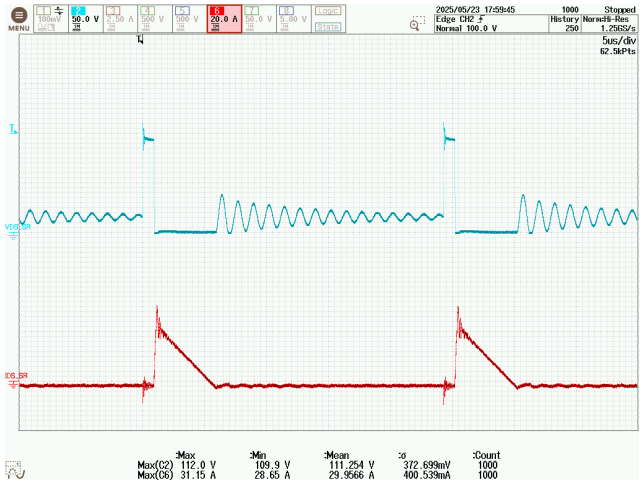


Figure 168 – SR FET Drain Voltage and Current.
1000 VDC, 2.33 A Load, 25 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH6: $I_{D(SR)}$, 20 A / div.
Time: 5 µs / div.

[58] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.2.3.3 Short-Circuit Response

The unit was tested by applying an output short-circuit during normal working conditions and then removing the short-circuit to determine whether the unit will recover and operate normally. The expected response during short-circuit is for the unit to go to auto-restart (AR) mode and attempt to recover every 1.7 to 2.11 seconds.

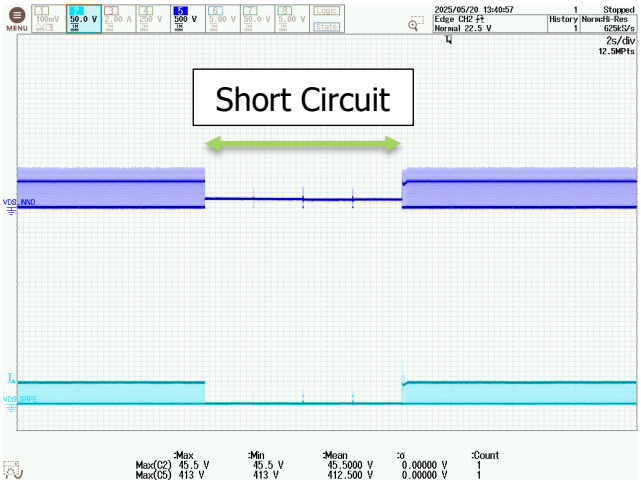


Figure 169 – InnoSwitch3-AQ and SR FET Drain Voltage. 80 VDC, 2.333 A-Short-2.333 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div
Time: 2 s / div.

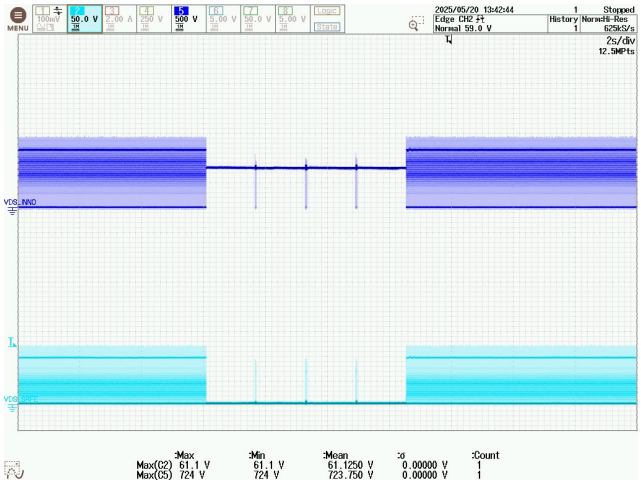


Figure 170 – InnoSwitch3-AQ and SR FET Drain Voltage. 400 VDC, 2.333 A-Short-2.333 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div
Time: 2 s / div.

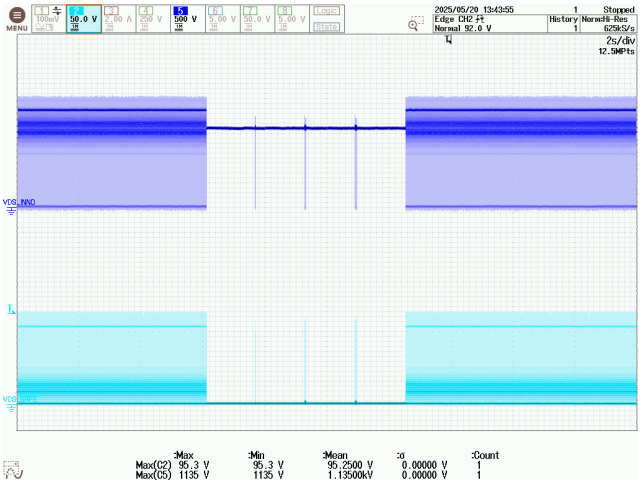


Figure 171 – InnoSwitch3-AQ and SR FET Drain voltage. 800 VDC, 2.333 A-Short-2.333 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div
Time: 2 s / div.

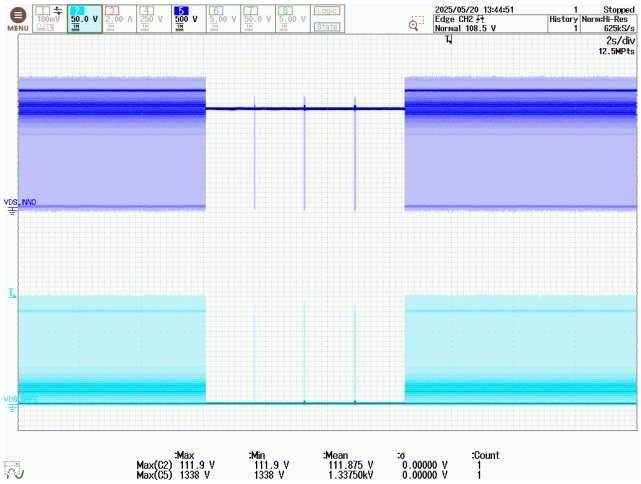


Figure 172 – InnoSwitch3-AQ and SR FET Drain voltage. 1000 VDC, 2.333 A-Short-2.333 A, 25 ºC Ambient.
CH2: $V_{DS(Q2)}$, 50 V / div.
CH5: $V_{DS(IC1)}$, 500 V / div
Time: 2 s / div.

12.2.3 Switching Waveforms at -40 ºC Ambient

12.2.3.1 Normal Operation Component Stress at No Load

	Steady-State Switching Waveforms -40 ºC Ambient, No Load					
Input	**INN3949CQ**			**SR FET**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[59]**	**V_{DS} (V)[60]**	**V_{STRESS} (%)**
80	0.74	306	18	4.61	25	16.7
400	0.91	630	37.1	6.91	60.8	40.5
800	1.08	1039	61.1	9.35	95.9	63.9
1000	1.18	1239	72.9	10.5	114	75.9

Table 17 – Summary of Voltage Stress on Critical Component at -40 ºC Ambient.

[59] SR FET current is the sum of Q1 and Q2 currents.
[60] SR FET voltage was taken from Q2.

12.2.3.1.1 InnoSwitch3-AQ Drain Voltage and Current at -40 ºC Ambient

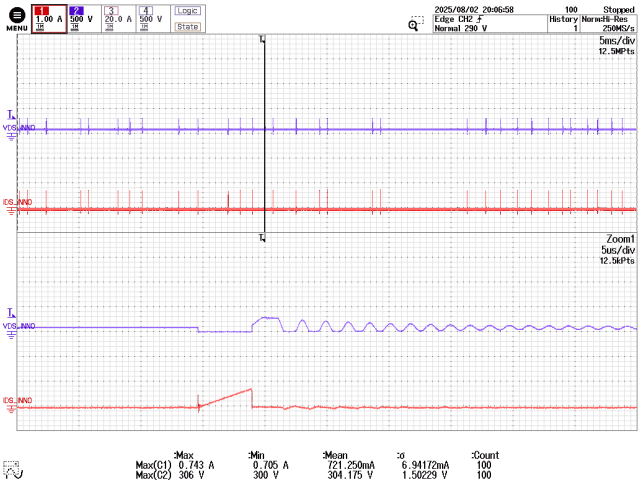


Figure 173 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, No Load, -40 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

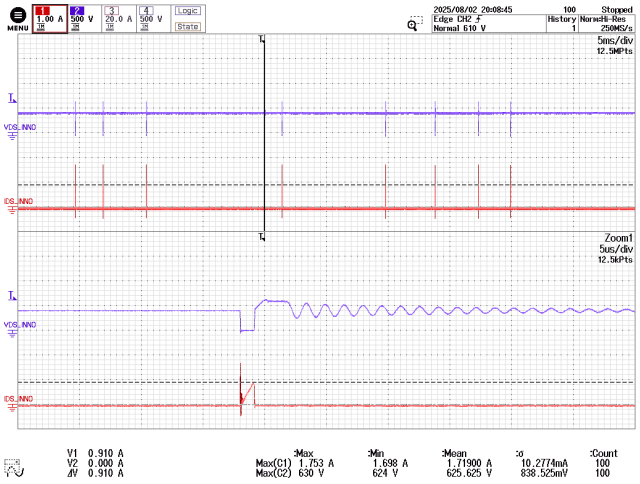


Figure 174 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, No Load, -40 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

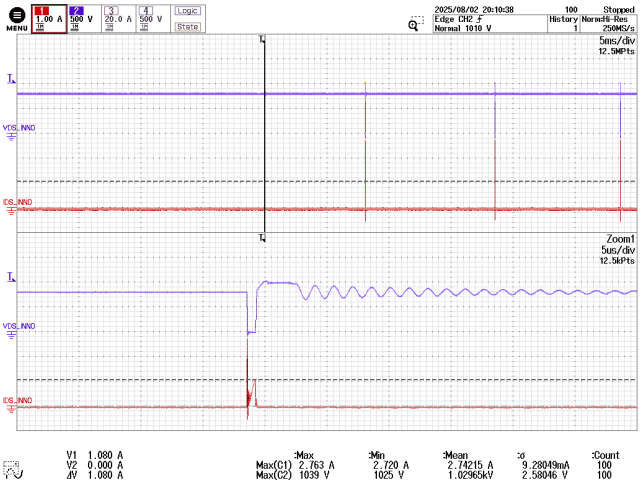


Figure 175 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, No Load, -40 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

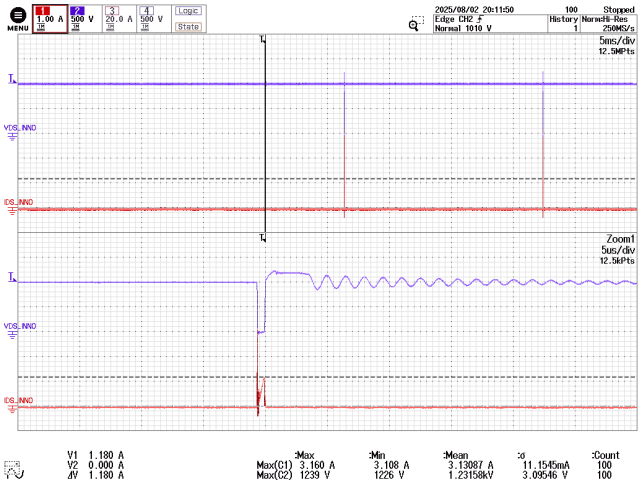


Figure 176 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, No Load, -40 ºC Ambient.
CH1: $I_{D(IC1)}$, 1 A / div.
CH2: $V_{DS(IC1)}$, 500 V / div.
Time: 5 ms / div.

12.2.3.1.2 SR FET Drain Voltage and Current at -40 ºC Ambient[61]

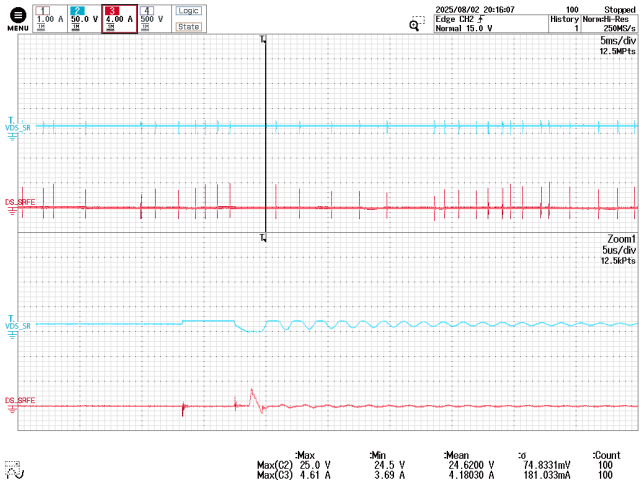


Figure 177 – SR FET Drain Voltage and Current.
80 VDC, No Load, -40 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

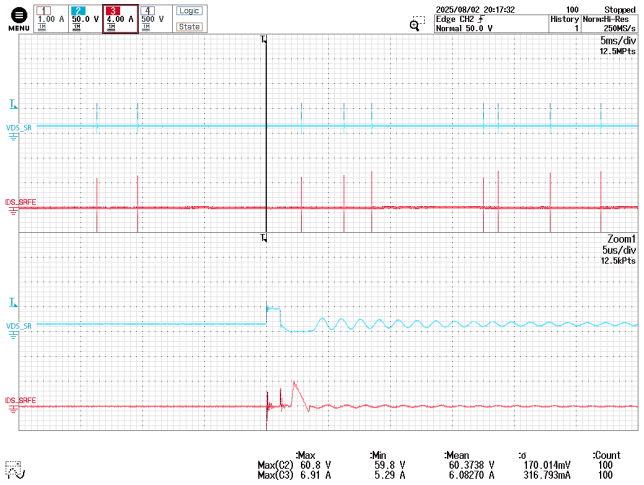


Figure 178 – SR FET Drain Voltage and Current.
400 VDC, No Load, -40 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

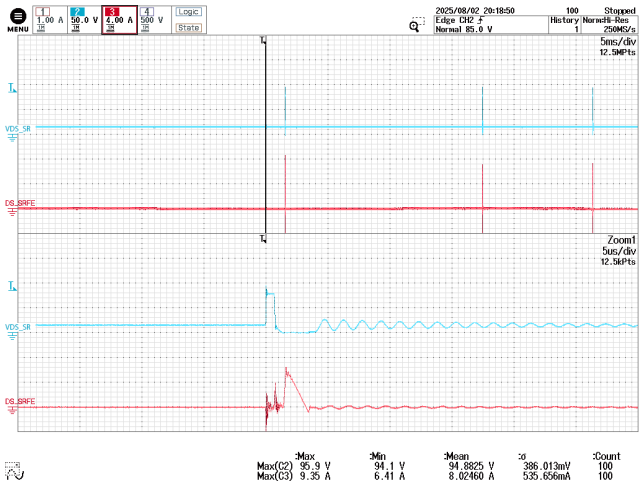


Figure 179 – SR FET Drain Voltage and Current.
800 VDC, No Load, -40 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

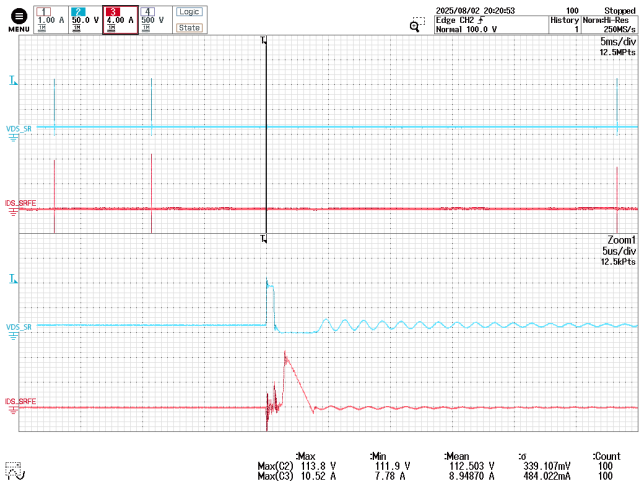


Figure 180 – SR FET Drain Voltage and Current.
1000 VDC, No Load, -40 ºC Ambient.
CH2: $V_{DS(SR)}$, 50 V / div.
CH3: $I_{D(SR)}$, 4 A / div.
Time: 5 ms / div.

[61] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.3.2 Normal Operation Component Stress at 27 W Continuous Output

	Steady-State Switching Waveforms -40 ºC Ambient, Full Load					
Input	**INN3949CQ**			**SR FET**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[62]**	**V_{DS} (V)[63]**	**V_{STRESS} (%)**
80	1.91	440	25.9	24.8	23.1	15.4
400	1.95	744	43.8	26.35	60.4	40.3
800	2.10	1155	67.9	27.9	96	64
1000	2.13	1365	80.3	29.3	112.6	75.1

Table 18 – Summary of Voltage Stress on Critical Component at -40 ºC Ambient.

[62] SR FET current is the sum of Q1 and Q2 currents.
[63] SR FET voltage was taken from Q2.

12.2.3.2.1 InnoSwitch3-AQ Drain Voltage and Current at -40 ºC Ambient

Figure 181 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, 1.8 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

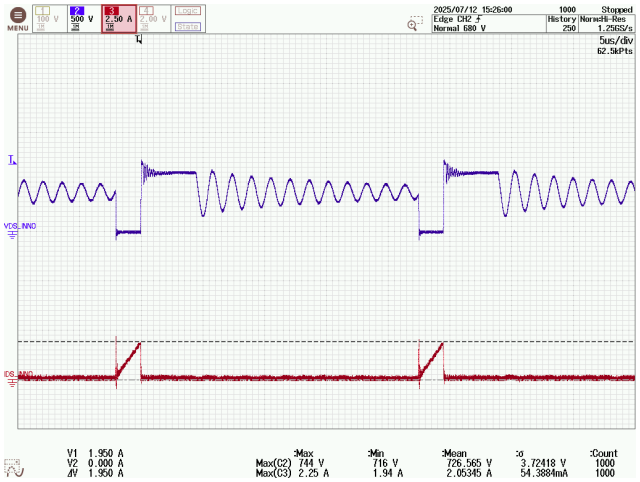


Figure 182 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 1.8 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 183 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, 1.8 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 184 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 1.8 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

12.2.3.2.2 SR FET Drain Voltage and Current at -40 ºC Ambient[64]

Figure 185 – SR FET Drain Voltage and Current.
80 VDC, 1.8 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

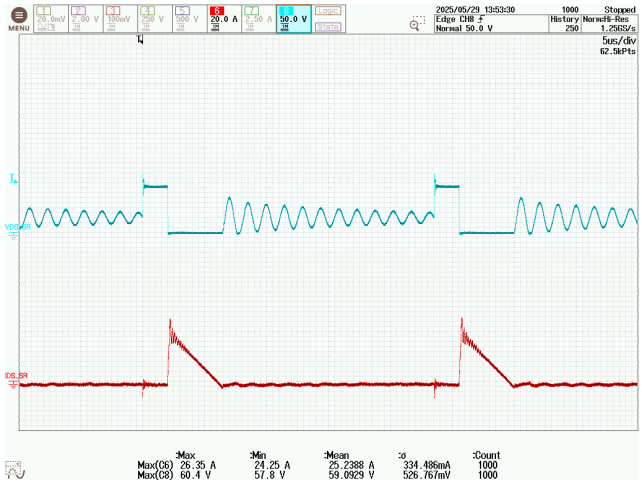


Figure 186 – SR FET Drain Voltage and Current.
400 VDC, 1.8 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

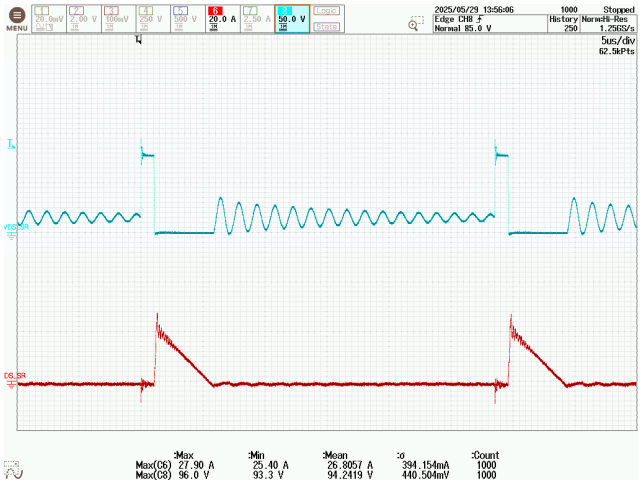


Figure 187 – SR FET Drain Voltage and Current.
800 VDC, 1.8 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

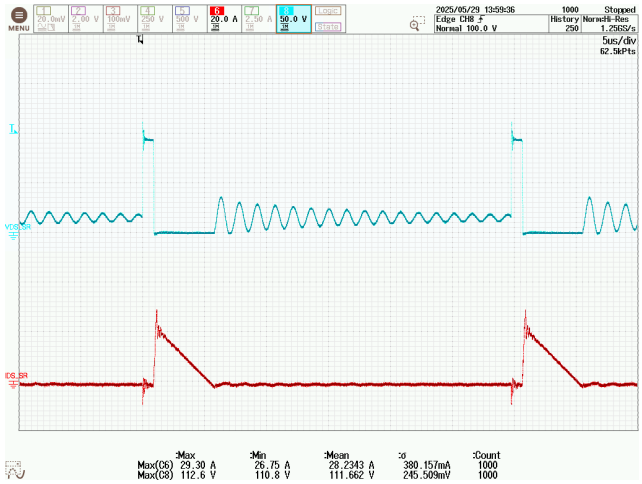


Figure 188 – SR FET Drain Voltage and Current.
1000 VDC, 1.8 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

[64] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.2.3.3 Normal Operation Component Stress at 35 W Peak Output

	Steady-State Switching Waveforms -40 ºC Ambient, Peak Load					
Input	**INN3949CQ**			**SR MOSFETs**		
V_{IN} (V)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)[65]**	**V_{DS} (V)[66]**	**V_{STRESS} (%)**
80	2.03	456	26.8	27.35	23.8	15.9
400	2.10	766	45.1	27.00	60.5	40.3
800	2.13	1163	68.4	28.55	96.0	64.0
1000	2.15	1383	81.4	29.40	112.1	74.7

Table 19 – Summary of Voltage Stress on Critical Component at -40 ºC Ambient.

[65] SR FET current is the sum of Q1 and Q2 currents.
[66] SR FET voltage was taken from Q2.

12.2.3.3.1 InnoSwitch3-AQ Drain Voltage and Current at -40 ºC Ambient

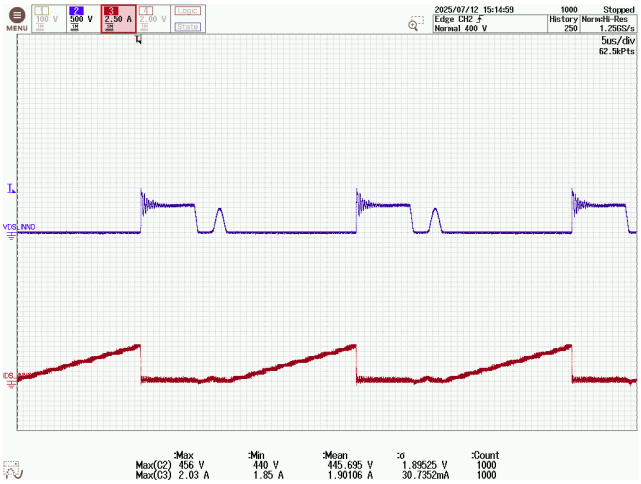


Figure 189 – InnoSwitch3-AQ Drain Voltage and Current.
80 VDC, 2.33 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

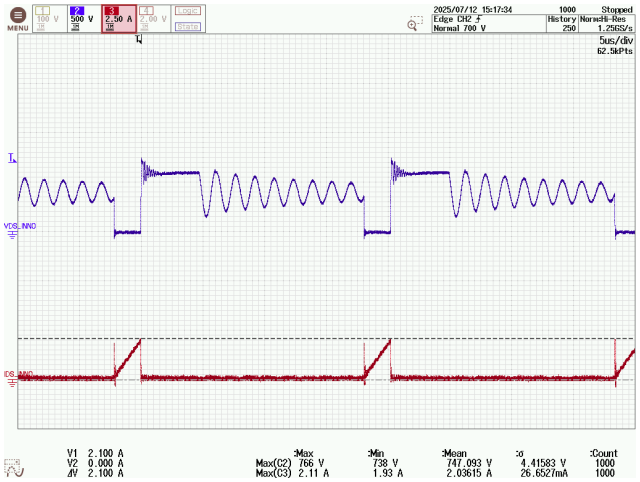


Figure 190 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 2.33 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 191 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, 2.33 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 192 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 2.33 A Load, -40 ºC Ambient.
CH2: $V_{DS(IC1)}$, 500 V / div.
CH3: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

12.2.3.3.2 SR FET Drain Voltage and Current at -40 ºC Ambient[67]

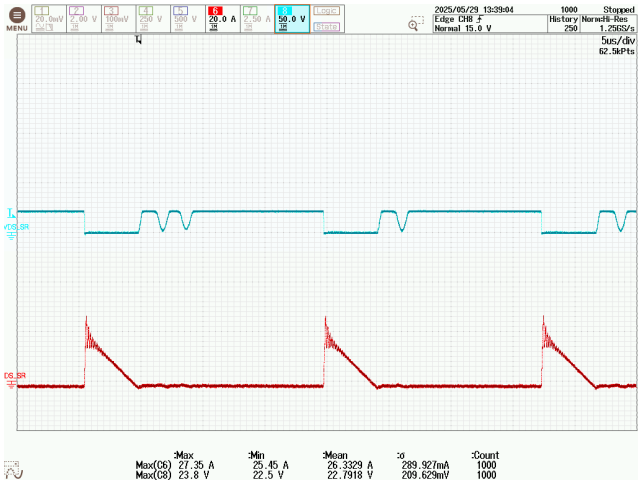


Figure 193 – SR FET Drain Voltage and Current.
80 VDC, 2.33 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

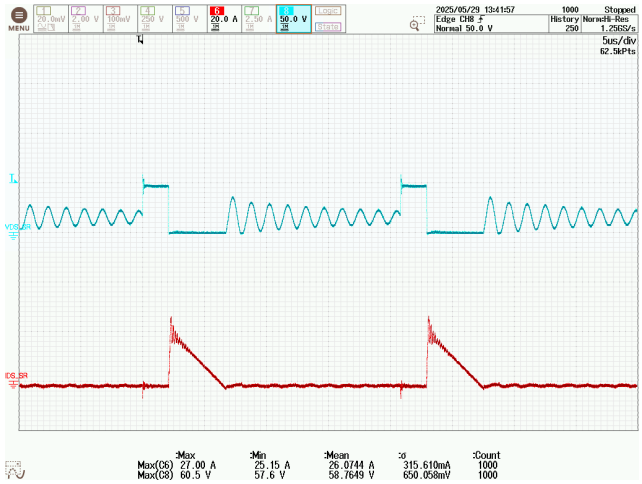


Figure 194 – SR FET Drain Voltage and Current.
400 VDC, 2.33 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

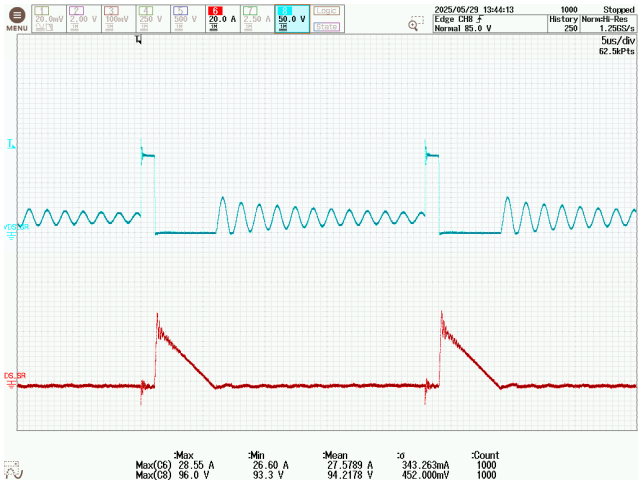


Figure 195 – SR FET Drain Voltage and Current.
800 VDC, 2.33 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

Figure 196 – SR FET Drain Voltage and Current.
1000 VDC, 2.33 A Load, -40 ºC Ambient.
CH6: $I_{D(SR)}$, 20 A / div.
CH8: $V_{DS(SR)}$, 50 V / div.
Time: 5 µs / div.

[67] Current waveforms were measured using a 120 A_{peak} Rogowski Coil.

12.3 Load Transient Response

Output voltage waveforms were captured under a dynamic load-transient from 0% to 50% and 50% to 100%. The time duration for the load at each state was set to 100 ms with a load slew rate of 100 mA / µs. The test was performed at 85 ºC ambient.

Dynamic Load Settings	V_{IN} (VDC)	ΔV_{OUT} (V)	$V_{OUT(Overshoot)}$ (V)	$V_{OUT(Undershoot)}$ (V)
0% - 50% - 0% (0 A – 0.9 A – 0 A)	80	0.290	0.117	-0.201
	400	0.260	0.121	-0.173
	800	0.310	0.152	-0.191
	1000	0.337	0.173	-0.175
50% - 100% - 50% (0.9 A – 1.8 A – 0.9 A)	80	0.294	0.168	-0.131
	400	0.292	0.161	-0.141
	800	0.369	0.210	-0.192
	1000	0.422	0.220	-0.222

Table 20 – Load Transient Response.

12.3.1 Output Voltage Ripple with 0% to 50% Transient Load at 85 ºC Ambient

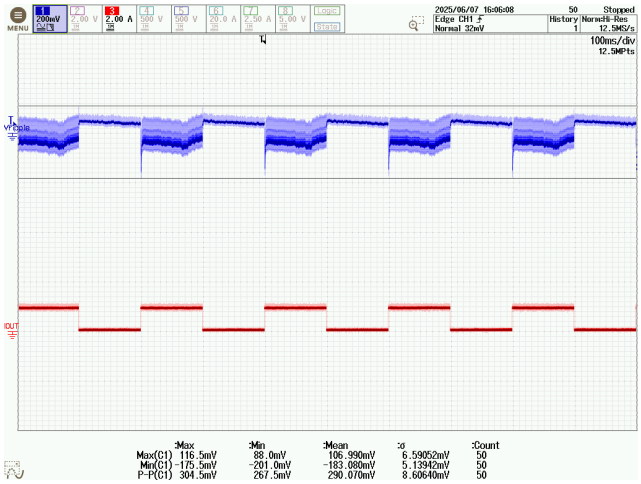


Figure 197 – Output Voltage and Current.
80 VDC,
0 A – 0.9 A – 0 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 290 mV.

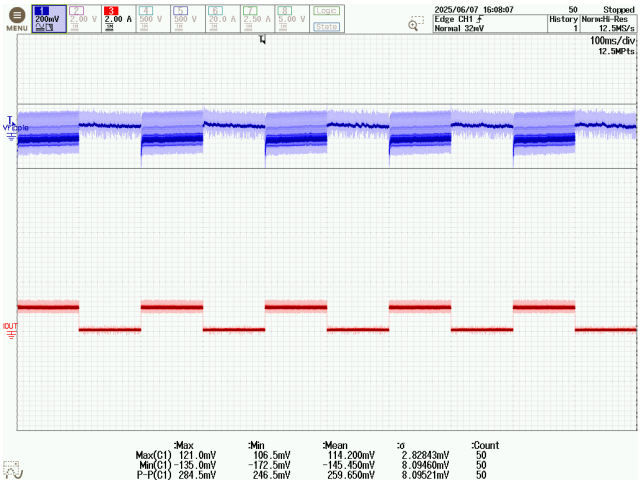


Figure 198 – Output Voltage and Current.
400 VDC,
0 A – 0.9 A – 0 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 260 mV.

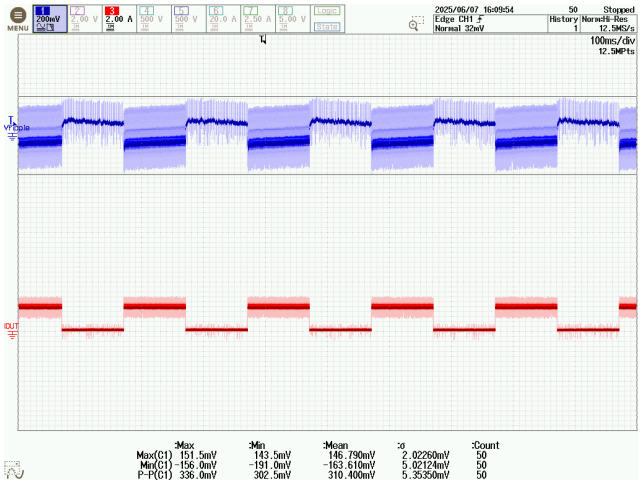


Figure 199 – Output Voltage and Current.
800 VDC,
0 A – 0.9 A – 0 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 310 mV.

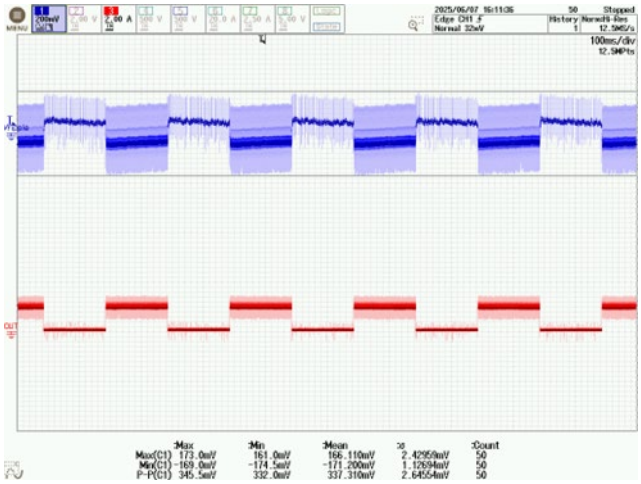


Figure 200 – Output Voltage and Current.
1000 VDC,
0 A – 0.9 A – 0 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 337 mV.

12.3.2 Output Voltage Ripple with 50% to 100% Transient Load at 85 ºC Ambient

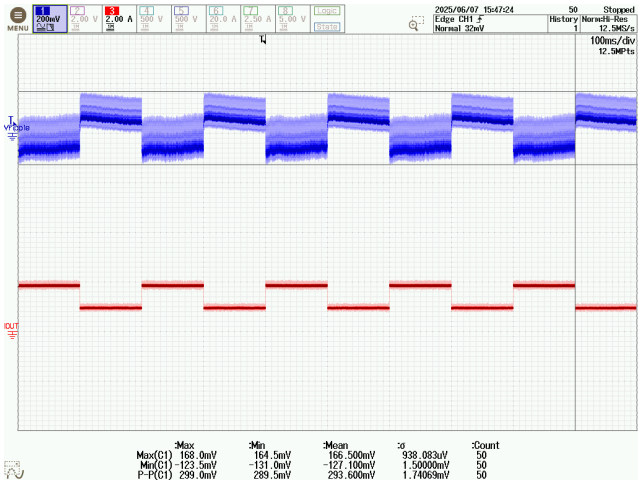


Figure 201 – Output Voltage and Current.
80 VDC,
0.9 A – 1.8 A – 0.9 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 294 mV.

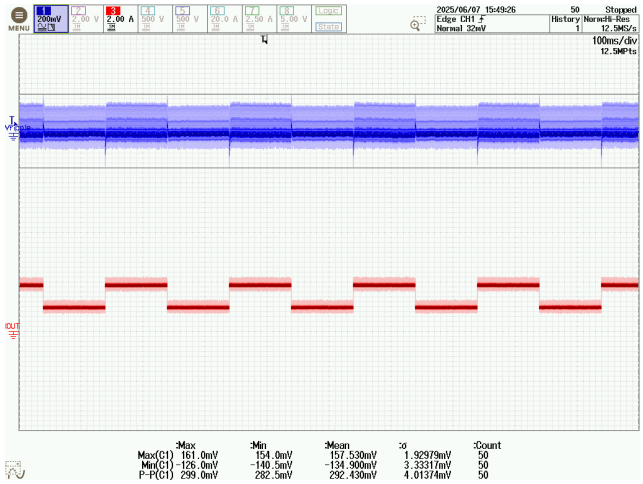


Figure 202 – Output Voltage and Current.
400 VDC,
0.9 A – 1.8 A – 0.9 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 292 mV.

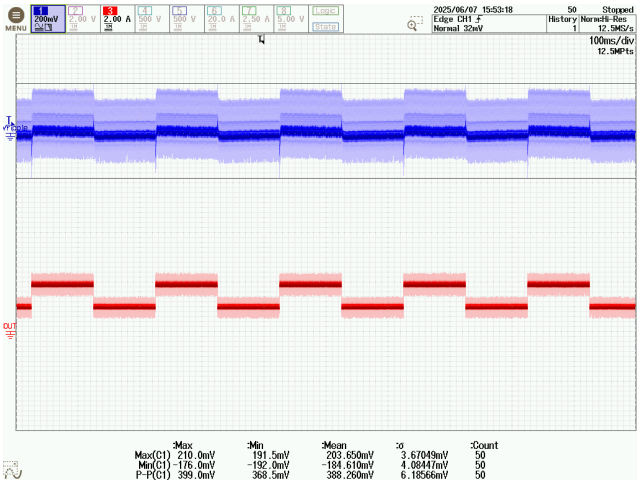


Figure 203 – Output Voltage and Current.
800 VDC,
0.9 A – 1.8 A – 0.9 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 369 mV.

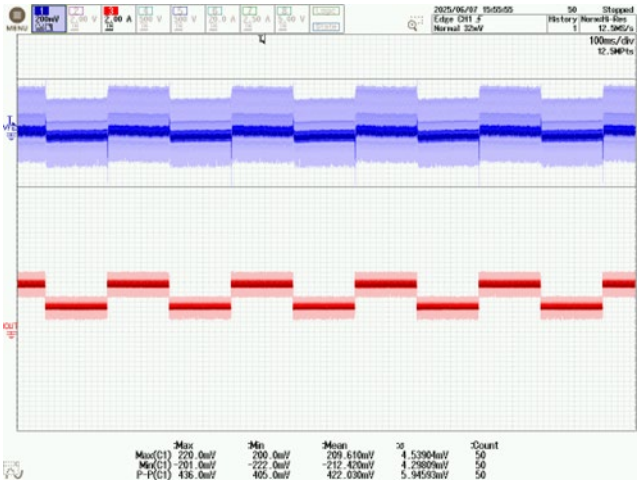


Figure 204 – Output Voltage and Current.
1000 VDC,
0.9 A – 1.8 A – 0.9 A Transient Load,
85 ºC Ambient.
CH1: V_{OUT}, 200 mV / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.
ΔV = 422 mV.

12.4 Output Ripple Measurements

12.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to eliminate spurious signals due to pick-up. Details of the probe modification were provided in Figure 205 and Figure 206 below.

A 1 µF / 50 V ceramic capacitor was attached in parallel across the probe tip of a CT2708 probe adapter. A twisted pair of wires, kept as short as possible, were then soldered directly between the probe and the output terminals of the unit under test.

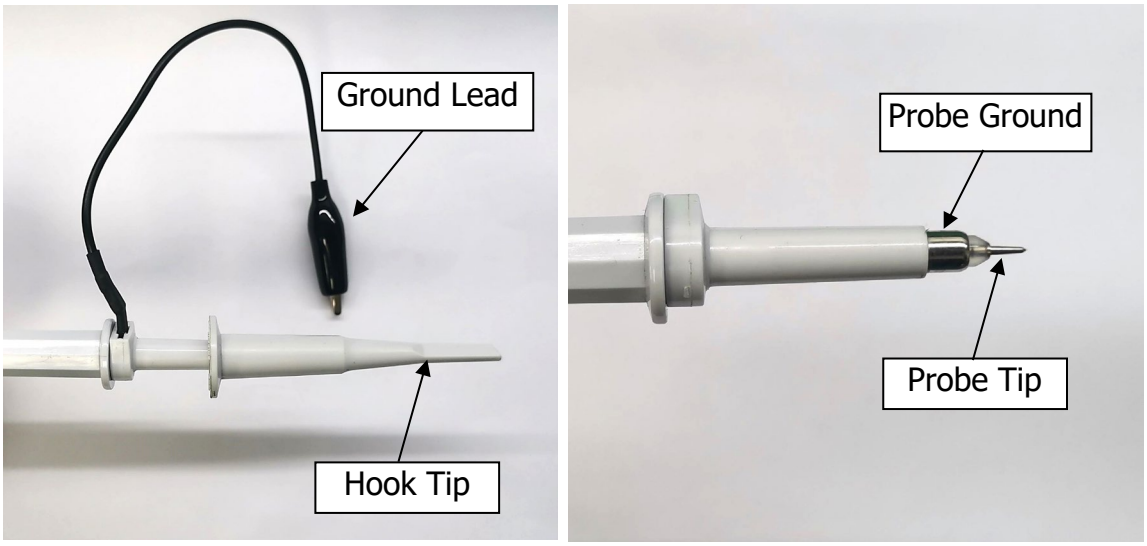


Figure 205 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

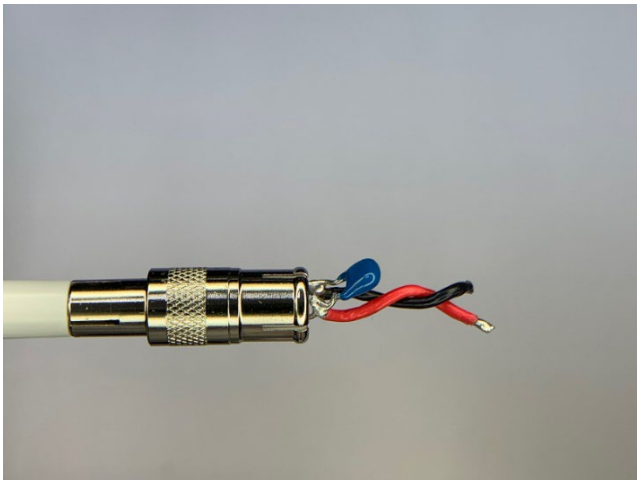


Figure 206 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement, and a Parallel Decoupling Capacitor Added.)

12.4.2 Output Voltage Ripple Waveforms

The output voltage ripple waveform was recorded at the output terminals at full load using the ripple measurement probe with decoupling capacitor.

12.4.2.1 Output Voltage Ripple at 85 ºC Ambient with Constant Full Load[68]

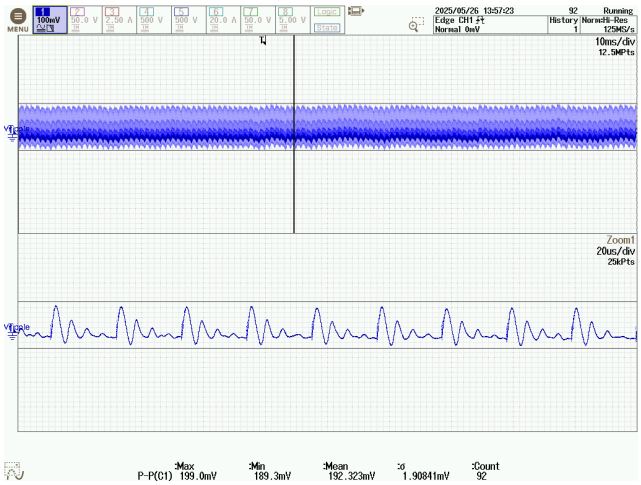


Figure 207 – Output Voltage Ripple.
80 VDC, 1.8 A, 85 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 192 mV.

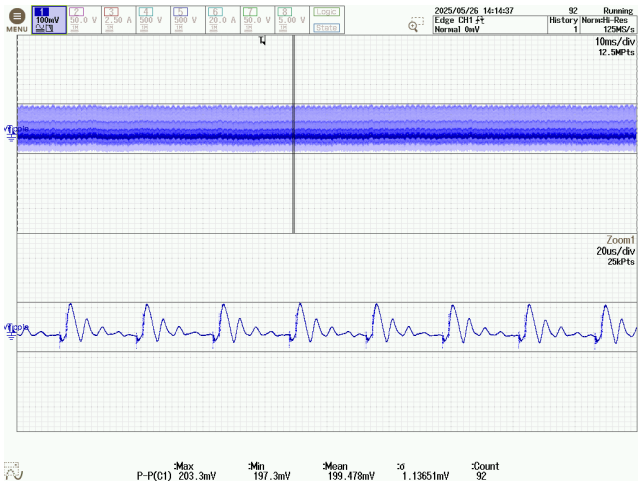


Figure 208 – Output Voltage Ripple.
400 VDC, 1.8 A, 85 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 199 mV.

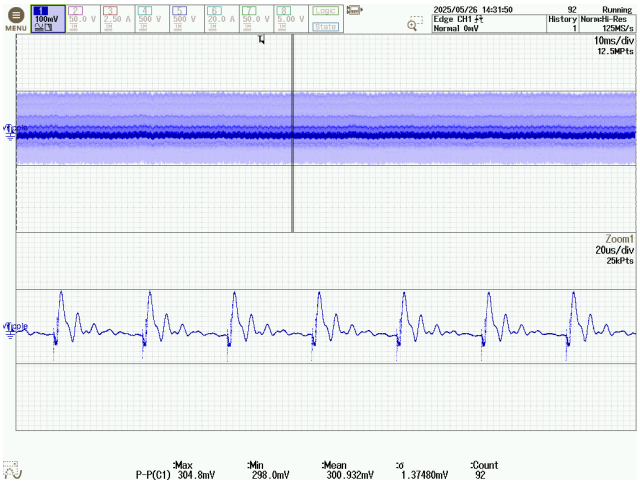


Figure 209 – Output Voltage Ripple.
800 VDC, 1.8 A, 85 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 301 mV.

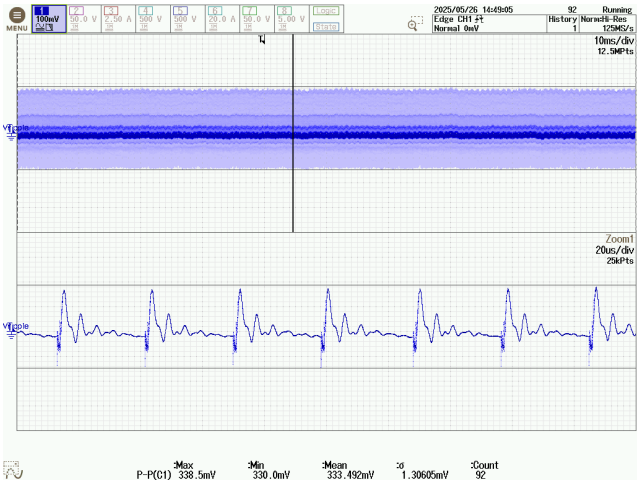


Figure 210 – Output Voltage Ripple.
1000 VDC, 1.8 A, 85 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 333 mV.

[68] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.4.2.2 Output Voltage Ripple at 25 ºC Ambient with Constant Full Load[69]

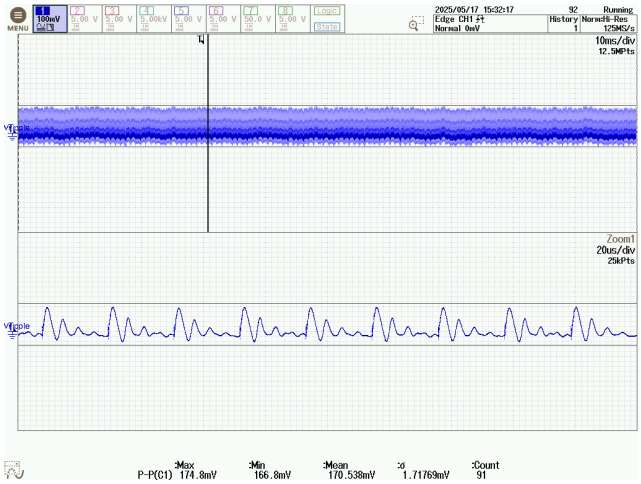


Figure 211 – Output Voltage Ripple.
80 VDC, 1.8 A, 25 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 171 mV.

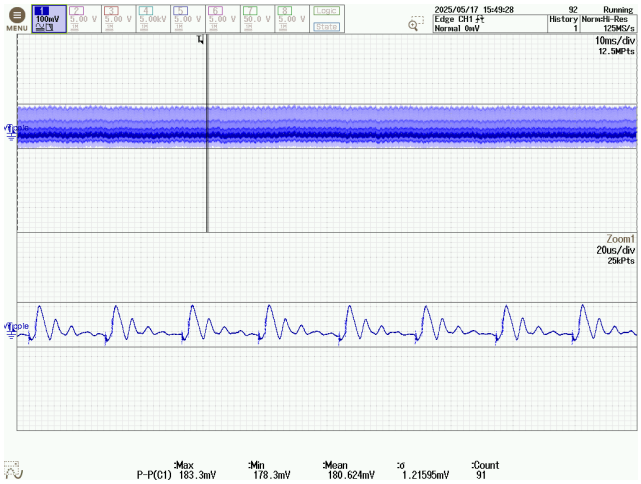


Figure 212 – Output Voltage Ripple.
400 VDC, 1.8 A, 25 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 181 mV.

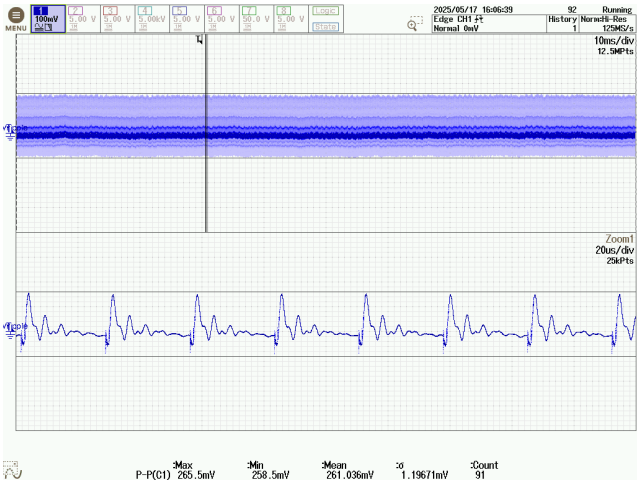


Figure 213 – Output Voltage Ripple.
800 VDC, 1.8 A, 25 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 261 mV.

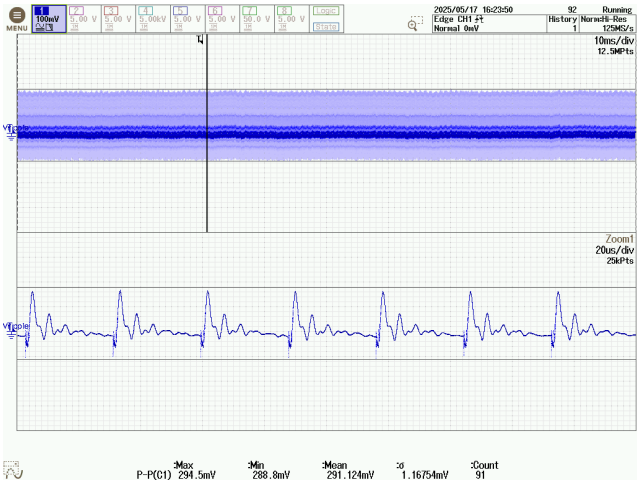


Figure 214 – Output Voltage Ripple.
1000 VDC, 1.8 A, 25 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 291 mV.

[69] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.4.2.3 Output Voltage Ripple at -40 ºC Ambient with Constant Full Load[70]

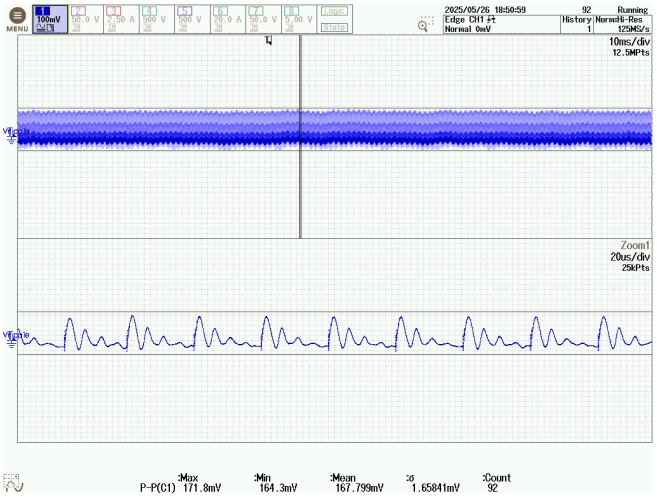


Figure 215 – Output Voltage Ripple.
80 VDC, 1.8 A, -40 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 168 mV.

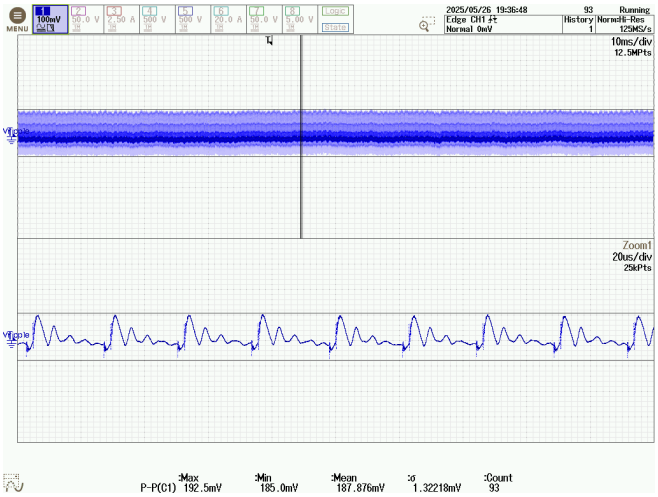


Figure 216 – Output Voltage Ripple.
400 VDC, 1.8 A, -40 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 188 mV.

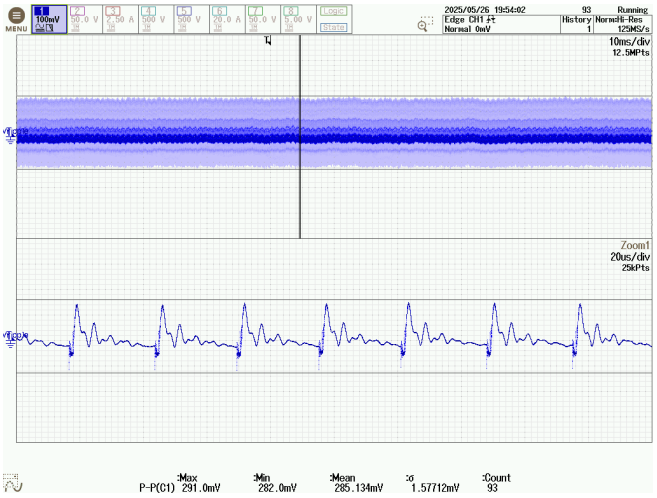


Figure 217 – Output Voltage Ripple.
800 VDC, 1.8 A, -40 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 285 mV.

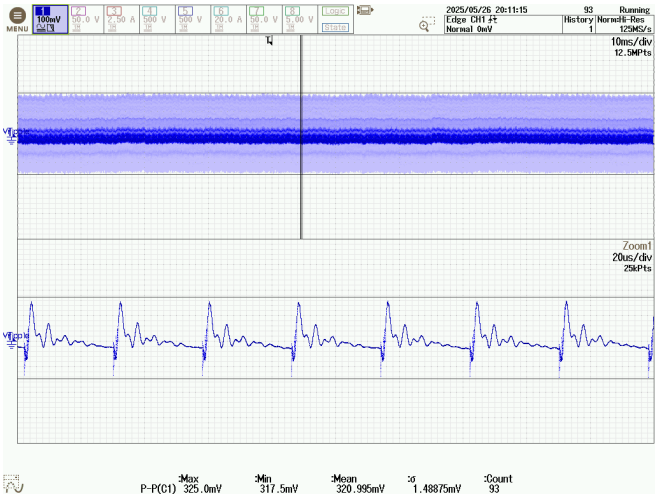


Figure 218 – Output Voltage Ripple.
1000 VDC, 1.8 A, -40 ºC Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 321 mV.

[70] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.4.3 Output Ripple vs. Load

12.4.3.1 Output Ripple at 85 ºC Ambient

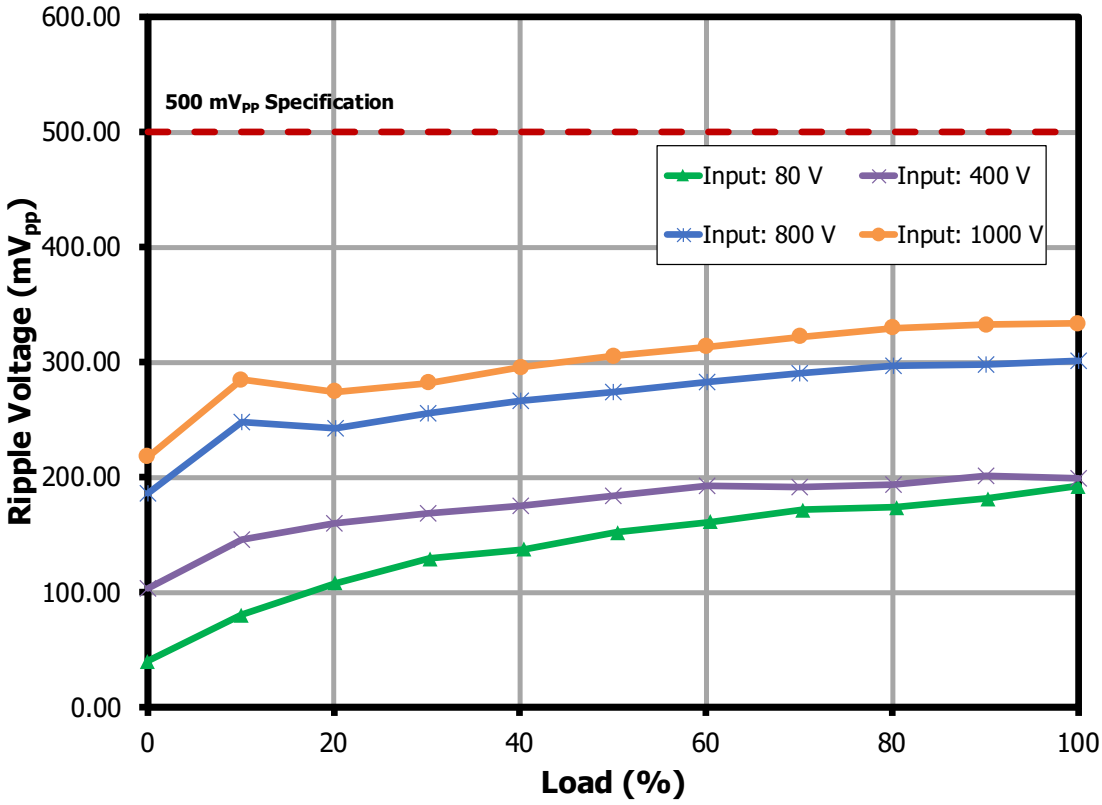


Figure 219 – Output Ripple Voltage Across Full Load Range (85 ºC Ambient).

12.4.3.2 Output Ripple at 25 ºC Ambient

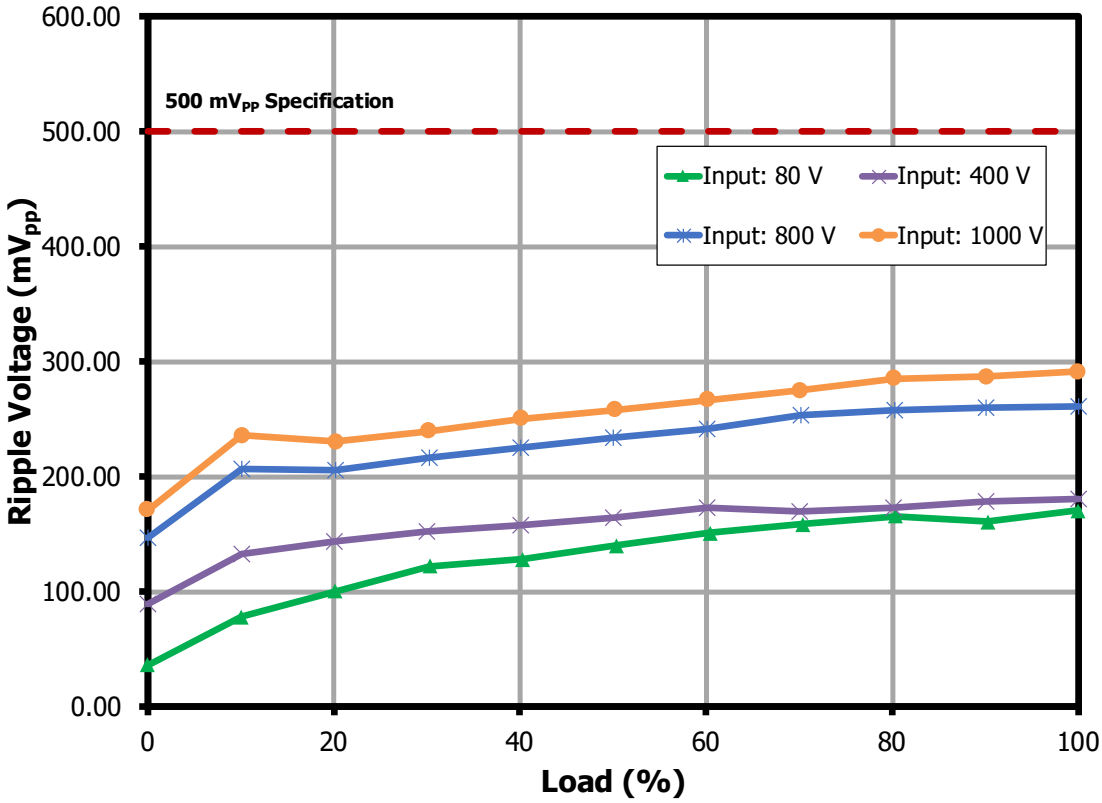


Figure 220 – Output Ripple Voltage Across Full Load Range (25 ºC Ambient).

12.4.3.3 Output Ripple at -40 ºC Ambient

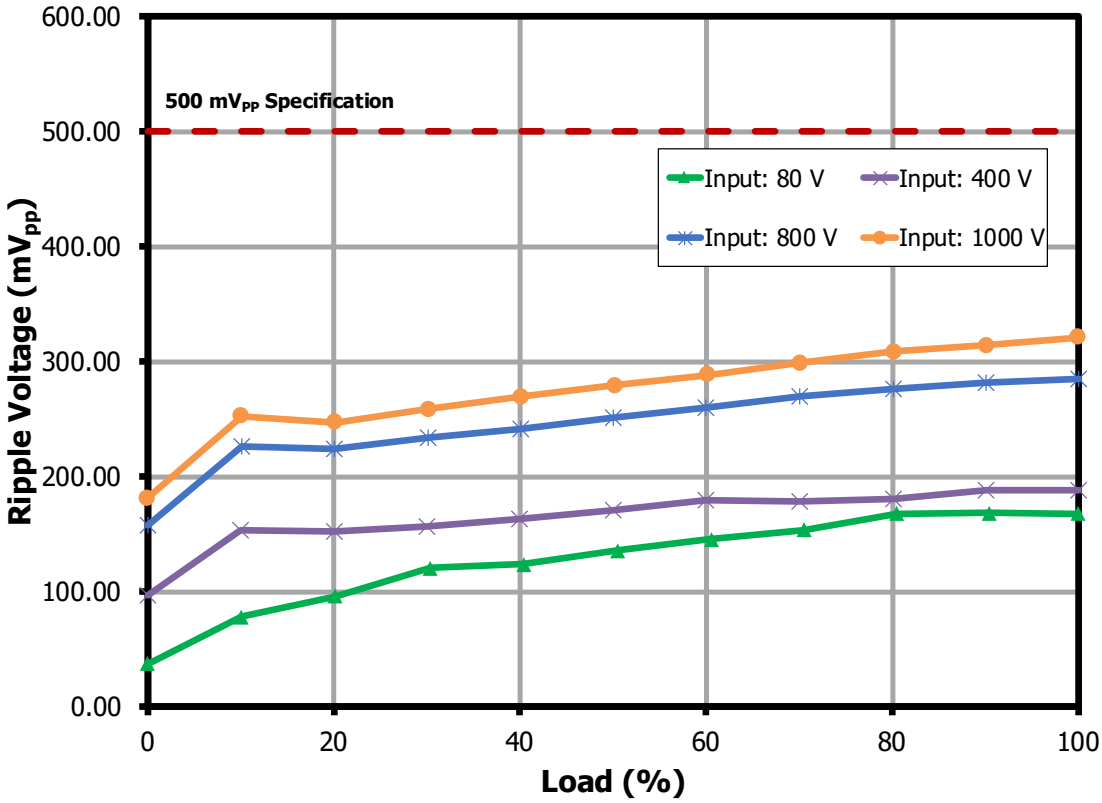


Figure 221 – Output Ripple Voltage Across Full Load Range (-40 ºC Ambient).

13 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before turning on the unit under test. The unit was also allowed to stabilize for 20 minutes after each change in input voltage. Output voltage and output current measurements were taken 60 seconds after every change in loading condition.

Since the unit was designed for 27 W continuous power, operating beyond 2.33 A load might trigger overtemperature protection (OTP) before output overload is reached. A 1-minute cooling time at no-load after each change in loading condition was added to the test sequence to prevent this.

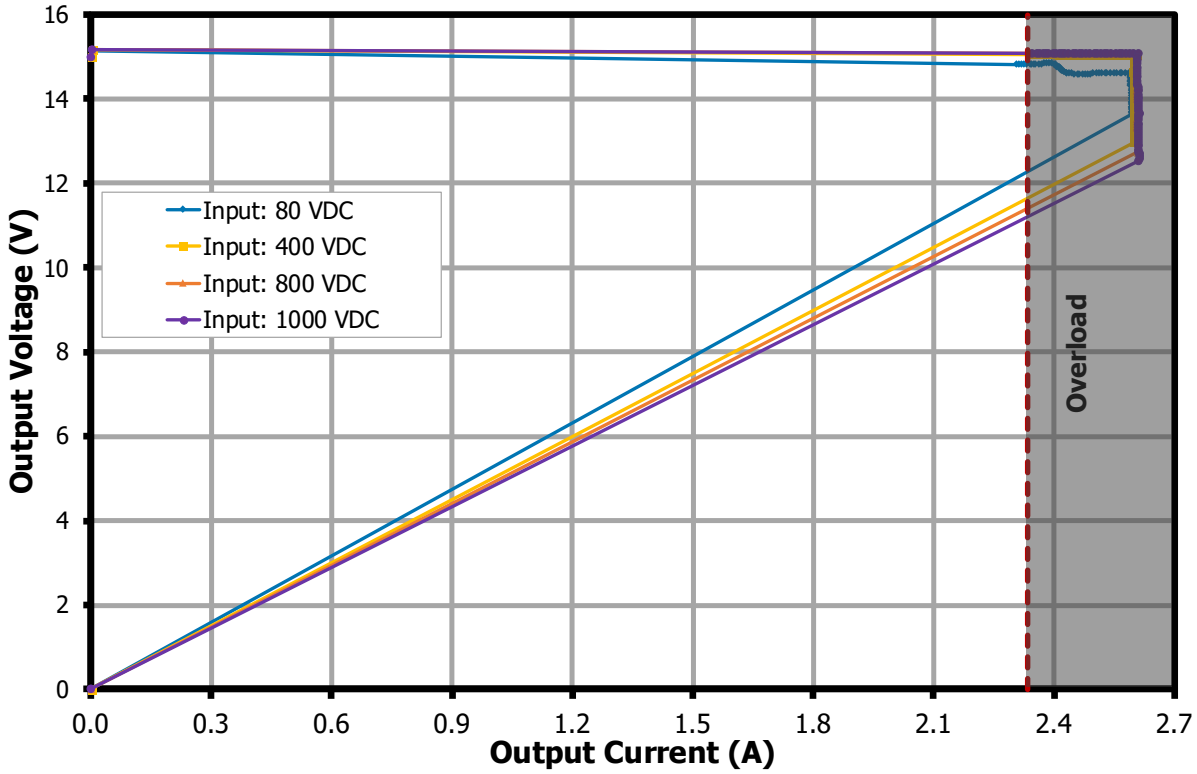


Figure 222 – Output Overload Curve at 85 °C Ambient.

14 Maximum Output Power Derating

The unit under test was placed inside a thermal chamber with ambient temperature set to 85 °C. Maximum output power at each given input voltage was determined by finding the maximum loading condition at which the unit started up without entering auto-restart (AR) or triggering any overtemperature protection. Case temperatures for critical components were also considered when determining the maximum output power capability for the power supply.

14.1 Continuous Output Power

The unit was allowed to stabilize for 30 minutes for each change in input voltage and loading condition during the start of each test sequence.

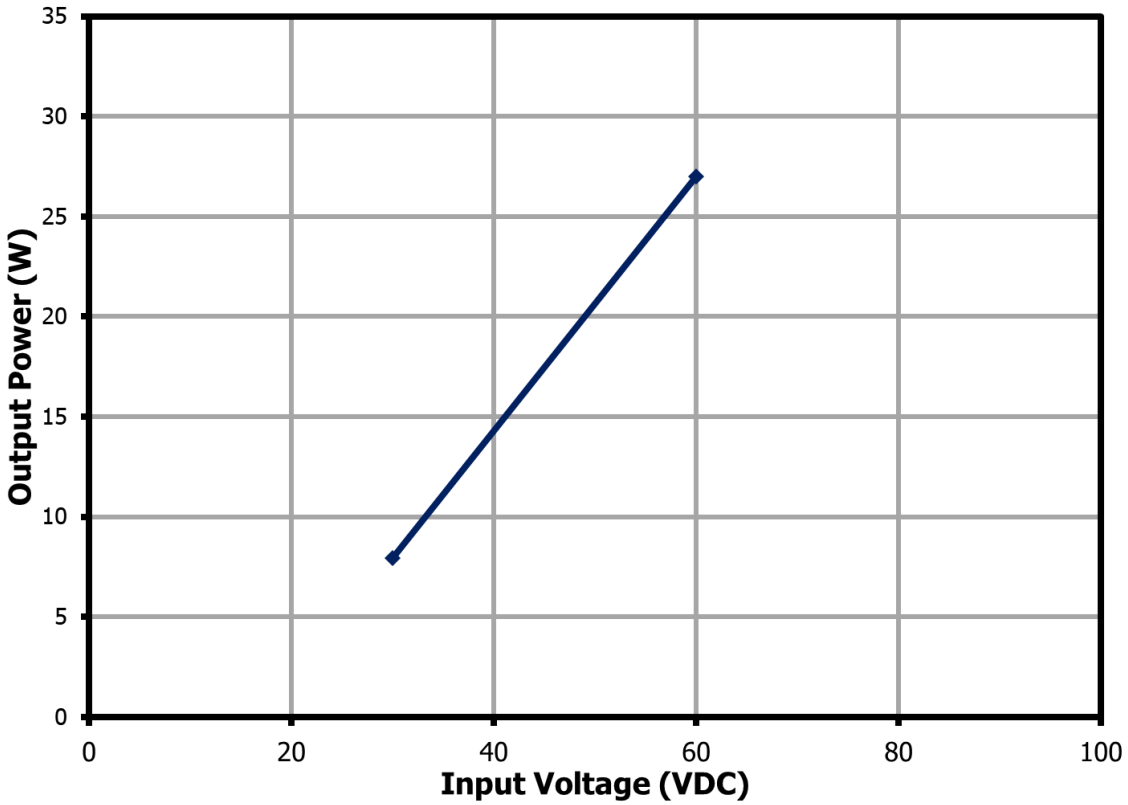


Figure 223 – Maximum Continuous Output Power Curve at 85 °C Ambient.

Input Voltage	Maximum Output Power	Limiting Factor	Value
60 VDC	27 W	Design maximum output power reached	-
30 VDC	7.95 W	InnoSwitch3-AQ power limit	-

Table 21 – Maximum Continuous Output Power Capability Limiting Factor at 85 °C Ambient.

14.2 Start-Up Waveforms at 30 VDC Input

The measurement was taken by connecting the unit to a fully charged DC-link capacitor at 30 VDC. A constant resistance load configuration was used for the start-up test.

14.2.1 Output Voltage and Current at 85 °C Ambient[71]

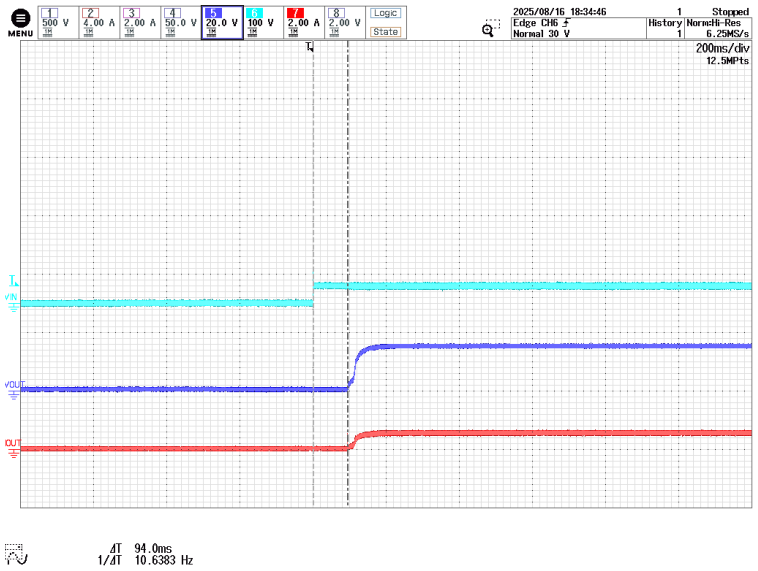


Figure 224 – Output Voltage and Current.
30 VDC, 28.3 Ω Load.
CH5: V_{OUT}, 20 V / div.
CH6: V_{IN}, 100 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

[71] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

14.3 Start-Up Waveforms at 60 VDC Input

The measurement was taken by connecting the unit to a fully charged DC-link capacitor[72] at 60 VDC. A constant resistance load configuration was used for the start-up test.

14.3.1 Output Voltage and Current at 85 °C Ambient[73]

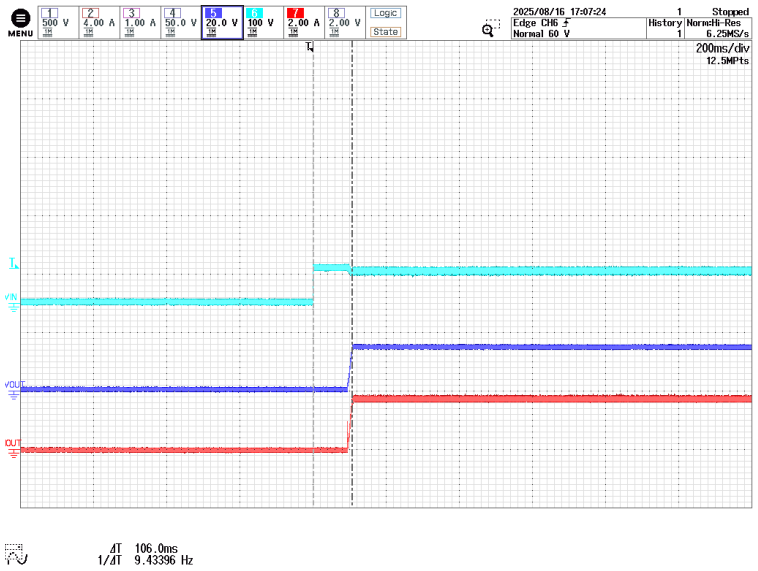


Figure 225 – Output Voltage and Current.
60 VDC, 8.333 Ω Load.
CH5: V_{OUT}, 20 V / div.
CH6: V_{IN}, 100 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

14.4 Peak Output Power

The unit was allowed to stabilize for 30 minutes at 1000 VDC with no load before applying peak output current during the start of each test sequence.

Maximum Peak Output Power	Limiting Factor	Value
35 W for 7 Minutes	InnoSwitch3-AQ overtemperature protection	-

Table 22 – Maximum Peak Output Power Capability Limiting Factor, 1000 VDC Input at 85 °C Ambient.

[72] Inrush current was limited by adding a 10 Ω series resistor between the DC-link capacitor and the unit under test.
[73] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
6-Nov-25	RV	A	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

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