Design Example Report

Title	***10 W USB Charger Using InnoSwitch™3-CE INN3162C-H102***
Specification	85 VAC – 265 VAC Input; 5 V, 2 A Output (End of USB Cable)
Application	Cell Phone / USB Charger
Author	Applications Engineering Department
Document Number	DER-610
Date	May 21, 2021
Revision	1.2

Summary and Features

- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - ±3% CV, ±5% CC regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
  - Smaller, lower cost output capacitors
  - <15 mW no-load input power
  - Cable voltage drop compensation
- Built in synchronous rectification for high efficiency

Power Integrations
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 2 A, 5.0 V USB charger utilizing a device from the InnoSwitch3-CE family of ICs. This design is intended to show the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

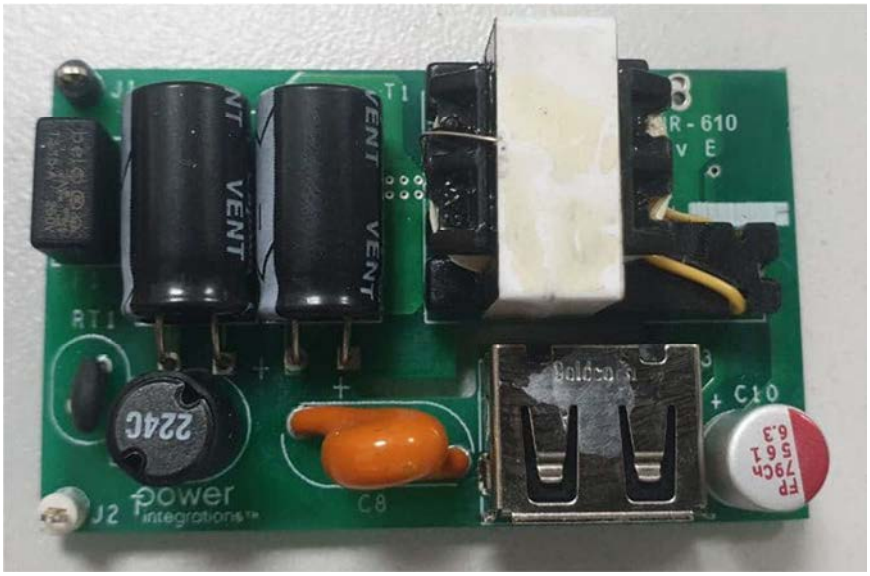

Figure 1 – Populated Circuit Board Photograph, Top.

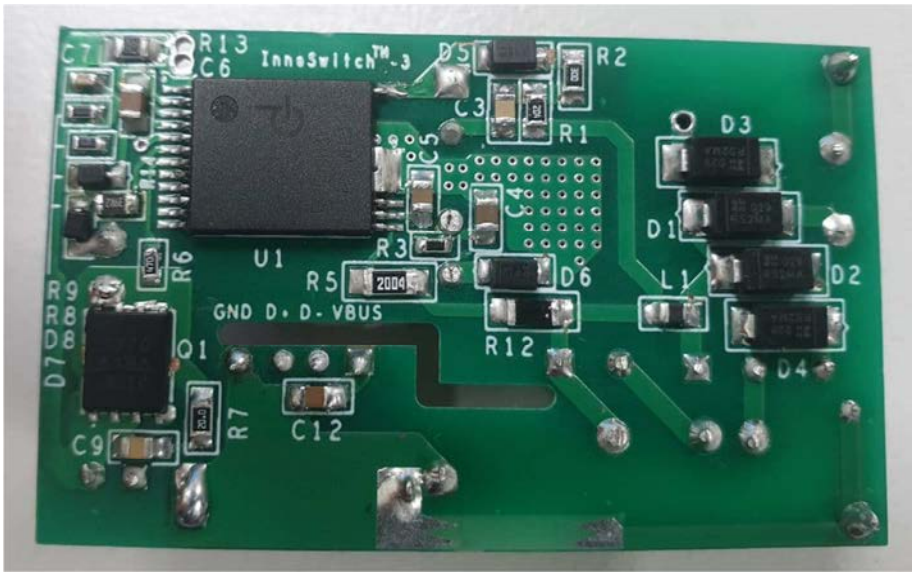

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	50	50/60	60	Hz	
No-load Input Power				15	mW	230 VAC
Output						
Output Voltage	V_{OUT}		5.0		V	±3%
Transient Output Voltage	$V_{OUT(T)}$	4.2		5.5	V	0 A - 2 A - 0 A Load Step End of Cable.
Output Ripple Voltage	V_{RIPPLE}			150	mV	At End of the Output Cable.
Output Cable Compensation	V_{CBL}		300		mV	At 2 A Output Current.
Output Current CC Point	I_{OUT}	2.0		2.3	A	
Rated Output Power	P_{OUT}			10	W	
Efficiency						
Average	$\eta_{AVE[BRD]}$	82			%	Measured at USB Socket.
25%, 50%, 75%, and 100%	$\eta_{AVE[CBL]}$	79			%	With 0.3 V Cable Resistance Drop.
10%	$\eta_{10\%}$	75			%	
Environmental						
Output Cable Impedance	R_{CBL}		150		mΩ	
Conducted EMI		CISPR22B / EN55022B Load Floating or Grounded via Artificial Hand				Resistive Load, 6 dB Margin.
		Connected to Mobile Phone and TV (MHL Connection Enabled)				6 dB Margin.
Line Surge						
Common mode (L1/L2-PE)				6	kV	Ring Wave, Common Mode: 12 Ω.
ESD		±16.5			kV	Air Discharge.
		±8			kV	Contact.
						No Degradation in Performance.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic

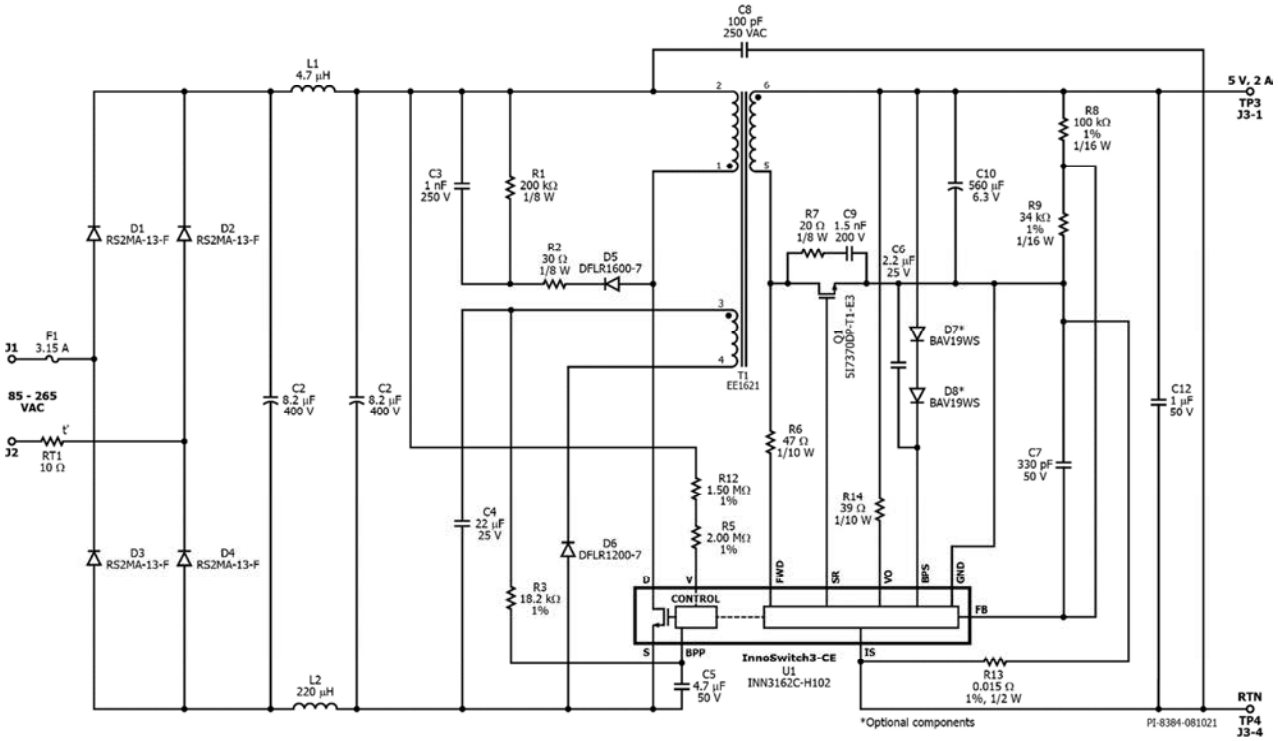

Figure 3 – Schematic.

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4 Circuit Description

4.1 Input EMI Filtering

Fuse F1 provides protection against catastrophic failure of components on the primary-side.

An inrush limiting thermistor (RT1) was necessary due to the low surge current rating of the rectifier diodes (D1-D4) and the relatively high value and therefore low impedance of the bulk storage capacitors C1 and C2.

Physically small diodes were selected for D1 to D4 due to the limited space, specifically height from PCB to case.

Capacitors C1 and C2 provide filtering of the rectified AC Input and together with L1 and L2 form a π (pi) filter to attenuate differential mode EMI. A low value Y capacitor (C8) reduces common mode EMI.

4.2 INN3162C IC Primary

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 650 V power MOSFET inside the INN3162C IC (U1).

A low cost RCD clamp formed by D5, R1, R2, and C3 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C5, when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D6 and capacitor C4, and fed in the BPP pin via a current limiting resistor R3.

Resistor R5 and R12 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C2. At approximately 100 V DC, the current through these resistors exceeds the line under-voltage threshold, which results in enabling of U1. At approximately 460 V DC, the current through these resistors exceeds the line over-voltage threshold, which results in disabling of U1.

4.3 INN3162C IC Secondary

The secondary side of the INN3162C provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 5 V output is provided by SR FET Q1. Very low ESR capacitor C10 provides filtering. Although a 60 V SR FET is chosen in Figure 3, further cost reduction may be realized with a 40V SR FET.

RC snubber network comprising R7 and C9 for Q1 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gate of Q1 is turned on based on the winding voltage sensed via R6 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary side control of the primary-side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output of the SR pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, feeds into the VO pin, and charges the decoupling capacitor C6 via an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V. Resistor R14 provides ESD protection by dampening the ESD energy that is fed onto the VO pin.

Resistor R8 and R9 form a voltage divider network that senses the output voltage from both outputs for better cross-regulation. The INN3162C IC has an internal reference of 1.265 V. Capacitor C7 provides decoupling from high frequency noise affecting power supply operation. Total output current is sensed by R13 with a threshold of approximately 33 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

An optional secondary-side overvoltage protection circuit can be implemented by using two diodes, D7 and D8. In the event of an output overvoltage, the increased voltage at the output causes both diodes to conduct and triggers the auto-restart in the secondary-side controller of the INN3162C IC. Such an implementation for OVP detection is more cost-effective than using a Zener diode with a resistor.

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5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated.

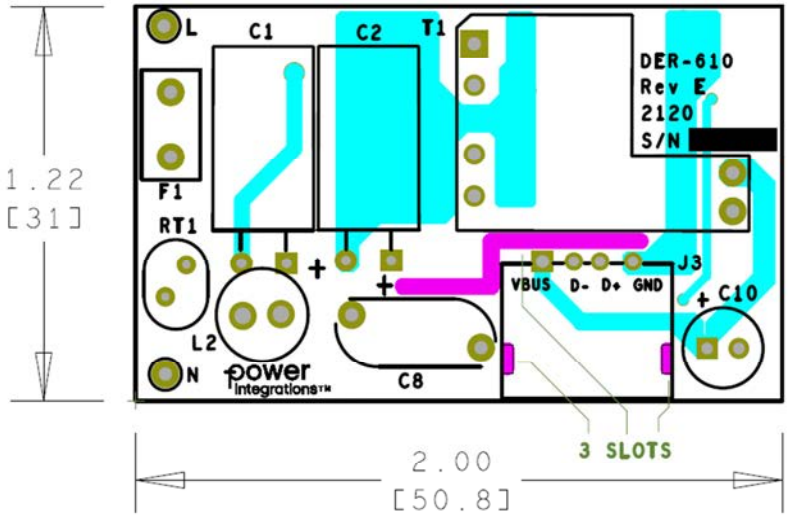

Figure 4 – Printed Circuit Layout, Top.

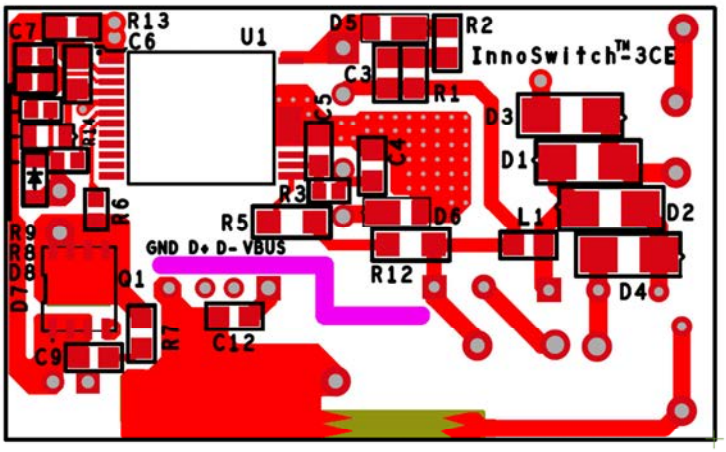

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C2	8.2 µF, 400 V, Electrolytic, (8 x 14)	KM8R2M400F140A	Capxon
2	1	C3	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
3	1	C4	22 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E226M125AC	TDK
4	1	C5	4.7 µF, 50 V, Ceramic, X5R, 0805	CL21A475KBQNNNE	Samsung
5	1	C6	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK Corp
6	1	C7	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
7	1	C8	100 pF, Ceramic, Y1	440LT10-R	Vishay
8	1	C9	1.5 nF, 200 V,10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
9	1	C10	560 µF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
10	1	C12	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
11	4	D1 D2 D3 D4	1000 V, 1.5 A, Glass Passivated, DO-214AC	RS2MA-13-F	Diodes, Inc.
12	1	D5	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
13	1	D6	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
14	2	D7 D8	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
15	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
16	1	L1	4.7 µH, 600 mA SMD INDUCTOR, MULTILAYER	MLZ2012N4R7LT000	TDK
17	1	L2	Inductor, Fixed, 220 µH 0.4 3A 5.4 MHz, Radial Lead	22R224C	Murata
18	1	Q1	60 V, 9.6 A, N-Channel, PowerPAK SO-8	SI7370DP-T1-E3	Vishay
19	1	R1	RES, 200 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ204V	Panasonic
20	1	R2	RES, 30 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ300V	Panasonic
21	1	R3	RES, 18.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1822V	Panasonic
22	1	R5	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
23	1	R6	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
24	1	R7	RES, 20 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ200V	Panasonic
25	1	R8	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
26	1	R9	RES, 34 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3402V	Panasonic
27	1	R12	RES, 1.50 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
28	1	R13	RES, 0.015 Ω, 0.5 W, 1%, 0805	ERJ-6BWFR015V	Panasonic
29	1	R14	RES, 39 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ390V	Panasonic
30	1	RT1	NTC Thermistor, 10 Ω, 0.7 A	MF72-010D5	Cantherm
31	1	T1	Bobbin, EE1621, Vertical, 8 pins, 4pri, 4sec	EE-1621	Shen Zhen Xin Yu Jia Tech
32	1	U1	InnoSwitch3-CE, InSOP24D	INN3162C	Power Integrations

Miscellaneous

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	J1	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
2	1	J2	Test Point, WHT,Miniature THRU-HOLE MOUNT	5002	Keystone
3	1	J3	CONN USB FMALE TYPE A	USB-AF-DIP-094-H	GOLDCONN
4	30mmx20mm		Insulation Paper	560GC- ND	GC Electronics

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7 Transformer Specification

7.1 Electrical Diagram

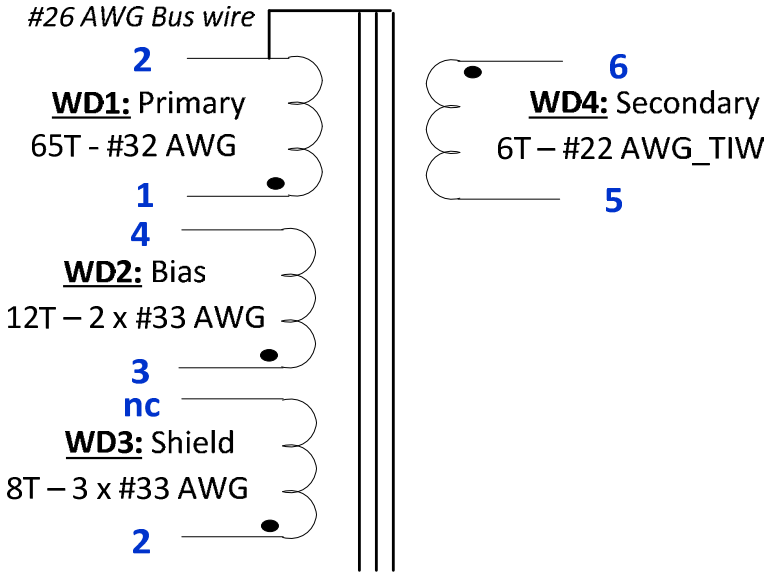

Figure 6– Transformer Electrical Diagram.

7.2 Electrical Specification

Electrical Strength	1 sec, 60 Hz, from pins 1-4 to pins 5-6	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	1230 µH ±7%
Resonant Frequency	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	800 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with pins 5-6 shorted, measured at 100 kHz, 0.4 V_{RMS}.	50.0 µH (Max.)

7.3 Material List

Item	Description
[1]	Core: EE1621; Hong Kong Magnetics, ME 95;or Equivalent; gapped for ALG of 218nH/T².
[2]	Bobbin: EE1621-Vertical – 8 pins (4/4), SHEN ZEN XIN YU JIA Technology LTD.
[3]	Magnet Wire: #32 AWG, Double Coated.
[4]	Magnet Wire: #33 AWG, Double Coated.
[5]	Magnet Wire: #21 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 5.5 mm Wide.
[7]	Bus Wire: #26 AWG, Belden Electronics Div.; or Equivalent.
[8]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

WD4: Secondary 6T – #22 AWG_TIW

WD3: Shield 8T – 3 x #33 AWG

WD2: Bias 12T – 2 x #33 AWG

WD1: Primary 65T - #32 AWG

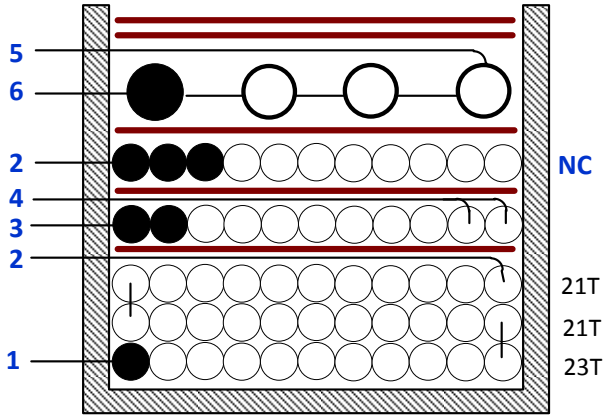

Figure 7– Transformer Build Diagram.

7.5 Transformer Instructions

Winding Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start at pin 1, wind 65 turns of wire Item [3] in 3 layers (23T+21T+21T) with tight tension. At the last turn bring the wire back to the left and finish at pin 2.
Insulation	1 layer of tape item [6] for insulation.
WD2 Bias	Use 2 wires of Item [4], start at pin 3, and wind 12 turns from left to right with tight tension. At the last turn, bring the wires back to the left to terminate at 4.
Insulation	1 1ayer of tape Item [6] for insulation.
WD3 Shield	Use 3 wires of Item [4], start at pin 2, and wind 8 turns from left to right. At the last turn, cut short wires for no-connect.
Insulation	1 1ayer of tape Item [6] for insulation.
WD4 Secondary	Start at pin 6, wind 6 turns of wire Item [5] from left to right. At the last turn, bring the wire back to the left and finish at pin 5.
Insulation	2 layers of tape Item [6] to secure the windings.
Finish	Gap core halves for 1230 µH inductance. Use 2”of bus wire Item [7] solder to pin 2. Wrap core halves and bus wire above which lean along the core with tape (see illustration below). Varnish Item [8].

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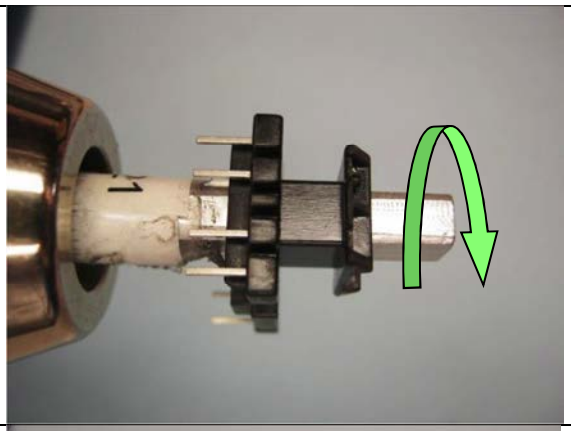
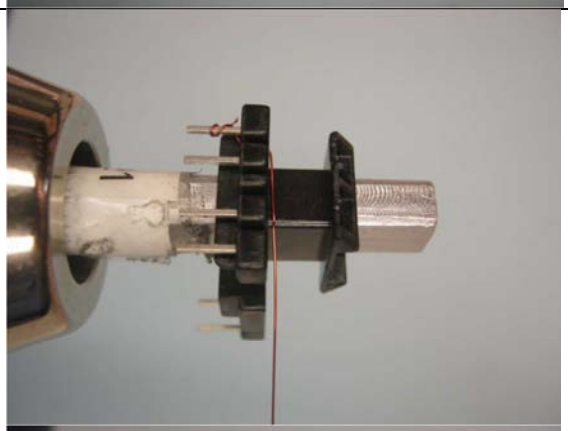
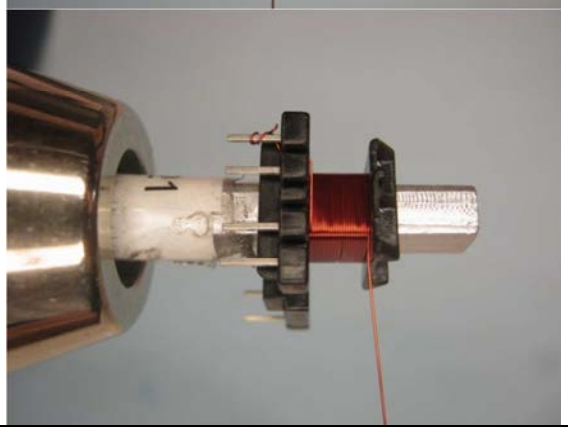
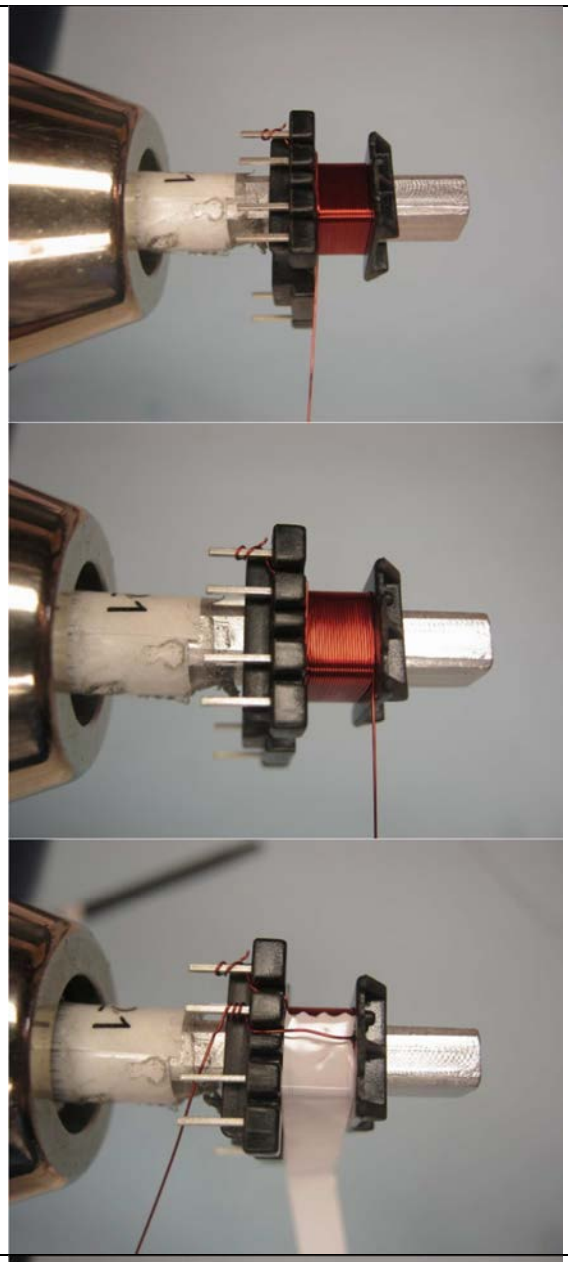
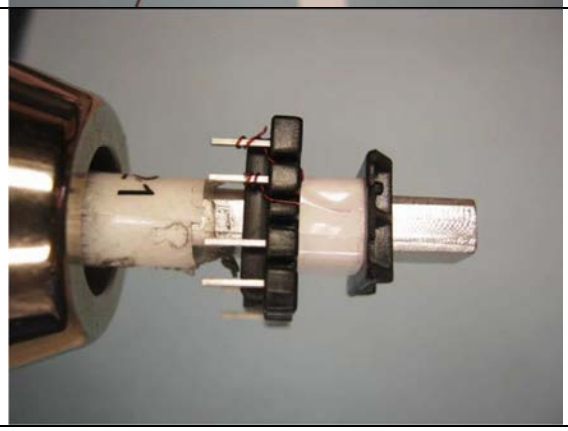
7.6 Winding Illustrations

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	 	Start at pin 1, wind 65 turns of wire Item [3] in 3 layers (23T+21T+21T) with tight tension. At the last turn bring the wire back to the left and finish at pin 2.

		
Insulation		1 layer of tape Item [7] for insulation.

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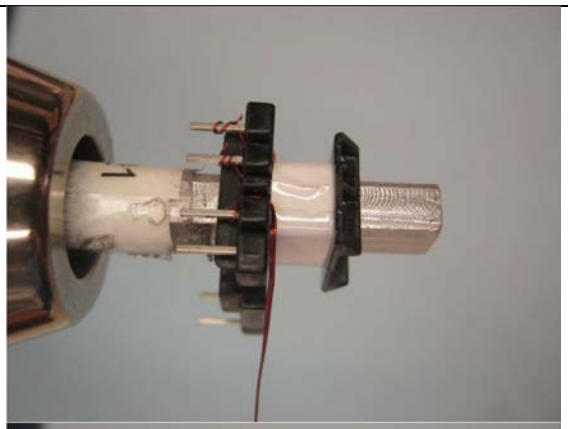
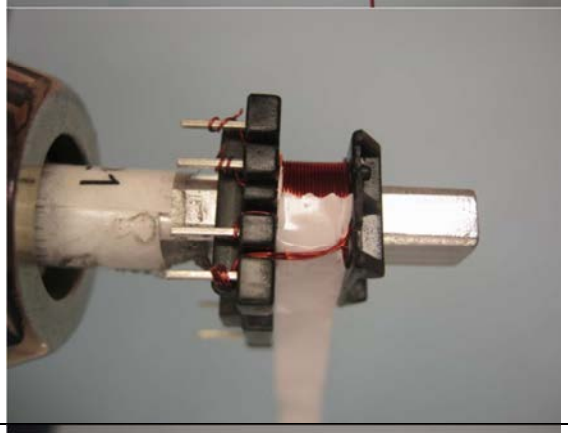
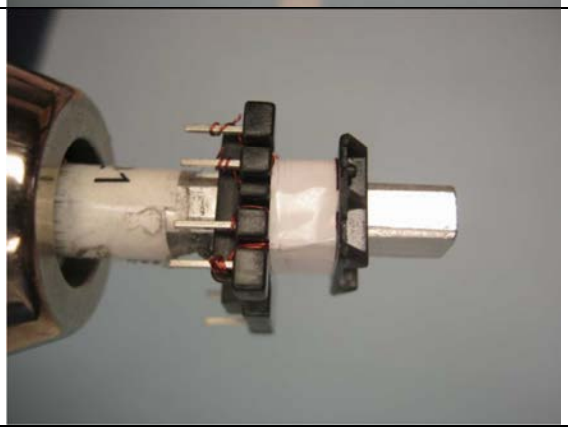
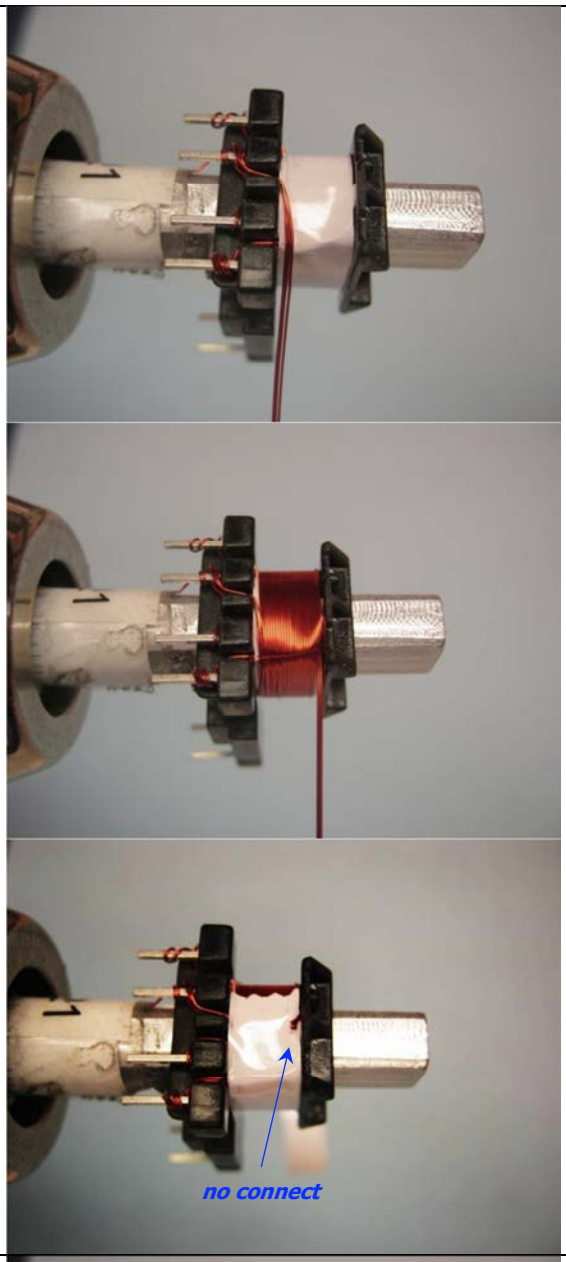
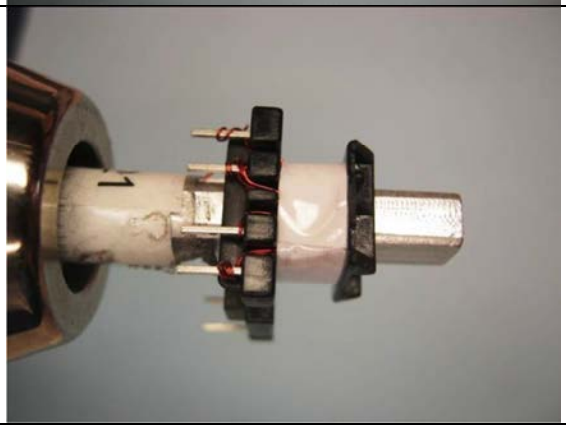
WD2 **Bias**	  	Use 2 wires of Item [4], start at pin 3, and wind 12 turns from left to right with tight tension. At the last turn, bring the wires back to the left to terminate at 4.
Insulation		1 layer of tape Item [6] for insulation.

WD3 **Shield**		Use 3 wires of Item [4], start at pin 2, and wind 8 turns from left to right. At the last turn, cut short wires for no-connect.
Insulation		1 layer of tape Item [6] for insulation.

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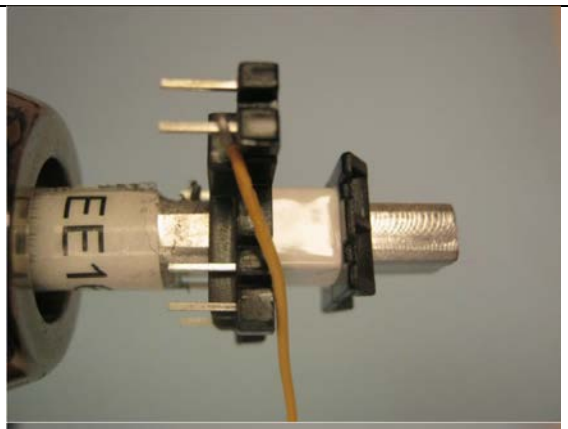
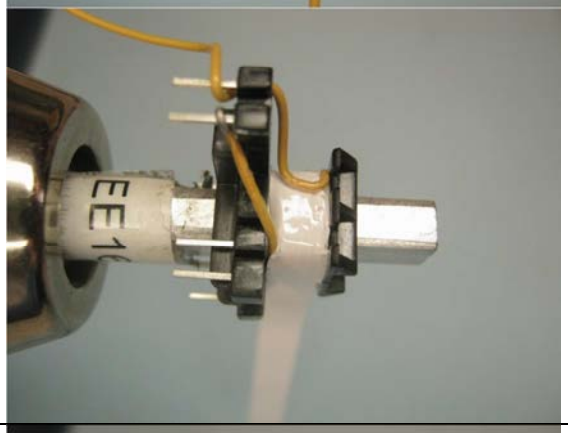
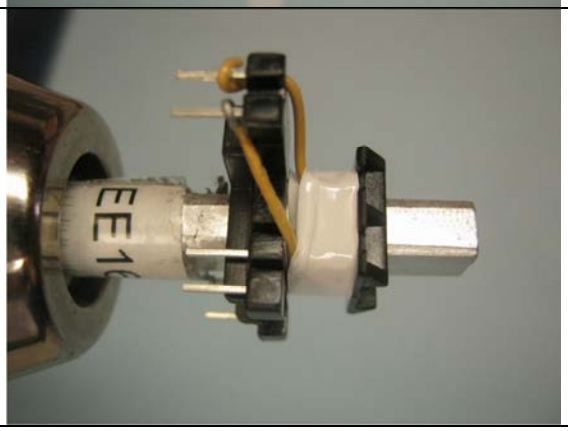
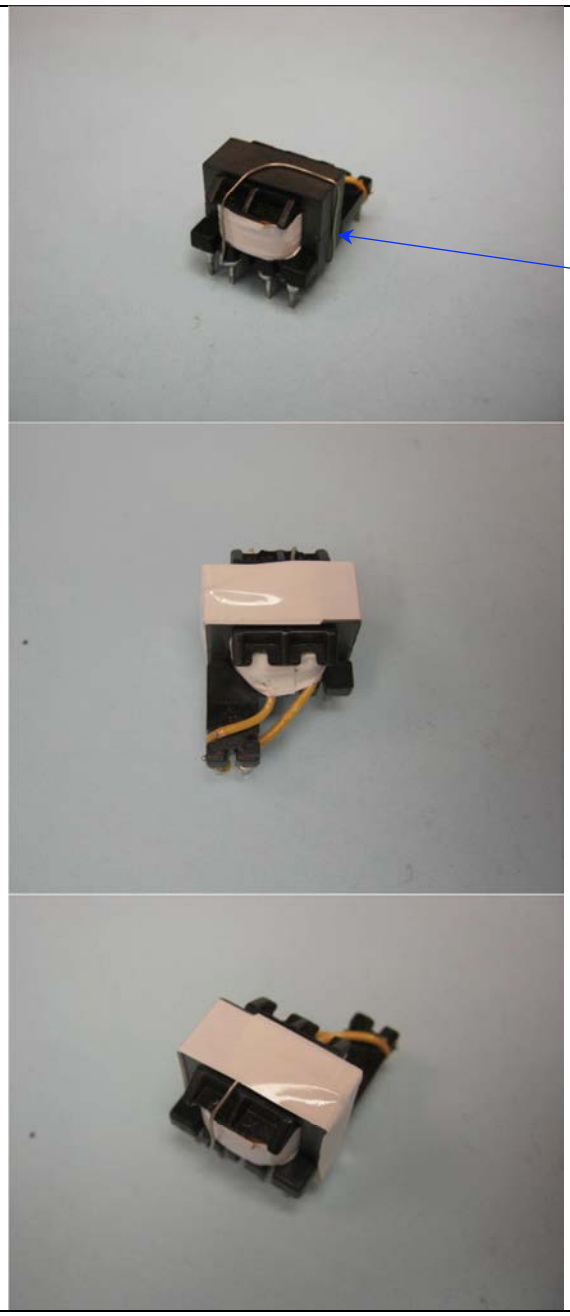
WD4 Secondary	  	Start at pin 6, wind 6 turns of wire Item [5] from left to right. At the last turn, bring the wire back to the left and finish at pin 5.
Insulation		2 layers of tape Item [6] to secure the windings.

Finish		Gap core halves for 1230 µH inductance. Use 2”of bus wire Item [7] solder to pin 2. Wrap core halves and bus wire above which lean along the core with tape. Varnish Item [8].

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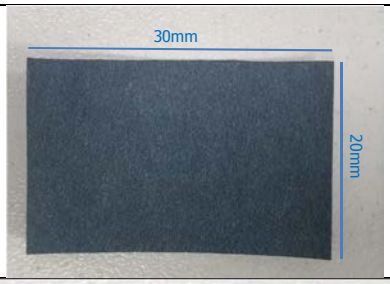
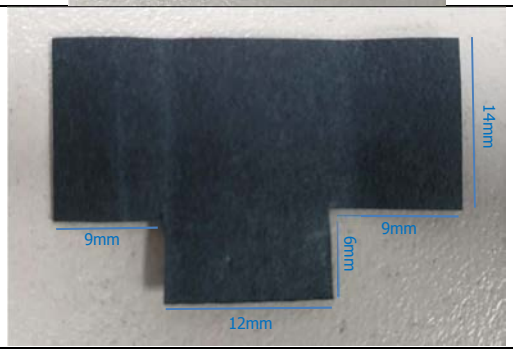
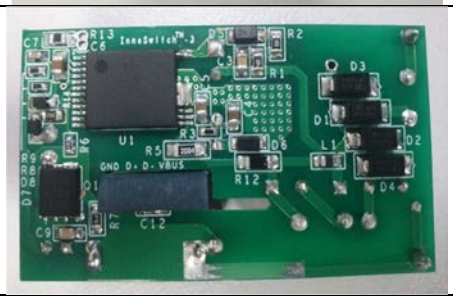
8 Board Preparation

Insulator Preparation		For the purpose of providing better isolation between the primary and secondary, a 30mm by 20mm insulation paper is needed.
Insulator Preparation		Provided measurements are needed for the preparation to isolate both primary and secondary of the top side and the bottom side of the PCB.
Insulator: Top side		Chip in the insulation paper onto the slot of the test vehicle. Ensure that the height of the paper and the transformer are equal.
Insulator: Bottom side		Folding the paper inwards will hold the position of the paper and at the same time, provide isolation between the primary and secondary of the bottom side of the PCB.

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-CE_Flyback_082217; Rev.1.0; Copyright Power Integrations 2017	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 CE Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VIN_MIN			85	V	Minimum AC input voltage
4	VIN_MAX			265	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	16.4		16.4	uF	Input capacitor
8	VOUT	5.00		5.30	V	Output voltage at the board
9	PERCENT_CDC	6%	Info	6%		Refer to the device H-code in the datasheet to ensure that the desired H-code is available for the device selected
10	IOUT	2.00		2.00	A	Output current
11	POUT		Info	10.60	W	The specified output power exceeds the device power capability: Verify thermal performance
12	EFFICIENCY	0.85		0.85		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
18	**PRIMARY CONTROLLER SELECTION**					
19	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
20	DEVICE_GENERIC	INN31X2		INN31X2		Generic device code
21	DEVICE_CODE			INN3162C		Actual device code
22	POUT_MAX			10	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			11.60	Ω	Primary MOSFET on time drain resistance at 100 degC
24	ILIMIT_MIN			0.50	A	Minimum current limit of the primary MOSFET
25	ILIMIT_TYP			0.55	A	Typical current limit of the primary MOSFET
26	ILIMIT_MAX			0.60	A	Maximum current limit of the primary MOSFET
27	VDRAIN_BREAKDOWN			650	V	Device breakdown voltage
28	VDRAIN_ON_MOSFET			1.87	V	Primary MOSFET on time drain voltage
29	VDRAIN_OFF_MOSFET			501.4	V	Peak drain voltage on the primary MOSFET during turn-off
33	**WORST CASE ELECTRICAL PARAMETERS**					
34	FSWITCHING_MAX	98000		98000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	58.0		58.0	V	Seconday voltage reflected to the primary when the primary MOSFET turns off
36	VMIN			73.44	V	Valley of the rectified minimum AC input voltage at full power
37	KP			0.55		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			CCM		Mode of operation
39	DUTYCYCLE			0.448		Primary MOSFET duty cycle
40	TIME_ON			7.37	us	Primary MOSFET on-time
41	TIME_OFF			5.64	us	Primary MOSFET off-time
42	LPRIMARY_MIN			1174.9	uH	Minimum primary inductance

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43	LPRIMARY_TYP			1236.7	uH	Typical primary inductance
44	LPRIMARY_TOL	5.0		5.0	%	Primary inductance tolerance
45	LPRIMARY_MAX			1298.5	uH	Maximum primary inductance
47	**PRIMARY CURRENT**					
48	IPEAK_PRIMARY			0.57	A	Primary MOSFET peak currrent
49	IPEDESTAL_PRIMARY			0.22	A	Primary MOSFET current pedestal
50	IAVG_PRIMARY			0.16	A	Primary MOSFET average current
51	IRIPPLE_PRIMARY			0.42	A	Primary MOSFET ripple current
52	IRMS_PRIMARY			0.25	A	Primary MOSFET RMS current
54	**SECONDARY CURRENT**					
55	IPEAK_SECONDARY			6.17	A	Secondary winding peak current
56	IPEDESTAL_SECONDARY			2.43	A	Secondary winding current pedestal
57	IRMS_SECONDARY			3.41	A	Secondary winding RMS current
61	**TRANSFORMER CONSTRUCTION PARAMETERS**					
62	**CORE SELECTION**					
63	CORE	Custom	Info	Custom		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
64	CORE CODE	EE1621		EE1621		Core code
65	AE	32.50		32.50	mm^2	Core cross sectional area
66	LE	39.30		39.30	mm	Core magnetic path length
67	AL	2800		2800	nH/turns^2	Ungapped core effective inductance
68	VE	980.0		980.0	mm^3	Core volume
69	BOBBIN	EE1621		EE1621		Bobbin
70	AW	12.33		12.33	mm^2	Window area of the bobbin
71	BW	5.40		5.40	mm	Bobbin width
72	MARGIN	0.0		0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
74	**PRIMARY WINDING**					
75	NPRIMARY			65		Primary turns
76	BPEAK			3775	Gauss	Peak flux density
77	BMAX			3461	Gauss	Maximum flux density
78	BAC			946	Gauss	AC flux density
79	ALG			293	nH/turns^2	Typical gapped core effective inductance
80	LG			0.125	mm	Core gap length
81	LAYERS_PRIMARY			3		Number of primary layers
82	AWG_PRIMARY	32		32	AWG	Primary winding wire AWG
83	OD_PRIMARY_INSULATED			0.244	mm	Primary winding wire outer diameter with insulation
84	OD_PRIMARY_BARE			0.202	mm	Primary winding wire outer diameter without insulation
85	CMA_PRIMARY			249	Cmil/A	Primary winding wire CMA
87	**SECONDARY WINDING**					
88	NSECONDARY	6		6		Secondary turns
89	AWG_SECONDARY			22	AWG	Secondary winding wire AWG
90	OD_SECONDARY_INSULATED			0.947	mm	Secondary winding wire outer diameter with insulation
91	OD_SECONDARY_BARE			0.644	mm	Secondary winding wire outer diameter without insulation
92	CMA_SECONDARY			210	Cmil/A	Secondary winding wire CMA
94	**BIAS WINDING**					
95	NBIAS			15		Bias turns
99	**PRIMARY COMPONENTS SELECTION**					
100	**Line undervoltage**					
101	BROWN-IN REQURED			72.3	V	Required AC RMS line voltage brown-in threshold
102	RLS			4.30	MΩ	Connect two 2.15 MOhm resistors to the V-pin for the required UV/OV threshold

103	BROWN-IN ACTUAL			73.3	V	Actual AC RMS brown-in threshold
104	BROWN-OUT ACTUAL			67.2	V	Actual AC RMS brown-out threshold
106	**Line overvoltage**					
107	OVERVOLTAGE_LINE			322.8	V	Actual AC RMS line over-voltage threshold
109	**Bias diode**					
110	VBIAS			12.0	V	Rectified bias voltage
111	VF_BIAS			0.70	V	Bias winding diode forward drop
112	VREVERSE_BIASDIODE			98.16	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
113	CBIAS			22	uF	Bias winding rectification capacitor
114	CBPP			4.70	uF	BPP pin capacitor
118	**SECONDARY COMPONENTS**					
119	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
120	RFB_LOWER			31.60	kΩ	Lower feedback resistor
121	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
125	**MULTIPLE OUTPUT PARAMETERS**					
126	**OUTPUT 1**					
127	VOUT1			5.30	V	Output 1 voltage
128	IOUT1			2.00	A	Output 1 current
129	POUT1			10.60	W	Output 1 power
130	IRMS_SECONDARY1			3.06	A	Root mean squared value of the secondary current for output 1
131	IRIPPLE_CAP_OUTPUT1			2.31	A	Current ripple on the secondary waveform for output 1
132	AWG_SECONDARY1			22	AWG	Wire size for output 1
133	OD_SECONDARY1_INSULATED			0.947	mm	Secondary winding wire outer diameter with insulation for output 1
134	OD_SECONDARY1_BARE			0.644	mm	Secondary winding wire outer diameter without insulation for output 1
135	CM_SECONDARY1			612	Cmils	Bare conductor effective area in circular mils for output 1
136	NSECONDARY1			6		Number of turns for output 1
137	VREVERSE_RECTIFIER1			39.76	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
138	SRFET1	Auto		Si4436DY		SRFET selection for output 1
139	VF_SRFET1			0.086	V	SRFET on-time drain voltage for output 1
140	VBREAKDOWN_SRFET1			60	V	SRFET breakdown voltage for output 1
141	RDSON_SRFET1			43.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
182	**TOLERANCE ANALYSIS**					
183	CORNER_VAC			85	V	Input AC RMS voltage corner to be evaluated
184	CORNER_ILIMIT	TYP		0.55	A	Current limit corner to be evaluated
185	CORNER_LPRIMARY	TYP		1236.7	uH	Primary inductance corner to be evaluated
186	MODE_OPERATION			CCM		Mode of operation
187	KP			0.648		Measure of continuous/discontinuous mode of operation
188	FSWITCHING			75038	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
189	DUTYCYCLE			0.448		Steady state duty cycle
190	TIME_ON			5.97	us	Primary MOSFET on-time
191	TIME_OFF			7.36	us	Primary MOSFET off-time
192	IPEAK_PRIMARY			0.53	A	Primary MOSFET peak currrent

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193	IPEDESTAL_PRIMARY			0.19	A	Primary MOSFET current pedestal
194	IAVERAGE_PRIMARY			0.16	A	Primary MOSFET average current
195	IRIPPLE_PRIMARY			0.35	A	Primary MOSFET ripple current
196	IRMS_PRIMARY			0.25	A	Primary MOSFET RMS current
197	CMA_PRIMARY			253	Cmil/A	Primary winding wire CMA
198	BPEAK			3296	Gauss	Peak fux density
199	BMAX			3118	Gauss	Maximum flux density

10 Performance Data

All measurements performed with external room ambient temperature and 60 Hz input for 115 VAC range and 50 Hz for 230 VAC input range.

10.1 Average Efficiency

10.1.1 Efficiency Requirements

Test	Average	Average	Average	Average	10% Load	10% Load
Model	Low Voltage	Low Voltage	Low Voltage	Low Voltage	Low Voltage	Low Voltage
Effective	Now	2016	Now	2016	Now	2016
Power [W]	**Energy Star 2**	**New IESA2007**	**CoC v5 Tier 1**	**CoC v5 Tier 2**	**CoC v5 Tier 1**	**CoC v5 Tier 2**
10	**74.2%**	**78.7%**	**76.0%**	**79.0%**	**66.6%**	**69.7%**

10.1.2 Average Efficiency Measured (at the PCB Output Terminal)

Load	115 VAC	230 VAC
100%	86.04%	88.44%
75%	87.02%	87.32%
50%	87.34%	87.40%
25%	88.04%	86.61%
10%	87.20%	82.14%
Average	**87.11%**	**87.44%**

10.1.3 Average Efficiency Measured (at the End of Cable)

Load	115 VAC	230 VAC
100%	81.15%	83.42%
75%	83.25%	83.54%
50%	84.80%	84.87%
25%	86.75%	85.33%
10%	86.69%	81.66%
Average	**83.99%**	**84.29%**

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10.2 Efficiency vs. Line

10.2.1 Measured at 2 A Full Load

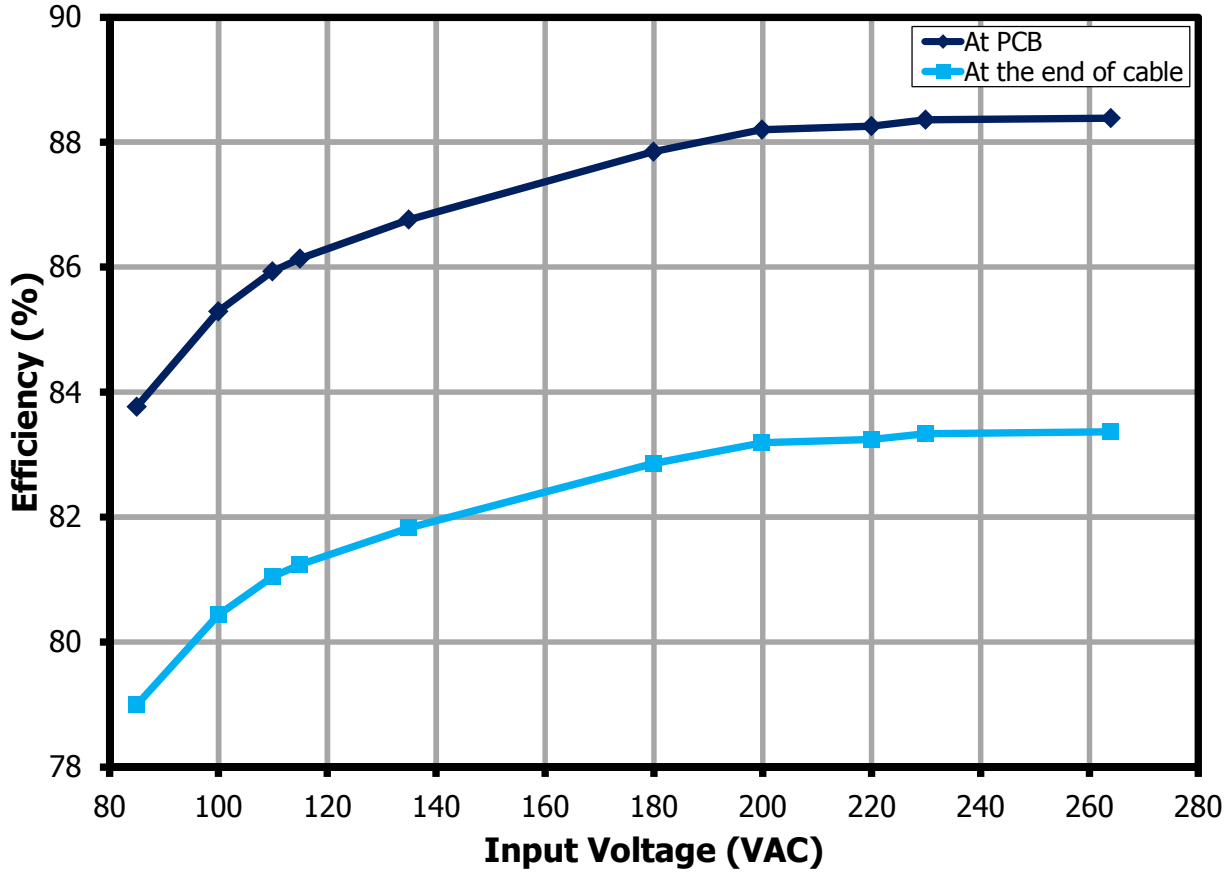

Figure 8 – Efficiency vs. Line.

10.3 Efficiency vs. Load

10.3.1 Measured at PCB Output Terminal

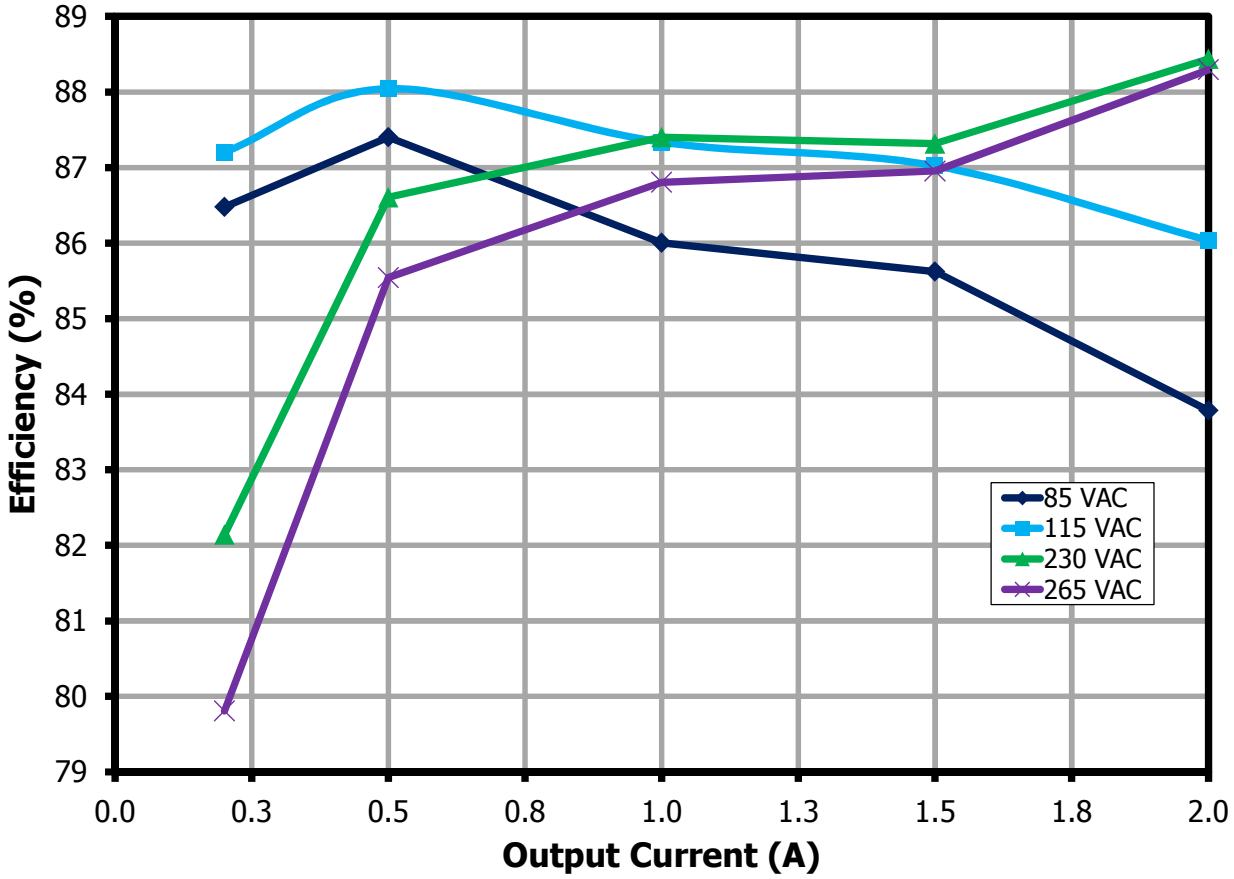

Figure 9 – Efficiency vs. Load (Measured at PCB Output Terminal).

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10.3.2 Measured at End of 150 mΩ Cable

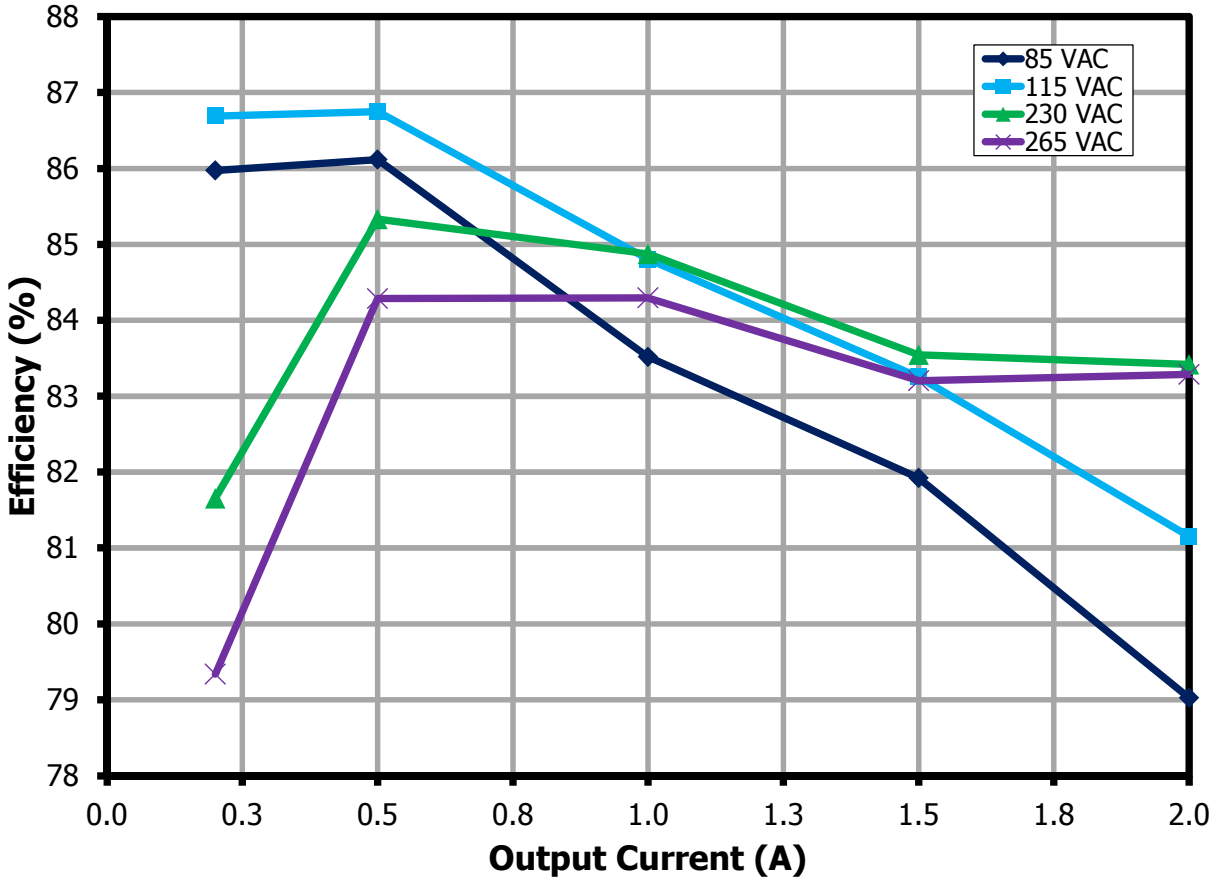

Figure 10 – Efficiency vs Load (Measured at End of 150 mΩ Cable).

11 *CV/CC Regulation*

11.1 CV/CC Regulation at 25 ºC Measured on PCB Output Terminal

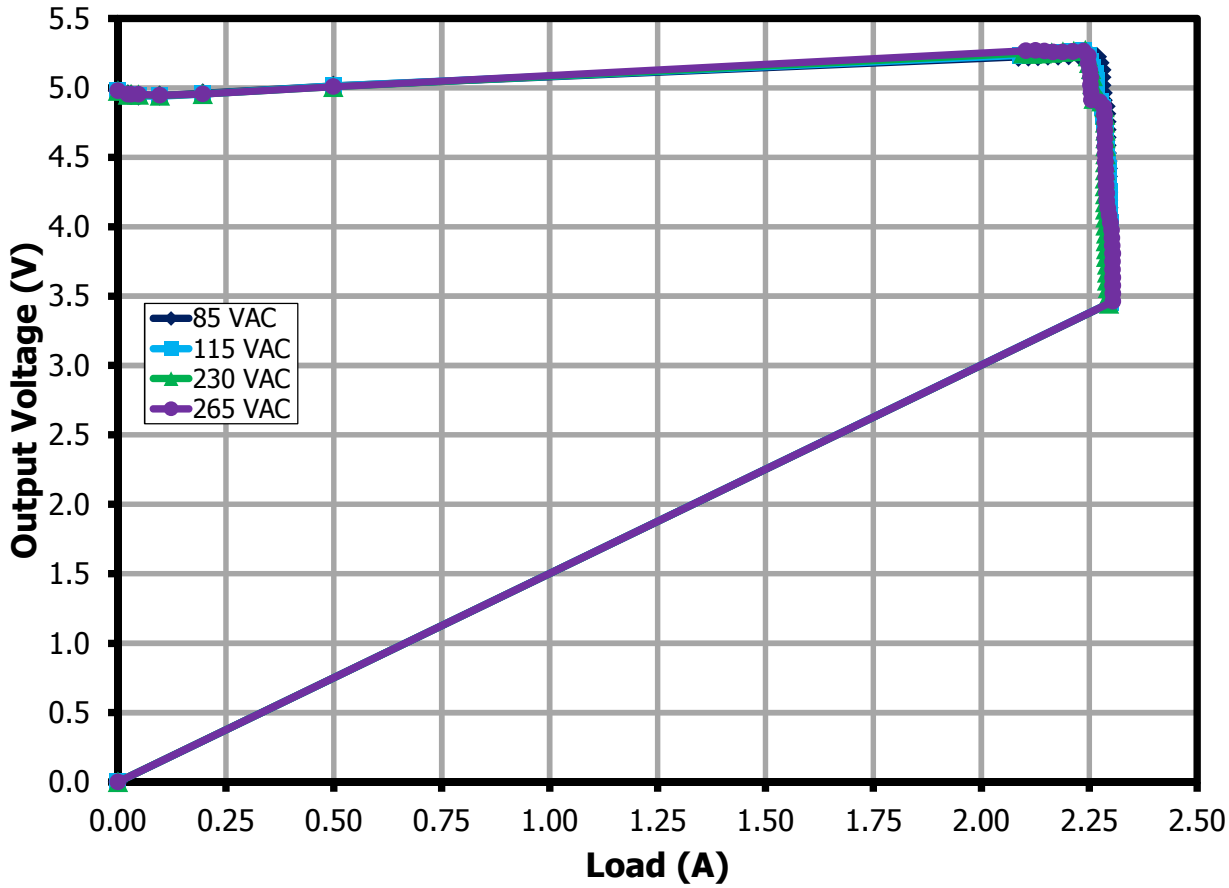

Figure 11 – CVCC at PCB Output Terminal. Room Temperature.

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11.2 CV/CC Regulation at 25 ºC Measured on End of 150 mΩ Cable

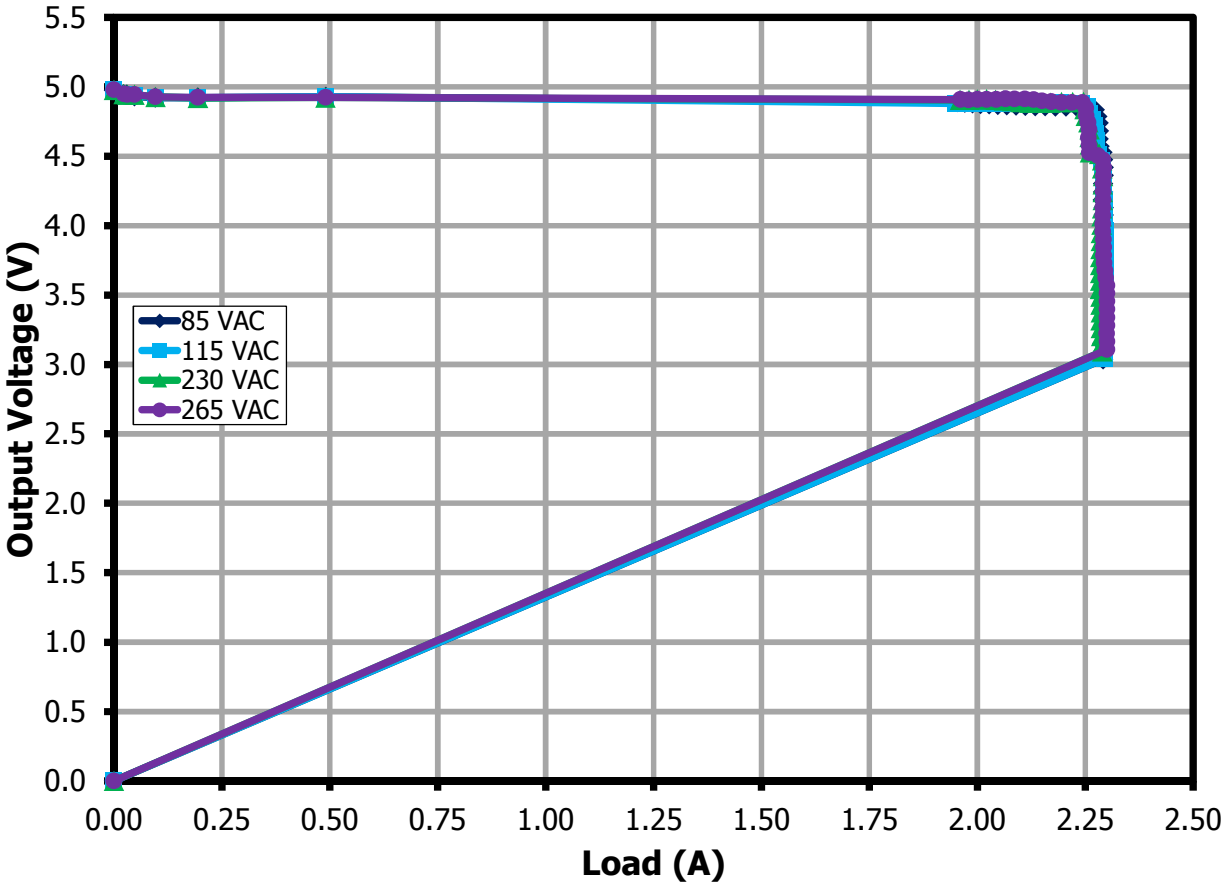

Figure 12 – CV/CC measured with 47 µF at the end of 150 mΩ Cable. Room Temperature.

11.3 CV/CC Regulation at Hot and Cold Temperature

11.3.1 85 VAC

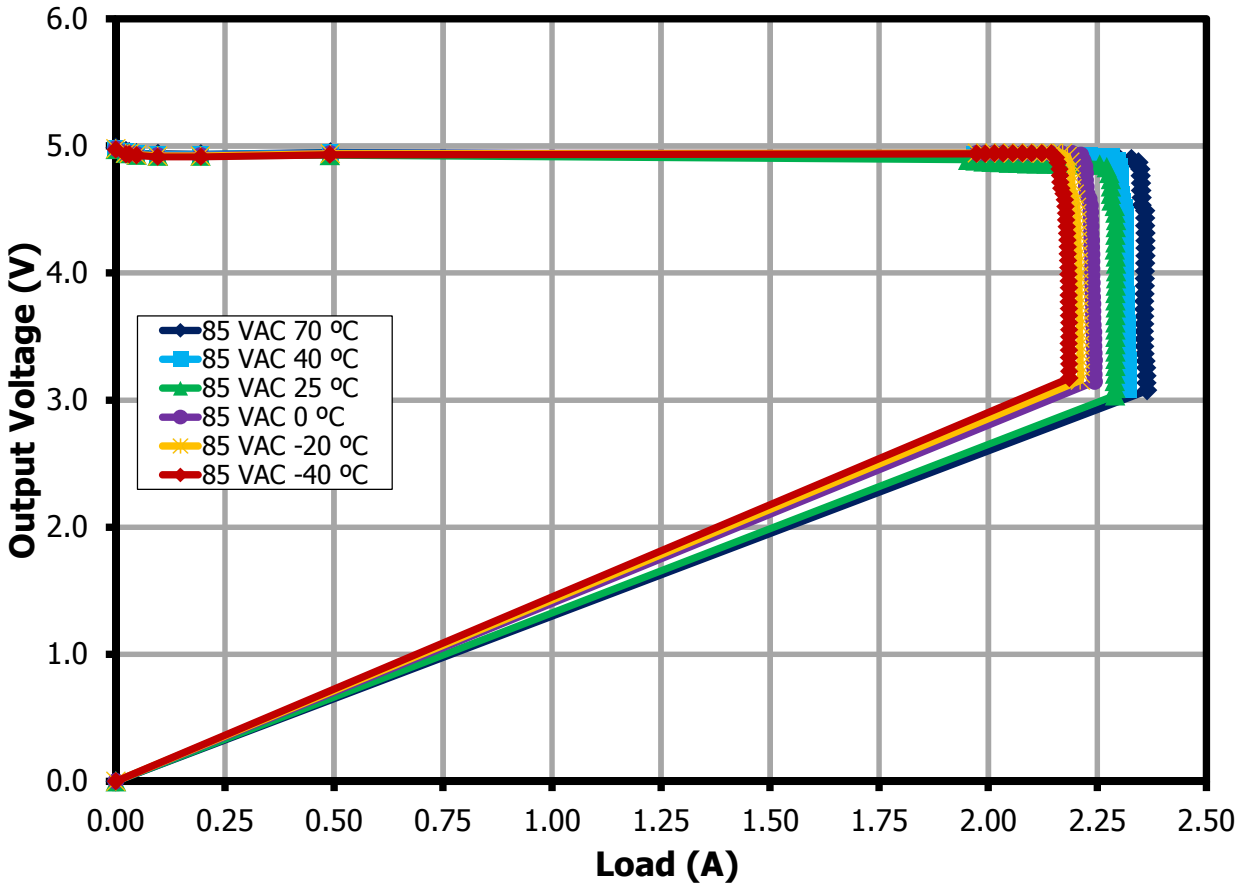

Figure 13 – 85 VAC CV/CC Measured with 47 µF Capacitor at the End of 150 Ω Cable.

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11.3.2 115 VAC

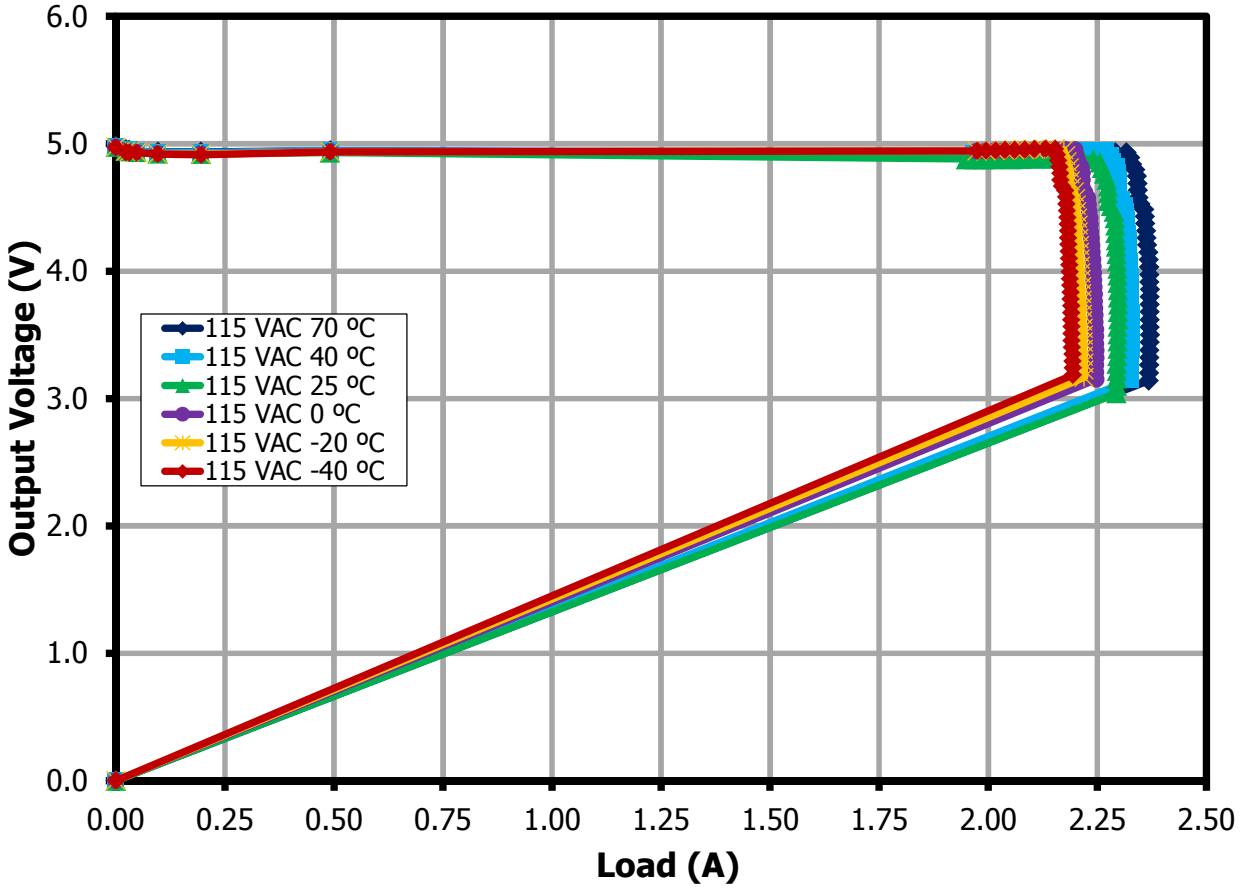

Figure 14 – 115 VAC CV/CC Measured with 47 µF Capacitor at the End of 150 Ω Cable.

11.3.3 230 VAC

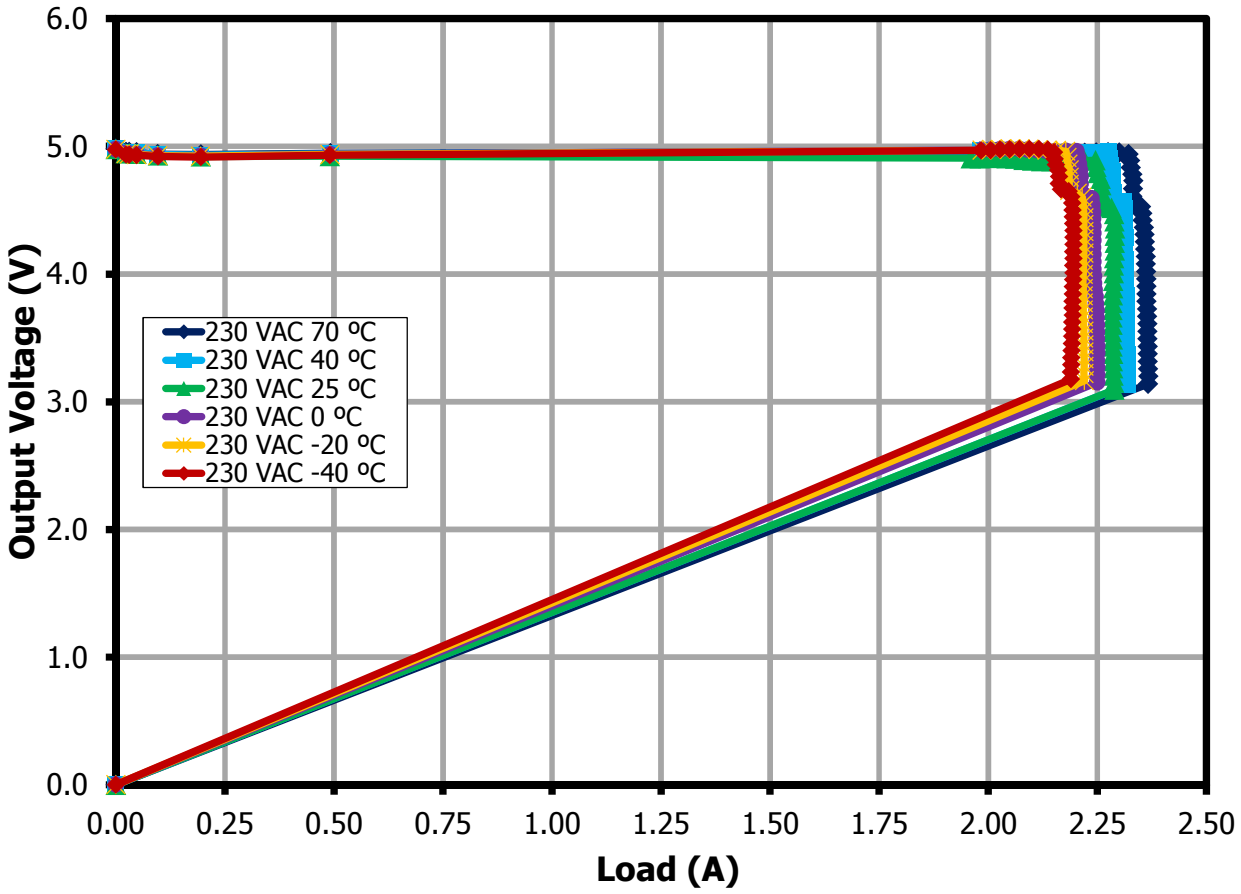

Figure 15 – 230 VAC CV/CC Measured with 47 µF Capacitor at the End of 150 Ω Cable.

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11.3.4 265 VAC

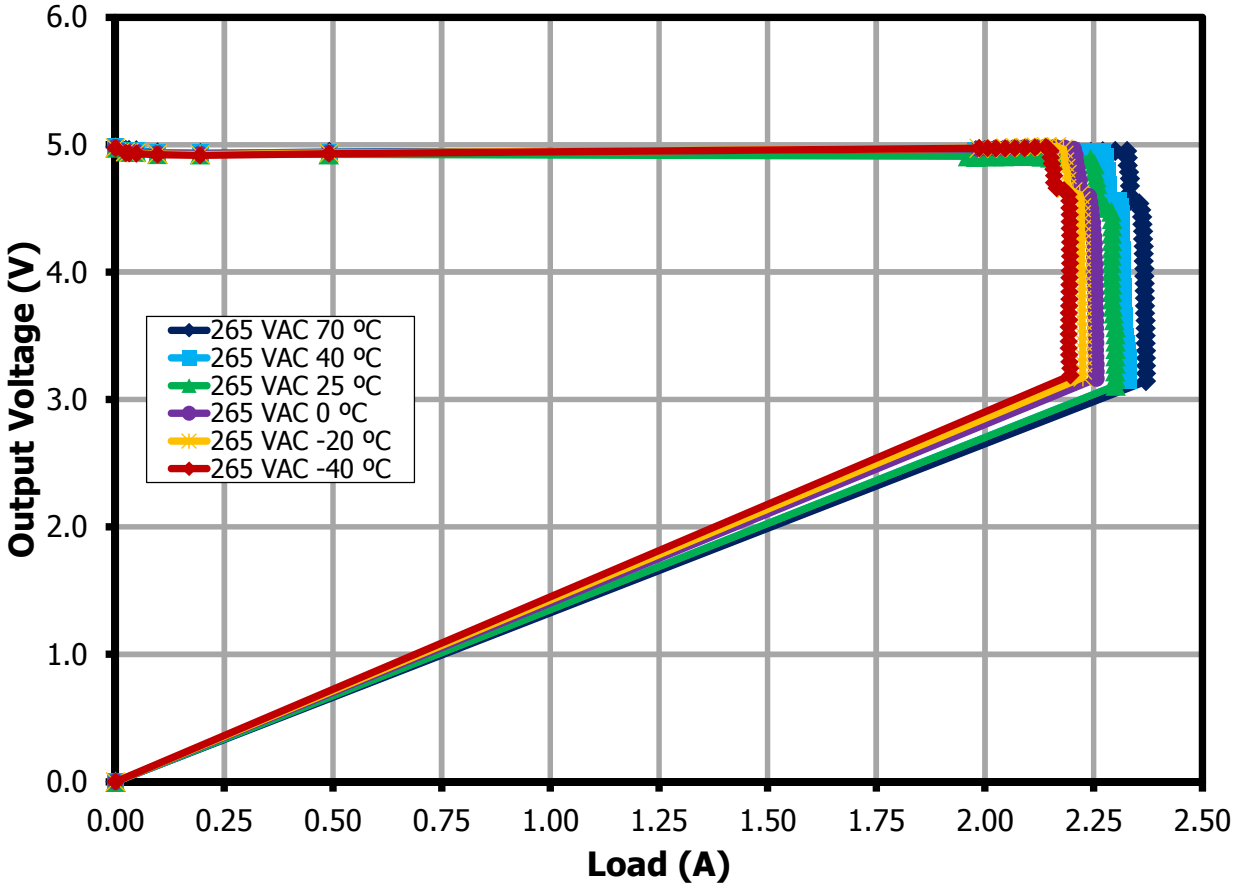

Figure 16 – 265 VAC CV/CC Measured with 47 µF Capacitor at the End of 150 Ω Cable.

11.4 No-Load Input Power

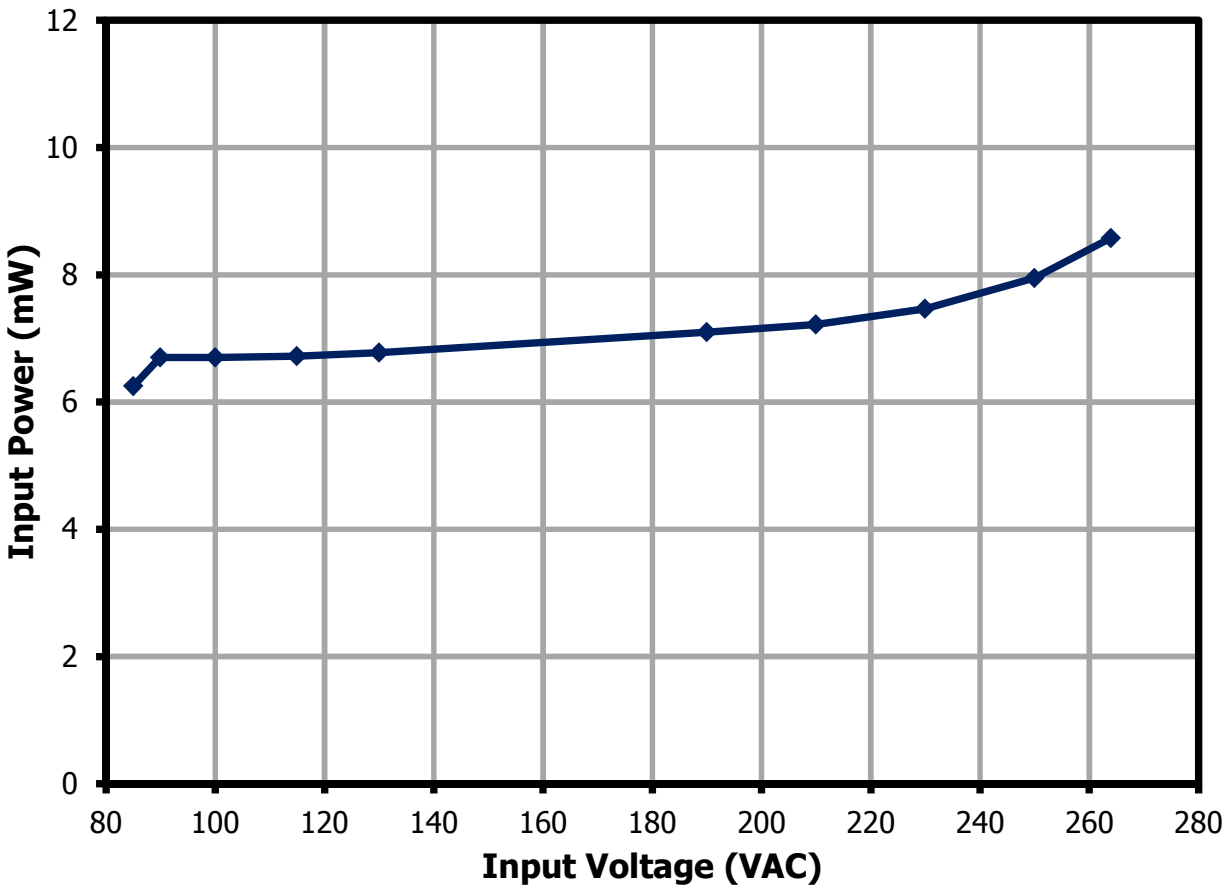

Figure 17 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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11.5 Line Regulation

11.5.1 Measured at End of 150 mΩ Cable

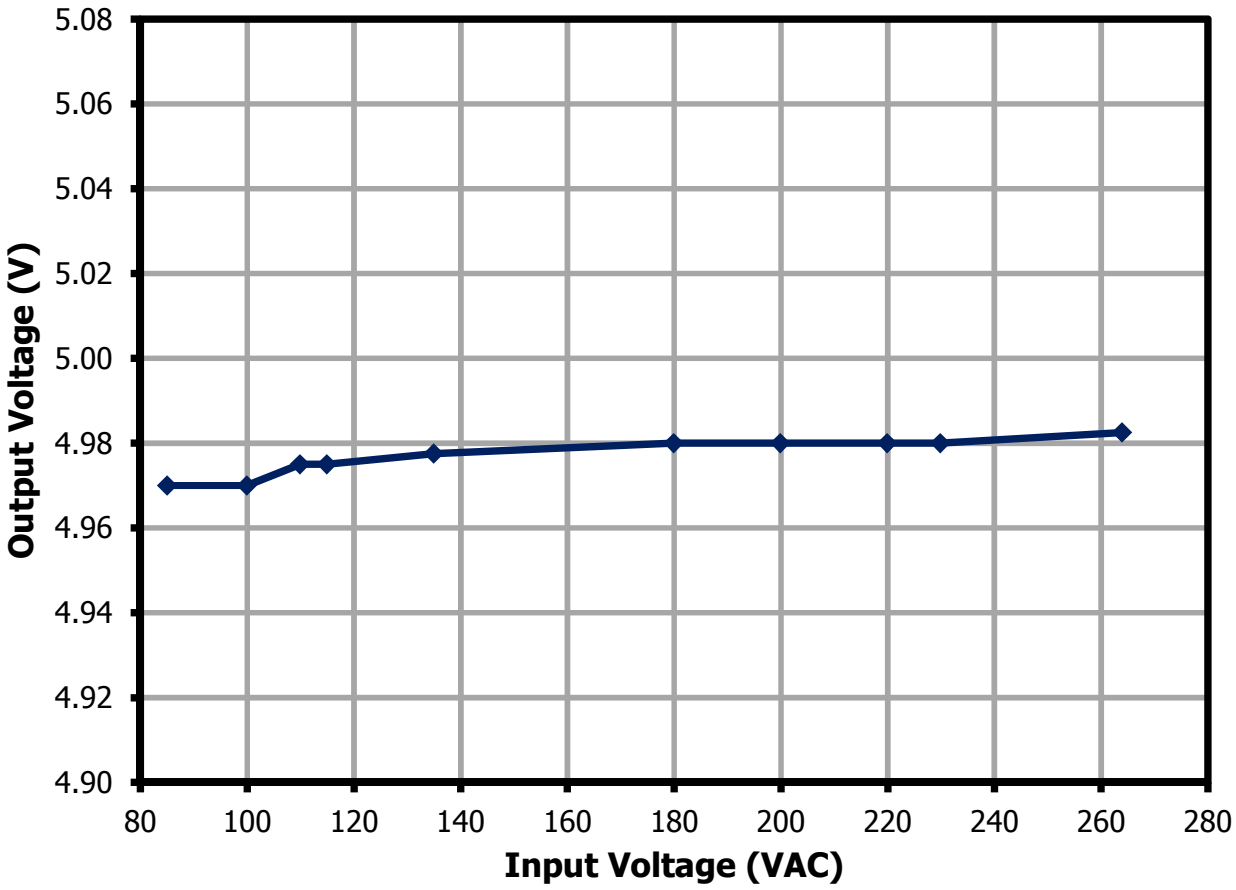

Figure 18 – Line Regulation.

12 Load Regulation

12.1 Measured at End of 150 mΩ Cable.

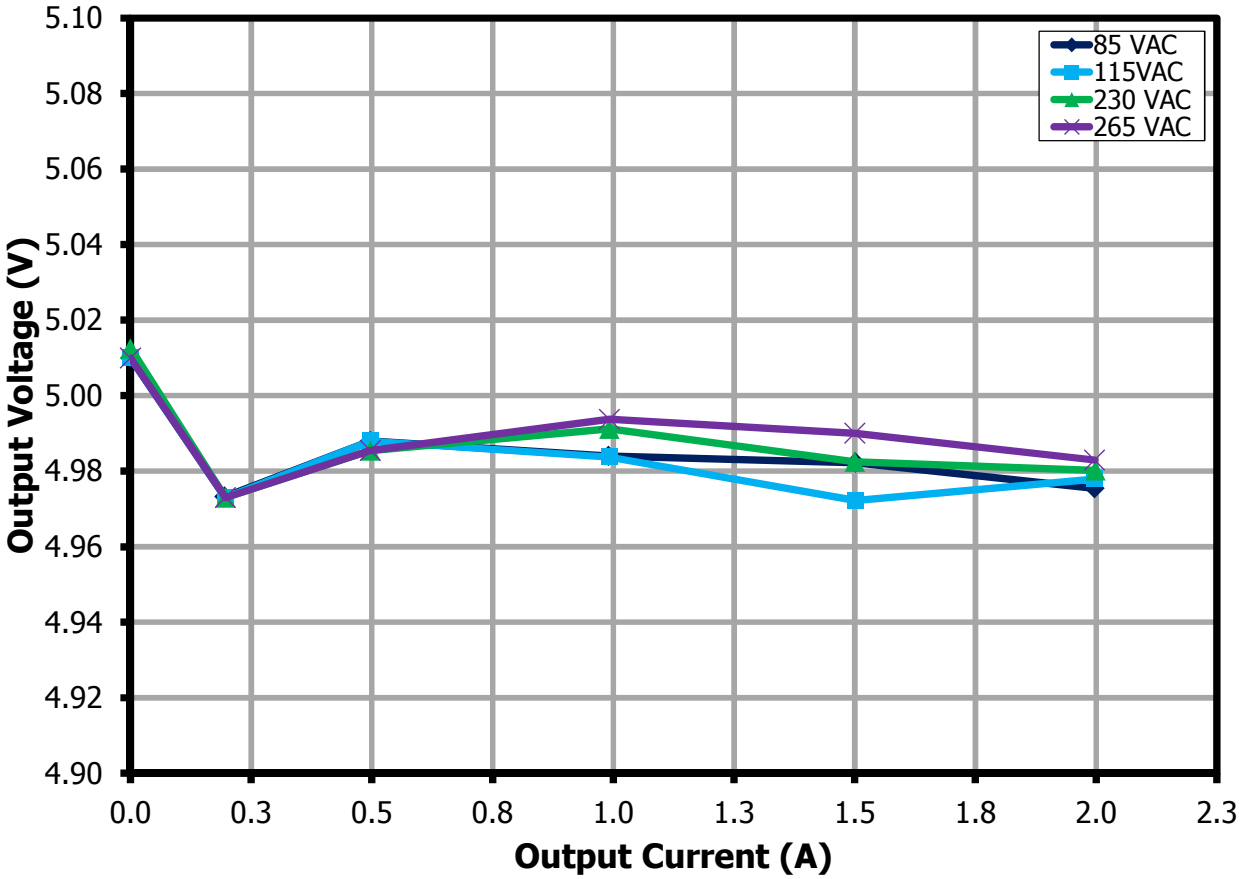

Figure 19 – Efficiency vs. Load (At End of Cable).

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13 Thermal Performance

13.1 Thermal Scan at Room Temperature

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Temperature was measured using thermal camera. Soak time at full load is 2 hours.

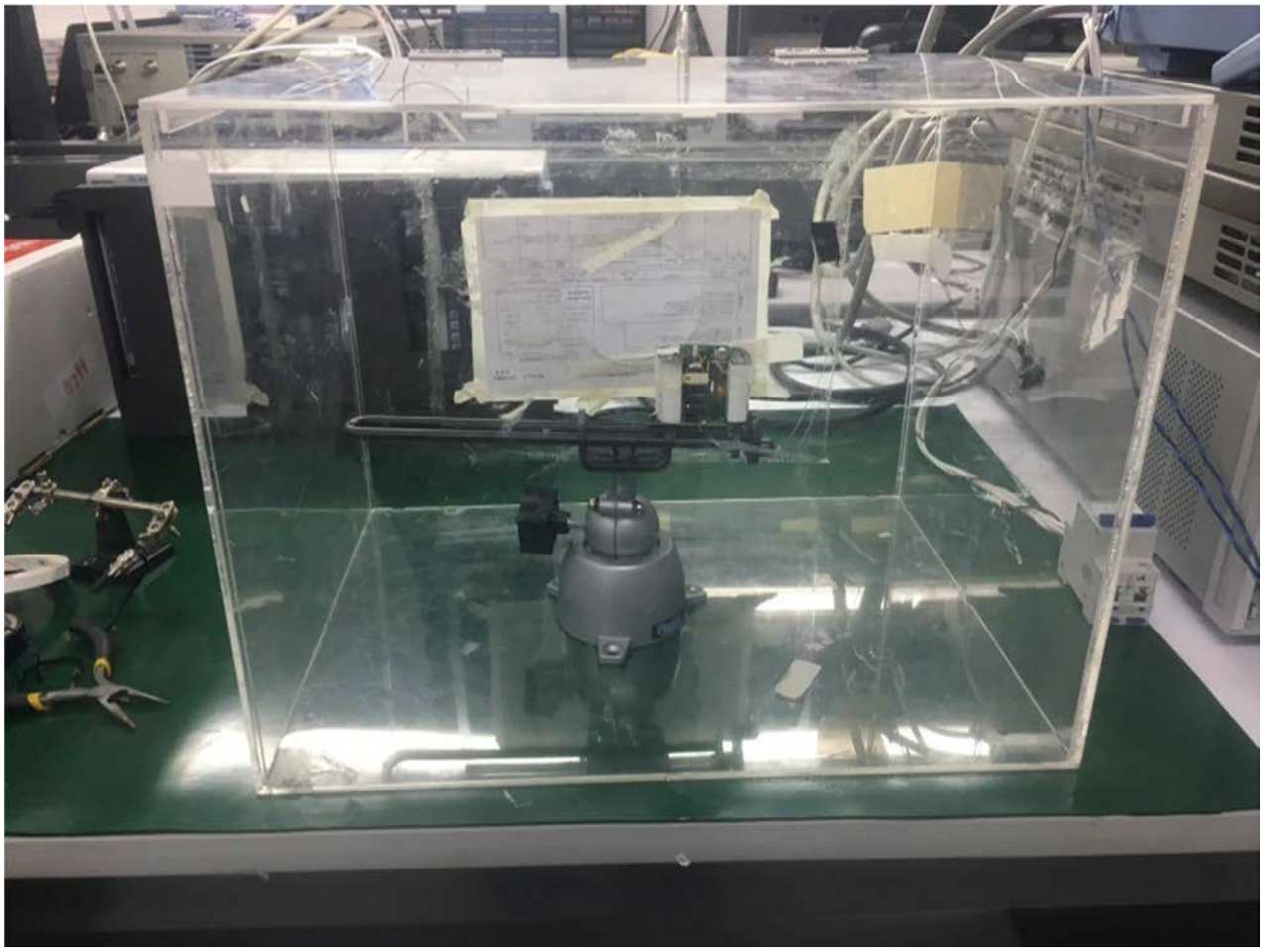

Figure 20 – Test Set-up.

13.2 85 VAC

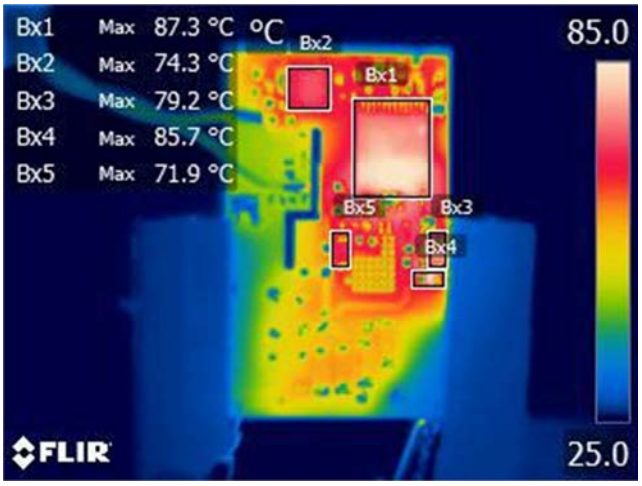

Figure 21 – 85 VAC, 2 A Load. Top Side.
Ambient = 26.1 ºC.

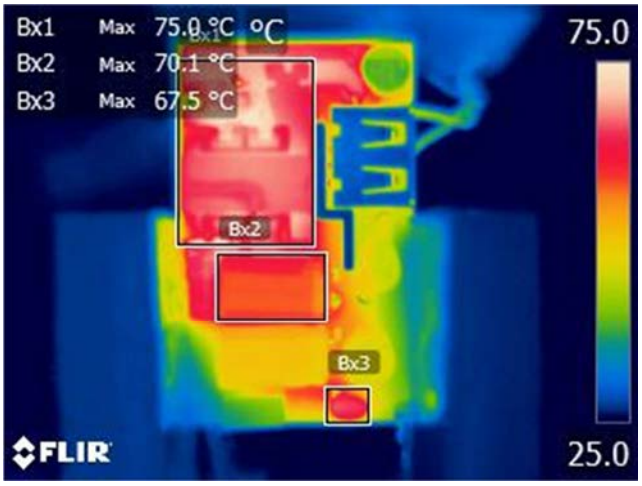

Figure 22 – 85 VAC, 2 A Load. Bottom Side.
Ambient = 26.1 ºC.

Component	Temperature (°C)
IC (U1)	87.3
SR FET (Q1)	74.3
Snubber Diode (D5)	79.2
Snubber Resistor (R2)	85.7
Bias Diode (D6)	71.9
Transformer (T1)	75.0
Input Capacitor (C2)	64.3
Thermistor (RT1)	67.5

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13.3 265 VAC

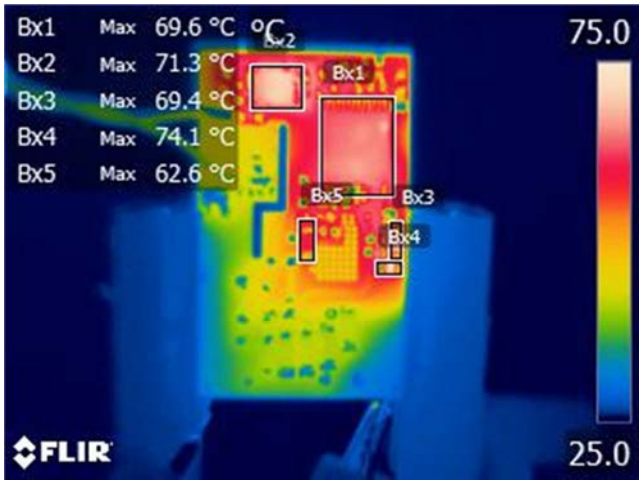

Figure 23 – 265 VAC, 2 A Load.
INN3162C (U1) = 75.0 ºC.
Ambient = 26.7 ºC.

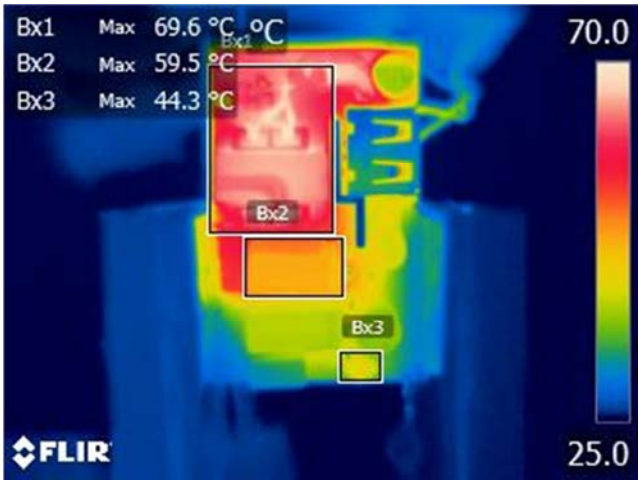

Figure 24 – 265 VAC, 2 A Load.
SRFET (Q1) = 71.3 ºC.
Ambient = 26.7 ºC.

Component	Temperature (°C)
IC (U1)	69.6
SR FET (Q1)	71.3
Snubber Diode (D5)	69.4
Snubber Resistor (R2)	74.1
Bias Diode (D6)	62.6
Transformer (T1)	69.6
Input Capacitor (C2)	59.5
Thermistor (RT1)	44.3

14 Thermal Performance at 70 °C

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Ambient temperature inside enclosure is 70 ºC. Temperature was measured using type T thermocouple. Soak time at full load is 1 hour and 30 minutes.

Figure 25 – Test Set-up.

Component		Temperature (°C)	
		85 VAC	265 VAC
INN3162C	U1	116.3	101.9
SR FET	Q1	103.1	101.1
Snubber Diode	D5	99.2	95.7
Snubber Resistor	R2	104.9	99.6
Bias Diode	D6	105.7	90.3
Transformer	T1	107.9	102.8
Input Capacitor	C2	97.3	78.7
Thermistor	RT1	93.1	89.6
Ambient	TAMBIENT	73.4	72.8

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15 Over Temperature Protection

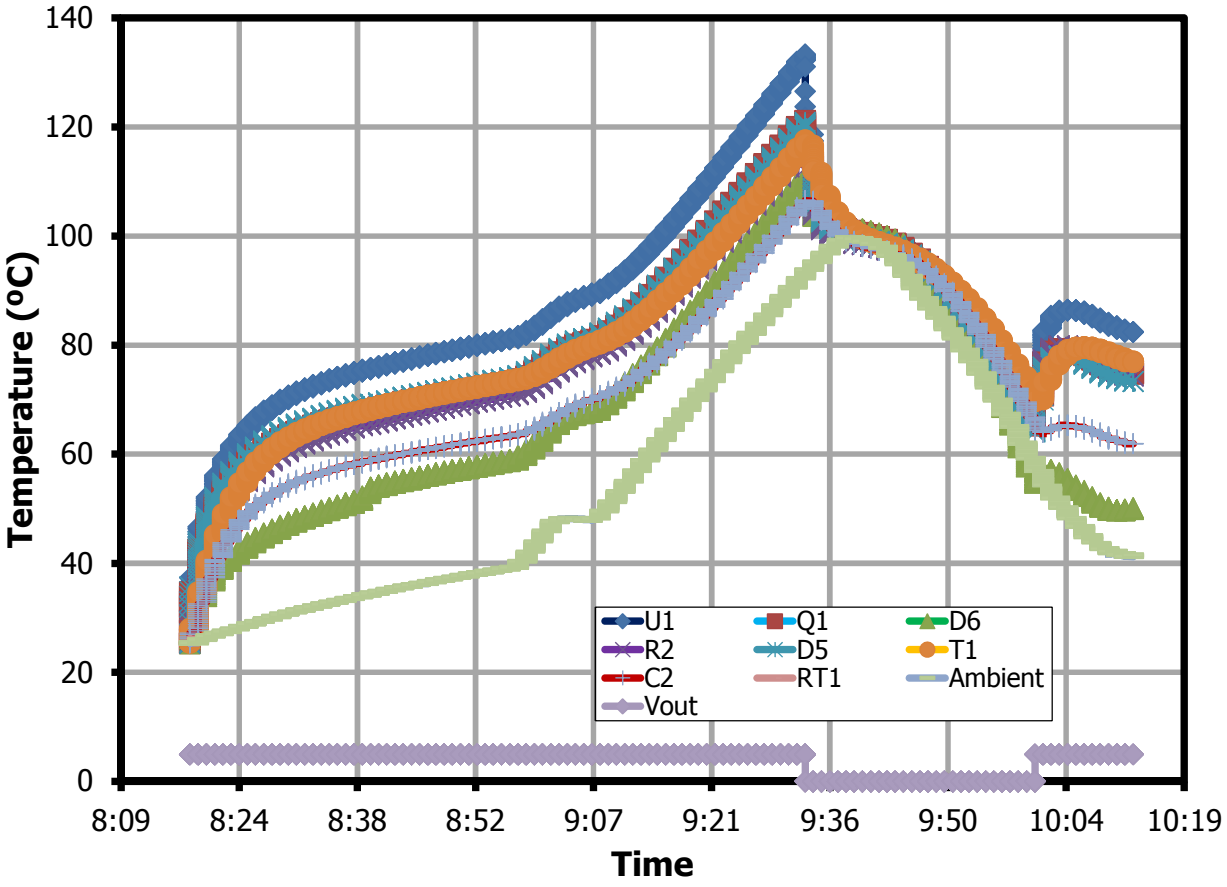

Figure 26 – 85 VAC Over Temperature Protection.

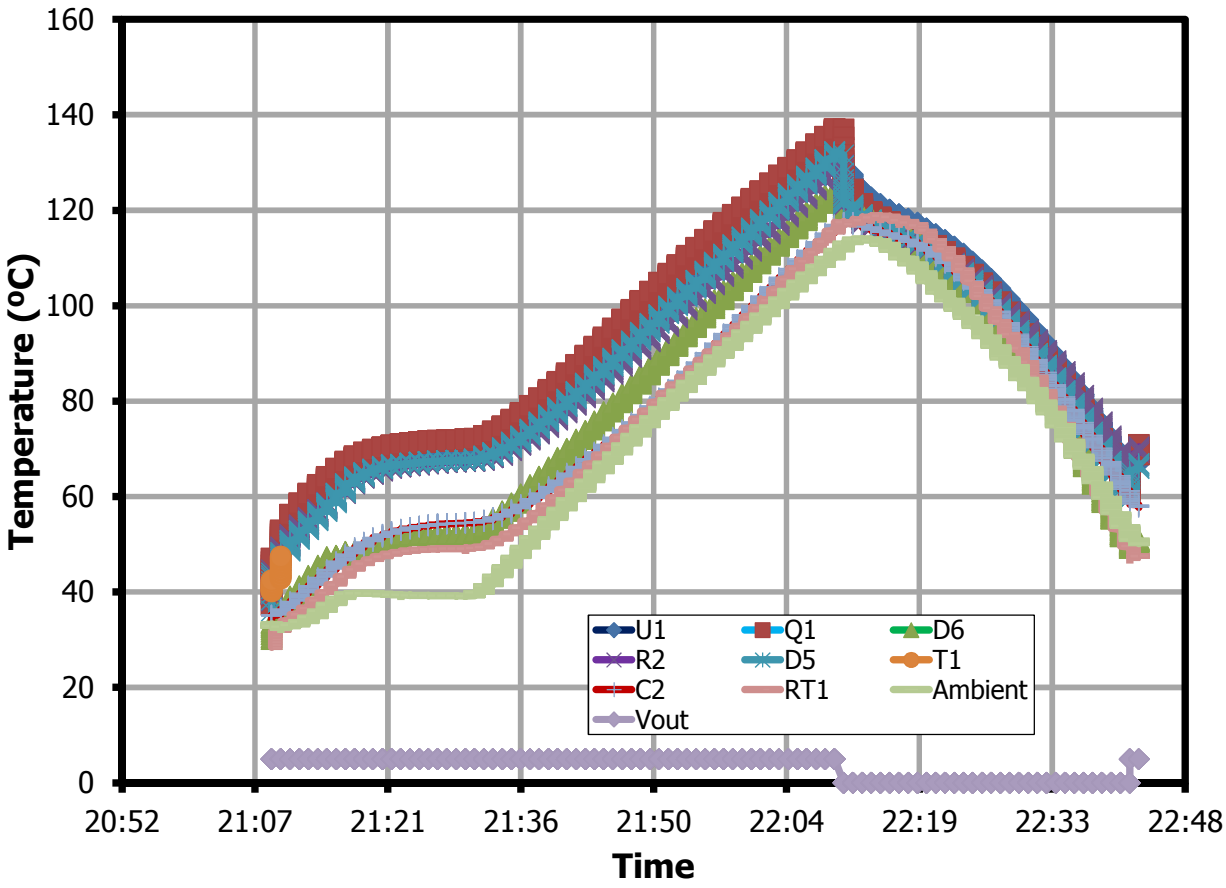

Figure 27 – 265 VAC Over Temperature Protection.

Component		Temperature (°C)	
		85 VAC	265 VAC
INN3162C	U1	133.3	135.1
SR FET	Q1	121.2	137
Snubber Diode	D5	110.9	124.2
Snubber Resistor	R2	117.2	129.6
Bias Diode	D6	120.8	132.3
Transformer	T1	117.5	134
Input Capacitor	C2	106.5	117.4
Thermistor	RT1	106.2	118.9
Ambient	TAMBIENT	99.6	114

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16 Test Waveforms

16.1 Line UV and OV at 2A CC Mode

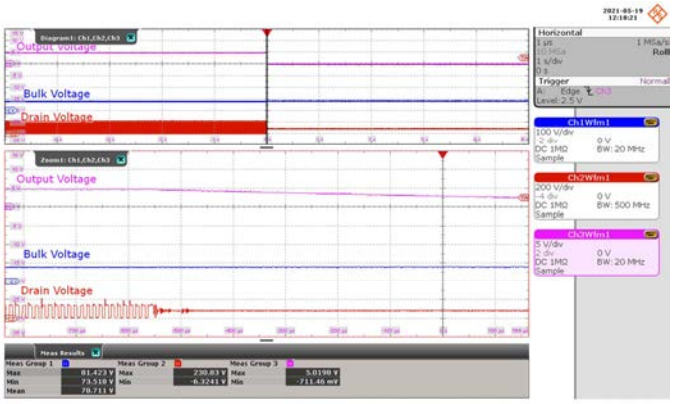

Figure 28 – Line Undervoltage (Vbulk$_{max}$ = 78.711 V)
CH1: V_{BULK}, 100 V / div., 1 s / div.
CH2: V_{DS}, 200 V / div., 1 s / div.
CH3: V_{OUT}, 5 V / div., 1 s / div.

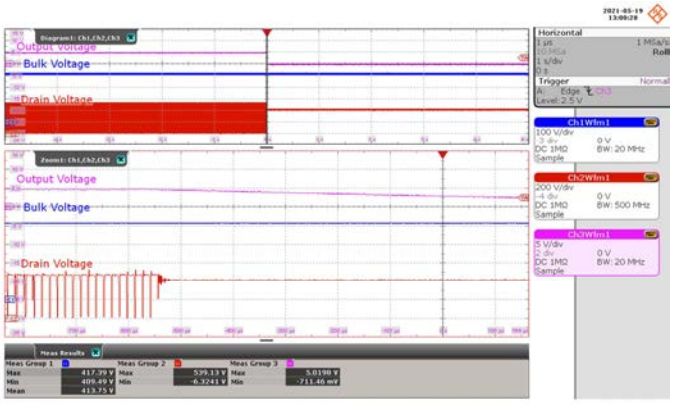

Figure 29 – Line Overvoltage (Vbulk$_{max}$ = 413.75 V)
CH1: V_{BULK}, 100 V / div., 1 s / div.
CH2: V_{DS}, 200 V / div., 1 s / div.
CH3: V_{OUT}, 5 V / div., 1 s / div.

16.2 Load Transient Response

16.3 0% - 100% Load Condition (Measured at End of 150 mΩ Cable)

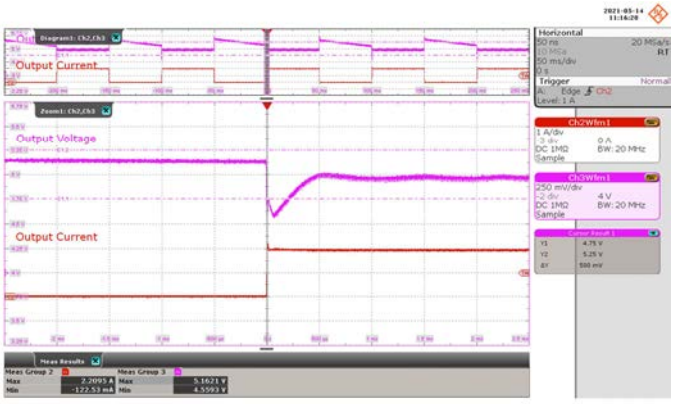

Figure 30 – 85 VAC 60 Hz, 0% - 100% Load Change.
Vo$_{max}$ = 5.1621 V Vo$_{min}$ = 4.5593 V
CH2: I_{OUT}, 1 A / div. , 50 ms/ div
CH3: V_{OUT}, 250 mV / div., 50 ms/ div.
Zoom: 500 µs / div.

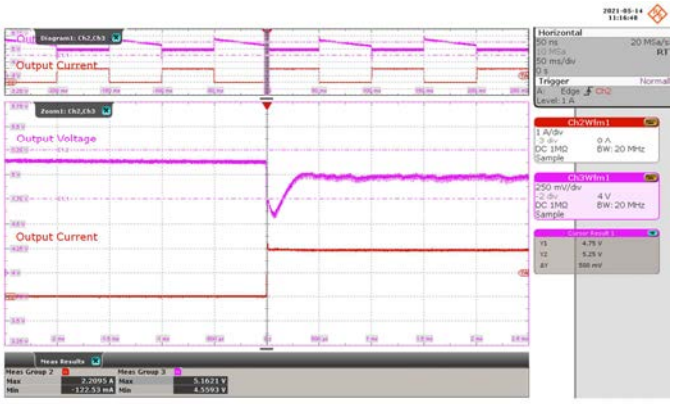

Figure 31 – 265 VAC 50 Hz, 0% - 100% Load Change.
Vo$_{max}$ = 5.1621 V, Vo$_{min}$ = 4.5593 V
CH2: I_{OUT}, 1 A / div. , 50 ms/ div
CH3: V_{OUT}, 250 mV / div., 50 ms/ div.
Zoom: 500 µs / div.

16.4 Output OVP

16.4.1 0% Load Condition

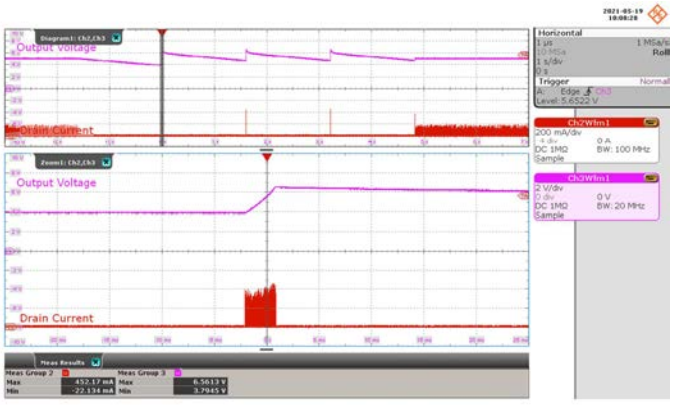

Figure 32 – Maximum Output Voltage (6.5613 V_{MAX}).
85 VAC Input.
CH2: I_{DS}, 200 mA / div., 1 s / div.
CH3: V_{OUT}, 2 V / div., 1 s / div.
Zoom: 5 ms / div.

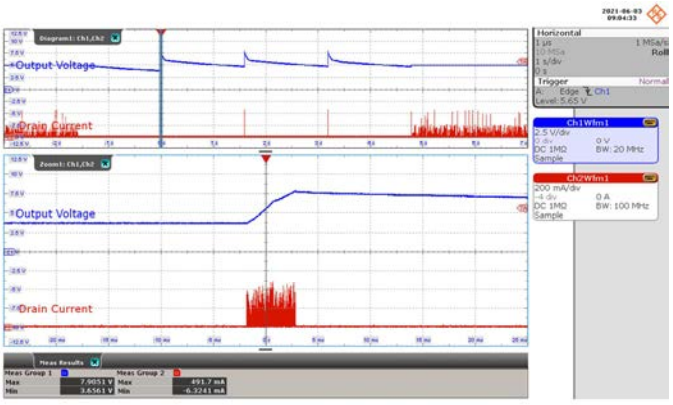

Figure 33 – Maximum Output Voltage (7.9051 V_{MAX}).
265 VAC Input.
CH1: V_{OUT}, 2.5 V / div., 1 s / div.
CH2: I_{DS}, 200 mA / div., 1 s / div.
Zoom: 5 ms / div.

16.4.2 100% Load Condition

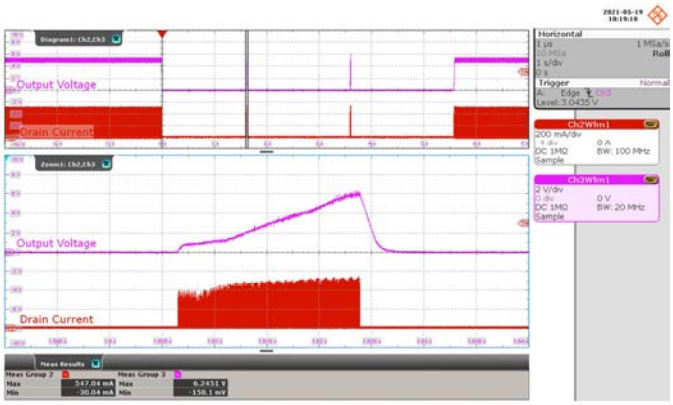

Figure 34 – Maximum Output Voltage (6.2451 V_{MAX}).
85 VAC Input.
CH2: I_{DS}, 200 mA / div., 1 s / div.
CH3: V_{OUT}, 2 V / div., 1 s / div.
Zoom: 5 ms / div.

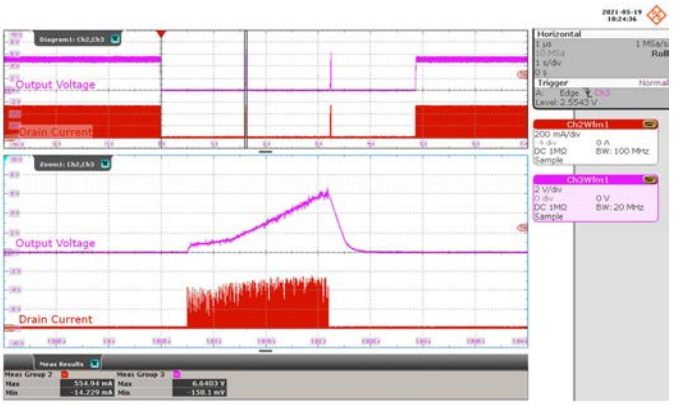

Figure 35 – Maximum Output Voltage (6.6403 V_{MAX}).
265 VAC Input.
CH2: I_{DS}, 200 mA / div., 1 s / div.
CH3: V_{OUT}, 2 V / div., 1 s / div.
Zoom: 5 ms / div.

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16.5 Output Voltage at Start-up

Measured on the USB socket.

16.5.1.1 100% Load

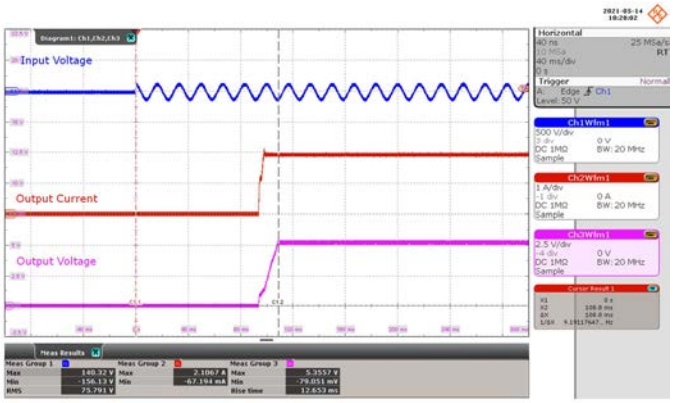

Figure 36 – 85 VAC 60 Hz, Full Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.3557 V
Output Voltage, rise time= 12.653 ms
Start- up time= 108.8 ms

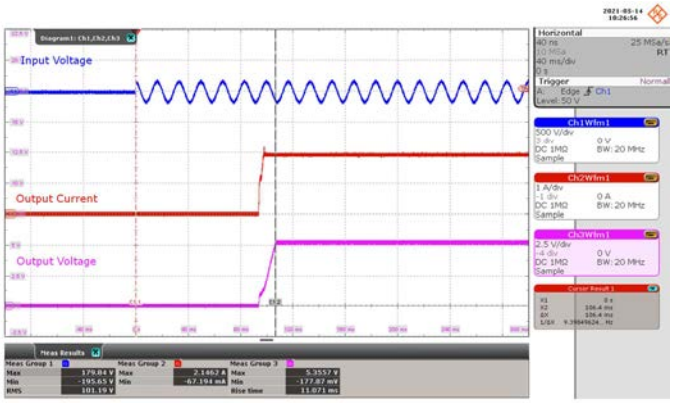

Figure 37 – 115 VAC 60 Hz, Full Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.3557 V
Output Voltage, rise time= 11.071 ms
Start- up time= 106.4 ms

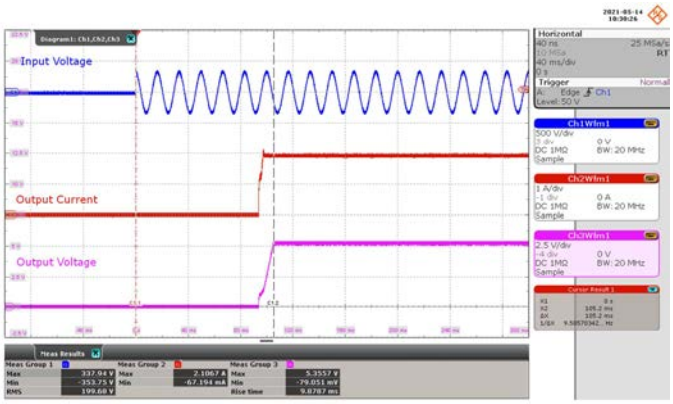

Figure 38 – 230 VAC 50 Hz, Full Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.3557 V
Output Voltage, rise time= 9.8787 ms
Start- up time= 105.2 ms

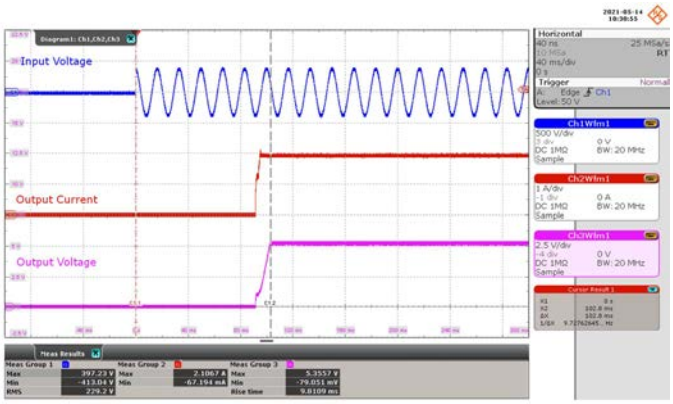

Figure 39 – 265 VAC 50 Hz, Full Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.3557 V
Output Voltage, rise time= 9.8109 ms
Start- up time= 102.8 ms

16.5.1.2 0% Load

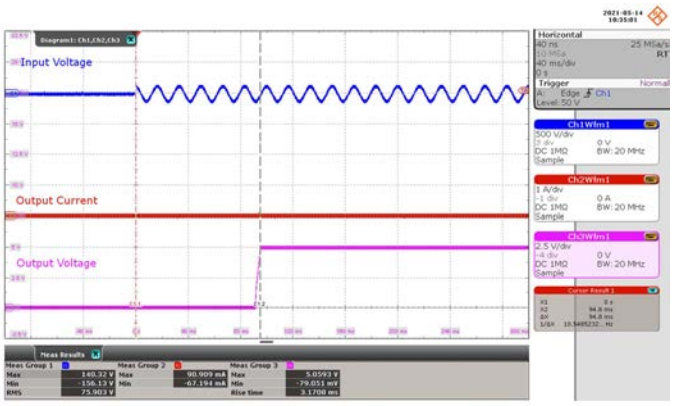

Figure 40 – 85 VAC 60 Hz, No-Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.0593 V
Output Voltage, rise time= 3.1708 ms
Start- up time= 94.8 ms

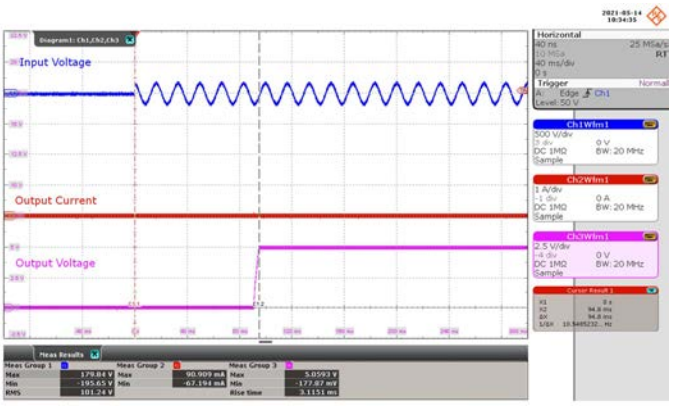

Figure 41 – 115 VAC 60 Hz, No-Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.0593 V
Output Voltage, rise time= 3.1151 ms
Start- up time= 94.8 ms

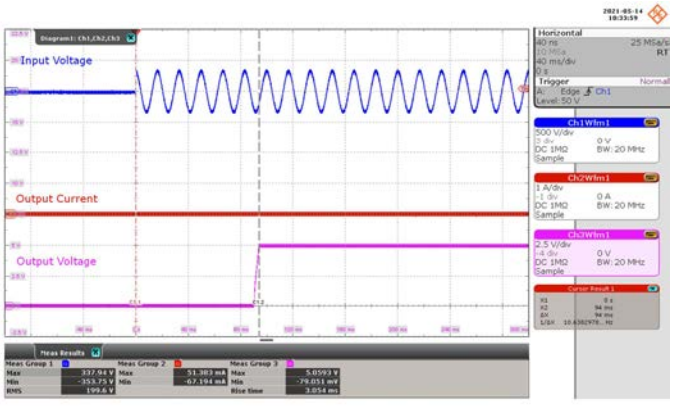

Figure 42 – 230 VAC 50 Hz, No-Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.0593 V
Output Voltage, rise time= 3.054 ms
Start- up time= 94 ms

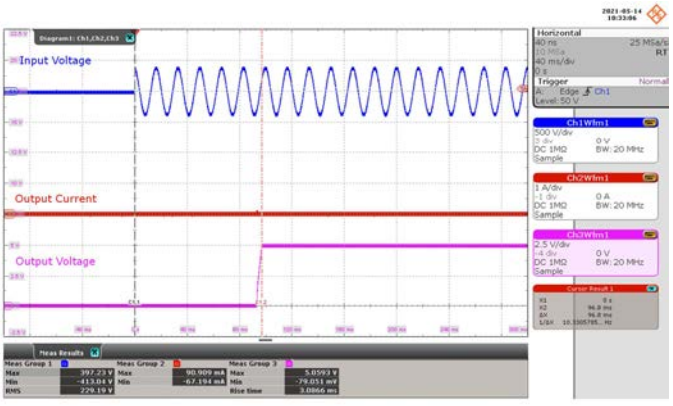

Figure 43 – 265 VAC 50 Hz, No-Load Start-up.
CH1: V_{IN}, 500 V / div., 40 ms/ div.
CH2: I_{OUT}, 1 A / div., 40 ms / div.
CH3: V_{OUT}, 2.5 V / div., 40 ms / div.
Output Voltage, max= 5.0593 V
Output Voltage, rise time= 3.0866 ms
Start- up time= 96.8 ms

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16.6 Switching Waveforms

16.6.1 Drain Voltage at Normal Operation

16.6.1.1 100% Load

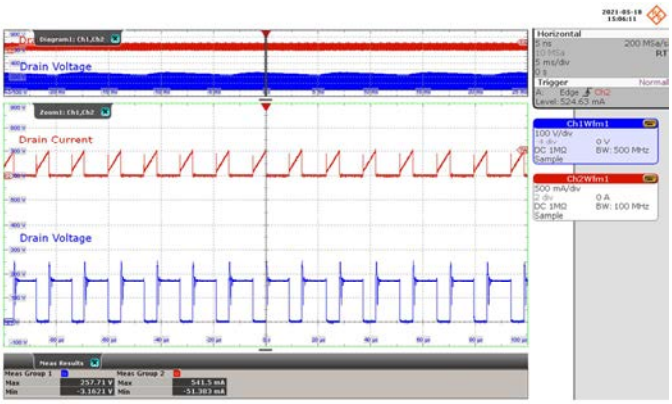

Figure 44 – 85 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 257.71 V
$I_{DS(MAX)}$ = 541.5 mA

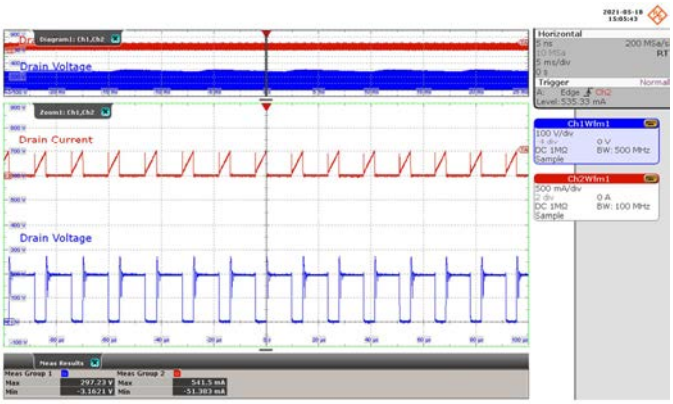

Figure 45 – 115 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 297.23 V
$I_{DS(MAX)}$ = 541.5 mA

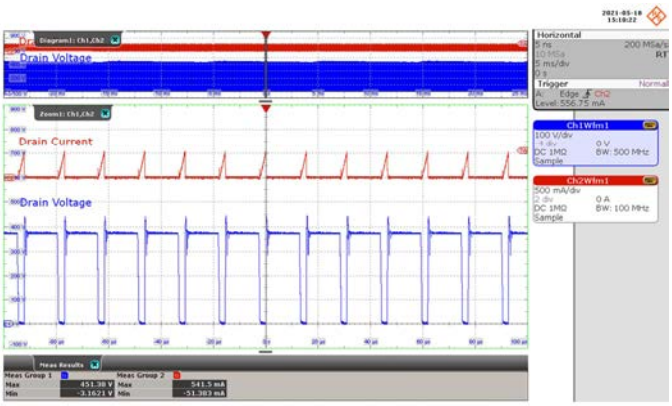

Figure 46 – 230 VAC 50 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 451.38 V
$I_{DS(MAX)}$ = 541.5 mA

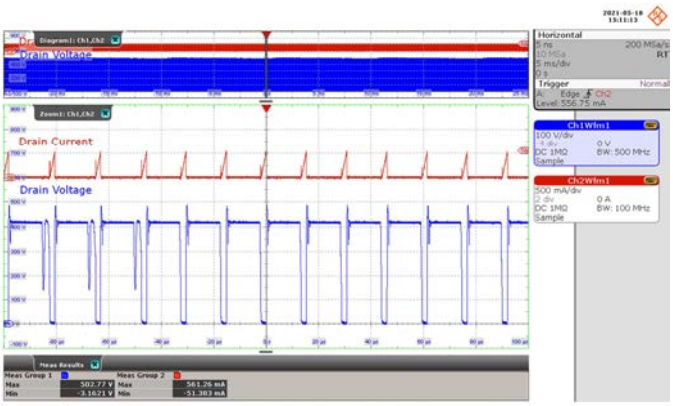

Figure 47– 265 VAC 50 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 502.77 V
$I_{DS(MAX)}$ = 561.26 mA

16.6.2 Drain Voltage at Start-up Operation

16.6.2.1 100% Load

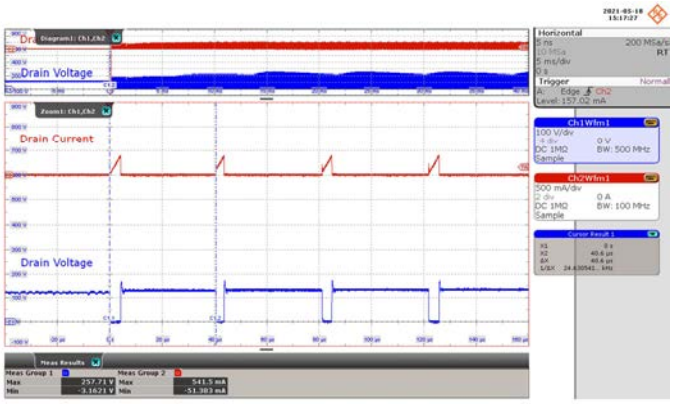

Figure 48 – 85 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 257.71 V
$I_{DS(MAX)}$ = 541.5 mA
Start-up switching = 24.6305 kHz

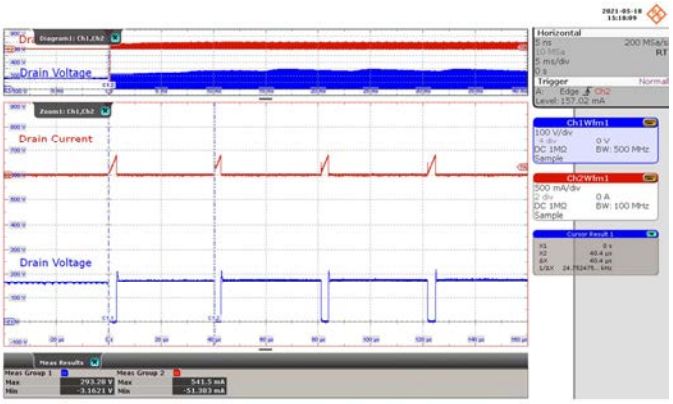

Figure 49 – 115 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 293.28 V
$I_{DS(MAX)}$ = 541.5 mA
Start-up switching = 24.7525 kHz

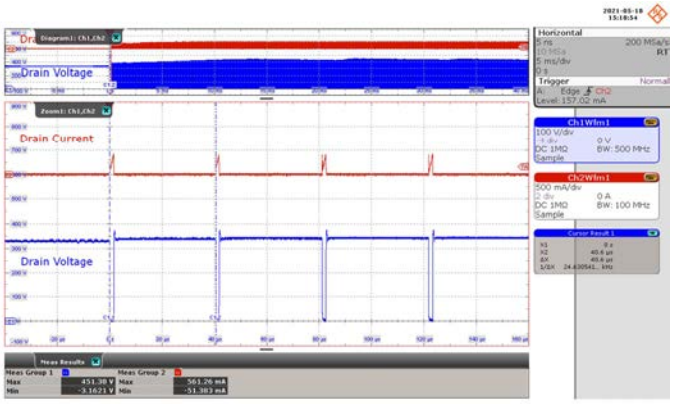

Figure 50 – 230 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 451.38 V
$I_{DS(MAX)}$ = 561.26 mA
Start-up switching = 24.6305 kHz

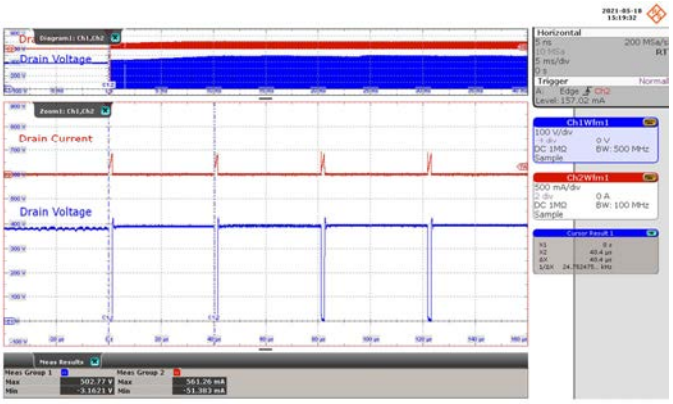

Figure 51 – 265 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 5 ms/ div.
CH2: I_{DS}, 500 mA / div., 5 ms / div.
Zoom: 20 µs/ div.
$V_{DS(MAX)}$ = 502.77 V
$I_{DS(MAX)}$ = 561.26 mA
Start-up switching = 24.7525 kHz

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16.6.3 SR FET Waveforms

16.6.3.1 SRFET at Normal Operation

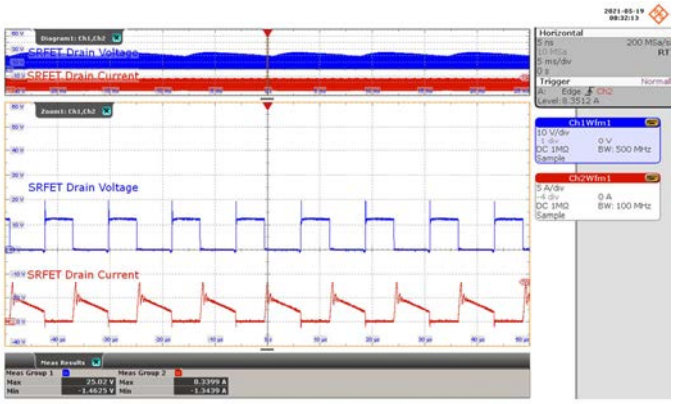

Figure 52 – 85 VAC 60 Hz, Full Load Normal.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 10 µs/ div.
$V_{DS(MAX)}$ = 25.02 V
$I_{DS(MAX)}$ = 8.3399 A

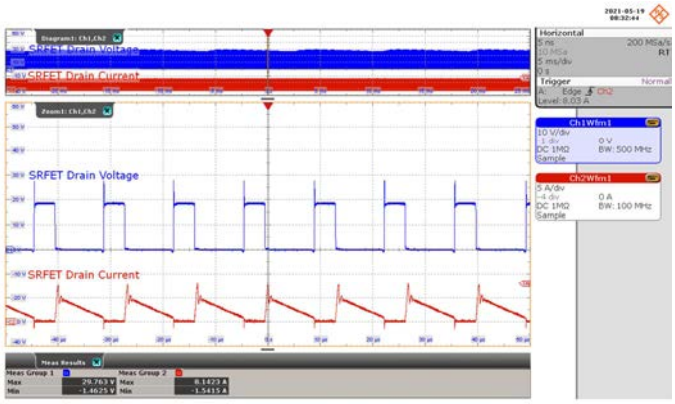

Figure 53 – 115 VAC 60 Hz, Full Load Normal.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 10 µs/ div.
$V_{DS(MAX)}$ = 29.763 V
$I_{DS(MAX)}$ = 8.1423 A

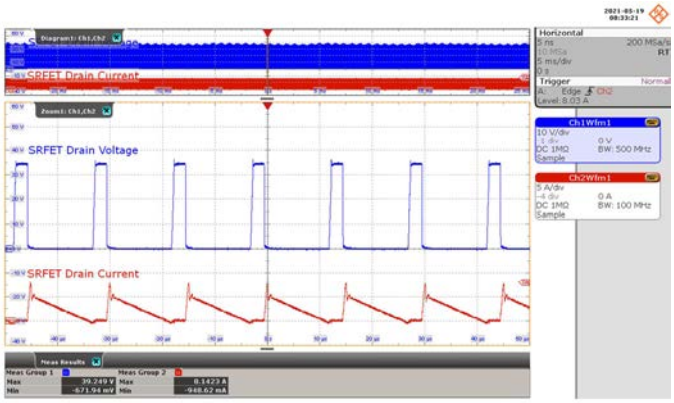

Figure 54 – 230 VAC 50 Hz, Full Load Normal.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 10 µs/ div.
$V_{DS(MAX)}$ = 39.249 V
$I_{DS(MAX)}$ = 8.1423 A

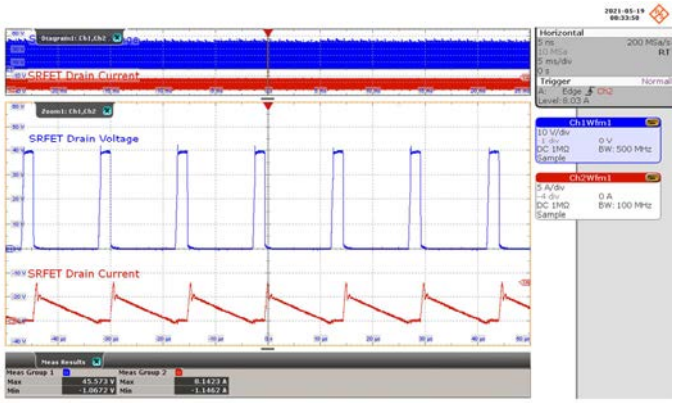

Figure 55 – 265 VAC 50 Hz, Full Load Normal.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 10 µs/ div.
$V_{DS(MAX)}$ = 45.573 V
$I_{DS(MAX)}$ = 8.1423 A

16.6.3.2 SR FET at Start-up Operation

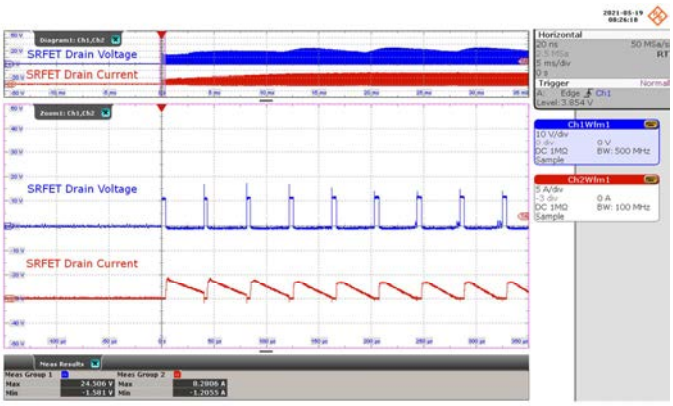

Figure 56 – 85 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 50 µs/ div.
$V_{DS(MAX)}$ = 24.506 V
$I_{DS(MAX)}$ = 8.2806 A

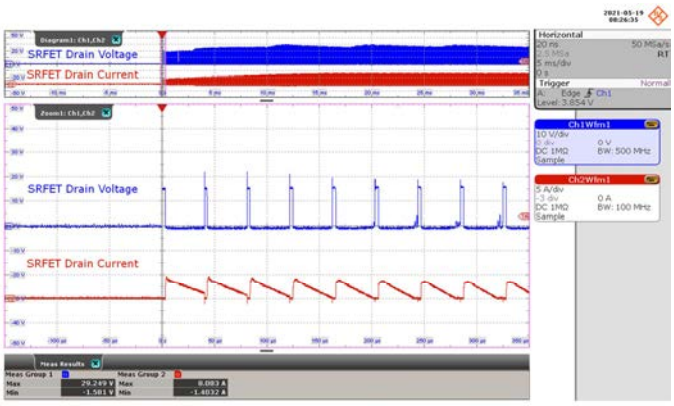

Figure 57 – 115 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 50 µs/ div.
$V_{DS(MAX)}$ = 29.249 V
$I_{DS(MAX)}$ = 8.083 A

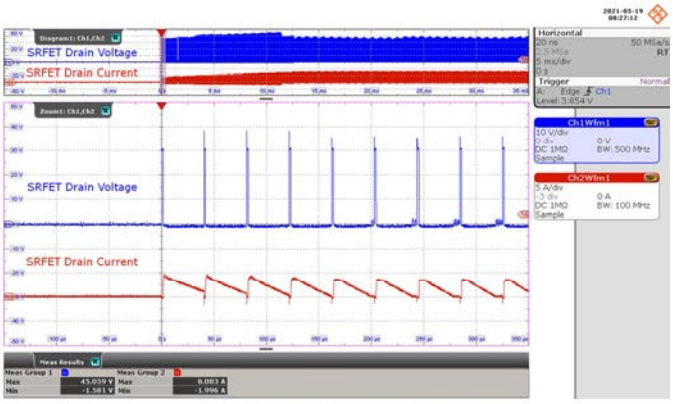

Figure 58 – 230 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 10 µs/ div.
$V_{DS(MAX)}$ = 45.059 V
$I_{DS(MAX)}$ = 8.083 A

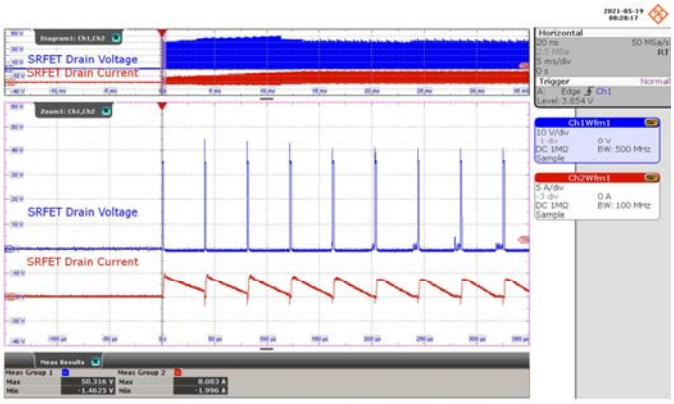

Figure 59 – 265 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 10 V / div., 5 ms/ div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom: 10 µs/ div.
$V_{DS(MAX)}$ = 50.316 V
$I_{DS(MAX)}$ = 8.083 A

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16.7 Brown-in / Brown-out Test

No abnormal overheating nor voltage overshoot / undershoot was observed during and after 0.1 V / s brown-in and brown-out test.

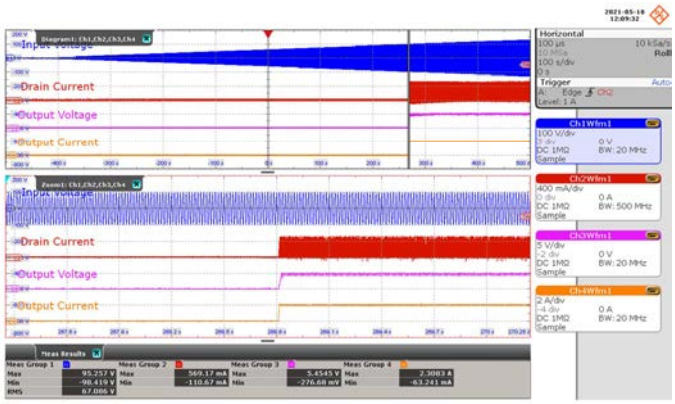

Figure 60 – Brown-in Test.
0 to 90 VAC 0.1 V / s.
CH1: V_{IN}, 100 V / div., 100 s /div.
CH2: I_{DS}, 400 mA / div., 100 s / div.
CH3: V_{OUT}, 5 V / div., 100 s / div.
CH4: I_{OUT}, 2 A / div., 100 s / div.
Zoom: 300 ms / div.
Drain current, max= 569.17 mA
Brown- in voltage, rms= 67.086 V

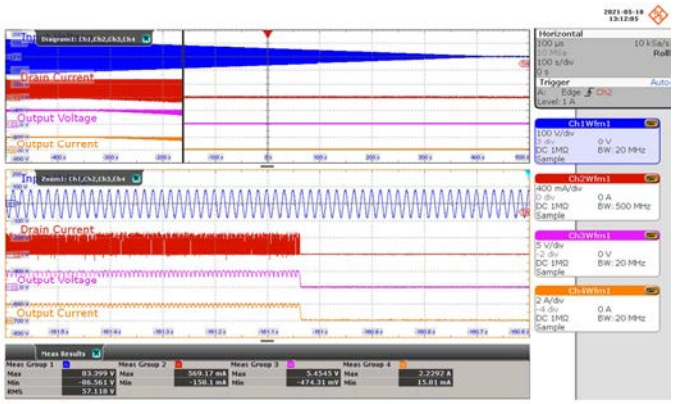

Figure 61 – Brown-out Test.
90 to 0 VAC at 0.1 V / s.
CH1: V_{IN}, 100 V / div., 100 s /div.
CH2: I_{DS}, 400 mA / div., 100 s / div.
CH3: V_{OUT}, 5 V / div., 100 s / div.
CH4: I_{OUT}, 2 A / div., 100 s / div.
Zoom: 100 ms / div.
Drain current, max= 569.17 mA
Brown- out voltage, rms= 57.118 V

16.8 2 A CC mode Start-up Test at 85 VAC Input

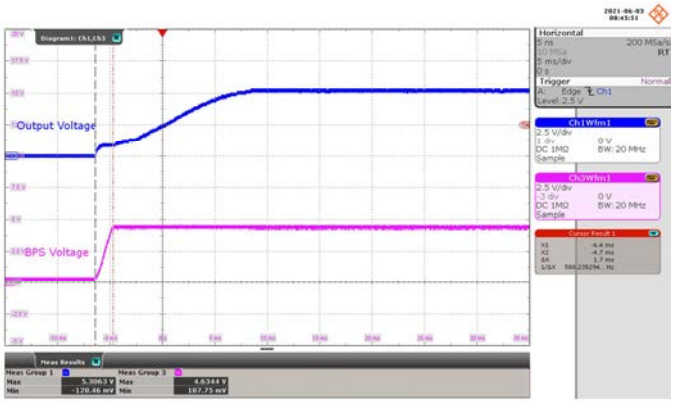

Figure 62 – BPS Voltage Waveform During Start-up .
CH1: V_{BPS}, 2.5 V / div., 5 ms / div.
CH3: V_{OUT}, 2.5 V / div., 5 ms / div.

16.9 Output Ripple Measurements

16.9.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

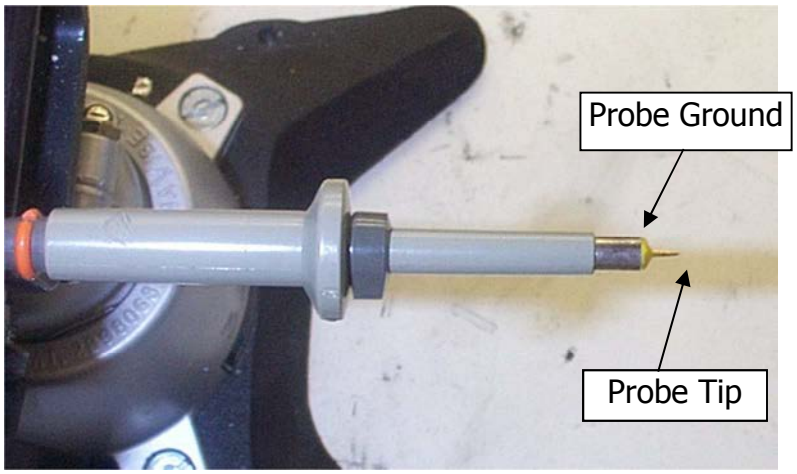

Figure 63 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

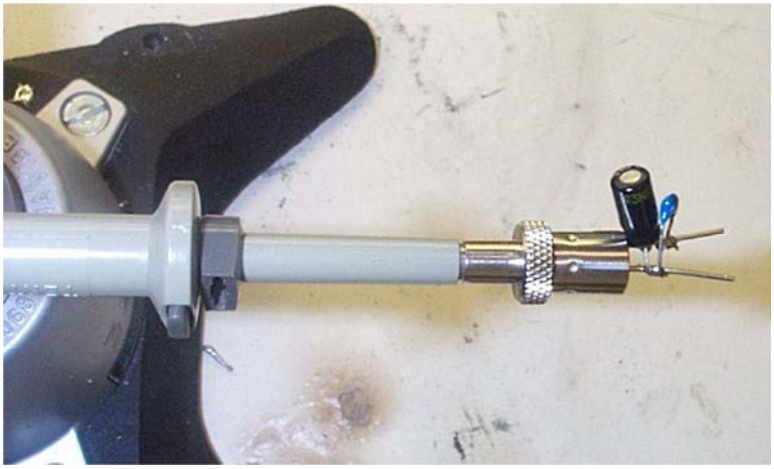

Figure 64 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

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16.9.2 Measurement Results

Measured at the end of 150 mΩ cable.

16.9.2.1 100% Load Condition

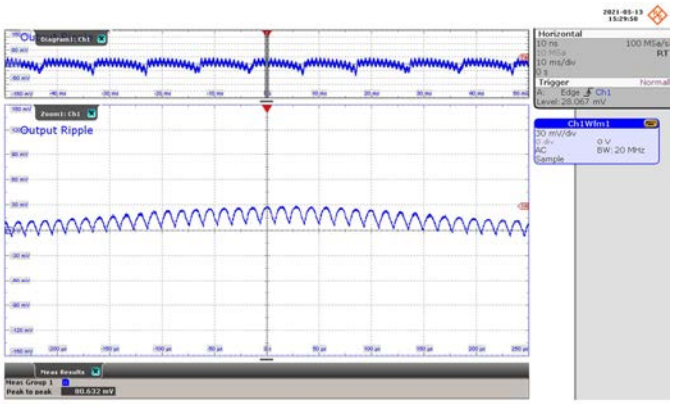

Figure 65 – 85 VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 80.632 mV

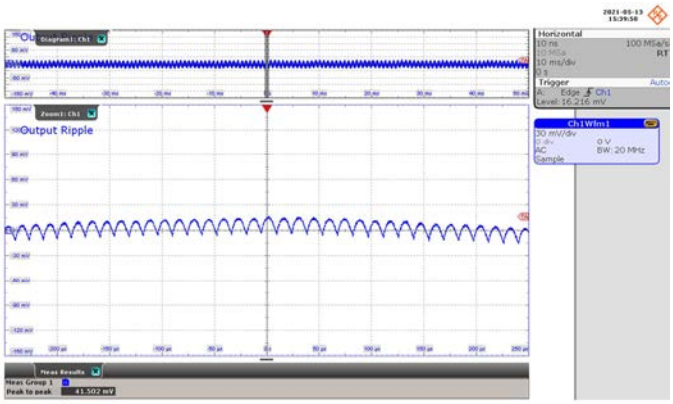

Figure 66 – 115 VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 41.502 mV

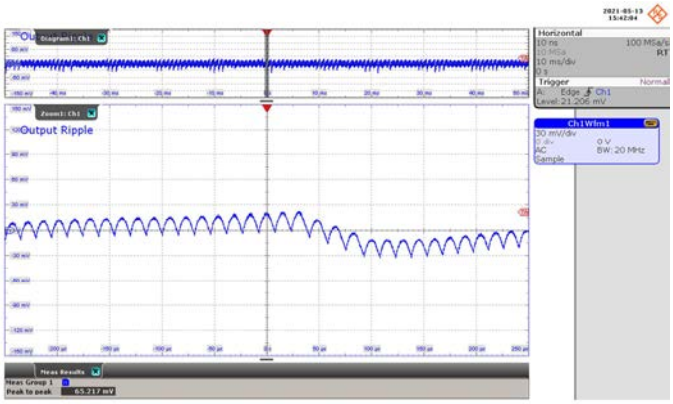

Figure 67 – 230VAC 50 Hz, 100% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 65.217 mV

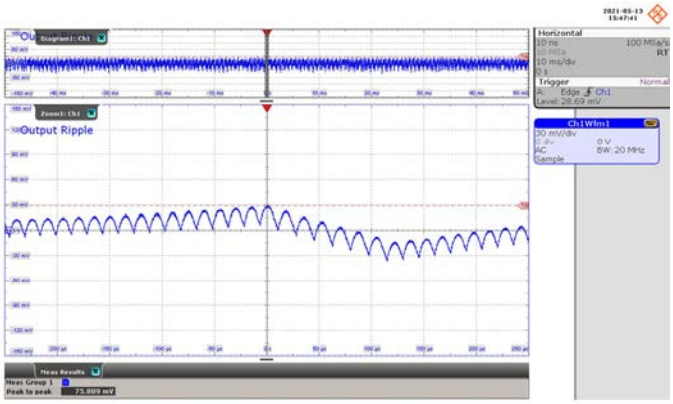

Figure 68 – 265VAC 50 Hz, 100% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 75.889 mV

16.9.2.2 75% Load Condition

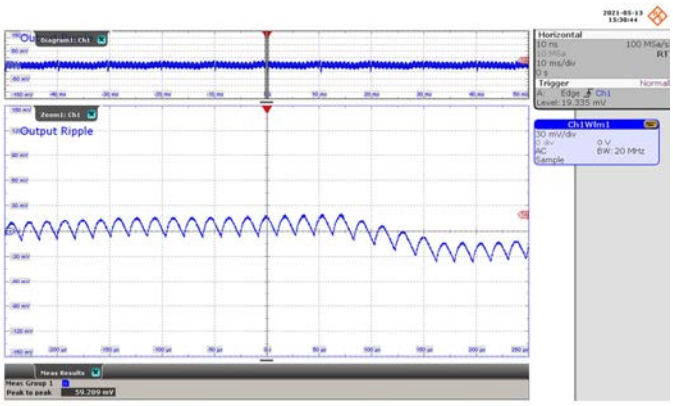

Figure 69 – 85 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 59.289 mV

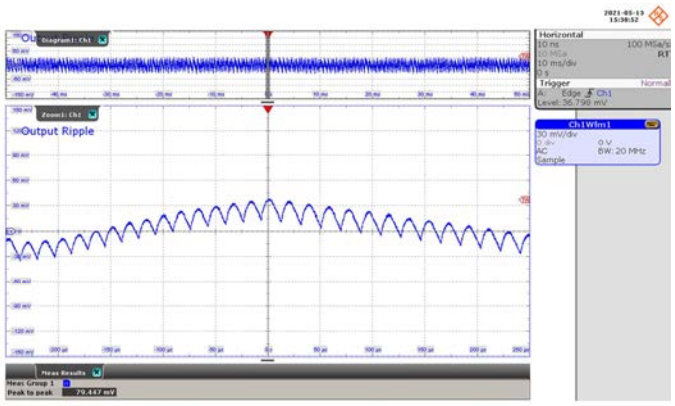

Figure 70 – 115 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 79.417 mV

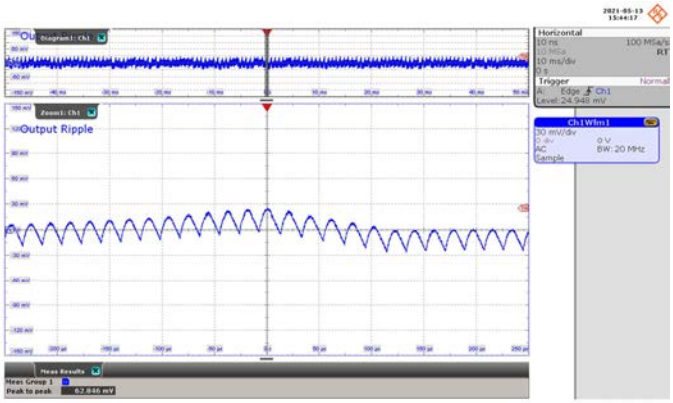

Figure 71 – 230 VAC 50 Hz, 75% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 62.846 mV

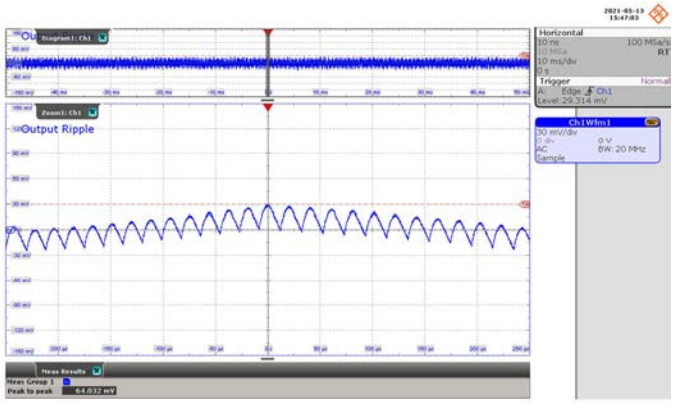

Figure 72 – 265 VAC 50 Hz, 75% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 64.032 mV

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16.9.2.3 50% Load Condition

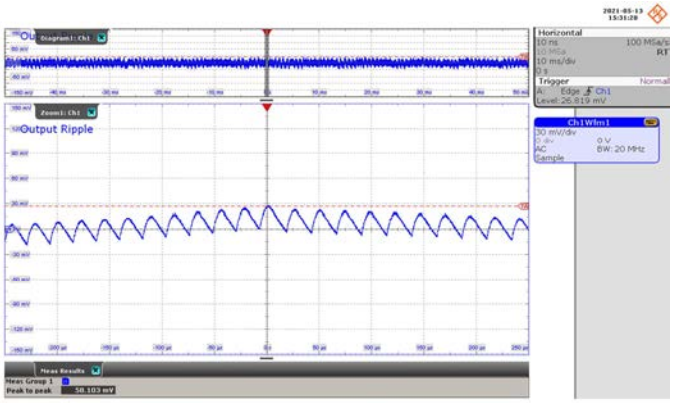

Figure 73 – 85 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 58.103 mV

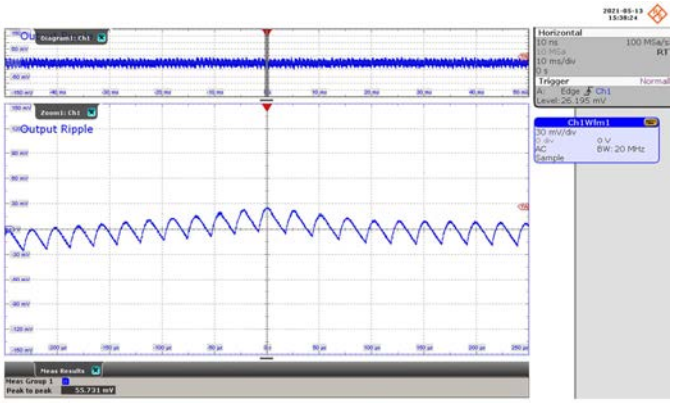

Figure 74 – 115 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 55.731 mV

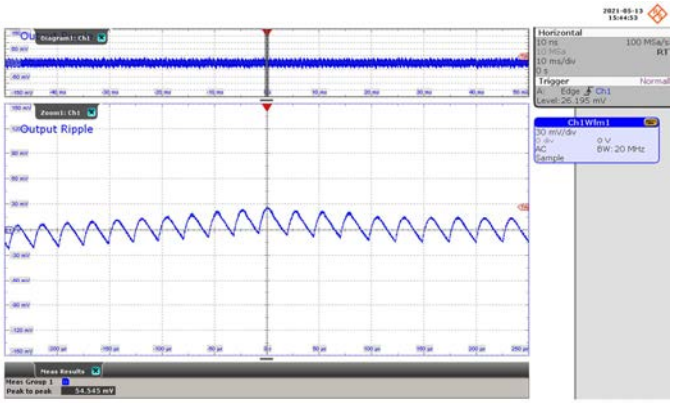

Figure 75 – 230 VAC 50 Hz, 50% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 54.545 mV

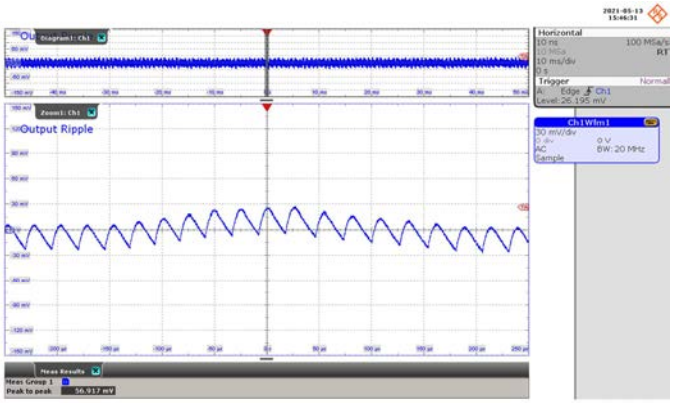

Figure 76 – 265 VAC 50 Hz, 50% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 56.917 mV

16.9.2.4 25% Load Condition

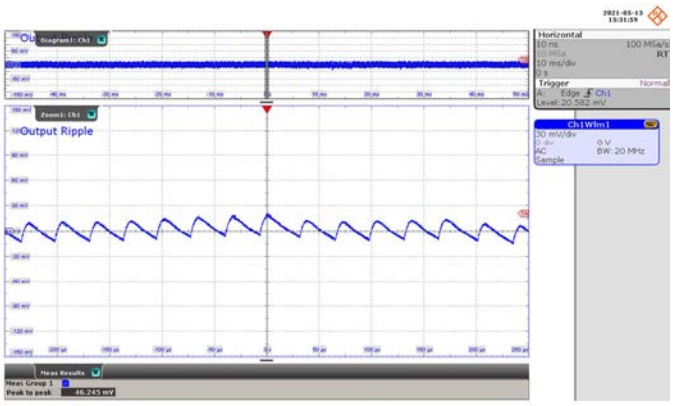

Figure 77 – 85 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 46.245 mV

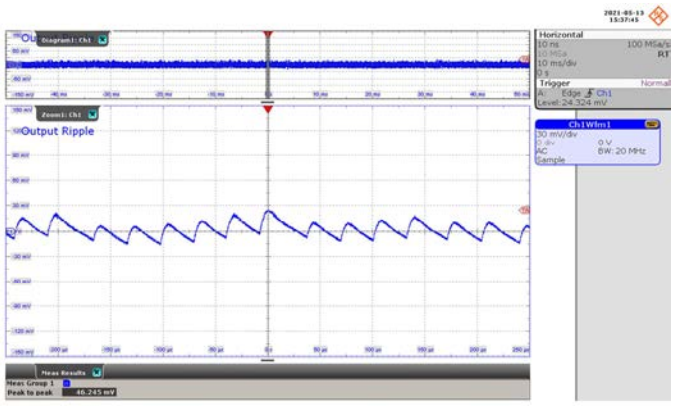

Figure 78 – 115 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 46.245 mV

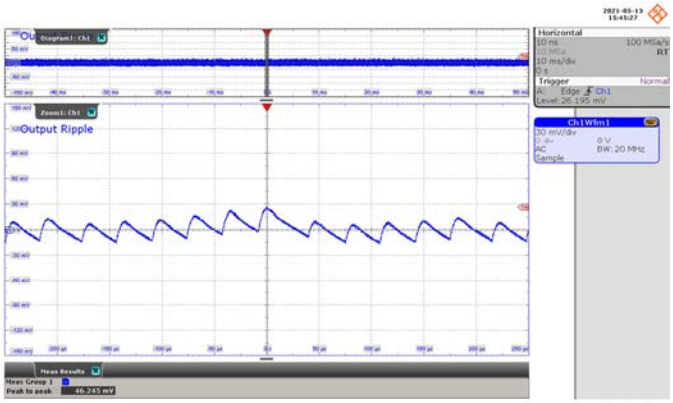

Figure 79 – 230 VAC 50 Hz, 25% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 46.425 mV

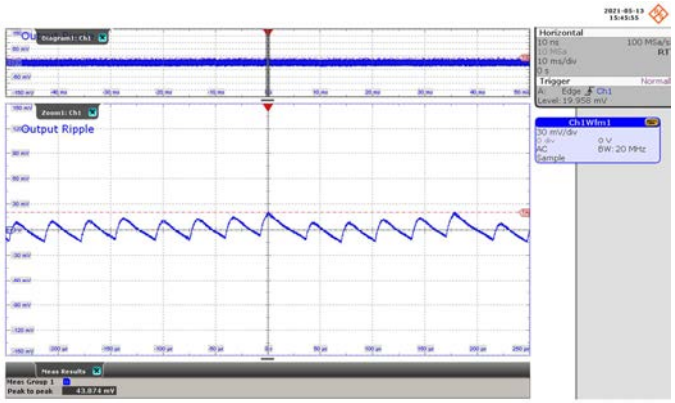

Figure 80 – 265 VAC 50 Hz, 25% Load.
CH1: V_{OUT}, 30 mV / div., 10 ms / div.
Zoom: 50 µs / div.
$V_{OUT(PK-PK)}$ = 43.874 mV

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17 Conductive EMI

17.1 Test Set-up

Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. Full Load with input voltage set at 230 VAC 50 Hz and 115 VAC.

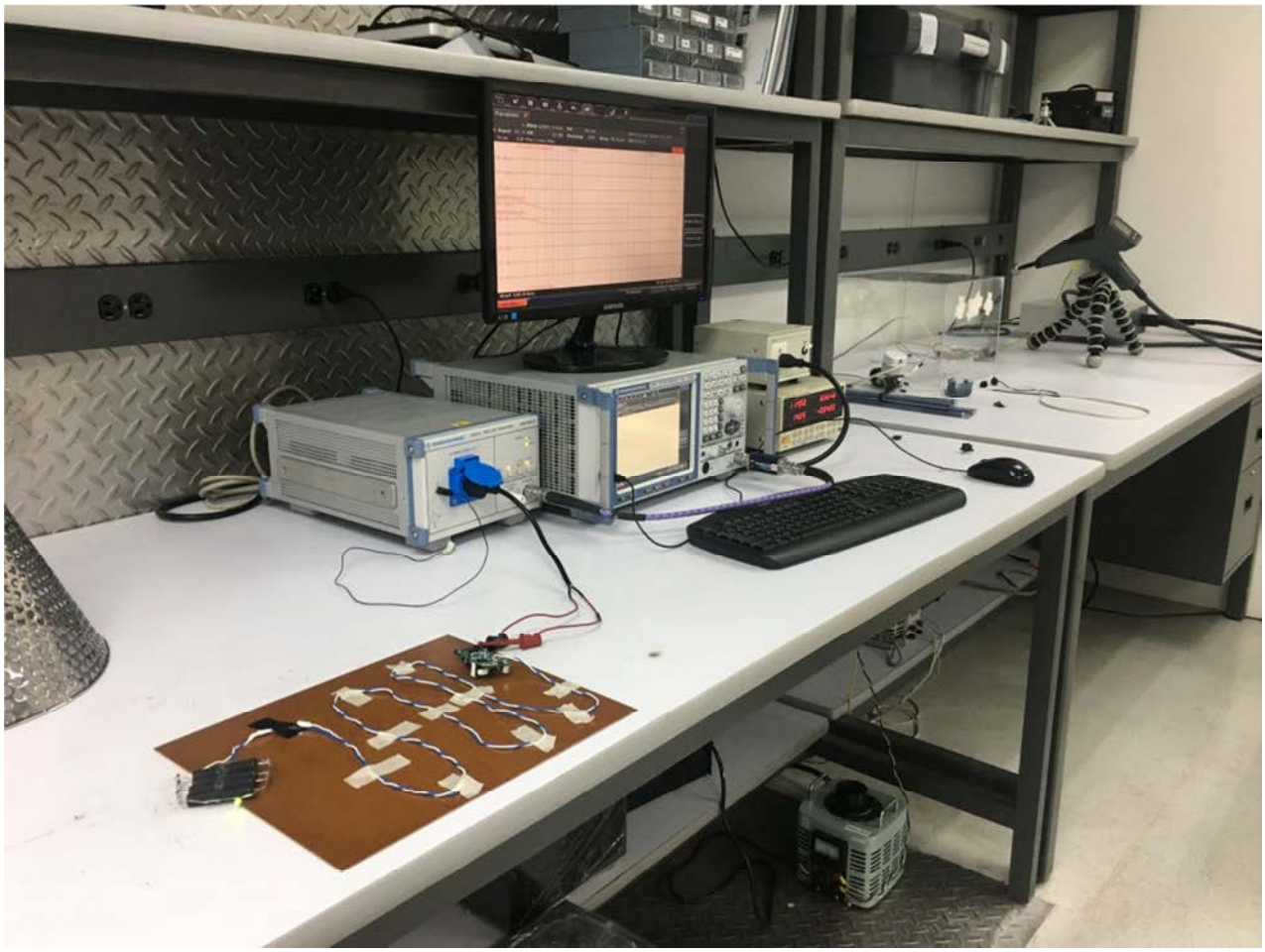

Figure 81 – Conducted EMI Test Set-up.

17.2 2 A Resistive Load, Floating Output

17.2.1 115 VAC

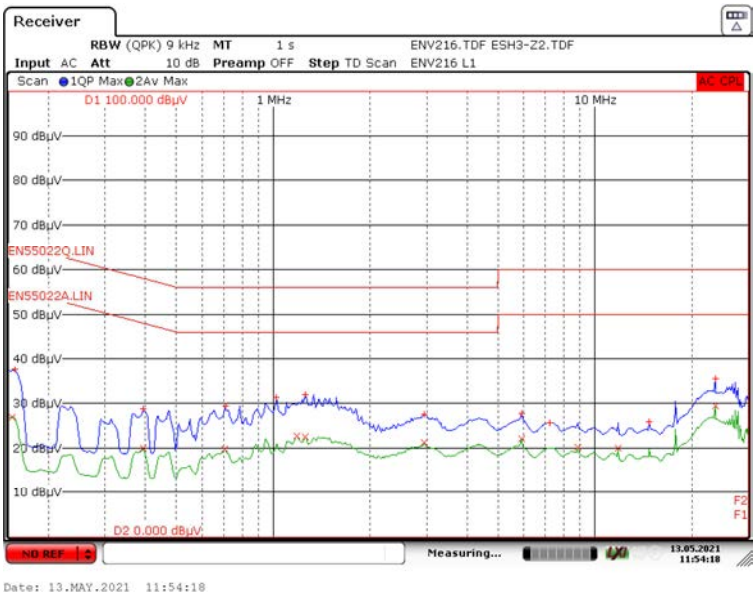

Figure 82 – Floating Ground EMI at 115 VAC, Line.

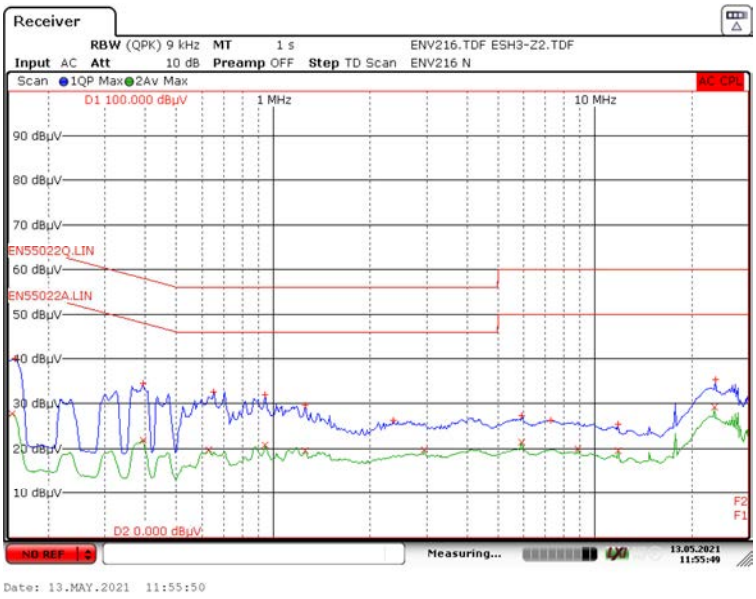

Figure 83 – Floating Ground EMI at 115 VAC, Neutral.

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17.2.2 230 VAC, Line

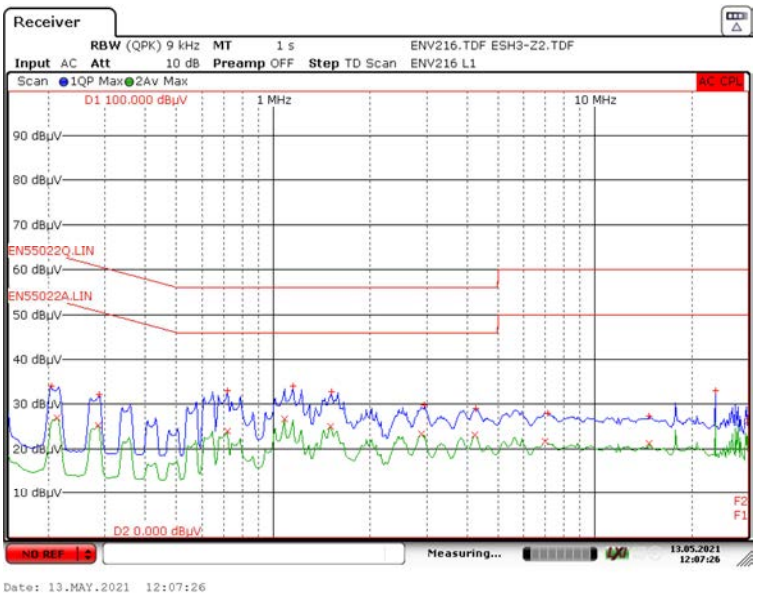

Figure 84 – Floating Ground EMI at 230 VAC, Line.

17.2.3 230 VAC, Neutral

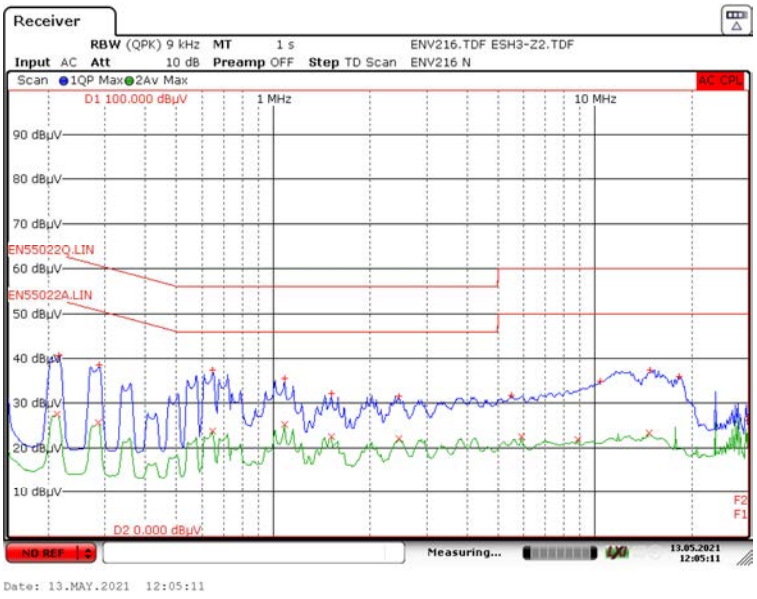

Figure 85 – Floating Ground EMI at 230 VAC, Neutral.

17.3 2 A Resistive Load, Artificial Hand

17.3.1 115 VAC, Line

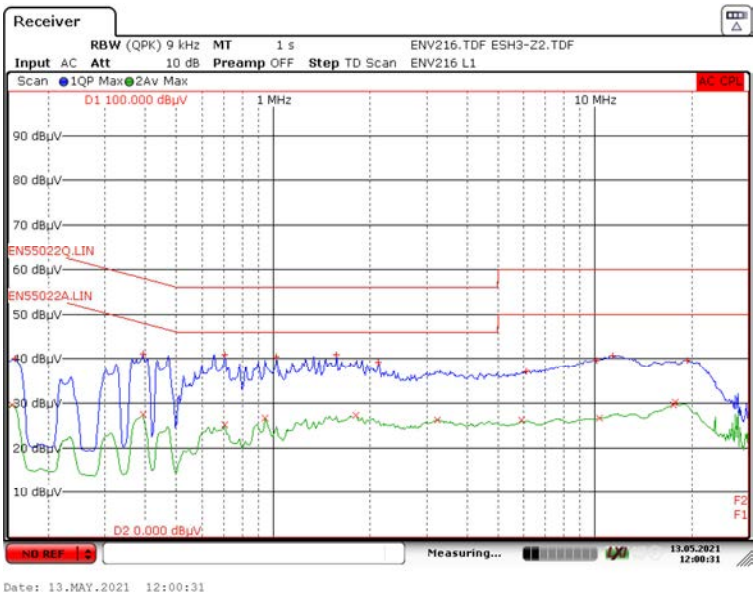

Figure 86 – Artificial Hand Ground EMI at 115 VAC, Line.

17.3.2 115 VAC, Neutral

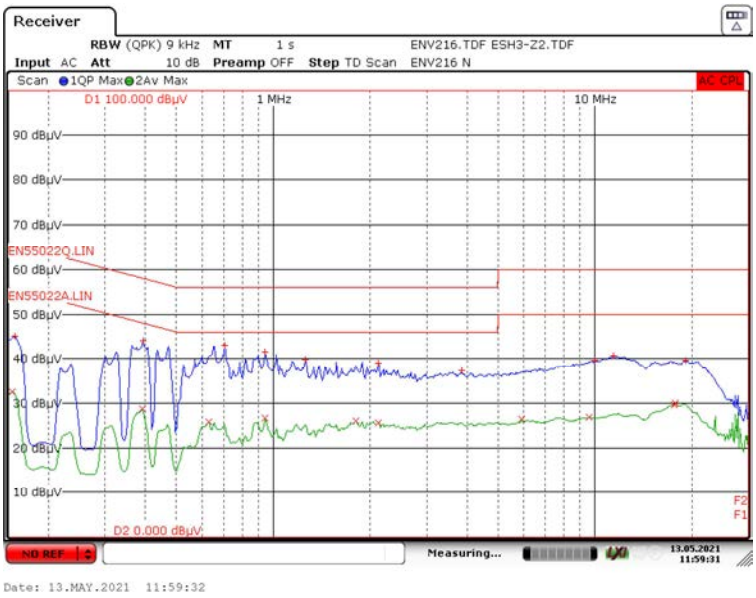

Figure 87 – Artificial Hand Ground EMI at 115 VAC, Neutral.

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17.3.3 230 VAC, Line

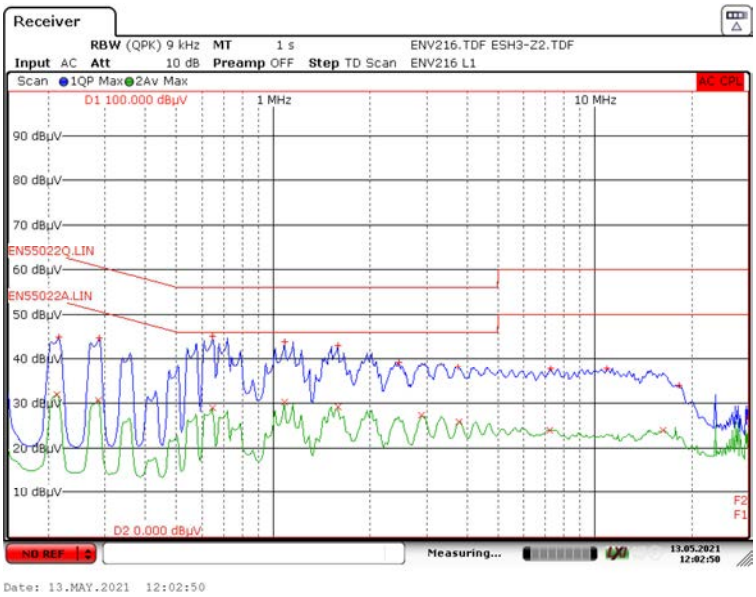

Figure 88 – Artificial Hand Ground EMI at 230 VAC, Line.

17.3.4 230 VAC, Neutral

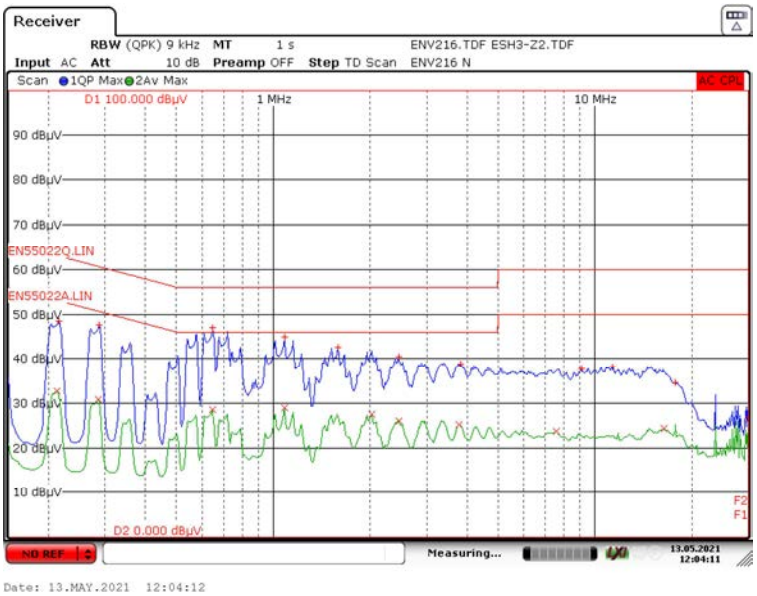

Figure 89 – Artificial Hand Ground EMI at 230 VAC, Neutral.

18 Lightning Surge and ESD Test

18.1 Differential Surge Test Summary

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number Strikes	Result
+1 kV	0	L to N	2 Ω	10	No Damage
-1 kV	0	L to N	2 Ω	10	No Damage
+1 kV	90	L to N	2 Ω	10	No Damage
-1 kV	90	L to N	2 Ω	10	No Damage
+1 kV	180	L to N	2 Ω	10	No Damage
-1 kV	180	L to N	2 Ω	10	No Damage
+1 kV	270	L to N	2 Ω	10	No Damage
-1 kV	270	L to N	2 Ω	10	No Damage

18.2 Common Mode Ring Wave Test Summary

Passed ±6 kV, 500 A ring wave test.

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number Strikes	Result
+3 kV	0	L to PE	12 Ω	10	No Damage
-3 kV	0	L to PE	12 Ω	10	No Damage
+3 kV	90	L to PE	12 Ω	10	No Damage
-3 kV	90	L to PE	12 Ω	10	No Damage
+3 kV	180	L to PE	12 Ω	10	No Damage
-3 kV	180	L to PE	12 Ω	10	No Damage
+3 kV	270	L to PE	12 Ω	10	No Damage
-3 kV	270	L to PE	12 Ω	10	No Damage
+4 kV	0	L to PE	12 Ω	10	No Damage
-4 kV	0	L to PE	12 Ω	10	No Damage
+4 kV	90	L to PE	12 Ω	10	No Damage
-4 kV	90	L to PE	12 Ω	10	No Damage
+4 kV	180	L to PE	12 Ω	10	No Damage
-4 kV	180	L to PE	12 Ω	10	No Damage
+4 kV	270	L to PE	12 Ω	10	No Damage
-4 kV	270	L to PE	12 Ω	10	No Damage

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Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number Strikes	Result
+5 kV	0	L to PE	12 Ω	10	No Damage
-5 kV	0	L to PE	12 Ω	10	No Damage
+5 kV	90	L to PE	12 Ω	10	No Damage
-5 kV	90	L to PE	12 Ω	10	No Damage
+5 kV	180	L to PE	12 Ω	10	No Damage
-5 kV	180	L to PE	12 Ω	10	No Damage
+5 kV	270	L to PE	12 Ω	10	No Damage
-5 kV	270	L to PE	12 Ω	10	No Damage
+6 kV	0	L to PE	12 Ω	10	No Damage
-6 kV	0	L to PE	12 Ω	10	No Damage
+6 kV	90	L to PE	12 Ω	10	No Damage
-6 kV	90	L to PE	12 Ω	10	No Damage
+6 kV	180	L to PE	12 Ω	10	No Damage
-6 kV	180	L to PE	12 Ω	10	No Damage
+6 kV	270	L to PE	12 Ω	10	No Damage
-6 kV	270	L to PE	12 Ω	10	No Damage

18.3 ESD Test

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result
+8000	230	Contact	10	No Damage
+16500	230	Air	10	No Damage

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result
-8000	230	Contact	10	No Damage
-16500	230	Air	10	No Damage

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19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
05-Sep-17	MA	1.0	Initial Release.	Apps & Mktg
12-Oct-17	KM	1.1	Updated Schematics, Graphs and Waveforms.	Apps & Mktg
21-May-21	JD	1.2	Added R14 and insulator. Updated Schematics, and Waveforms.	Apps & Mktg

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