Design Example Report

Title	***8 W Wide Range Input, Dual Output, Non-Isolated Flyback Converter Using LinkSwitch™-XT2 900 V LNK3696P***
Specification	85 VAC – 350 VAC Input 5 V / 650 mA, 12 V / 400 mA Outputs
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	DER-744
Date	September 27, 2018
Revision	1.0

Summary and Features

- High standby mode efficiency design to deliver up to 46 mA with 0.3 W input power
- Less than 50 mW no-load consumption across input range
- Using highly integrated solution with 900 V rated power MOSFET
- Programmable current limit selection feature of LinkSwitch™-XT2-900
- >81% average efficiency at 115 VAC and 230 VAC
- >6 dB conducted EMI margin
- Over-temperature protection with hysteretic recovery
- Auto-restart output short-circuit and open-loop protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a non-isolated flyback converter designed to provide dual output of 5 V at 650 mA and 12 V at 400 mA from a wide input range of 85 VAC to 350 VAC. This power supply utilizes the LNK3696P from the LinkSwitch™-XT2 900 V family of devices.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

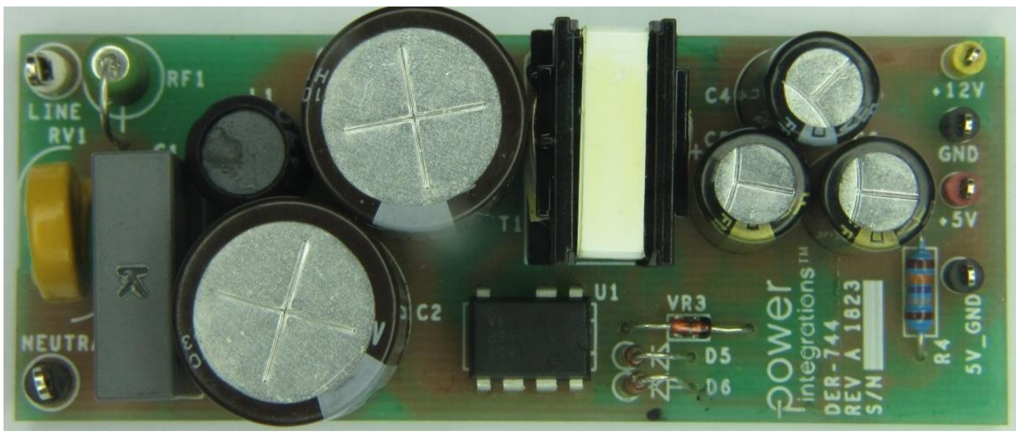

Figure 1 – Populated Circuit Board Photograph, Top.

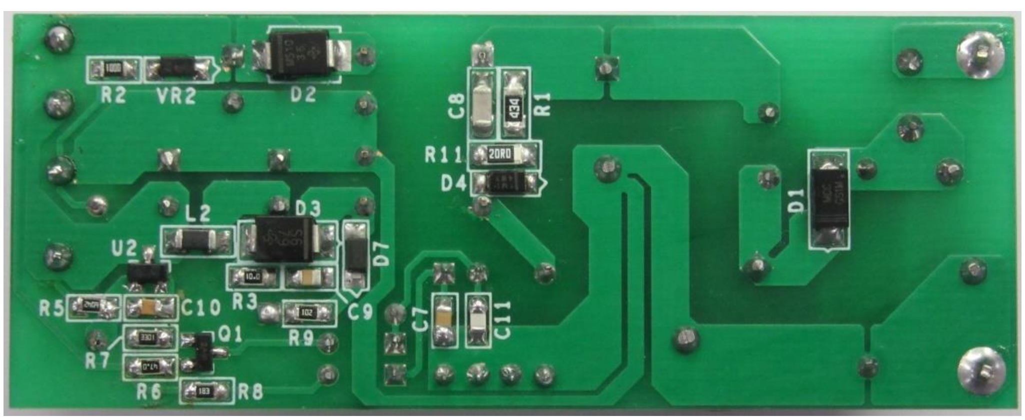

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	85	115/230	350	VAC	2 Wire – no P.E.
Frequency	$\mathbf{f_{LINE}}$	47	50/60	63	Hz	
No-load Input Power				50	mW	230 VAC Input.
Output						
Output Voltage 1	$\mathbf{V_{OUT1}}$		5		V	±5% PCB Connector Side.
Output Current 1	$\mathbf{I_{OUT1}}$		0.65		A	
Output Ripple Voltage 1	$\mathbf{V_{RIPPLE1}}$			150	mV_{PP}	Measured at the PCB Connector.
Output Voltage 2	$\mathbf{V_{OUT2}}$		12		V	±10% PCB Connector Side.
Output Current 2	$\mathbf{I_{OUT2}}$	0.02	0.40		A	
Output Ripple Voltage 2	$\mathbf{V_{RIPPLE2}}$			200	mV_{PP}	Measured at the PCB Connector.
Continuous Output Power	$\mathbf{P_{OUT}}$			8	W	
Efficiency						
Average 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	72			%	DoE Level VI, Basic Voltage.
Environmental						
Conducted EMI	CISPR22B / EN55022B Load floating					Resistive Load, 6 dB Margin.
Safety	IEC950 / UL1950 Class II					Designed to Meet.
Differential Line Surge		1			kV	
Common Mode Surge (L1/L2)		2			kV	Ring Wave, Common Mode: 12 Ω.
Ambient Temperature	$\mathbf{T_{AMB}}$	0		40	ºC	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic Diagram

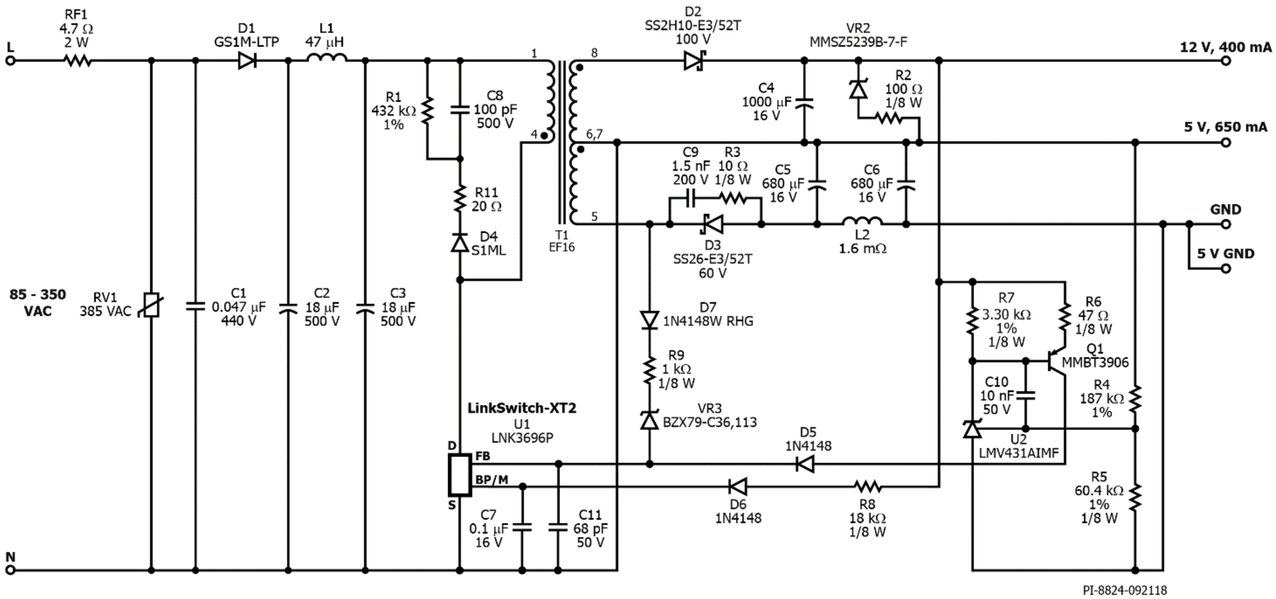

Figure 3 – Schematic.

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4 Circuit Description

The LinkSwitch-XT2 900 V family of devices integrates a 900 V rated power MOSFET with an internal oscillator and ON/OFF controller inside a single monolithic IC. Unlike conventional pulse width modulation (PWM) controllers, LinkSwitch-XT2 900 V devices utilize a simple ON/OFF control scheme combined with an internal current limit circuitry to regulate the output voltage. The LNK3696P IC is used in design of the 8 W non-isolated flyback with dual output of 5 V and 12 V delivering 650 mA and 400 mA, respectively.

4.1 *Input Filter and Rectifier*

Resistor RF1 is fusible, flameproof, wire-wound type and functions as a fuse and inrush current limiter which provide protection against catastrophic failure of components of the primary side and limits the inrush current when the power supply is connected to the AC input supply due to low impedance of the input capacitors, C2 and C3, during start-up operation.

Varistor RV1 clamps the AC input voltage across the power supply against surge and voltage transients.

Input X-capacitor C1 and pi filter combination of C2, L1, and C3 attenuate differential mode EMI.

Diode D1 rectifies the AC line voltage to half wave rectified DC and filtered by the input bulk storage capacitors C2 and C3.

4.2 *LinkSwitch-XT2 Primary-Side*

The rectified and filtered input voltage is applied to one end of the primary winding of flyback transformer T1. The other side of T1 primary winding is driven by the integrated power MOSFET of IC U1 via the DRAIN (D) pin.

The LNK3696P IC U1 operates at a fixed current limit, I_{LIMIT}. Every enabled switching cycle the primary current ramps to this current limit level. Output regulation is maintained by skipping switching cycles (ON/OFF control). The internal controller determines if the next switching cycle should be enabled or disabled (skipped) based on the current flowing into the FEEDBACK (FB) pin. If a current less than 49 μA flows into the FB pin when the oscillator's (internal) clock signal occurs, power MOSFET switching is enabled for that particular switching cycle and the power MOSFET turns on. If the current is greater than 49 μA then the power MOSFET is disabled for the current switching cycle.

The switching cycle terminates when the current through the power MOSFET reaches I_{LIMIT}, or the on-time of the power MOSFET reaches the maximum duty cycle, DC_{MAX} limit.

4.3 *Primary RCD Clamp*

A low cost RCD clamp is connected across the primary winding of transformer T1 composed of resistors R1 and R11, capacitor C8 and diode D4. The primary clamp limits the peak drain voltage of the internal power MOSFET of U1 due to the effects of transformer leakage reactance.

4.4 *Primary Bias*

LinkSwitch-XT2 devices can be completely self-powered from the DRAIN (D) pin, requiring only a bypass ceramic capacitor C7 across the BYPASS (BP) pin, which also sets the mode selector for the current limit value. However, connecting an external current source to the BP pin significantly decreases no-load input power and improves overall efficiency. This external current source for the BP pin is tapped from the 12 V output controlled by resistor R8 via diode D6.

4.5 *Output Rectification*

Transformer T1 has two secondary windings in AC-stacked configuration for the dual output of 5 V and 12 V. Each secondary switching voltage is rectified by Schottky diodes D2 and D3 and filtered by super low ESR type capacitors C4 and C5. A post-filter using L2 and C6 were added to further improve peak-to-peak voltage ripple at the output connector. The RC snubber network, R3 and C9, limits the peak inverse voltage spikes across the secondary rectifier diode D3.

4.6 *Output Feedback*

The 5 V output is sensed through resistor dividers R4 and R5. The sensed voltage is fed through a precision shunt regulator U2. The corresponding cathode current of U2, biased from the 12 V output through resistor R7, drives the base of transistor Q1 which controls the collector current supplied by the 12 V output through resistor R6. This collector current is fed to the FB pin of U1 via diode D5. As the current increases, the current into the FB pin of U1 also increases until the turnoff threshold current (~49 μA) is reached, disabling further switching cycles of U1. Just before the start of each cycle, the U1 controller checks the FB pin current to determine if the next switching cycle is enabled or disabled. The capacitors C7 and C10 provide stability and better transient response during load changes.

The 12 V output is quasi-regulated with the tight coupling between 5 V and 12 V secondary windings. A simple circuit using Zener diode VR2 and resistor R2 clamps the 12 V output up to ~14 V when then the 5 V output is fully loaded.

4.7 *Line Overvoltage Protection*

LNK3696P IC U1 indirectly senses the DC bus overvoltage condition during the power MOSFET on-time by monitoring the current flowing in the FB pin. During the MOSFET on-time, the voltage across the secondary winding is proportional to the voltage across the primary winding. When the DC bus voltage reaches the overvoltage limit, Zener diode

VR3 is turned on via diode D2 and resistor R9 causing the current to flow into the FB pin. IC U1 will enter into auto-restart mode if the FB pin current exceeds the FB pin shutdown current threshold, $I_{FB(SD)}$, for at least two consecutive switching cycles.

4.8 *Design Key Points*

The design targets to improve the standby mode efficiency by maximizing the available output power in a given input power required. Standby mode efficiency was optimized with the transformer design and selection of active devices, primary clamp, filter components and bias resistors values.

4.8.1 Transformer Design

- Z-winding technique on the primary-side of transformer resulting to low interwinding capacitance and a direct influence on the CV^2f loss
- Lower reflected output voltage (VOR) setting yields to lower secondary peak, RMS, and average currents which affects the $I_{AVE}V_F$ losses of the output diodes
- Proper selection of core material

4.8.2 Primary Clamp

- Proper tuning of primary clamp required to meet derated primary MOSFET V_{DS} at maximum input voltage and sufficient margin on EMI performance

4.8.3 Primary Bias

- Since the bias voltage for the BP pin is tapped from the 12 V output, BP pin bias current appears as a preload to the 12 V rail
- Optimize BP bias current within 90 μA to 100 μA during standby mode

4.8.4 Secondary Output Diodes

- Use of Schottky rectifiers due to its lower forward voltage and faster reverse recovery time specification
- Selecting higher current rating of diodes of at least three times the actual DC current through the diode results to lower bulk resistance and, in turn, allowing the diode to operate at lower current density. Bigger packages also contribute to better thermal management because of lower thermal resistance

4.8.5 Filter Components

- Lower ESR causes capacitor to dissipate less power when subjected to secondary ripple current
- Lower DC resistance directly decreases the dissipation across the ferrite bead

5 PCB Layout

PCB copper thickness is 2 oz. (2.8 mils / 70 µm) unless otherwise stated.

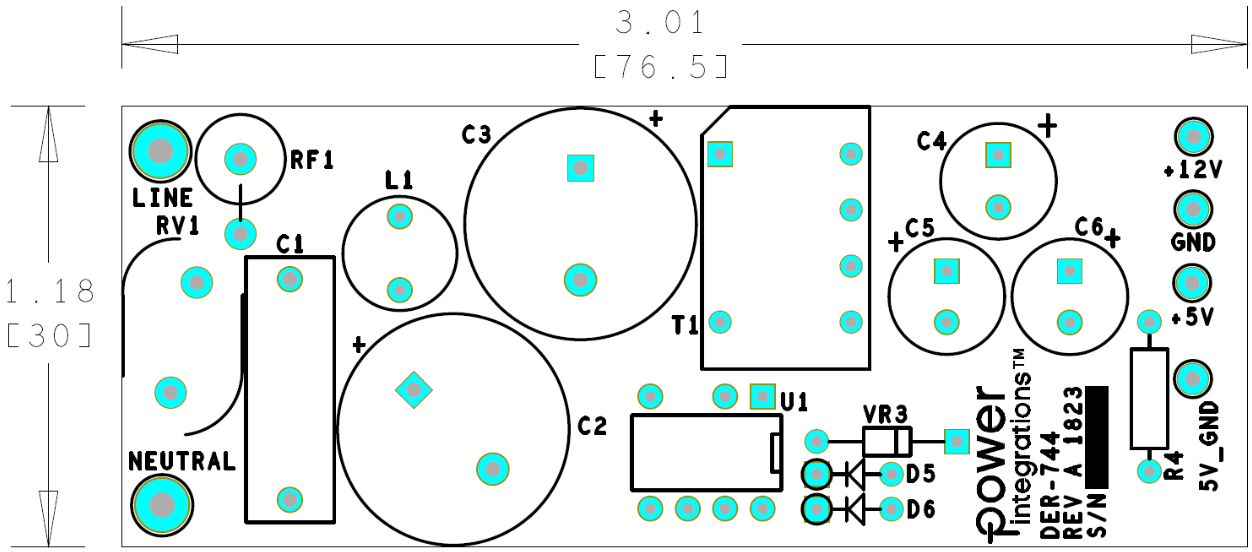

Figure 4 – Printed Circuit Layout, Top.

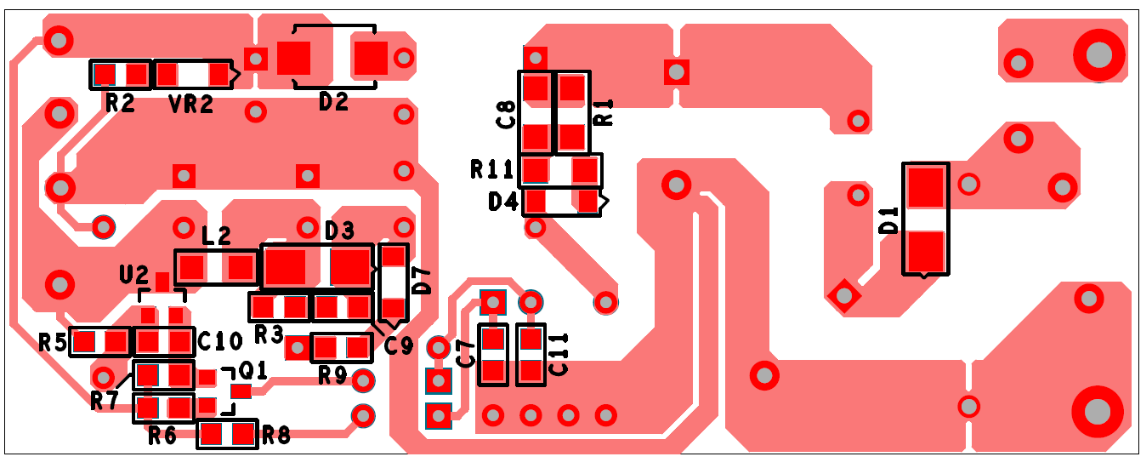

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C1	CAP, FILM, 0.047 μF, 10%, 1 kVDC, 440 VAC, RADIAL	R474I247050A2K	Kemet
2	2	C2, C3	18 μF, ±20%, 500 V, Electrolytic, High Voltage, 10000 Hrs @ 105 °C,(16 x 21.5)	UCY2H180MHD3TN	Nichicon
3	1	C4	1000 μF, 16 V, Electrolytic, Very Low ESR, (8 x 20)	EEU-FR1C102LB	Panasonic
4	2	C5, C6	680 μF, ±20%, 16 V, Electrolytic, Radial, Gen Purpose, 30 mΩ, (8 x 22), LS 3.5 mm	EEU-FM1C681L	Panasonic
5	1	C7	0.1 μF, ±5%, 16V, X7R, 0805	C0805C104J4RACTU	Kemet
6	1	C8	100 pF, ±10%,500 V, Ceramic, X7R, 1206	C1206C101KCRACTU	Kemet
7	1	C9	1.5 nF, 200 V,10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
8	1	C10	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
9	1	C11	68 pF, ±1%, 50 V, C0G, NP0, Ceramic, -55 °C ~ 125 °C, SMT, MLCC 0805	C0805C680F5GACTU	Kemet
10	1	D1	1000 V, 1 A, DO-214AC	GS1M-LTP	Micro Commercial
11	1	D2	100 V, 2 A, Schottky, SMD, SMB	SS2H10-E3/52T	Vishay
12	1	D3	60 V, 2 A, Schottky, SMD, DO-214AA	SS26-E3/52T	Vishay
13	1	D4	1 kV, 1 A, Standard Recovery, SMA	S1ML	Taiwan Semi
14	2	D5, D6	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
15	1	D7	DIODE, GEN PURP, 100 V, 150 mA, SOD123, SOD-123F	1N4148W RHG	Taiwan Semi
16	1	L1	47 μH, ±10%, Unshielded, Wirewound Inductor, 1.56 A, 140 mΩ Max, Radial	RLB0914-470KL	Bourns
17	1	L2	FERRITE BEAD, 50 Ω, 1206, 1LN, 1.6 mΩ	BLM31SN500SN1L	Murata
18	1	Q1	PNP, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3906LT1G	On Semi
19	1	R1	RES, 432 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4323V	Panasonic
20	1	R2	RES, 100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
21	1	R3	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
22	1	R4	RES, 187 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-187K	Yageo
23	1	R5	RES, 60.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6042 V	Panasonic
24	1	R6	RES, 47 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
25	1	R7	RES, 3.30 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3301V	Panasonic
26	1	R8	RES, 18 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ183V	Panasonic
27	1	R9	RES, 1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102 V	Panasonic
28	1	R11	RES, 20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
29	1	RF1	RES, 4.7 Ω, 5%, 2 W, Wirewound, Fusible	FW20A4R70JA	Bourns
30	1	RV1	385 VAC, 67 J, 7 mm, RADIAL	VDRS10P385BSE	Vishay
31	1	T1	Bobbin, Vertical, EF16, 8 Pins	B66308W1108T001	TDK
32	1	U1	LinkSwitch-XT2 900 V,DIP-8C	LNK3696P	Power Integrations
33	1	U2	1.24 V Shunt Regulator IC, 1%, -40 to 85 C, SOT23-3	LMV431AIMF/NOPB	Texas Instruments
34	1	VR2	DIODE ZENER 9.1 V 500 mW SOD123	MMSZ5239B-7-F	Diodes, Inc.
35	1	VR3	36 V, 500 mW, 5%, DO-35	BZX79-C36,113	NXP Semi

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	LINE	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
2	1	NEUTRAL	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	+12 V	Test Point, YEL, Miniature THRU-HOLE MOUNT	5004	Keystone
4	1	+5 V	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
5	2	GND, 5 V_GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

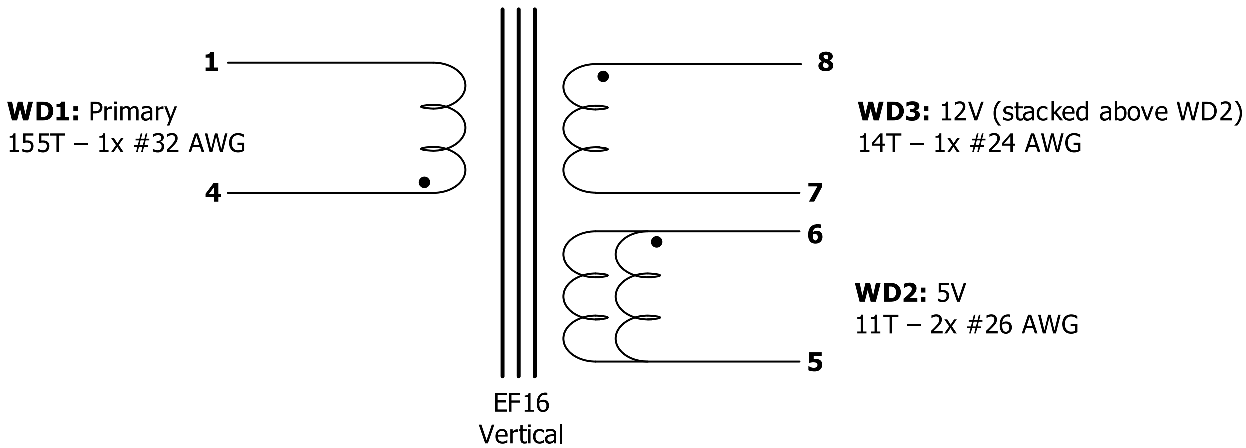

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specification*

Electrical Strength	1 sec, 60 Hz, from pins 5-8 to pins 1, 4.	3000 VAC
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 1 V_{RMS}.	1731 μH ±10%
Primary Leakage Inductance	Pins 1-4, with pins 5-8 shorted, measured at 100 kHz, 0.4 V_{RMS}.	60 μH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EF16, Ferrite Core N87 gapped for ALG of 72nH/T². Part Number: B66307G0000X187 EPCOS TDK.
[2]	Bobbin: EF16 Vertical.
[3]	Magnet Wire: #32 AWG, Double Coated.
[4]	Magnet Wire: #26 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Double Coated.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 10 mm Wide.
[7]	Tape: 3M 1298 Polyester Film 1 mil Thick, 4.5 mm Wide.
[8]	Varnish: Dolph BC-359.

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7.4 *Transformer Build Diagram*

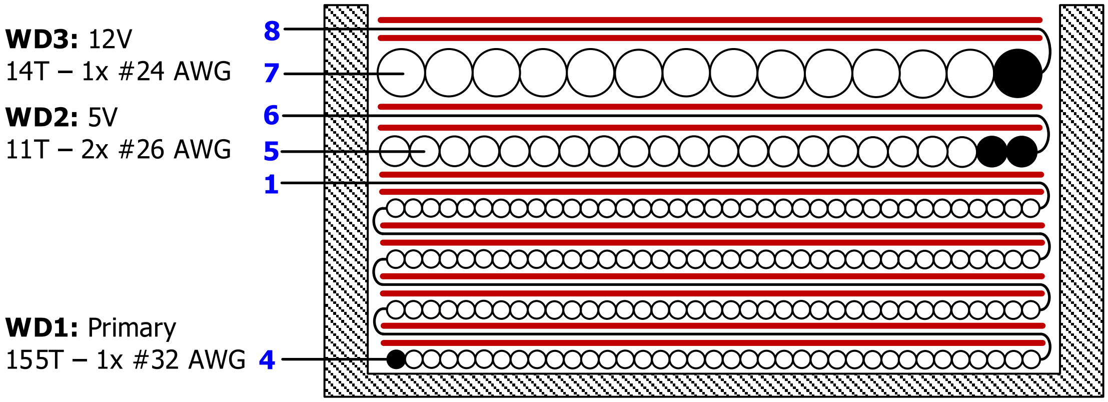
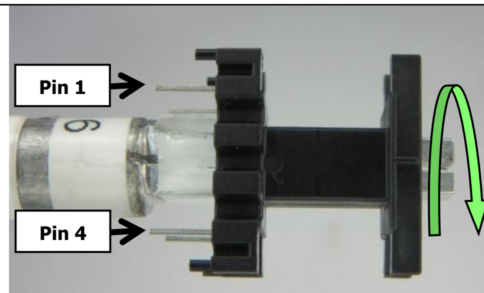
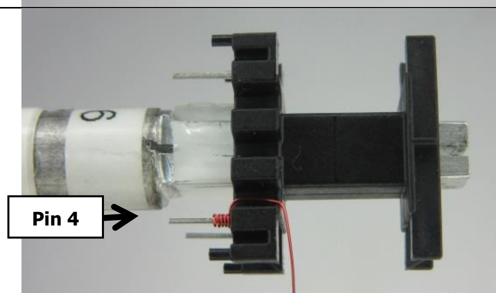
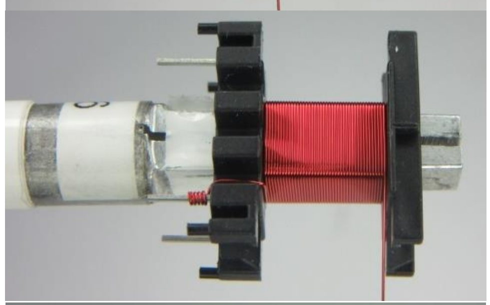
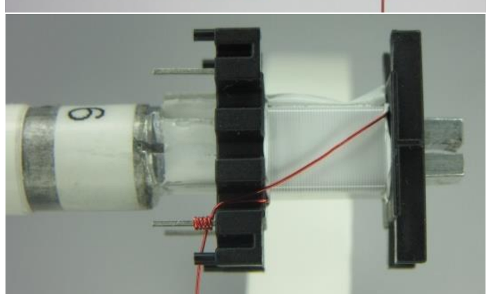
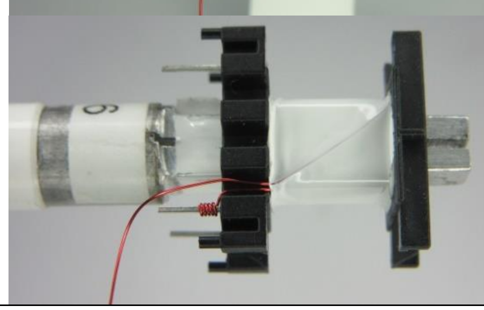


Figure 7– Transformer Build Diagram.

7.5 *Transformer Instructions*

Winding Preparation	Remove unused pin 2 and pin 3. For the purpose of these instructions, bobbin is oriented on winder such that primary side is on the left side with pin 4 at the bottom. Winding direction is clockwise direction.
WD1 Primary	Start at pin 4, wind 155 turns (x1 filar) of wire Item [3] in 4 layers using Z-winding configuration with tight tension (Layer 1 – 42T, Layer 2 – 41T, Layer 3 – 42T, Layer 4 – 30T).
Insulation	At the end of each layer, add 1 layer of tape Item [6]. Bring the wire back to the left. And add another one-half layer of tape Item [6]. Terminate at pin 1 after the fourth layer of winding.
WD2 5 V	Start winding at the right side of the bobbin with 11 turns (x2 filar) of wire Item [4]. Terminate winding at pin 5.
Insulation	Add 1 layer of tape Item [6] for insulation. Terminate the floating start of WD2 to pin 6 and add another 1 layer of tape Item [6].
WD3 12 V	Start winding at the right side of the bobbin with 14 turns (x1 filar) of wire Item [5]. Terminate winding at pin 7.
Insulation	Add 1 layer of tape Item [6] for insulation. Terminate the floating start of WD3 to pin 8 and add another 1 layer of tape Item [6].
Finish	Gap core halves for 1731 µH inductance. Wrap core halves with tape Item [7]. Coat with Varnish Item [8].

7.6 *Winding Illustrations*

Winding Preparation		Remove unused pin 2 and pin 3. For the purpose of these instructions, bobbin is oriented on winder such that primary side is on the left side with pin 4 at the bottom. Winding direction is clockwise direction.
WD1 Primary and Insulation		Start at pin 4, wind 155 turns (x1 filar) of wire Item [3] in 4 layers using Z-winding configuration with tight tension
		Layer 1 – 42T, Layer 2 – 41T, Layer 3 – 42T, Layer 4 – 30T.
		At the end of each layer, add 1 layer of tape Item [6]. Bring the wire back to the left.
		Add another one-half layer of tape Item [6].

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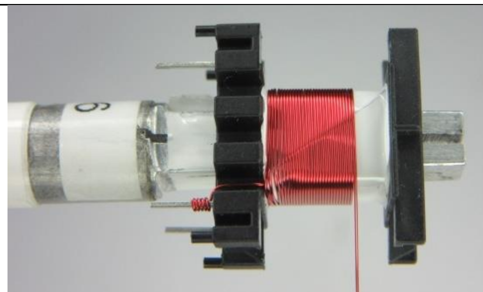
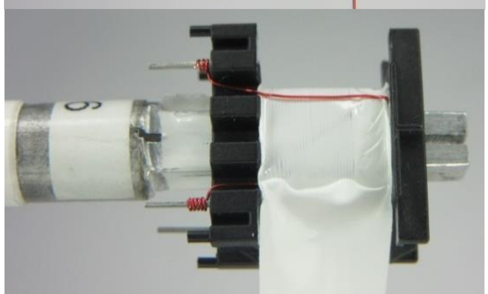
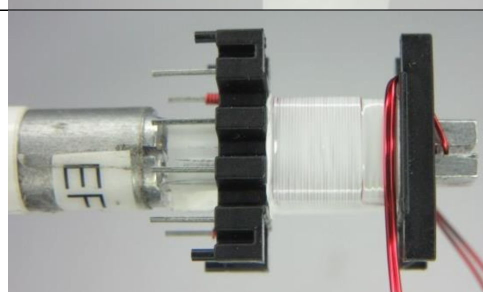
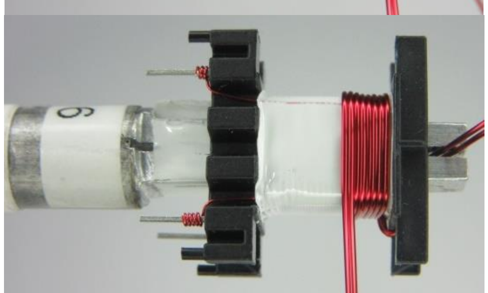
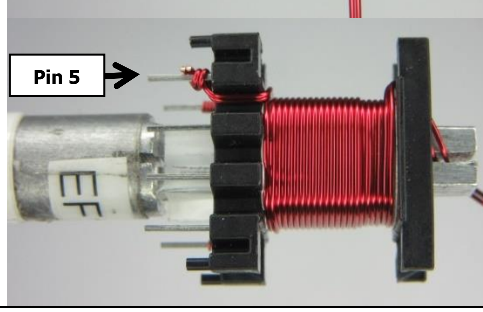
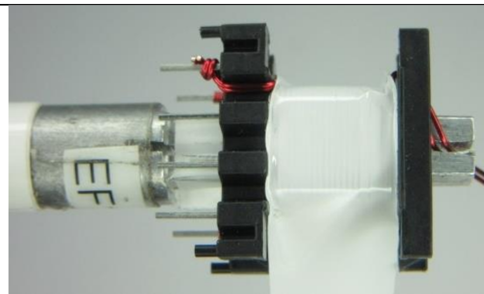
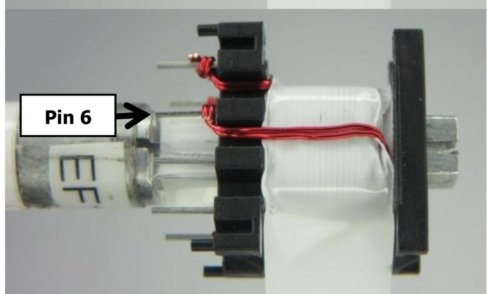
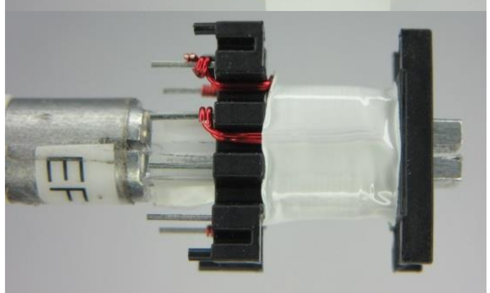
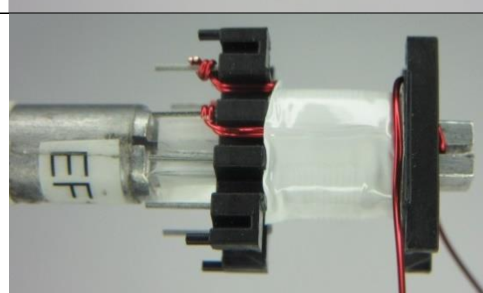
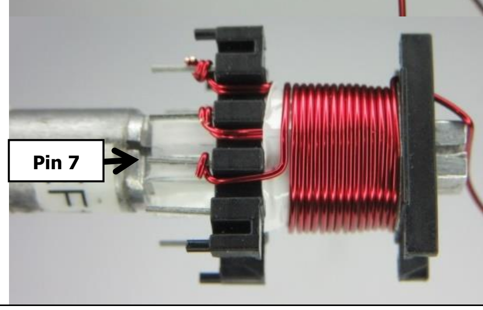
WD1 Primary and Insulation	 	At the end of the 4th winding layer, add one turn of tape Item [6] and terminate wire at pin 1. Add another one-half layer of tape Item [6].
WD2 5 V	  	Start winding at the right side of the bobbin with 11 turns (x2 filar) of wire Item [4]. Terminate winding at pin 5.

Insulation		Add 1 layer of tape Item [6] for insulation.
		Terminate the floating start of WD2 to pin 6.
		Add another 1 layer of tape Item [6].
WD3 **12 V**		Start winding at the right side of the bobbin with 14 turns (x1 filar) of wire Item [5].
		Terminate winding at pin 7.

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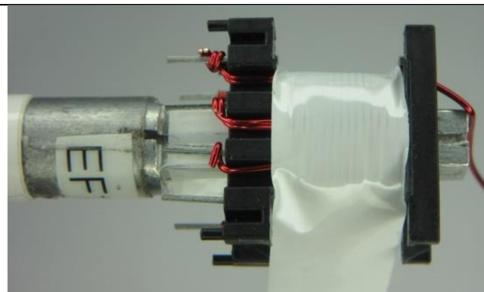
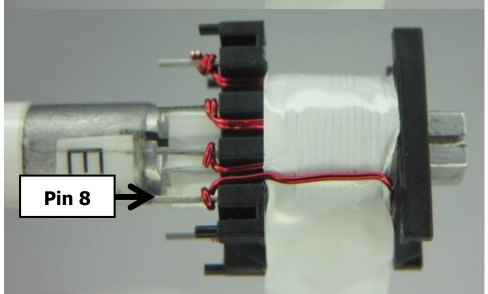
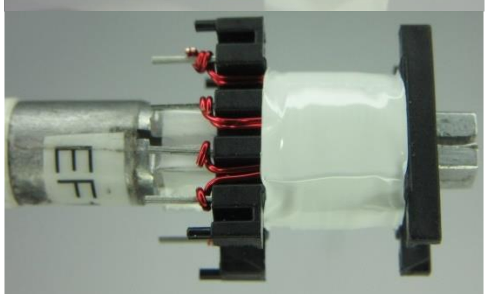
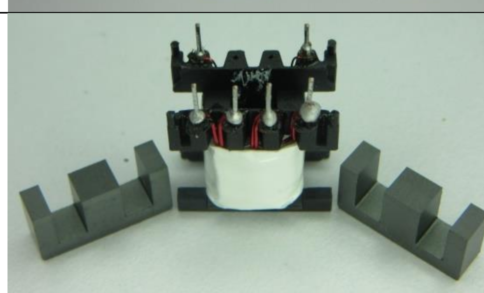
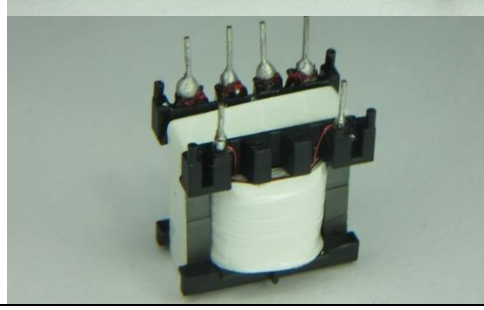
Insulation	  	Add 1 layer of tape Item [6] for insulation. Terminate the floating start of WD3 to pin 8. Add another 1 layer of tape Item [6].
Finish	 	Gap core halves for 1731 μH inductance. Wrap core halves with tape Item [7]. Coat with Varnish Item [8].

8 Transformer Design Spreadsheet

1	ACDC_LinkSwitchXT2900V_040318Rev.1.0; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchXT2 900V Flyback Design Spreadsheet
2	ENTER APPLICATION VARIABLES					
3	LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
4	VACMIN	85.00		85.00	Volts	Minimum AC line voltage
5	VACTYP	230.00		230.00	Volts	Typical AC line voltage
6	VACMAX	350.00		350.00	Volts	Maximum AC line voltage
7	fL			50	Hertz	AC mains frequency
8	TIME_BRIDGE_CONDUCTION			3.11	mseconds	Input bridge rectifier diode conduction time
9	LINE RECTIFICATION	H		H		Select 'F'ull wave rectification or 'H'alf wave rectification
10	VOUT	5.00		5.00	Volts	Output voltage
11	IOUT	1.600		1.600	Amperes	Average output current specification
12	CC THRESHOLD VOLTAGE			0.00	Volts	Voltage drop across the sense resistor
13	OUTPUT CABLE RESISTANCE			0.00	Ohms	Enter the resistance of the output cable (if used)
14	EFFICIENCY			0.80		Efficiency Estimate at output terminals. Under 0.8 if no better data available
15	LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the MOSFET off-state to the total system losses
16	POUT			8.00	Watts	Continuous Output Power
17	CIN	36.00		36.00	uFarads	Input capacitor
18	VMIN			71.17	Volts	Valley of the rectified VACMIN
19	VMAX			494.97	Volts	Peak of the VACMAX
20	FEEDBACK			OPTO		Select the type of feedback required
21	BIAS WINDING			NO		Select whether a bias winding is required
22	LINKSWITCH-XT2 VARIABLES					
23	CURRENT LIMIT MODE			STD		Pick between RED(Reduced) or STD(Standard) current limit mode of operation
24	PACKAGE			DIP-8C		Device package
25	ENCLOSURE			ADAPTER		Pick the device enclosure
26	GENERIC DEVICE	LNK3696		LNK3696		Device series
27	DEVICE CODE			LNK3696P		Device code
28	PMAX			8.00	Watts	Device maximum power capability
29	VOR	80		80	Volts	Voltage reflected to the primary winding when the MOSFET is off
30	VDSON			10.0	Volts	MOSFET on-time drain to source voltage
31	VDSOFF			683.0	Volts	Estimated MOSFET off-time drain to source voltage
32	ILIMITMIN			0.450	Amperes	Minimum current limit
33	ILIMITTYP			0.482	Amperes	Typical current limit
34	ILIMITMAX			0.515	Amperes	Maximum current limit
35	FSMIN			62000	Hertz	Minimum switching frequency
36	FSTYP			66000	Hertz	Typical switching frequency
37	FSMAX			70000	Hertz	Maximum switching frequency
38	RDSON			7.00	Ohms	MOSFET drain to source resistance
39	PRIMARY WAVEFORM PARAMETERS					
40	MODE OF OPERATION			CCM		Mode of operation
41	KRP/KDP			0.718		Measure of continuous/discontinuous mode of operation
42	KP_TRANSIENT			0.484		KP under conditions of a transient
43	DMAX			0.567		Maximum duty cycle
44	TIME_ON			9.140	useconds	MOSFET conduction time at the minimum

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						line voltage
45	TIME_ON_MIN			1.741	useconds	MOSFET conduction time at the maximum line voltage
46	IAVG_PRIMARY			0.163	Amperes	Average input current
47	IRMS_PRIMARY			0.228	Amperes	Root mean squared value of the primary current
48	LPRIMARY_MIN			1558	uH	Minimum primary inductance
49	LPRIMARY_TYP			1731	uH	Typical primary inductance
50	LPRIMARY_MAX			1904	uH	Maximum primary inductance
51	LPRIMARY_TOL			10		Primary inductance tolerance
52	**SECONDARY WAVEFORM PARAMETERS**					
53	IPEAK_SECONDARY			7.257	Amperes	Peak secondary current
54	IRMS_SECONDARY			3.218	Amperes	Root mean squared value of the secondary current
55	PIV_SECONDARY			40.13	Volts	Peak inverse voltage on the secondary diode, not including the leakage spike
56	VF_SECONDARY			0.70	Volts	Secondary diode forward voltage drop
57	**TRANSFORMER CONSTRUCTION PARAMETERS**					
58	**Core selection**					
59	CORE	Custom		Custom		Select the transformer core
60	BOBBIN	EF 16 Vertical		EF 16 Vertical		Bobbin name
61	AE	20.10		20.10	mm^2	Cross sectional area of the core
62	LE	37.60		37.60	mm	Effective magnetic path length of the core
63	AL	1000.0		1000.0	nH/(turns^2)	Ungapped effective inductance of the core
64	VE	756.0		756.0	mm^3	Volume of the core
65	AW	22.30		22.30	mm^2	Window area of the bobbin
66	BW	10.00		10.00	mm	Width of the bobbin
67	MLT	34.00		34.00	mm	Mean length per turn of the bobbin
68	MARGIN			0.00	mm	Safety margin
69	**Primary winding**					
70	NPRIMARY			155		Primary number of turns
71	BMAX_TARGET			1500	Gauss	Target value of the magnetic flux density
72	BMAX_ACTUAL		Info	2861	Gauss	The actual flux density of the device has been exceeded, increase the secondary number of turns
73	BAC			1027	Gauss	AC flux density
74	ALG			72	nH/T^2	Gapped core effective inductance
75	LG			0.325	mm	Core gap length
76	LAYERS_PRIMARY			4		Number of primary layers
77	AWG_PRIMARY			32		Primary winding wire AWG
78	OD_PRIMARY_INSULATED			0.244	mm	Primary winding wire outer diameter with insulation
79	OD_PRIMARY_BARE			0.202	mm	Primary winding wire outer diameter without insulation
80	CMA_PRIMARY			277	mil^2/Amperes	Primary winding wire CMA
81	**Secondary winding**					
82	NSECONDARY	11		11		Secondary turns
83	AWG_SECONDARY			21		Secondary winding wire AWG
84	OD_SECONDARY_INSULATED			1.029	mm	Secondary winding wire outer diameter with insulation
85	OD_SECONDARY_BARE			0.723	mm	Secondary winding wire outer diameter without insulation
86	CMA_SECONDARY			252	mil^2/Amperes	Secondary winding CMA
87	**Bias winding**					
88	NBIAS			N/A		Bias turns
89	VF_BIAS			N/A	Volts	Bias diode forward voltage drop
90	VBIAS			N/A	Volts	Bias winding voltage
91	PIVB			N/A	Volts	Peak inverse voltage on the bias diode

92	CBP			0.1	uF	BP pin capacitor
93	**FEEDBACK PARAMETERS**					
94	DIODE_BIAS			1N4003-4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI
95	RUPPER			500 - 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT2 Design Guide
96	RLOWER			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT2 Design Guide
97	**MULTIPLE OUTPUT PARAMETERS**					
98	**Output 1**					
99	VOUT1			5.00	Volts	Output Voltage 1
100	IOUT1	0.650		0.650	Amperes	Output Current 1
101	POUT1			3.25	Watts	Output Power 1
102	VD1			0.70	Volts	Secondary diode forward voltage drop for output 1
103	NS1			11		Number of turns for output 1
104	ISRMS1			1.307	Amperes	Root mean squared value of the secondary current for output 1
105	IRIPPLE1			1.134	Amperes	Current ripple on the secondary waveform for output 1
106	PIV1			40.13	Volts	Peak inverse voltage on the secondary diode for output 1
107	DIODE1_RECOMMENDED			SB360		Recommended diode for output 1
108	PRELOAD			N/A	kohms	Preload resistor to ensure a load of at least 3mA on the first output
109	CMS1			261.5	Cmils	Bare conductor effective area in circular mils for output 1
110	AWGS1			25	AWG	Wire size for output 1
111	**Output 2**					
112	VOUT2	12.00		12.00	Volts	Output Voltage 2
113	IOUT2	0.400		0.400	Amperes	Output Current 2
114	POUT2			4.80	Watts	Output Power 2
115	VD2			0.70	Volts	Secondary diode forward voltage drop for output 2
116	NS2			25		Number of turns for output 2
117	ISRMS2			0.805	Amperes	Root mean squared value of the secondary current for output 2
118	IRIPPLE2			0.698	Amperes	Current ripple on the secondary waveform for output 2
119	PIV2			91.83	Volts	Peak inverse voltage on the secondary diode for output 2
120	DIODE2_RECOMMENDED			MUR120		Recommended diode for output 2
121	CMS2			160.9	Cmils	Bare conductor effective area in circular mils for output 2
122	AWGS2			28	AWG	Wire size for output 2
123	**Output 3**					
124	VOUT3			0.00	Volts	Output Voltage 3
125	IOUT3			0.000	Amperes	Output Current 3
126	POUT3			0.00	Watts	Output Power 3
127	VD3			0.70	Volts	Secondary diode forward voltage drop for output 3
128	NS3			2		Number of turns for output 3
129	ISRMS3			0.000	Amperes	Root mean squared value of the secondary current for output 3
130	IRIPPLE3			0.000	Amperes	Current ripple on the secondary waveform for output 3
131	PIV3			6.39	Volts	Peak inverse voltage on the secondary diode for output 3
132	DIODE3_RECOMMEND			NA		Recommended diode for output 3

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	ED					
133	CMS3			0.0	Cmils	Bare conductor effective area in circular mils for output 3
134	AWGS3			0	AWG	Wire size output for 3
136	PO_TOTAL		Warning	8.05	Watts	The total power of all outputs exceeds the design power. Increase the design power in the first section of the spreadsheet
137	NEGATIVE OUTPUT			N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

9 Performance Data

9.1 *Efficiency*

9.1.1 Average Efficiency Measured across PCB Connector

9.1.1.1 85 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
83	242.5	10.03	5.02	650.2	3.26	11.41	399.8	4.57	78.0
84	182.5	7.43	5.02	487.7	2.45	11.43	299.9	3.43	79.1
84	124.9	4.93	5.03	325.2	1.64	11.45	199.9	2.29	79.5
85	66.6	2.46	5.04	162.8	0.82	11.46	100.0	1.15	80.1
						Average Efficiency (%)			**79.2**

9.1.1.2 115 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
114	181.8	9.75	5.02	650.2	3.26	11.42	399.9	4.57	80.3
114	139.4	7.29	5.02	487.7	2.45	11.44	300.0	3.43	80.6
114	96.6	4.85	5.03	325.2	1.64	11.45	199.9	2.29	80.9
115	52.1	2.43	5.04	162.8	0.82	11.47	100.0	1.15	80.9
						Average Efficiency (%)			**80.7**

9.1.1.3 230 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
229	105.1	9.57	5.02	650.2	3.26	11.43	399.9	4.57	81.9
229	81.5	7.19	5.02	487.7	2.45	11.44	300.0	3.43	81.9
229	57.1	4.81	5.03	325.2	1.64	11.46	199.9	2.29	81.7
230	31.3	2.42	5.03	162.8	0.82	11.47	100.0	1.15	81.4
						Average Efficiency (%)			**81.7**

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9.1.1.4 265 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
264	94.2	9.57	5.02	650.2	3.26	11.43	399.9	4.57	81.9
264	73.2	7.19	5.02	487.7	2.45	11.44	300.0	3.43	81.8
265	51.4	4.81	5.03	325.3	1.64	11.46	199.9	2.29	81.6
265	28.3	2.43	5.03	162.8	0.82	11.47	100.0	1.15	81.1
						Average Efficiency (%)			**81.6**

9.1.1.5 350 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
349	76.5	9.63	5.02	650.2	3.26	11.44	399.8	4.57	81.4
350	59.6	7.24	5.02	487.7	2.45	11.45	299.9	3.43	81.2
350	42.0	4.85	5.03	325.2	1.64	11.46	199.8	2.29	81.0
350	23.4	2.45	5.04	162.7	0.82	11.48	99.9	1.15	80.3
						Average Efficiency (%)			**81.0**

9.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 10 minutes and 5 minutes for each line/step

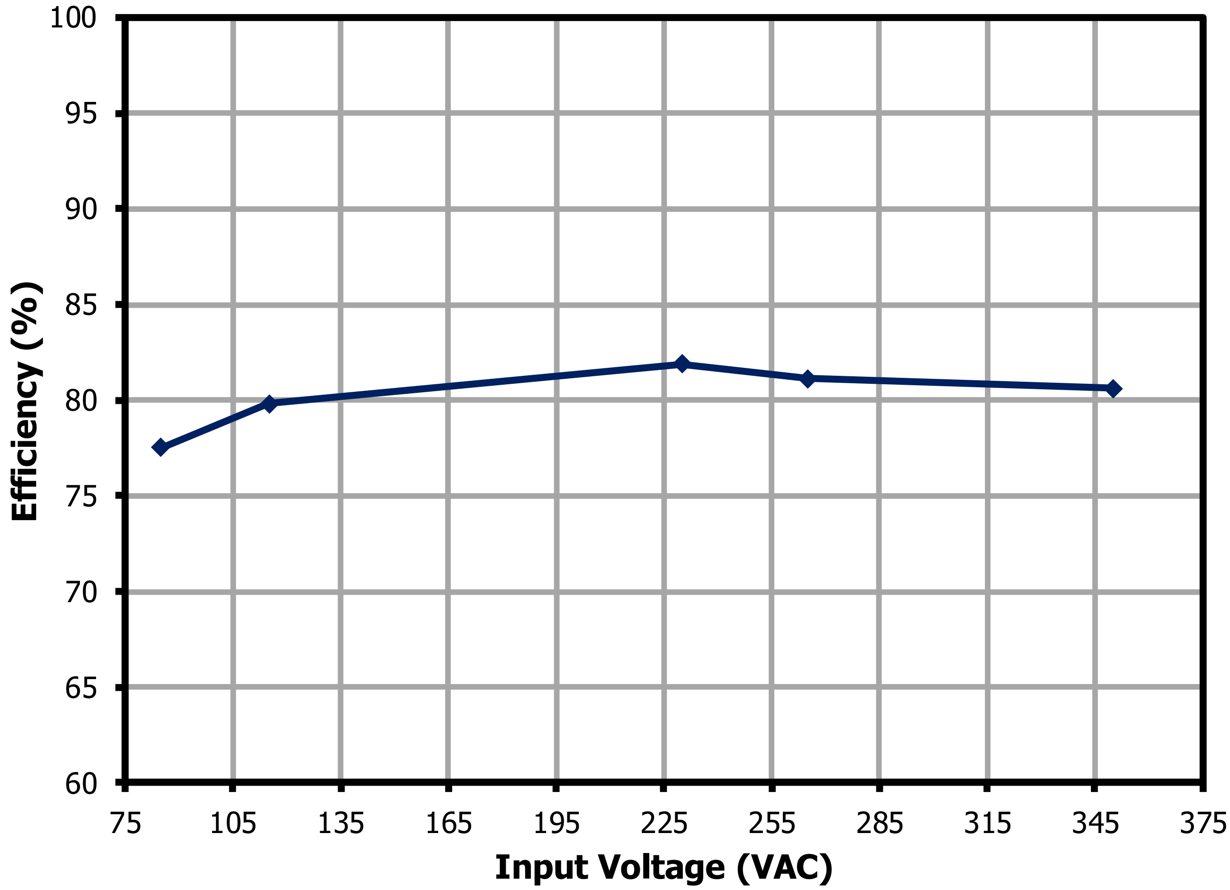

Figure 8 – Full Load Efficiency vs. Line.

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9.1.3 Efficiency vs. Load

Test Condition: Soak for 10 minutes and 5 minutes for each line/step

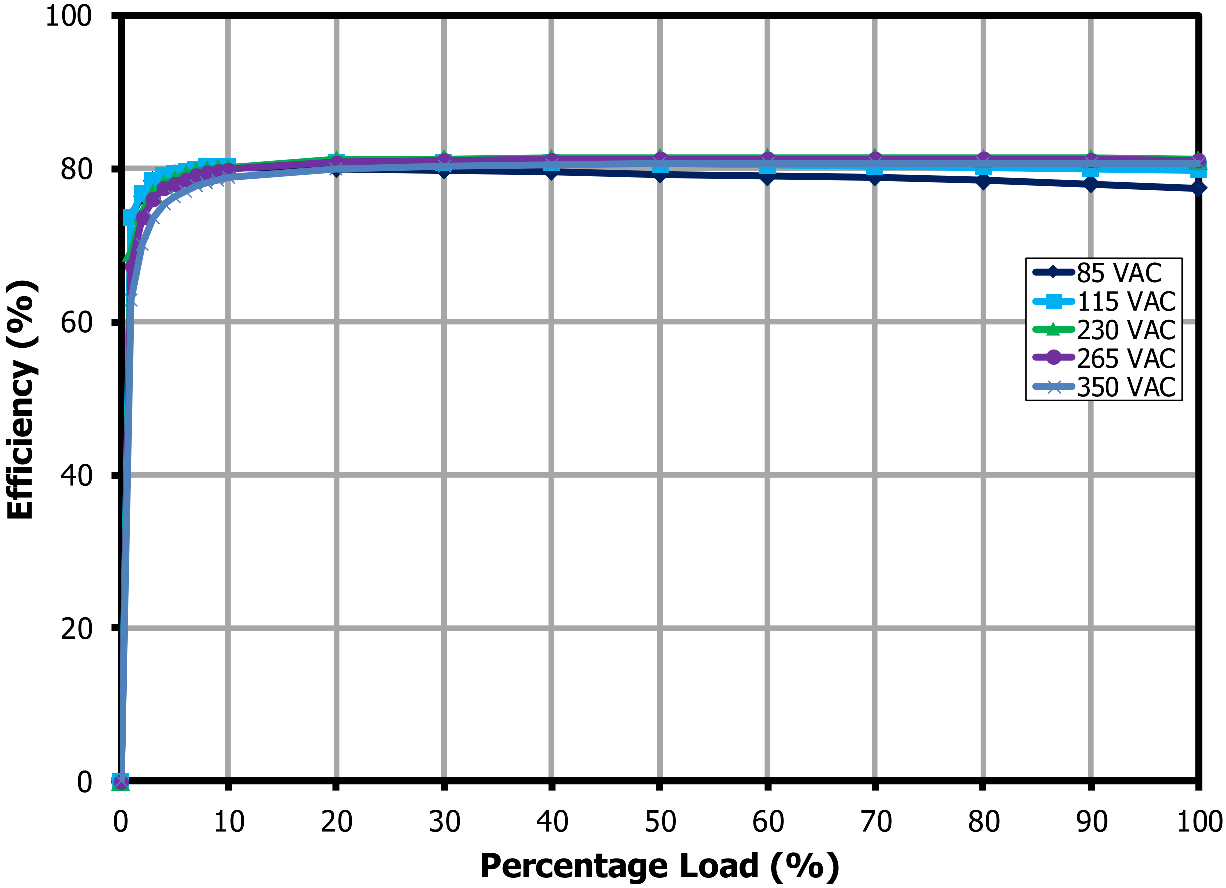

Figure 9 – Efficiency vs. Percentage Load.

9.1.4 Standby Mode Efficiency

Test Condition: Soak at full load for 5 minutes and decrease load to standby mode for 5 minutes for each line step.

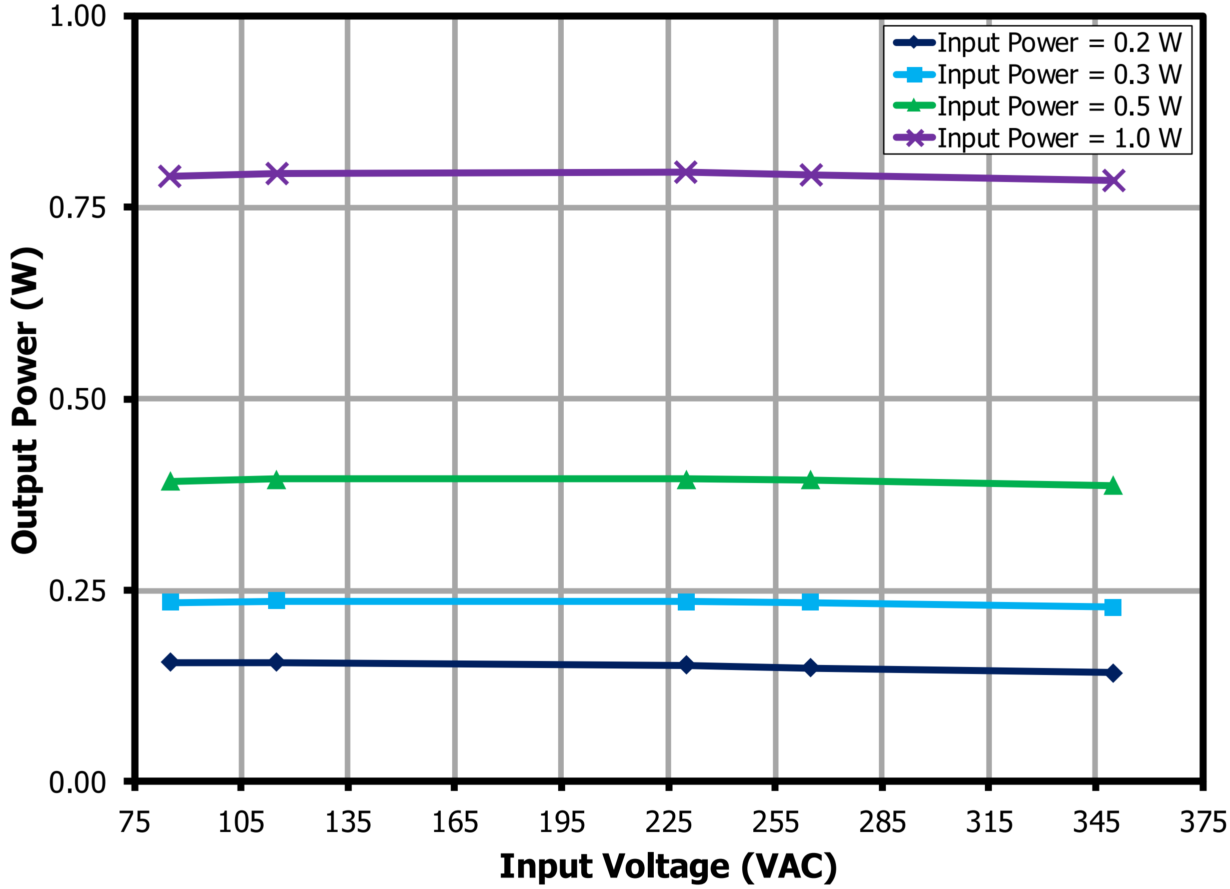

Figure 10 – Available Output Power per Input Power

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9.1.4.1 0.2 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	7.5	0.20	5.06	30.7	0.16	12.12	0.0	0.00	77.6
115	6.1	0.20	5.06	30.7	0.16	12.13	0.0	0.00	77.8
230	4.9	0.20	5.06	30.0	0.15	12.13	0.0	0.00	75.7
265	5.0	0.20	5.06	29.4	0.15	12.14	0.0	0.00	74.4
350	5.8	0.20	5.06	28.0	0.14	12.14	0.0	0.00	70.8

9.1.4.2 0.3 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	10.4	0.30	5.05	46.4	0.24	12.20	0.0	0.00	78.1
115	8.5	0.30	5.05	46.7	0.24	12.20	0.0	0.00	78.6
230	6.4	0.30	5.05	46.6	0.24	12.21	0.0	0.00	78.3
265	6.5	0.30	5.05	46.3	0.23	12.22	0.0	0.00	77.8
350	7.3	0.30	5.05	45.0	0.23	12.23	0.0	0.00	75.8

9.1.4.3 0.5 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	16.2	0.50	5.05	77.8	0.39	12.50	0.0	0.00	78.5
115	13.0	0.50	5.05	78.3	0.40	12.50	0.0	0.00	79.1
230	8.7	0.50	5.05	78.3	0.40	12.48	0.0	0.00	79.0
265	8.4	0.50	5.05	78.0	0.39	12.47	0.0	0.00	78.7
350	8.4	0.50	5.05	76.6	0.39	12.45	0.0	0.00	77.4

9.1.4.4 1.0 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	30.1	1.01	5.04	156.8	0.79	12.73	0.0	0.00	78.7
115	23.8	1.00	5.04	157.3	0.79	12.71	0.0	0.00	79.3
230	14.6	1.00	5.04	157.9	0.80	12.69	0.0	0.00	79.6
265	13.4	1.00	5.04	157.3	0.79	12.68	0.0	0.00	79.3
350	12.0	1.01	5.05	155.6	0.79	12.64	0.0	0.00	78.1

9.2 ***No-Load Input Power***

Soak for 15 minutes and 3 minutes integration time for each line/step.

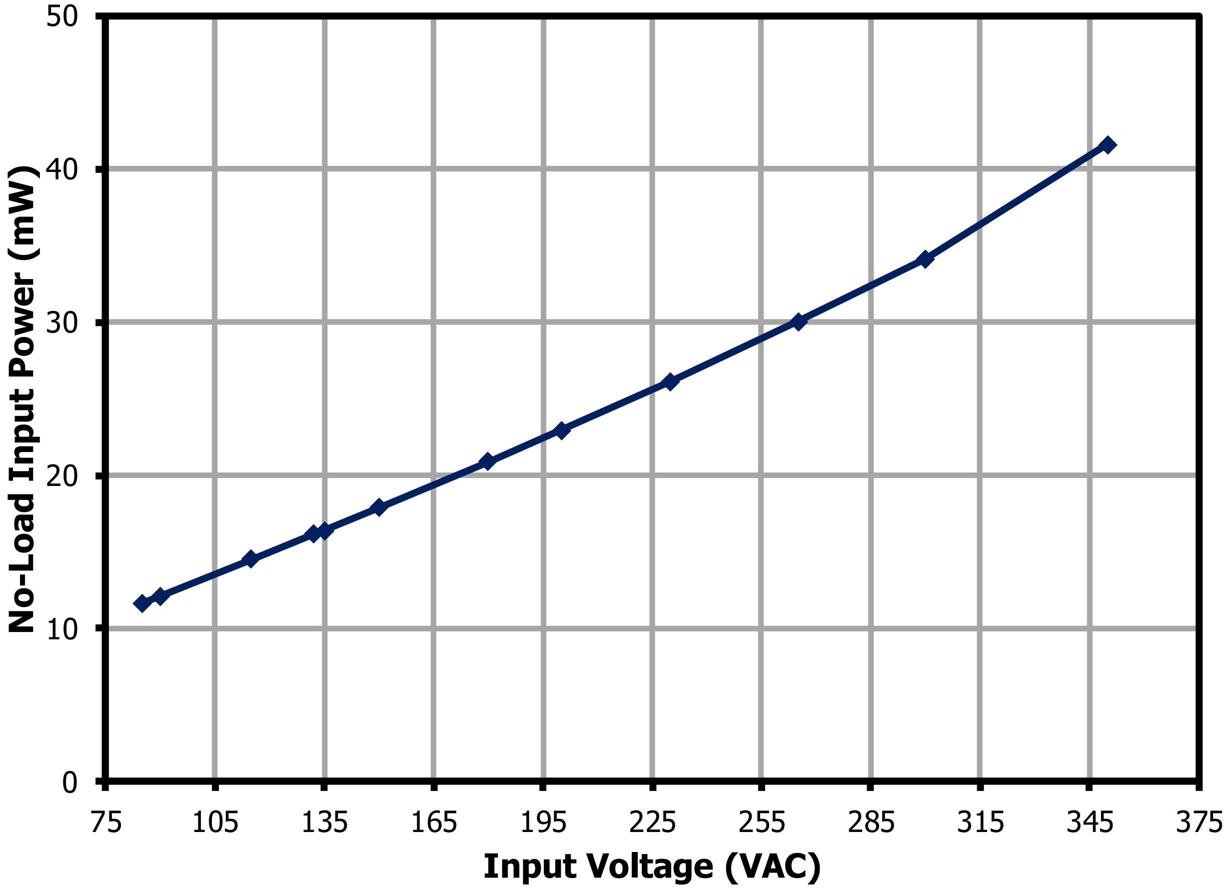

Figure 11 – No-Load Input Power vs. Input Line Voltage (Room Temperature).

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9.3 *Line Regulation*

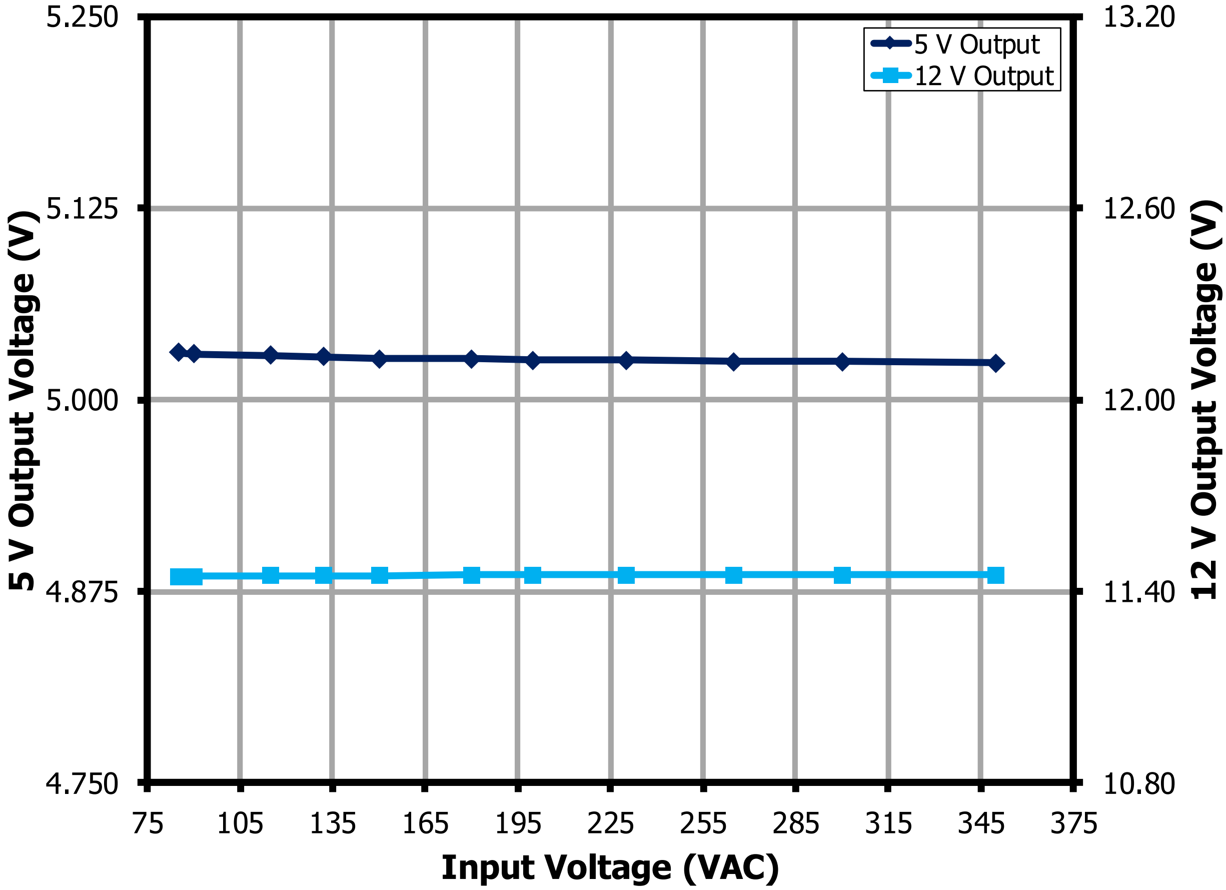

Figure 12 – Line Regulation.

9.4 ***Load Regulation***

9.4.1 5 V Load Regulation with Balanced Load

Test Condition: Simultaneous load change across 5 V and 12 V output

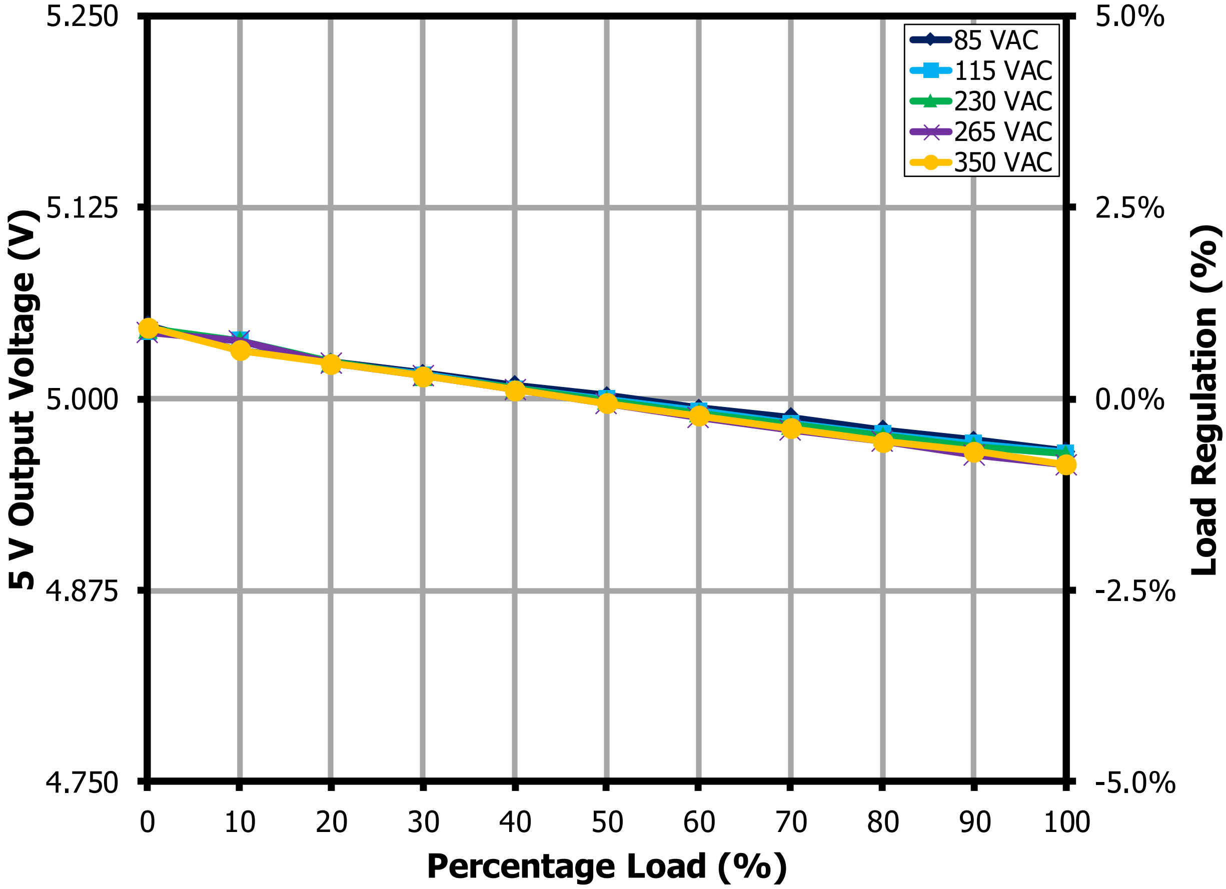

Figure 13 – 5 V Load Regulation with Balanced Load.

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9.4.2 12 V Load Regulation with Balanced Load

Test Condition: Simultaneous load change across 5 V and 12 V output

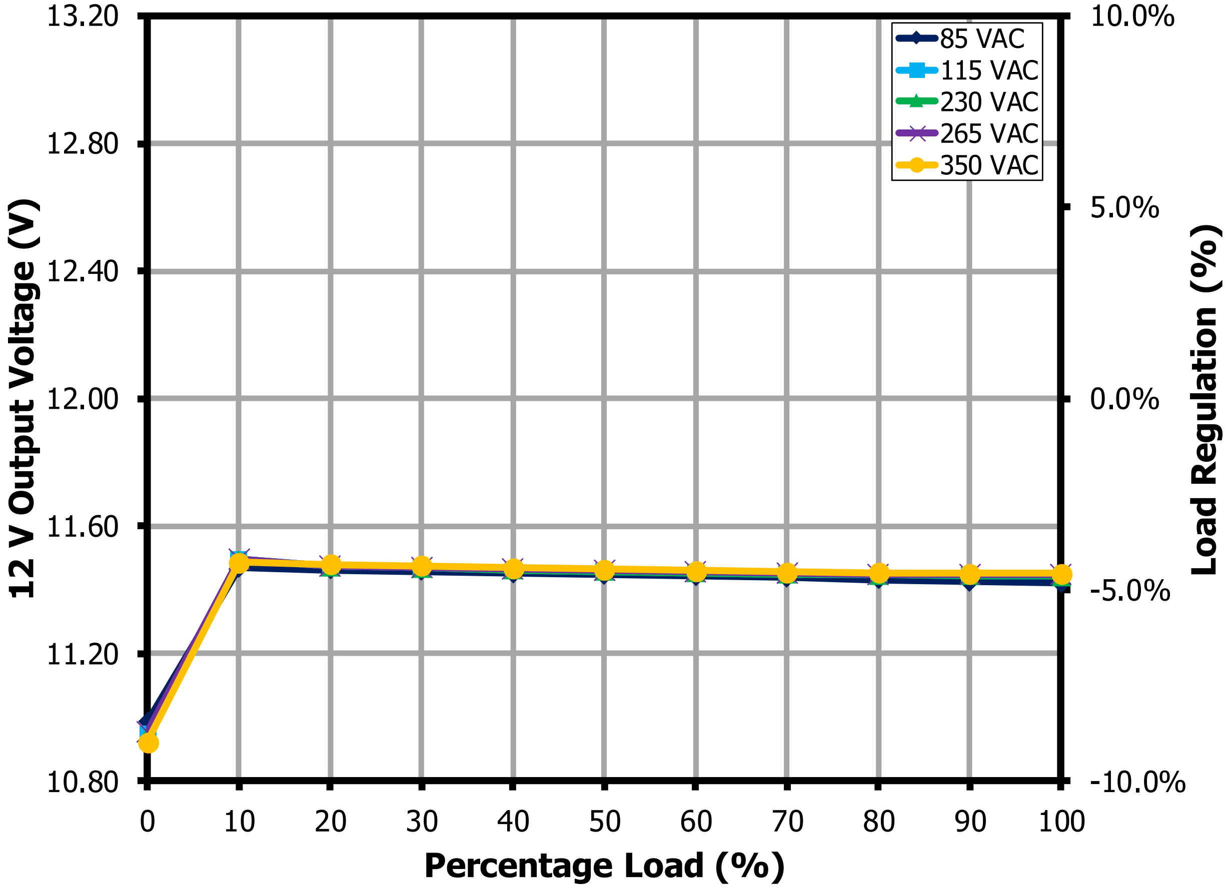

Figure 14 – 12 V Load Regulation with Balanced Load.

9.4.3 5 V Load Regulation with Fixed Full Load Across 12 V Output

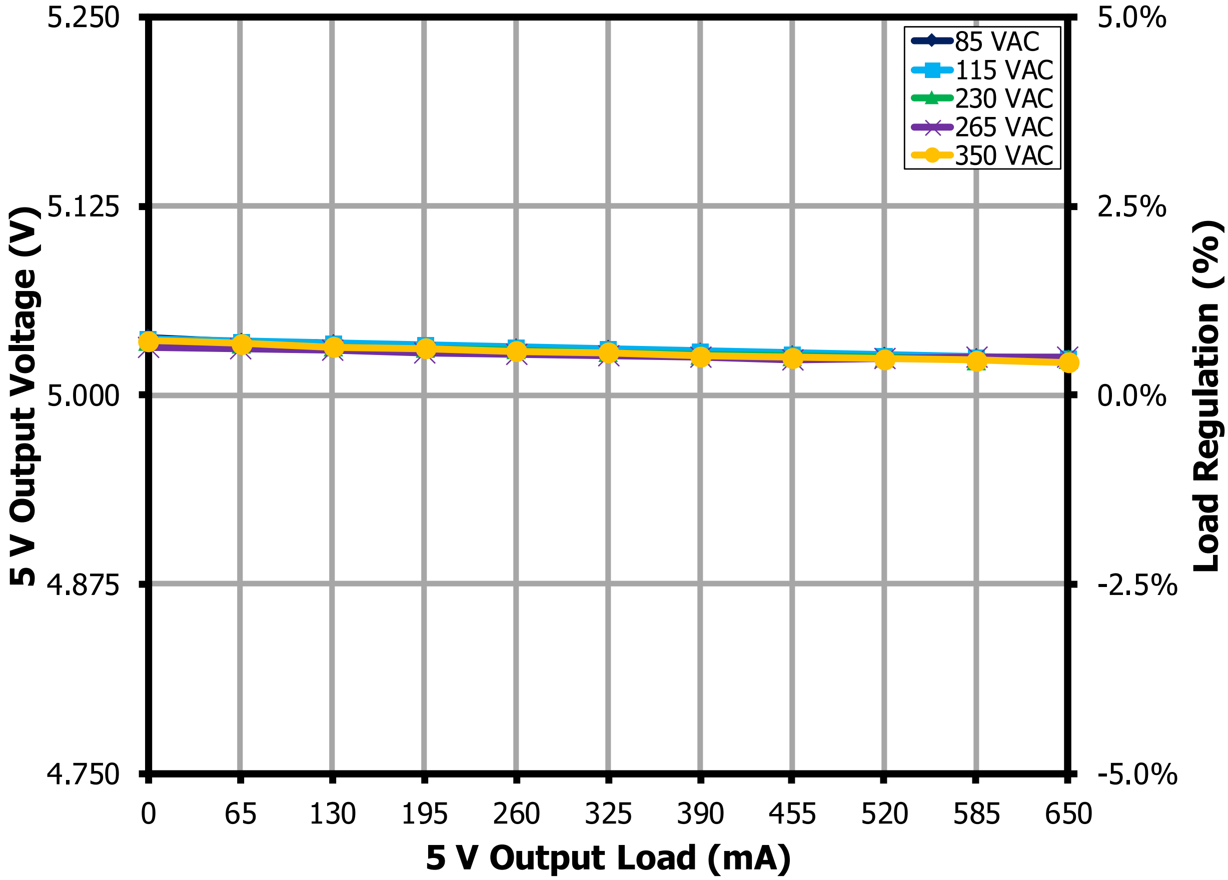

Figure 15 – 5 V Load Regulation with Fixed Full Load Across 12 V Output.

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9.4.4 5 V Load Regulation with Fixed Minimum Load Across 12 V Output

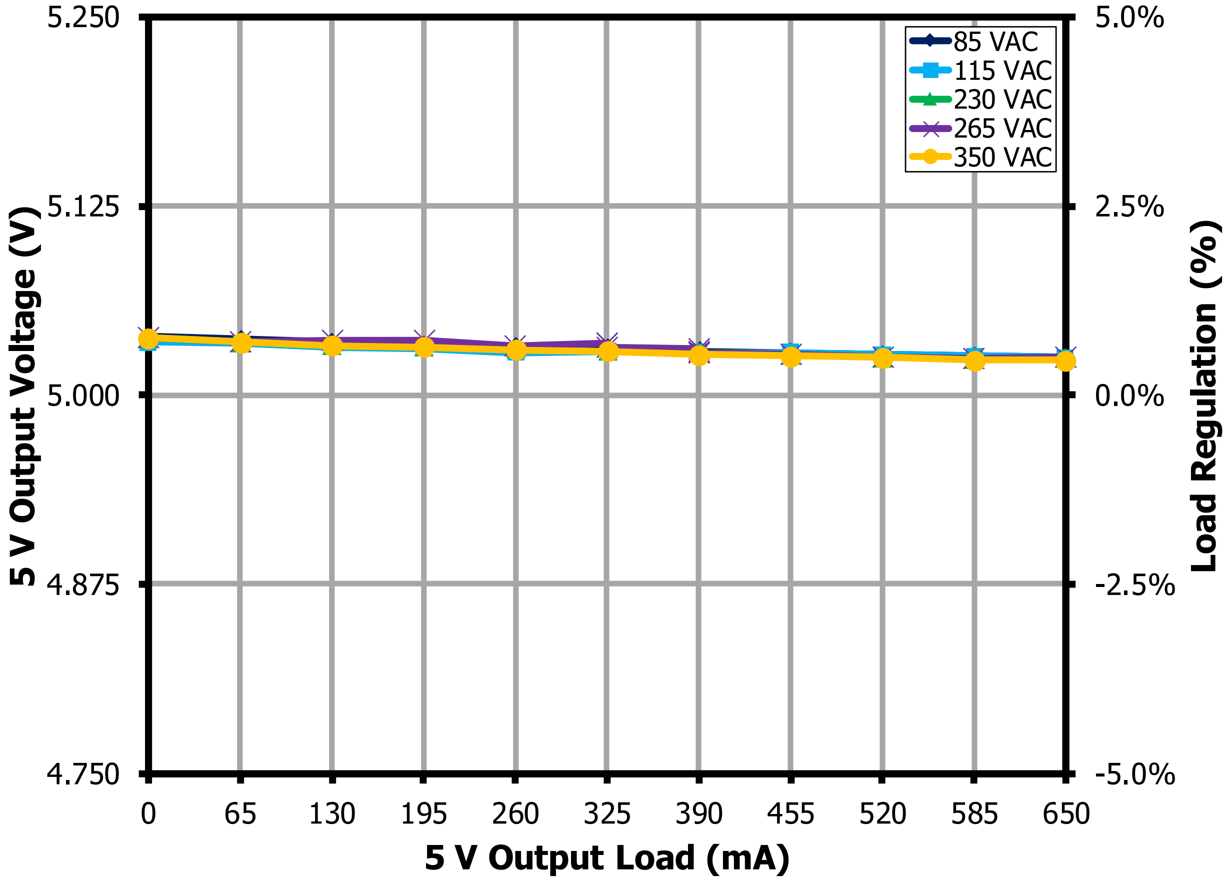

Figure 16 – 5 V Load Regulation with Fixed Minimum Load Across 12 V Output.

9.4.5 12 V Load Regulation with Fixed Full Load Across 5 V Output

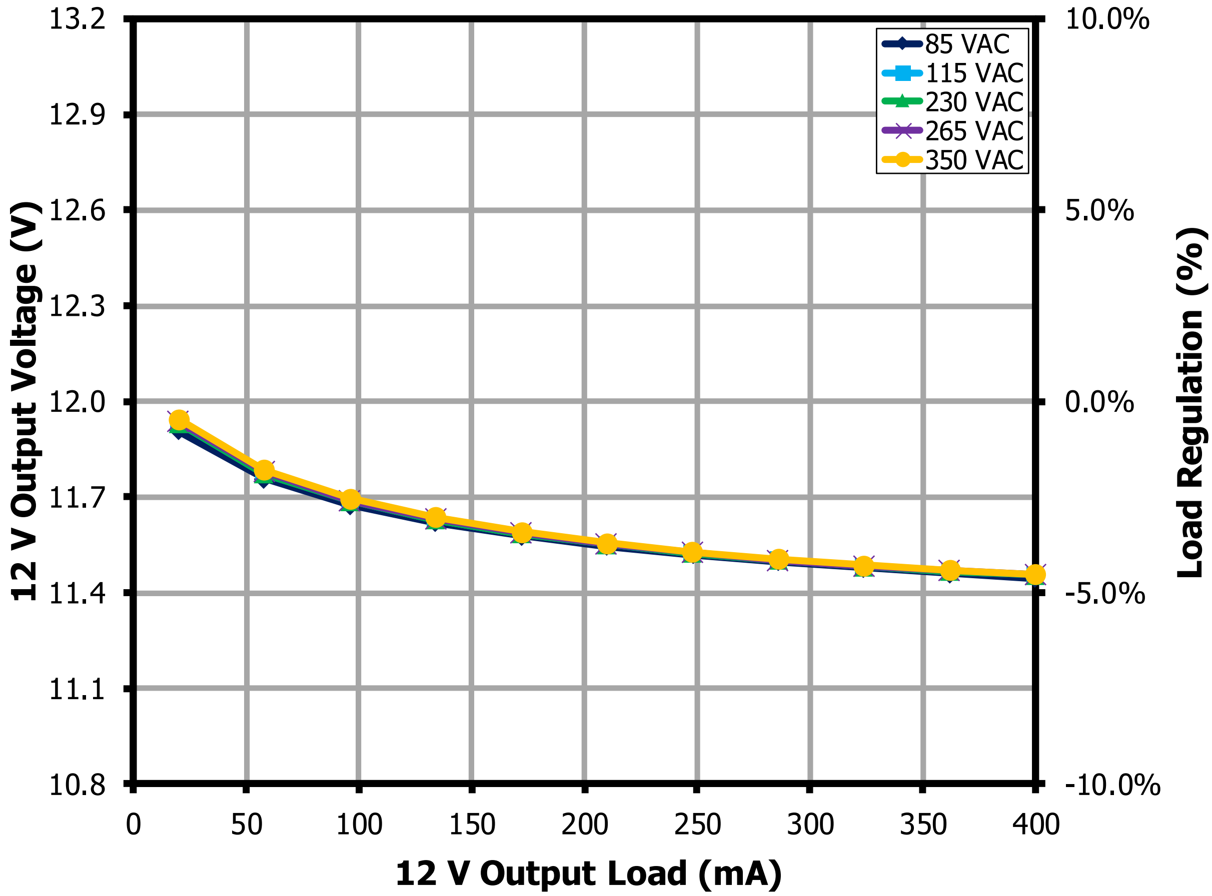

Figure 17 – 12 V Load Regulation with Fixed Full Load Across 5 V Output.

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9.4.6 12 V Load Regulation with Fixed Minimum Load Across 5 V Output

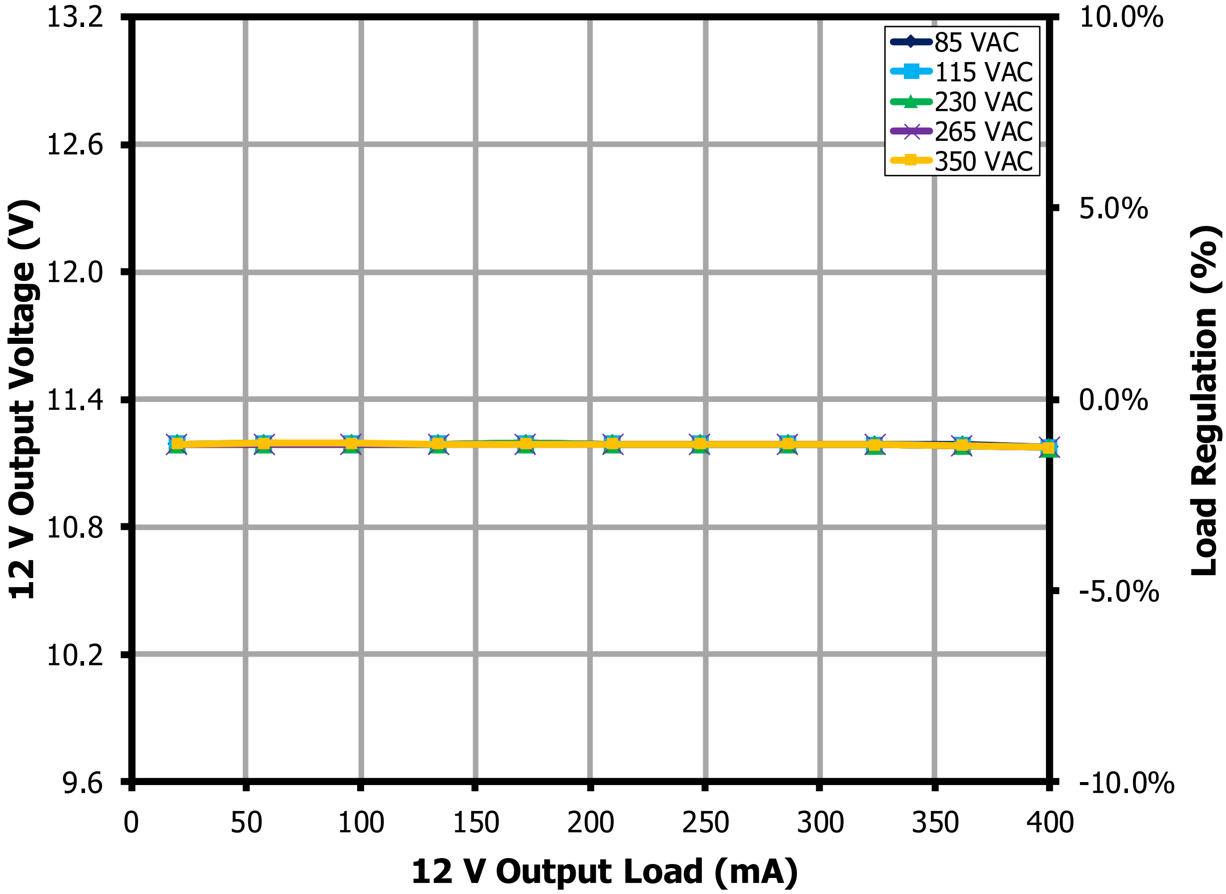

Figure 18 – 12 V Load Regulation with Fixed Minimum Load Across 5 V Output.

10 Test Waveforms

10.1 *Load Transient Response*

10.1.1 5 V and 12 V 0% - 100% Load Change

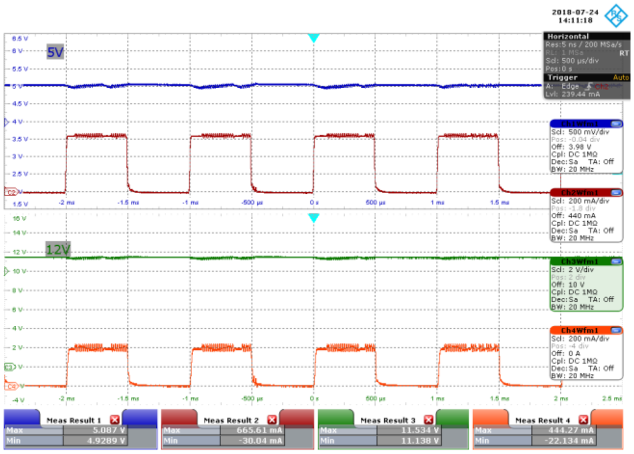

Figure 19 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.534 V, 12 V_{MIN}: 11.138 V.

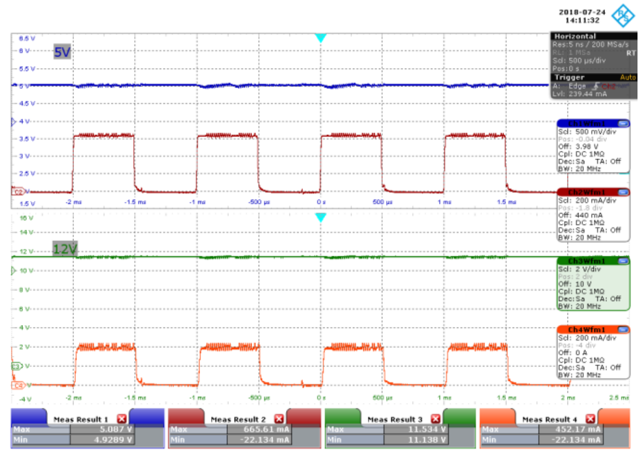

Figure 20 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.534 V, 12 V_{MIN}: 11.138 V.

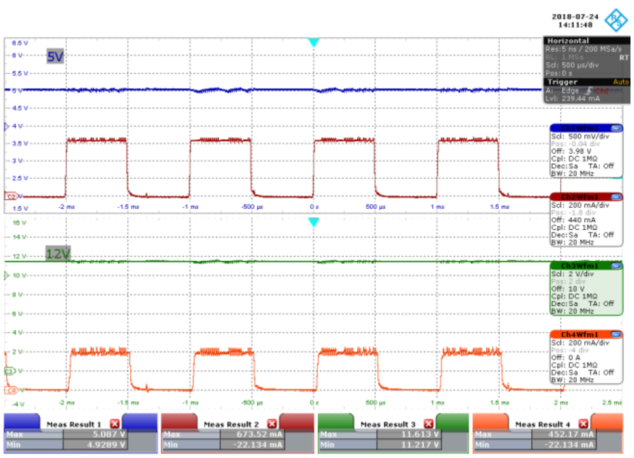

Figure 21 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.613 V, 12 V_{MIN}: 11.217 V .

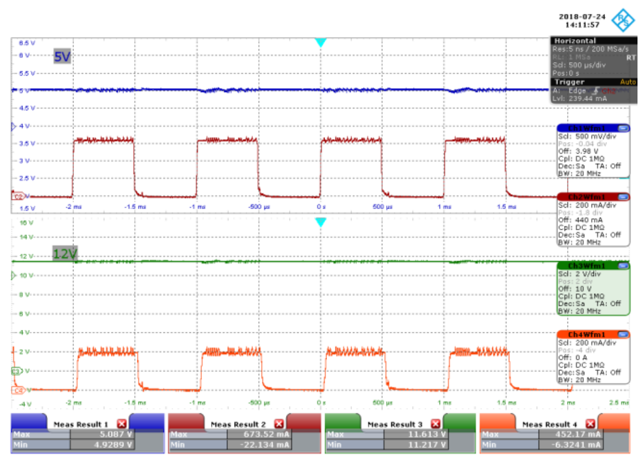

Figure 22 – 350 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.613 V, 12 V_{MIN}: 11.217 V.

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10.1.2 5 V and 12 V 0% - 50% Load Change

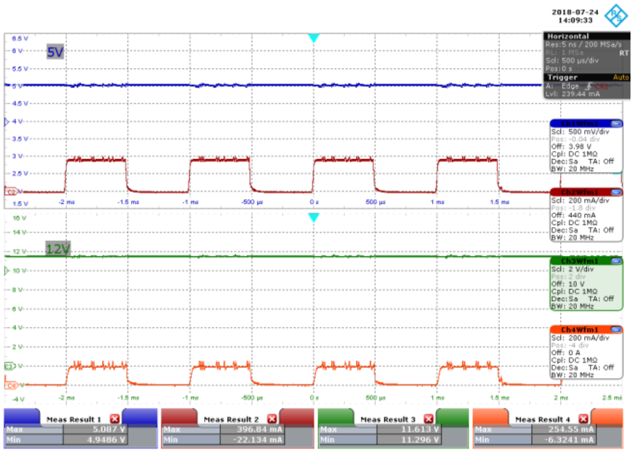

Figure 23 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.613 V, 12 V_{MIN}: 11.296 V.

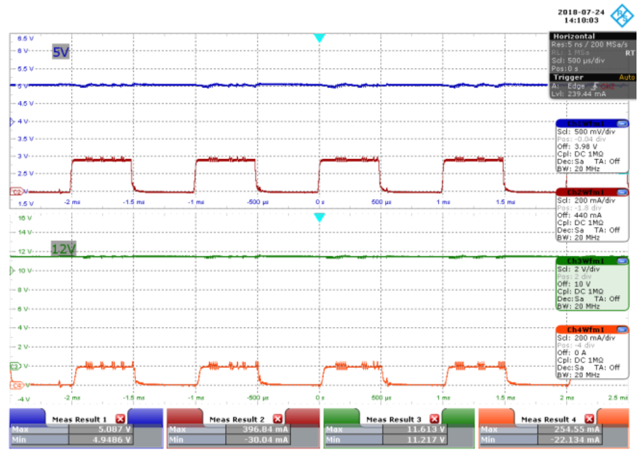

Figure 24 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.613 V, 12 V_{MIN}: 11.217 V.

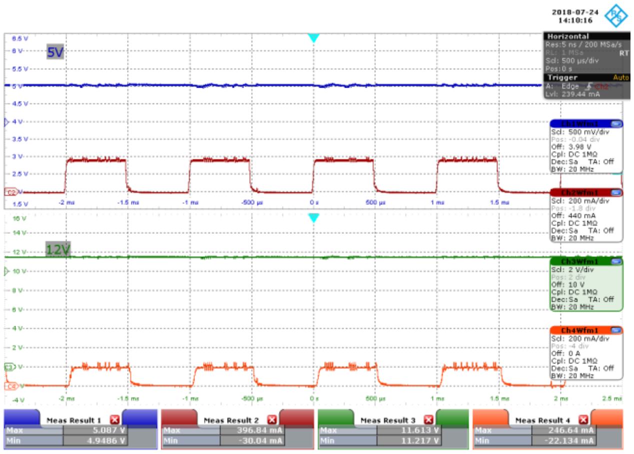

Figure 25 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.613 V, 12 V_{MIN}: 11.217 V.

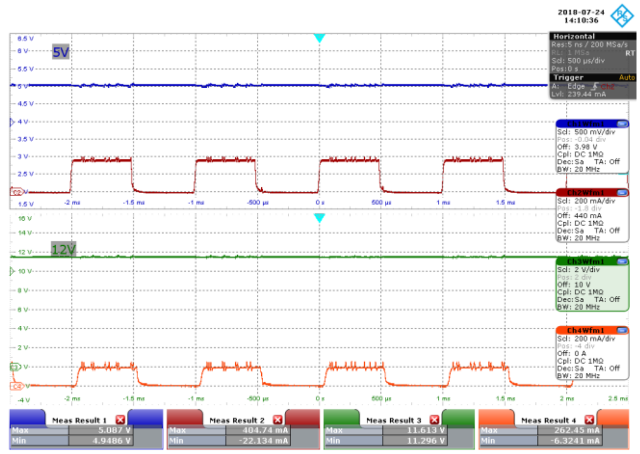

Figure 26 – 350 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.613 V, 12 V_{MIN}: 11.296 V.

10.1.3 5 V 0% - 100% Load Change, 12 V Fixed 100% Load

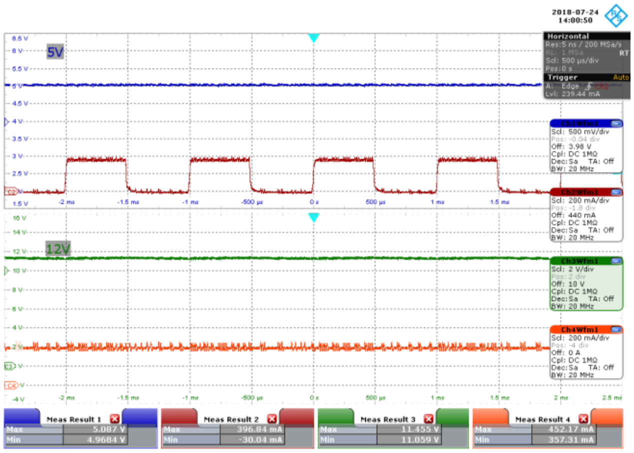

Figure 27 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.455 V, 12 V_{MIN}: 11.059 V.

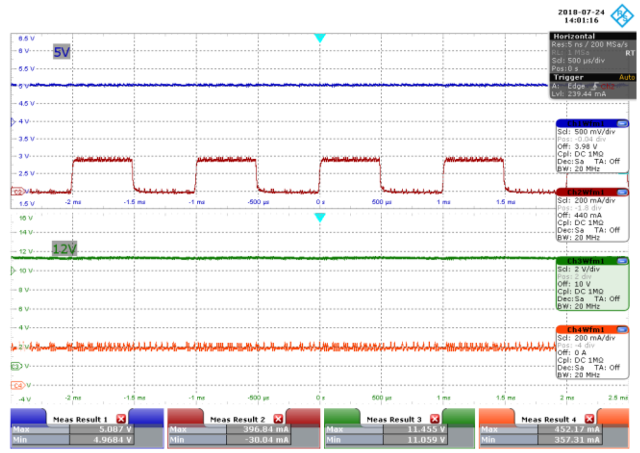

Figure 28 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.455 V, 12 V_{MIN}: 11.059 V.

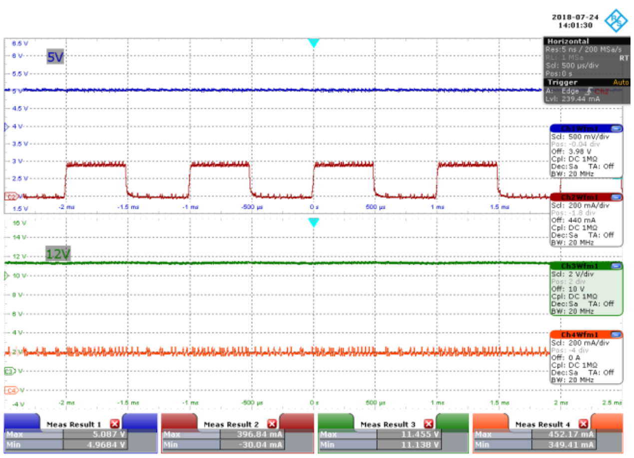

Figure 29 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.455 V, 12 V_{MIN}: 11.138 V.

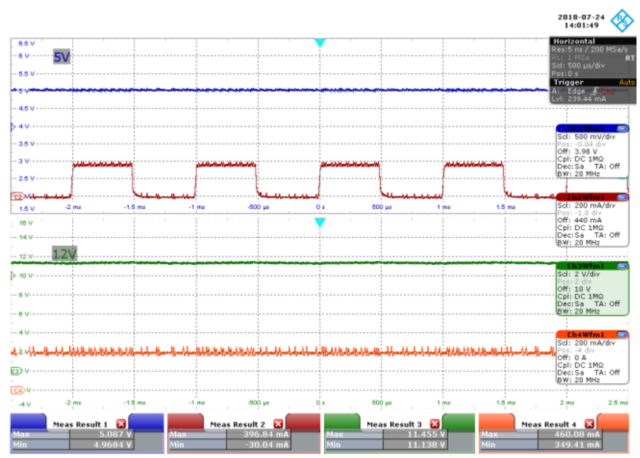

Figure 30 – 350 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.455 V, 12 V_{MIN}: 11.138 V.

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10.1.4 12 V 0% - 100% Load Change, 5 V Fixed 100% Load

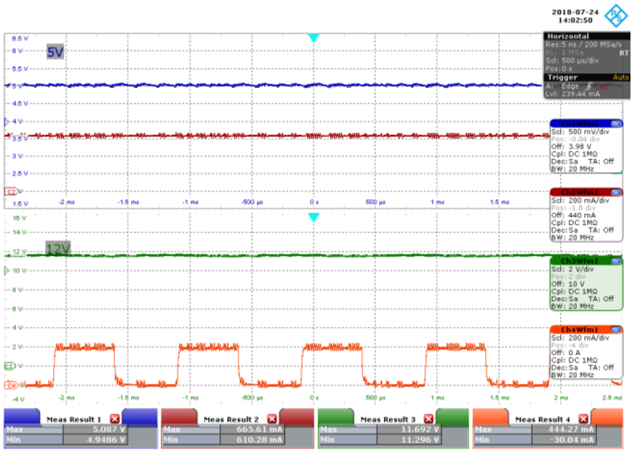

Figure 31 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.692 V, 12 V_{MIN}: 11.296 V.

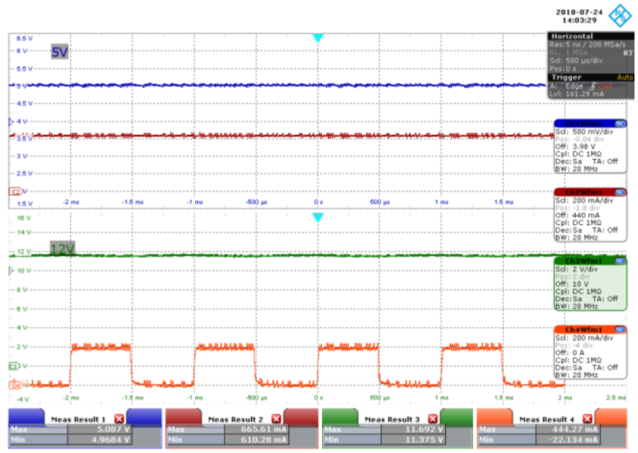

Figure 32 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.692 V, 12 V_{MIN}: 11.375 V.

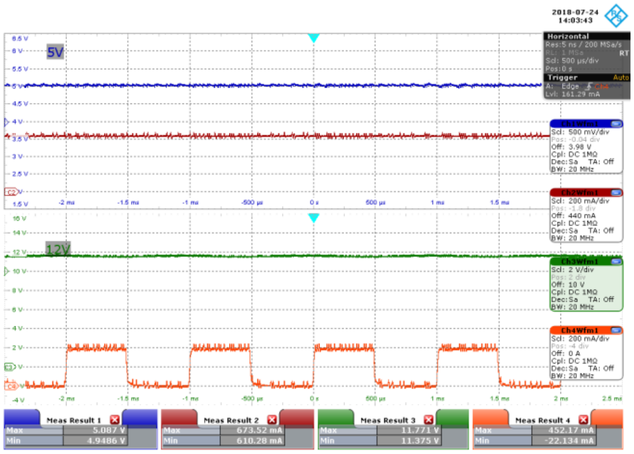

Figure 33 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.771 V, 12 V_{MIN}: 11.335 V.

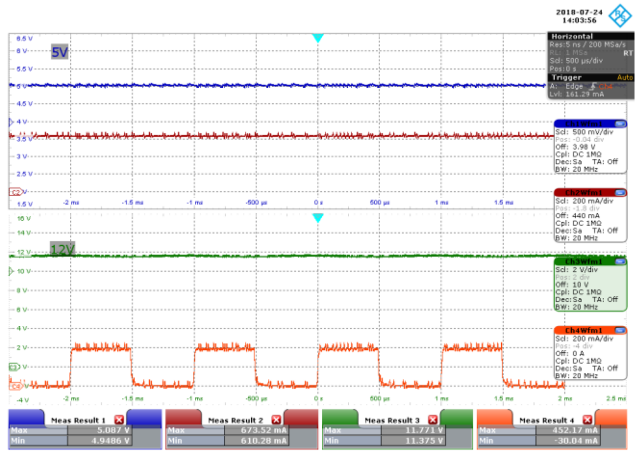

Figure 34 – 350 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 500 µs / div.
5 V_{MAX}: 5.087 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.771 V, 12 V_{MIN}: 11.375 V.

10.2 ***Output Voltage at Start-up***

10.2.1 CC Mode

10.2.1.1 100% Load

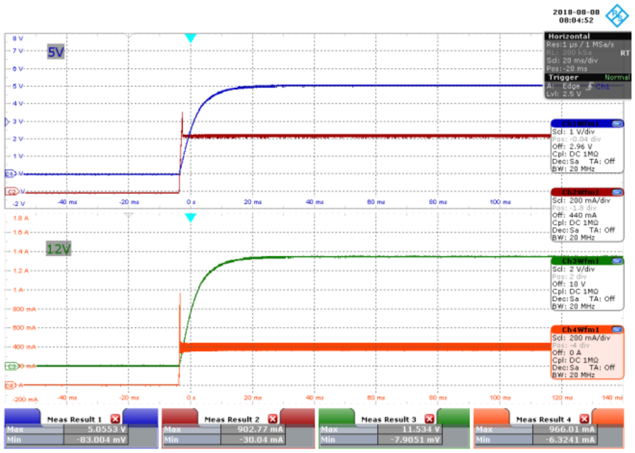

Figure 35 – 85 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

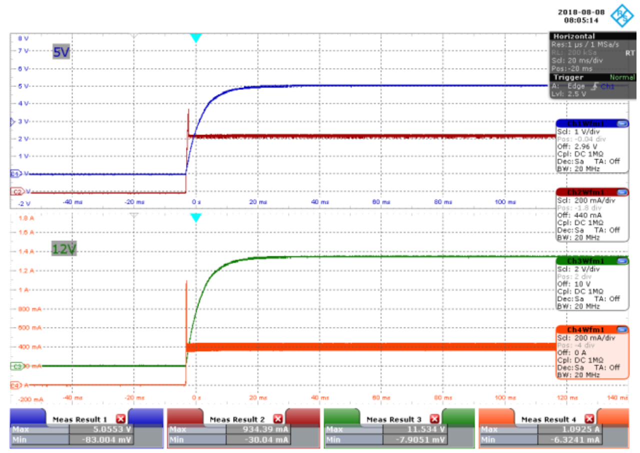

Figure 36 – 115 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

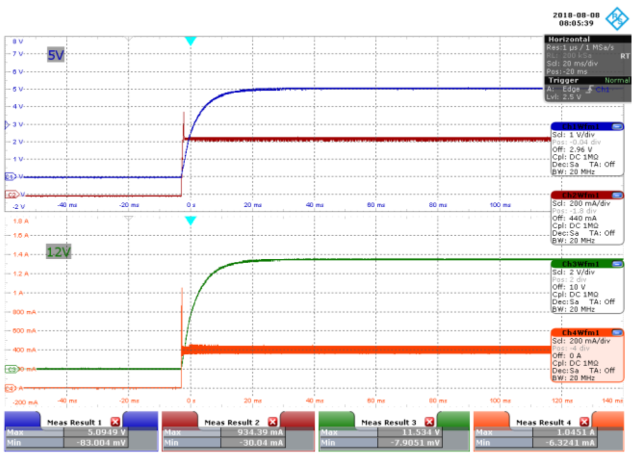

Figure 37 – 230 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

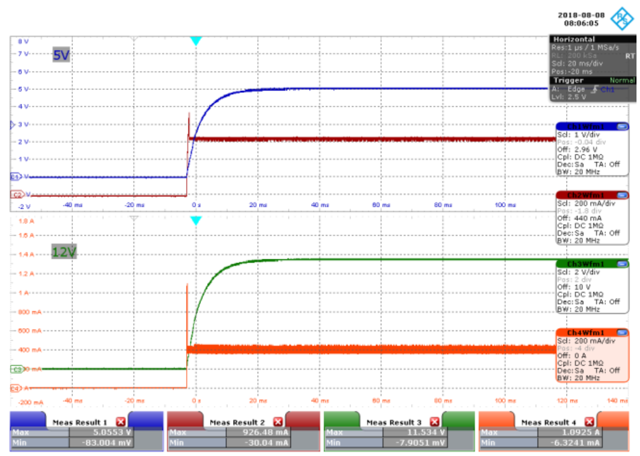

Figure 38 – 350 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

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10.2.1.2 0% Load

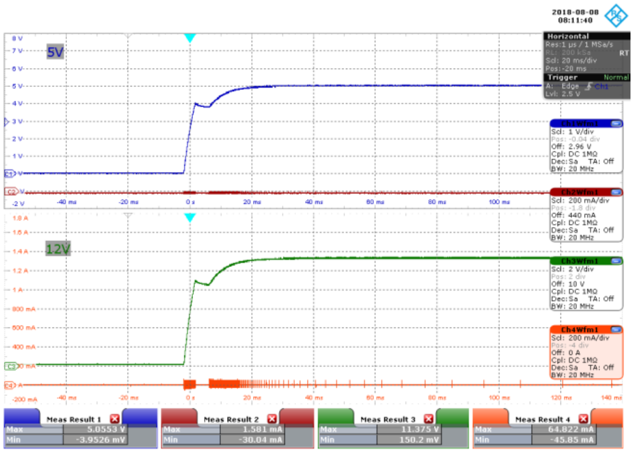

Figure 39 – 85 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

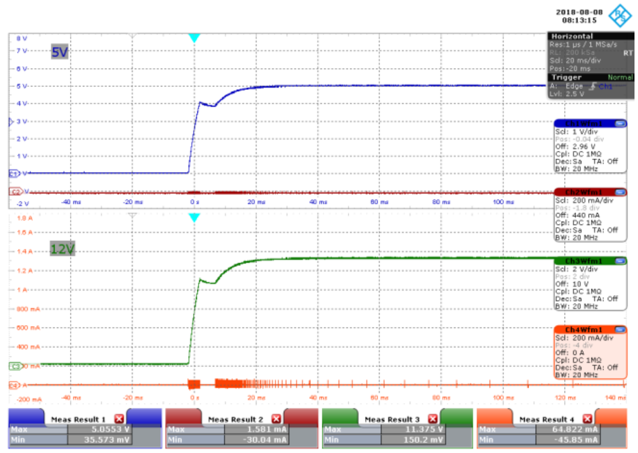

Figure 40 – 115 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

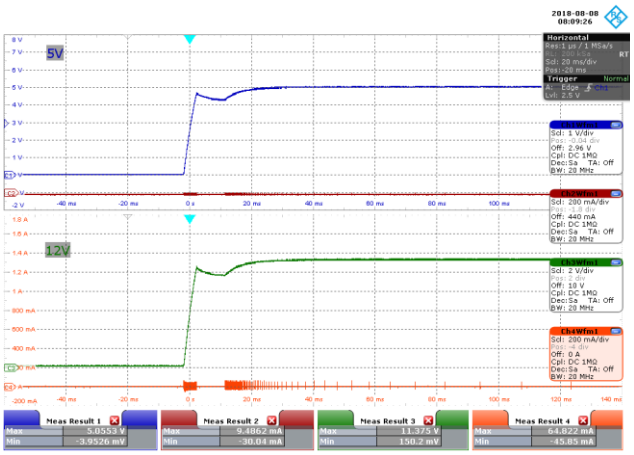

Figure 41 – 230 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

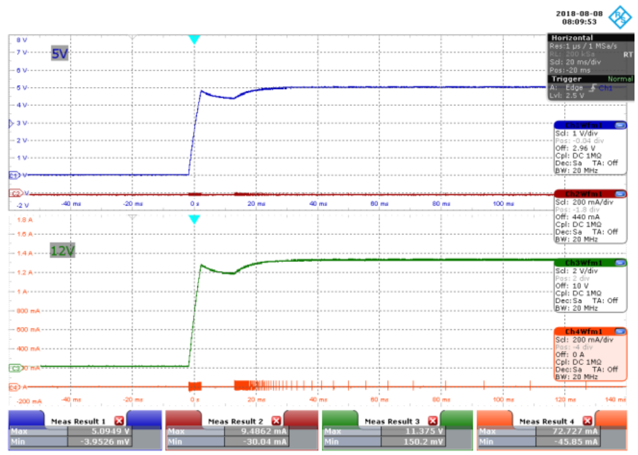

Figure 42 – 350 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

10.2.2 CR Mode

10.2.2.1 100% Load

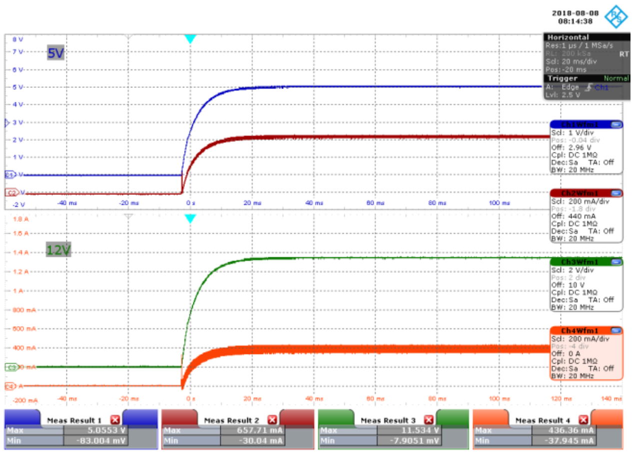

Figure 43 – 85 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

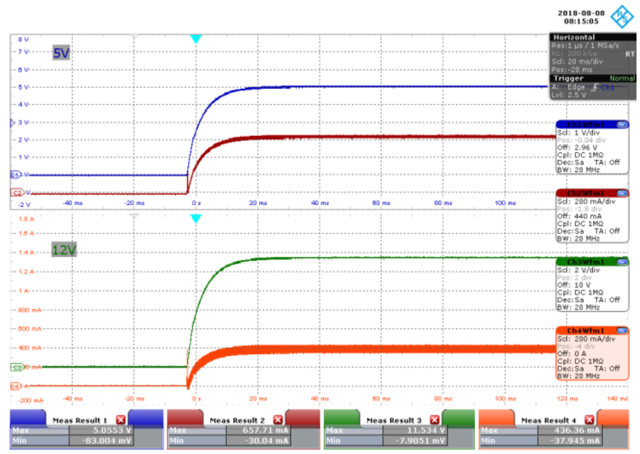

Figure 44 – 115 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

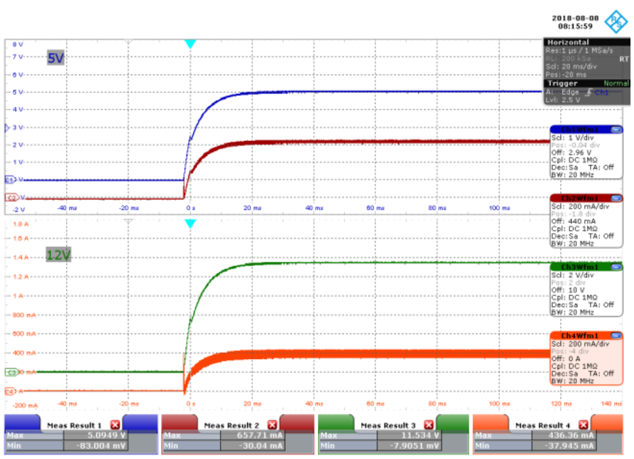

Figure 45 – 230 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

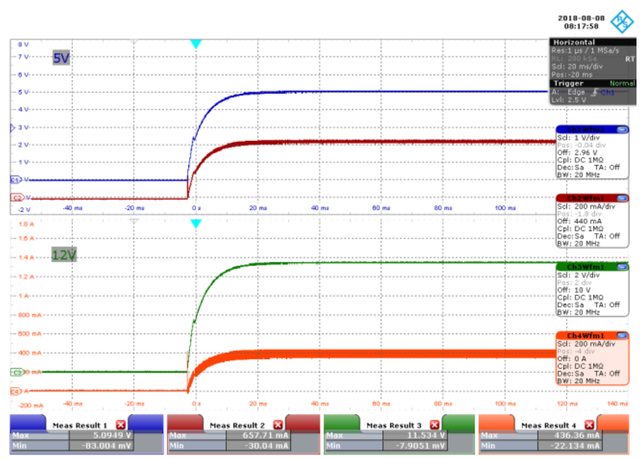

Figure 46 – 350 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 20 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 20 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 20 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 20 ms / div.

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10.2.2.2 0% Load

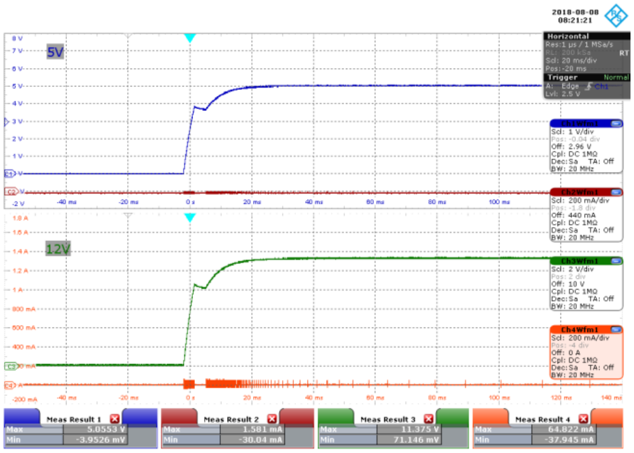

Figure 47 – 85 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 10 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 10 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 10 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 10 ms / div.

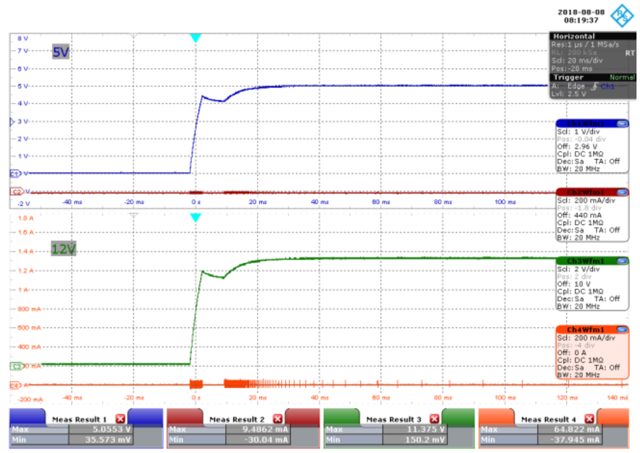

Figure 48 – 115 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 10 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 10 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 10 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 10 ms / div.

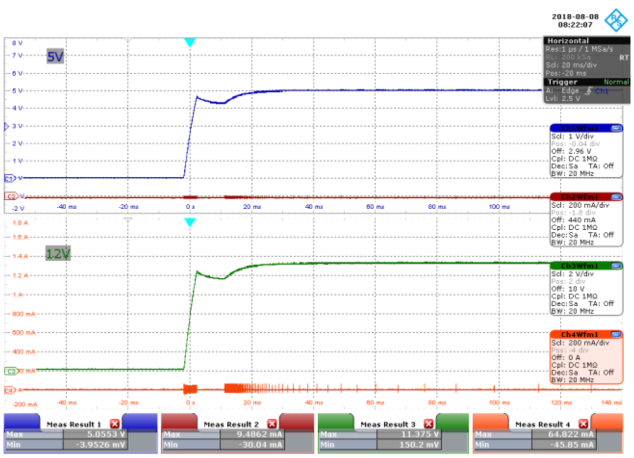

Figure 49 – 230 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 10 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 10 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 10 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 10 ms / div.

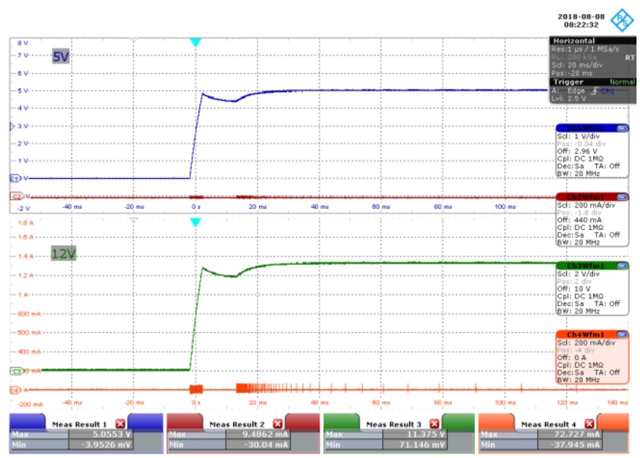

Figure 50 – 350 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 10 ms / div.
CH2: 5 V I_{LOAD}, 200 mA / div., 10 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 10 ms / div.
CH4: 12 V I_{LOAD}, 200 mA / div., 10 ms / div.

10.3 *Switching Waveforms*

10.3.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

10.3.1.1 100% Load

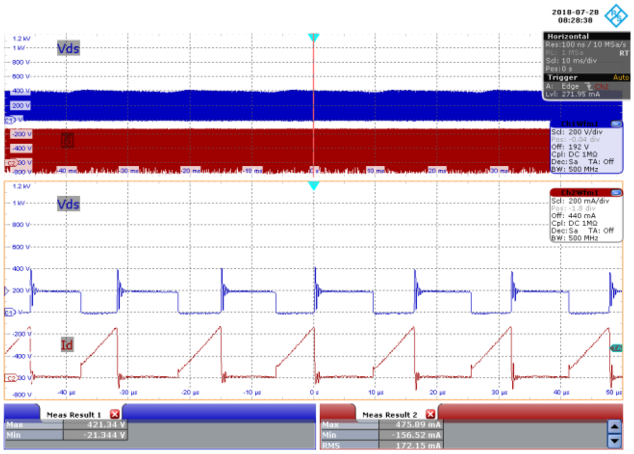

Figure 51 – 85 VAC 60 Hz, Full Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 421.34 V, $I_{DS(MAX)}$ = 475.9 mA.

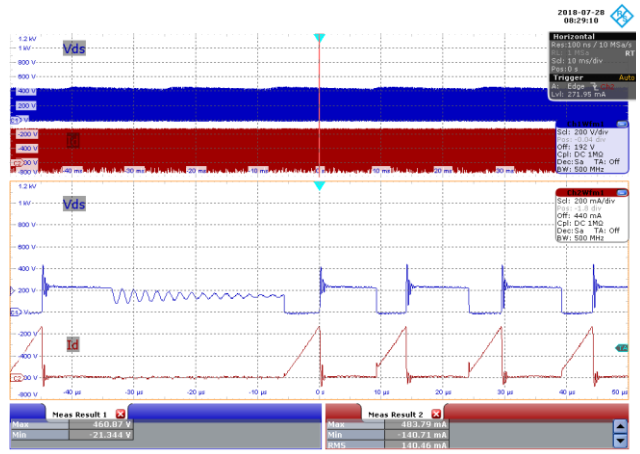

Figure 52 – 115 VAC 60 Hz, Full Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 460.87 V, $I_{DS(MAX)}$ = 483.8 mA.

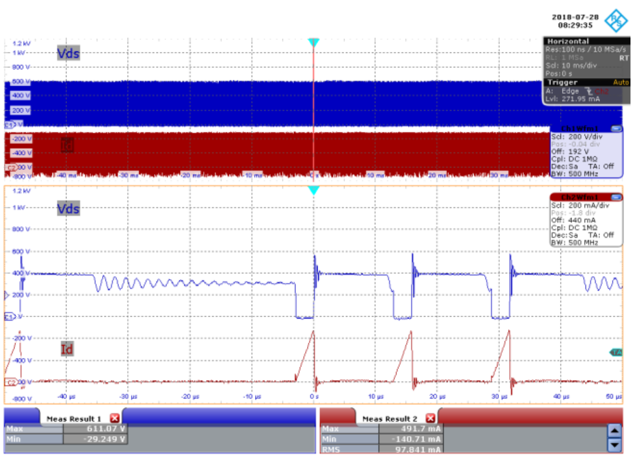

Figure 53 – 230 VAC 50 Hz, Full Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 611.07 V, $I_{DS(MAX)}$ = 491.7 mA.

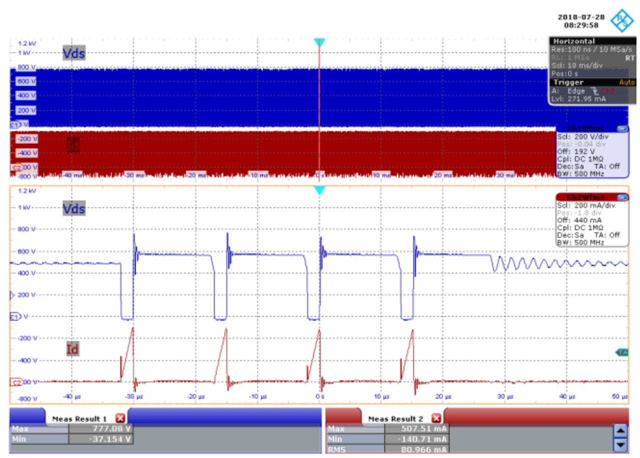

Figure 54 – 350 VAC 50 Hz, Full Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 777.08 V, $I_{DS(MAX)}$ = 507.51 mA.

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10.3.1.2 0% Load

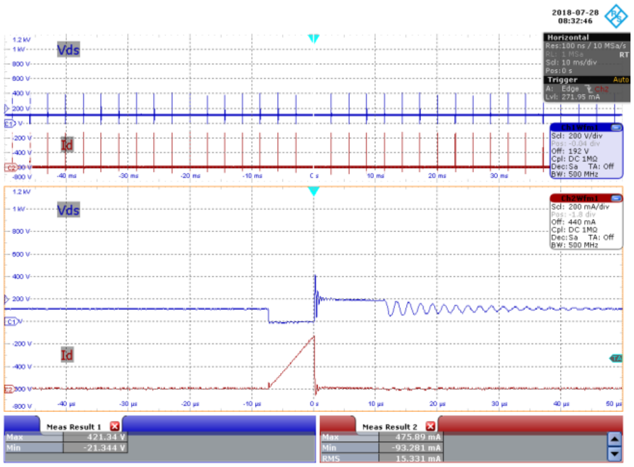

Figure 55 – 85 VAC 60 Hz, No-Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 421.34 V, $I_{DS(MAX)}$ = 475.89 mA.

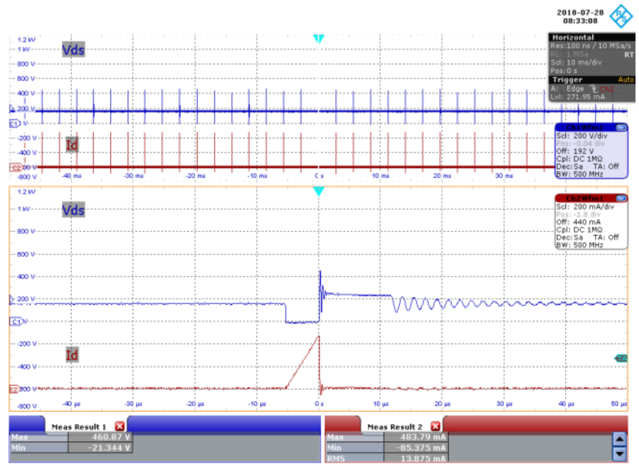

Figure 56 – 115 VAC 60 Hz, No-Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 460.87 V, $I_{DS(MAX)}$ = 489.79 mA.

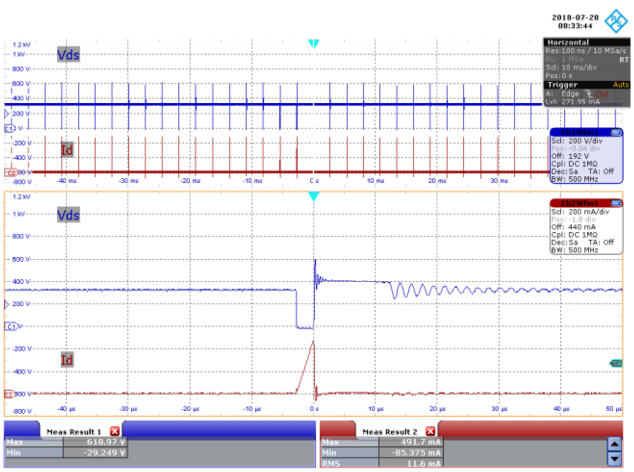

Figure 57 – 230 VAC 50 Hz, No-Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 618.97 V, $I_{DS(MAX)}$ = 491.7 mA.

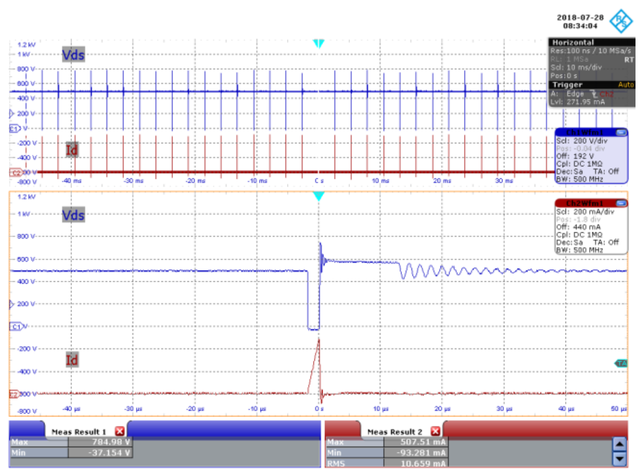

Figure 58 – 350 VAC 50 Hz, No-Load.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 784.98 V, $I_{DS(MAX)}$ = 507.51 mA.

10.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

10.3.2.1 100% Load

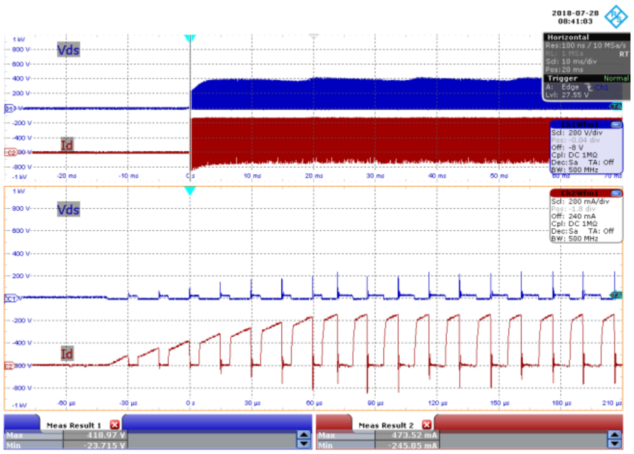

Figure 59 – 85 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 30 µs / div.
$V_{DS(MAX)}$ = 418.97 V, $I_{DS(MAX)}$ = 473.52 mA.

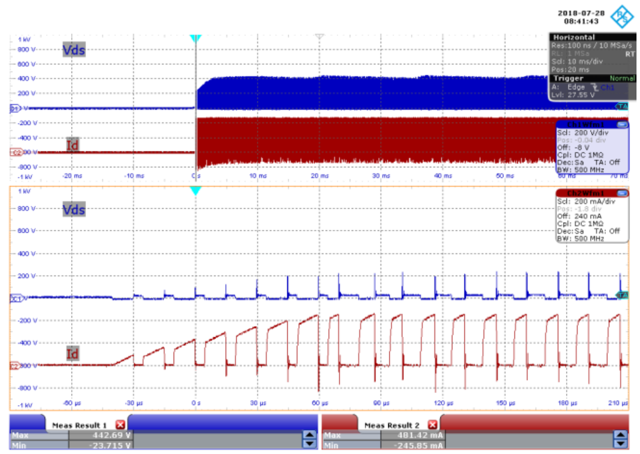

Figure 60 – 115 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 30 µs / div.
$V_{DS(MAX)}$ = 442.69 V, $I_{DS(MAX)}$ = 481.42 mA.

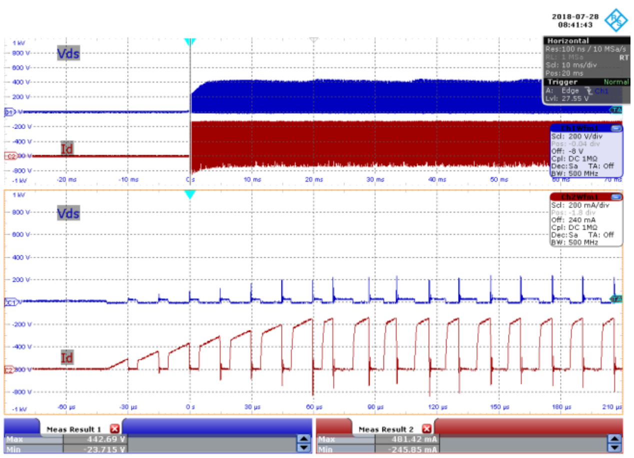

Figure 61 – 230 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 30 µs / div.
$V_{DS(MAX)}$ = 624.51 V, $I_{DS(MAX)}$ = 489.33 mA.

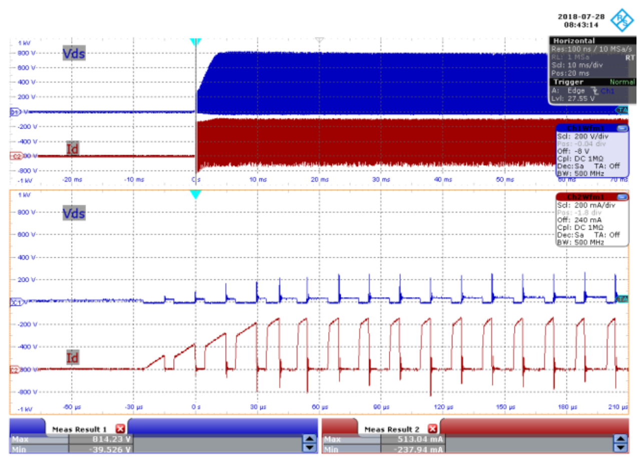

Figure 62 – 350 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 30 µs / div.
$V_{DS(MAX)}$ = 814.23 V, $I_{DS(MAX)}$ = 513.04 mA.

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10.3.3 5 V Output Diode Voltage and Current at Normal Operation

10.3.3.1 100% Load

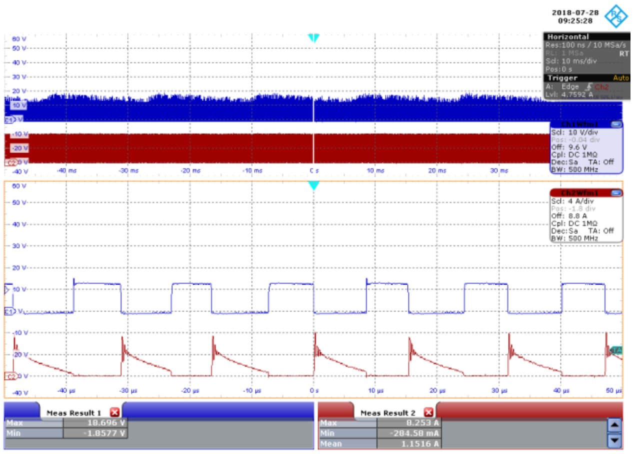

Figure 63 – 85 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\ V}$, 4 A / div., 10 ms / div.
Zoom: 10 μs / div.
5 V PIV_{MAX} = 18.696 V, $I_{AVE\_5\ V}$ = 1.15 A.

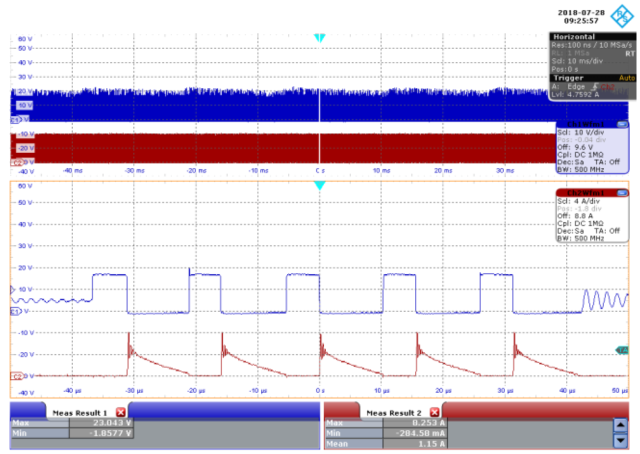

Figure 64 – 115 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\ V}$, 4 A / div., 10 ms / div.
Zoom: 10 μs / div.
5 V PIV_{MAX} = 23.043 V, $I_{AVE\_5\ V}$ = 1.15 A.

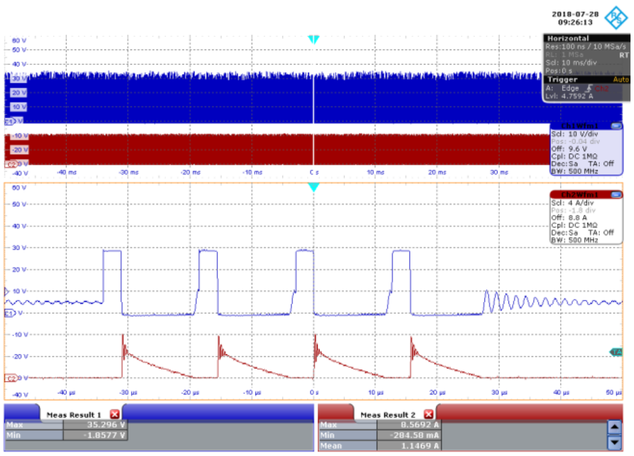

Figure 65 – 230 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\ V}$, 4 A / div., 10 ms / div.
Zoom: 10 μs / div.
5 V PIV_{MAX} = 35.296 V, $I_{AVE\_5\ V}$ = 1.147 A.

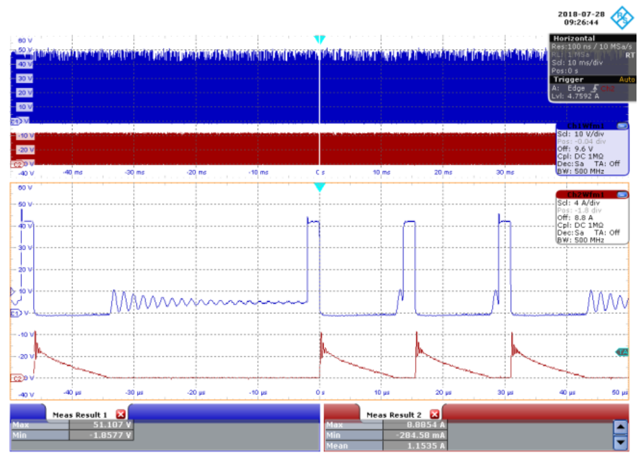

Figure 66 – 350 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\ V}$, 4 A / div., 10 ms / div.
Zoom: 10 μs / div.
5 V PIV_{MAX} = 51.107 V, $I_{AVE\_5\ V}$ = 1.1535 A.

10.3.3.2 0% Load

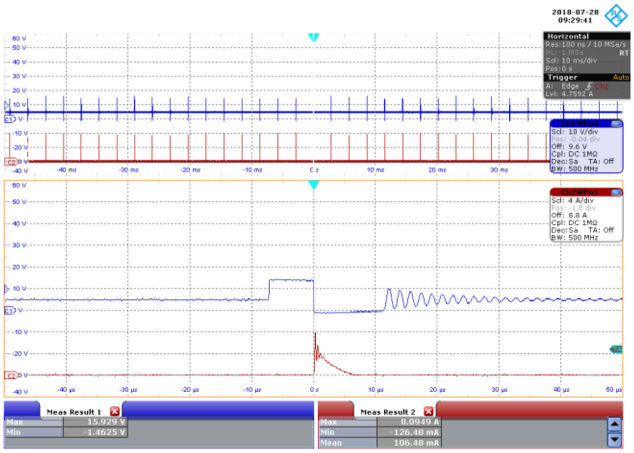

Figure 67 – 85 VAC 60 Hz, No-Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 15.929 V, $I_{AVE\_5\,V}$ = 0.1065 A.

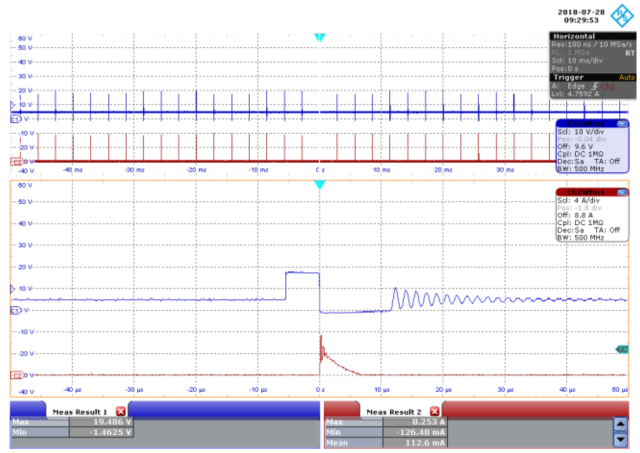

Figure 68 – 115 VAC 60 Hz, No-Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 19.486 V, $I_{AVE\_5\,V}$ = 0.1126 A.

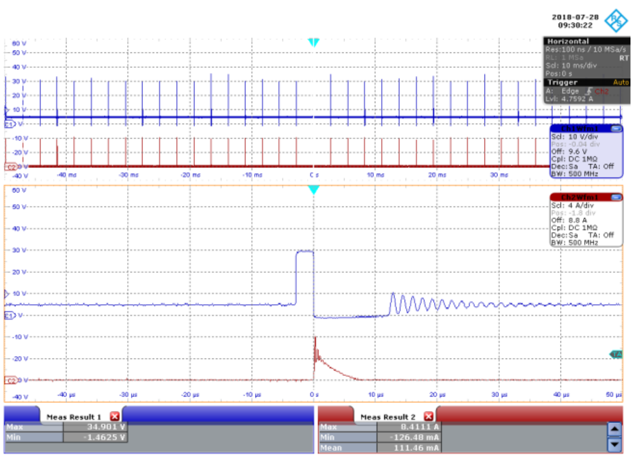

Figure 69 – 230 VAC 50 Hz, No-Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 34.901 V, $I_{AVE\_5\,V}$ = 0.1115 A.

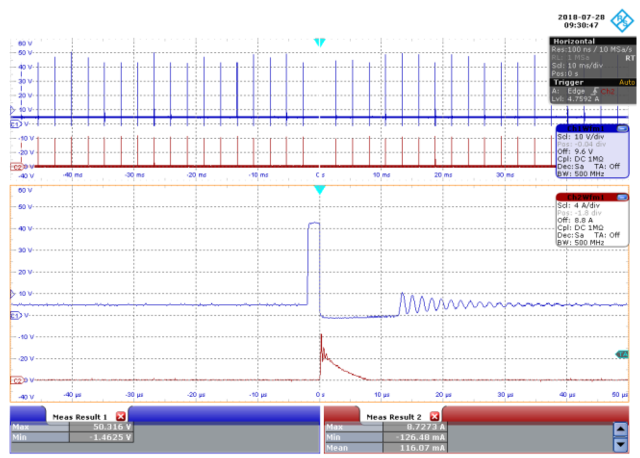

Figure 70 – 350 VAC 50 Hz, No-Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 50.316 V, $I_{AVE\_5\,V}$ = 0.1161 A.

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10.3.4 5 V Output Diode Voltage and Current at Start-up Operation

10.3.4.1 100% Load

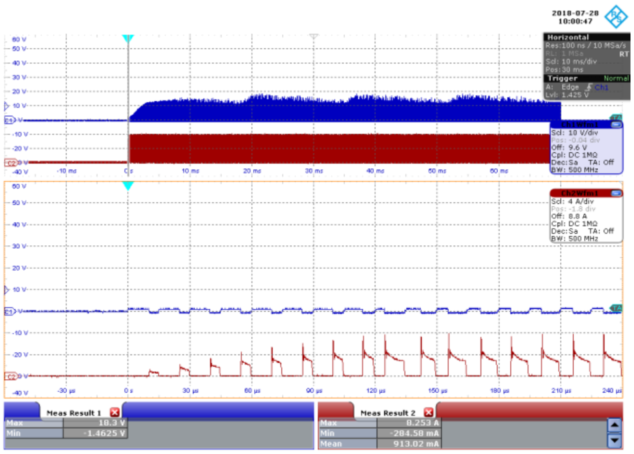

Figure 71 – 85 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 18.3 V, $I_{MAX\_5\,V}$ = 8.253 A.

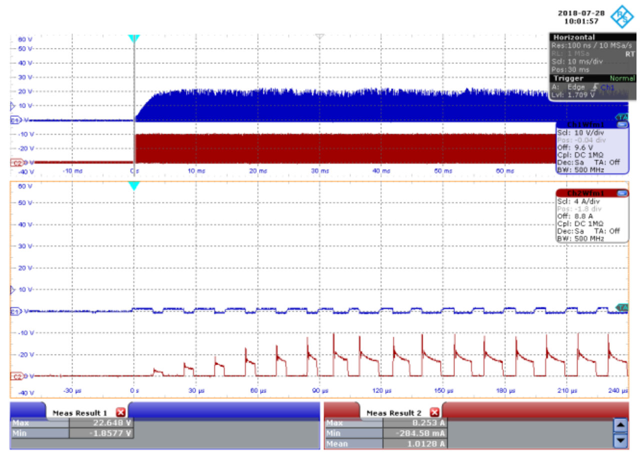

Figure 72 – 115 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 22.648 V, $I_{AVE\_5\,V}$ = 8.253 A.

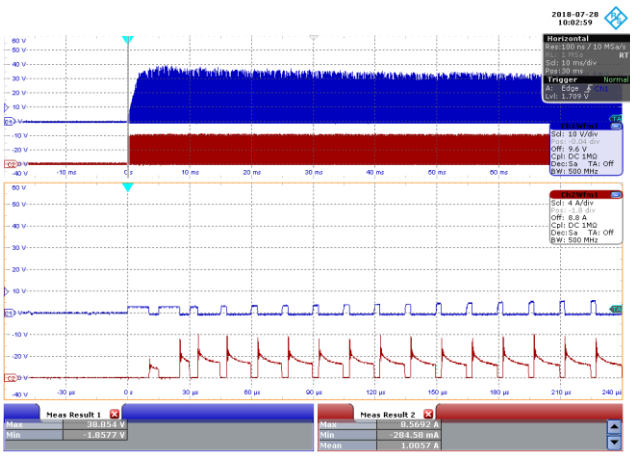

Figure 73 – 230 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 38.854 V, $I_{AVE\_5\,V}$ = 8.5642 A.

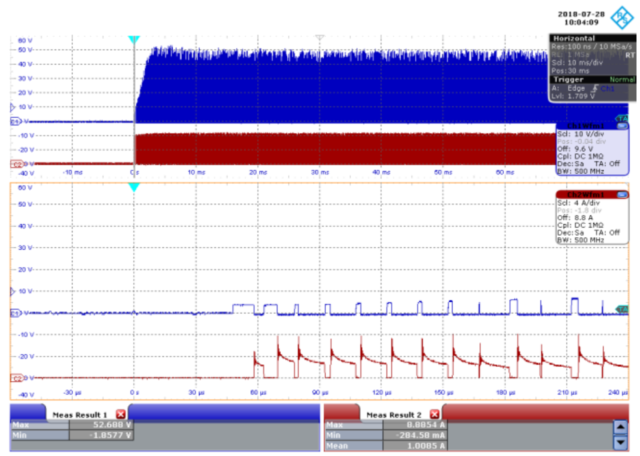

Figure 74 – 350 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_Diode}, 10 V / div., 10 ms / div.
CH2: 5 V $I_{AVE\_5\,V}$, 4 A / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 52.688 V, $I_{AVE\_5\,V}$ = 8.8854 A.

10.3.5 12 V Output Diode and Current Voltage at Normal Operation

10.3.5.1 100% Load

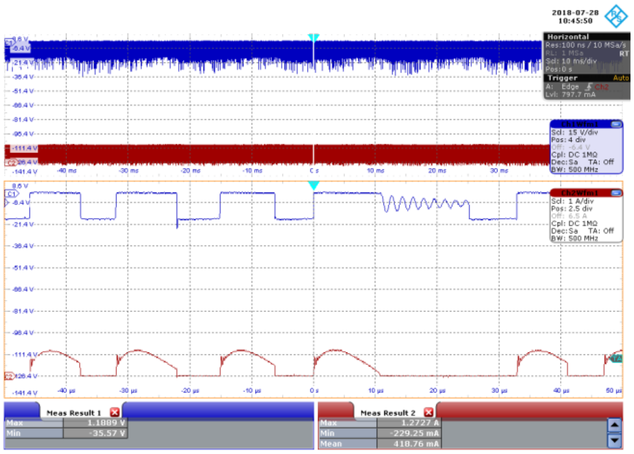

Figure 75 – 85 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 35.57 V, $I_{AVE\_12\ V}$ = 0.4187 A.

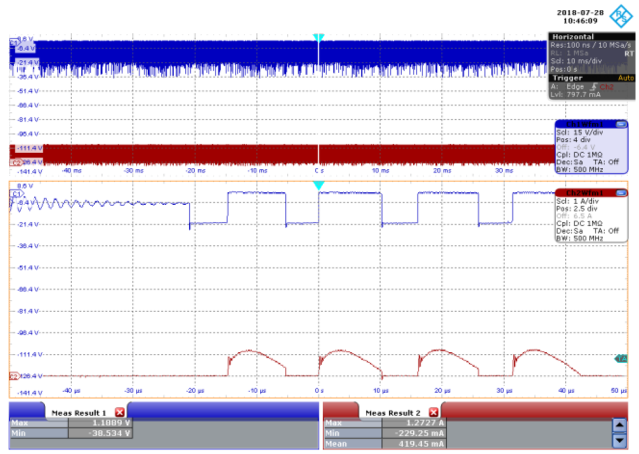

Figure 76 – 115 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 38.534 V, $I_{AVE\_12\ V}$ = 0.4194 A.

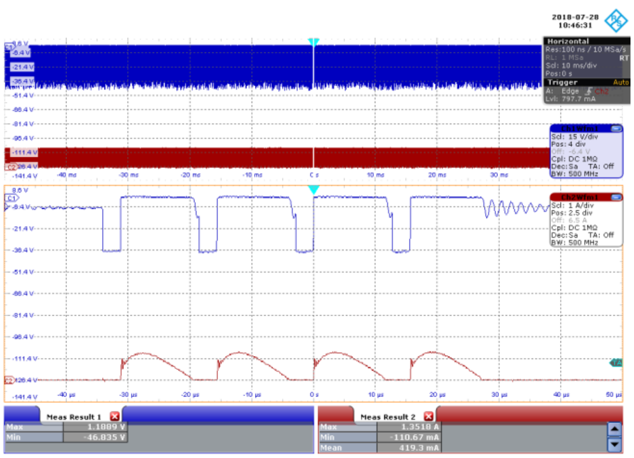

Figure 77 – 230 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_5\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 46.835 V, $I_{AVE\_12\ V}$ = 0.4193 A.

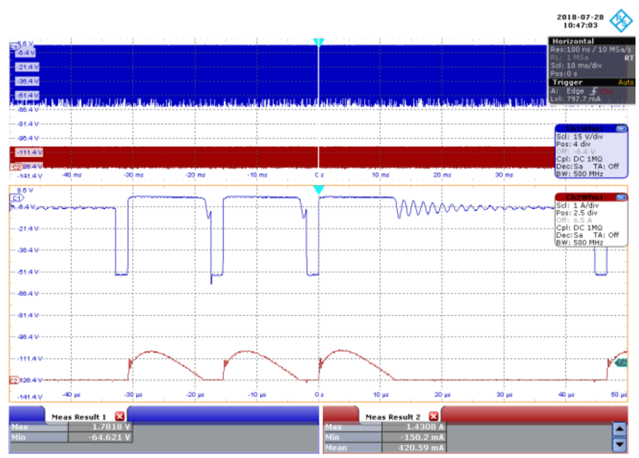

Figure 78 – 350 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_5\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 64.621 V, $I_{AVE\_12\ V}$ = 0.4206 A.

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10.3.5.2 0% Load

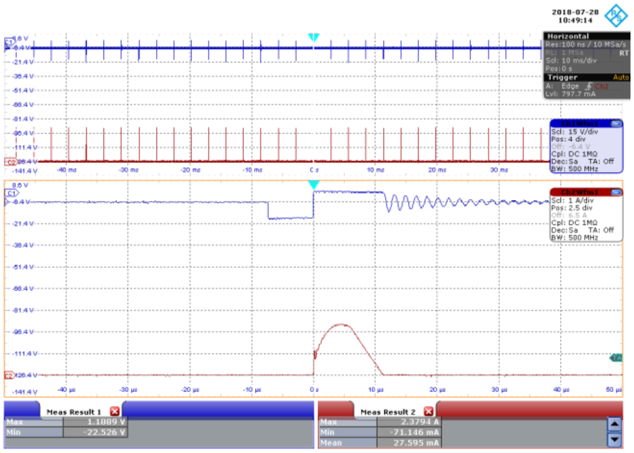

Figure 79 – 85 VAC 60 Hz, No-Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 22.256 V, $I_{AVE\_12\ V}$ = 0.0276 A.

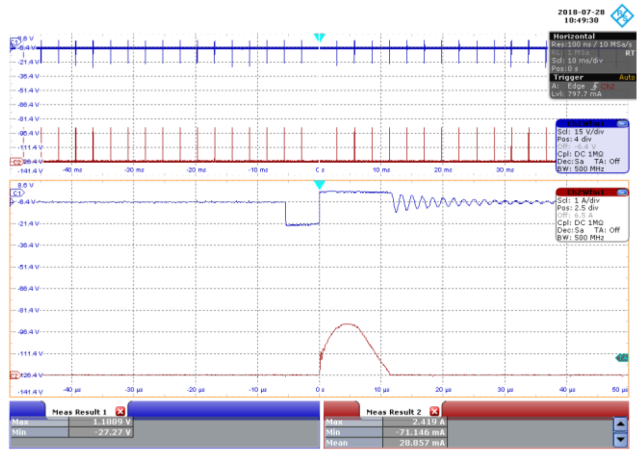

Figure 80 – 115 VAC 60 Hz, No-Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 27.27 V, $I_{AVE\_12\ V}$ = 0.0286 A.

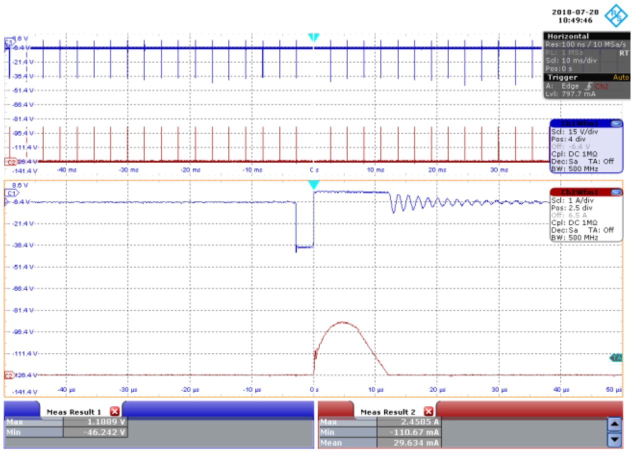

Figure 81 – 230 VAC 50 Hz, No-Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 46.242 V, $I_{AVE\_12\ V}$ = 0.0296 A.

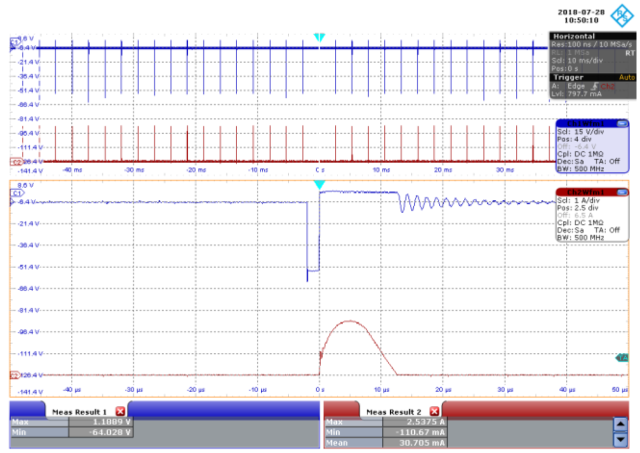

Figure 82 – 350 VAC 50 Hz, No-Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\ V}$, 1 A / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 64.028 V, $I_{AVE\_12\ V}$ = 0.0307 A.

10.3.6 12 V Output Diode Voltage and Current at Start-up Operation

10.3.6.1 100% Load

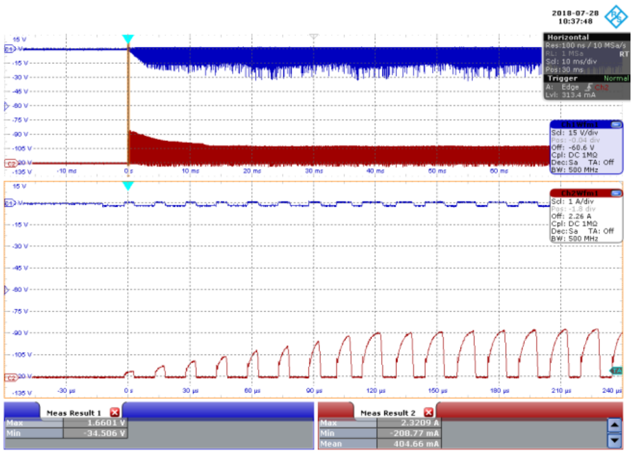

Figure 83 – 85 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\,V}$, 1 A / div., 10 ms / div.
Zoom: 30 μs / div.
12 V PIV_{MAX} = 34.506 V, $I_{MAX\_12\,V}$ = 2.2309 A.

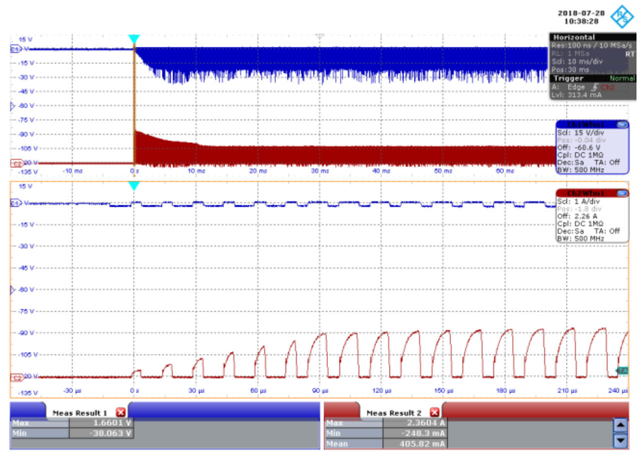

Figure 84 – 115 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\,V}$, 1 A / div., 10 ms / div.
Zoom: 30 μs / div.
12 V PIV_{MAX} = 38.063 V, $I_{AVE\_12\,V}$ = 2.3604 A.

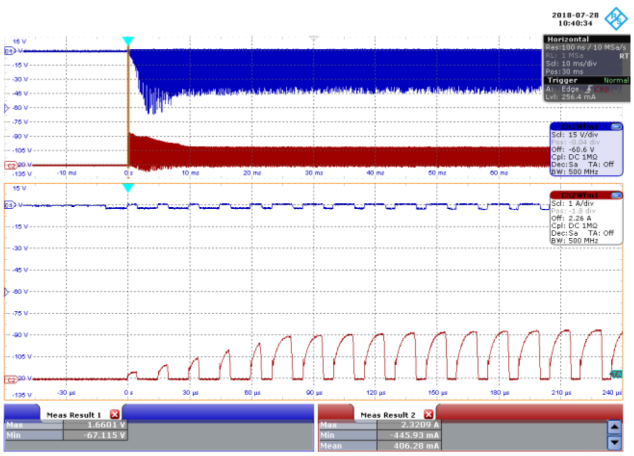

Figure 85 – 230 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\,V}$, 1 A / div., 10 ms / div.
Zoom: 30 μs / div.
12 V PIV_{MAX} = 67.115 V, $I_{AVE\_12\,V}$ = 2.2309 A.

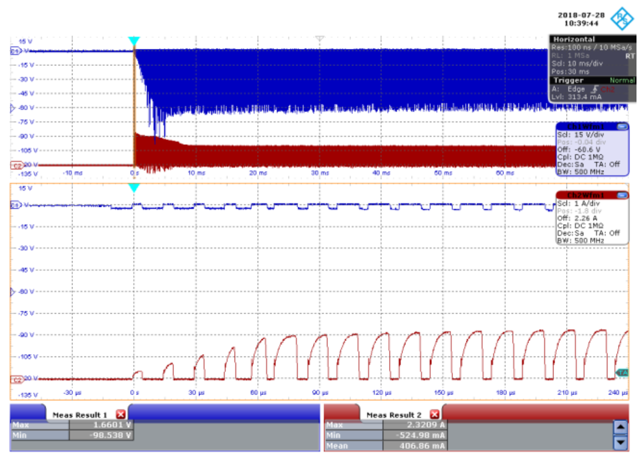

Figure 86 – 350 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_Diode}, 15 V / div., 10 ms / div.
CH2: 12 V $I_{AVE\_12\,V}$, 1 A / div., 10 ms / div.
Zoom: 30 μs / div.
12 V PIV_{MAX} = 98.538 V, $I_{AVE\_12\,V}$ = 2.3209 A.

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10.4 ***Brown-in / Brown-out Test***

No abnormal overheating or voltage overshoot / undershoot was observed during and after 0.1 V / s brown-in and brown-out test.

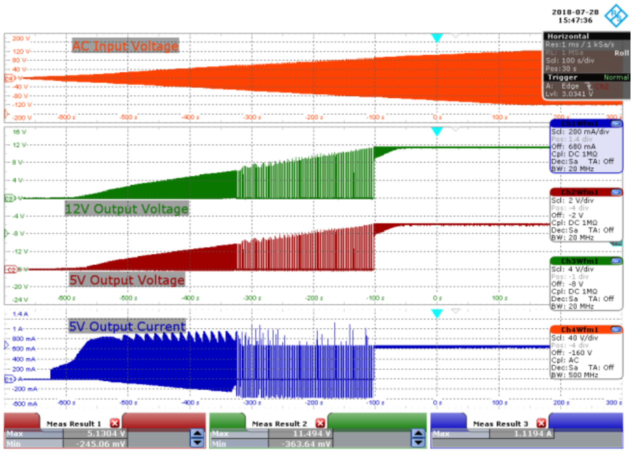

Figure 87 – Brown-in Test.
0 to 85 VAC 0.1 V / s.
CH1: 5 V I_{OUT}, 200 mA / div., 100 s /div.
CH2: 5 V_{OUT}, 2 V / div., 100 s / div.
CH3: 12 V_{OUT}, 4 V / div., 100 s / div.
CH4: AC_{IN}, 40 V / div., 100 s /div.
Highest Average Input Power: 10.754 W at 62.534 VAC.

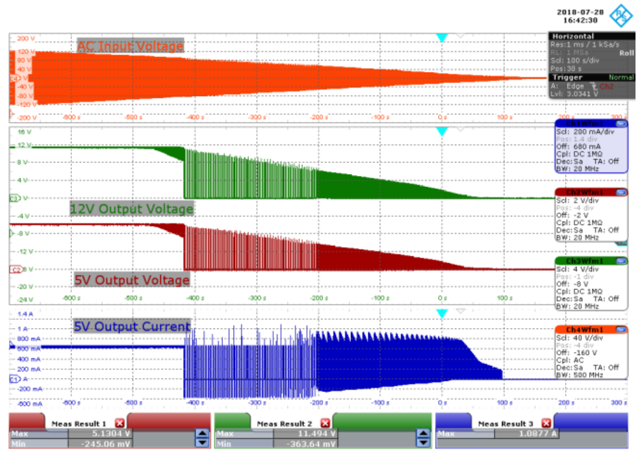

Figure 88 – Brown-out Test.
85 to 0 VAC 0.1 V / s.
CH1: 5 V I_{OUT}, 200 mA / div., 100 s /div.
CH2: 5 V_{OUT}, 2 V / div., 100 s / div.
CH3: 12 V_{OUT}, 4 V / div., 100 s / div.
CH4: AC_{IN}, 40 V / div., 100 s /div.
Highest Average Input Power: 10.721 W at 64.2 VAC.

10.5 ***Fault Conditions***

10.5.1 Output Short-Circuit

Test Condition: 5 V and 12 V output are shorted at the end of the cable.

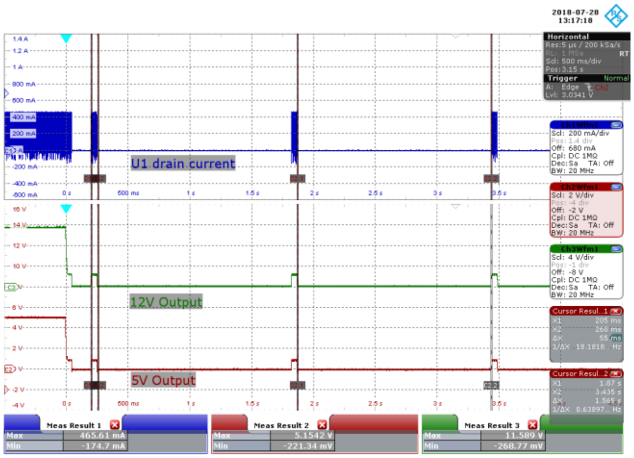

Figure 89 – 85 VAC, Short-Circuit during Normal Running Operation.
CH1: U1 I_{DRAIN}, 200 mA / div., 500 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 500 ms / div.
CH3: 12 V_{OUT}, 4 V / div., 500 ms / div.
$t_{AR(ON)}$: 55 ms.
$t_{AR(OFF)}$: 1.565 s.

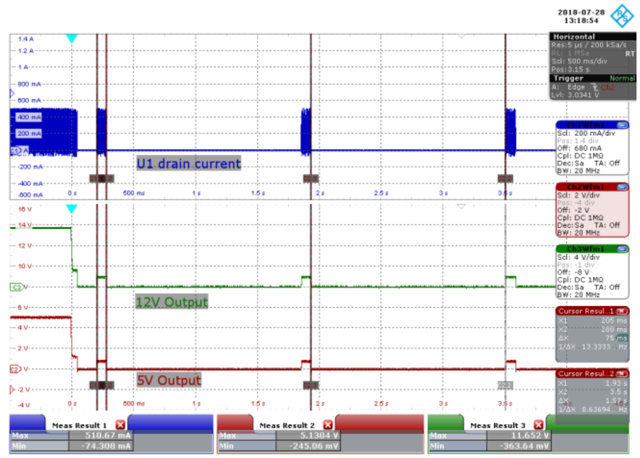

Figure 90 – 350 VAC, Short-Circuit during Normal Running Operation.
CH1: U1 I_{DRAIN}, 200 mA / div., 500 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 500 ms / div.
CH3: 12 V_{OUT}, 4 V / div., 500 ms / div.
$t_{AR(ON)}$: 75 ms.
$t_{AR(OFF)}$: 1.57 s.

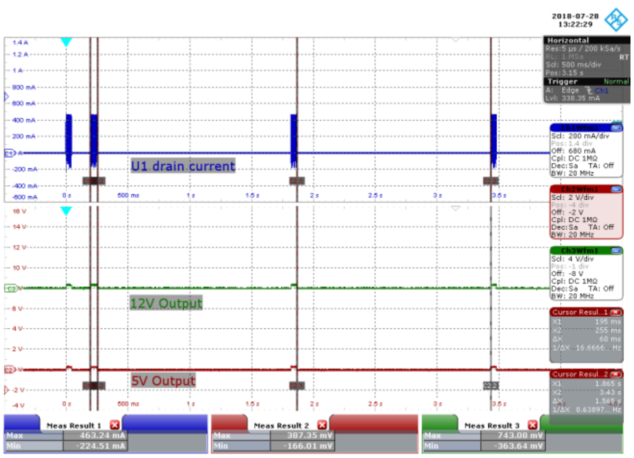

Figure 91 – 85 VAC, Short-Circuit during Start-up.
CH1: U1 I_{DRAIN}, 200 mA / div., 500 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 500 ms / div.
CH3: 12 V_{OUT}, 4 V / div., 500 ms / div.
$t_{AR(ON)}$: 60 ms.
$t_{AR(OFF)}$: 1.565 s.

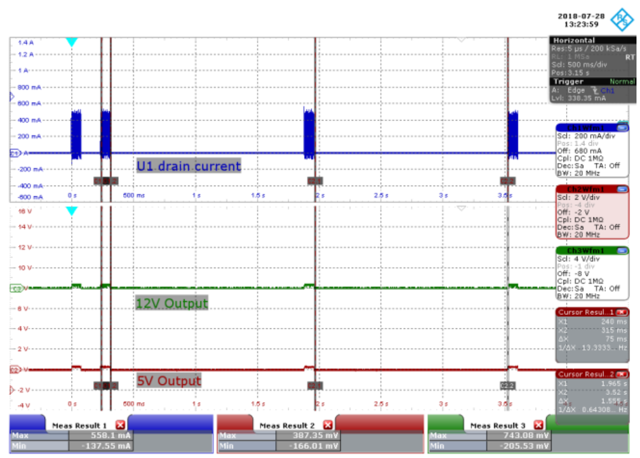

Figure 92 – 350 VAC, Short-Circuit during Start-up.
CH1: U1 I_{DRAIN}, 200 mA / div., 500 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 500 ms / div.
CH3: 12 V_{OUT}, 4 V / div., 500 ms / div.
$t_{AR(ON)}$: 75 ms.
$t_{AR(OFF)}$: 1.555 s.

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10.5.2 Line Overvoltage

Test Condition: Line Overvoltage Protection set to 402.5 VAC (+15% of 350 VAC)

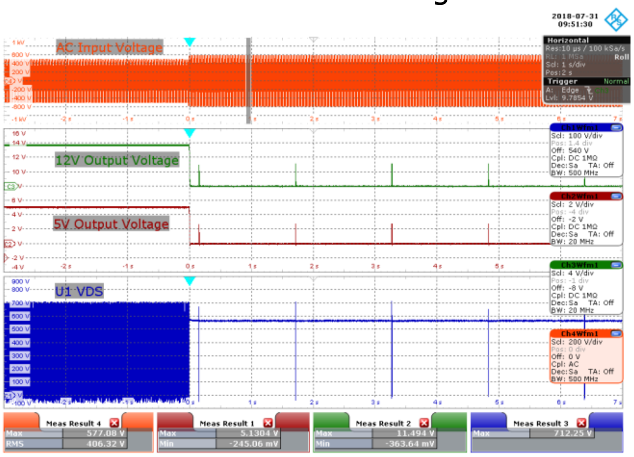

Figure 93 – Line Overvoltage during Normal Running Operation.
CH1: U1 V_{DS}, 100 V / div., 1 s /div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
CH4: AC_{IN}, 200 V / div., 1 s /div.

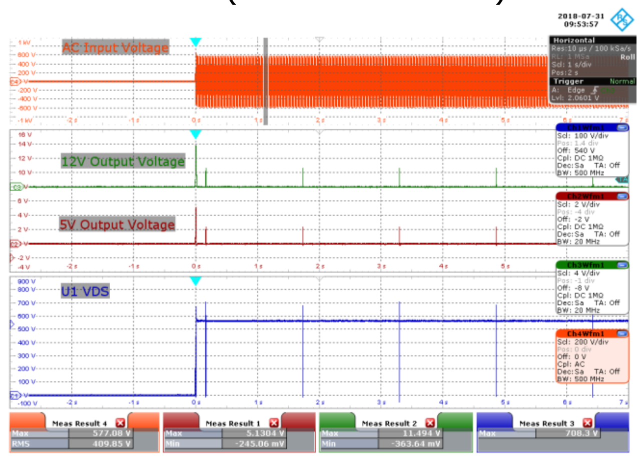

Figure 94 – Line Overvoltage during Start-up.
CH1: U1 V_{DS}, 100 V / div., 1 s /div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
CH4: AC_{IN}, 200 V / div., 1 s /div.

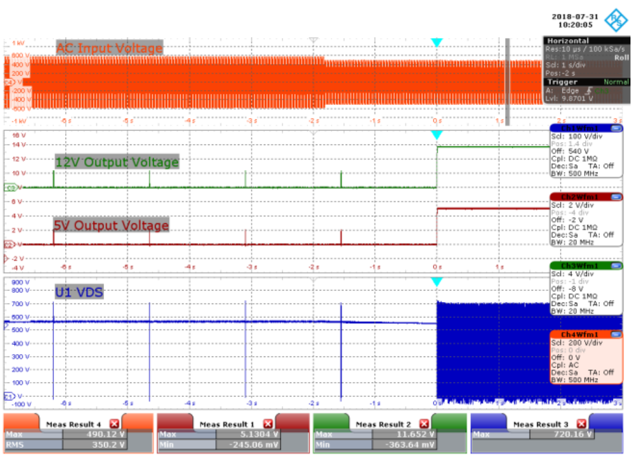

Figure 95 – Output Recovery after Line Overvoltage.
CH1: U1 V_{DS}, 100 V / div., 1 s /div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
CH4: AC_{IN}, 200 V / div., 1 s /div.

10.6 ***Output Ripple Measurements***

10.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

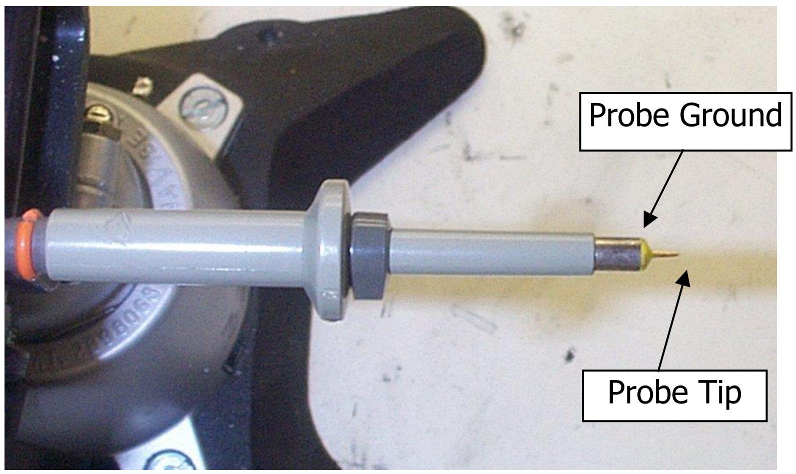

Figure 96 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

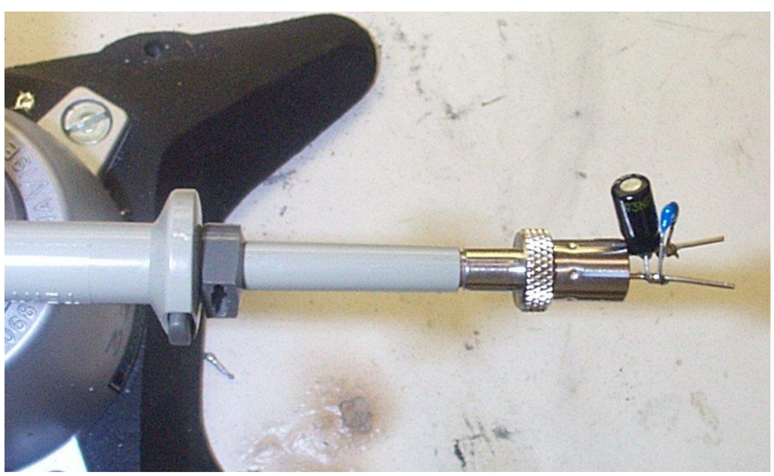

Figure 97 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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10.6.2 Measurement Results

Test Condition: Room Temperature, measured across the PCB connector

10.6.2.1 100% Load Condition

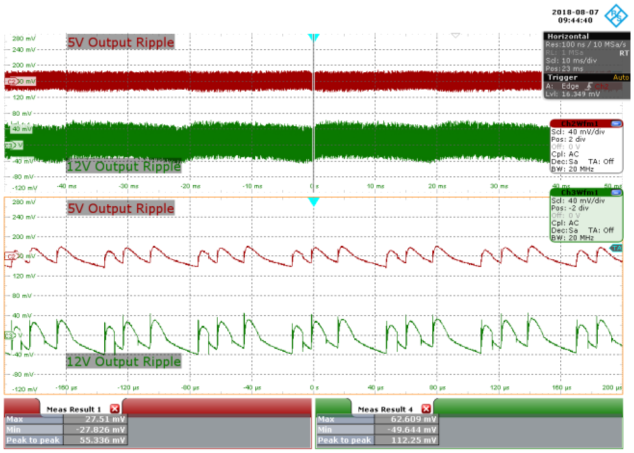

Figure 98 – 85 VAC 60 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 55.536 mV.
12 V Output Ripple = 112.25 mV.

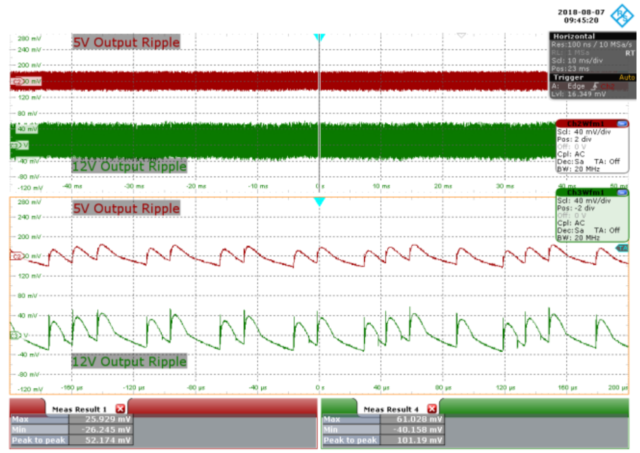

Figure 99 – 115 VAC 60 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 52.174 mV.
12 V Output Ripple = 101.19 mV.

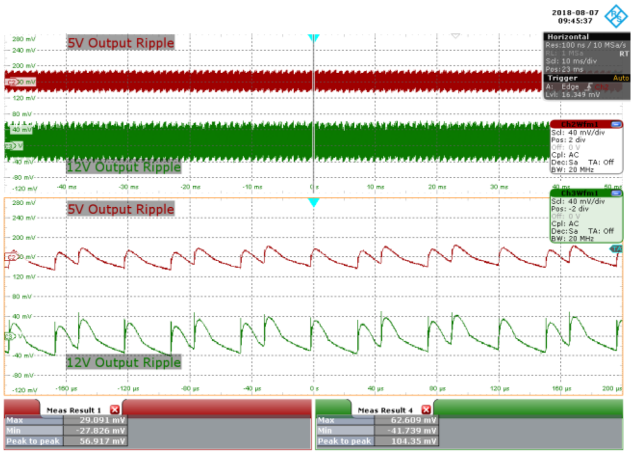

Figure 100 – 230 VAC 50 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 56.917 mV.
12 V Output Ripple = 104.35 mV.

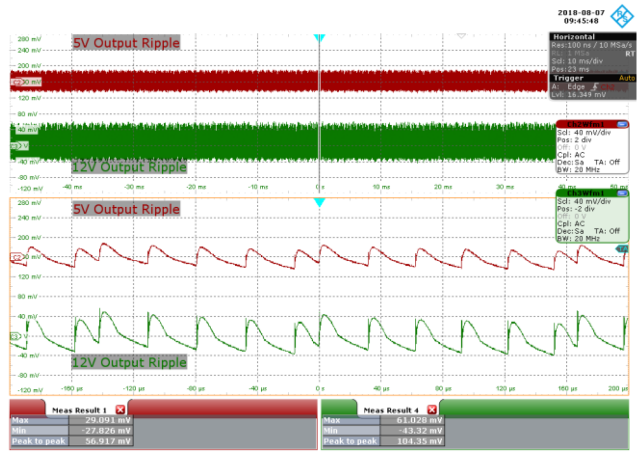

Figure 101 – 350 VAC 50 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 56.917 mV.
12 V Output Ripple = 104.35 mV.

10.6.2.2 75% Load Condition

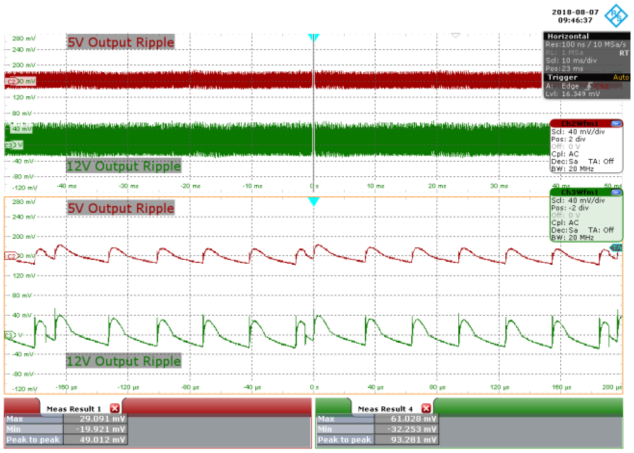

Figure 102 – 85 VAC 60 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 49.012 mV.
12 V Output Ripple = 93.281 mV.

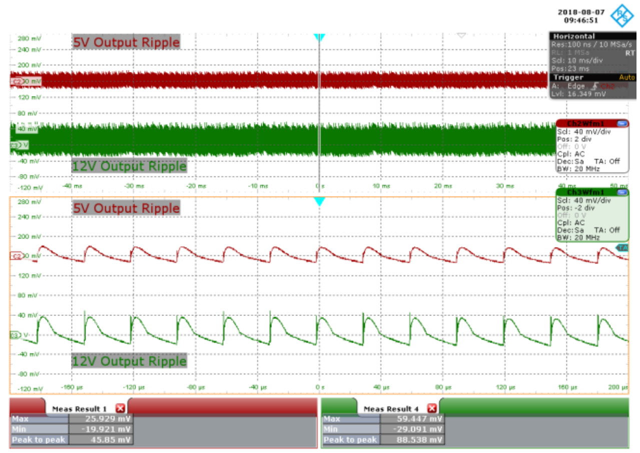

Figure 103 – 115 VAC 60 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 45.85 mV.
12 V Output Ripple = 88.538 mV.

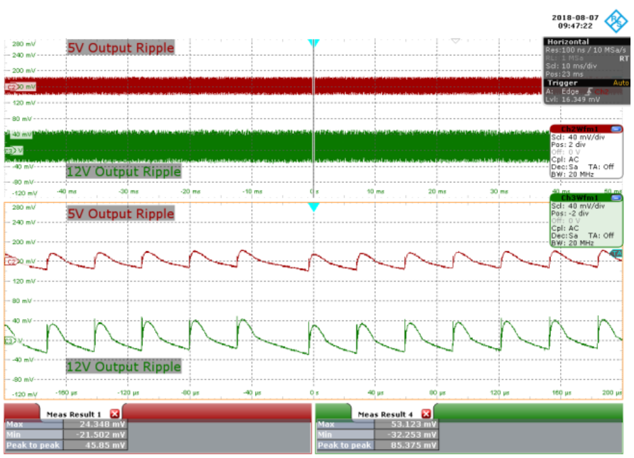

Figure 104 – 230 VAC 50 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 45.85 mV.
12 V Output Ripple = 85.375 mV.

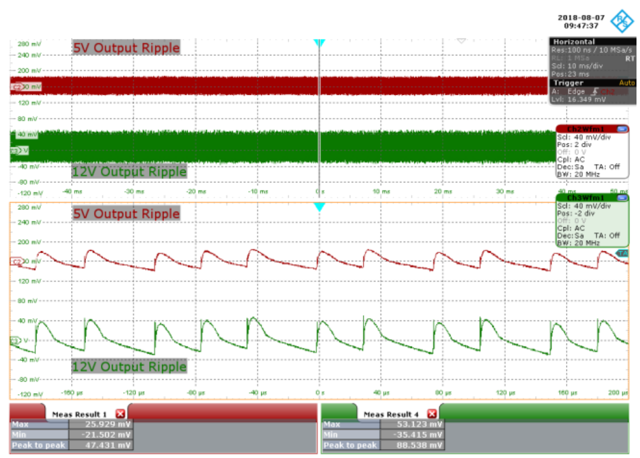

Figure 105 – 350 VAC 50 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 47.431 mV.
12 V Output Ripple = 88.538 mV.

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10.6.2.3 50% Load Condition

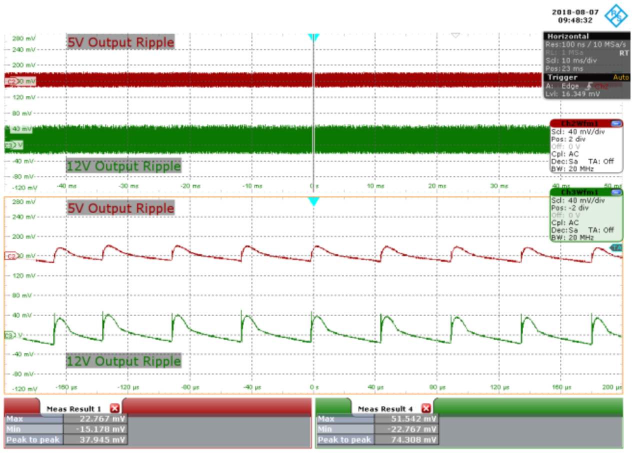

Figure 106 – 85 VAC 60 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 37.945 mV.
12 V Output Ripple = 74.308 mV.

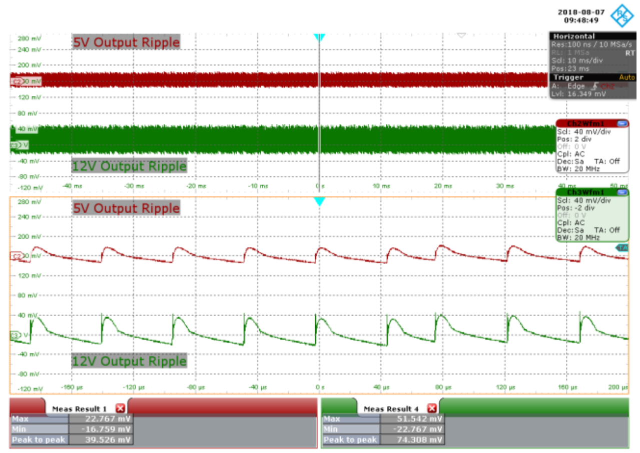

Figure 107 – 115 VAC 60 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 39.526 mV.
12 V Output Ripple = 74.308 mV.

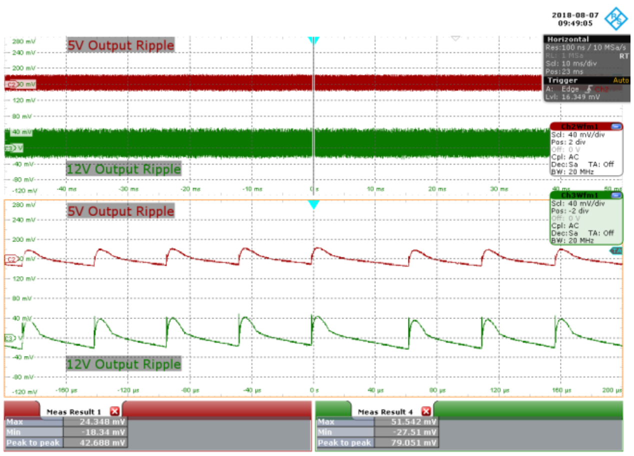

Figure 108 – 230 VAC 50 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 42.688 mV.
12 V Output Ripple = 79.051 mV.

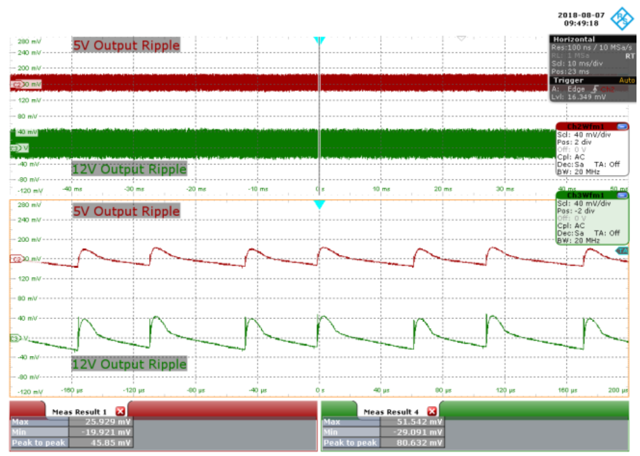

Figure 109 – 350 VAC 50 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 45.85 mV.
12 V Output Ripple = 80.632 mV.

10.6.2.4 25% Load Condition

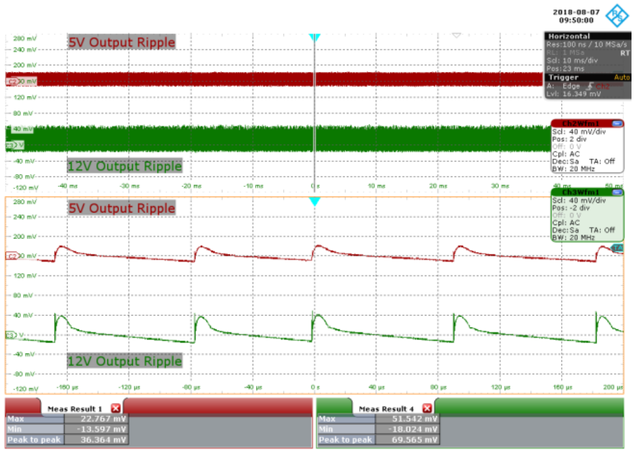

Figure 110 – 85 VAC 60 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 36.364 mV.
12 V Output Ripple = 69.565 mV.

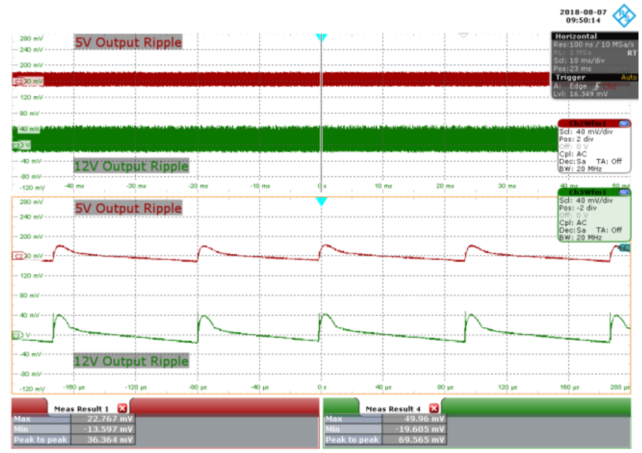

Figure 111 – 115 VAC 60 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 36.354 mV.
12 V Output Ripple = 69.565 mV.

Figure 112 – 230 VAC 50 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 39.526 mV.
12 V Output Ripple = 72.727 mV.

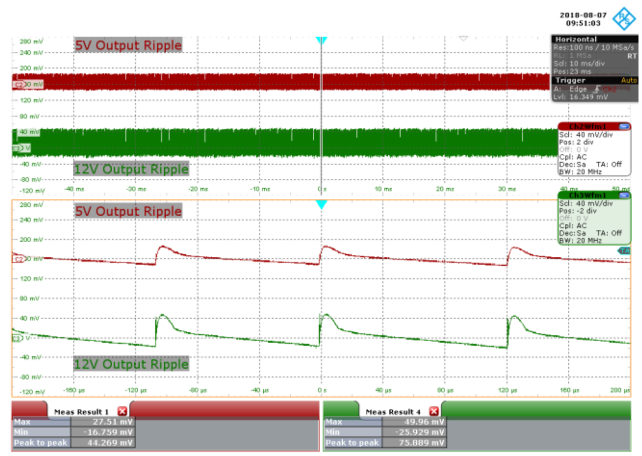

Figure 113 – 350 VAC 50 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 44.269 mV.
12 V Output Ripple = 75.389 mV.

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10.6.2.5 0% Load Condition

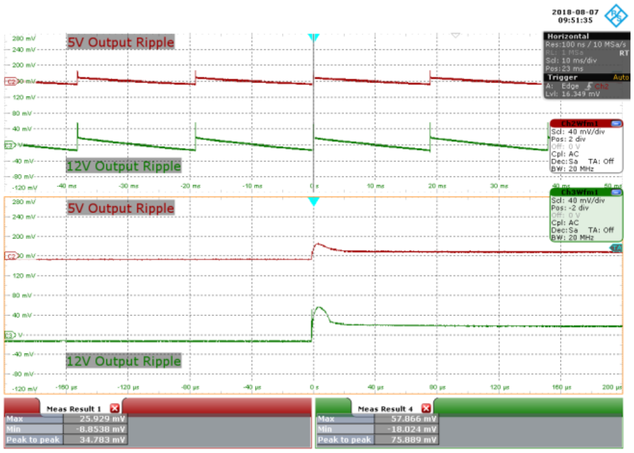

Figure 114 – 85 VAC 60 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 34.783 mV.
12 V Output Ripple = 75.889 mV.

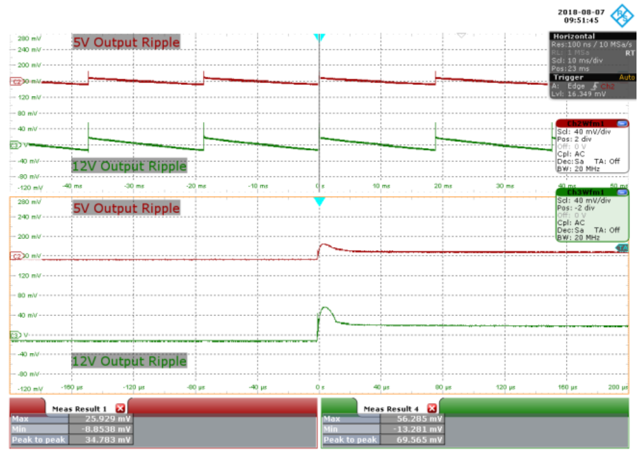

Figure 115 – 115 VAC 60 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 34.783 mV.
12 V Output Ripple = 69.565 mV.

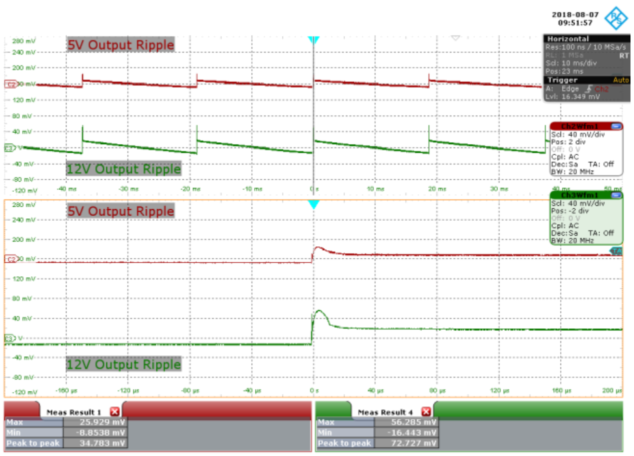

Figure 116 – 230 VAC 50 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 34.783 mV.
12 V Output Ripple = 72.727 mV.

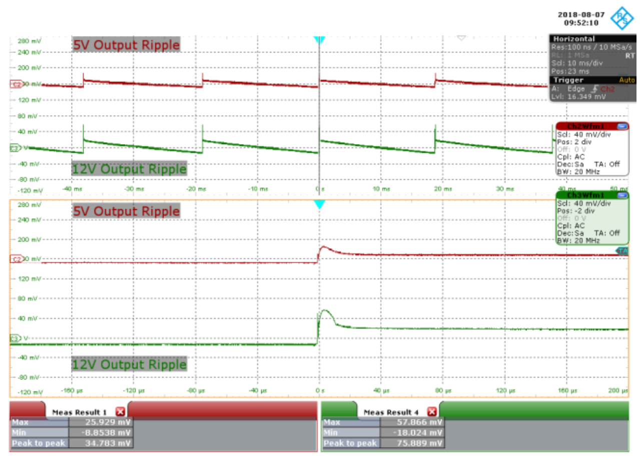

Figure 117 – 350 VAC 50 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 34.783 mV.
12 V Output Ripple = 75.889 mV.

10.6.3 Ripple at Hot and Cold Temperatures

10.6.3.1 85 VAC, 60 Hz

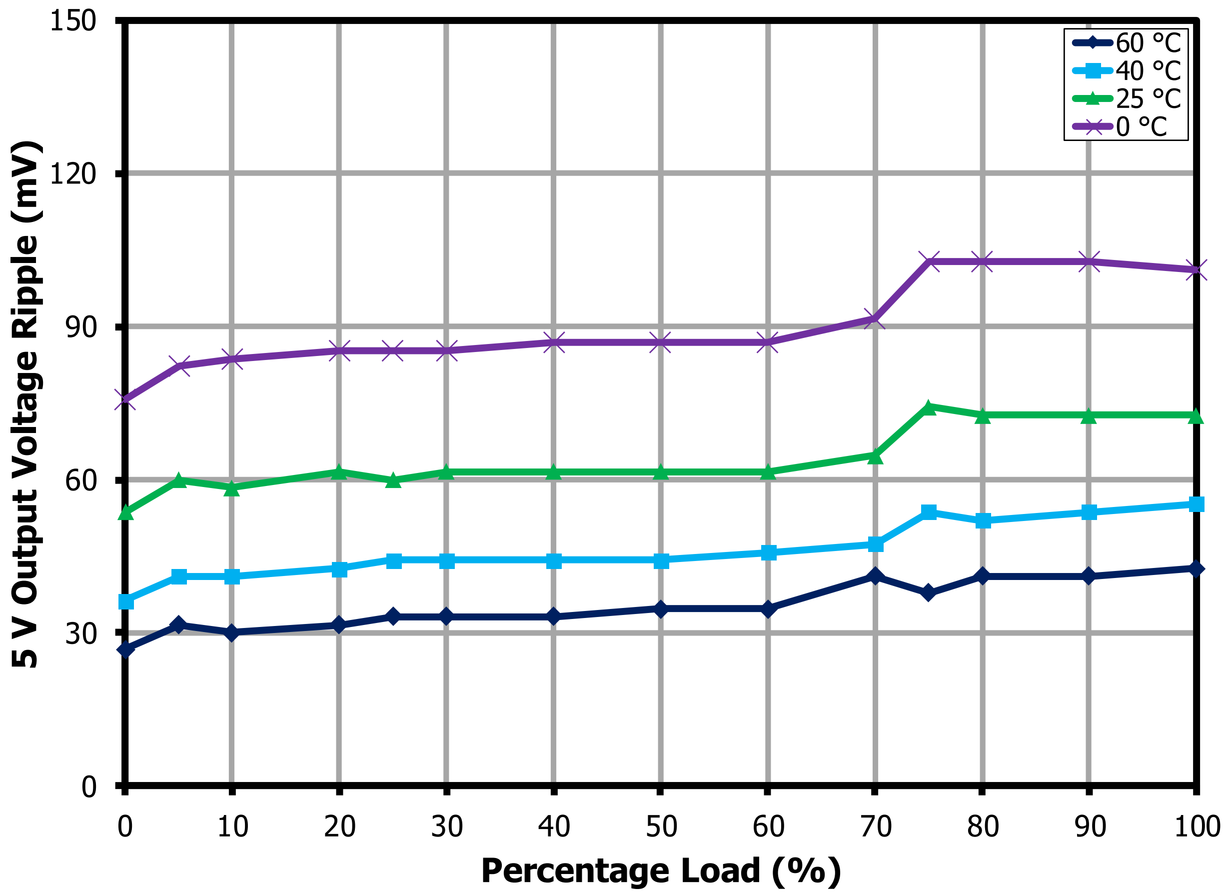

Figure 118 – 5 V Output Ripple at 85 VAC, 60 Hz.

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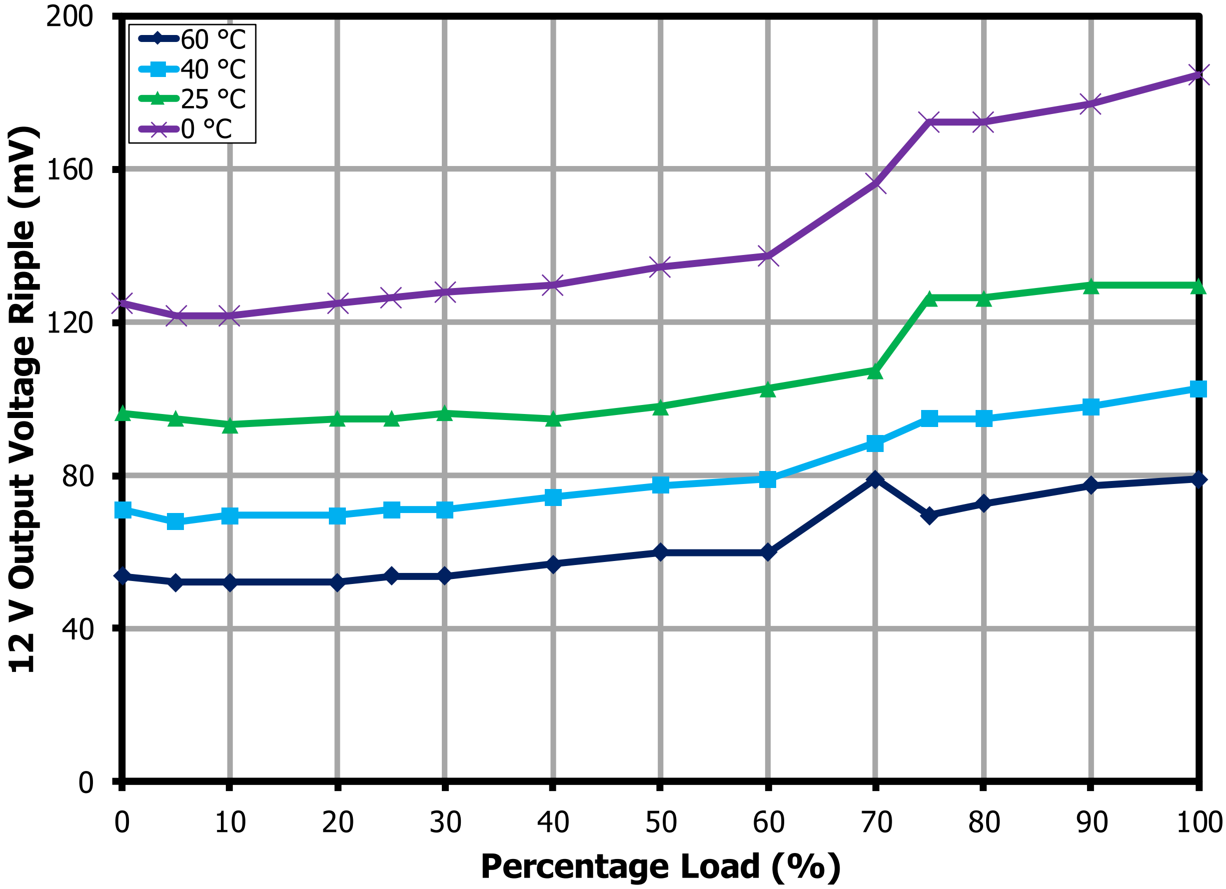

Figure 119 – 12 V Output Ripple at 85 VAC, 60 Hz.

10.6.3.2 115 VAC, 60 Hz

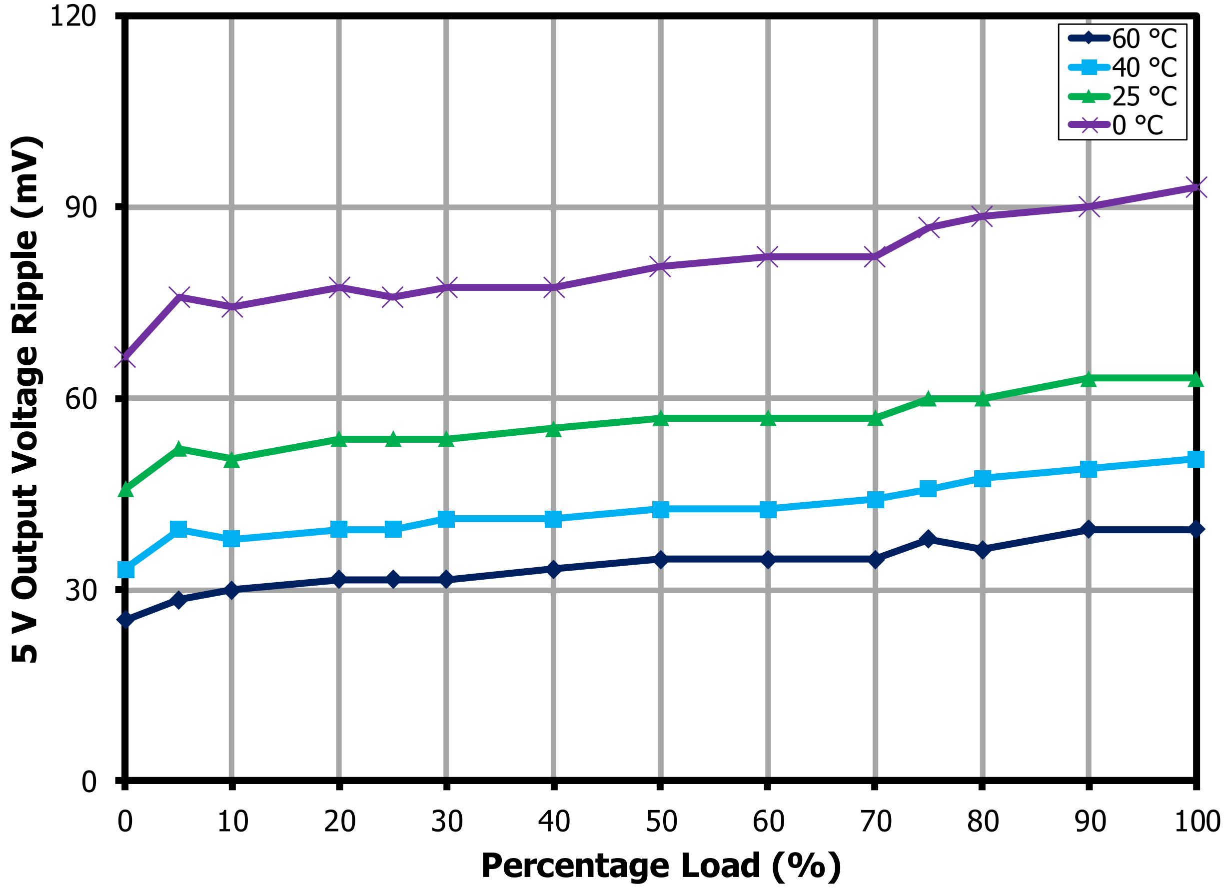

Figure 120 – 5 V Output Ripple at 115 VAC, 60 Hz.

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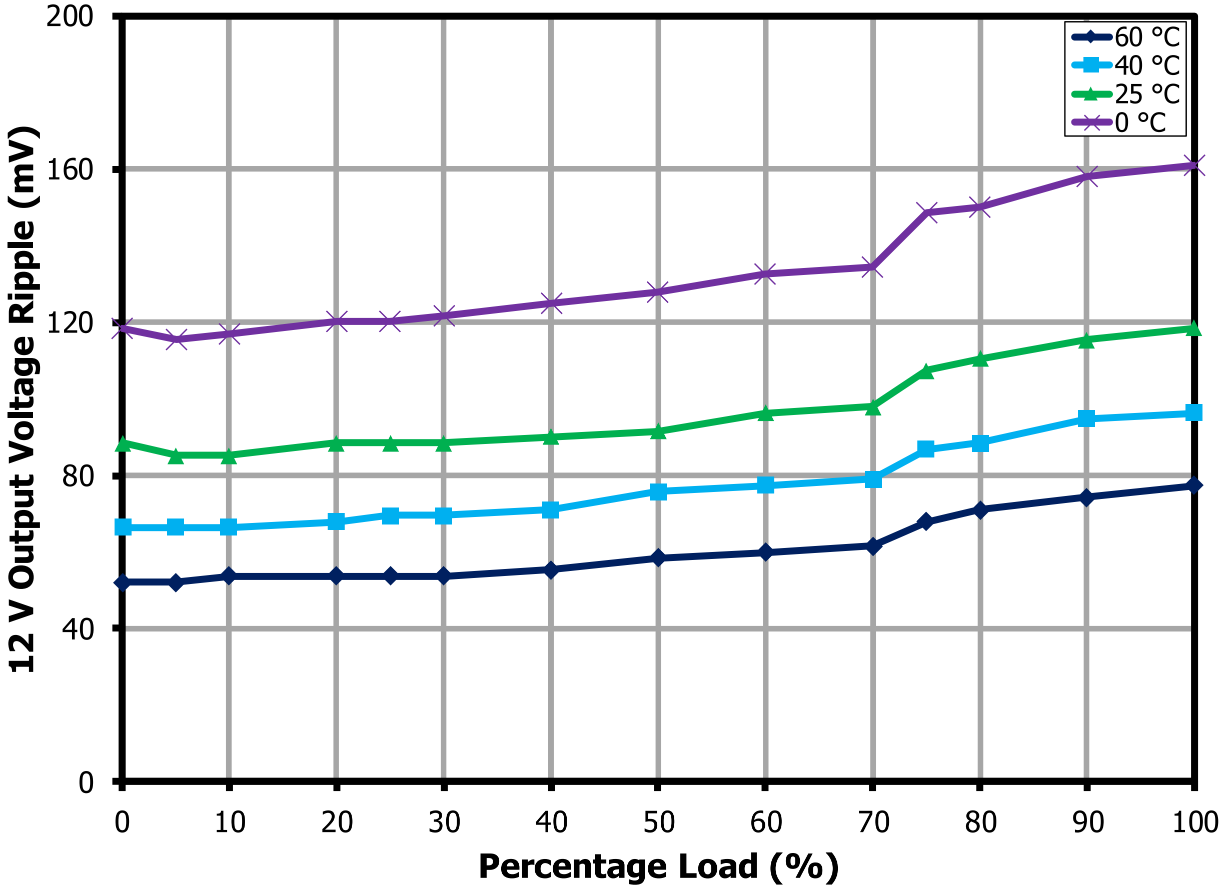

Figure 121 – 12 V Output Ripple at 115 VAC, 60 Hz.

10.6.3.3 230 VAC, 50 Hz

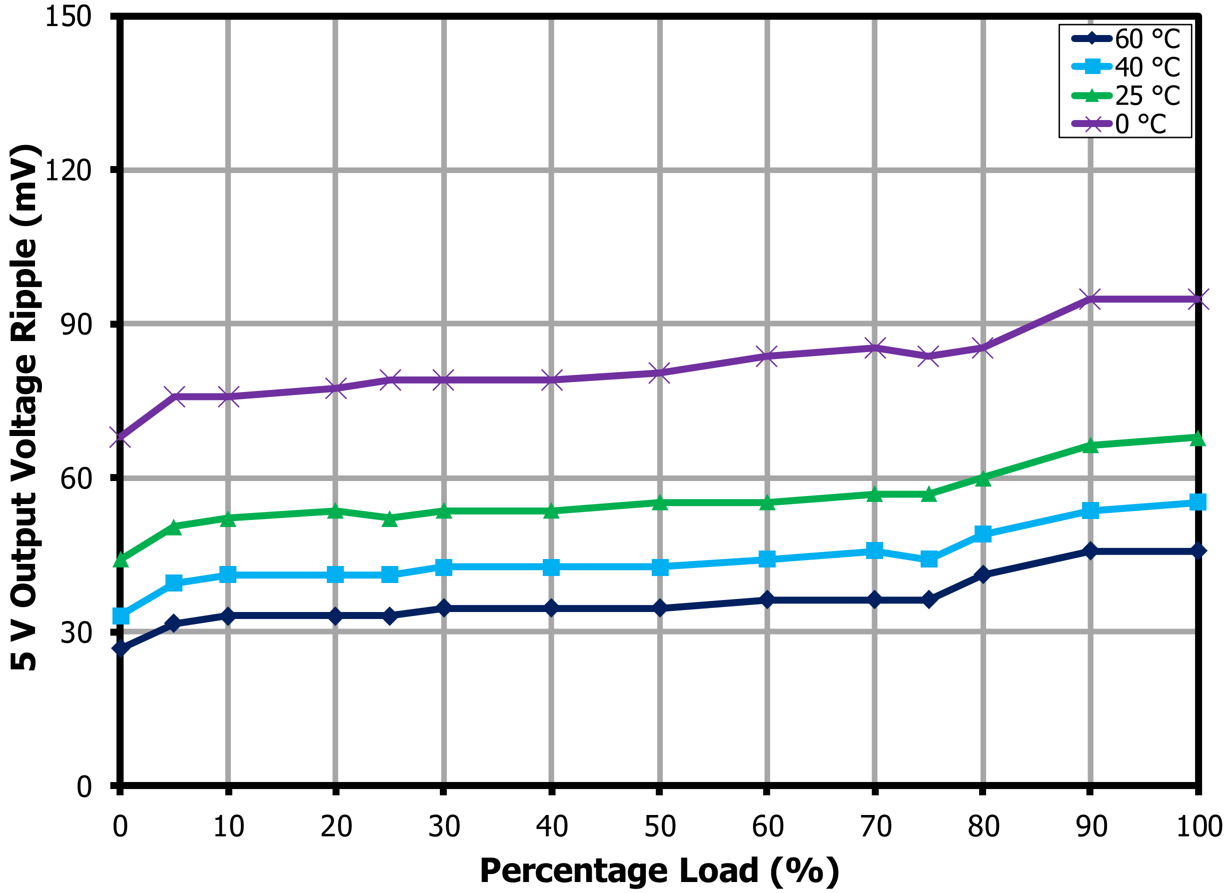

Figure 122 – 5 V Output Ripple at 230 VAC, 50 Hz.

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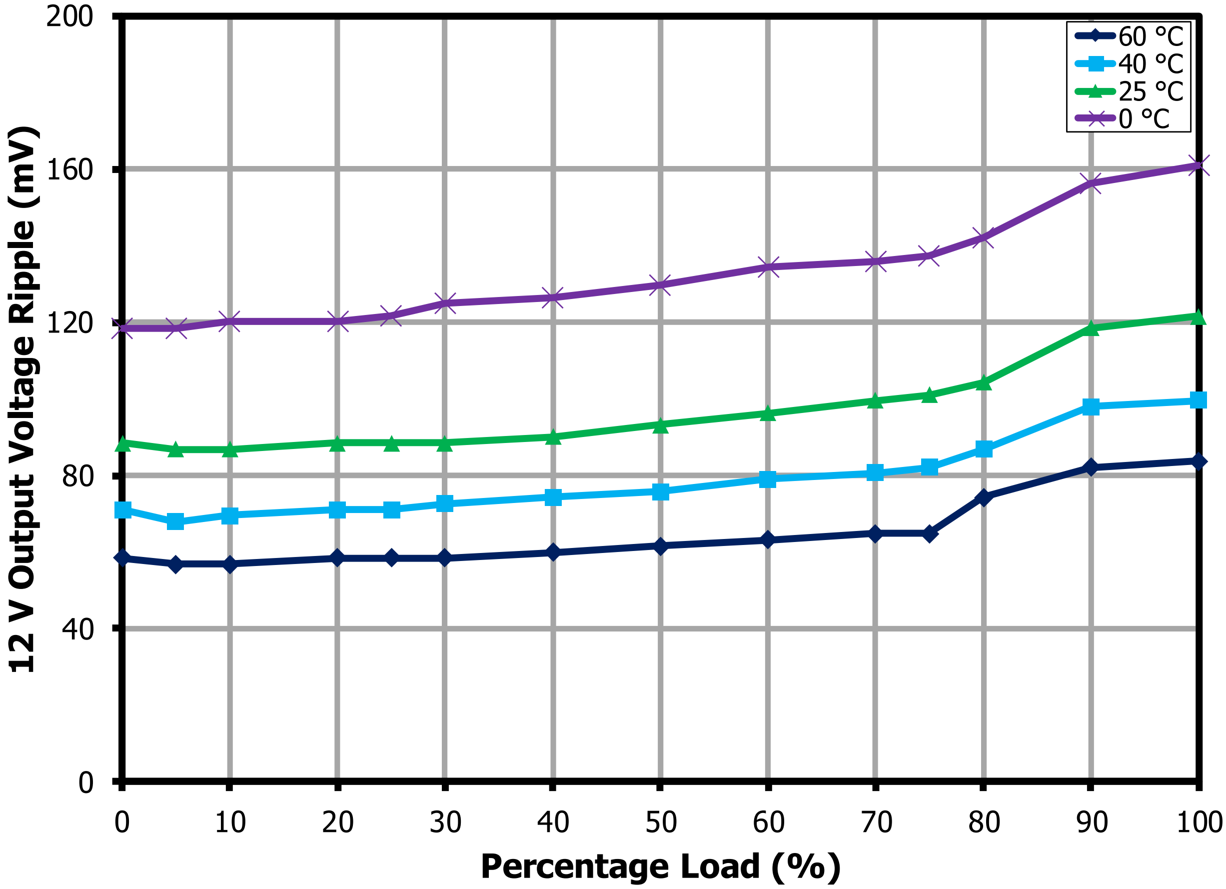

Figure 123 – 12 V Output Ripple at 230 VAC, 50 Hz.

10.6.3.4 350 VAC, 50 Hz

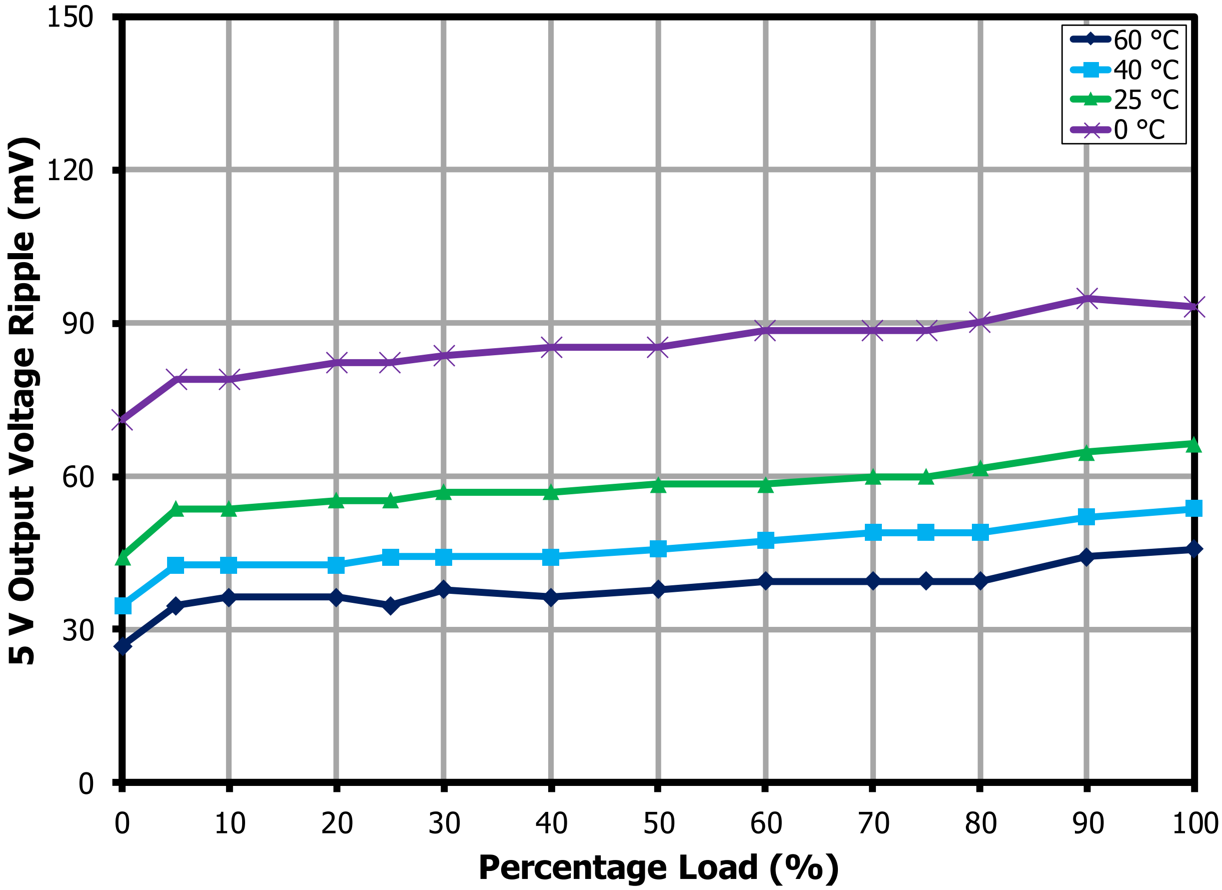

Figure 124 – 5 V Output Ripple at 350 VAC, 50 Hz.

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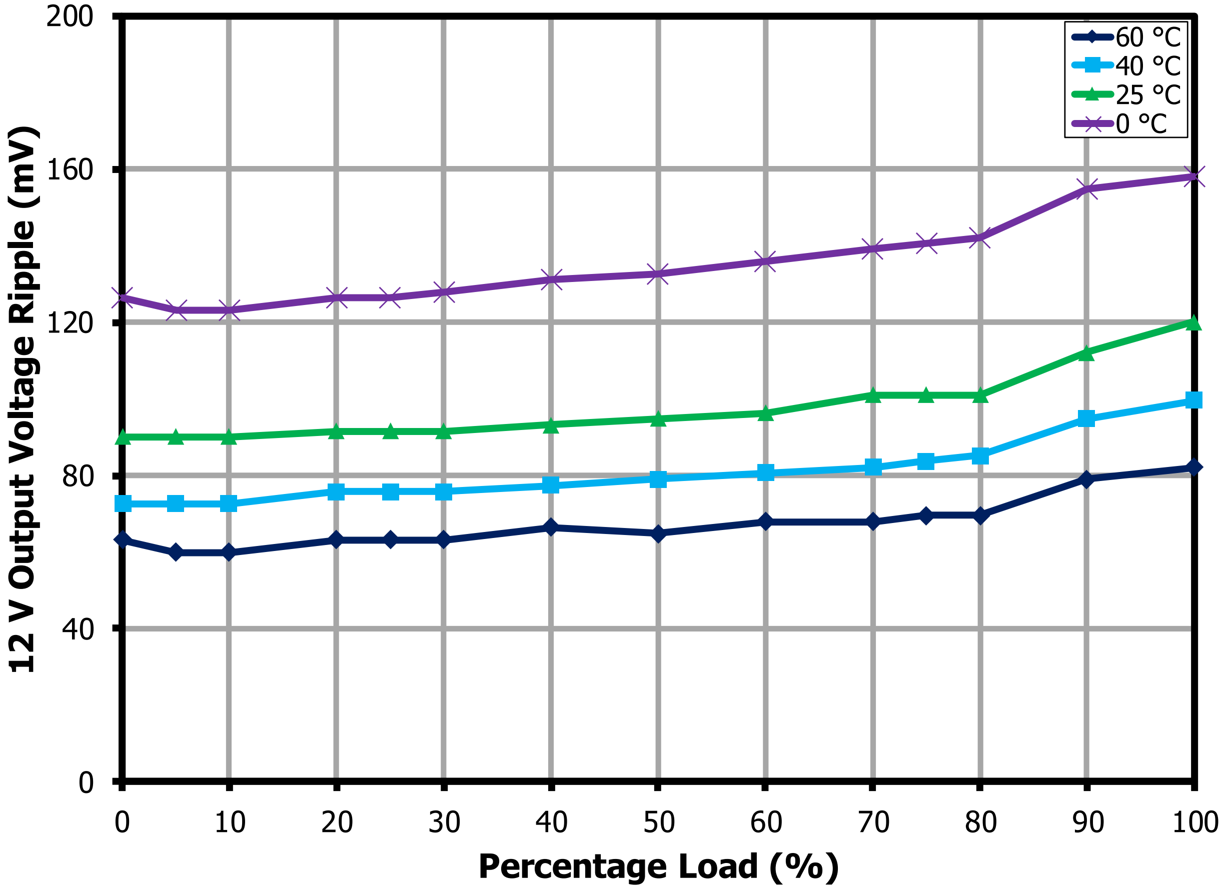

Figure 125 – 12 V Output Ripple at 350 VAC, 50 Hz.

11 Thermal Performance

11.1 *Room Temperature Thermal Scan*

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Temperature was measured using thermal camera. Soak time at full load is 2 hours.

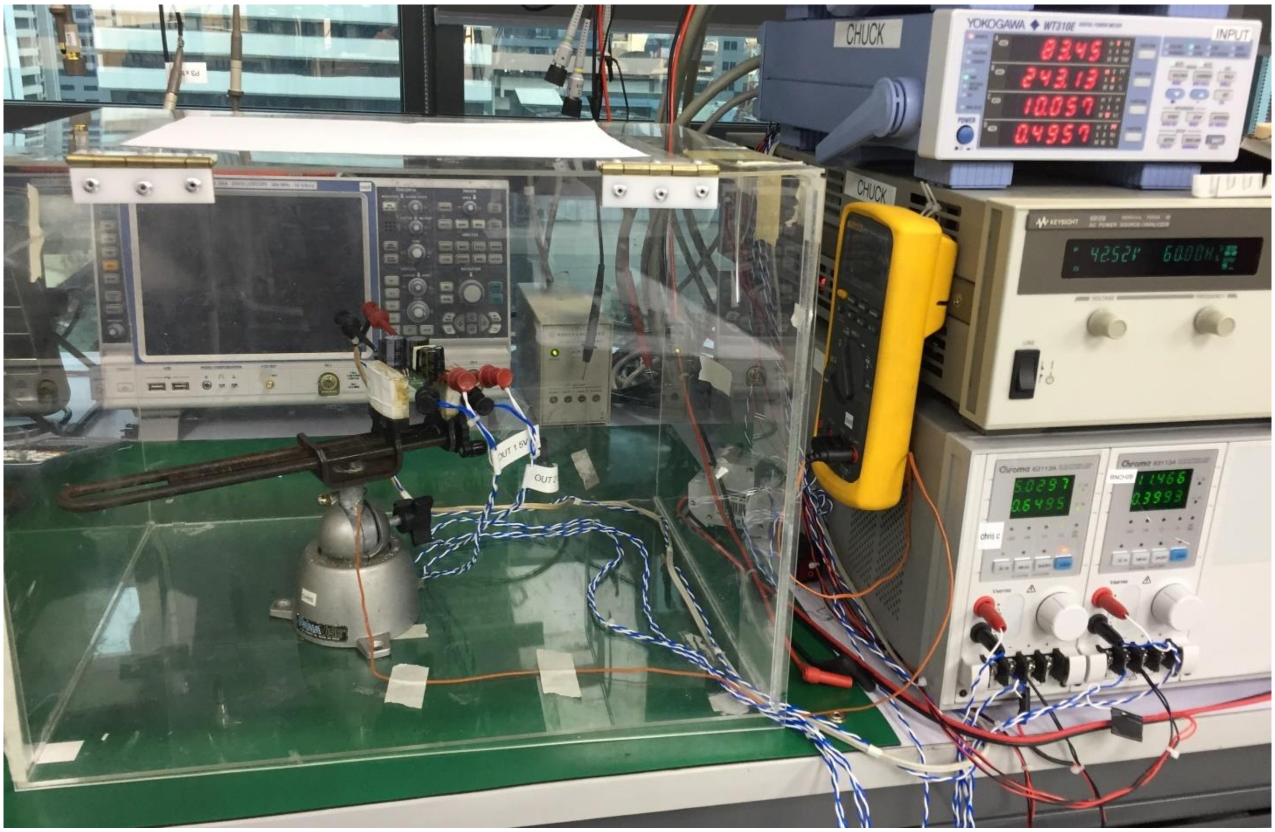

Figure 126 – Thermal Performance Set-up Using an Acrylic Box.

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11.1.1 85 VAC

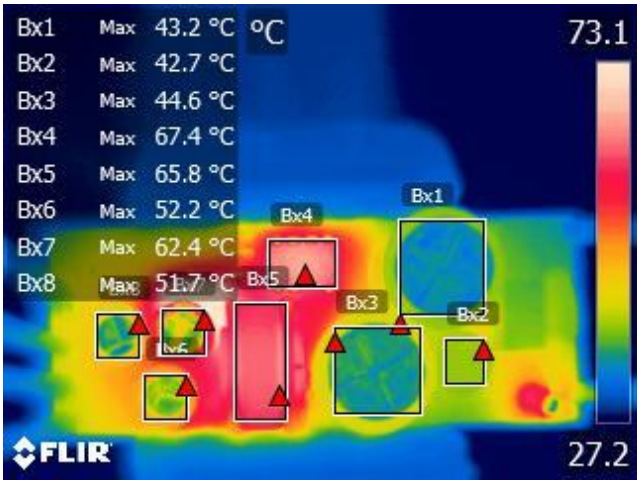

Figure 127 – 85 VAC, Full Load. Top Side.

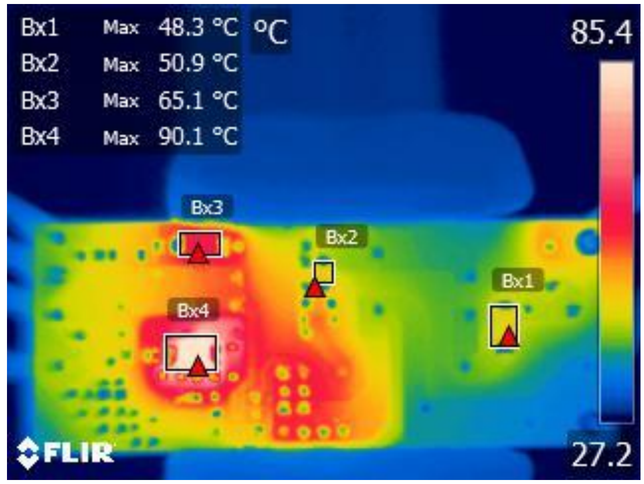

Figure 128 – 85 VAC, Full Load. Bottom Side.

Component	Temperature (°C)
LNK3696P IC (U1)	67.4
Input Rectifier (D1)	48.3
Input Capacitor (C2)	43.2
Input Choke Filter (L1)	42.7
Input Capacitor (C3)	44.6
Transformer (T1)	65.8
Snubber Resistor (R1)	50.9
12 V Output Diode (D2)	65.1
5 V Output Diode (D3)	90.1
12 V Output Capacitor (C4)	52.2
5 V Output Capacitor (C5)	62.4
5 V Output Capacitor (C6)	51.7
Ambient Temperature	25.9

11.1.2 115 VAC

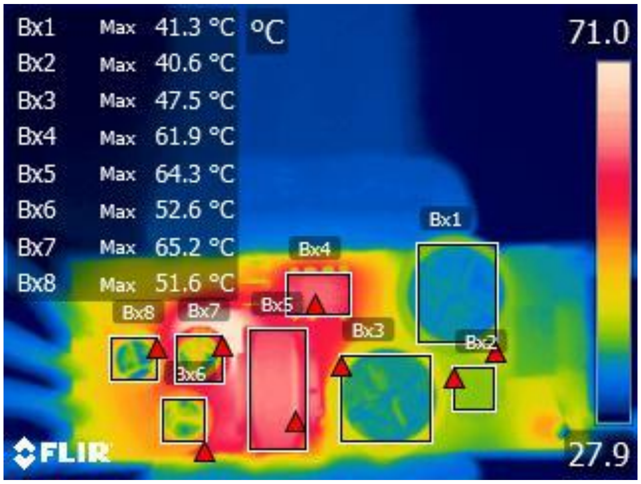

Figure 129 – 115 VAC, Full Load. Top Side.

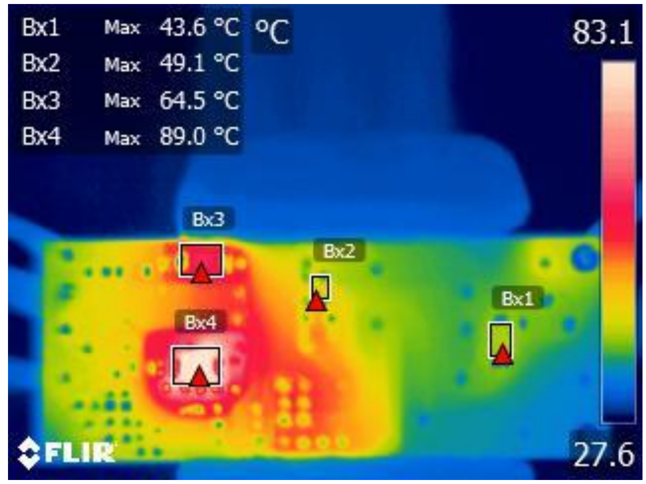

Figure 130 – 115 VAC, Full Load. Bottom Side.

Component	Temperature (ºC)
LNK3696P IC (U1)	61.9
Input Rectifier (D1)	43.6
Input Capacitor (C2)	41.3
Input Choke Filter (L1)	40.6
Input Capacitor (C3)	47.5
Transformer (T1)	64.3
Snubber Resistor (R1)	49.1
12 V Output Diode (D2)	64.5
5 V Output Diode (D3)	89.0
12 V Output Capacitor (C4)	52.6
5 V Output Capacitor (C5)	65.2
5 V Output Capacitor (C6)	51.6
Ambient Temperature	26.0

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11.1.3 230 VAC

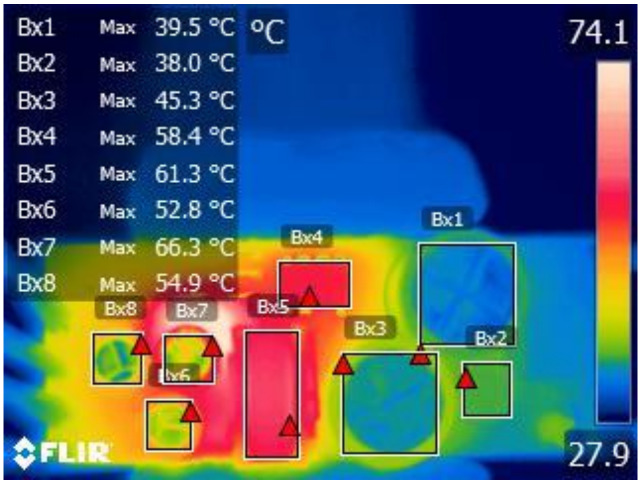

Figure 131 – 230 VAC, Full Load. Top Side.

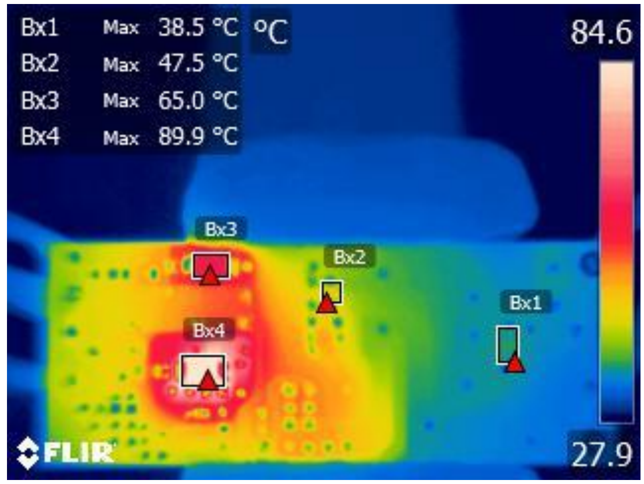

Figure 132 – 230 VAC, Full Load. Bottom Side.

Component	Temperature (ºC)
LNK3696P IC (U1)	58.4
Input Rectifier (D1)	38.5
Input Capacitor (C2)	39.5
Input Choke Filter (L1)	38.0
Input Capacitor (C3)	45.3
Transformer (T1)	61.3
Snubber Resistor (R1)	47.5
12 V Output Diode (D2)	65.0
5 V Output Diode (D3)	89.9
12 V Output Capacitor (C4)	52.8
5 V Output Capacitor (C5)	66.3
5 V Output Capacitor (C6)	54.9
Ambient Temperature	26.1

11.1.4 350 VAC

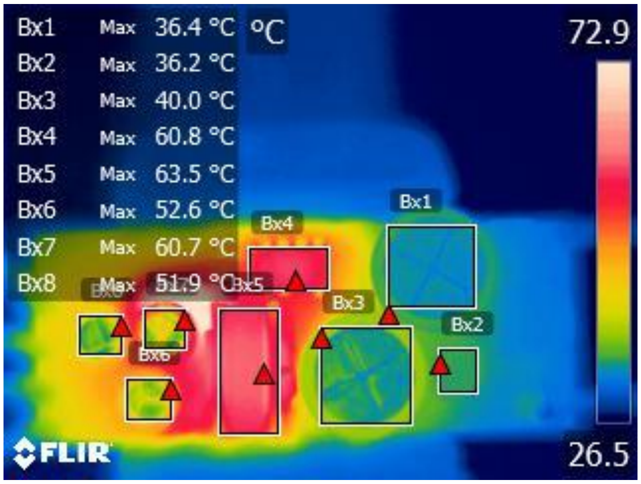

Figure 133 – 350 VAC, Full Load. Top Side.

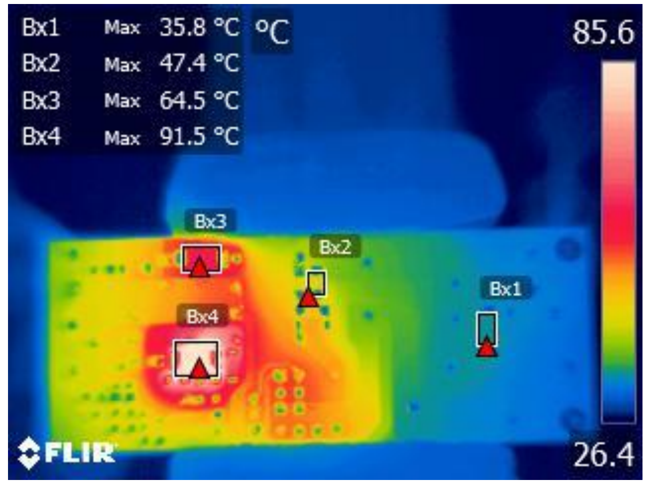

Figure 134 – 350 VAC, Full Load.

Component	Temperature (ºC)
LNK3696P IC (U1)	60.8
Input Rectifier (D1)	35.8
Input Capacitor (C2)	36.4
Input Choke Filter (L1)	36.2
Input Capacitor (C3)	40.0
Transformer (T1)	63.5
Snubber Resistor (R1)	47.4
12 V Output Diode (D2)	64.5
5 V Output Diode (D3)	91.5
12 V Output Capacitor (C4)	52.6
5 V Output Capacitor (C5)	60.7
5 V Output Capacitor (C6)	51.9
Ambient Temperature	26.2

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11.2 *70 °C Ambient Thermal Performance*

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Ambient temperature inside enclosure is 70 ºC. Temperature was measured using type T thermocouple. Soak time at full load is 1 hour.

Figure 135 – Thermal Performance Set-up using Thermal Chamber.

11.2.1 85 VAC

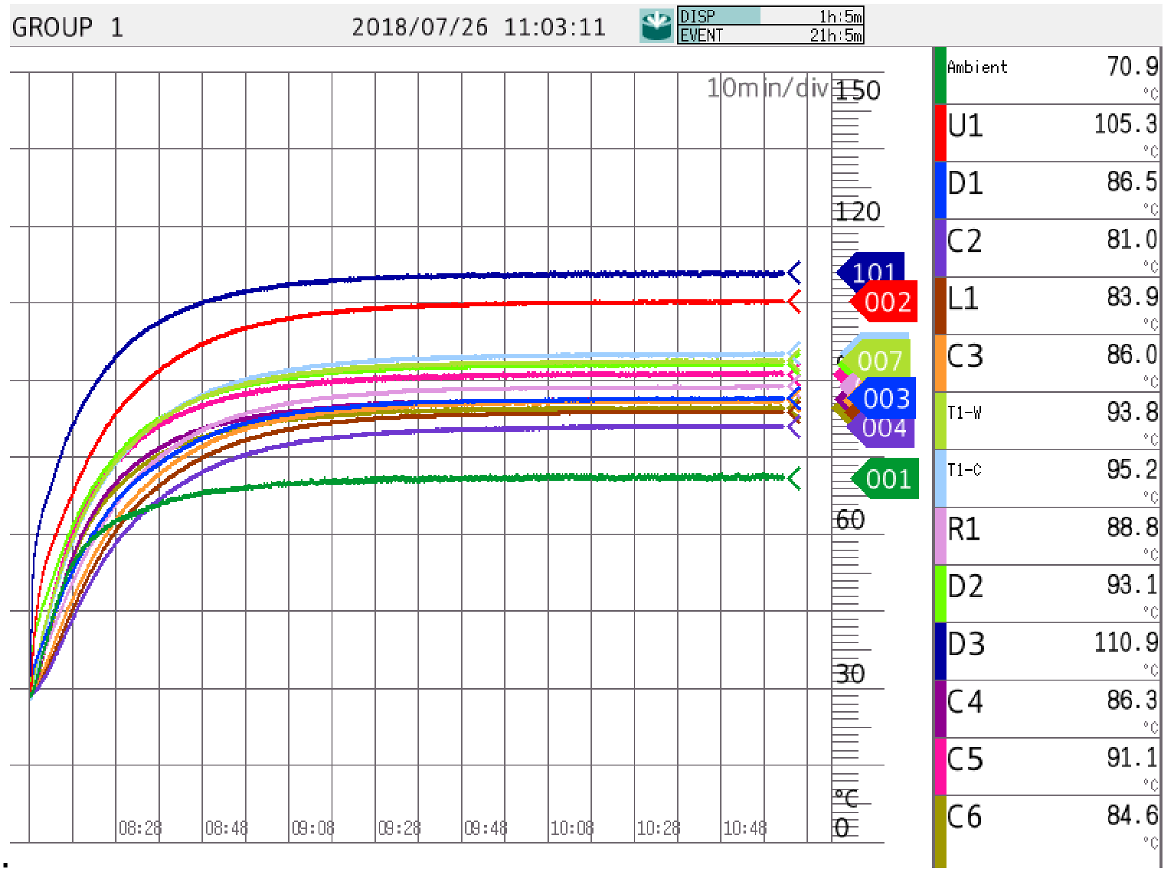

Figure 136 – Thermal Performance at 70 ºC (85 VAC).

Component	Temperature (ºC)
LNK3696P IC (U1)	105.3
Input Rectifier (D1)	86.5
Input Capacitor (C2)	81.0
Input Choke Filter (L1)	83.9
Input Capacitor (C3)	86.0
Transformer-Winding (T1-W)	93.8
Transformer-Core (T1-C)	95.2
Snubber Resistor (R1)	88.9
12 V Output Diode (D2)	93.1
5 V Output Diode (D3)	110.9
12 V Output Capacitor (C4)	86.3
5 V Output Capacitor (C5)	91.1
5 V Output Capacitor (C6)	84.6
Ambient Temperature	70.9

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11.2.2 350 VAC

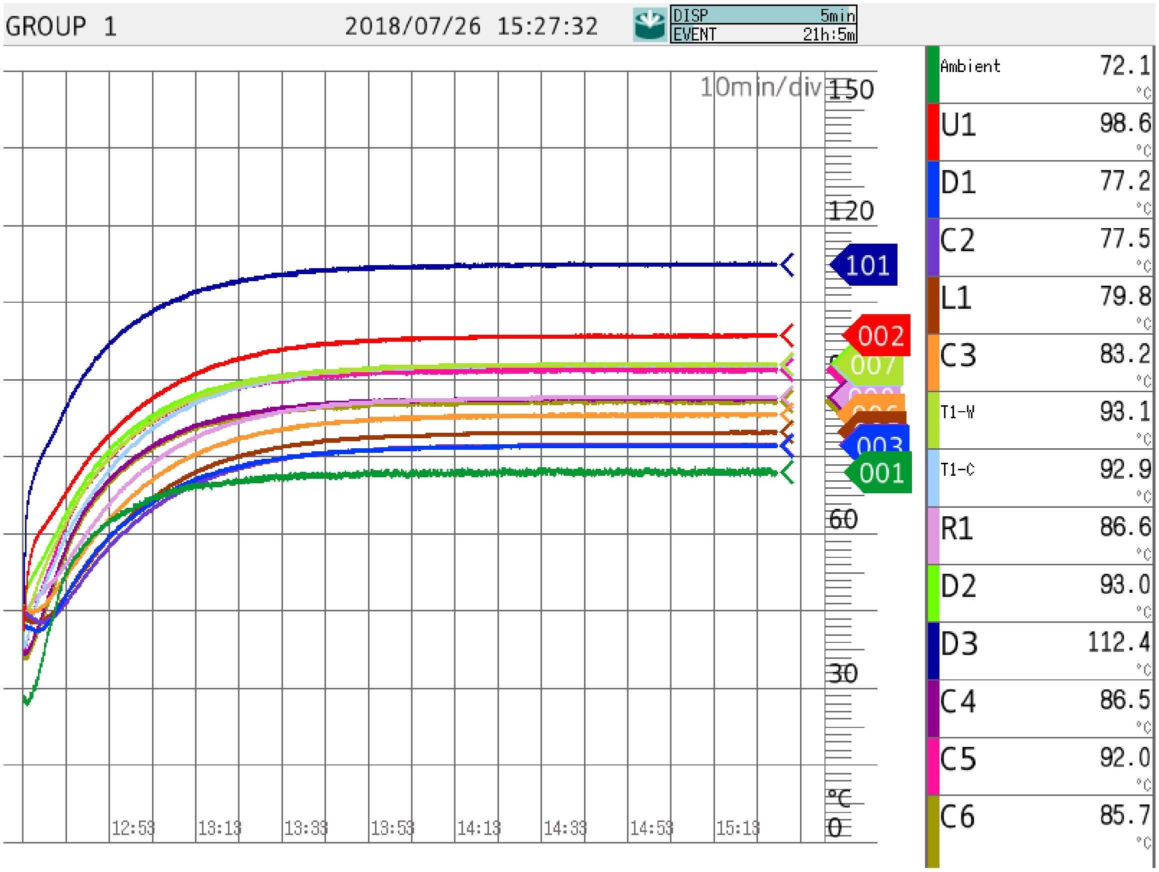

Figure 137 – Thermal Performance at 70 ºC (350 VAC).

Component	Temperature (ºC)
LNK3696P IC (U1)	98.6
Input Rectifier (D1)	77.2
Input Capacitor (C2)	77.5
Input Choke Filter (L1)	79.8
Input Capacitor (C3)	83.2
Transformer-Winding (T1-W)	93.1
Transformer-Core (T1-C)	92.9
Snubber Resistor (R1)	86.6
12 V Output Diode (D2)	93.0
5 V Output Diode (D3)	112.4
12 V Output Capacitor (C4)	86.5
5 V Output Capacitor (C5)	92.0
5 V Output Capacitor (C6)	85.7
Ambient Temperature	72.1

11.3 *Over-Temperature Protection*

11.3.1 85 VAC

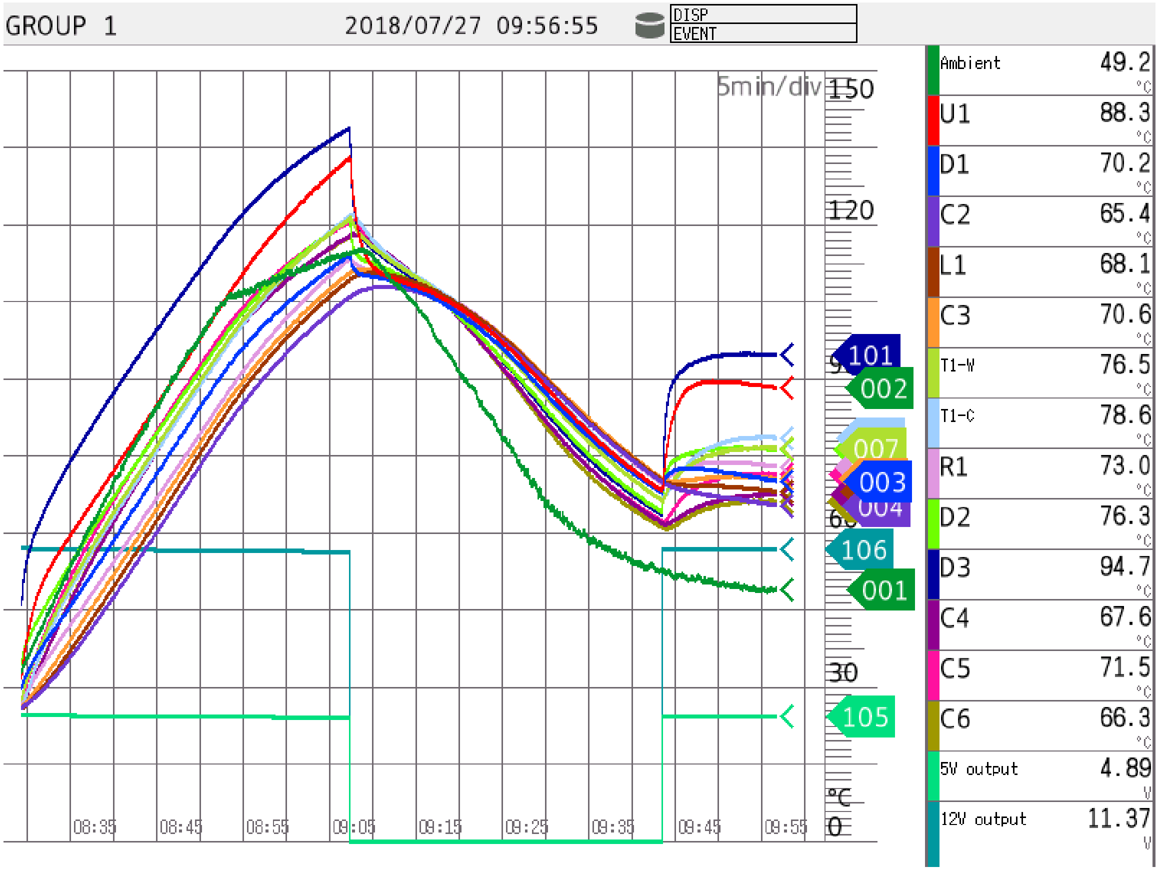

Figure 138 – 85 VAC Over Temperature Protection.

Component	Temperature (ºC) At OTP Trigger	Temperature (ºC) At Recovery
LNK3696P IC (U1)	133.1	68.3
Input Rectifier (D1)	114.1	67.9
Input Capacitor (C2)	106.0	69.9
Input Choke Filter (L1)	109.3	70.3
Input Capacitor (C3)	110.7	70.6
Transformer-Winding (T1-W)	121.2	66.3
Transformer-Core (T1-C)	121.7	67.7
Snubber Resistor (R1)	113.4	69.6
12 V Output Diode (D2)	121.1	64.2
5 V Output Diode (D3)	138.8	63.9
12 V Output Capacitor (C4)	117.9	62.0
5 V Output Capacitor (C5)	120.6	62.3
5 V Output Capacitor (C6)	117.7	61.2
Ambient Temperature	114.6	53.0

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11.3.2 350 VAC

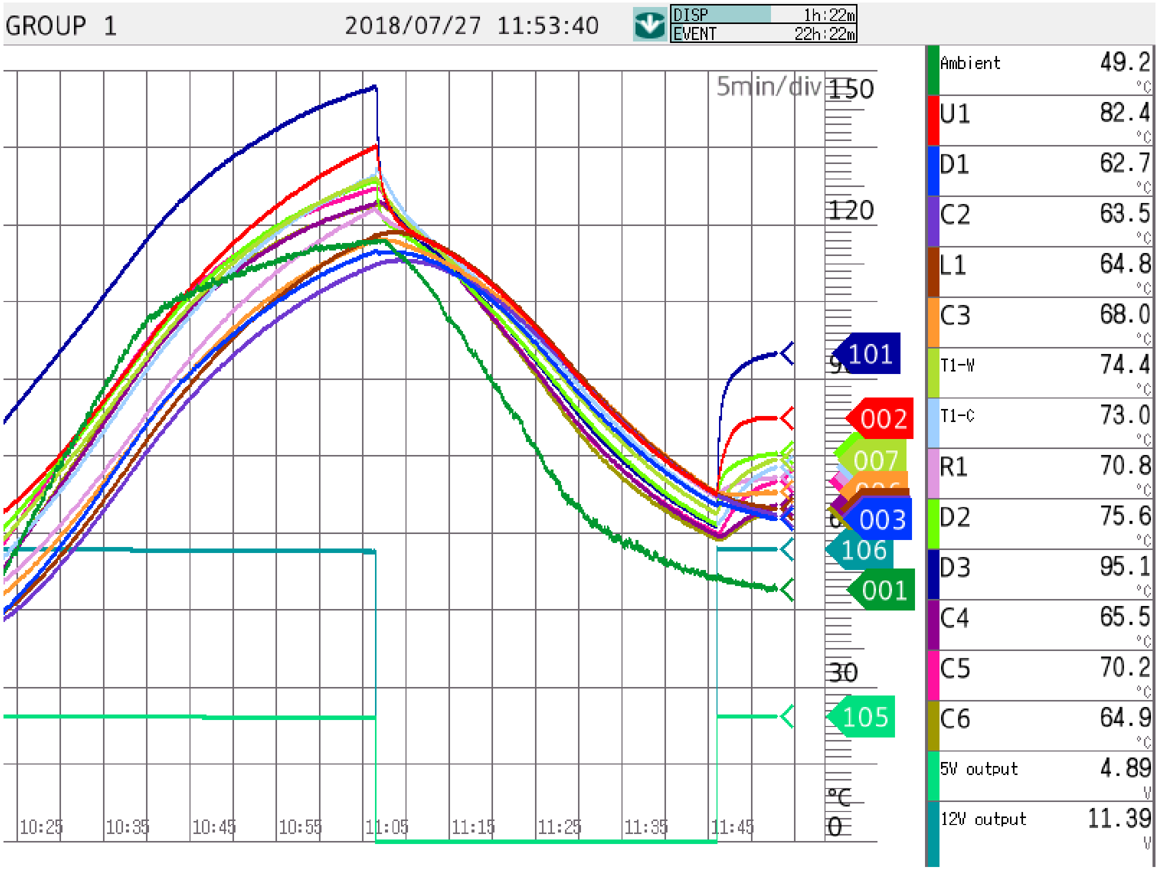

Figure 139 – 350 VAC Over Temperature Protection.

Component	Temperature (ºC) At OTP Trigger	Temperature (ºC) At Recovery
LNK3696P IC (U1)	135.3	67.6
Input Rectifier (D1)	115.0	65.5
Input Capacitor (C2)	112.3	67.4
Input Choke Filter (L1)	118.0	67.7
Input Capacitor (C3)	117.2	68.0
Transformer-Winding (T1-W)	129.2	64.0
Transformer-Core (T1-C)	129.7	63.7
Snubber Resistor (R1)	123.2	67.1
12 V Output Diode (D2)	128.6	61.8
5 V Output Diode (D3)	146.9	61.4
12 V Output Capacitor (C4)	124.2	59.6
5 V Output Capacitor (C5)	127.1	60.1
5 V Output Capacitor (C6)	124.0	59.0
Ambient Temperature	116.8	51.1

12 Conducted EMI

12.1 *Test Set-up*

Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. Full Load with input voltage set at 230 VAC and 115 VAC.

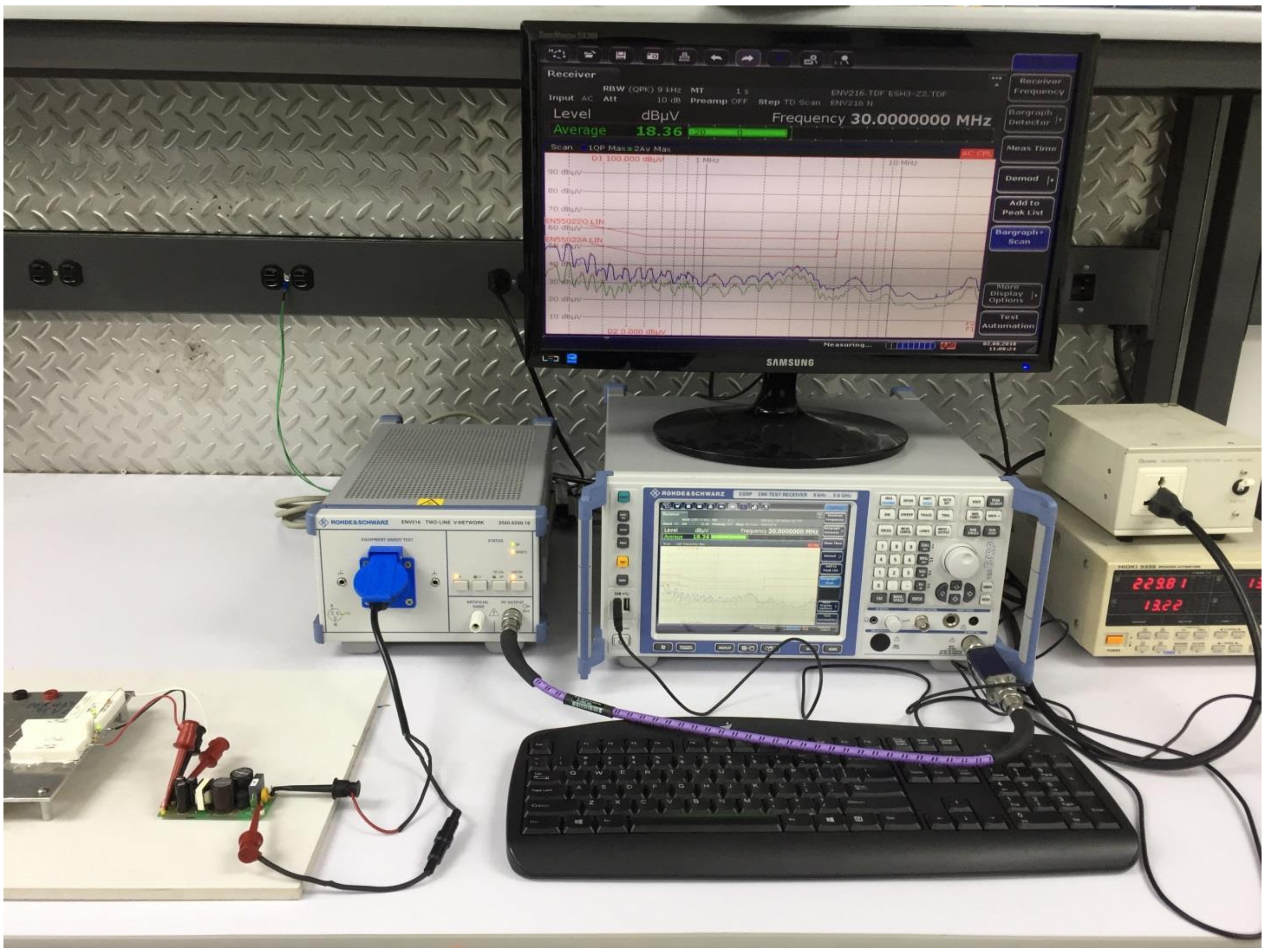

Figure 140 – Conducted EMI Test Set-up.

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12.2 ***8 W Resistive Load, Floating Output***

12.2.1 115 VAC, Line

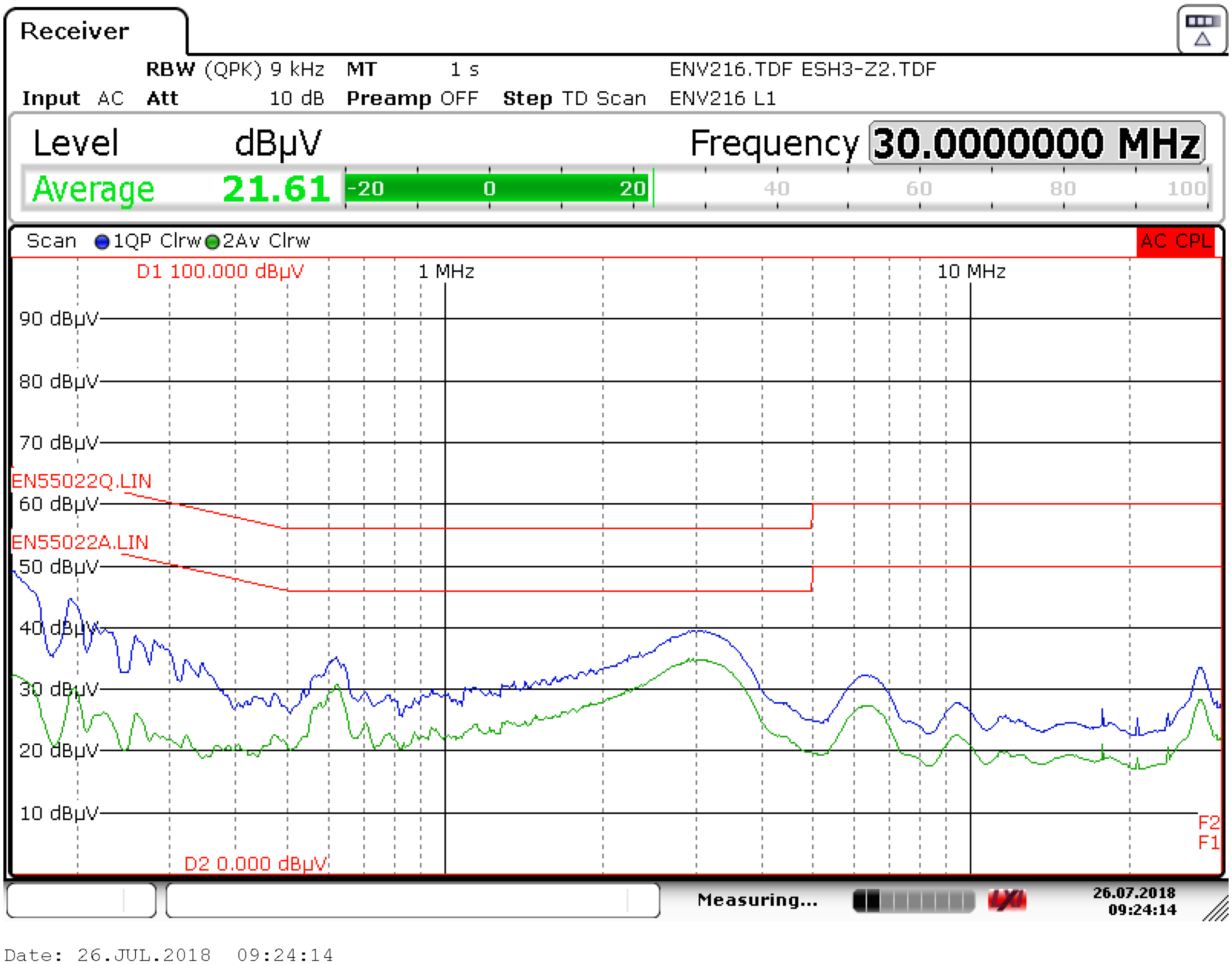
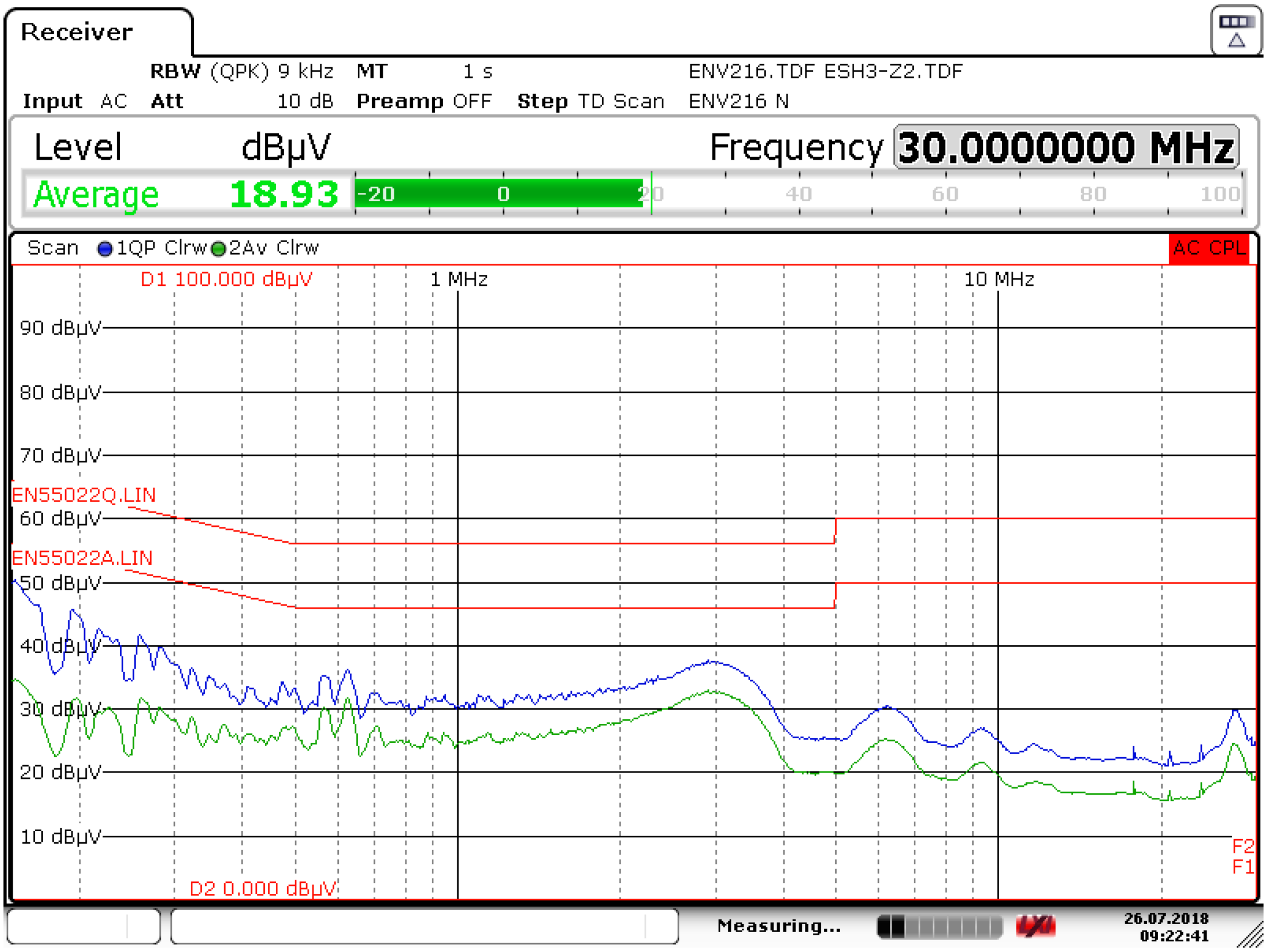


Figure 141 – Floating Ground EMI at 115 VAC, Line.

12.2.2 115 VAC, Neutral



Date: 26.JUL.2018 09:22:41

Figure 142 – Floating Ground EMI at 115 VAC, Neutral.

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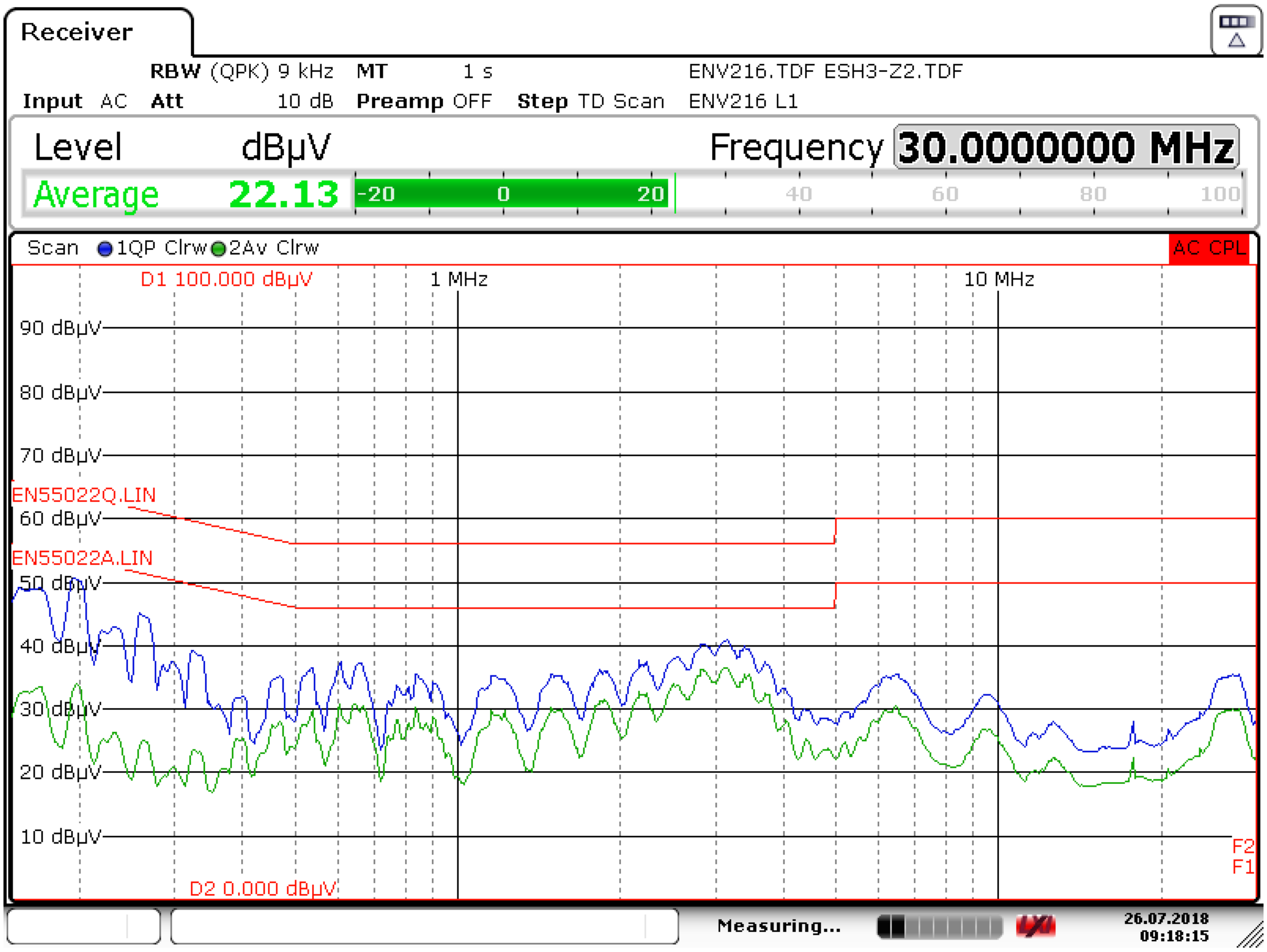
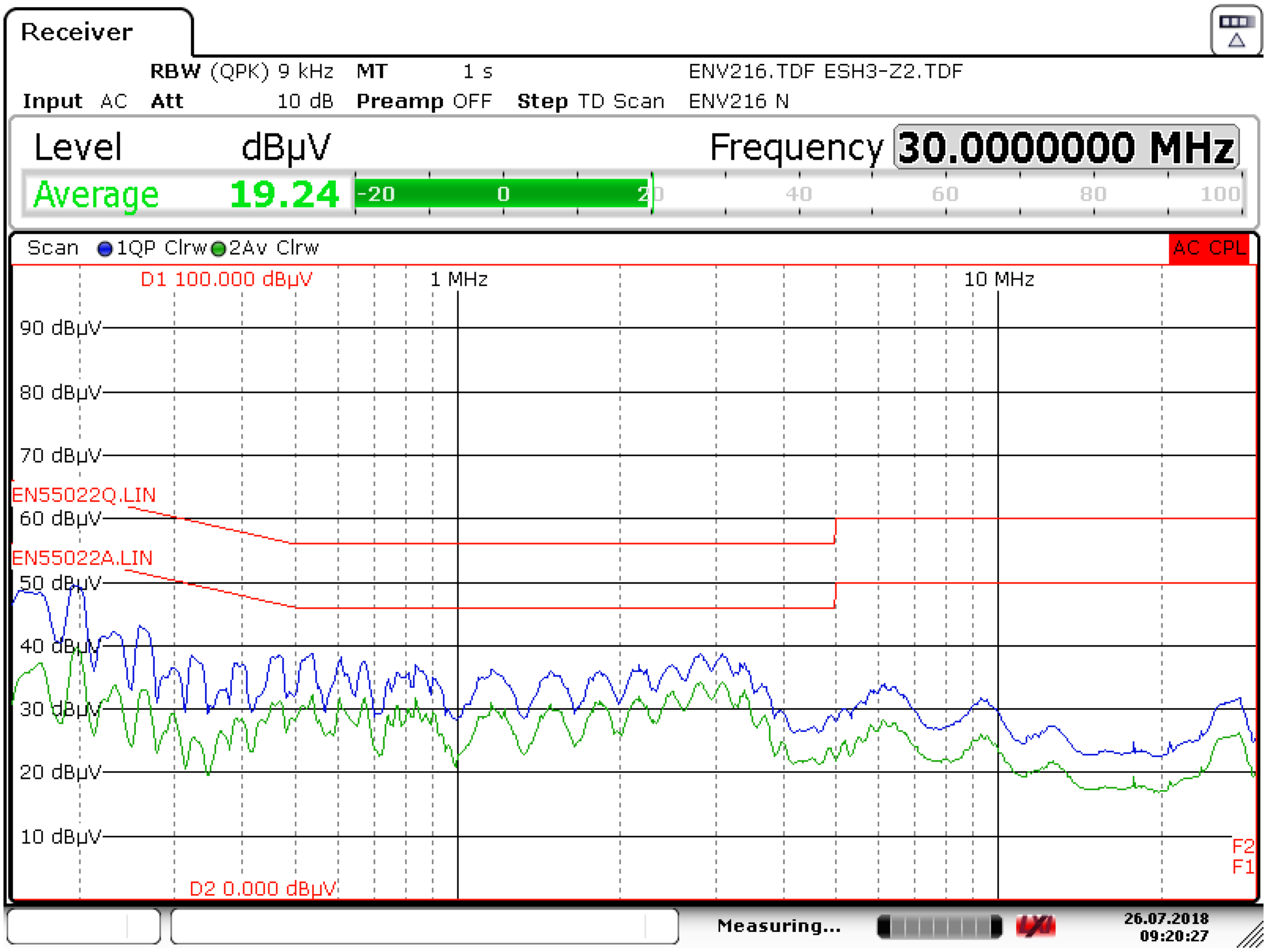
12.2.3 230 VAC, Line



Date: 26.JUL.2018 09:18:15

Figure 143 – Floating Ground EMI at 230 VAC, Line.

12.2.4 230 VAC, Neutral



Date: 26.JUL.2018 09:20:27

Figure 144 – Floating Ground EMI at 230 VAC, Neutral.

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13 Line Surge

The unit was subjected to ±2000 V, 100 kHz ring wave, and ±1000 V differential surge test using 10 strikes at each condition. A test failure is define as a non-recoverable interruption of output requiring repair or recycling of input voltage.

13.1 *Differential Surge Test*

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Result
+1	0	L1 / L2	2	10	PASS
-1	0	L1 / L2	2	10	PASS
+1	90	L1 / L2	2	10	PASS
-1	90	L1 / L2	2	10	PASS
+1	180	L1 / L2	2	10	PASS
-1	180	L1 / L2	2	10	PASS
+1	270	L1 / L2	2	10	PASS
-1	270	L1 / L2	2	10	PASS

Note: In all PASS results, no damage and no auto-restart was observed.

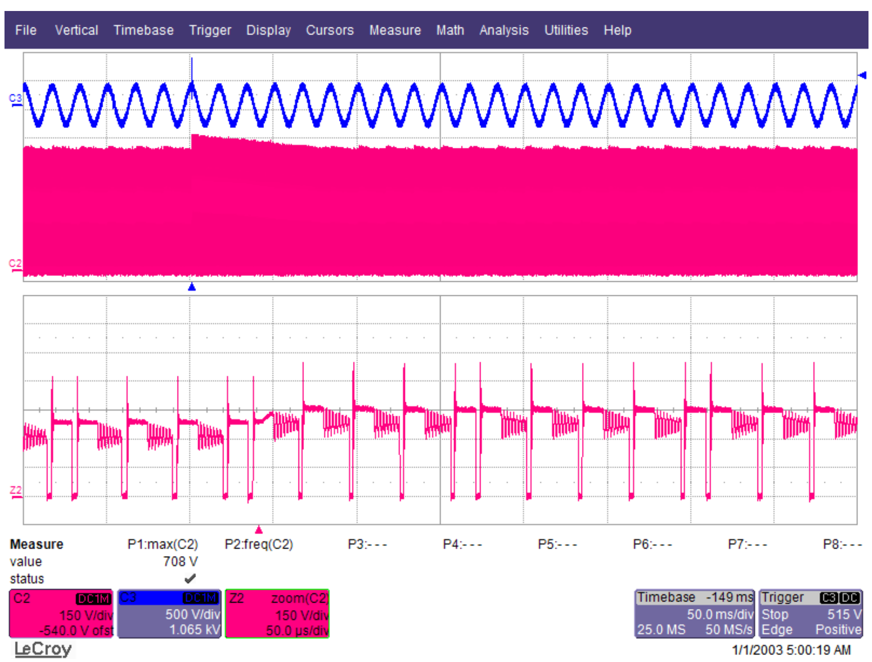

Figure 145 – Input AC Voltage vs. U1 MOSFET V_{DS} during 1 kV Differential Surge.

13.2 *Ring Wave Test*

Ring Wave Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Result
+2	0	L1/L2	12Ω	10	PASS
-2	0	L1/L2	12Ω	10	PASS
+2	90	L1/L2	12Ω	10	PASS
-2	90	L1/L2	12Ω	10	PASS
+2	180	L1/L2	12Ω	10	PASS
-2	180	L1/L2	12Ω	10	PASS
+2	270	L1/L2	12Ω	10	PASS
-2	270	L1/L2	12Ω	10	PASS

Note: In all PASS results, no damage and no auto restart were observed.

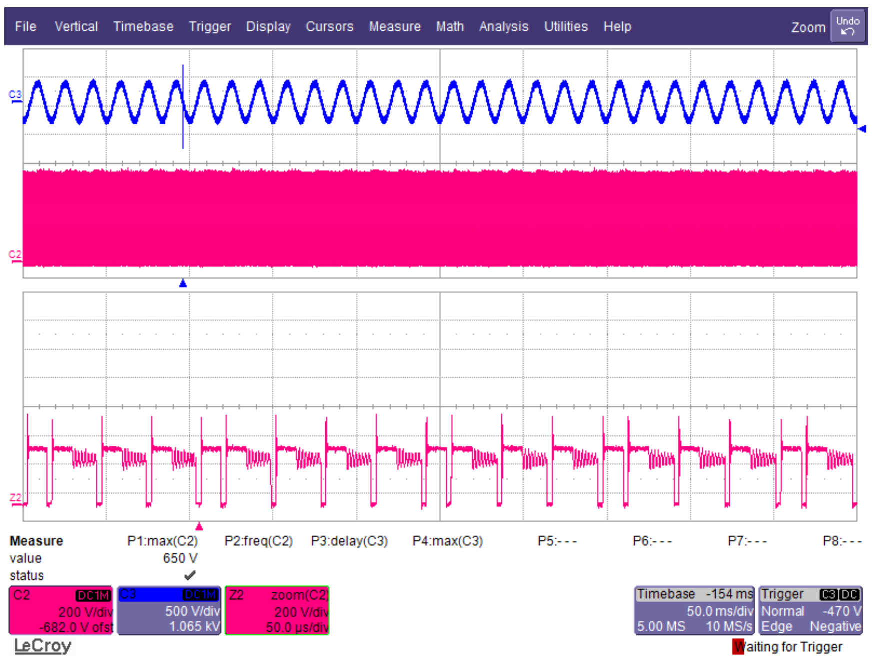

Figure 146 – Input AC Voltage vs. U1 MOSFET V_{DS} during 2 kV Ring Wave Surge.

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14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
13-Sep-18	CE	1.0	Initial Release	Apps & Mktg

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