Design Example Report

Title	***15 W Isolated Flyback Power Supply Using LinkSwitch™-HP LNK6774V***
Specification	90 VAC – 265 VAC Input; 12 V, 1.25 A Output
Application	Small Appliances, Adapter
Author	Applications Engineering Department
Document Number	DER-882
ate	December 15, 2020
Revision	1.1

Summary and Features

- Primary-side regulated isolated flyback converter with ±5% regulation.
- 132 kHz switching frequency for small transformer and output filter size
- Full load continuous conduction mode operation for improved efficiency and reduced output capacitor ripple current
- <30 mW no-load input power at 230 VAC
- Multimode operation maximizes efficiency over full load range
- Extensive protection features including OVP, OTP, brown-in/out, line overvoltage, and lost-regulation (auto-restart)
- Input voltage monitor with accurate brown-in/brown-out protection
- Meets EN550022 and CISPR-22 Class B conducted EMI with 6 dB margin
- Meets IEC61000-4-5, 1 kV
- Meets IEC 61000-4-2 ESD withstand (contact discharger to ±8 kV and air discharge to ±15 kV Class A)

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a universal input, 12 V, 15 W, isolated flyback using LNK6774V from the LinkSwitch-HP family of ICs. It contains the complete power supply specifications, bill of materials, transformer construction, schematic diagram and printed circuit board layout, along with performance data and electrical waveforms.

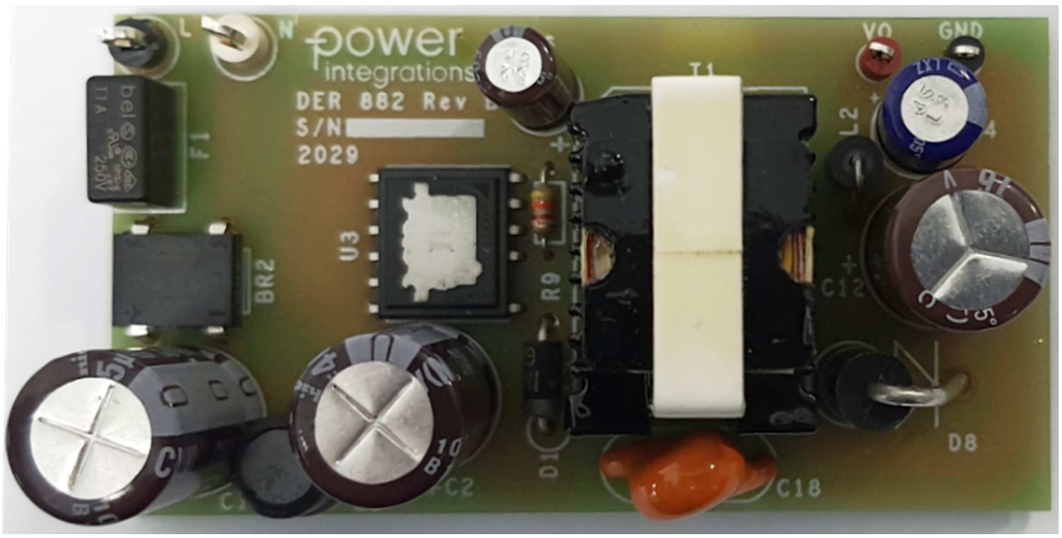

Figure 1 – Prototype Top View.

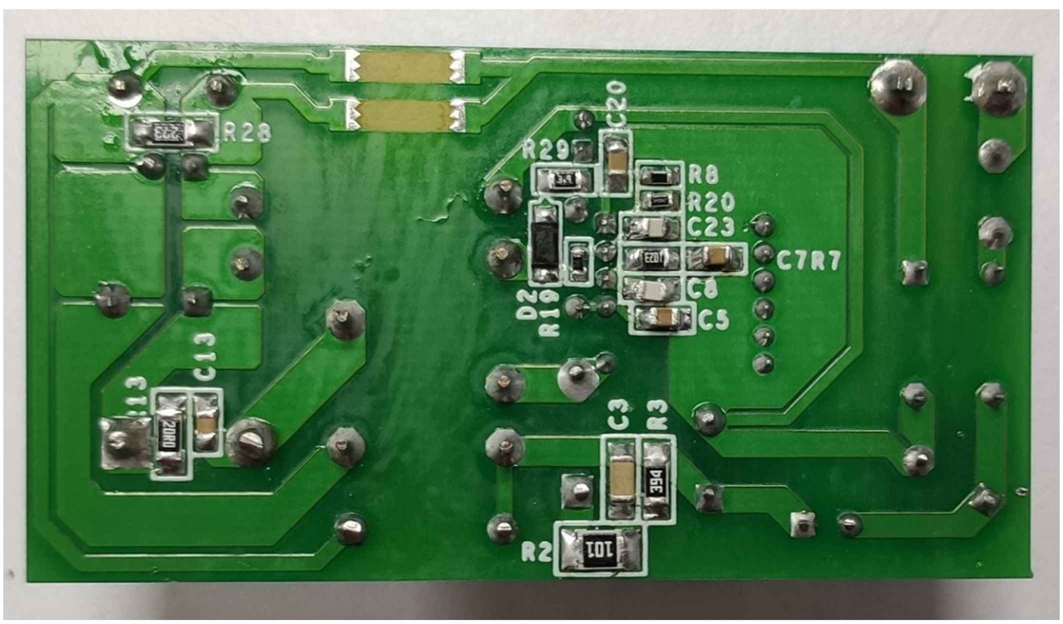

Figure 2 – Prototype Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2-Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Input Power at Standby				30	mW	230Vac
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz Bandwidth.
Output Current	I_{OUT}			1.25	A	
Min. Output Current	$I_{OUT,MIN}$			62.5	mA	System Load upon Insertion.
Total Output Power						
Continuous Output Power	P_{OUT}			15	W	
Efficiency						
Full Load (nominal)	η	84			%	Measured at P_{OUT} 25 °C.
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{DOE}	83			%	Measured at Nominal Input 115 VAC and 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				6dB Margin
Surge (Differential)				1	kV	1.2/50 μs Surge, IEC 61000-4-5, Series Impedance: 2 Ω
ESD – Air Discharge		-15		15	kV	Class A
ESD – Contact Discharge		-8		8	kV	Class A
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level.

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3 Schematic

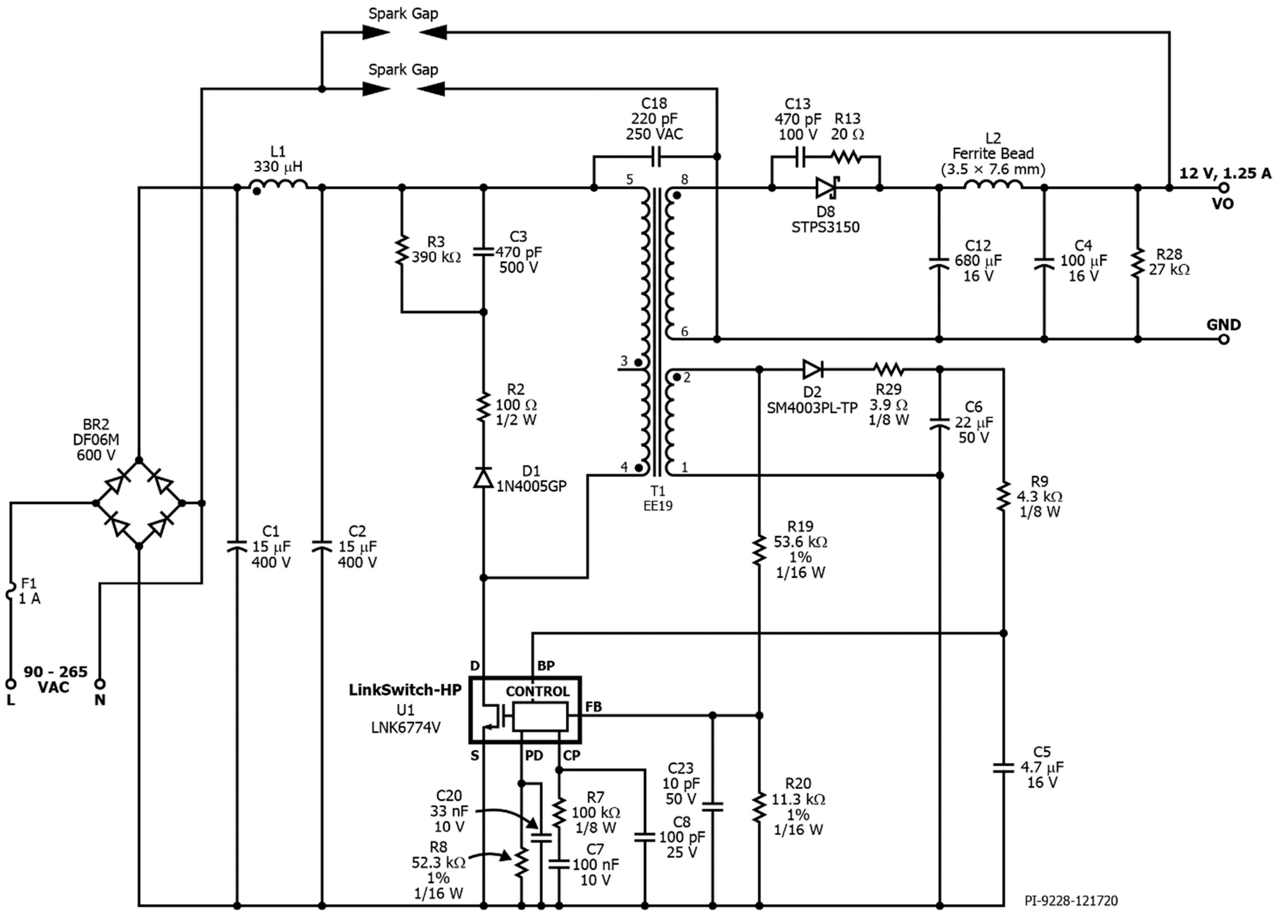

Figure 3 – Schematic.

4 Circuit Description

The circuit shown in Figure 3 utilizes the LNK6774V device in a 12 V, 15 W isolated flyback power supply.

4.1 *Input Rectifier and Filter*

Fuse, F1, isolates the circuit and provides protection from component failure. Bridge diode, D3, rectifies the input AC while capacitors C1, C2, and inductor L1 constitute a pi filter for EMI attenuation.

4.2 *LinkSwitch-HP Primary*

The LNK6774V IC combines a high-voltage power MOSFET and the power supply controller into a low cost monolithic IC.

When AC is first applied, an internal current source connected to the DRAIN (D) pin charges C5 to power the controller inside the IC. During steady-state, the device controller will now be powered via a bias winding through the current limiting resistor R9 to minimize losses.

At the start of a switching cycle, the internal power MOSFET turns on, allowing current to ramp up in the primary winding up to a threshold set by the output of the internal error amplifier pin voltage, CP. Due to the phase orientation of the transformer windings, the freewheeling diode, D8, is reverse biased at this cycle. D8 will only conduct when the internal power MOSFET is off, allowing the energy stored in the core of the transformer to be delivered to the output.

Capacitor C5 (4.7 μF) connected to the BYPASS (BP) pin sets over-temperature protection (OTP) to hysteretic mode, and overvoltage protection (OVP) and lost regulation protection to automatic-restart attempts, AR, after a given off-period (typ. 1.5 s).

4.3 *Primary RCD Snubber*

Snubber components, R3 and C3, limit the voltage stress across the internal power MOSFET while resistor R2 damps drain oscillations for better output voltage regulation and EMI response.

4.4 *Output Rectification*

DC output voltage is rectified via the freewheeling diode, D8, and filtered by the output capacitor, C12. Post-filtering with L2 and C4 provide further reduction of the high frequency components of the output ripple. R13 and C13 provide high frequency filtering for improved EMI.

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4.5 *External Current Limit Setting*

The maximum cycle-by-cycle current limit is set by the resistor R8 connected to the PROGRAM (PD) pin. A 52.3 kΩ resistor in the design sets the maximum current limit to 80% of the LNK6774V's default current limit.

4.6 *Feedback and Compensation Network*

The output voltage is indirectly sensed through the bias winding via a resistor divider (R19 and R20). The sensed output voltage is then compared to the FEEDBACK (FB) pin for proper regulation. This network is also used to indirectly monitor the bus voltage during start-up and enables output power delivery only when the input voltage reaches the brown-in threshold (100 V typ.), and stops below brown-out condition (40 V typ.). In case the bus voltage reaches excessive levels (e.g. caused by line surge) the device stops switching. Additionally, the cycle-by-cycle current limit is compensated over line to limit the available overload power. See the device data sheet for further details.

Since the design utilizes primary-side regulation, no optocoupler is required. This not only reduces the system cost, but also improves the long term reliability of the system.

The controller uses a high gain (typ. 70 dB) transconductance amplifier to ensure exceptional output regulation. Feedback compensation is provided by R7, C7 and C8 with the recommended values implemented in this design.

5 PCB Layout

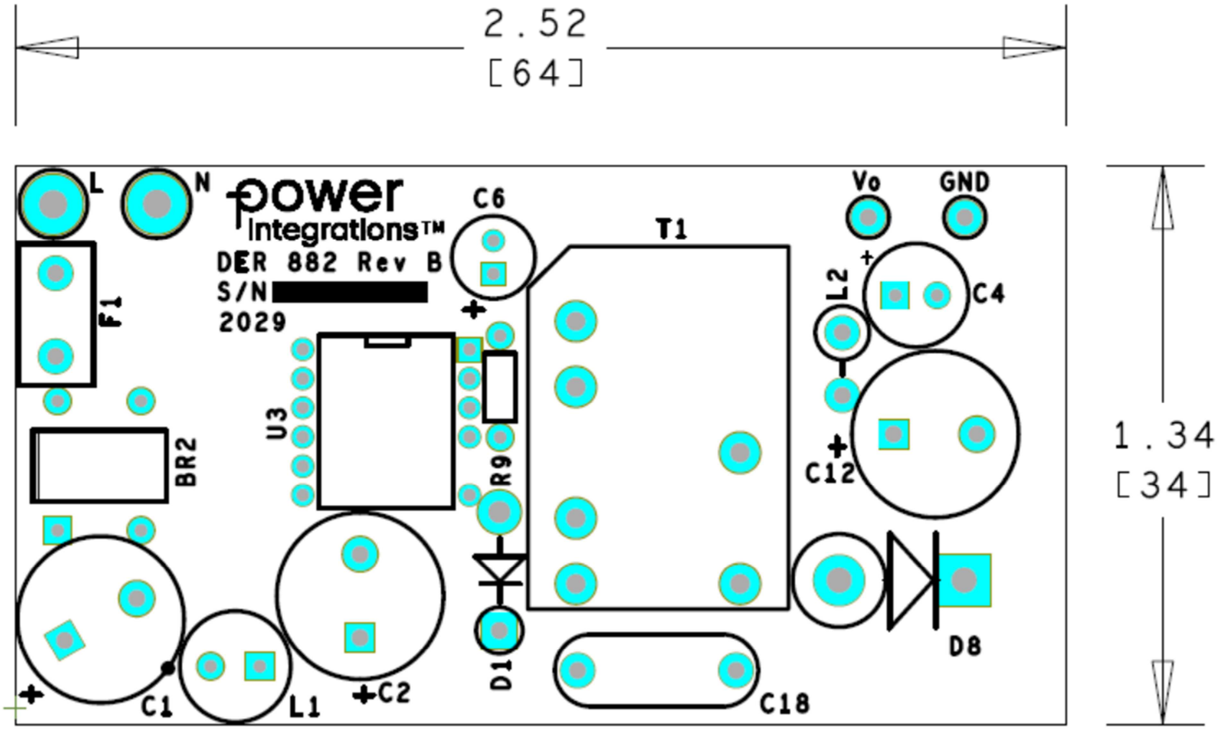

Figure 4 – Populated Circuit Board, Top View.

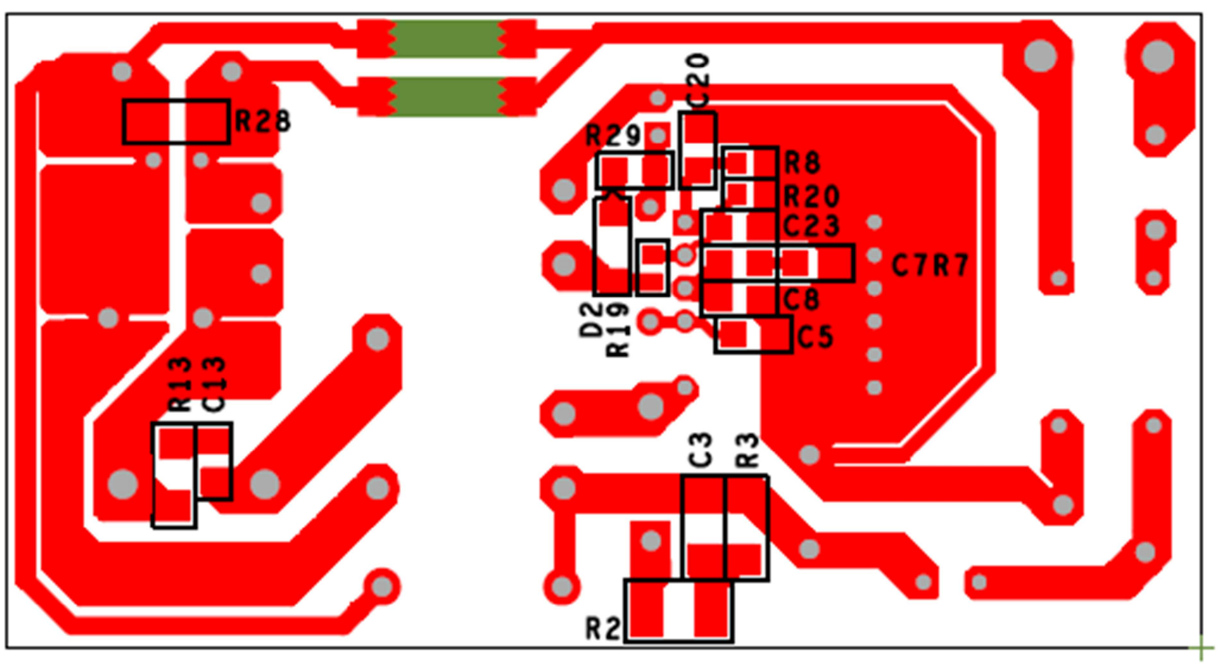

Figure 5 – Populated Circuit Board, Bottom View.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1, C2	15 µF, 400 V, Electrolytic, (10 x 20)	UCY2G150MPD	Nichicon
2	1	C3	470 pF, 500 V, Ceramic, X7R, 1206	CC1206KKX7RBBB471	Yageo
3	1	C4	100 µF, 16 V, 20%, Electrolytic, Low ESR 250 mΩ, (6.3 x 11.5)	ELXZ160ELL101MFB5D	Nippon Chemi-Con
4	1	C5	4.7 µF, +10%, 16 V, Ceramic, X7R, 0805	GRM21BR71C475KE51L	Murata
5	1	C6	22 µF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
6	1	C7	100 nF, 10 V, Ceramic, X7R, 0805	0805ZC104MAT2A	AVX
7	1	C8	100 pF, +10%, 25 V, Ceramic, X7R, 0805	C0805C101K3RAC7800	Kemet
8	1	C12	680 µF, 16 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE160ELL681MJ16S	Nippon Chemi-Con
9	1	C13	470 pF, 100 V, Ceramic, X7R, 0805	08051C471KAT2A	AVX
10	1	C18	220 pF, Ceramic Y1	440LT22-R	Vishay
11	1	C20	33 nF, 10 V, Ceramic, X7R, 0805	0805ZC333KAT2A	AVX
12	1	C23	10 pF, 50 V, Ceramic, NP0, 0805	C0805C100J5GACTU	Kemet
13	1	D1	600 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41	1N4005GP-E3/54	Vishay
14	1	D2	200 V, 1 A, Standard Recovery, SOD123-FL	SM4003PL-TP	Micro Commercial
15	1	BR2	600 V, 1 A, Bridge Rectifier, DFM	DF06M	Diodes, Inc.
16	1	D8	150 V, 3 A, Schottky, DO-201AD	STPS3150RL	ST Micro
17	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
18	1	L1	330 µH, 0.300 A, 20%	RL-5480-2-330	Renco
19	1	L2	Ferrite Bead (3.5 mm x 7.6 mm)	2743004112	Fair-Rite
20	1	R2	100 Ω, 5%, 1/2 W, Thick Film, 1210	ERJ-14YJ101U	Panasonic
21	1	R3	RES, 390 kΩ, 1/4 W, Thick Film, 1206	ERJ-8GEYJ394V	Panasonic
22	1	R7	100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
23	1	R8	52.3 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5232V	Panasonic
24	1	R9	RES, 4.3 kΩ, 5%, 1/8 W, Carbon Film	CF18JT4K30	Stackpole
25	1	R13	20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
26	1	R19	RES, 53.6 kΩ, 1%, 1/16 W, Thick Film 0603	ERJ-3EKF5362V	Panasonic
27	1	R20	RES, 11.3 kΩ, 1%, 1/16 W, Thick Film 0603	ERJ-3EKF1132V	Panasonic
28	1	R28	27 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ273V	Panasonic
29	1	R29	3.9 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ3R9V	Panasonic
30	1	T1	Bobbin EE19, Vertical, 10 Pins	TF-1932	Shulin Enterprise
31	1	U3	LinkSwitch-HP,eDIP-12P	LNK6774V	Power Integrations

Miscellaneous

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	L	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
2	1	N	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
3	1	VO	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
4	1	GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

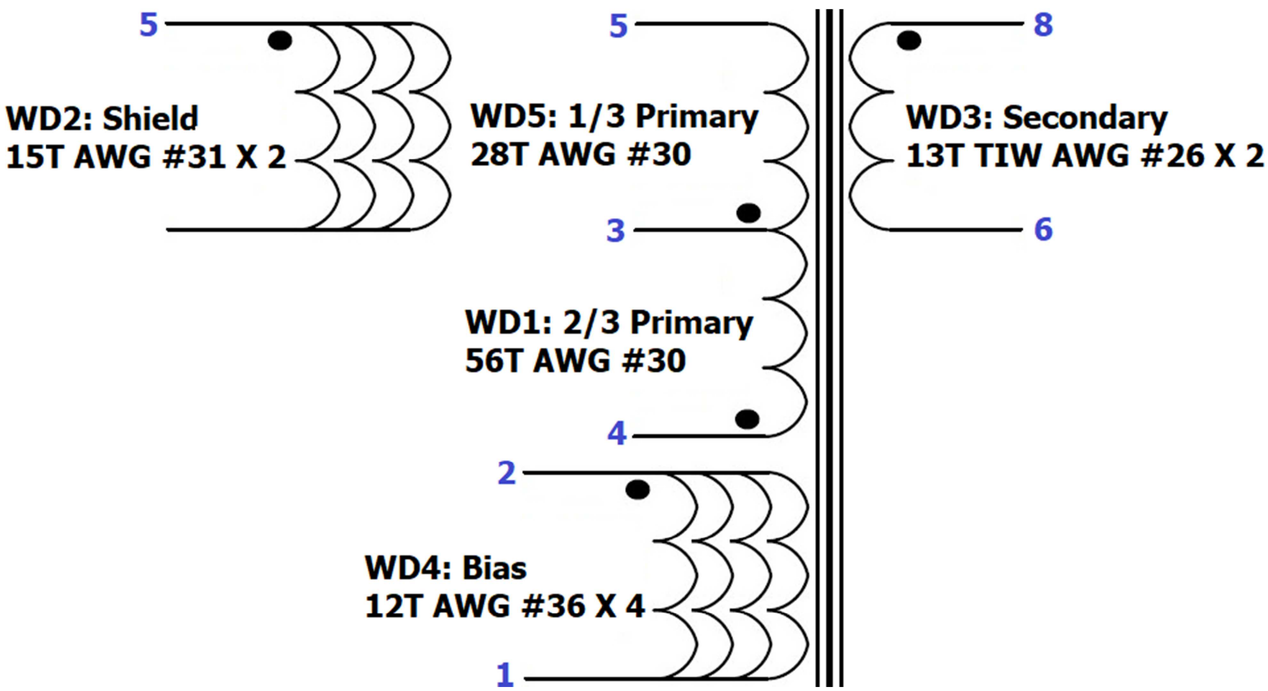

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and pin 5 with all other windings open.	660 µH ±10%
Leakage Inductance	Measured across primary winding with all other windings shorted.	<20 µH

7.3 *Material List*

Item	Description
[1]	Core: EE19, NC-2H (Nicera) or equivalent, gapped at 92 nH/t^2.
[2]	Bobbin: EE19 Bobbin Vertical 10-pin.
[3]	Magnet Wire: #30 AWG.
[4]	Magnet Wire: #31 AWG.
[5]	Magnet Wire: #36 AWG.
[6]	Tripe Insulated Wire: #26 AWG.
[7]	Polyester Tape: 9 mm.
[8]	Polyester Tape: 5 mm.

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7.4 *Transformer Build Diagram*

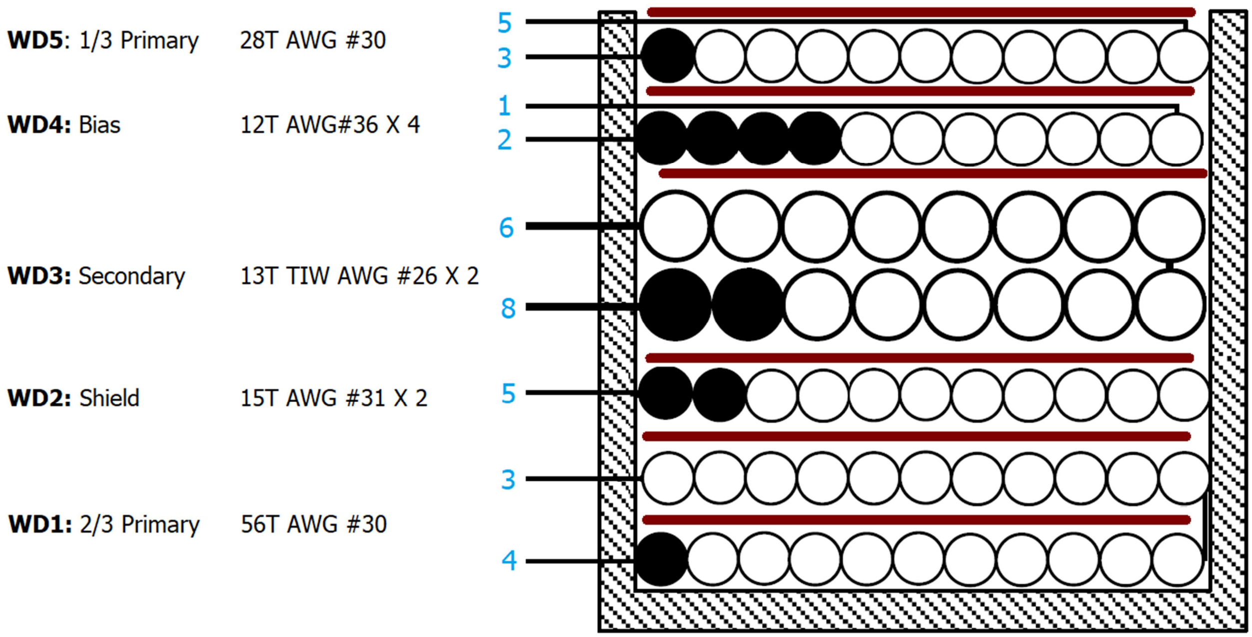
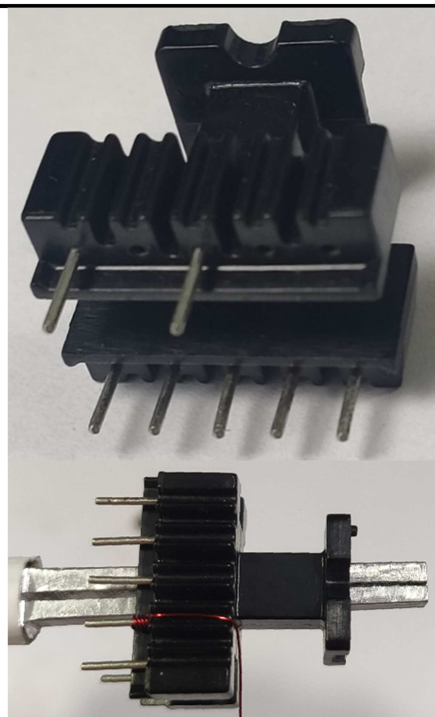
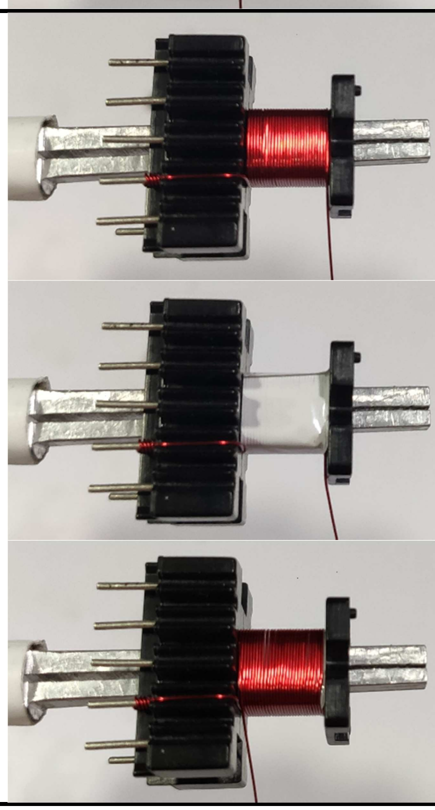


Figure 7 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Bobbin Preparation	For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise. Before winding, remove pins 7, 9, and 10.
WD1 2/3 Primary	Start at pin 4. Wind 28 turns of wire, Item [3] for the first layer. Add a layer of tape, Item [7], and then another 28 turns of wire, Item [3], for the second layer. Terminate to pin 3.
Insulation	1 layer of tape Item [7]
WD2 Shield	Prepare 2 strands of wire Item [4]. Start at pin 5 and wind 15 turns for layer 3. The end part of the wire is unterminated and will be cut after the 15 turns.
Insulation	1 layer of tape Item [7]
WD3 Secondary	Prepare 2 strands of wire Item [6]. Start at pin 8 and wind 13 turns for layers 5 and 6. Terminate to pin 6.
Insulation	1 layer of tape Item [7]
WD4 Bias	Prepare 4 strands of wire Item [5]. Start at pin 2 and wind 12 turns in one layer. Terminate to pin 1.
Insulation	1 layer of tape Item [7]
WD5 1/3 Primary	Start at pin 3. Wind 28 turns of wire, Item [3] for the last layer and terminate to pin 5.
Insulation	1 layer of tape Item [7]
Finish	Gap cores to get 660 μH. Wrap the core with Item [8] and solder the wire terminations. Cut the remaining portion of pin 3 just slightly above the bobbin for proper transformer mounting into the PCB.

7.6 ***Transformer Winding Illustrations***

Bobbin Preparation		For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise. Before winding, remove pins 7, 9, and 10.
WD1 2/3 Primary		Start at pin 4. Wind 28 turns of wire, Item [3] for the first layer. Add a layer of tape, Item [7], and then another 28 turns of wire, Item [3], for the second layer. Terminate to pin 3.

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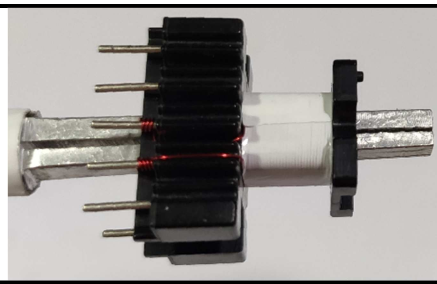
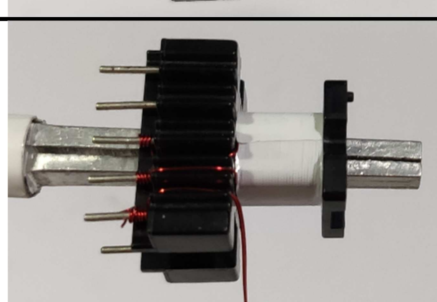
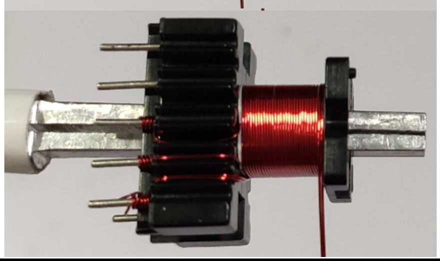
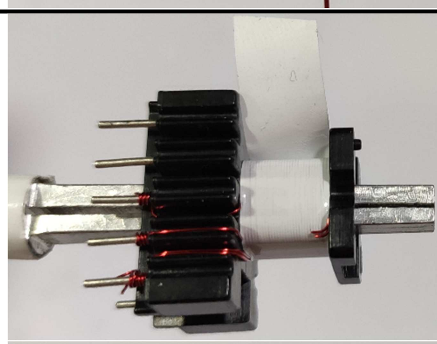
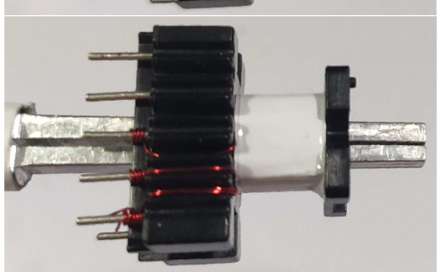
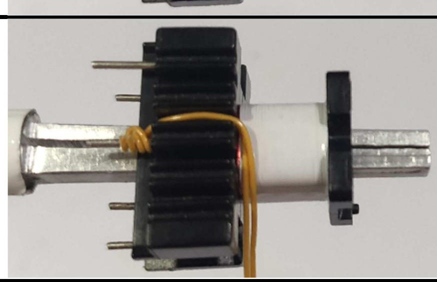
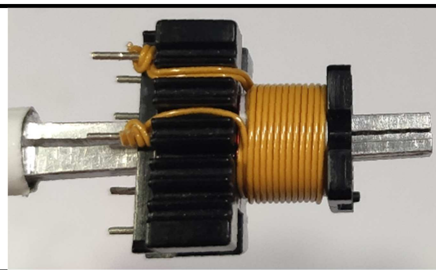
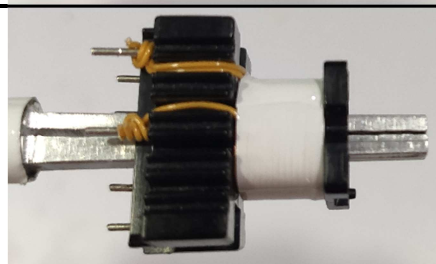
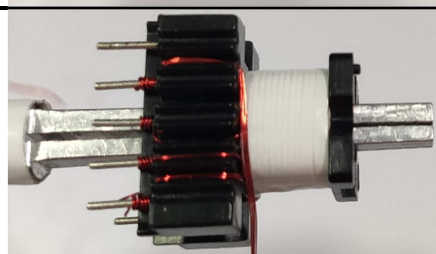
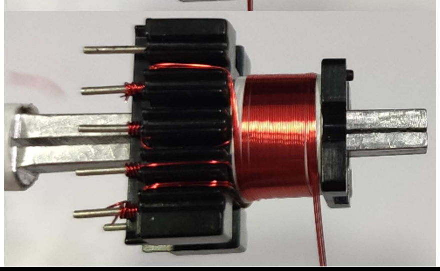
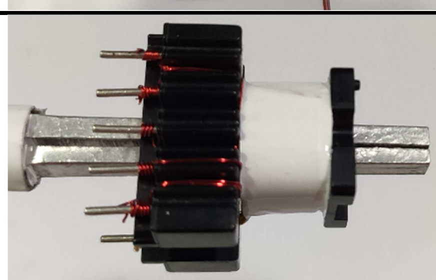
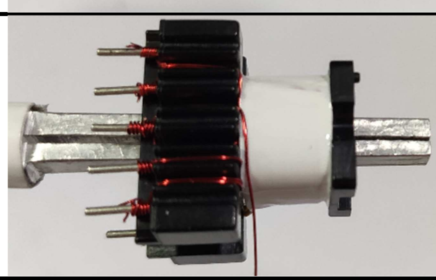
Insulation		1 layer of tape Item [7]
WD2 Shield	 	Prepare 2 strands of wire Item [4]. Start at pin 5 and wind 15 turns for layer 3. The end part of the wire is unterminated and will be cut after the 15 turns.
Insulation	 	1 layer of tape Item [7]
WD3 Secondary		Prepare 2 strands of wire Item [6]. Start at pin 8 and wind 13 turns for layers 5 and 6. Terminate to pin 6.

		
Insulation		1 layer of tape Item [7]
WD4 **Bias**	 	Prepare 4 strands of wire Item [5]. Start at pin 2 and wind 12 turns in one layer. Terminate to pin 1.
Insulation		1 layer of tape Item [7]
WD5 **1/3 Primary**		Start at pin 3. Wind 28 turns of wire, Item [3] for the last layer and terminate to pin 5.

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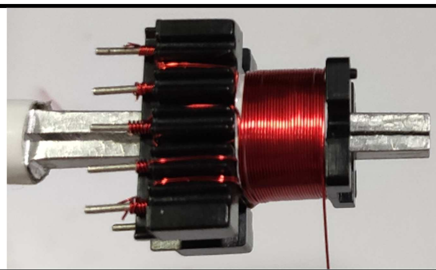
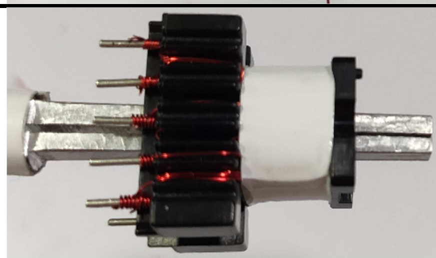
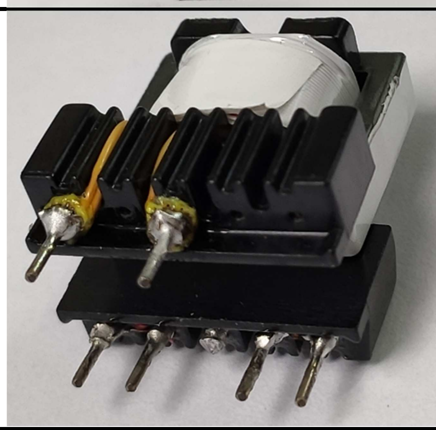
		
Insulation		1 layer of tape Item [7]
Finish		Gap cores to get 660 uH. Wrap the core with Item [8] and solder the wire terminations. Cut the remaining portion of pin 3 just slightly above the bobbin for proper transformer mounting into the PCB.

8 Design Spreadsheet

ACDC_LinkSwitch-HP_112818; Rev.2.1; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchHP_112818 Rev 2-1.xls: LinkSwitch-HP Flyback Continuous/Discontinuous Transformer Design Spreadsheet
APPLICATION VARIABLES					
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO			12.00	V	Output Voltage (main)
PO	15.00		15.00	W	Load Power
n	0.83		0.83		Efficiency Estimate
Z			0.50		Loss Allocation Factor
VB			10.00	V	Bias Voltage
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	30		30	uF	Input Filter Capacitor
Package	E/V		E/V		E and V Package Selected
Enclosure	Open Frame		Open Frame		Open Frame type enclosure
Heatsink	PCB-W		PCB-W		PCB heatsink with wave soldering
LinkSwitch-HP VARIABLES					
LinkSwitch-HP	LNK6774V		LNK6774V		Manual Device Selection
ILIMITMIN			0.967	A	Minimum Current limit
ILIMITMAX			1.113	A	Maximum current limit
ILIMITMIN_EXT			0.774	A	External Minimum Current limit
ILIMITMAX_EXT			0.89	A	External Maximum current limit
KI	Auto		0.8		Current limit reduction factor
Rpd			52.30	k-ohm	Program delay Resistor
Cpd			33.0	nF	Program delay Capacitor
Total programmed delay			0.38	sec	Total program delay
fS			132	kHz	LinkSwitch-HP Switching Frequency
fSmin			120	kHz	LinkSwitch-HP Minimum Switching Frequency
fSmax			136	kHz	LinkSwitch-HP Maximum Switching Frequency
KP	0.78		0.78		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	80.00		80.00	V	Reflected Output Voltage
Voltage Sense					
VUVON			96.94	V	Undervoltage turn on
VUVOFF			40.39	V	Undervoltage turn off
VOV			443.90	V	Overvoltage threshold
FMAX_FULL_LOAD			136.00	kHz	Maximum switching frequency at full load
FMIN_FULL_LOAD			120.00	kHz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD			3.81	us	Minimum available Diode conduction time at full load. This should be greater than 2.5 us
TSAMPLE_LIGHT_LOAD			1.44	us	Minimum available Diode conduction time at light load. This should be greater than 1.4 us
VDS			1.96	V	LinkSwitch-HP on-state Drain to Source Voltage.
VD			0.50	V	Output Winding Diode Forward Voltage Drop
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
FEEDBACK SENSING SECTION					
RFB1			54.90	k-ohms	Feedback divider upper resistor
RFB2			11.30	k-ohms	Feedback divider lowerr resistor
TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Select Core Size	EE19		EE19		Manual Core Selected
Core			EE19		Selected Core
Custom Core					Enter name of custom core is applicable
AE			0.23	cm^2	Core Effective Cross Sectional Area
LE			3.94	cm	Core Effective Path Length
AL			1250	nH/T^2	Ungapped Core Effective Inductance
BW			9.10	mm	Bobbin Physical Winding Width

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M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3		Number of Primary Layers
NS	13		13		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			88	V	Minimum DC Input Voltage
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.48		Maximum Duty Cycle
IAVG			0.21	A	Average Primary Current
IP			0.70	A	Peak Primary Current
IR			0.54	A	Primary Ripple Current
IRMS			0.32	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP_TYP			660	uH	Typical Primary Inductance
LP_TOL			10	%	Primary inductance Tolerance
NP			84		Primary Winding Number of Turns
NB			12		Bias Winding Number of Turns
ALG			94	nH/T^2	Gapped Core Effective Inductance
BM			2385	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3346	Gauss	Peak Flux Density (BP<3700)
BAC			930	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1704		Relative Permeability of Ungapped Core
LG			0.29	mm	Gap Length (Lg > 0.1 mm)
BWE			27.3	mm	Effective Bobbin Width
OD			0.33	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.27	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			322	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			4.51	A	Peak Secondary Current
ISRMS			2.11	A	Secondary RMS Current
IO			1.25	A	Power Supply Output Current
IRIPPLE			1.70	A	Output Capacitor RMS Ripple Current
CMS			423	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			23	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.58	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.70	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.06	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			563	V	Peak voltage across drain to source of Linkswitch-HP
PIVS			70	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB			64	V	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12.00	V	Output Voltage
IO1			1.25	A	Output DC Current
PO1			15	W	Output Power
VD1			0.50	V	Output Diode Forward Voltage Drop

NS1			13.00		Output Winding Number of Turns
ISRMS1			2.113	A	Output Winding RMS Current
IRIPPLE1			1.70	A	Output Capacitor RMS Ripple Current
PIVS1			70	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1			423	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			23	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.58	mm	Minimum Bare Conductor Diameter
ODS1			0.70	mm	Maximum Outside Diameter for Triple Insulated Wire

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9 Performance Data

9.1 *Efficiency*

9.1.1 Average Efficiency

9.1.1.1 90 VAC / 60 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	90	339.77	17.40	11.66	1250.10	14.57	83.78
75%	90	266.19	12.97	11.73	937.80	11.00	84.79
50%	90	192.12	8.65	11.81	625.30	7.39	85.38
25%	90	113.73	4.41	11.93	312.80	3.73	84.59
						Average	**84.64**

9.1.1.2 115 VAC / 60 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} m(A_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	115	287.01	17.18	11.70	1250.10	14.62	85.12
75%	115	228.60	12.88	11.75	937.70	11.02	85.53
50%	115	167.88	8.67	11.82	625.30	7.39	85.26
25%	115	100.00	4.44	11.93	312.80	3.73	84.13
						Average	**85.01**

9.1.1.3 230 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	230	186.61	17.12	11.71	1250.10	14.63	85.47
75%	230	152.25	13.04	11.76	937.70	11.03	84.58
50%	230	112.84	8.85	11.84	625.30	7.40	83.66
25%	230	66.44	4.59	11.96	312.80	3.74	81.45
						Average	**83.79**

9.1.1.4 265 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	265	174.52	17.15	11.71	1250.10	14.64	85.36
75%	265	142.17	13.13	11.77	937.70	11.04	84.07
50%	265	106.38	8.88	11.85	625.30	7.41	83.46
25%	265	61.77	4.67	11.99	312.80	3.75	80.34
						Average	**83.31**

9.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line.

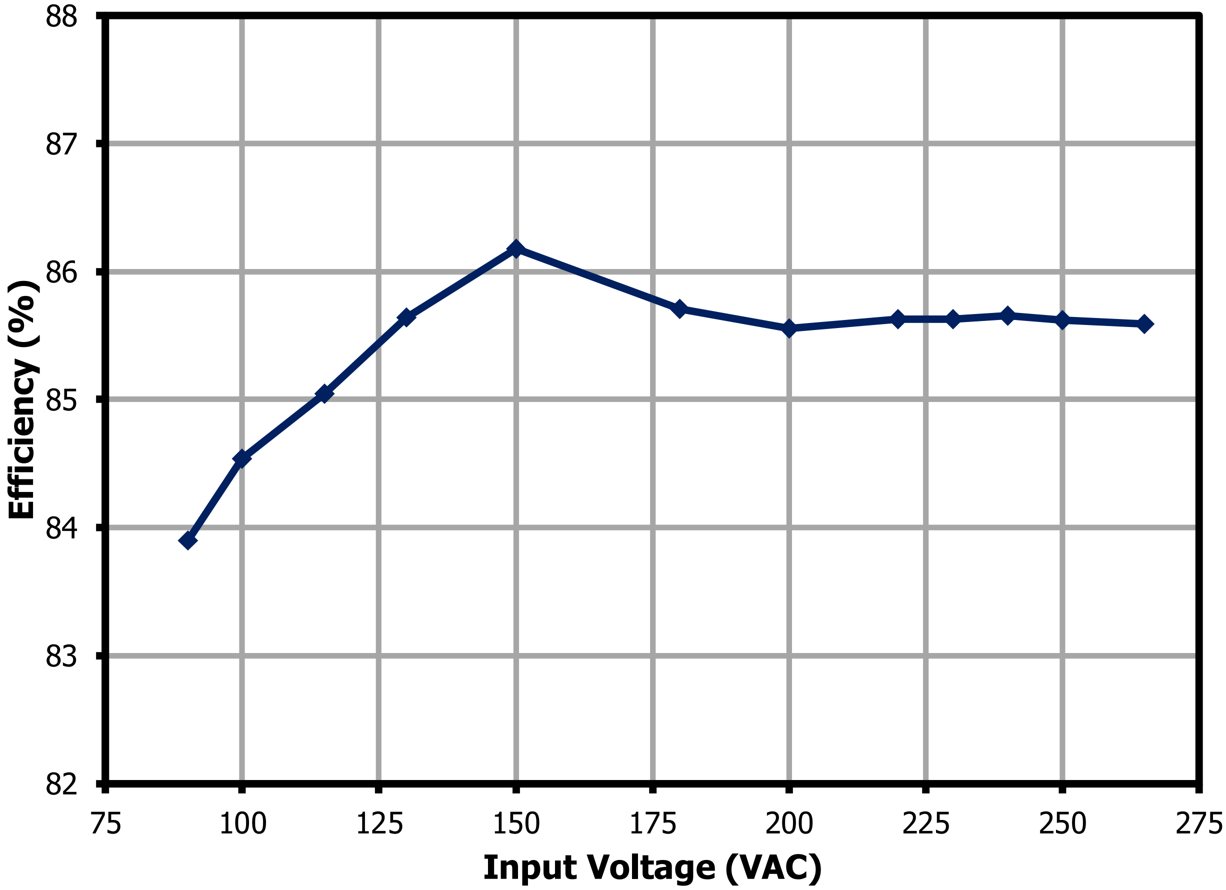

Figure 8 – Full Load Efficiency vs. Line.

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9.1.3 Efficiency vs. Load

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

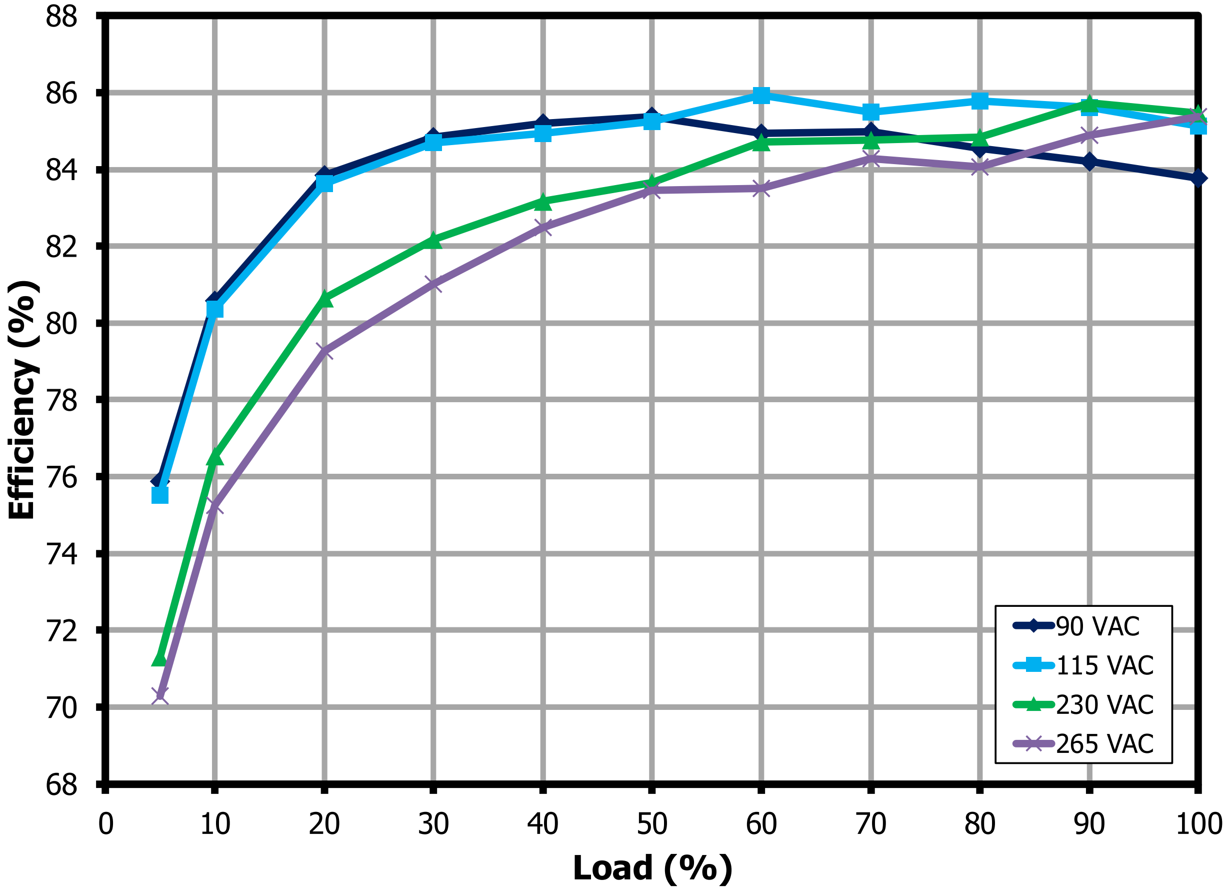

Figure 9 – Efficiency vs. Percentage Load.

9.2 *Available Standby Output Power*

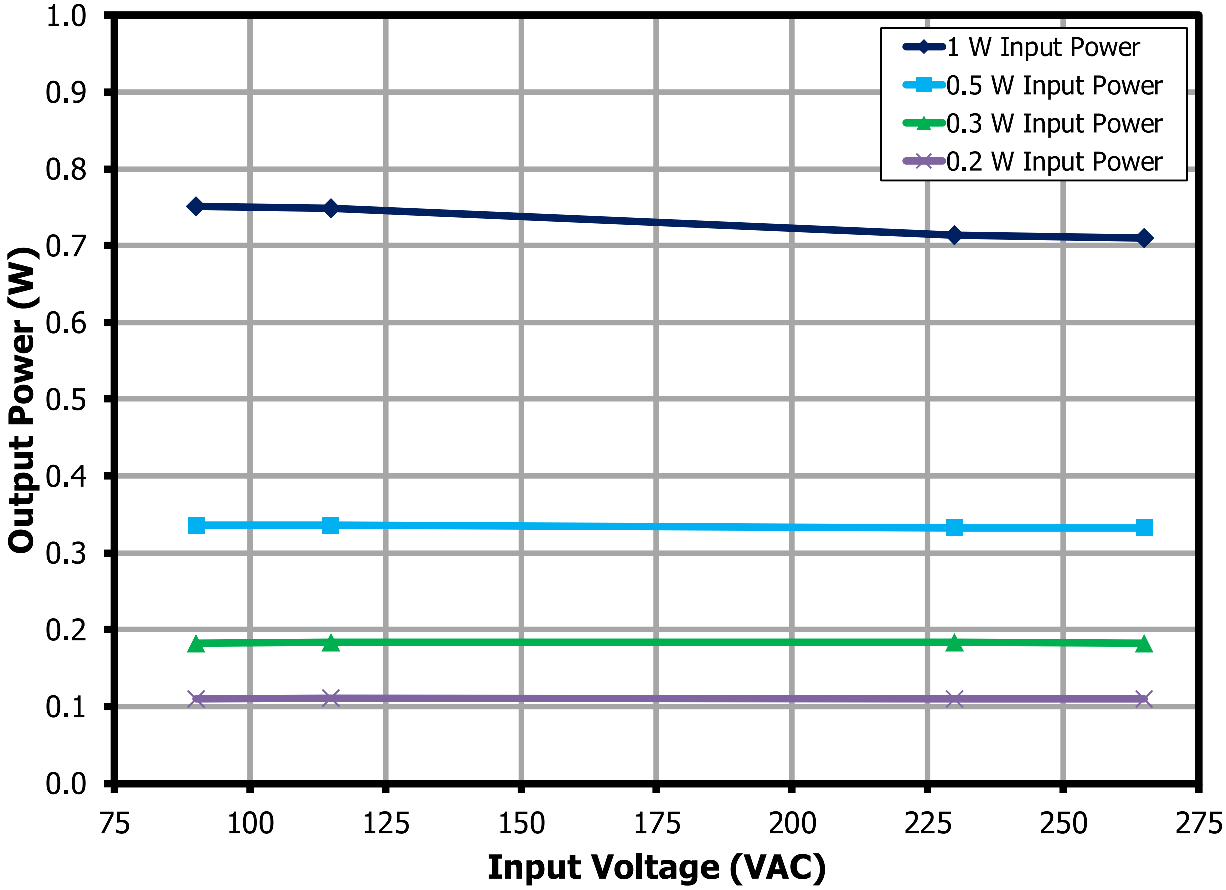

Figure 10 – Available Standby Output Power for 0.2 W, 0.3 W and 0.5 W and 1 W Input Power.

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9.2.1 0.2 W Input Power

Input Measurement			Output 1 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
90	11.768	0.2	12.126	9.004	0.1092	54.60
115	10.080	0.2	12.111	9.102	0.1103	55.15
230	5.557	0.2	12.103	9.103	0.1101	55.05
265	4.627	0.2	12.108	9.101	0.1102	55.10

9.2.2 0.3 W Input Power

Input Measurement			Output 1 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
90	14.959	0.3	12.093	15.085	0.1824	60.80
115	12.772	0.3	12.080	15.182	0.1834	61.13
230	7.309	0.3	12.076	15.182	0.1833	61.10
265	6.171	0.3	12.082	15.088	0.1823	60.77

9.2.3 0.5 W Input Power

Input Measurement			Output 1 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
90	21.07	0.5	12.062	27.817	0.3356	67.12
115	17.87	0.5	12.050	27.817	0.3362	67.24
230	10.553	0.5	12.051	27.526	0.3317	66.34
265	9.203	0.5	12.059	27.528	0.3320	66.40

9.2.4 1.0 W Input Power

Input Measurement			Output 1 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
90	35.82	1	12	62.61	0.7512	75.12
115	30.31	1	11.992	62.42	0.7485	74.85
230	18.22	1	12.025	59.38	0.7140	71.40
265	16.26	1	12.039	59.00	0.7102	71.02

9.3 *No-Load Input Power*

Test Condition: Soak for 15 minutes each line and 3-minute integration time.

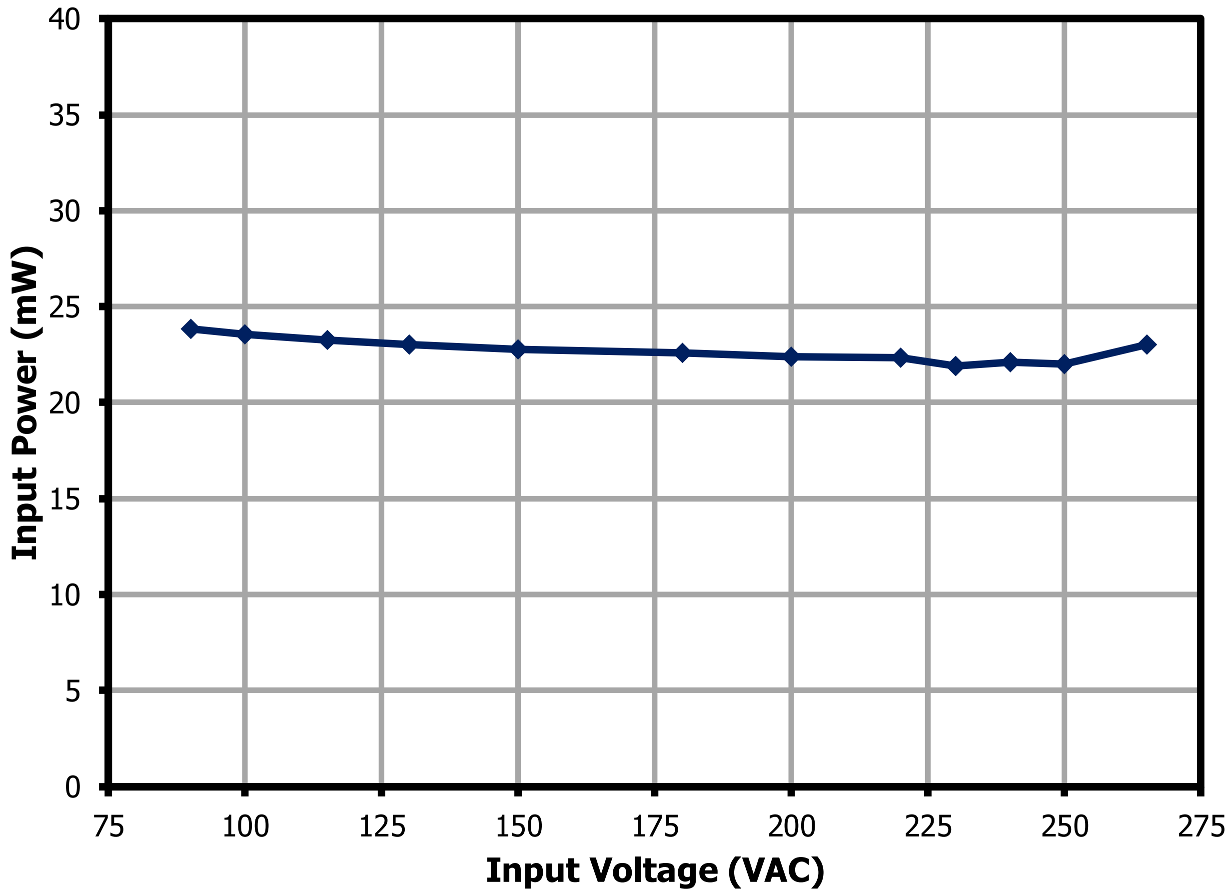

Figure 11 – No-Load Input Power vs. Line at Room Temperature.

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9.4 *Line Regulation*

Test Condition: Soak for 15 minutes for each line.

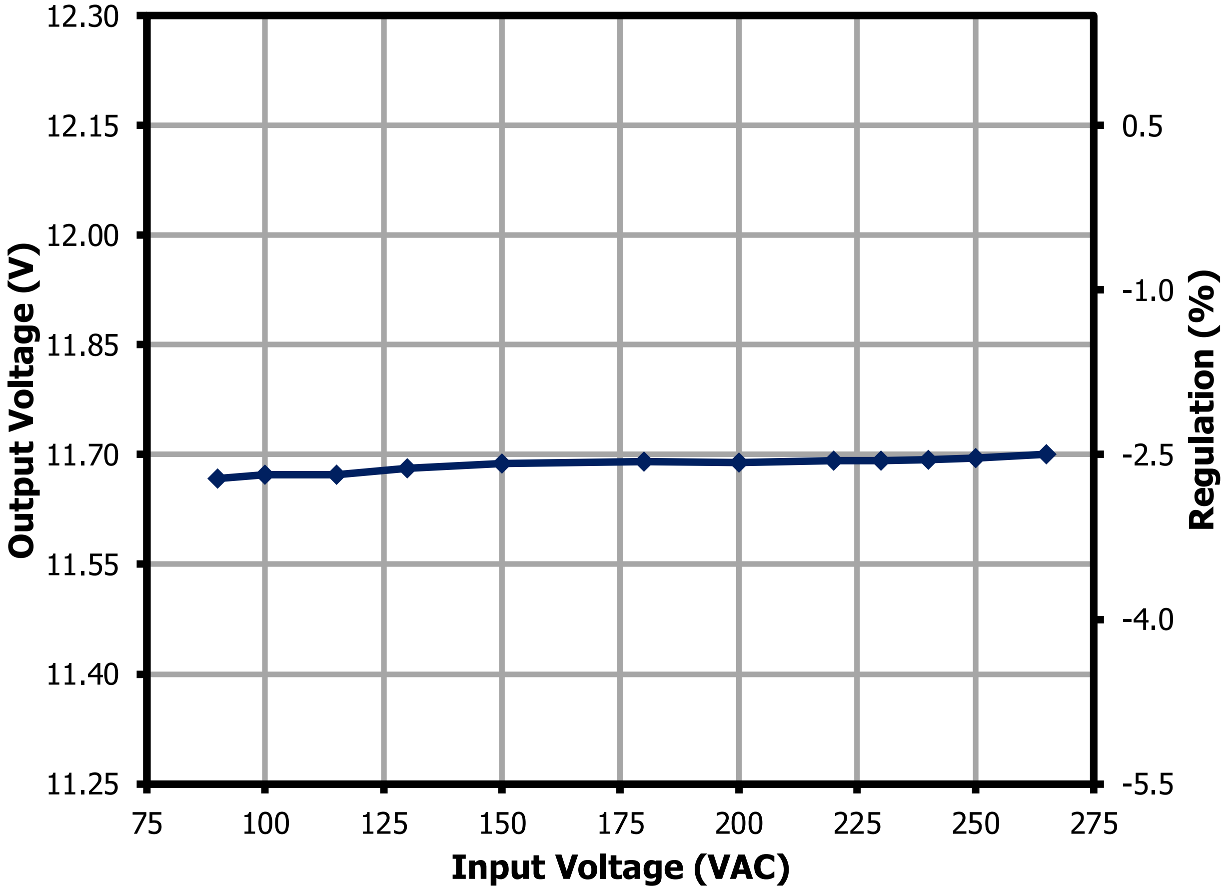

Figure 12 – Output Voltage vs. Line Voltage.

9.5 ***Load Regulation***

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

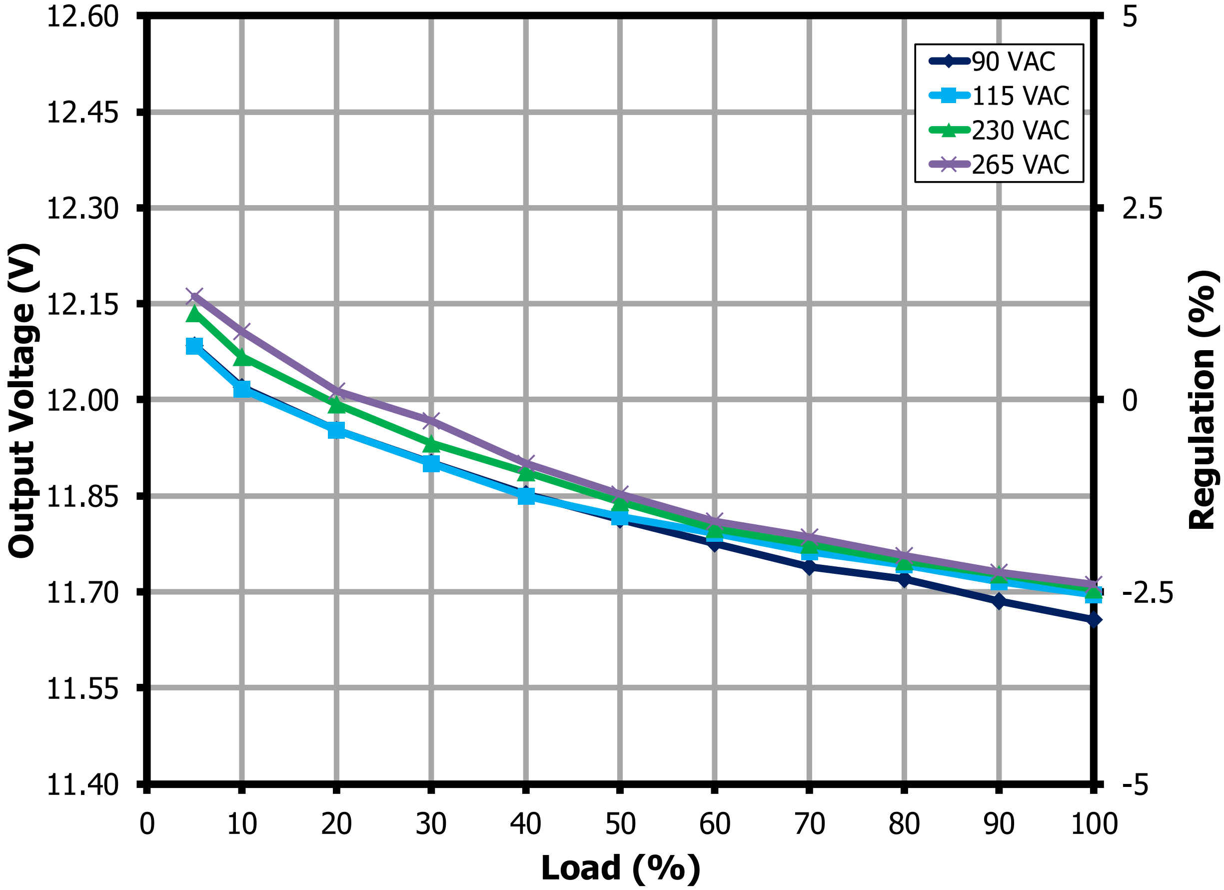

Figure 13 – Output Voltage vs. Percent Load.

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10 Waveforms

10.1 *Load Transient Response*

Test Condition: Dynamic load frequency = 200 Hz, Duty cycle = 50 %

10.1.1 5% - 100% Load Change

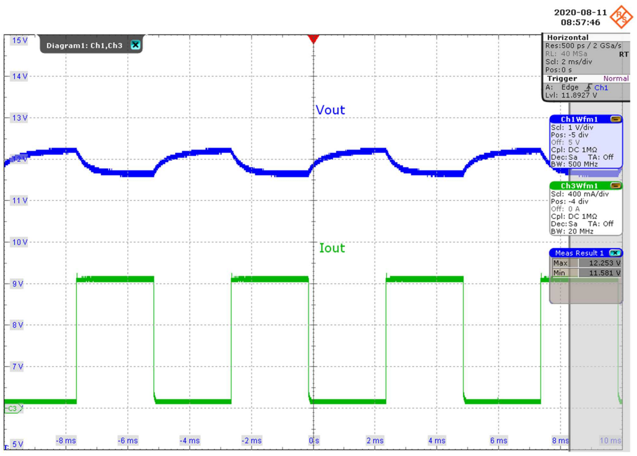

Figure 14 – 90 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.253 V, V_{MIN}: 11.581 V.

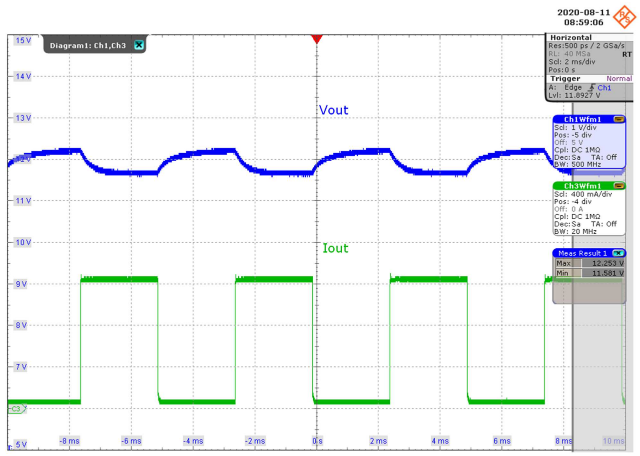

Figure 15 – 115 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.253 V, V_{MIN}: 11.581 V.

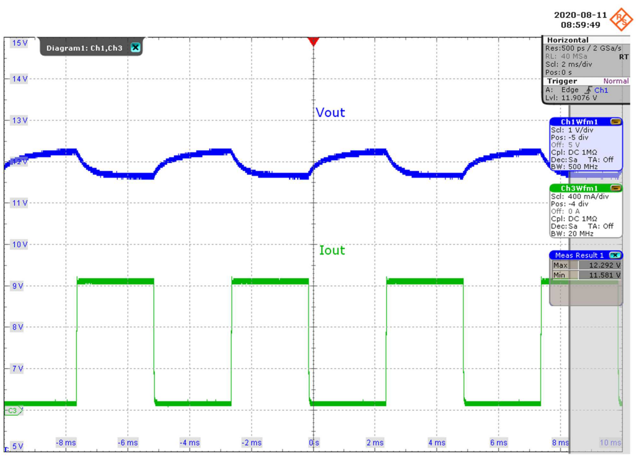

Figure 16 – 230 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.292 V, V_{MIN}: 11.581 V.

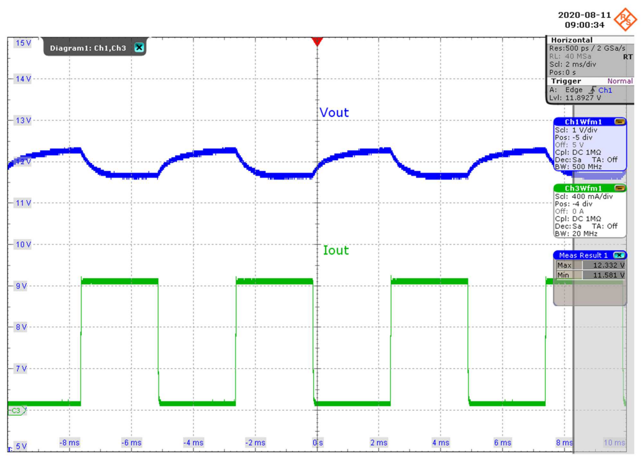

Figure 17 – 265 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.332 V, V_{MIN}: 11.581 V.

10.1.2 50% - 100% Load Change

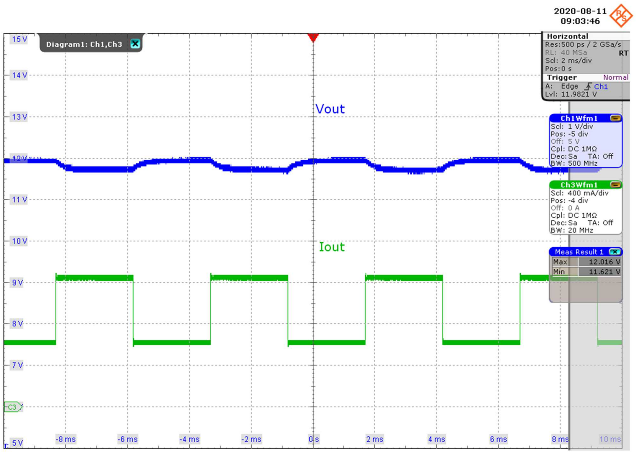

Figure 18 – 90 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.016 V, V_{MIN}: 11.621 V.

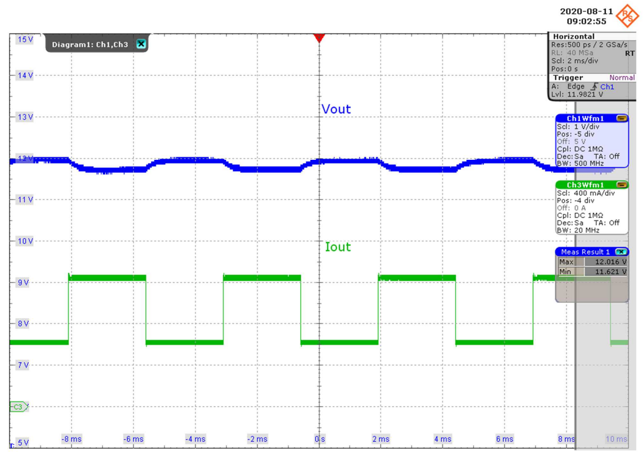

Figure 19 – 115 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.016 V, V_{MIN}: 11.621 V.

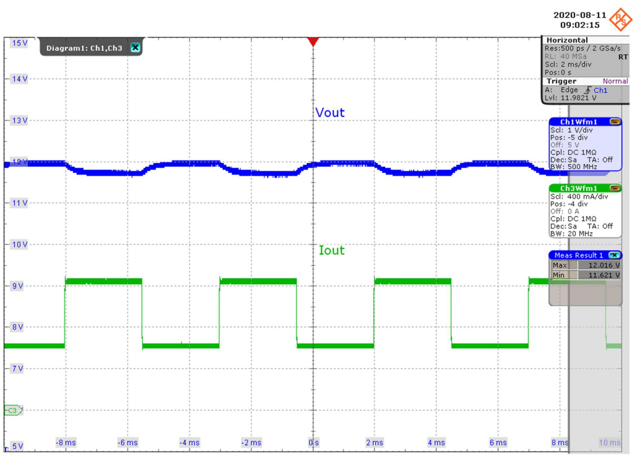

Figure 20 – 230 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.016 V, V_{MIN}: 11.621 V.

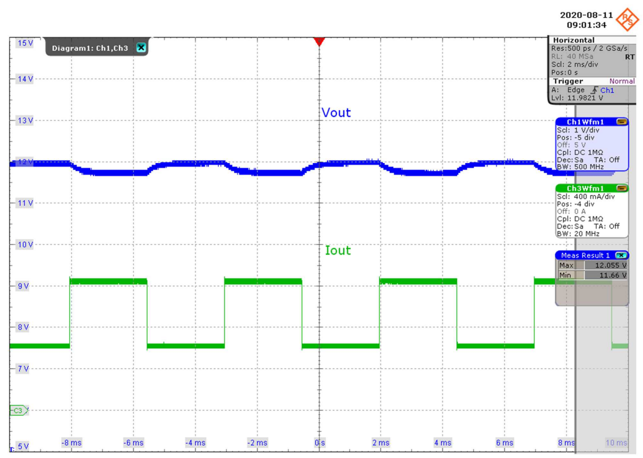

Figure 21 – 265 VAC.
CH1: V_{OUT}, 1 V / div., 2 ms / div.
CH3: I_{OUT}, 400 mA / div., 2 ms / div.
V_{MAX}: 12.055 V, V_{MIN}: 11.660 V.

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10.2 ***Output Voltage at Start-up***

10.2.1 CC Mode

10.2.1.1 100% Load

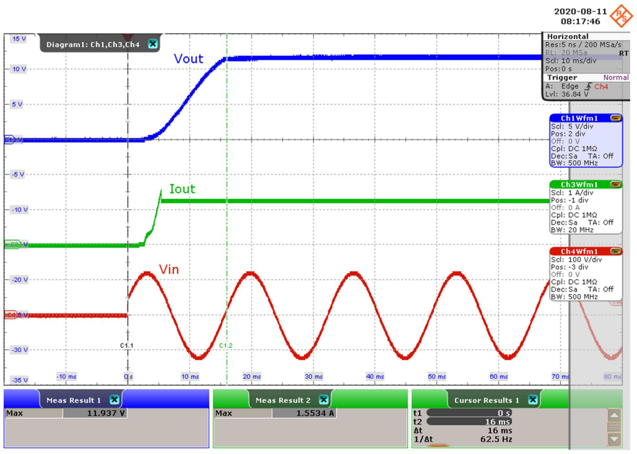

Figure 22 – 90 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 100 V / div., 10 ms / div.
On-Time Delay = 16 ms.
V_{MAX} = 11.94 V.

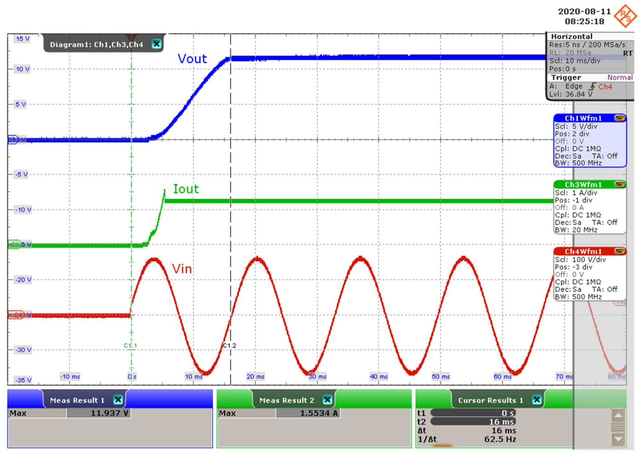

Figure 23 – 115 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 100 V / div., 10 ms / div.
On-Time Delay = 16 ms.
V_{MAX} = 11.94 V.

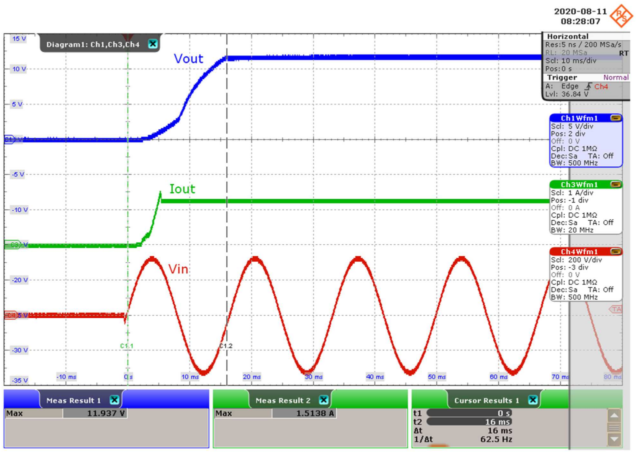

Figure 24 – 230 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 200 V / div., 10 ms / div.
On-Time Delay = 16 ms.
V_{MAX} = 11.94 V.

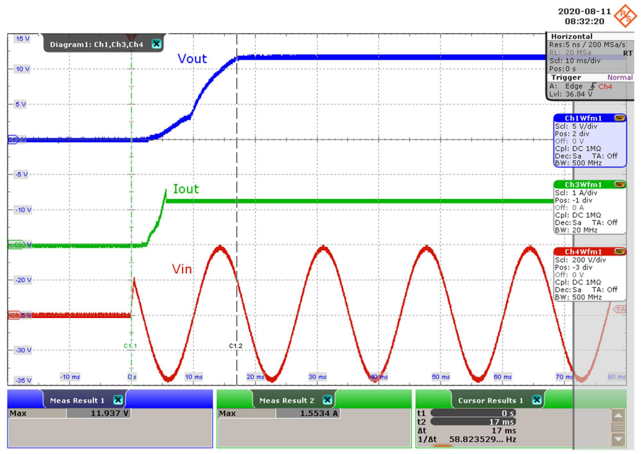

Figure 25 – 265 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 200 V / div., 10 ms / div.
On-Time Delay = 17 ms.
V_{MAX} = 11.94 V.

10.2.1.2 0% Load

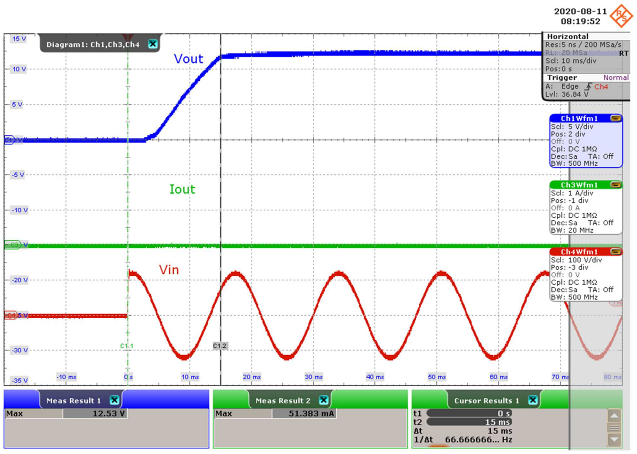

Figure 26 – 90 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 100 V / div., 10 ms / div.
On-Time Delay = 15 ms.
V_{MAX} = 12.53 V.

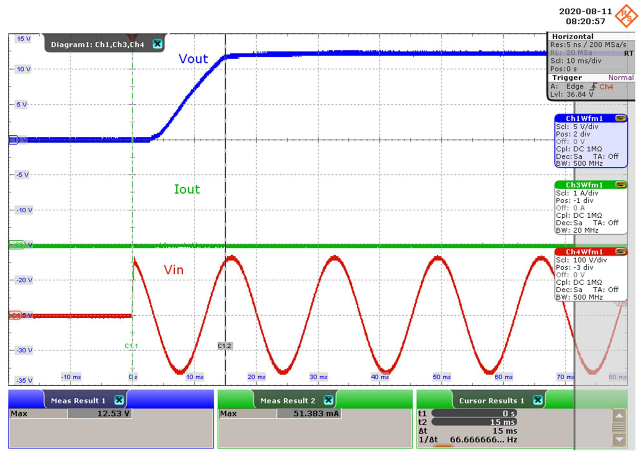

Figure 27 – 115 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 100 V / div., 10 ms / div.
On-Time Delay = 15 ms.
V_{MAX} = 12.53 V.

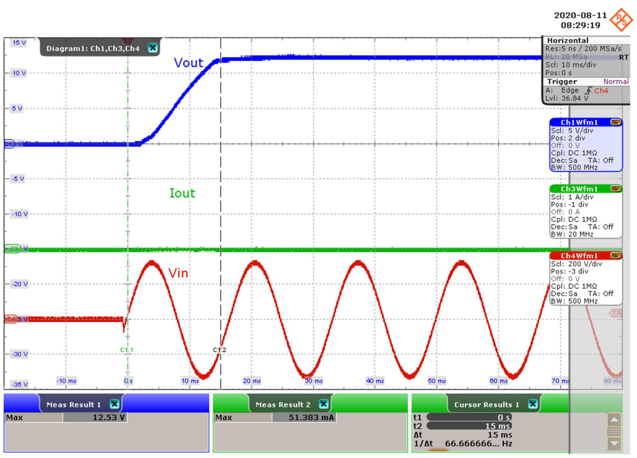

Figure 28 – 230 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 200 V / div., 10 ms / div.
On-Time Delay = 15 ms.
V_{MAX} = 12.53 V.

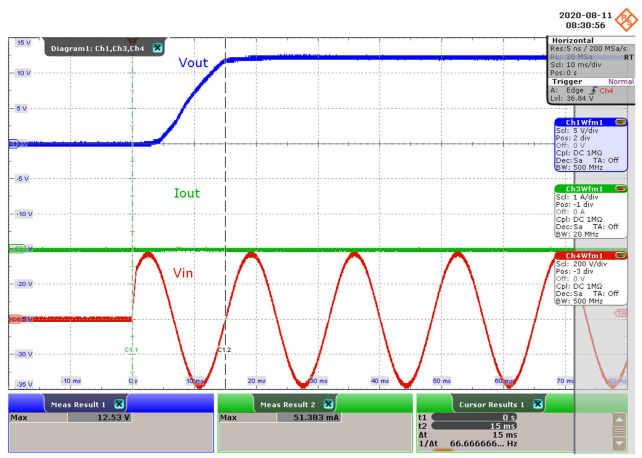

Figure 29 – 265 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 200 V / div., 10 ms / div.
On-Time Delay = 15 ms.
V_{MAX} = 12.53 V.

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10.2.2 CR Mode

10.2.2.1 100% Load

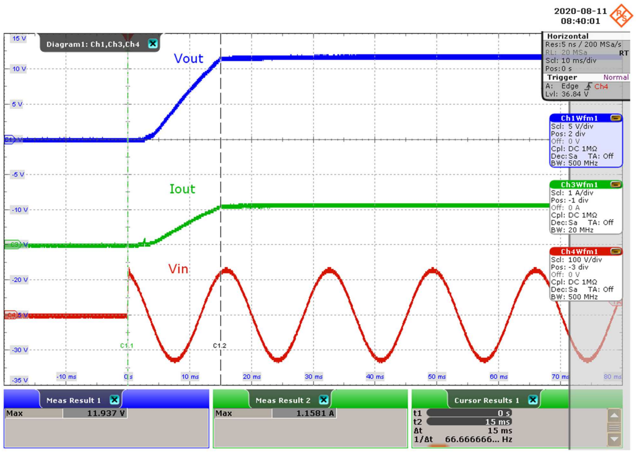

Figure 30 – 90 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 100 V / div., 10 ms / div.
On-Time Delay = 15 ms.
V_{MAX} = 11.94 V.

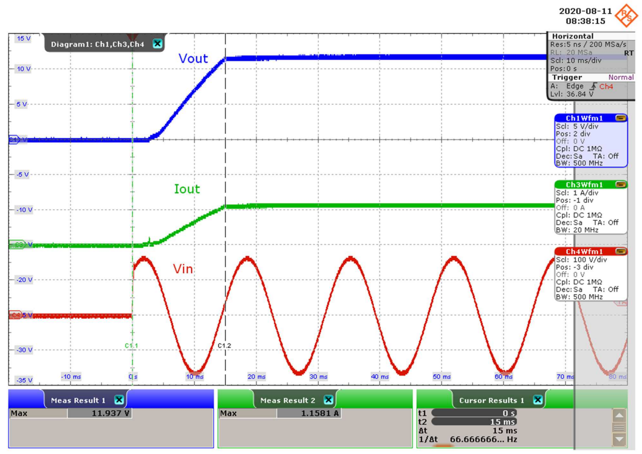

Figure 31 – 115 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 100 V / div., 10 ms / div.
On-Time Delay = 15 ms.
V_{MAX} = 11.94 V.

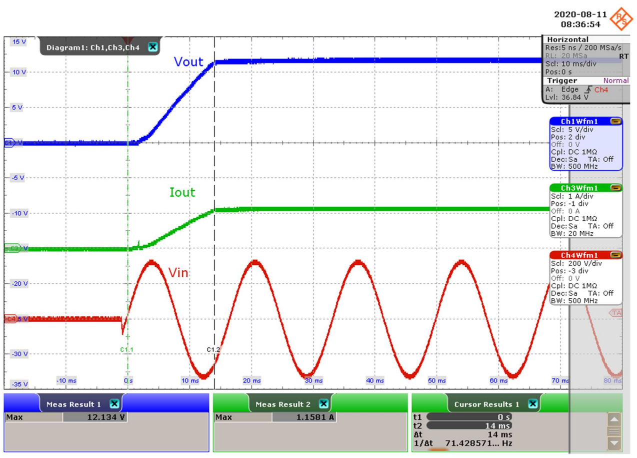

Figure 32 – 230 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 200 V / div., 10 ms / div.
On-Time Delay = 14 ms.
V_{MAX} = 12.13 V.

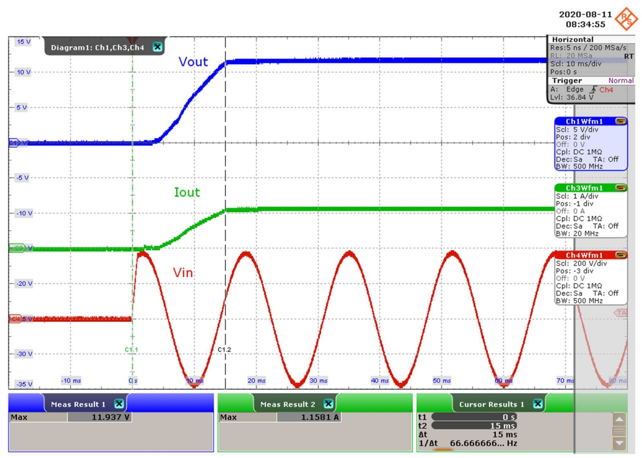

Figure 33 – 265 VAC.
CH1: V_{OUT}, 5 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
CH4: V_{IN}, 200 V / div., 10 ms / div.
On-Time Delay = 15 ms.
V_{MAX} = 11.94 V.

10.3 *Switching Waveforms*

10.3.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

10.3.1.1 100% Load

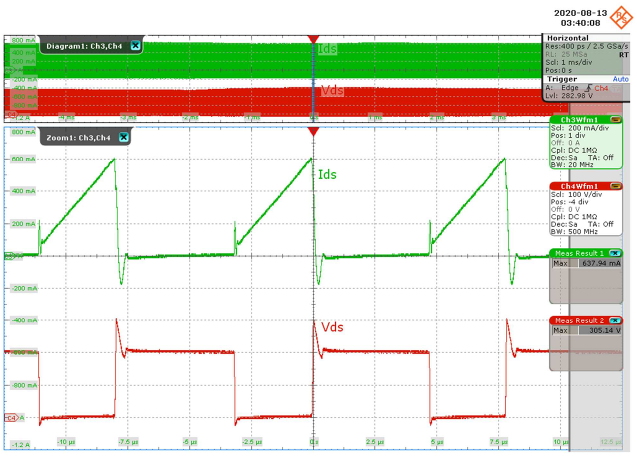

Figure 34 – 90 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 2.5 μs / div.
$V_{DS(MAX)}$ = 305.14 V, $I_{DS(MAX)}$ = 0.638 A.

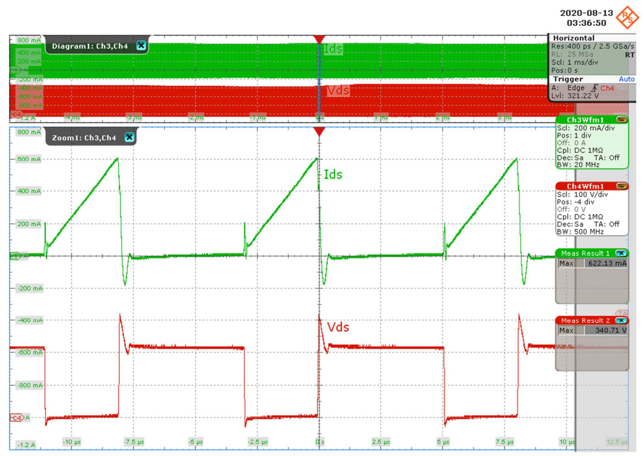

Figure 35 – 115 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 2.5 μs / div.
$V_{DS(MAX)}$ = 340.71 V, $I_{DS(MAX)}$ = 0.622 A.

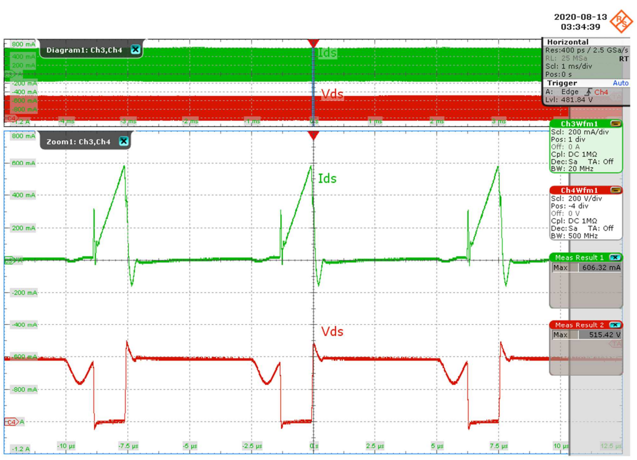

Figure 36 – 230 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 2.5 μs / div.
$V_{DS(MAX)}$ = 515.42 V, $I_{DS(MAX)}$ = 0.606 A.

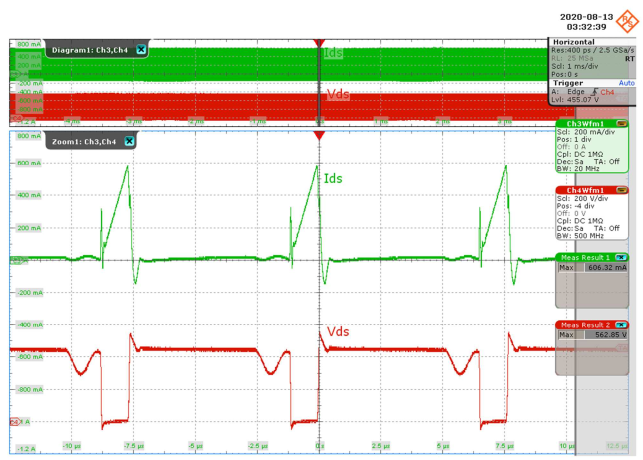

Figure 37 – 265 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 2.5 μs / div.
$V_{DS(MAX)}$ = 562.85 V, $I_{DS(MAX)}$ = 0.606 A.

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10.3.1.2 0% Load

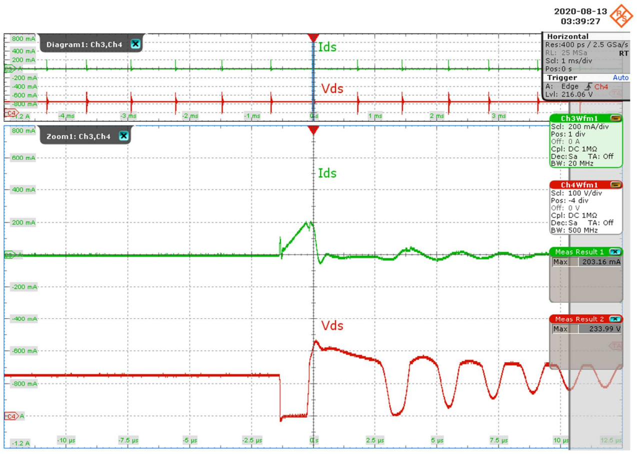

Figure 38 – 90 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
$V_{DS(MAX)}$ = 233.99 V, $I_{DS(MAX)}$ = 0.203 A.

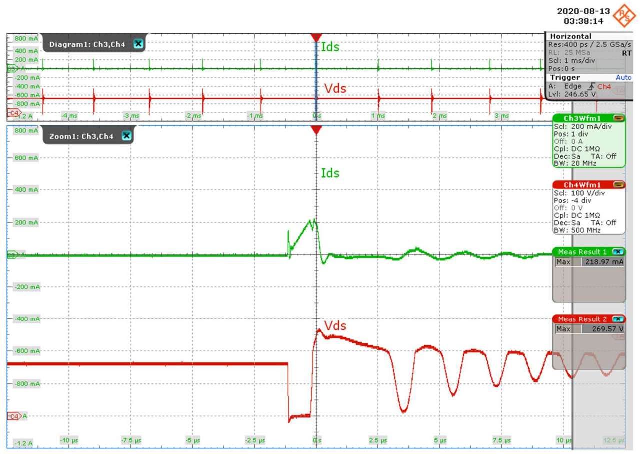

Figure 39 – 115 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
$V_{DS(MAX)}$ = 269.57 V, $I_{DS(MAX)}$ = 0.219 A.

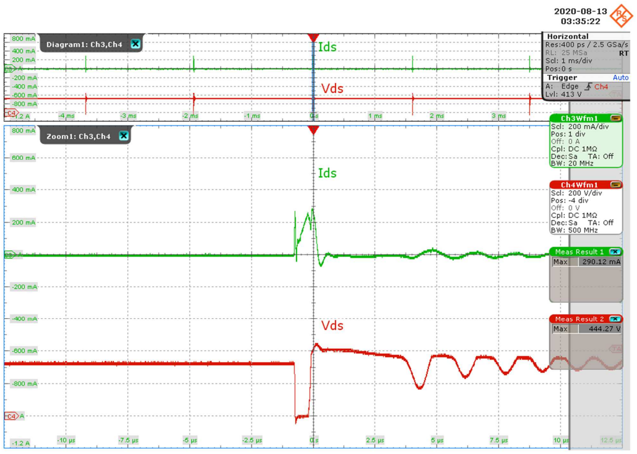

Figure 40 – 230 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
$V_{DS(MAX)}$ = 444.27 V, $I_{DS(MAX)}$ = 0.290 A.

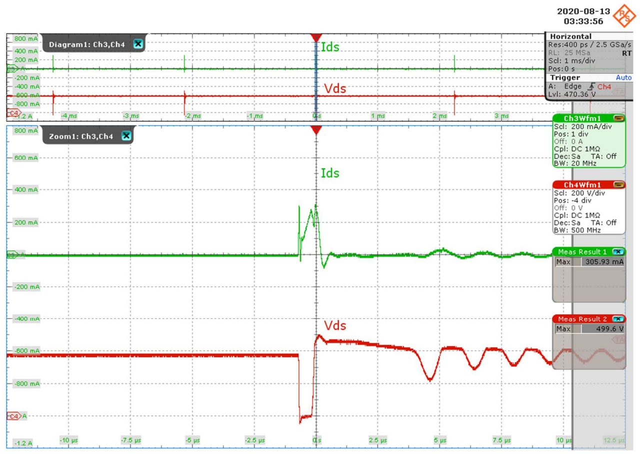

Figure 41 – 265 VAC.
CH3: I_{DS}, 200 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
$V_{DS(MAX)}$ = 499.60 V, $I_{DS(MAX)}$ = 0.306 A.

10.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

10.3.2.1 100% Load

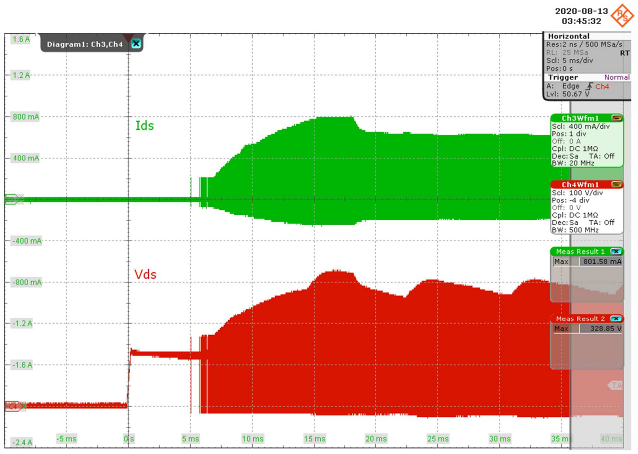

Figure 42 – 90 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 100 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 328.85 V, $I_{DS(MAX)}$ = 0.802 A.

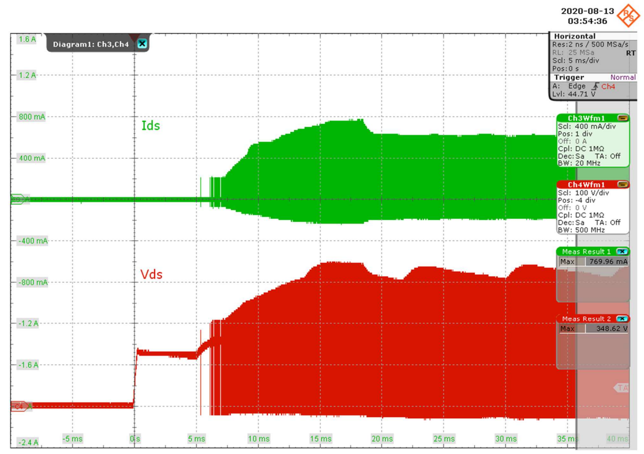

Figure 43 – 115 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 100 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 348.62 V, $I_{DS(MAX)}$ = 0.770 A.

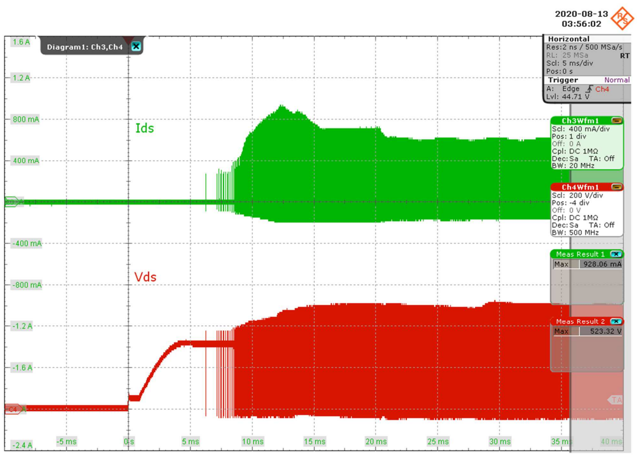

Figure 44 – 230 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 523.32 V, $I_{DS(MAX)}$ = 0.928 A.

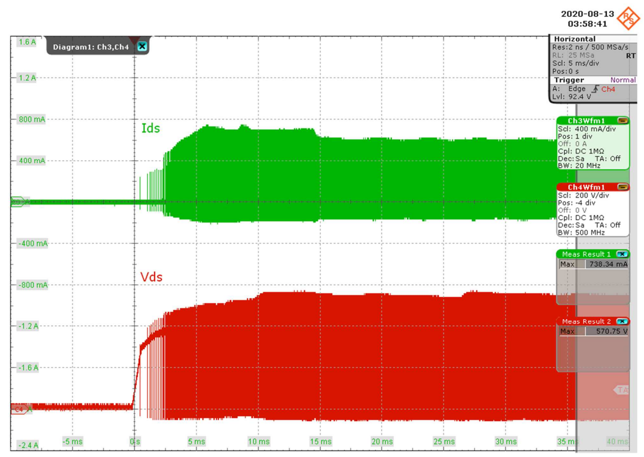

Figure 45 – 265 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 570.75 V, $I_{DS(MAX)}$ = 0.738 A.

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10.3.2.2 0% Load

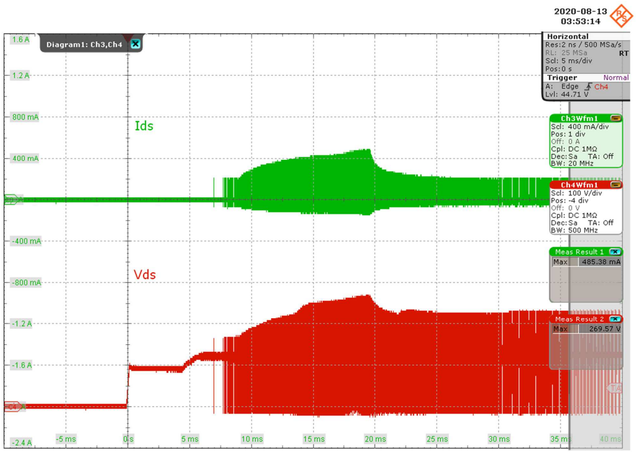

Figure 46 – 90 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 100 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 269.57 V, $I_{DS(MAX)}$ = 0.485 A.

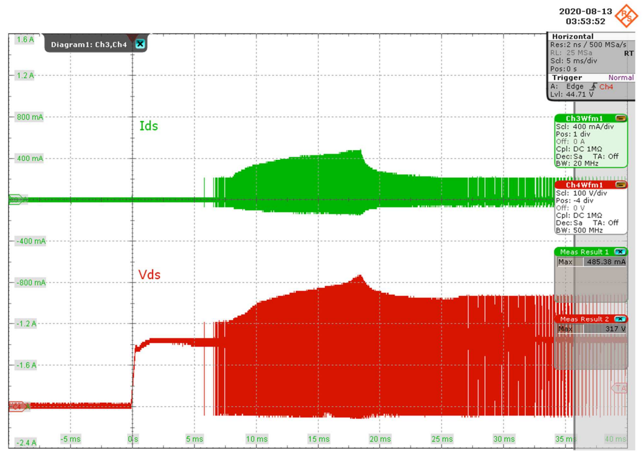

Figure 47 – 115 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 100 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 317.00 V, $I_{DS(MAX)}$ = 0.485 A.

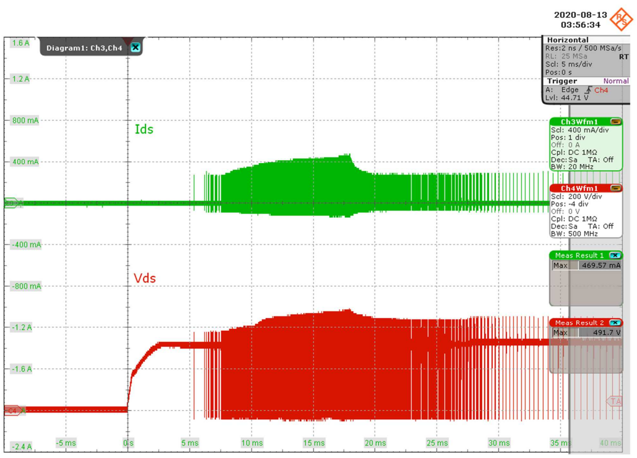

Figure 48 – 230 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 491.70 V, $I_{DS(MAX)}$ = 0.470 A.

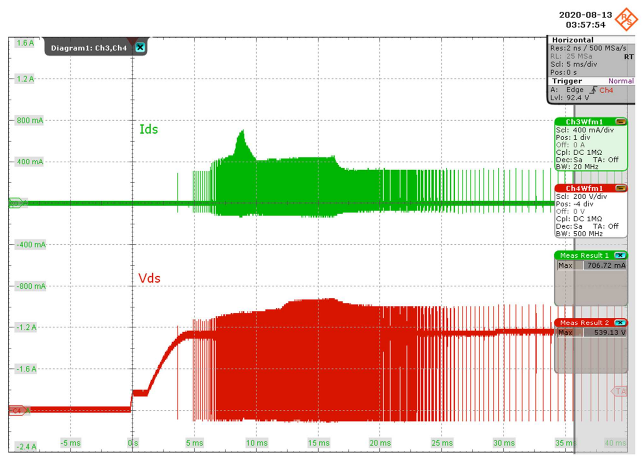

Figure 49 – 265 VAC.
CH3: I_{DS}, 400 mA / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
$V_{DS(MAX)}$ = 539.13 V, $I_{DS(MAX)}$ = 0.707 A.

10.3.3 Freewheeling Diode Voltage

10.3.3.1 100% Load

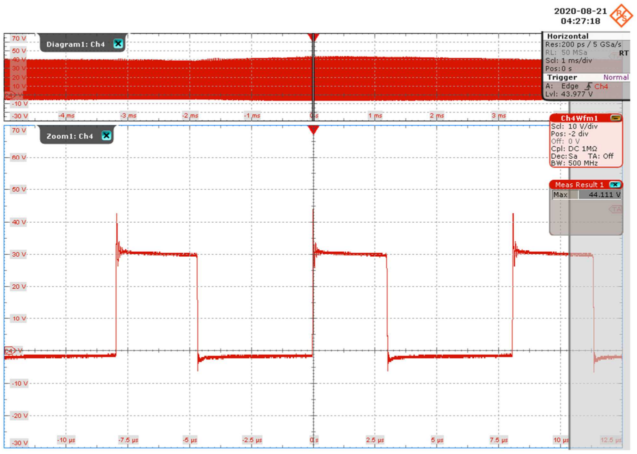

Figure 50 – 90 VAC.
CH4: V_D, 10 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 44.11 V.

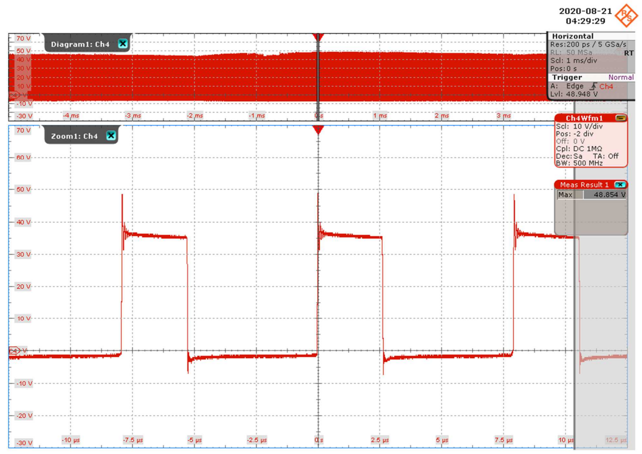

Figure 51 – 115 VAC.
CH4: V_D, 10 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 48.85 V.

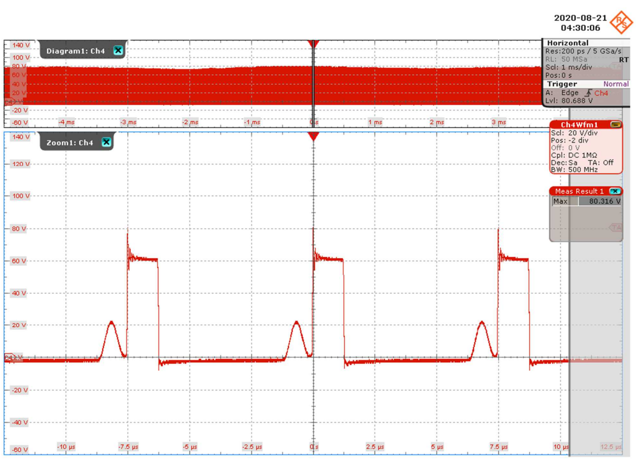

Figure 52 – 230 VAC.
CH4: V_D, 20 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 80.31 V.

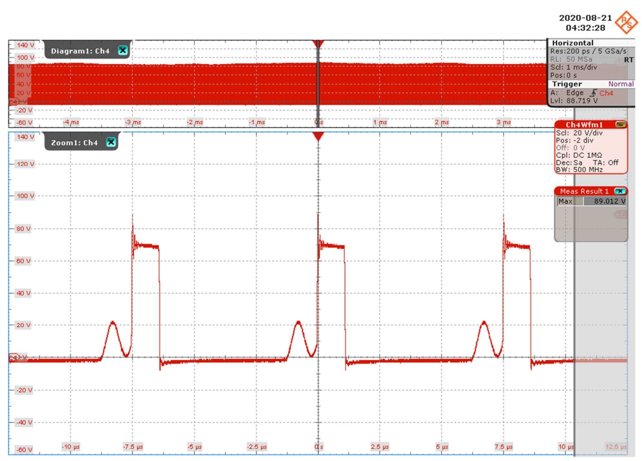

Figure 53 – 265 VAC.
CH4: V_D, 20 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 89.01 V.

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10.3.3.2 0% Load

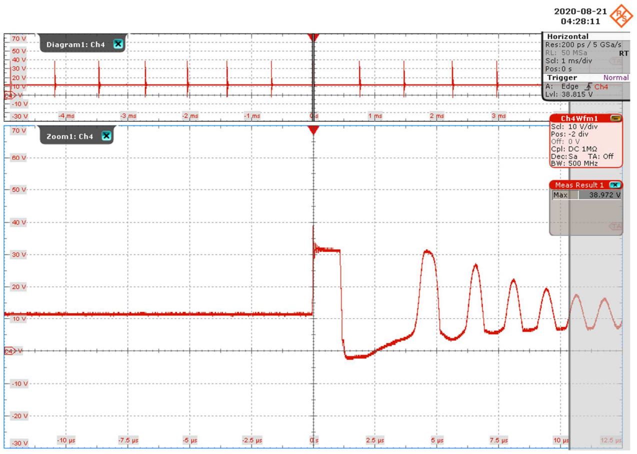

Figure 54 – 90 VAC.
CH4: V_D, 10 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 38.97 V.

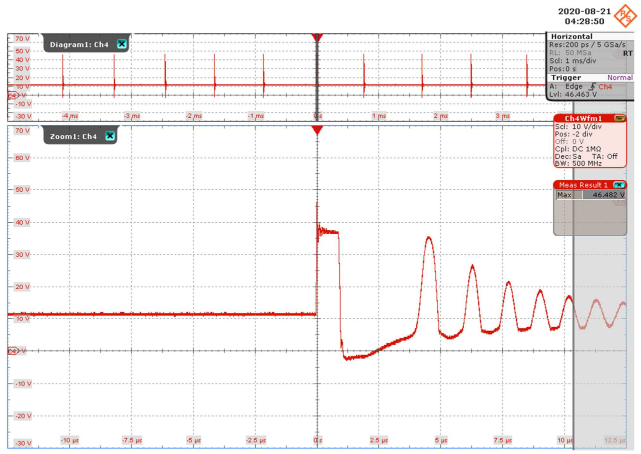

Figure 55 – 115 VAC.
CH4: V_D, 10 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 46.48 V.

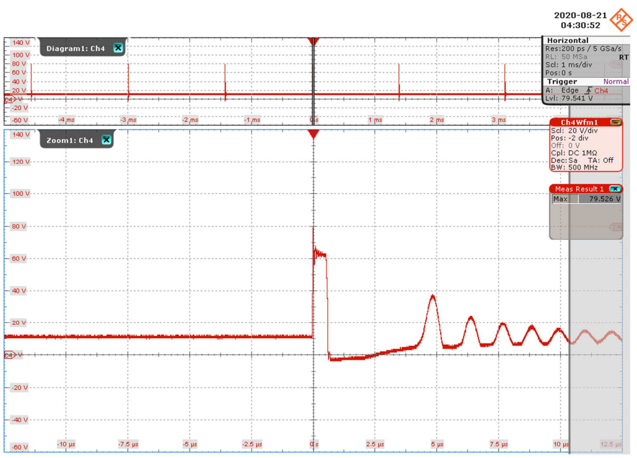

Figure 56 – 230 VAC.
CH4: V_D, 20 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 79.53 V.

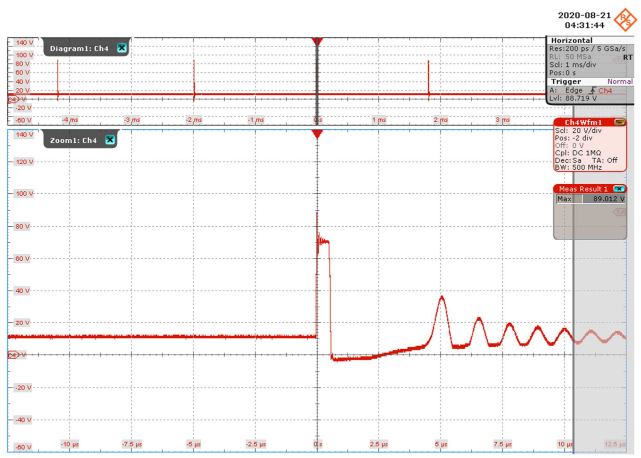

Figure 57 – 265 VAC.
CH4: V_D, 20 V / div., 1 ms / div.
Zoom: 2.5 µs / div.
PIV = 89.01 V.

10.3.4 Freewheeling Diode Voltage at Start-up

10.3.4.1 100% Load

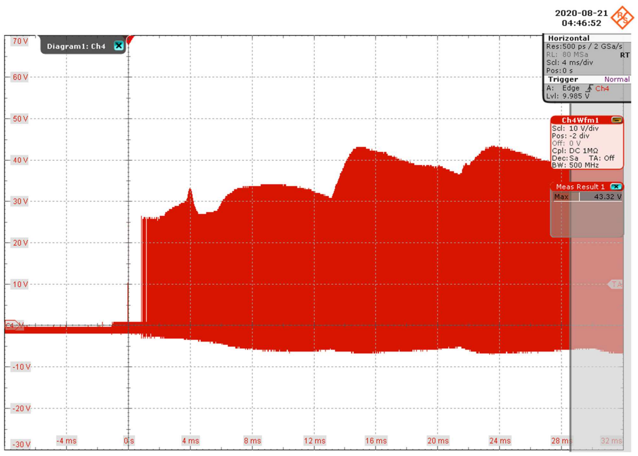

Figure 58 – 90 VAC.
CH4: V_D, 10 V / div., 4 ms / div.
PIV = 43.32 V.

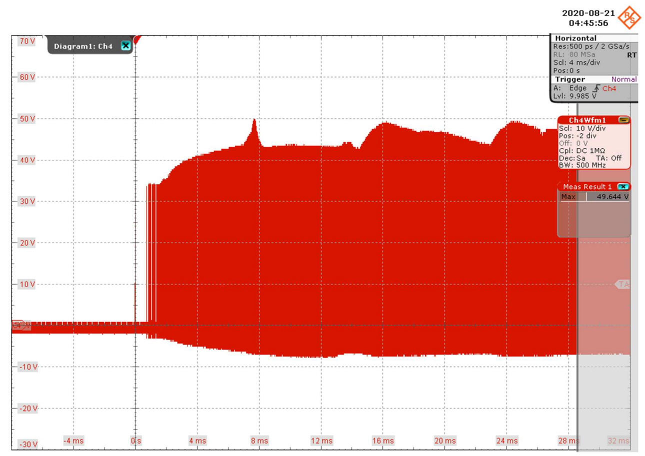

Figure 59 – 115 VAC.
CH4: V_D, 10 V / div., 4 ms / div.
PIV = 49.64 V.

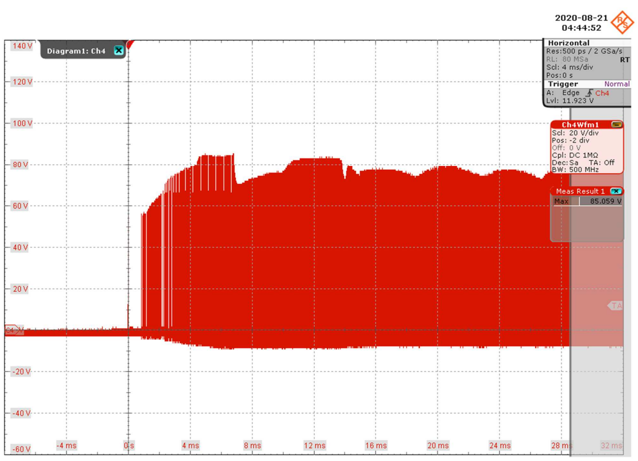

Figure 60 – 230 VAC.
CH4: V_D, 20 V / div., 4 ms / div.
PIV = 85.06 V.

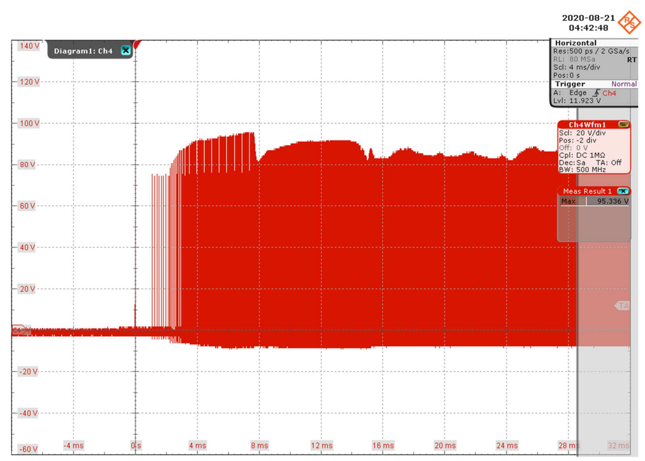

Figure 61 – 265 VAC.
CH4: V_D, 20 V / div., 4 ms / div.
PIV = 95.34 V.

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10.3.4.2 0% Load

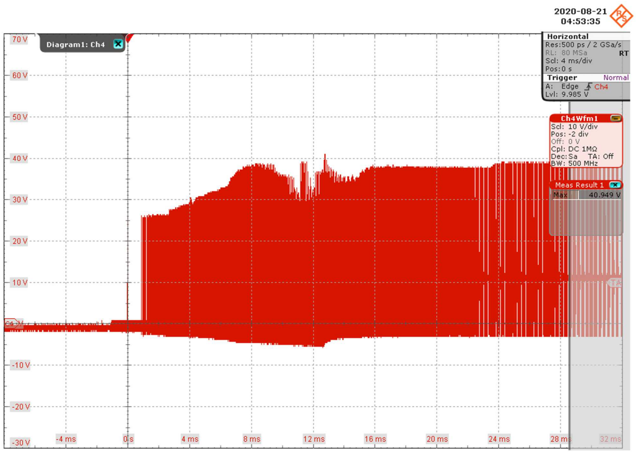

Figure 62 – 90 VAC.
CH4: V_D, 10 V / div., 4 ms / div.
PIV = 40.95 V.

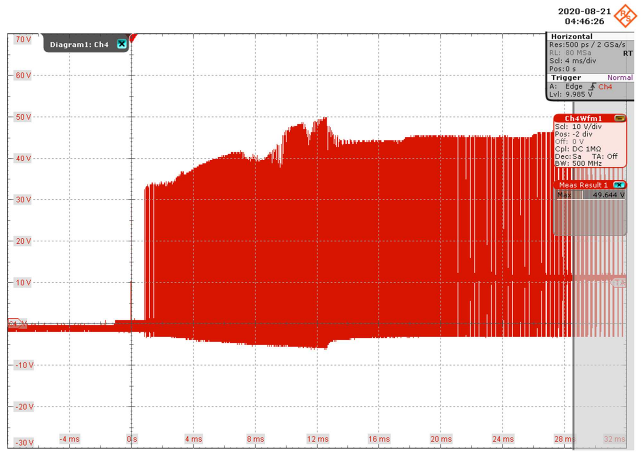

Figure 63 – 115 VAC.
CH4: V_D, 10 V / div., 4 ms / div.
PIV = 49.64 V.

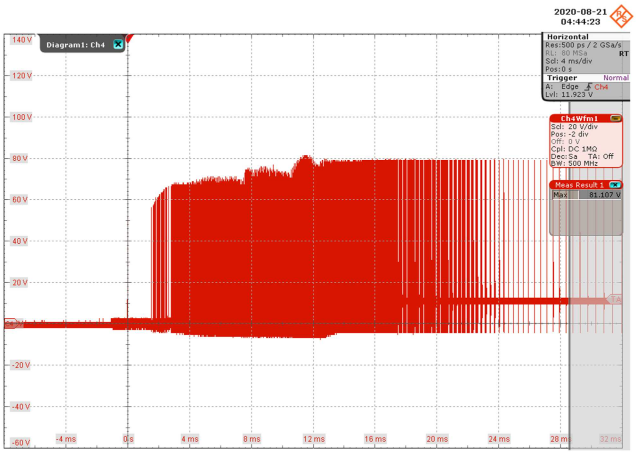

Figure 64 – 230 VAC.
CH4: V_D, 20 V / div., 4 ms / div.
PIV = 81.11 V.

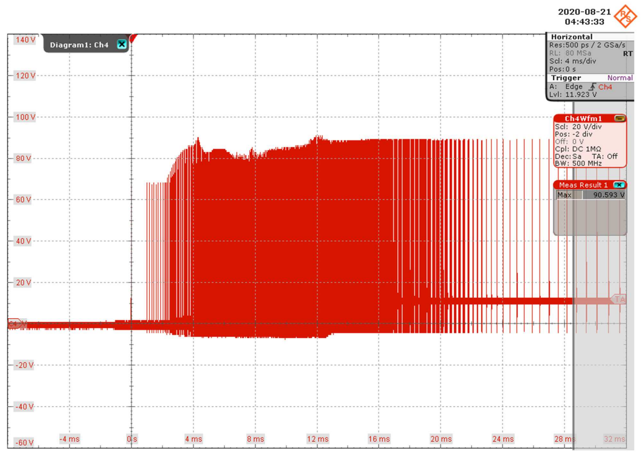

Figure 65 – 265 VAC.
CH4: V_D, 20 V / div., 4 ms / div.
PIV = 90.59 V.

10.4 ***Fault Conditions***

10.4.1 Output Overvoltage

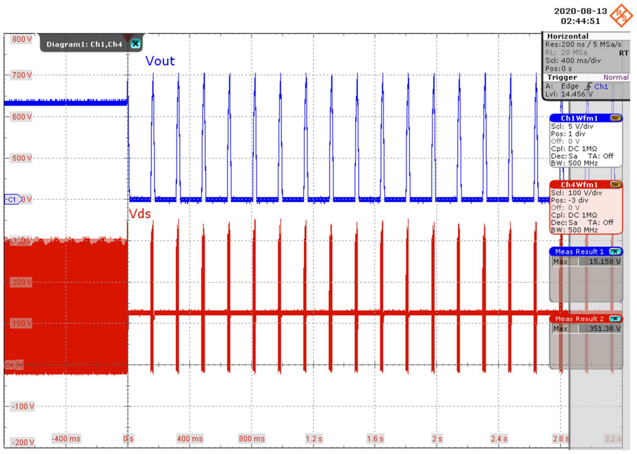

Figure 66 – 90 VAC, Full Load.
CH1: V_{OUT}, 5 V / div., 400 ms / div.
CH4: V_{DS}, 100 V / div., 400 ms / div.
$V_{DS(MAX)}$ = 351.38 V.
$V_{O(MAX)}$ = 15.16 V.

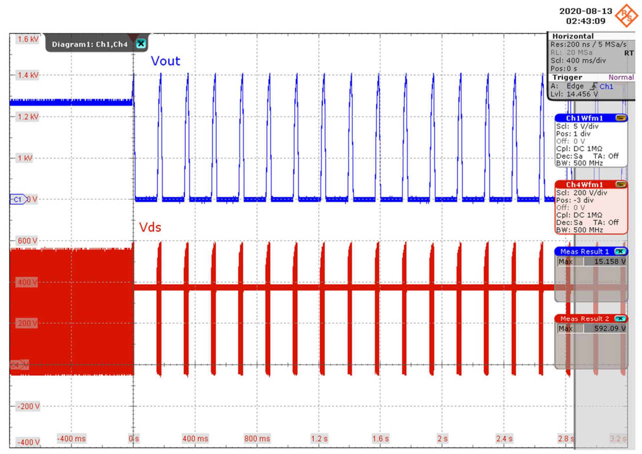

Figure 67 – 265 VAC, Full Load.
CH1: V_{OUT}, 5 V / div., 400 ms / div.
CH4: V_{DS}, 200 V / div., 400 ms / div.
$V_{DS(MAX)}$ = 592.09 V.
$V_{O(MAX)}$ = 15.16 V.

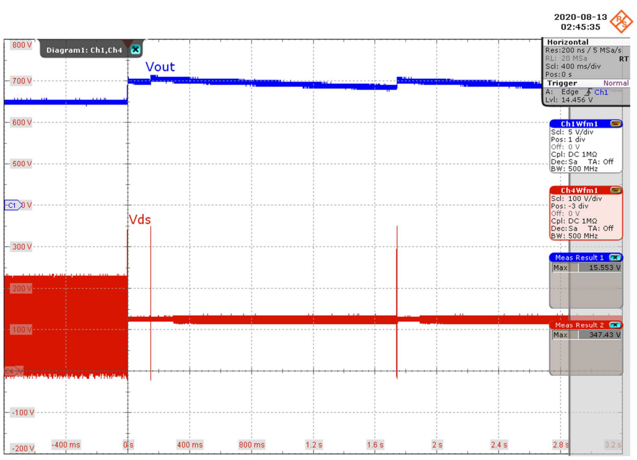

Figure 68 – 90 VAC, No-Load.
CH1: V_{OUT}, 5 V / div., 400 ms / div.
CH4: V_{DS}, 100 V / div., 400 ms / div.
$V_{DS(MAX)}$ = 347.43 V.
$V_{O(MAX)}$ = 15.55 V.

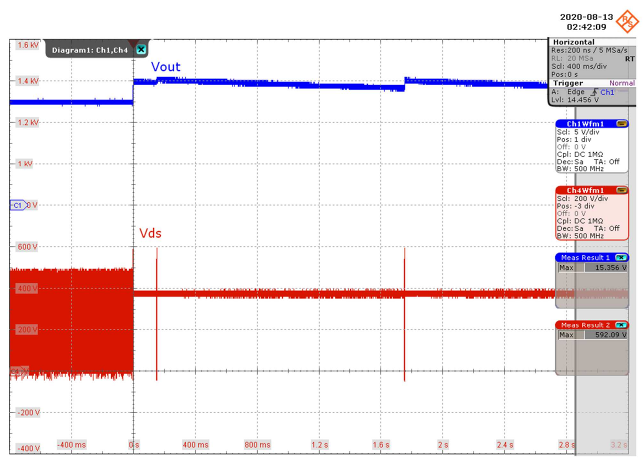

Figure 69 – 265 VAC, No-Load.
CH1: V_{OUT}, 5 V / div., 400 ms / div.
CH4: V_{DS}, 200 V / div., 400 ms / div.
$V_{DS(MAX)}$ = 592.09 V.
$V_{O(MAX)}$ = 15.36 V.

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10.4.2 Output Short-Circuit

Test Condition: Short circuit applied at startup

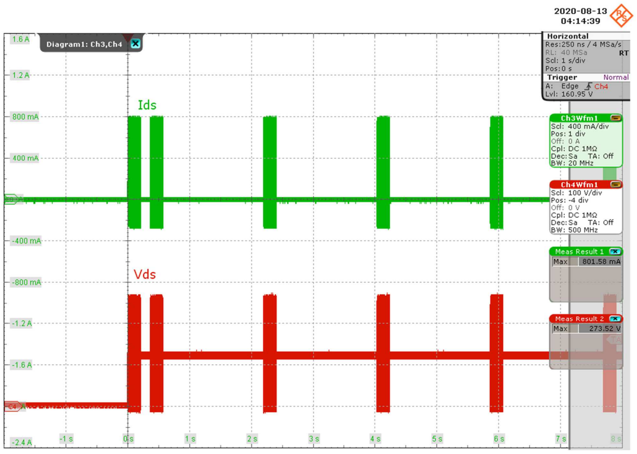

Figure 70 – 90 VAC.
CH3: $I_{DS,}$ 400 mA / div., 1 s / div.
CH4: V_{DS}, 100 V / div., 1 s / div.
$V_{DS(MAX)}$ = 273.52 V.
$I_{DS(MAX)}$ = 0.802 A.

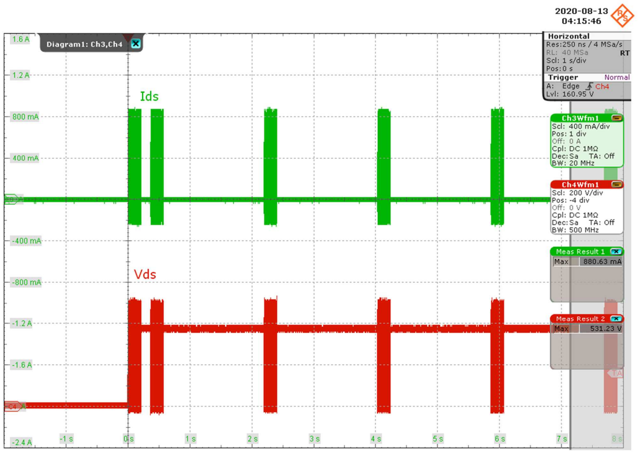

Figure 71 – 265 VAC.
CH3: $I_{DS,}$ 400 mA / div., 1 s / div.
CH4: V_{DS}, 200 V / div., 1 s / div.
$V_{DS(MAX)}$ = 531.23 V.
$I_{DS(MAX)}$ = 0.881 A.

10.5 ***Output Voltage Ripple***

10.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

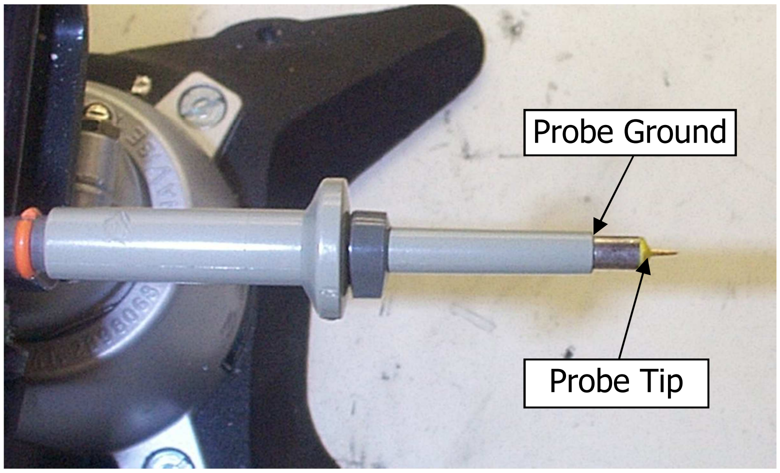

Figure 72 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

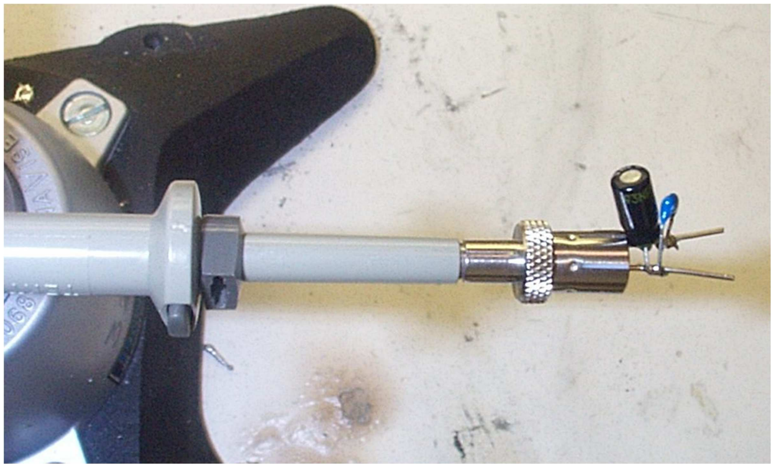

Figure 73 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

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10.5.2 Measurement Results

Note: All ripple measurements were taken at the PCB output terminals.

10.5.2.1 100% Load Condition

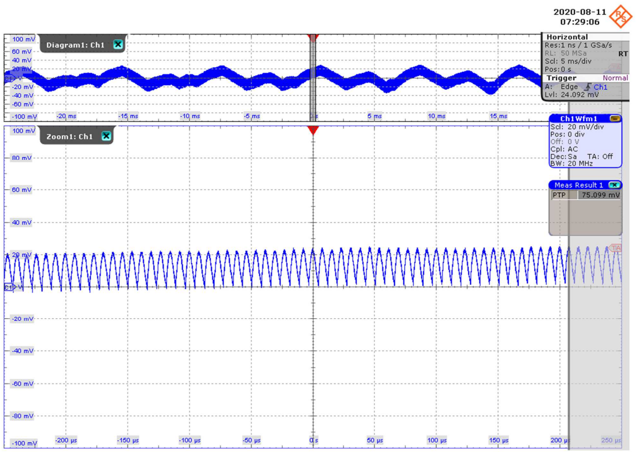

Figure 74 – 90 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 75.10 mV.

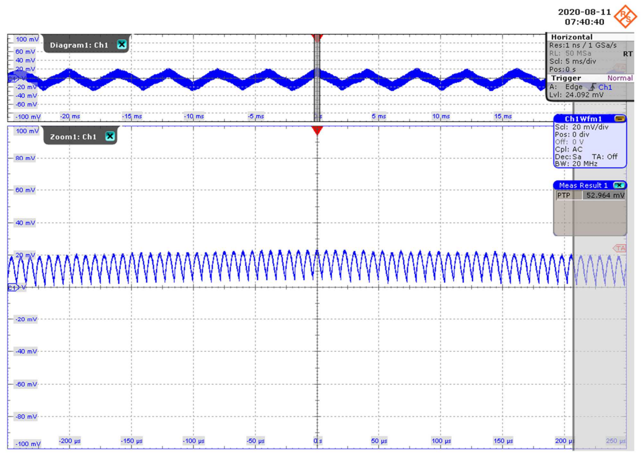

Figure 75 – 115 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 52.96 mV.

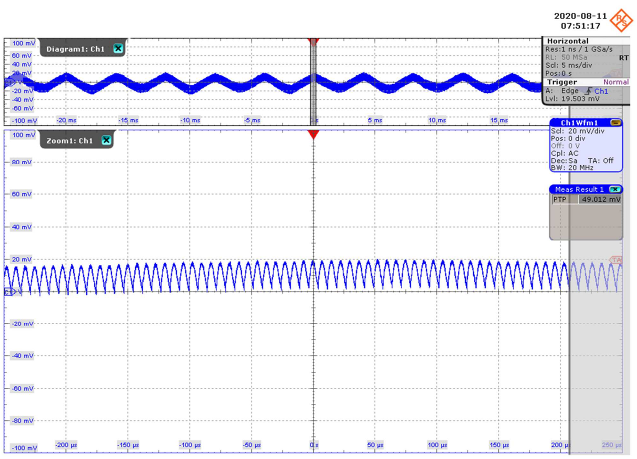

Figure 76 – 230 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 49.01 mV.

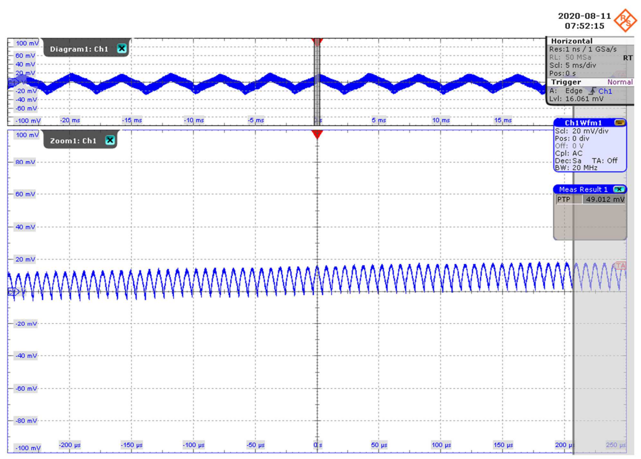

Figure 77 – 265 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 49.01 mV.

10.5.2.2 75% Load Condition

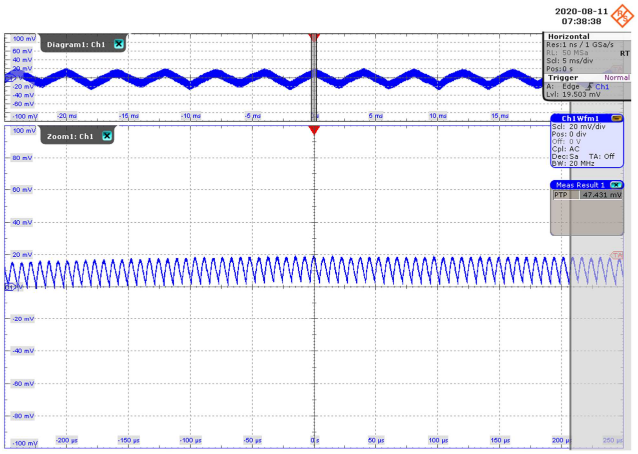

Figure 78 – 90 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 47.43 mV.

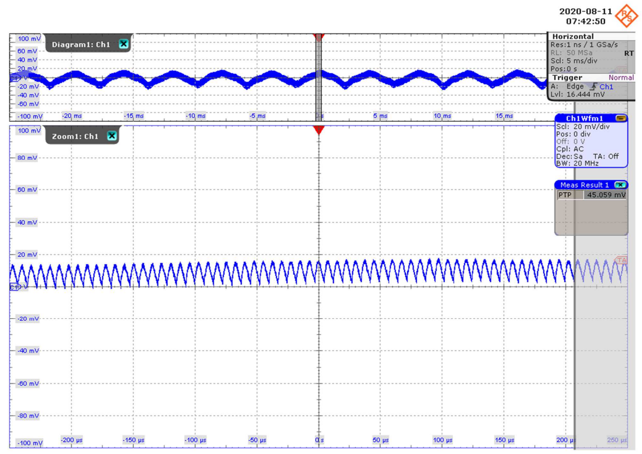

Figure 79 – 115 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 45.06 mV.

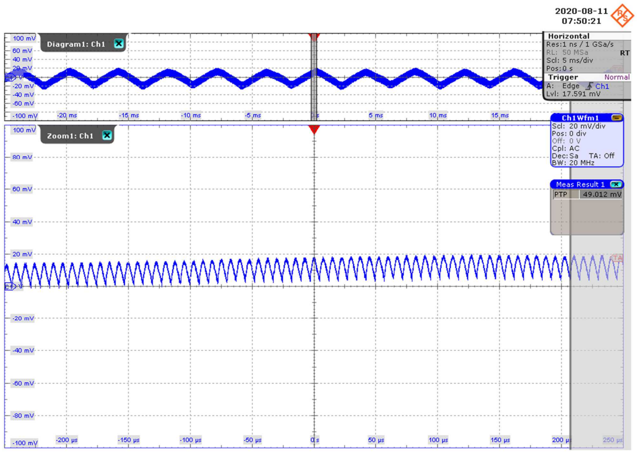

Figure 80 – 230 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 49.01 mV.

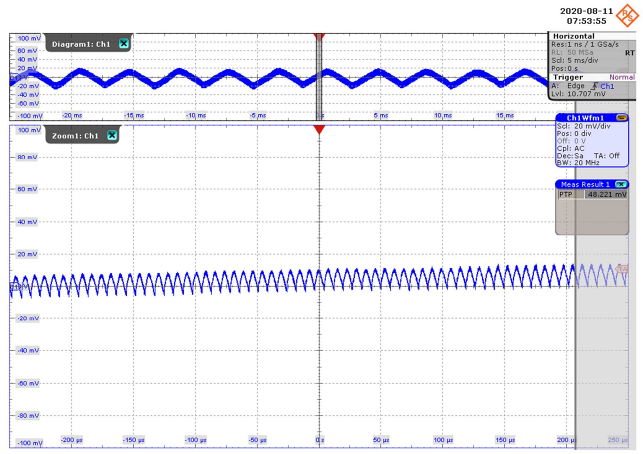

Figure 81 – 265 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 48.22 mV.

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10.5.2.3 50% Load Condition

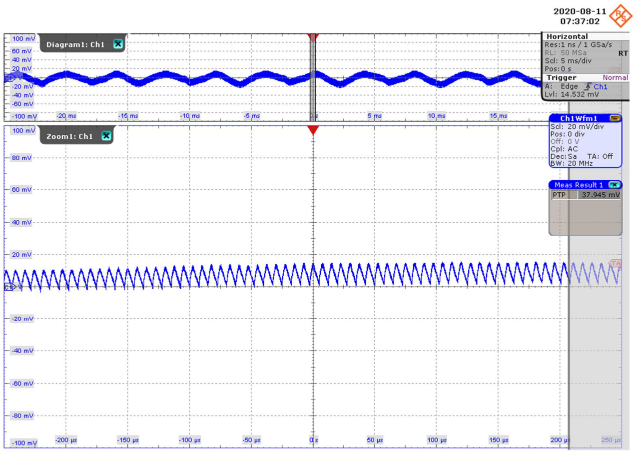

Figure 82 – 90 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 37.95 mV.

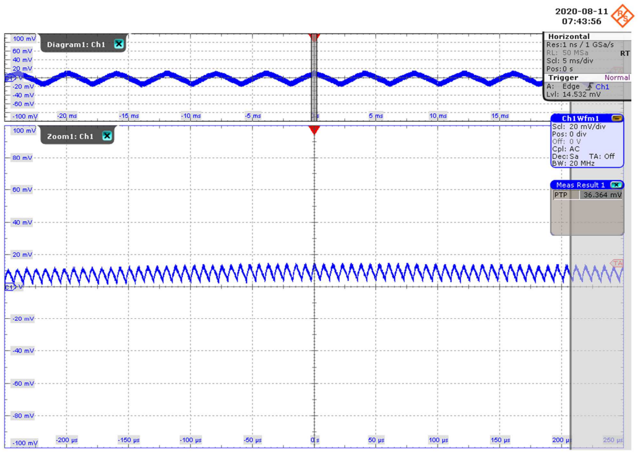

Figure 83 – 115 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 36.36 mV.

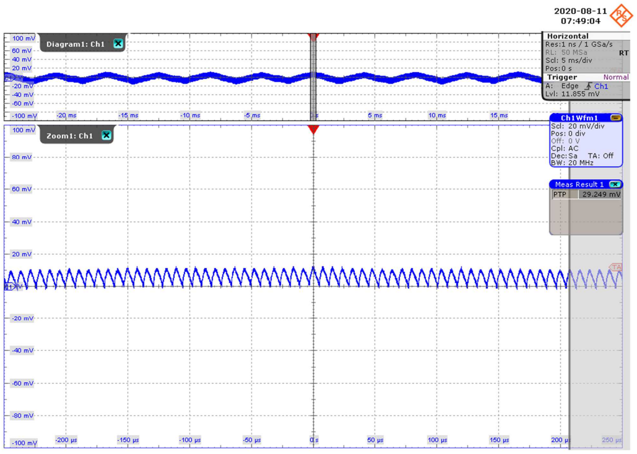

Figure 84 – 230 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 29.25 mV.

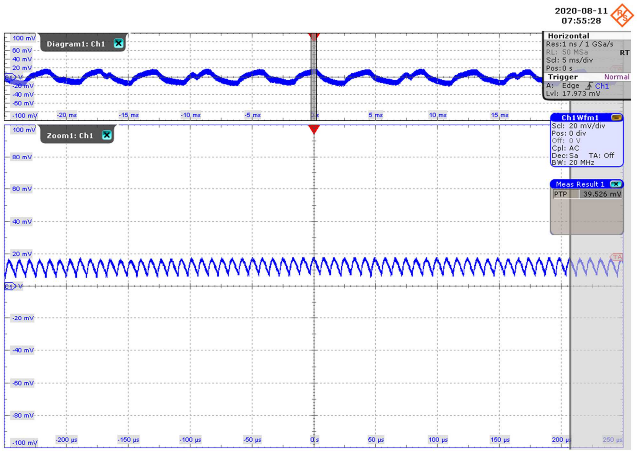

Figure 85 – 265 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 39.53 mV.

10.5.2.4 25% Load Condition

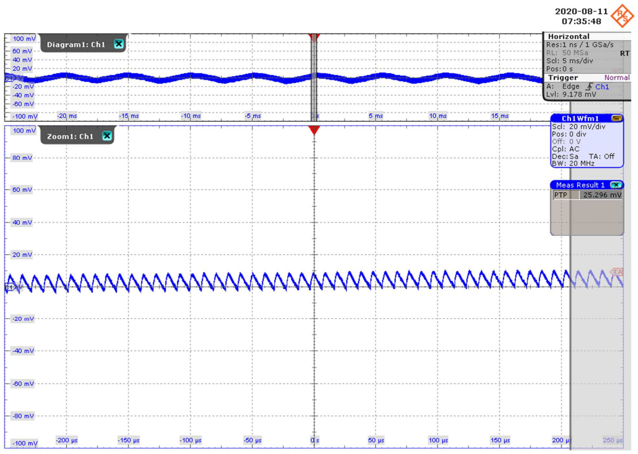

Figure 86 – 90 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 25.30 mV.

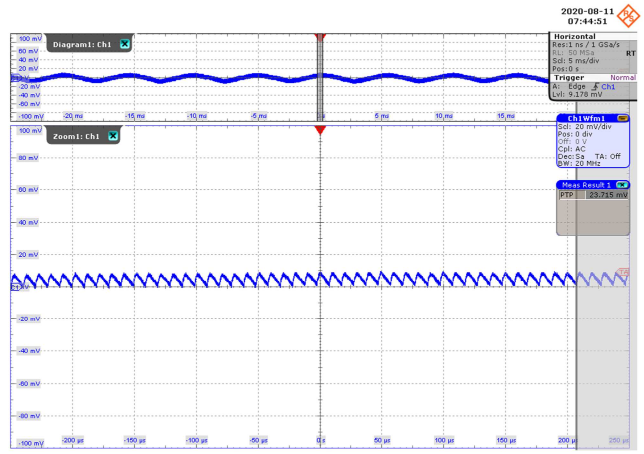

Figure 87 – 115 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 23.72 mV.

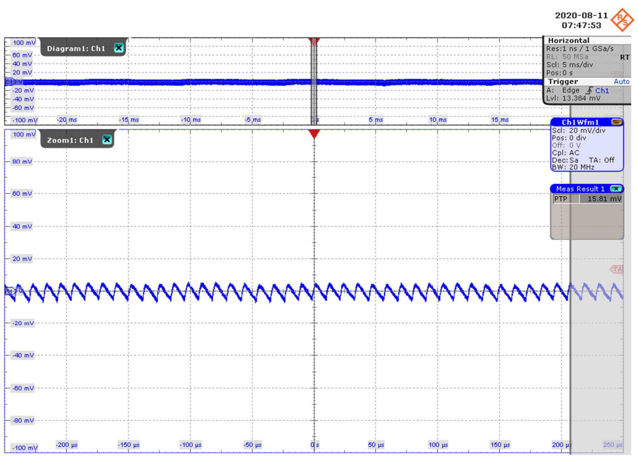

Figure 88 – 230 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 15.81 mV.

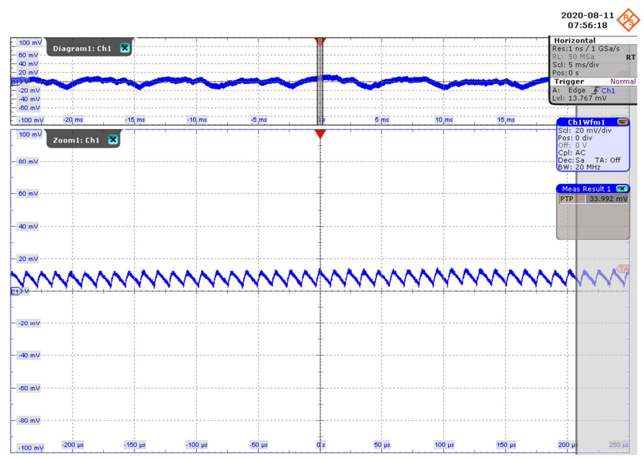

Figure 89 – 265 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 33.99 mV.

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10.5.2.5 0% Load Condition

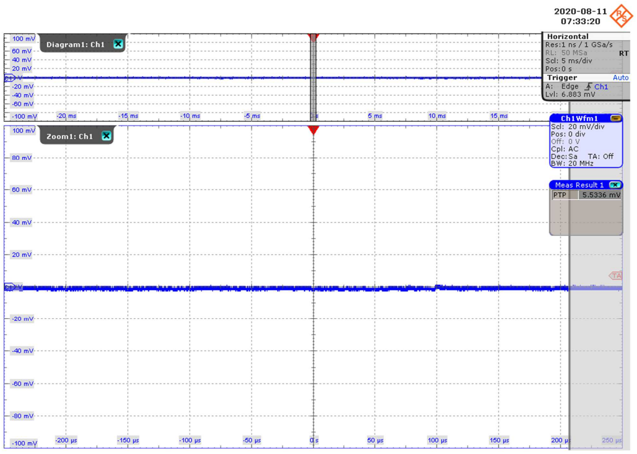

Figure 90 – 90 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 5.53 mV.

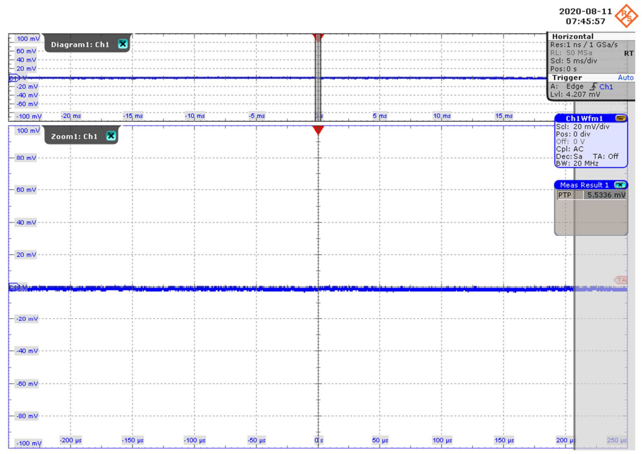

Figure 91 – 115 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 5.53 mV.

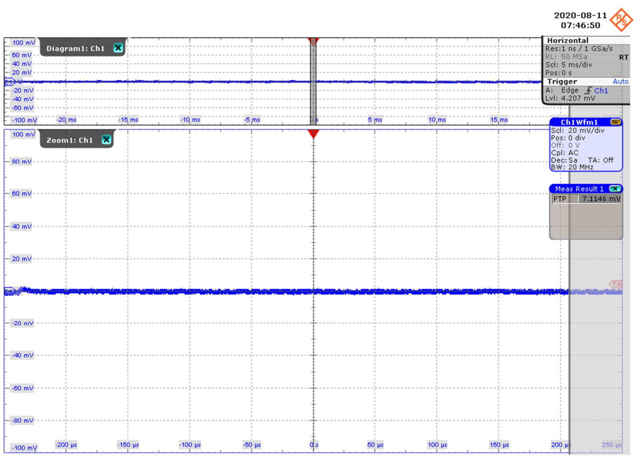

Figure 92 – 230 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 7.11 mV.

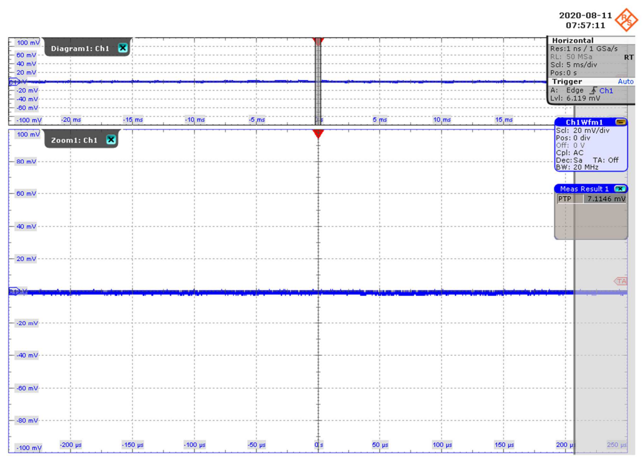

Figure 93 – 265 VAC.
CH2: V_{OUT}, 20 mV / div., 5 ms / div.
Zoom: 50 µs / div.
Output Ripple = 7.11 mV.

10.5.3 Output Ripple Voltage Graph from 0% - 100%

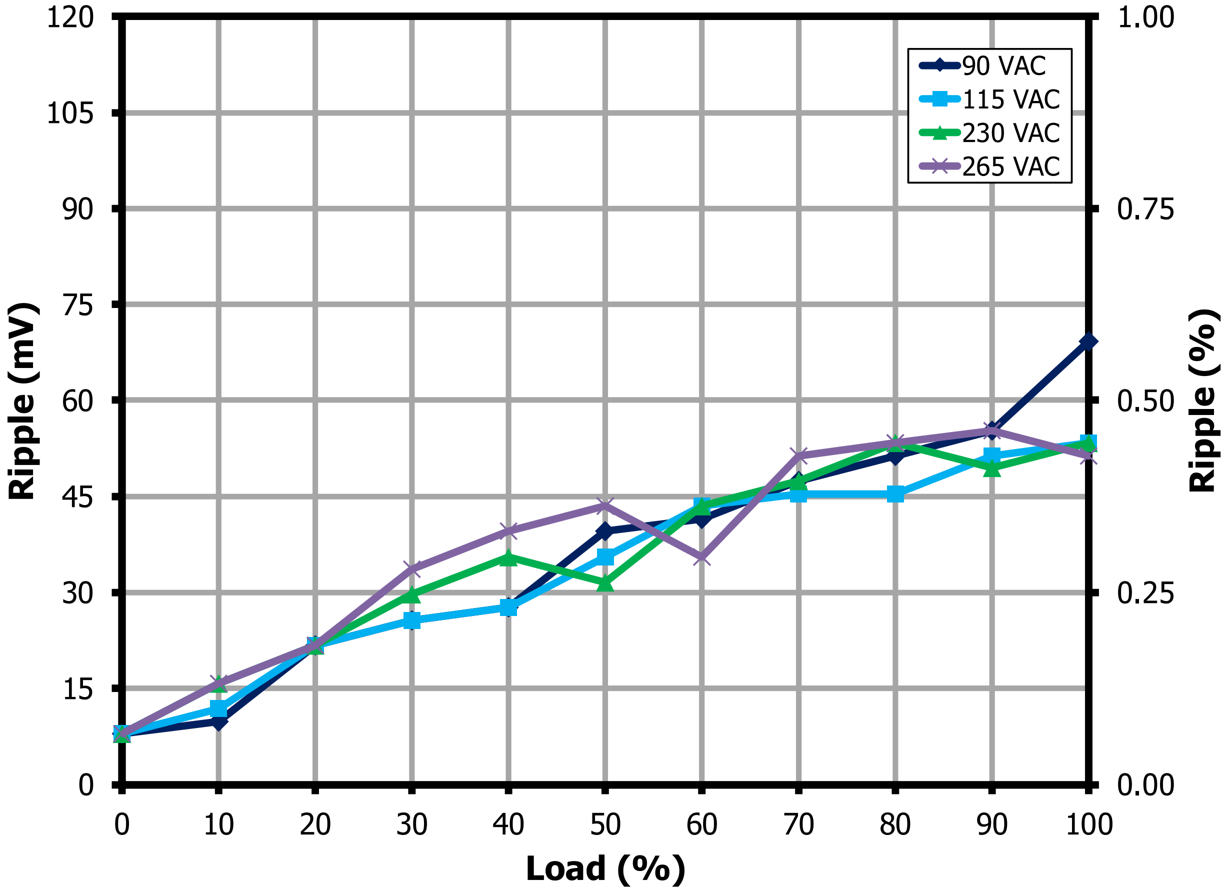

Figure 94 – Measured at the PCB Output Terminals, Room Temperature.

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11 Thermal Performance

11.1 *Thermal Performance at Room Temperature*

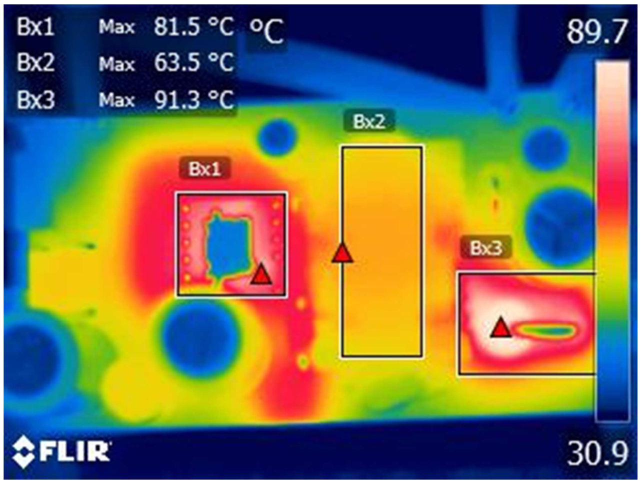

Figure 95 – 90 VAC, Full Load, Top.
Bx1: LNK6774V, 81.5 °C.
Bx2: Transformer, 63.5 °C.
Bx3: Flyback Diode, 91.3 °C.

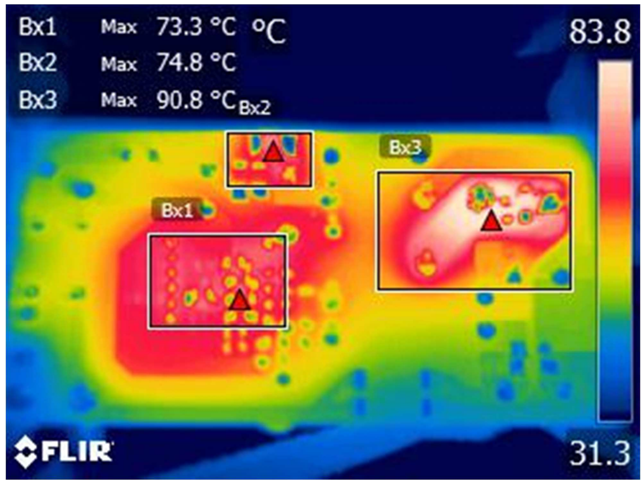

Figure 96 – 90 VAC, Full Load, Bottom.
Bx1: LNK6774V GND Trace, 73.3 °C.
Bx2: Snubber Damping Resistor, 74.8 °C.
Bx3: Flyback Diode Trace, 90.8 °C.

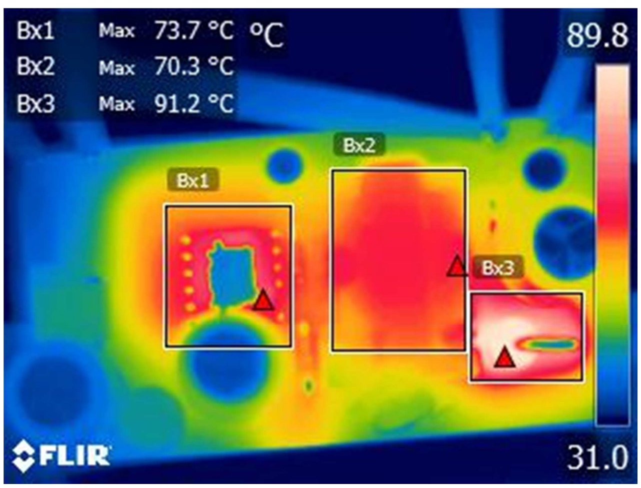

Figure 97 – 265 VAC, Full Load, Top.
Bx1: LNK6774V, 73.7 °C.
Bx2: Transformer, 70.3 °C.
Bx3: Flyback Diode, 91.2 °C.

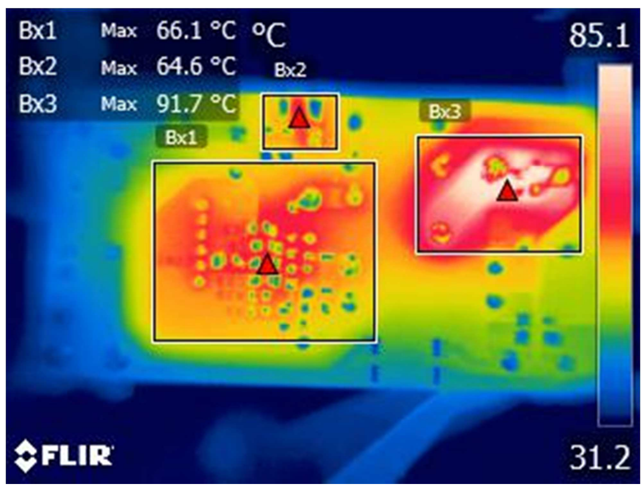

Figure 98 – 265 VAC, Full Load, Bottom.
Bx1: LNK6774V GND Trace, 66.1 °C.
Bx2: Snubber Damping Resistor, 64.6 °C.
Bx3: Flyback Diode Trace, 91.7 °C.

11.2 *Thermal Performance at 50 °C*

11.2.1 90 VAC at 50 °C

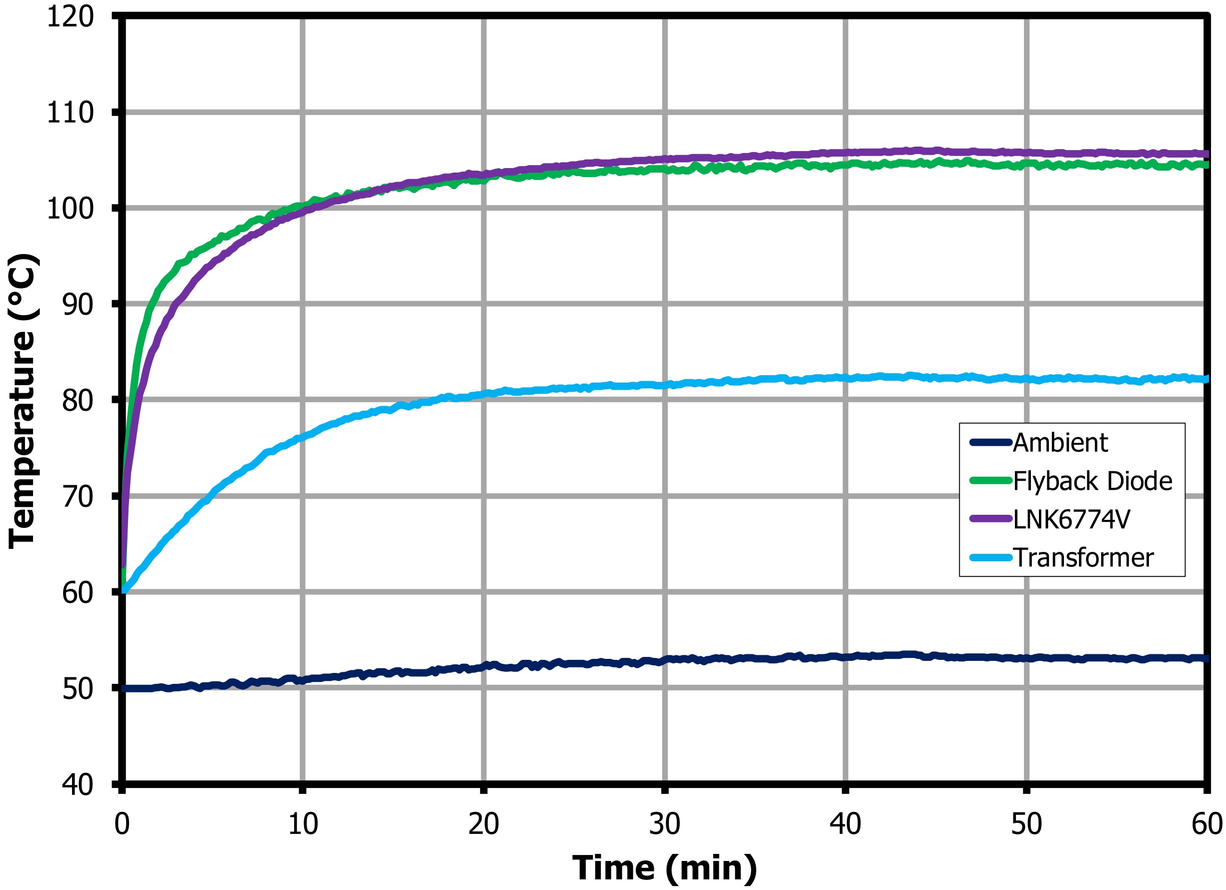

Figure 99 – Thermal Performance at 90 VAC, Full Load.

Component	Temperature (°C)
Ambient	53.0
Flyback Diode	104.6
LNK6774V	105.6
Transformer	82.2

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11.2.2 265 VAC at 50 °C

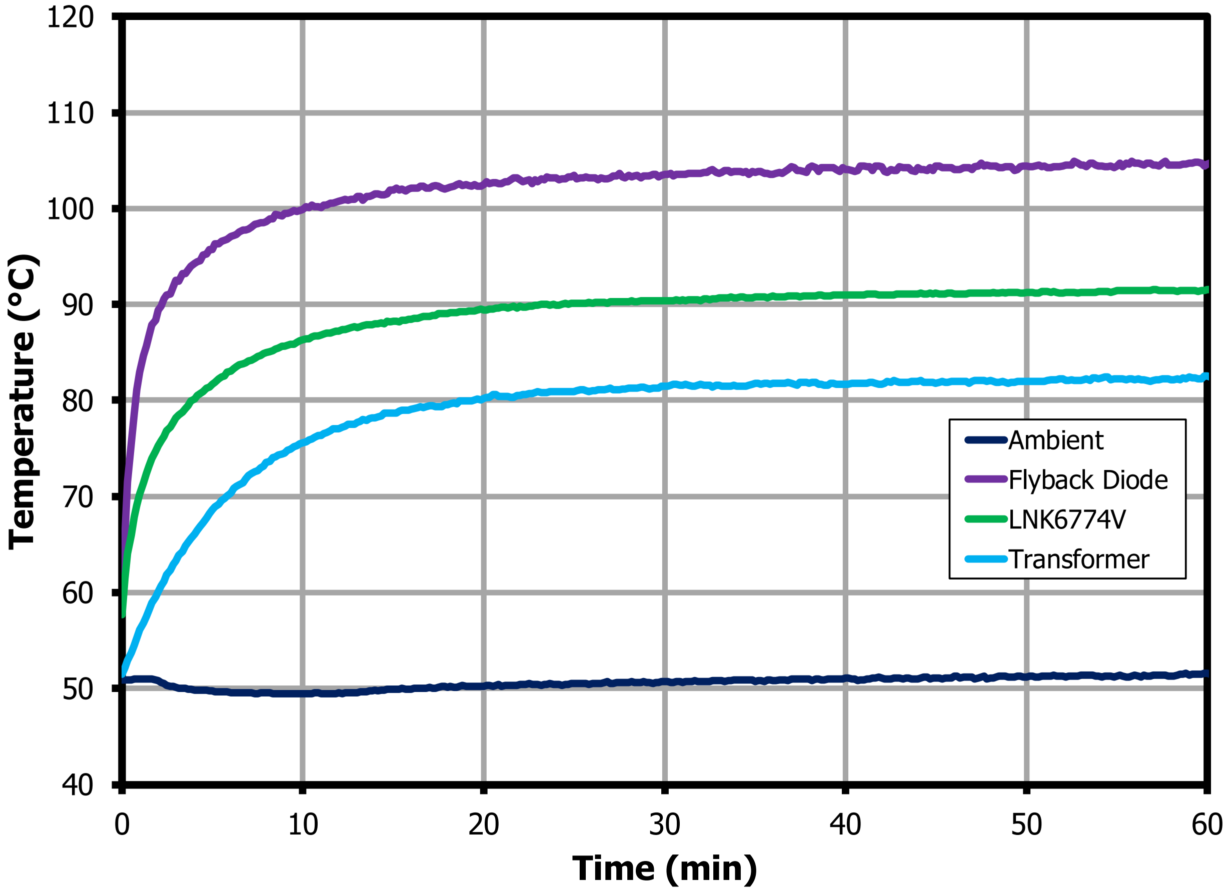
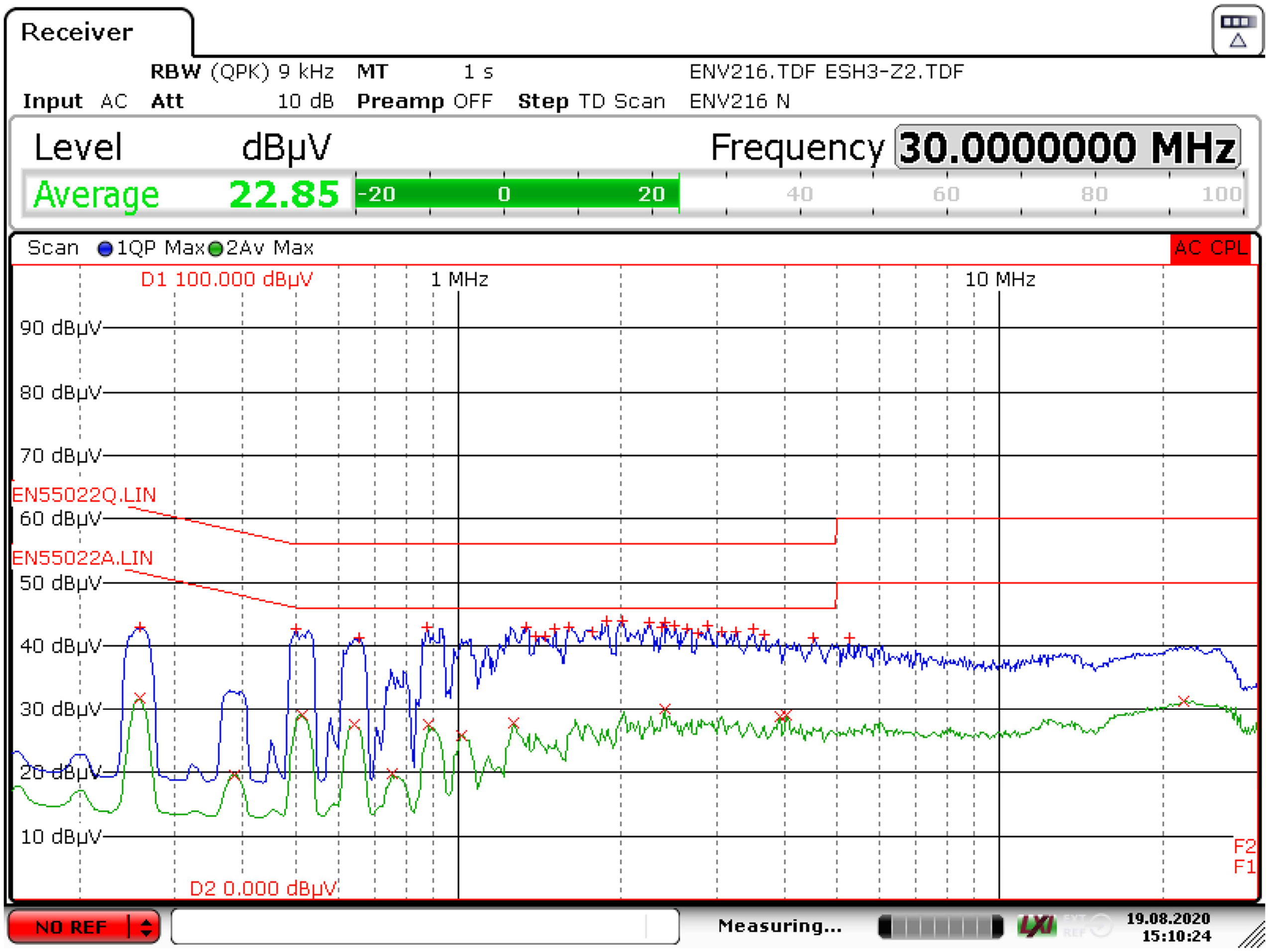


Figure 100 – Thermal Performance at 265 VAC, Full Load.

Component	Temperature (°C)
Ambient	51.6
Flyback Diode	104.6
LNK6774V	91.7
Transformer	82.3

12 Conducted EMI

12.1 *115 VAC 1.25 A Resistive Load*



Date: 19.AUG.2020 15:10:24

Figure 101 – Floating Ground EMI at 115 VAC.

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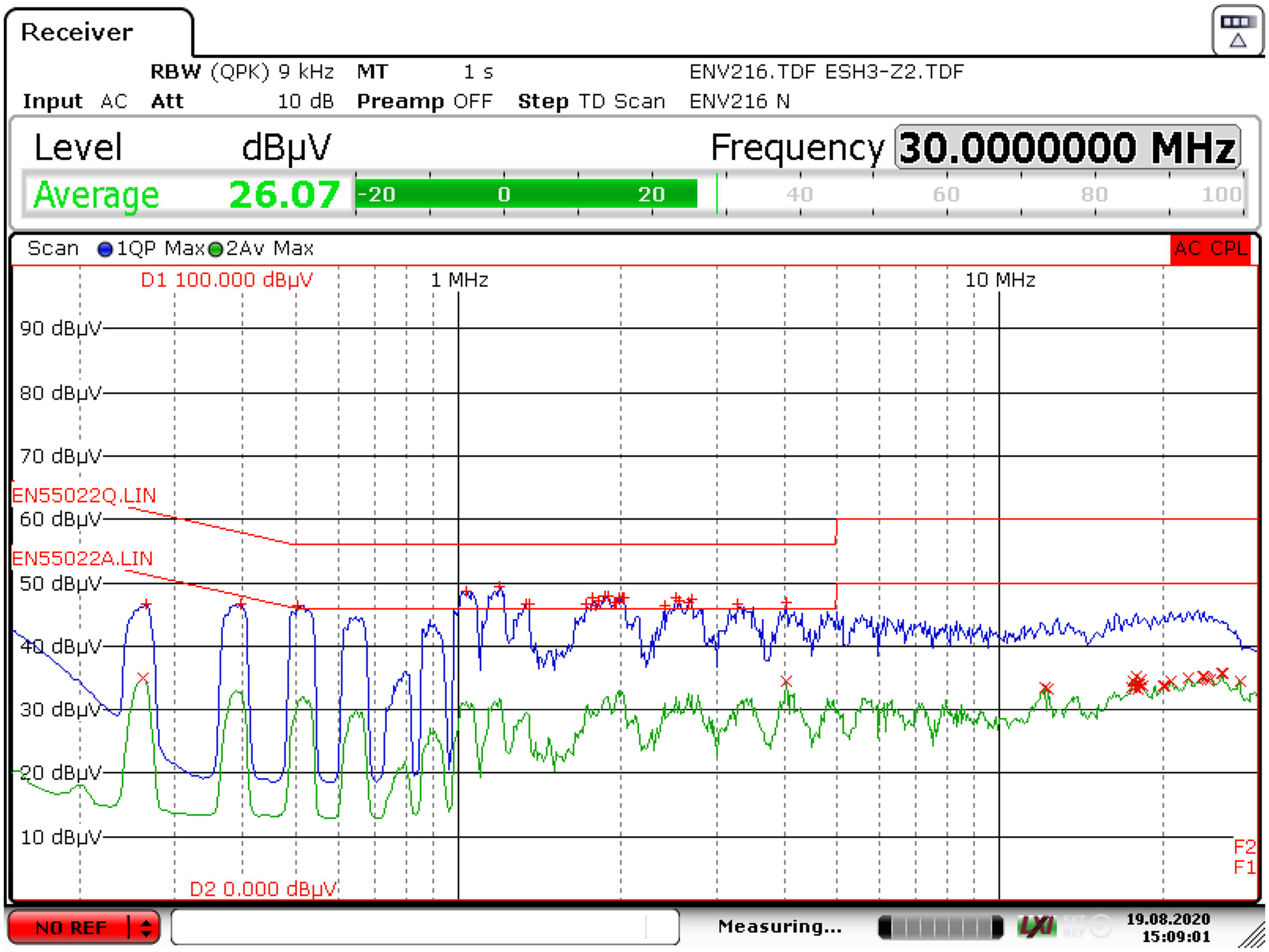
12.2 ***230 VAC 1.25 A Resistive Load***



Date: 19.AUG.2020 15:09:01

Figure 102 – Floating Ground EMI at 115 VAC.

13 Line Surge

Differential input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

13.1 ***Differential Mode Surge***

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

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14 ESD

Note: ESD performance was tested on limited number of units. All ESD strikes were applied at end of cable.

Passed ±8 kV contact discharge

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
+8	VOUT	10	Pass
	GND	10	Pass
-8	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS results, no damage observed.

Passed ±15 kV Air discharge

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+15	VOUT	10	Pass
	GND	10	Pass
-15	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS Results, No Damage was Observed.

15 Appendix A: Primary RCDZ Snubber Implementation for Improved Overall Efficiency

Improved overall efficiency can be achieved by modifying the clamp circuit of the primary RCD snubber. Implementing the primary RCDZ clamp (Zener bleed) configuration, shown below, is done by adding Zener diode, VR1, in series with the clamp resistor R3 in addition to modifying the values of R3 and C3. It is worth pointing out that the Zener bleed configuration is not the same as a Zener clamp, as the latter has no series resistor R3 and parallel capacitor C3. Discussions of the benefits of using this configuration is further explained in the primary clamp section of the Application Note AN58.

At the nominal and extreme line input voltages, the primary RCDZ clamp configuration increased, on average, the full load efficiency by 0.6%, the average efficiency by 0.7%, and the 5% light load efficiency by 4.1%.

15.1 *Schematic*

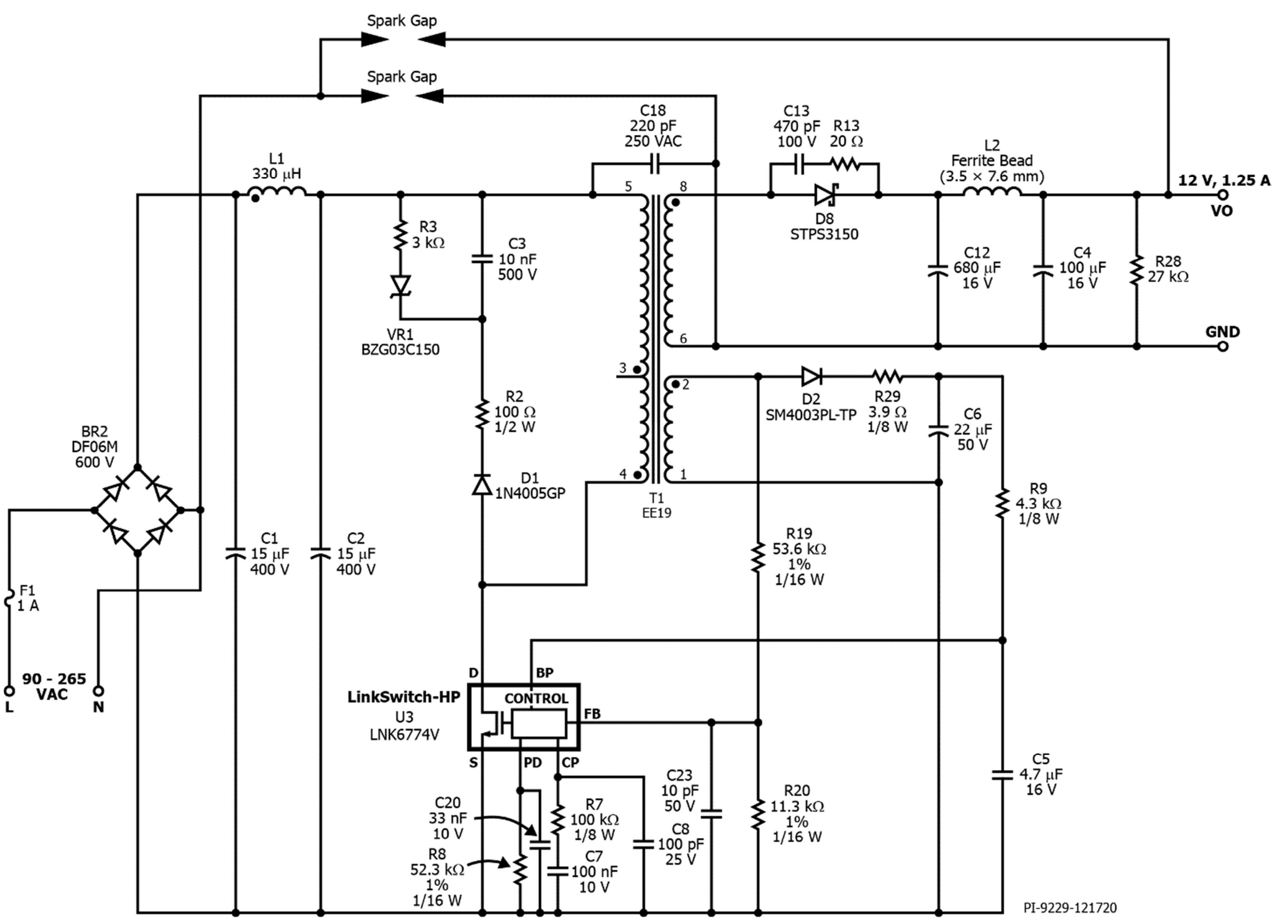

Figure 103 – Schematic.

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15.2 *Average Efficiency*

15.2.1 90 VAC / 60 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	90	340.40	17.34	11.71	1249.90	14.63	84.39
75%	90	266.76	12.93	11.76	937.60	11.03	85.29
50%	90	192.58	8.61	11.83	625.10	7.40	85.87
25%	90	113.91	4.38	11.93	312.60	3.73	85.21
						Average	**85.19**

15.2.2 115 VAC / 60 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} m(A_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	115	286.91	17.14	11.72	1249.90	14.65	85.50
75%	115	228.61	12.85	11.78	937.50	11.04	85.91
50%	115	167.82	8.63	11.84	625.10	7.40	85.72
25%	115	99.49	4.38	11.93	312.60	3.73	85.10
						Average	**85.56**

15.2.3 230 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	230	186.34	17.05	11.74	1249.90	14.67	86.05
75%	230	151.95	12.97	11.79	937.50	11.05	85.23
50%	230	112.47	8.78	11.87	625.10	7.42	84.53
25%	230	66.27	4.53	11.97	312.60	3.74	82.56
						Average	**84.59**

15.2.4 265 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	265	174.31	17.07	11.74	1249.90	14.68	86.00
75%	265	141.81	13.04	11.80	937.50	11.06	84.85
50%	265	106.23	8.83	11.88	625.10	7.43	84.12
25%	265	61.26	4.59	11.99	312.60	3.75	81.67
						Average	**84.16**

15.3 *Efficiency vs Load (RCD and RCDZ)*

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

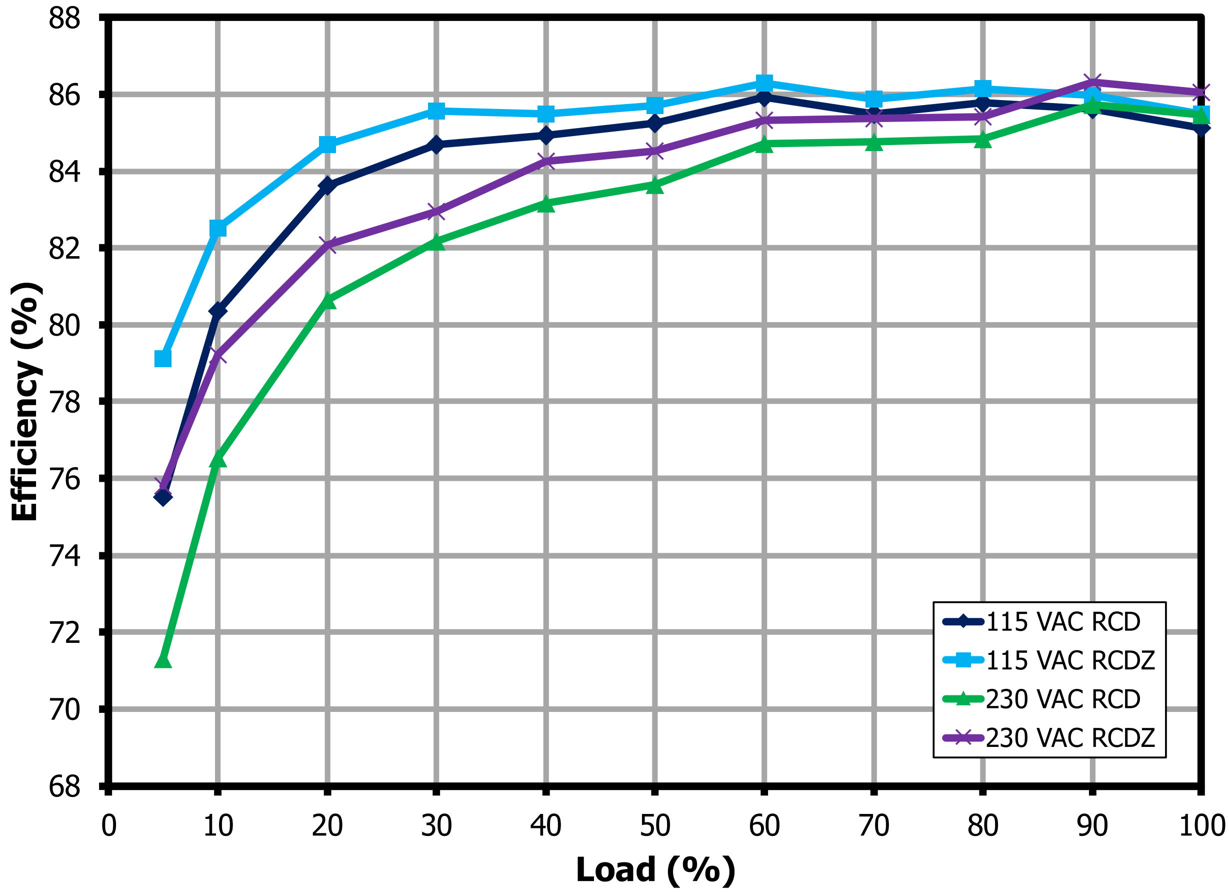

Figure 104 – RCD and RCDZ Efficiency vs. Percentage Load.

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16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
31-Aug-20	VRA	1.0	Initial Release.	Apps & Mktg
15-Dec-20	KM	1.1	Updated Schematic and BOM.	Apps & Mktg

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