



Design Example Report

Title	84 W Isolated Flyback Power Supply Using InnoSwitch™3-CP PowiGaN™ INN3279C-H218
Specification	160 VAC – 264 VAC Input; 42 V / 2 A Output
Application	Adapter / Charger
Author	Applications Engineering Department
Document Number	DER-915
Date	July 23, 2021
Revision	1.1

Summary and Features

- InnoSwitch3-CP is industry first AC/DC IC with isolated, safety rated integrated feedback
- All the benefits of secondary-side control with the simplicity of primary-side regulation
 - In insensitive to transformer variation
 - Built-in synchronous rectification for high efficiency
- <70 mW no-load input power, 230 VAC
- Primary sensed overvoltage protection
- Very high power density
- Very low component count
- Very high efficiency
 - >93% at 230 VAC

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at <https://www.power.com/company/intellectual-property-licensing/>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing a high-line input 42 V / 2 A output power supply/charger using the InnoSwitch3-CP INN3279C-H218 flyback controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-CP controller, providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

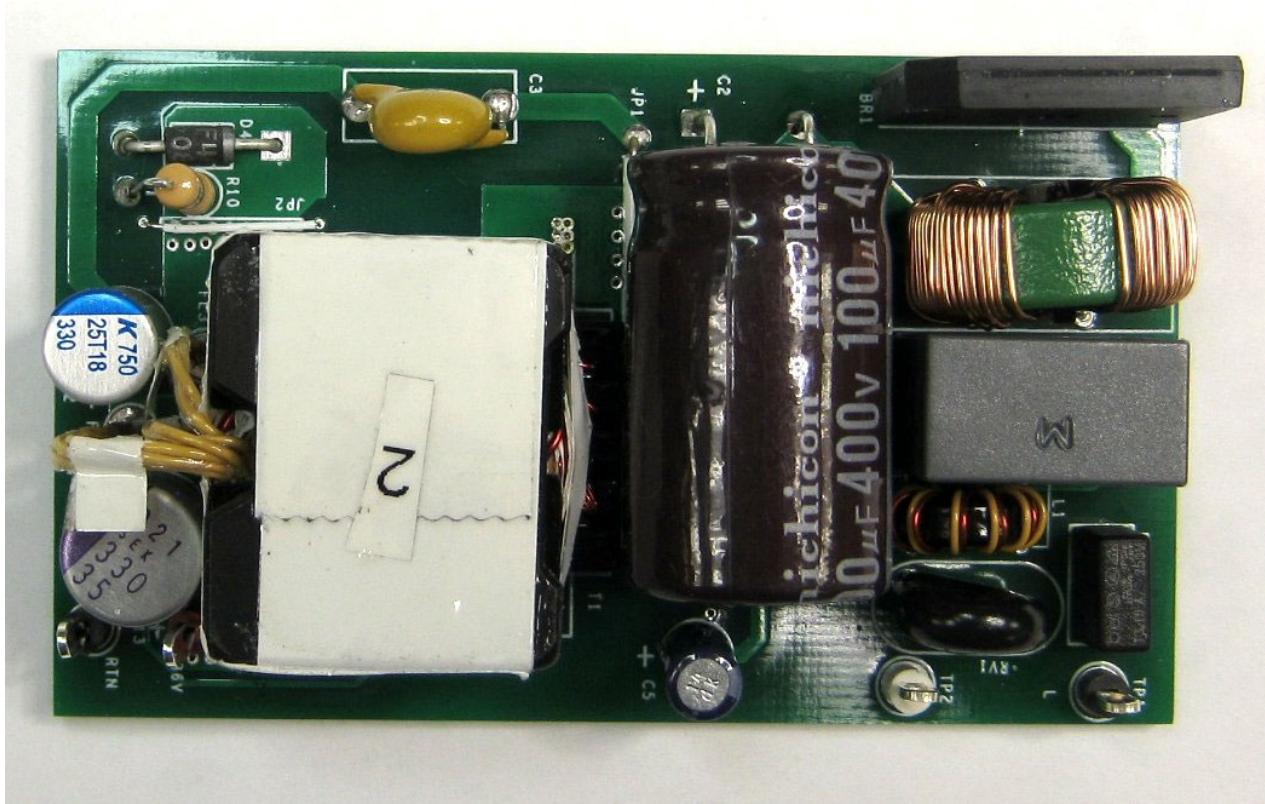


Figure 1 – Populated Circuit Board Photograph, Top.



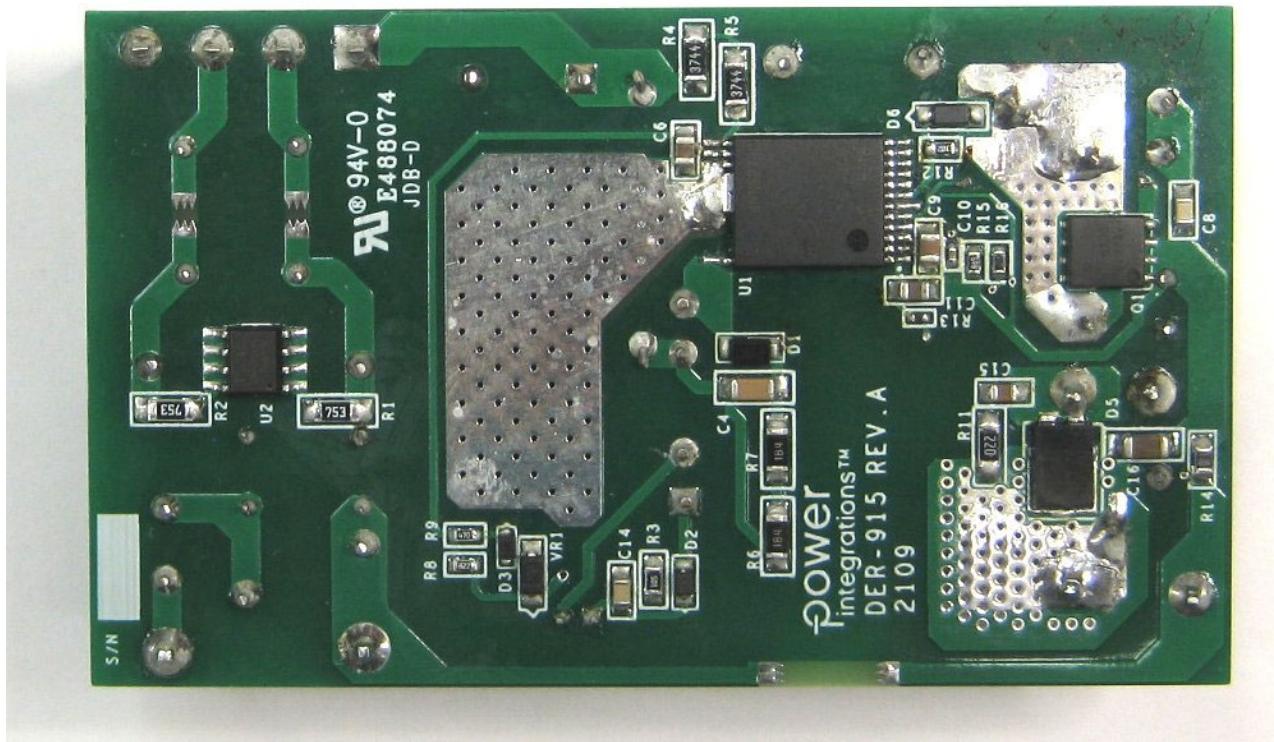


Figure 2 – Populated Circuit Board Photograph, Bottom.



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	160		264	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50	64	Hz	
No-load Input Power (230 VAC)				70	mW	Measured at 230 VAC.
Output						
Output Voltage	V_{OUT}	7	42		V	36V Nominal Output.
Output Ripple Voltage	V_{RIPPLE}		1		V	Peak-Peak On Board.
Output Current	I_{OUT}	0		2	A	On Board.
Continuous Output Power	P_{OUT}	0	84		W	
Conducted EMI						
Safety		Designed to meet IEC60950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	°C	Enclosed in Adapter, Sea Level.



3 Schematic

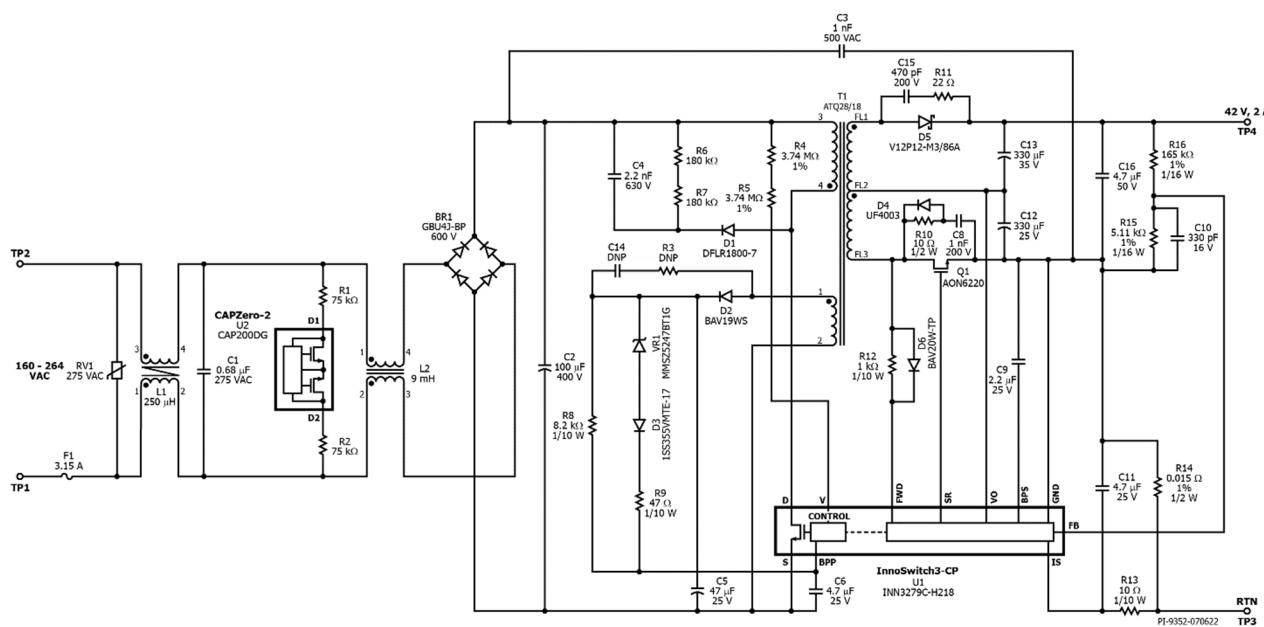


Figure 3 – Schematic.



4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure. The common mode chokes L1 and L2 along with capacitor C1 attenuate EMI. Bridge rectifier BR1 and capacitor C2 rectify the AC line voltage and provide a full wave rectified B+.

Resistors R1 and R2, with U2, discharge capacitor C1 when the power supply is disconnected from AC mains.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

4.2 *InnoSwitch3-CP IC Primary*

One end of the transformer (T1) primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch3-CP IC (U1). Resistors R4-5 provide input voltage sense protection for undervoltage and overvoltage conditions.

An RCD clamp formed by diode D1, resistors R6-7 and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

Controller/switch IC U1 is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when HVDC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on transformer T1. Output of this auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-CP IC (U1), while providing enough current to ensure that the high-voltage tap inside U1 is turned off during normal operation. This reduces the low/no-load input power consumption.

Output regulation is achieved using ramp time modulation control, the frequency and I_{LIM} of switching cycles are adjusted based on the output load. At high load, most switching cycles that are enabled have high value for I_{LIM} in the selected I_{LIM} range, and at light load or no-load most cycles are disabled and the ones enabled have low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the switch will remain on until the primary current ramps to the device current limit for the specific operating state.

Zener diode VR1 and diode D3, along with R9, offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1, which then causes a current to flow into the BPP pin of InnoSwitch3-CP IC U1. If the current flowing into the BPP pin increases



above the I_{SD} threshold, the InnoSwitch3-CP controller will latch off and prevent any further increase in output voltage.

4.3 *InnoSwitch3-CP IC Secondary*

The secondary-side of the InnoSwitch3-CP IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The transformer secondary is split into two stacked windings to provide an intermediate voltage feeding the U1 VOUT pin that is within the rating for that pin. This measure is necessary because the 42 V design V_{OUT} exceeds the U1 VOUT pin voltage rating. The top side of the secondary winding stack is rectified by diode D5 and filtered by C13, while the bottom side is rectified by MOSFET Q1 and filtered by capacitor C12. Capacitor C16 serves to filter the summed output of the two stacked windings. High frequency ringing during switching transients that would otherwise create radiated EMI and/or exceed the PIV ratings of Q1 or D5 is reduced via RCD snubber R10, C8, and D4, as well as RC snubber C15 and R11.

The gate of Q1 is turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R12 and D6 and fed into the FWD pin of the IC.

This power supply operates in discontinuous mode over the entire input voltage range of 160-264 VAC. In discontinuous mode of operation, synchronous rectifier MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 3 mV. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage through R12 and D6 or the intermediate output voltage from the stacked secondary windings. Capacitor C9 connected to the BPS pin of InnoSwitch3-CP IC U1 provides decoupling for the internal circuitry.

Output current is sensed by monitoring the voltage drop across resistor R14 between the IS and GND pins, with a threshold of approximately 35 mV to reduce losses. Resistor R13 and capacitor C11 provide filtering on the IS pin to reduce noise sensitivity.

Output voltage is regulated to achieve a voltage of 1.265 V on the FB pin. Resistors R15-16 set the nominal output voltage to 42 V. Capacitor C10 provides noise filtering of the signal at the FB pin.



5 PCB Layout

PCB copper thickness is 2.0 oz.

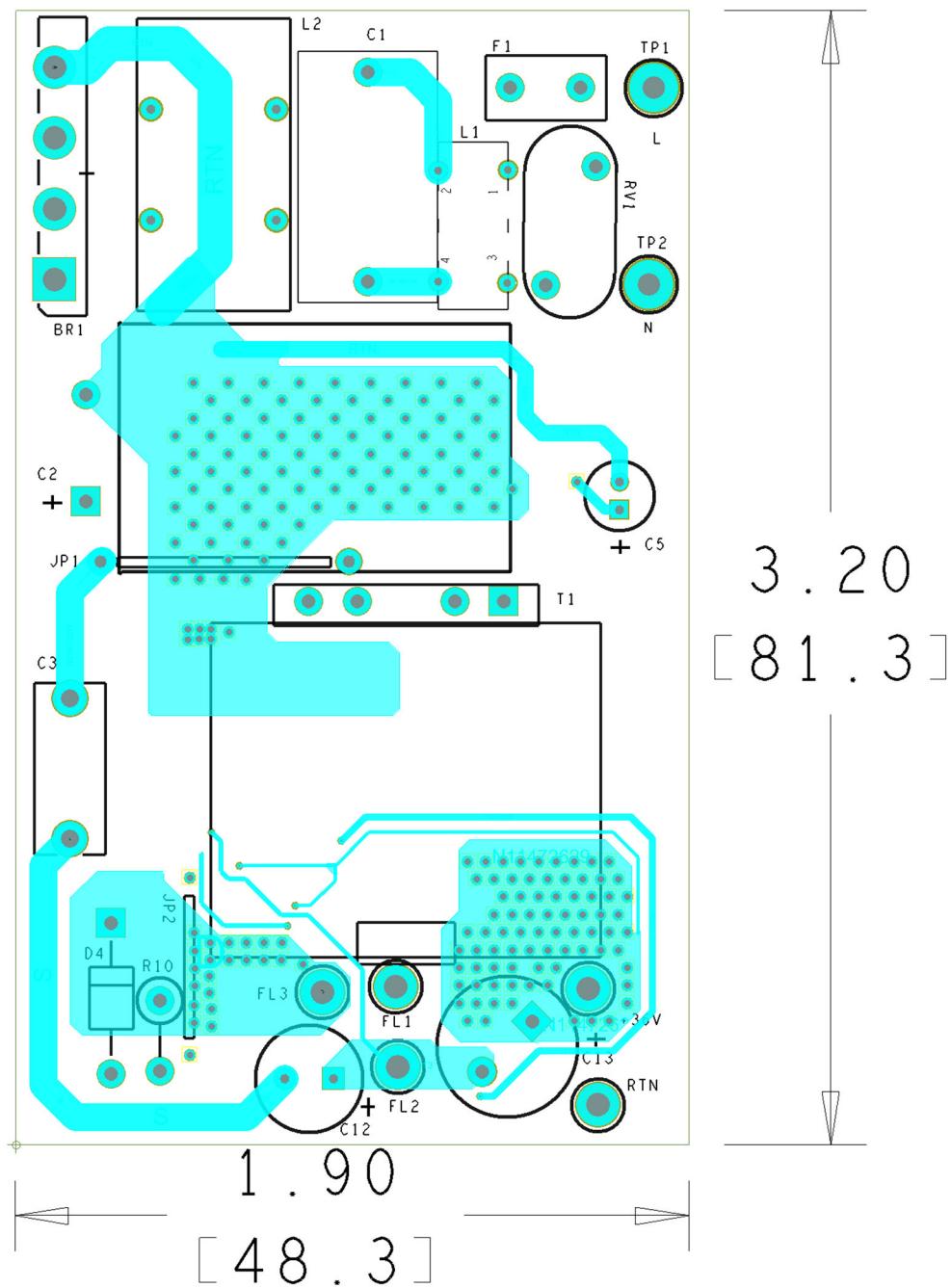


Figure 4 – Printed Circuit Layout, Top.

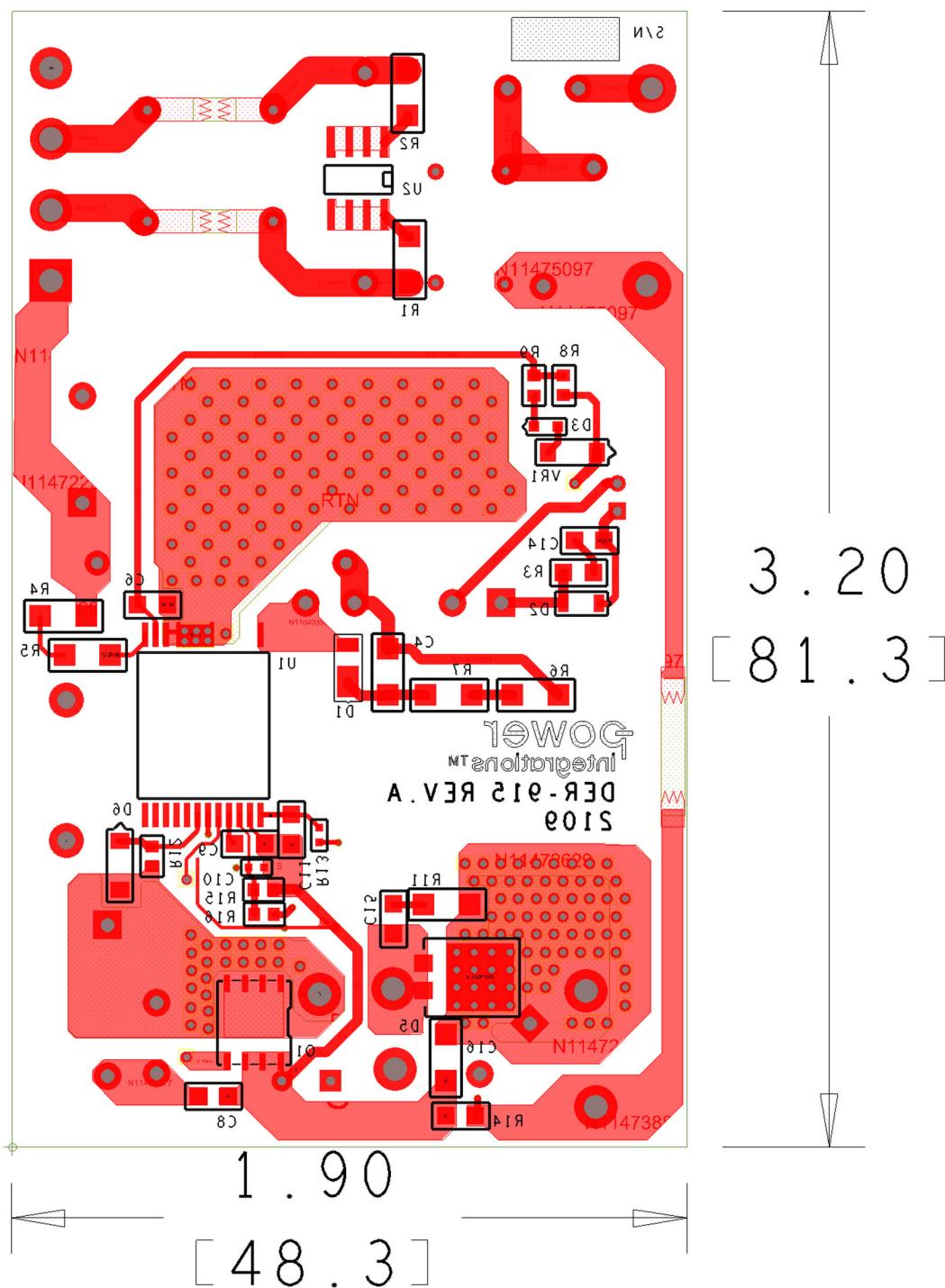


Figure 5 – Printed Circuit Layout, Bottom.



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 4 A, Bridge Rectifier, GBU Case	GBU4J-BP	Micro Commercial
2	1	C1	0.68 μ F, Film, 275VAC, 560VDC, Polypropylene (PP), Metallized Radial, 0.709"" L x 0.394"" W (18.00 mm x 10.00 mm), 0.634"" H (16.10 mm)	R46KI368045P1M	KEMET
3	1	C2	100 μ F, 400 V, Electrolytic, (18 x 31.5)	UPT2G101MHD6	Nichicon
4	1	C3	1 nF, 500Vac, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay
5	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK
6	1	C5	47 μ F, 25 V, Electrolytic, Low ESR, 500 m Ω , (5 x 11.5)	ELXZ250ELL470MEB5D	Nippon Chemi-Con
7	2	C6 C11	4.7 μ F \pm 10%, 25V, X7R, 0805, -55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
8	2	C8 C14	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
9	1	C9	2.2 μ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M125AB	TDK
10	1	C10	330 pF 16 V, Ceramic, X7R, 0402	C0402C331K4RACTU	Kemet
11	1	C12	330 μ F, \pm 20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 m Ω , 2000 Hrs @ 105°C, (8 mm x 13 mm)	A750KS337M1EAAE018	KEMET
12	1	C13	330 μ F, \pm 20%, 35 V, Aluminum Polymer Radial, Can, 18 m Ω , 1000 Hrs @ 125°C	35SEK330M	Panasonic
13	1	C15	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
14	1	C16	4.7 μ F, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
15	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc,
16	1	D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc,
17	1	D3	DIODE SML SIG 80V 100 mA SSMINI2	1SS355VMTE-17	Rohm Semi
18	1	D4	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
19	1	D5	Diode, Schottky, 120V, 12A, Surface Mount, TO-277A (SMPC)	V12P12-M3/86A	Vishay
20	1	D6	150 V, 0.2 A, SOD-123	BAV20W-TP	Micro Commercial
21	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
22	1	JP1	Wire Jumper, Insulated, TFE, #22 AWG, 0.7 in	C2004-12-02	Alpha
23	1	JP2	Wire Jumper, Insulated, #28 AWG, 0.5 in	2842/1 WH005	Alpha Wire
24	1	L1	250 μ H, Toroidal Common Mode Choke, custom, DER-538, wound on 32-00275-00 core.	32-00367-00	Power Integrations
25	1	L2	9 mH, 2 A, Common Mode Choke	T18107V-902S P.I. Custom	Fontaine
26	1	Q1	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
27	2	R1 R2	RES, 75 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ753V	Panasonic
28	1	R3	RES, 1.0 M Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ105V	Panasonic
29	2	R4 R5	RES, 3.74 M Ω , 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay
30	2	R6 R7	RES, 180 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ184V	Panasonic
31	1	R8	RES, 8.2 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ822V	Panasonic
32	1	R9	RES, 47 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
33	1	R10	RES, 10 Ω , 5%, 1/2 W, Carbon Film	CFR-50JB-10R	Yageo
34	1	R11	RES, 22 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ220V	Panasonic
35	1	R12	RES, 1 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
36	1	R13	RES, 10 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ100X	Panasonic
37	1	R14	RES, 0.015 Ω , 0.5 W, 1%, 0805	ERJ-6BWFR015V	Panasonic
38	1	R15	RES, 5.11 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5111V	Panasonic
39	1	R16	RES, 165 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1653V	Panasonic
40	1	RV1	275 VAC, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic



41	1	T1	Transformer, ATQ28/18, Vertical, 4 pins	Custom	Custom
42	2	TP1 TP3	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
43	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
44	1	TP4	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
45	1	U1	InnoSwitch3-CP3 Switch Integrated Circuit, InSOP24D	INN3279C-H218	Power Integrations
46	1	U2	CAPZero-2, SO-8C	CAP200DG	Power Integrations
47	1	VR1	DIODE, ZENER, 17 V, ±5%, 500 mW, SOD123, SOD-123	MMSZ5247BT1G	ON Semi

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7 Flyback Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-CP_Flyback_032321 ; Rev.1.7; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-CP Flyback Design Spreadsheet
2 APPLICATION VARIABLES						
3	VAC_MIN	160		160	V	Minimum AC line voltage
4	VAC_MAX	264		264	V	Maximum AC input voltage
5	VAC_RANGE			HIGH LINE		AC line voltage range
6	FLINE	50		50	Hz	AC line voltage frequency
7	CAP_INPUT	100.0		100.0	uF	Input capacitance
9 SET-POINT 1						
10	VOUT1	42.00	Warning	42.00	V	The output voltage exceeds the Vout Pin voltage rating. Reduce the output voltage
11	IOUT1	2.000		2.000	A	Output current 1
12	POUT1		Info	84.00	W	The output power required exceeds the device capability: Verify thermal performance if no other warnings
13	EFFICIENCY1	0.93		0.93		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
72	CDC	0		0	mV	Cable drop compensation desired at maximum output current
73	BASE_SETPOINT	1		1		Base SET-POINT voltage to determine the feedback network lower resistor value
77 PRIMARY CONTROLLER SELECTION						
78	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
79	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
80	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
81	DEVICE_GENERIC	INN32X9-H218		INN32X9-H218		Device selection
82	DEVICE_CODE			INN3279C-H218		Device code
83	PDEVICE_MAX			80	W	Device maximum power capability
84	RDSON_25DEG			0.44	Ω	Primary switch on-time resistance at 25°C
85	RDSON_100DEG			0.62	Ω	Primary switch on-time resistance at 100°C
86	ILIMIT_MIN			2.395	A	Primary switch minimum current limit
87	ILIMIT_TYP			2.576	A	Primary switch typical current limit
88	ILIMIT_MAX			2.756	A	Primary switch maximum current limit
89	VDRAIN_ON_PRSW			0.28	V	Primary switch on-time voltage drop
90	VDRAIN_OFF_PRSW			581.896	V	Peak drain voltage on the primary switch during turn-off
94 WORST CASE ELECTRICAL PARAMETERS						
95	FSWITCHING_MAX	73000		73000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
96	VOR	140.0		140.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
97	VMIN			192.10	V	Valley of the rectified minimum input AC voltage at full load
98	KP			1.106		Measure of continuous/discontinuous mode of operation
99	MODE_OPERATION			DCM		Mode of operation
100	DUTYCYCLE			0.398		Primary switch duty cycle
101	TIME_ON			6.54	us	Primary switch on-time



102	TIME_OFF			8.31	us	Primary switch off-time
103	LPRIMARY_MIN			447.1	uH	Minimum primary magnetizing inductance
104	LPRIMARY_TYP			470.6	uH	Typical primary magnetizing inductance
105	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
106	LPRIMARY_MAX			494.2	uH	Maximum primary magnetizing inductance
108	PRIMARY CURRENT					
109	IAVG_PRIMARY			0.454	A	Primary switch average current
110	ipeak_PRIMARY			2.573	A	Primary switch peak current
111	ipedestal_PRIMARY			0.000	A	Primary switch current pedestal
112	iripple_PRIMARY			2.573	A	Primary switch ripple current
113	irms_PRIMARY			0.883	A	Primary switch RMS current
115	SECONDARY CURRENT					
116	ipeak_SECONDARY			8.821	A	Secondary winding peak current
117	ipedestal_SECONDARY			0.000	A	Secondary winding pedestal current
118	irms_SECONDARY			3.543	A	Secondary winding RMS current
119	iripple_CAP_OUT			2.925	A	Output capacitor ripple current
123	TRANSFORMER CONSTRUCTION PARAMETERS					
124	CORE SELECTION					
125	CORE	ATQ28/18.1B	Info	ATQ28/18.1B		Refer to the Transformer Parameters tab to verify fit factor
126	CORE NAME			ATQ28/18.1B		Core code
127	AE			153.0	mm^2	Core cross sectional area
128	LE			47.7	mm	Core magnetic path length
129	AL			9800	nH	Ungapped core effective inductance per turns squared
130	VE			7298	mm^3	Core volume
131	BOBBIN NAME			TBI-238-07271.17XX		Bobbin name
132	AW			37.4	mm^2	Bobbin window area
133	BW			8.50	mm	Bobbin width
134	MARGIN			0.0	mm	Bobbin safety margin
136	PRIMARY WINDING					
137	NPRIMARY			24		Primary winding number of turns
138	BPEAK			3796	Gauss	Peak flux density
139	BMAX			3417	Gauss	Maximum flux density
140	BAC			1708	Gauss	AC flux density (0.5 x Peak to Peak)
141	ALG			817	nH	Typical gapped core effective inductance per turns squared
142	LG			0.216	mm	Core gap length
143	LAYERS_PRIMARY			2		Primary winding number of layers
144	AWG_PRIMARY			23		Primary wire gauge
145	OD_PRIMARY_INSULATED			0.642	mm	Primary wire insulated outer diameter
146	OD_PRIMARY_BARE			0.573	mm	Primary wire bare outer diameter
147	CMA_PRIMARY		Info	577.1	Cmils/A	The primary winding wire CMA is higher than 500 mil^2/Ampères: Decrease the primary layers or wire thickness
149	SECONDARY WINDING					
150	NSECONDARY	7		7		Secondary winding number of turns
151	AWG_SECONDARY			21		Secondary wire gauge
152	OD_SECONDARY_INSULATED			1.029	mm	Secondary wire insulated outer diameter



153	OD_SECONDARY_BAR_E			0.723	mm	Secondary wire bare outer diameter
154	CMA_SECONDARY			228.6	Cmils/A	Secondary winding wire CMA
155						
156	BIAS WINDING					
157	NBIAS			3		Bias winding number of turns
161	PRIMARY COMPONENTS SELECTION					
162	LINE UNDERVOLTAGE					
163	BROWN-IN REQUIRED			128.00	V	Required line brown-in threshold
164	RLS			6.48	MΩ	Connect two 3.24 MΩ resistors to the V-pin for the required UV/OV threshold
165	BROWN-IN ACTUAL			129.58	V	Actual brown-in threshold using standard resistors
166	BROWN-OUT ACTUAL			117.16	V	Actual brown-out threshold using standard resistors
168	LINE OVERVOLTAGE					
169	OVERVOLTAGE_LINE		Warning	541.14	V	The device voltage stress will be higher than 650V when overvoltage is triggered
171	BIAS WINDING					
172	VBIAS	12.00		12.00	V	Rectified bias voltage at the lowest output set-point
173	VF_BIAS			0.70	V	Bias winding diode forward drop
174	VREVERSE_BIASDIODE			58.49	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
175	CBIAS			22	uF	Bias winding rectification capacitor
176	CBPP			4.70	uF	BPP pin capacitor
180	SECONDARY COMPONENTS SELECTION					
181	RECTIFIER					
182	VDRAIN_OFF_SRFET			150.47	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
183	SRFET	AUTO	Info	AON7254		The voltage stress (including the parasitic ring) on the secondary MOSFET selected may exceed the device BVDSS: pick a MOSFET with a higher BVDSS
184	VBREAKDOWN_SRFET			150	V	Secondary rectifier breakdown voltage
185	RDSON_SRFET			66.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
187	FEEDBACK COMPONENTS					
188	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
189	RFB_LOWER			3.09	kΩ	Lower feedback resistor required to obtain the output for cable drop compensation
190	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor

Note: The spreadsheet displays a warning for output voltage, as the specified 42 V output is greater than the rating of the Innoswitch VOUT pin. This problem is addressed by using two stacked output voltage windings and feeding the VOUT pin with the lower winding stack such that the voltage is within the ratings of the Innoswitch VOUT pin. Output synchronous rectifier MOSFET, Output Rectifier, and output filter capacitor are selected based on the lower voltages present on the two stacked winding rather than for a single winding as represented in the spreadsheet.



8 Transformer Specification

8.1 Electrical Diagram

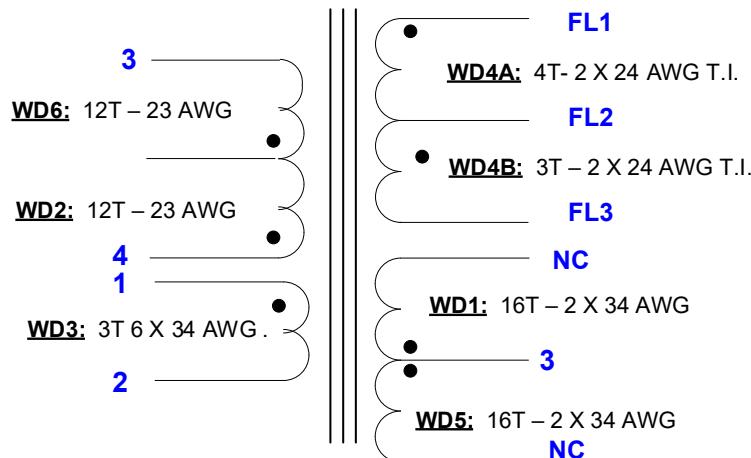


Figure 6 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-4 to FL1-3.	3000 VAC
Primary Inductance	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	471 μ H, $\pm 5\%$
Resonant Frequency	Pins 3-4, all other windings open.	600 kHz (Min.)
Primary Leakage	Pins 3-4, with FL1 and FL3 shorted, measured at 100 kHz, 0.4 V _{RMS} .	4 μ H (Max.)

8.3 Material List

Item	Description
[1]	Core Pair: ATQ28-18, A_{LG} of 818 nH/T ² ;
[2]	Bobbin: ATQ28-18 Vertical, 4 pins; PI#: 25-01170-00. (Pin-out to be indicated as in picture below)
[3]	Triple Insulated Wire: #24 AWG Furukawa Tex-E or Equivalent.
[4]	Magnet Wire: #34 AWG Solderable Double Coated.
[5]	Magnet Wire: #25 AWG Solderable Double Coated.
[6]	Tape: Polyester Film, 3M 1350F-1 or Equivalent, 8.4 mm wide.
[7]	Tape: Polyester Film, 3M 1350F-1 or Equivalent, 30 mm Wide.
[8]	Tape: Polyester Film, 3M 1350F-1 or Equivalent, 18 mm Wide.
[9]	Varnish. Dolph BC-359 or Equivalent.



8.4 Transformer Build Diagram

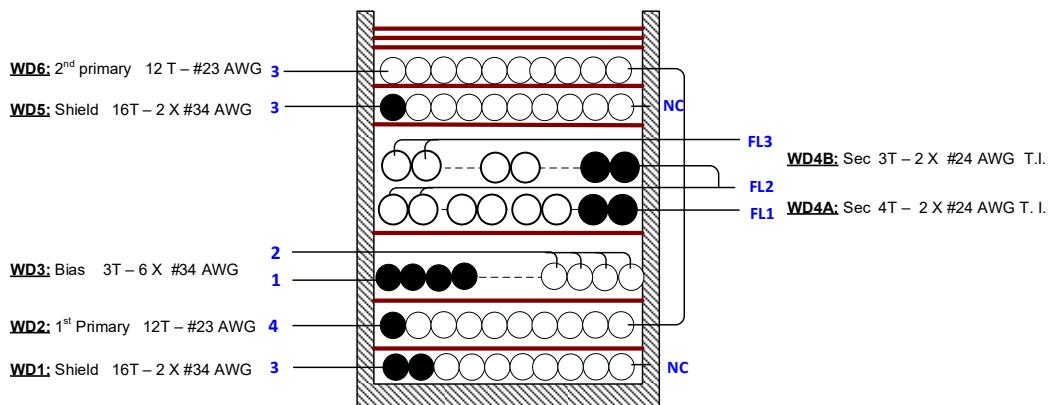


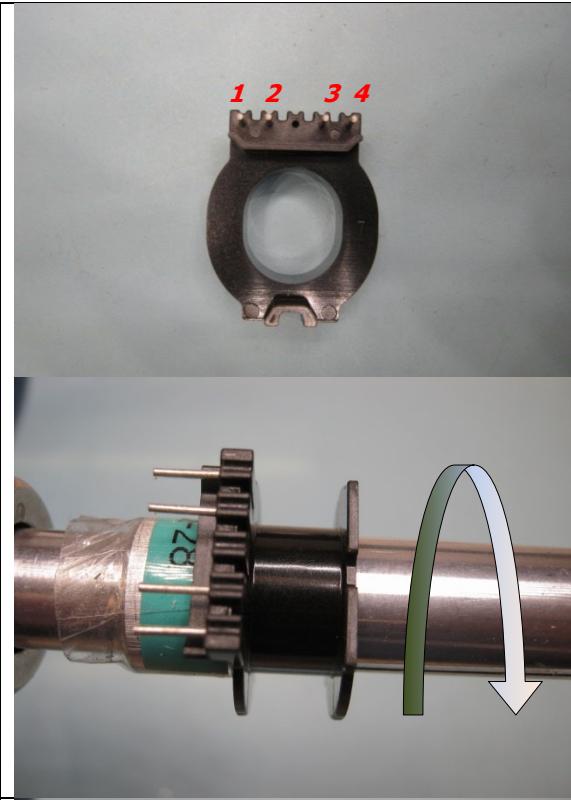
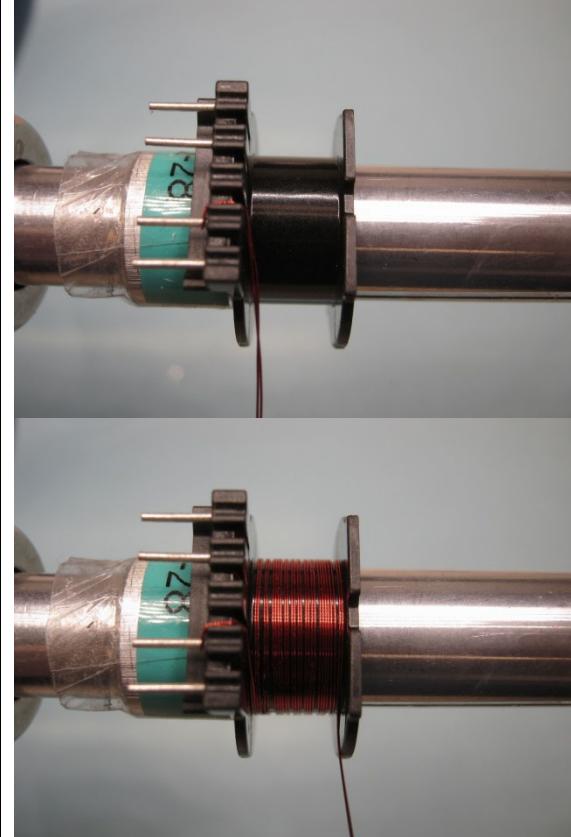
Figure 7 – Transformer Build Diagram.

8.5 Transformer Construction

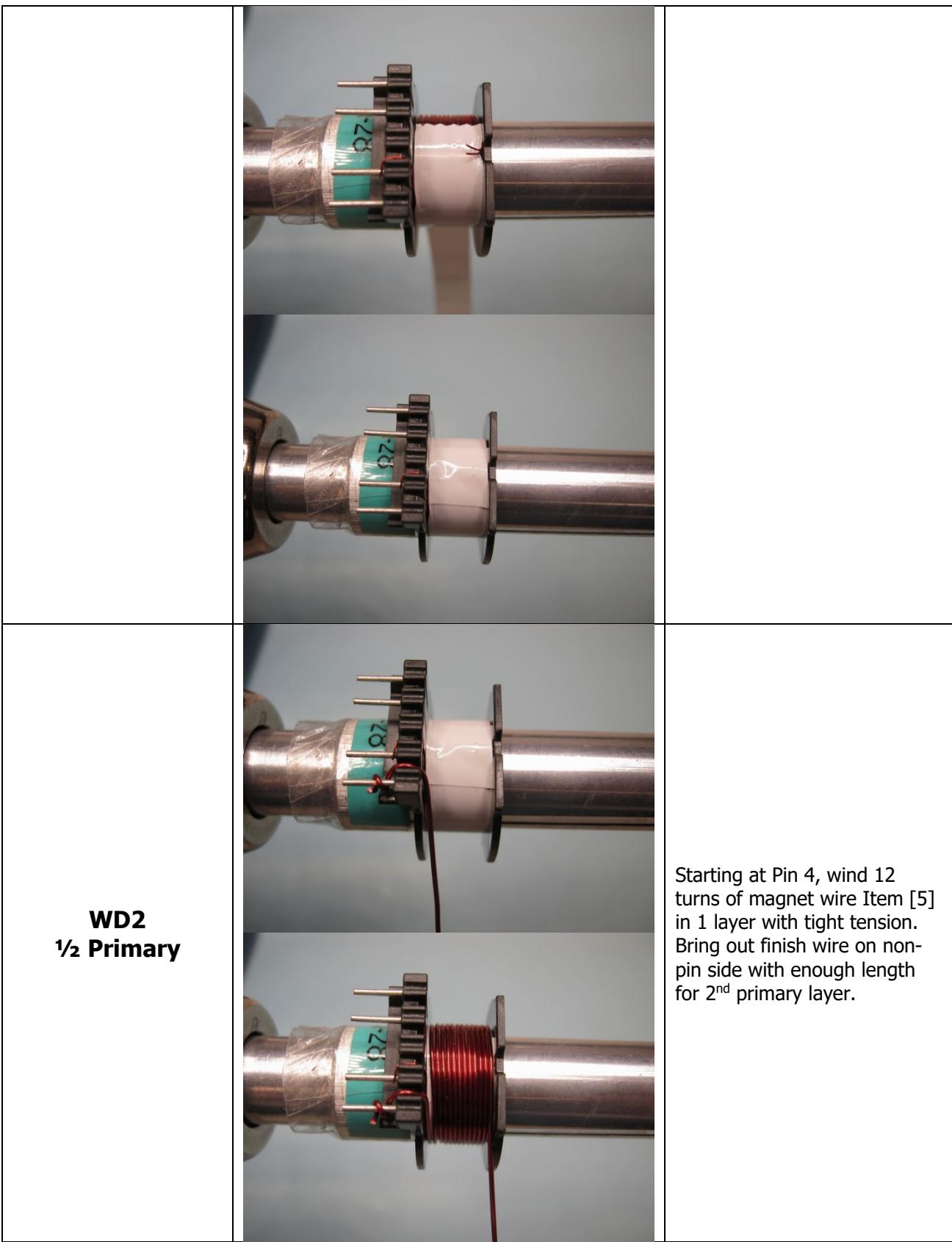
Winding Preparation	Position the bobbin Item [2] on the mandrel such that the pin side is on the left. Winding direction is clock-wise direction.
WD1 Shield/Insulation	Starting at pin 3, wind 16 bifilar turns of wire [4] in one layer. Place 1.5 layer of tape Item [6]. Cut finish lead of previous winding short, trap between tape layers.
WD2 1st half Primary	Starting at Pin 4, wind 12 turns of magnet wire Item [5] in 1 layer with tight tension. Bring out finish wire on non-pin side with enough length for 2 nd primary layer.
Insulation	Place 1 layer of tape Item [6].
WD3 Bias	Starting at pin 1, wind 3 hexafilar turns of wire [4] in 1 layer, spread wire evenly on the bobbin, and finish at pin 2.
Insulation	Place 1 layer of tape Item [6].
WD4A Secondary	Start with _ cm bifilar length of TIW [3] with 3 cm flying start lead exiting from secondary winding slot opposite to bobbin pin side per picture. Tape to mandrel as shown. Mark start lead. Wind 4 bifilar turns of TIW [3], bring finish back to secondary slot as shown. Leave 3 cm of finish lead, tape to mandrel to secure.
WD4B Secondary	Start with _ cm bifilar length of TIW with 3 cm flying start lead exiting from secondary winding slot as shown. Tape start lead to mandrel as shown. Mark start lead. Wind 3 bifilar turns of TIW [3], bring finish back to secondary slot. Leave 3 cm of finish lead, tape to mandrel to secure.
Insulation	Place 2 layers of tape Item [6].
WD5 Shield/Insulation	Starting at pin 3, wind 13 bifilar turns of wire [4] in 1 layer with tight tension Use 1.5 turns of tape to secure winding – bury finish between tape layers.
Insulation	Place 1 layer of tape Item [6].
WD6 2nd half Primary	Starting with wire left from first primary layer, wind 12 bifilar turns of wire [5] in 1 layer with tight tension, and finish at pin 3.
Finish Wrap	Place 3 layers of tape Item [6].
Finish	Gap core halves for 471 μ H \pm 5%. Assemble core halves in bobbin, secure with two turns of tape [6]. Wrap secondary side of assembled transformer as shown with 3 layers of tape [7] as shown. Secure tape wrap with 3 turns of tape [8] as shown. Twist finish of WDG 4A and start of WDG 4B together, trim to 30 mm and tin 5 mm. Twist WDG 4A start wires together, trim to 30mm and tin 5 mm. Twist finish leads of WD 4B tightly together, trim to 30 mm and tin 5 mm. Dip varnish Item [8].

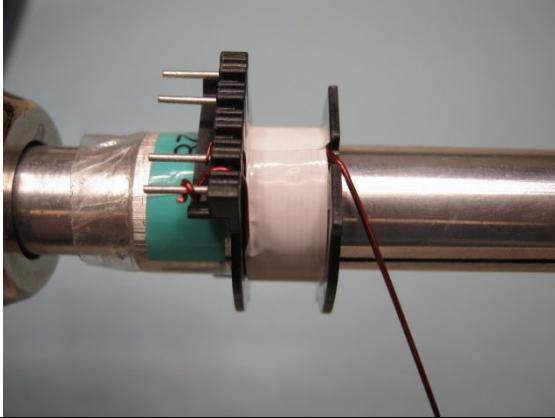
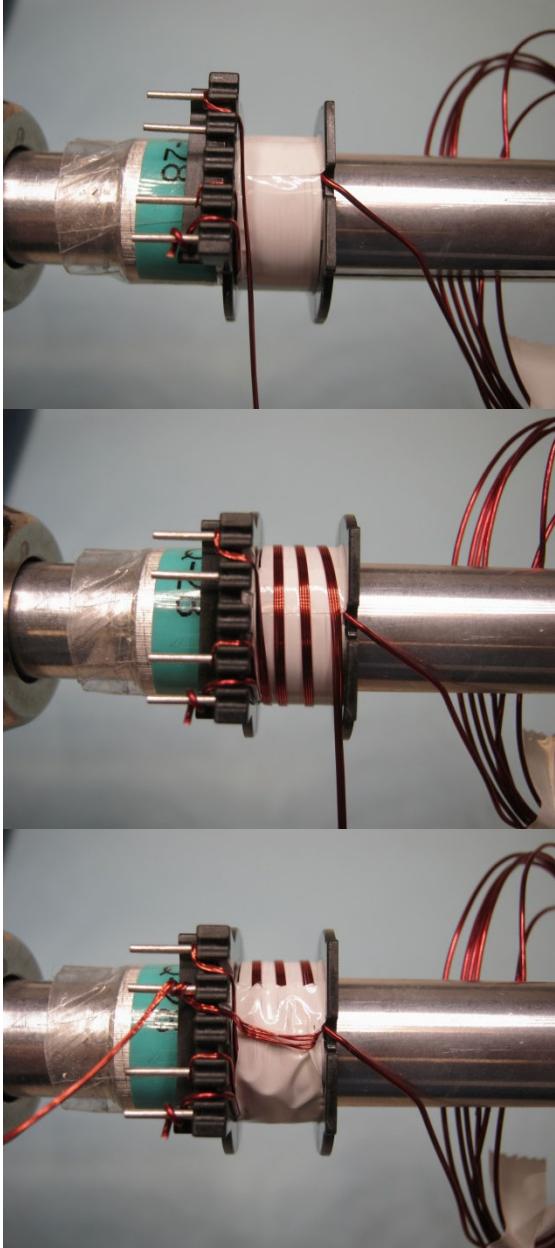


8.6 *Winding Illustrations*

Winding Preparation		<p>Pin-out of bobbin is indicated as in picture beside. Position the bobbin Item [2] on the mandrel such that the pin side is on the left. Winding direction is clock-wise direction.</p>
WD1 Shield/Insulation		<p>Starting at pin 3, wind 16 bifilar turns of wire [4] in one layer. Place 1.5 layer of tape Item [6]. Cut finish lead of previous winding short, trap between tape layers.</p>



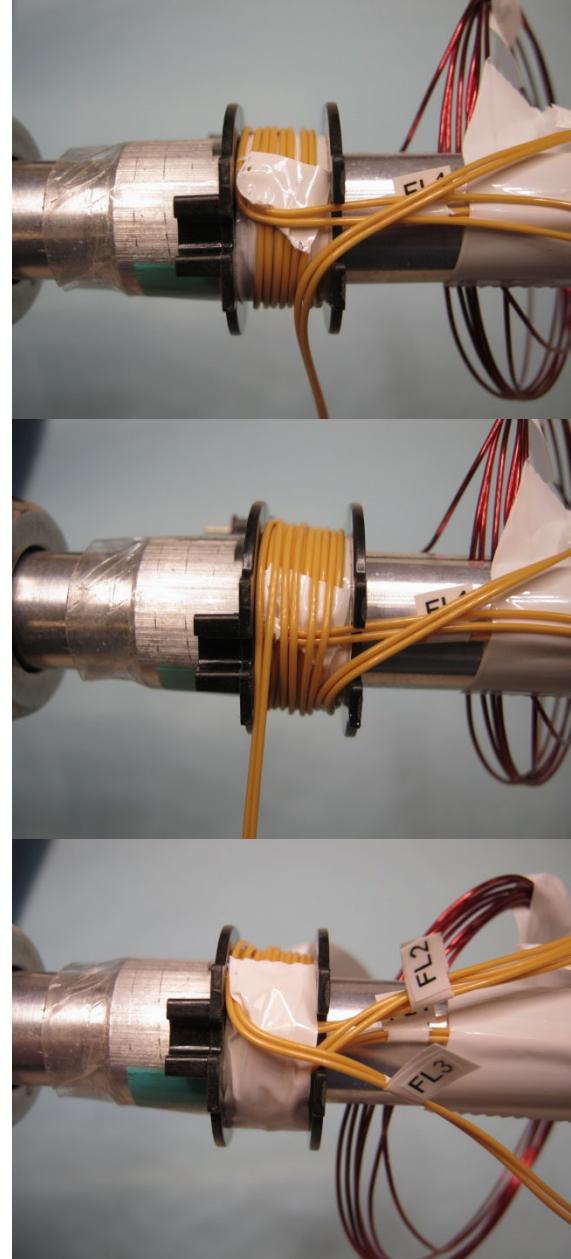
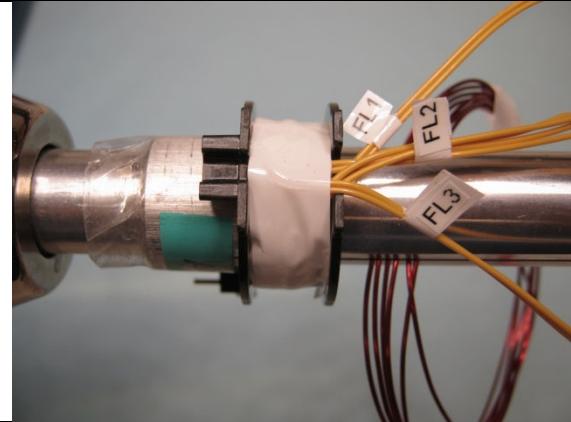


Insulation		Place 1 layer of tape Item [6].
WD3 Bias		Starting at pin 1, wind 3 hexafilar turns of wire [4] in 1 layer, spread wire evenly on the bobbin, and finish at pin 2.

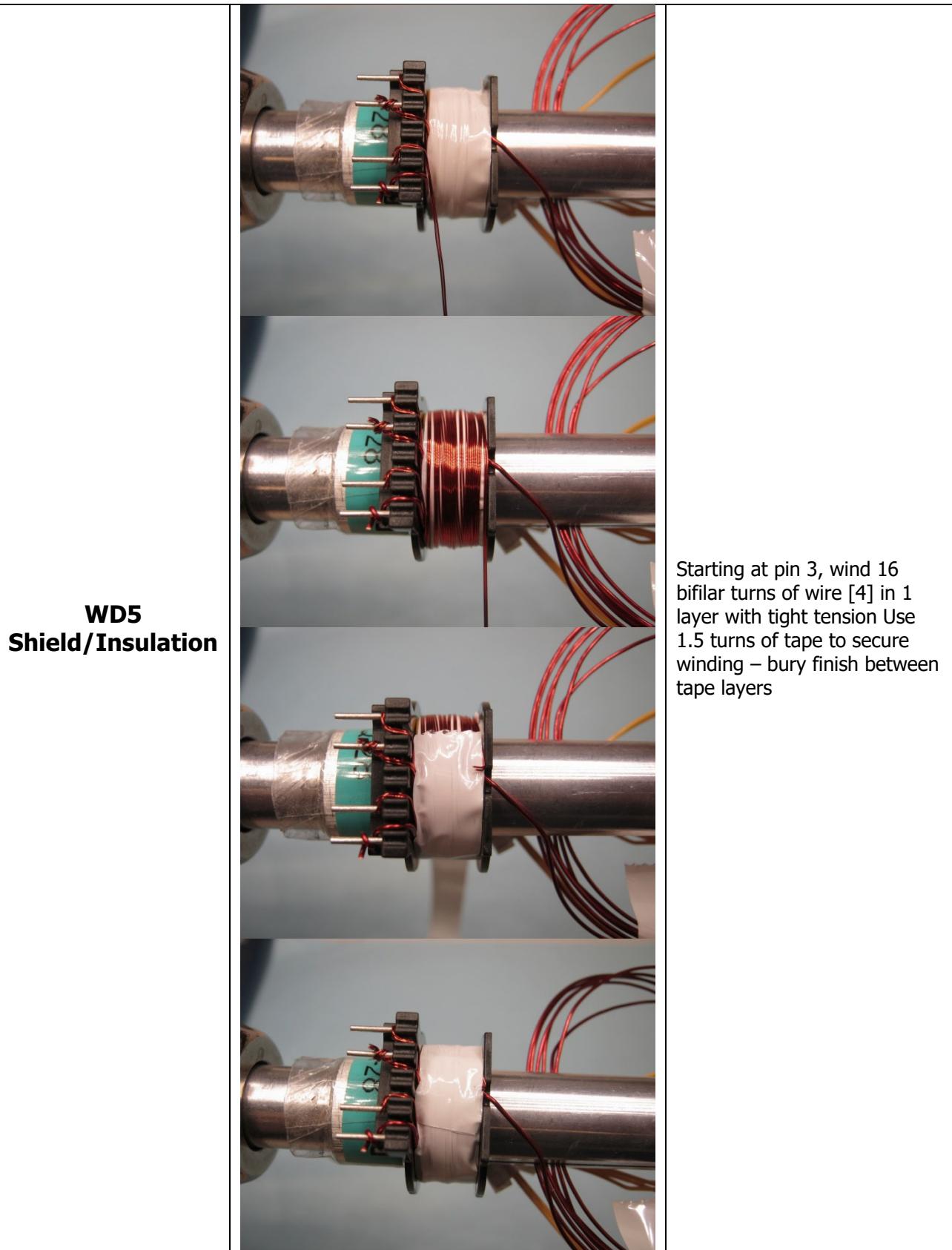


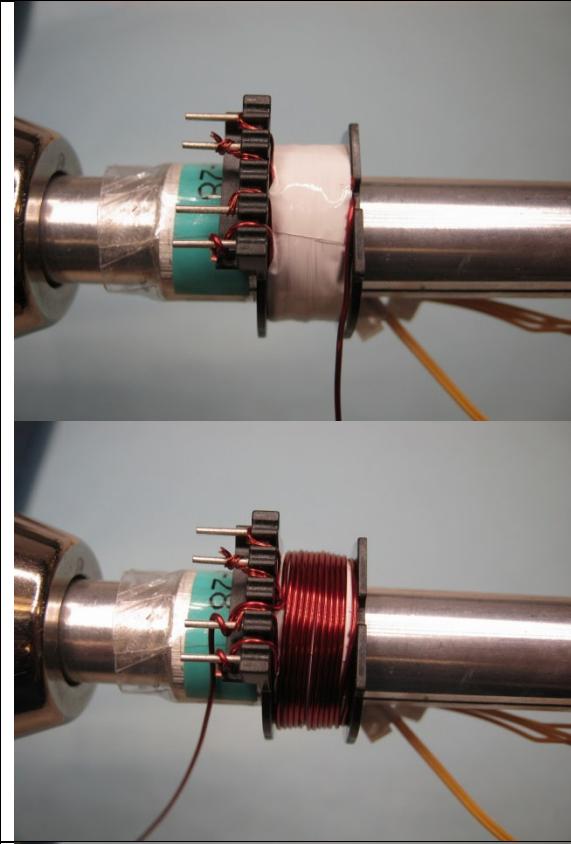
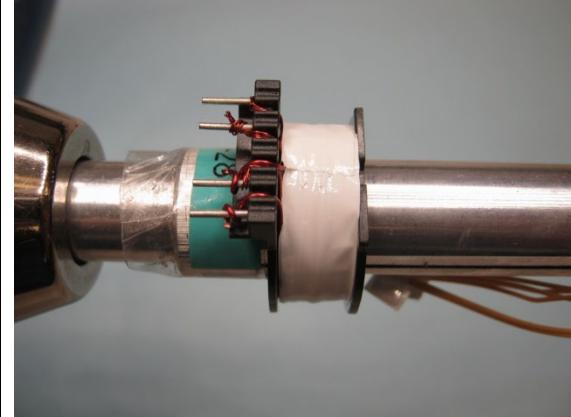
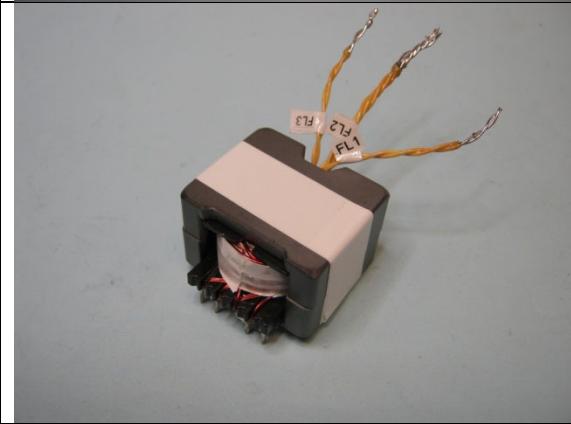
Insulation		Place 1 layer of tape Item [6].
WD4A Secondary		Start with _cm bifilar length of TIW [3] with 3 cm flying start lead exiting from secondary winding slot opposite to bobbin pin side per picture. Tape to mandrel as shown. Mark start lead. Wind 4 bifilar turns of TIW [3], place a piece of to hold wires in place then bring finish back to secondary slot as shown. Leave 3 cm of finish lead, tape to mandrel to secure.



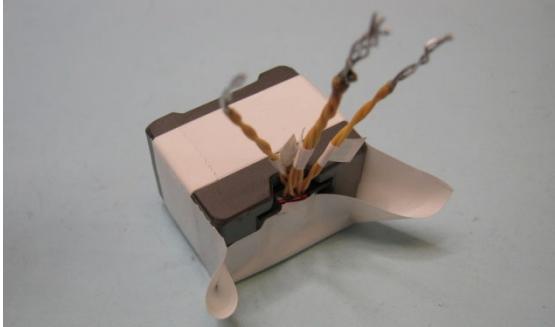
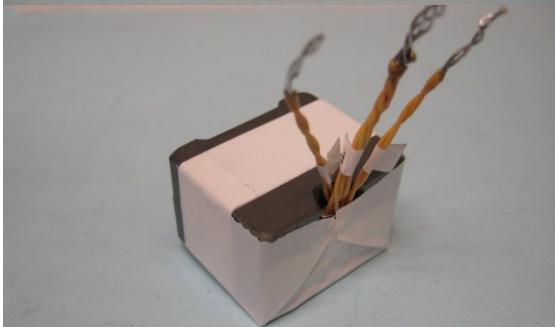
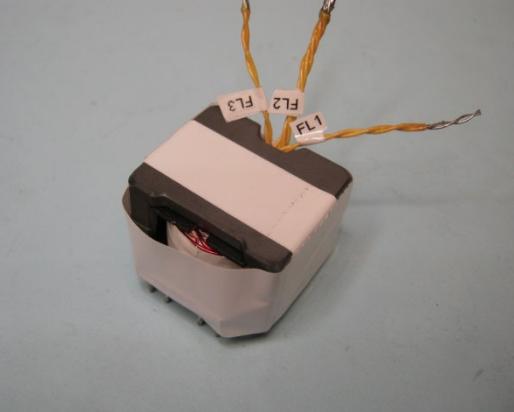
WD4b Secondary		<p>Start with _ cm bifilar length of TIW with 3 cm flying start lead exiting from secondary winding slot as shown. Tape start lead to mandrel as shown. Mark start lead. Wind 3 bifilar turns of TIW [3], bring finish back to secondary slot. Leave 3 cm of finish lead, tape to mandrel to secure.</p>
Insulation		<p>Place 1 layer of tape Item [6].</p>





WD6 2nd half Primary		<p>Starting with wire left from first primary layer, wind 12 bifilar turns of wire [5] in 1 layer with tight tension, and finish at pin 3.</p>
Finish Wrap		<p>Place 3 layers of tape Item [6].</p>
Finish		<p>Gap core halves for $471 \mu\text{H} \pm 5\%$. Assemble core halves in bobbin, secure with two turns of tape [6]. Wrap secondary side of assembled transformer as shown with 3 layers of tape [7]. Secure tape wrap with 3 turns of tape [6] as shown. Twist finish of WDG 4A and start of WDG 4B together, trim to 30 mm and tin 5 mm. Twist WDG 4A startwires together, trim to 30mm and</p>



	 	tin 5 mm. Twist finish leads of WD 4B tightly together, trim to 30 mm and tin 5 mm. Dip varnish Item [8].
		Finished transformer.



9 Input HF Common Mode Choke Specifications

9.1 250 μ H Common Mode Choke (L3)

9.1.1 Electrical Diagram

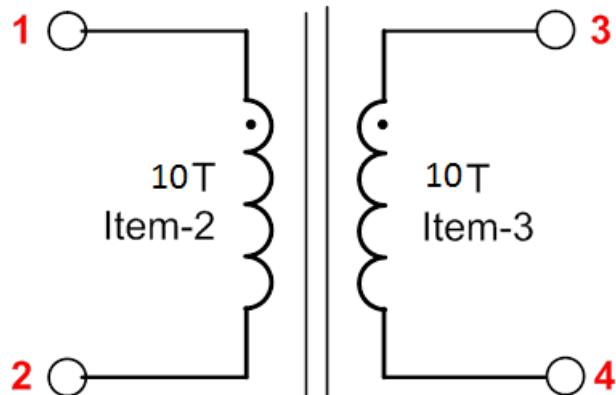


Figure 8 – Inductor Electrical Diagram.

9.1.2 Electrical Specifications

Winding Inductance	Pin 1-pin 2 (pin 3-pin 4), all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	250 μ H ± 20%
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9.1.3 Material List

Item	Description
[1]	Toroidal Core: 35T0375-10H, PI#: 32-00275-00.
[2]	Triple Insulated Wire: #27 AWG, Triple Coated.
[3]	Magnet Wire: #27 AWG, Double Coated.



Figure 9 – Finished Choke.

10 Performance Data

All the performance data have been taken at the board output terminals unless otherwise specifically mentioned.

10.1 *Efficiency vs. Output Power*

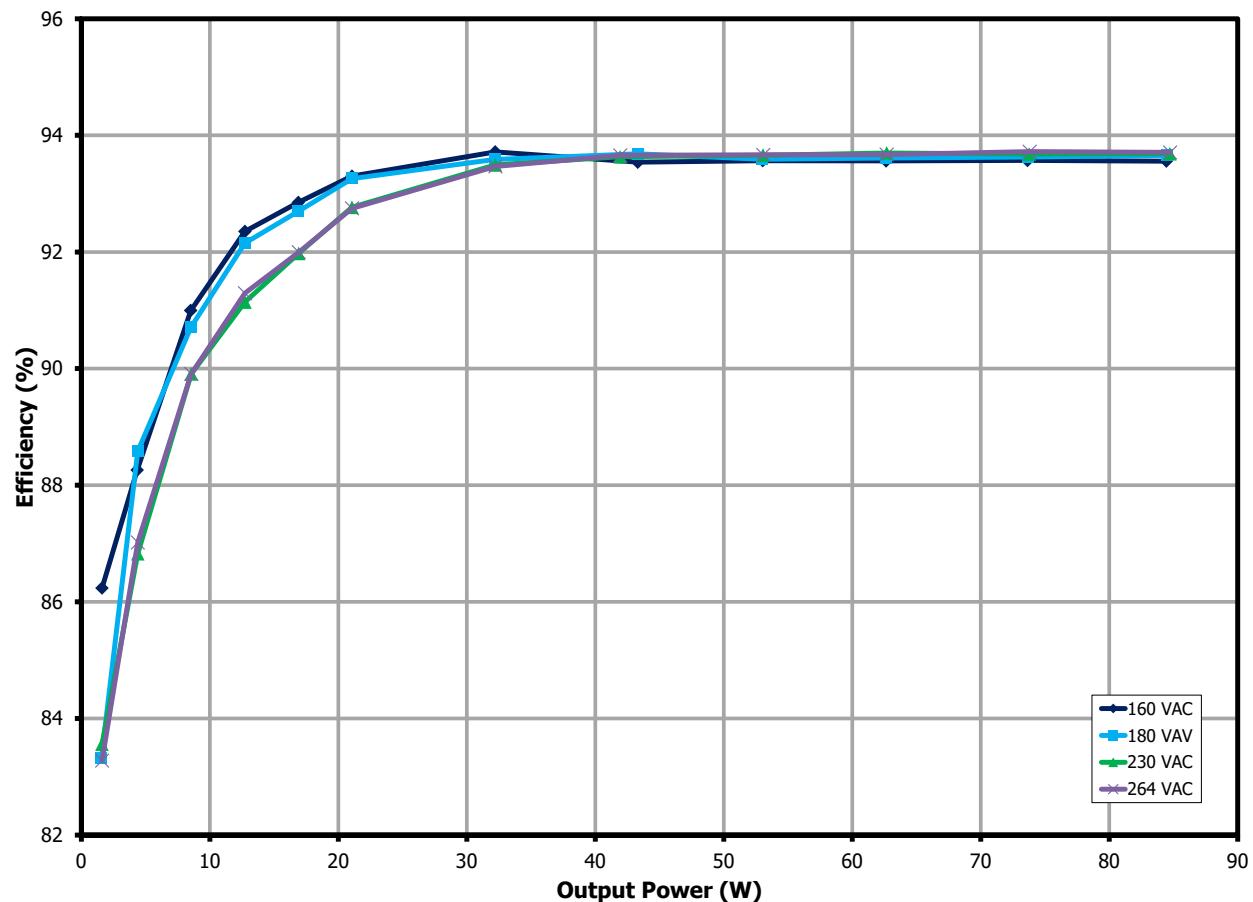


Figure 10 – Efficiency vs. Output Power, Room Ambient.

10.2 **No-Load Input Power**

No-load power was measured using a Yokogawa WT210 operating in watt-seconds mode, with 10 minute integration time.

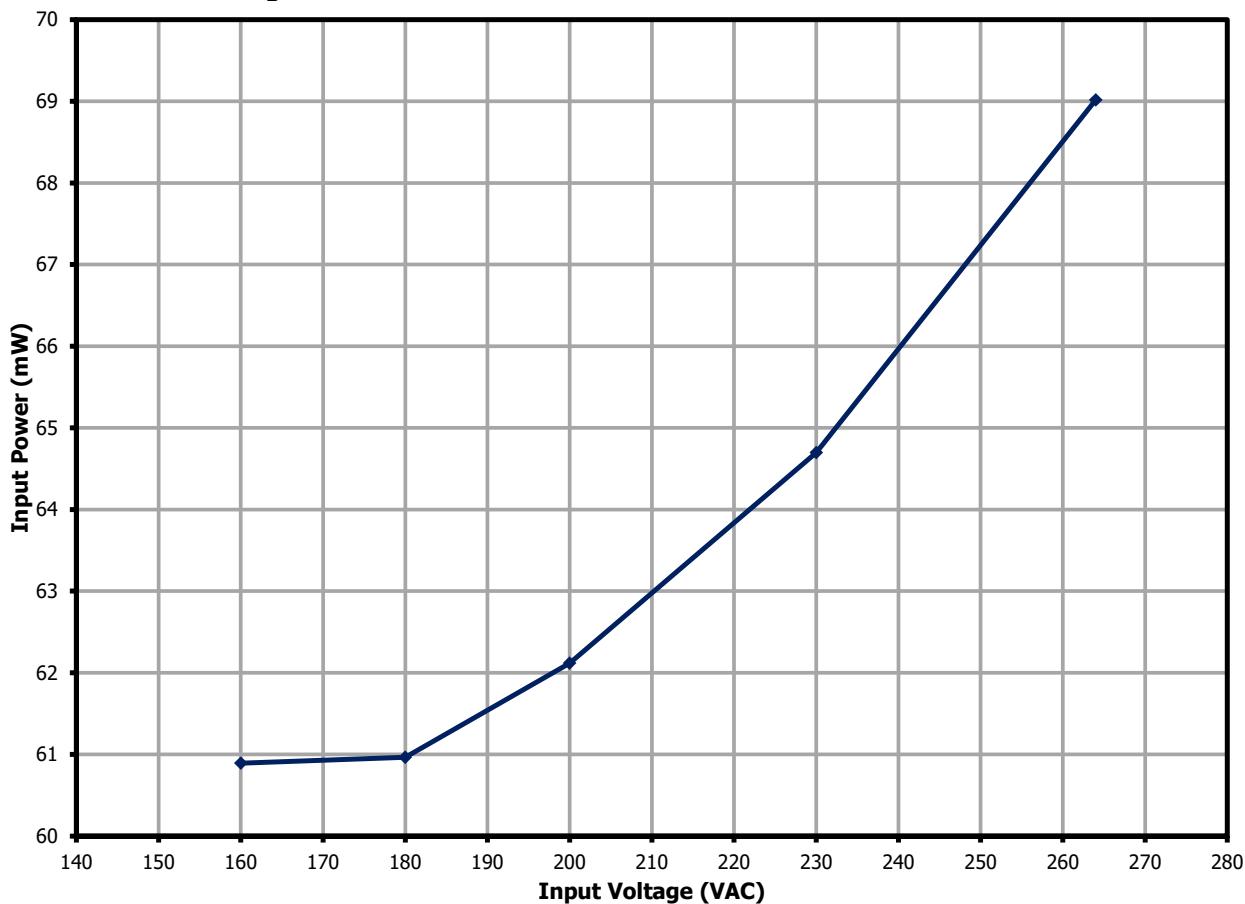


Figure 11 – No-Load Input Power vs. Input Line Voltage, Room Temperature.



10.3 ***Line Regulation***

Line regulation data was captured at supply output terminals.

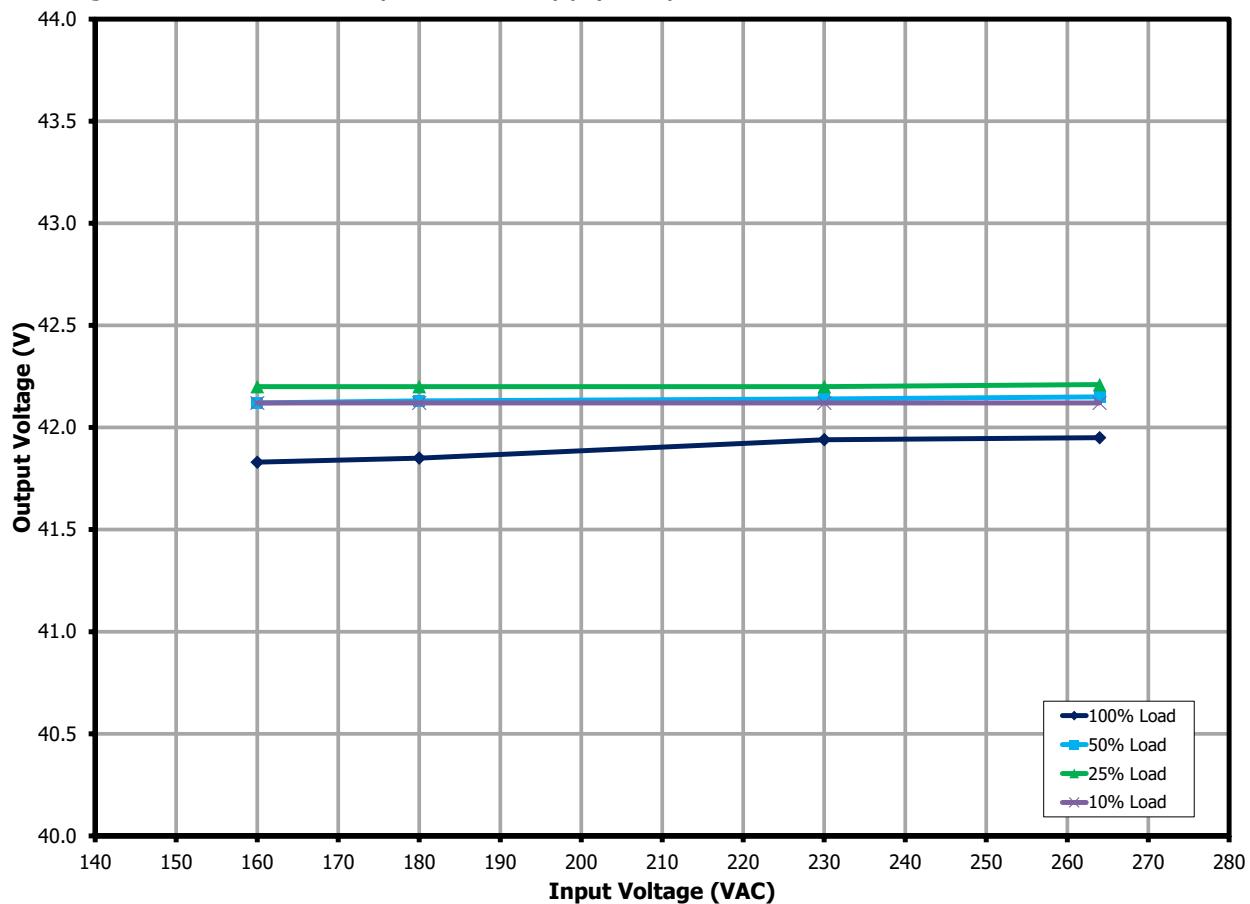


Figure 12 – Line Regulation, Room Temperature.

10.4 ***Load Regulation***

Load regulation data was captured at supply output terminals.

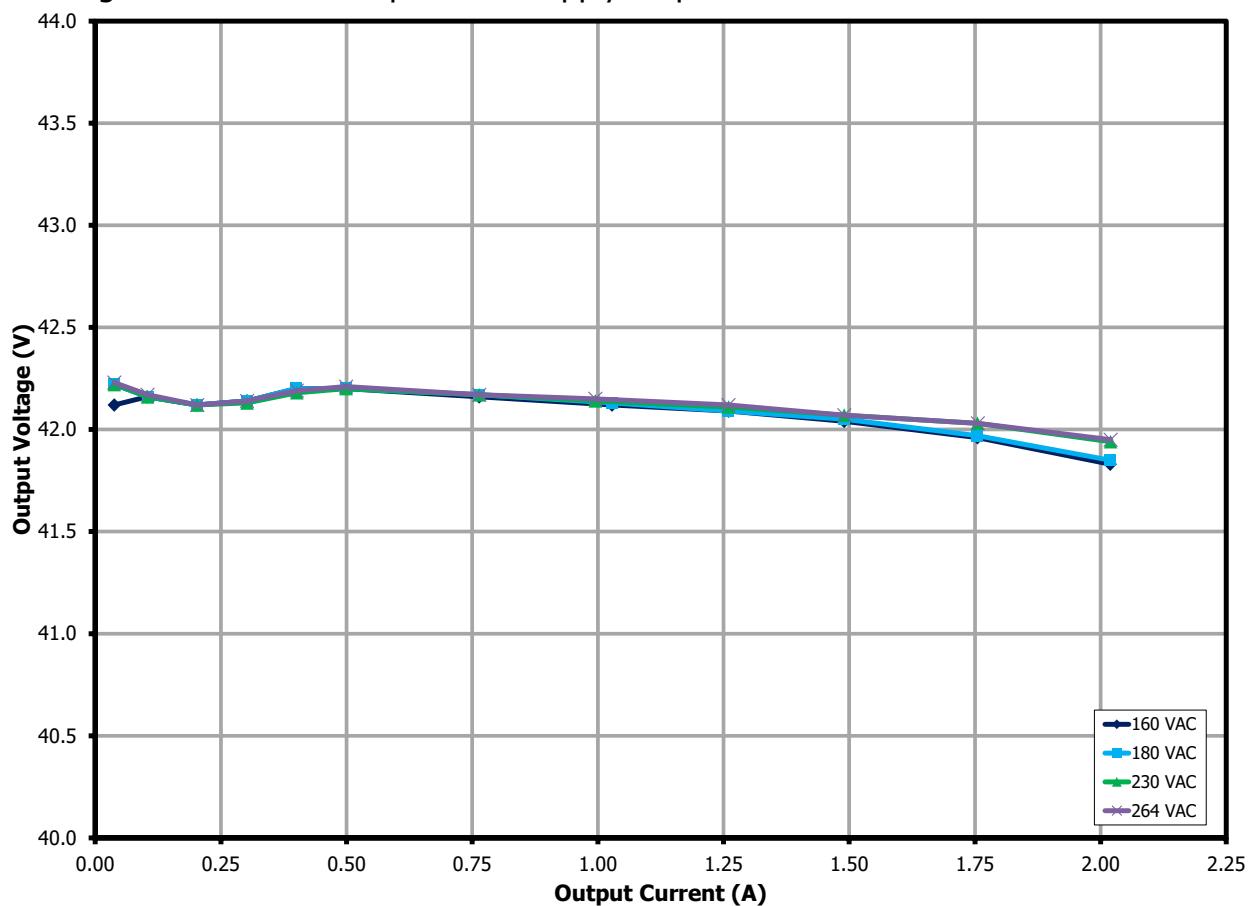


Figure 13 – Load Regulation, Room Temperature.

10.5 **V-I Characteristic**

The V-I characteristic was measured at 230 VAC input using an electronic load set to constant resistance, to plot the V-I characteristic in both the constant voltage and constant current region.

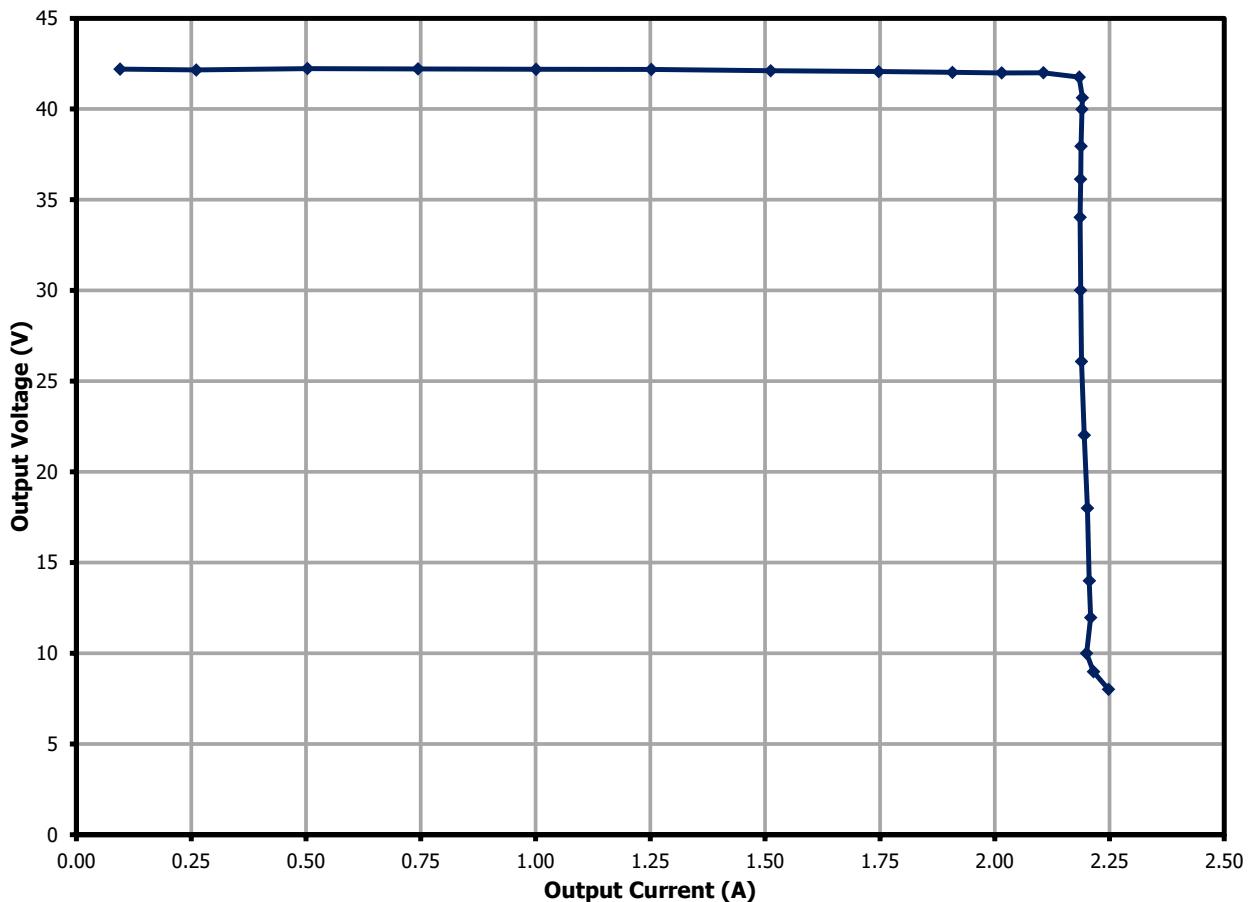


Figure 14 – V-I Characteristic, 230 VAC Input.

10.6 *Average Efficiency***10.6.1 230 VAC**

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	84.719	93.68	93.44
75	62.684	93.7	
50	41.929	93.63	
25	21.058	92.77	



10.7 ***Thermal Performance***

Thermal performance is measured room temperature.

10.7.1 160 VAC, 100% Load

Amb	U1	Q1	D5	T1 Core	T1 Wdg
24	68.9	61.8	82.5	67.3	71.6
BR1					
61.4					

10.7.2 180 VAC, 100% Load

Amb	U1	Q1	D5	T1 Core	T1 Wdg
25	69.7	61.8	81.5	68.4	77.2
BR1					
57.4					

10.7.3 230 VAC, 100% Load

Amb	U1	Q1	D5	T1 Core	T1 Wdg
24	73.3	64.7	85.5	72.4	79.7
BR1					
53.6					

10.7.4 264 VAC, 100% Load

Amb	U1	Q1	D5	T1 Core	T1 Wdg
25	79.5	67.6	86.7	72.4	83
BR1					
48.1					



11 Waveforms

11.1 Load Transient Response (at output terminals)

11.1.1 0-100% Load Transient

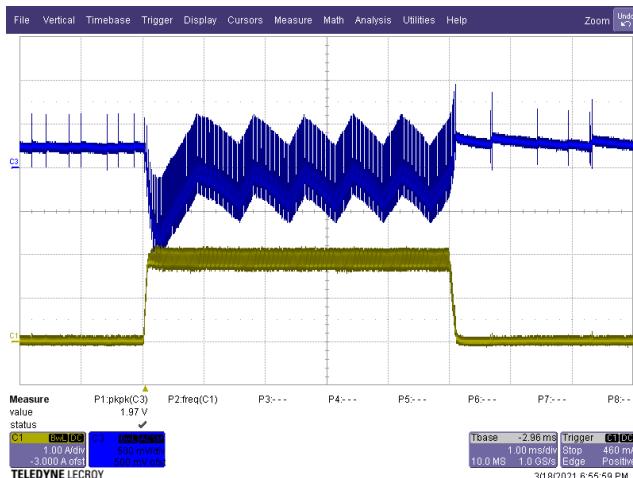


Figure 15 – Transient Response 160 VAC, 0 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.

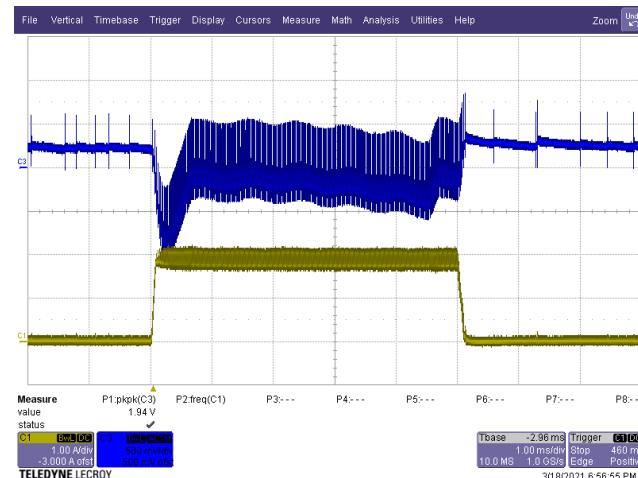


Figure 16 – Transient Response, 180 VAC, 0 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.

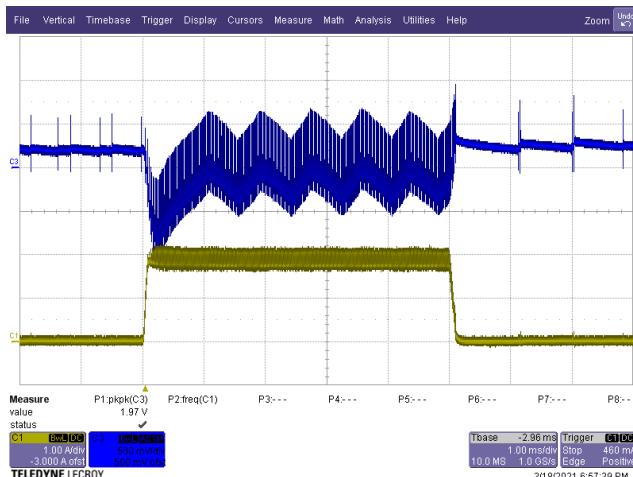


Figure 17 – Transient Response, 230 VAC, 0 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.

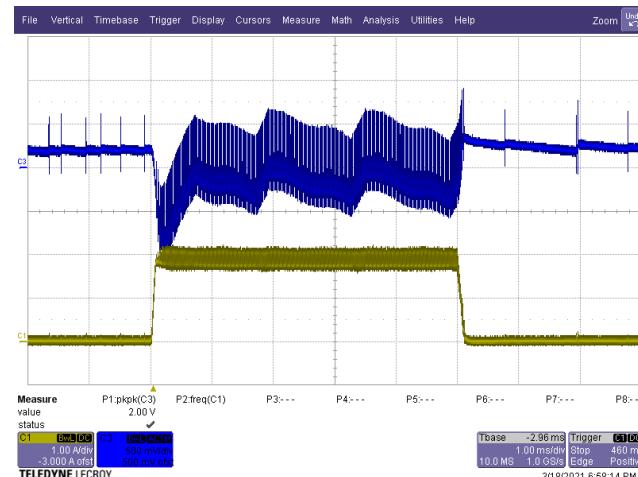


Figure 18 – Transient Response, 264 VAC, 0 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.



11.1.2 10%-100% Load Transient

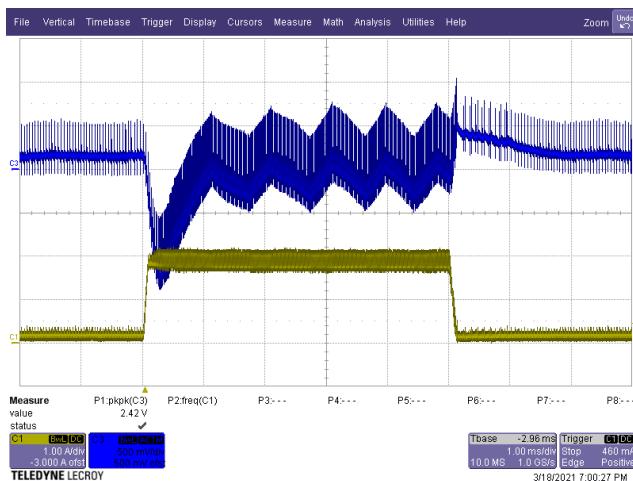


Figure 19 – Transient Response, 160 VAC, 0.2 - 2 A Load Step.
 Upper: V_{OUT} , 500 mV / div.
 Lower: I_{LOAD} , 1 A, 1 ms / div.

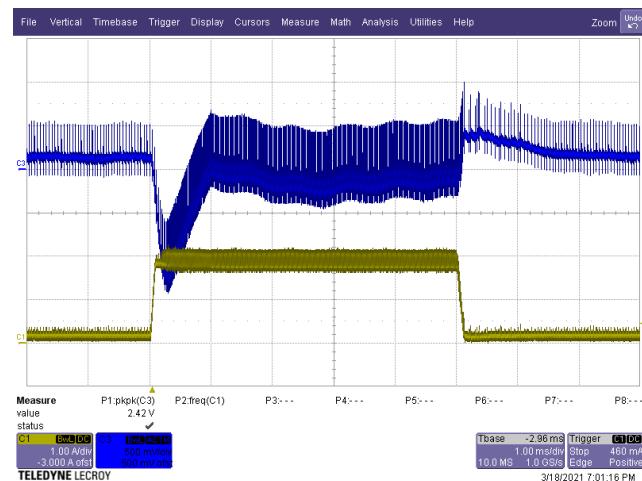


Figure 20 – Transient Response, 180 VAC, 0.2 - 2 A Load Step.
 Upper: V_{OUT} , 500 mV / div.
 Lower: I_{LOAD} , 1 A, 1 ms / div.

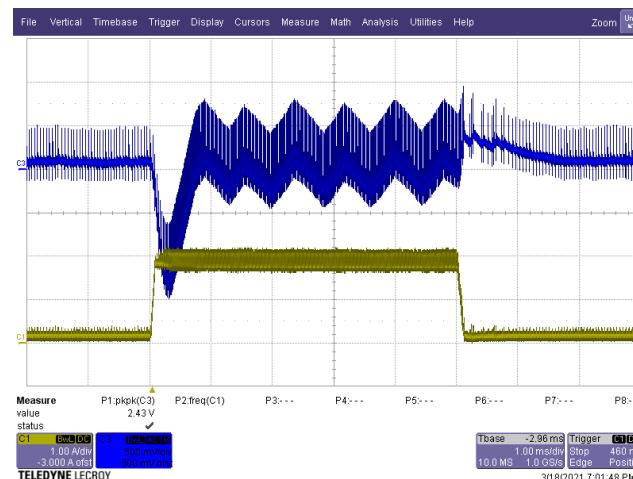


Figure 21 – Transient Response, 160 VAC, 0.2 - 2 A Load Step.
 Upper: V_{OUT} , 500 mV / div.
 Lower: I_{LOAD} , 1 A, 1 ms / div.

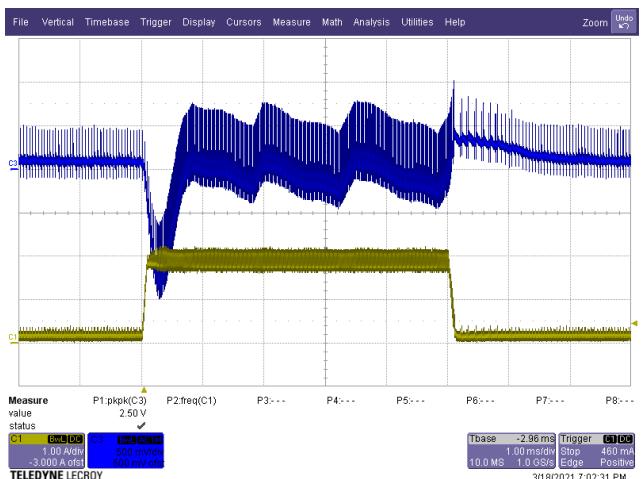


Figure 22 – Transient Response, 180 VAC, 0.2 - 2 A Load Step.
 Upper: V_{OUT} , 500 mV / div.
 Lower: I_{LOAD} , 1 A, 1 ms / div.



11.1.3 50%-100% Load Transient

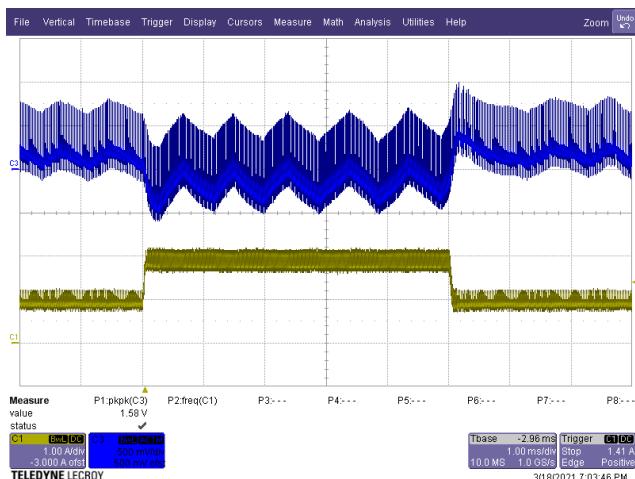


Figure 23 – Transient Response, 160 VAC, 1 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.

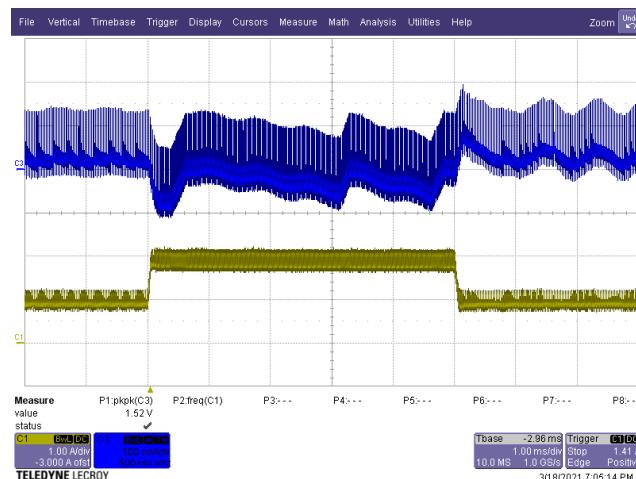


Figure 24 – Transient Response, 180 VAC, 1 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.

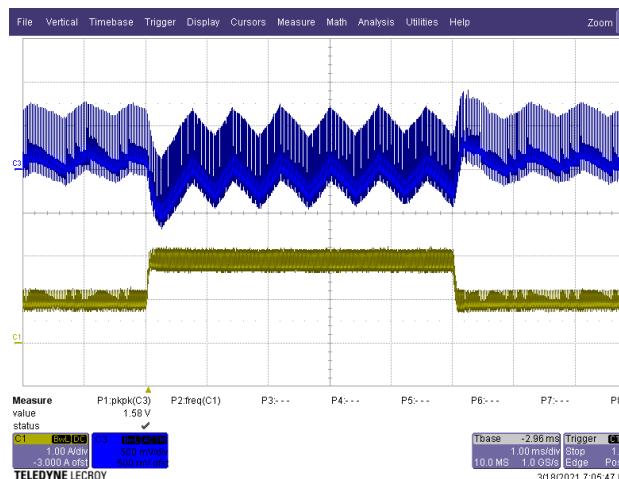


Figure 25 – Transient Response, 230 VAC, 1 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.

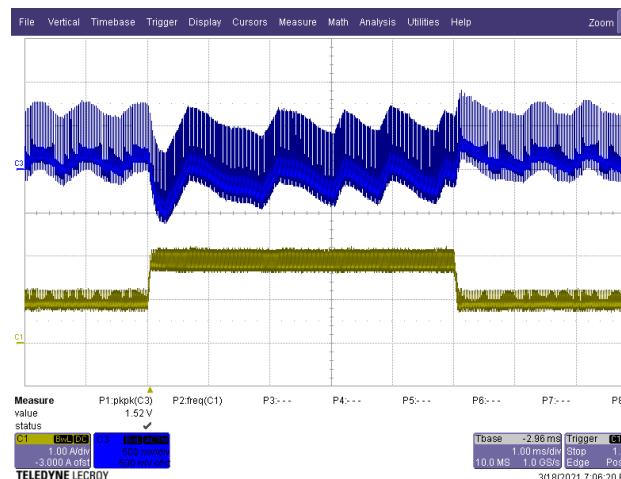


Figure 26 – Transient Response, 264 VAC, 1 - 2 A Load Step.
Upper: V_{OUT} , 500 mV / div.
Lower: I_{LOAD} , 1 A, 1 ms / div.



11.2 *Switching Waveforms*

11.2.1 Primary Drain Voltage and Current



Figure 27 – Flyback Drain Voltage and Current, 160 VAC Input, 2 A Load.
Upper: Drain Voltage, 200 V / div.
Lower: Drain Current, 1 A, 5 μ s / div.



Figure 28 – Flyback Drain Voltage and Current, 180 VAC Input, 2 A Load.
Upper: Drain Voltage, 200 V / div.
Lower: Drain Current, 1 A, 5 μ s / div.



Figure 29 – Flyback Drain Voltage and Current, 230 VAC Input, 2 A Load.
Upper: Drain Voltage, 200 V / div.
Lower: Drain Current, 1 A, 5 μ s / div.

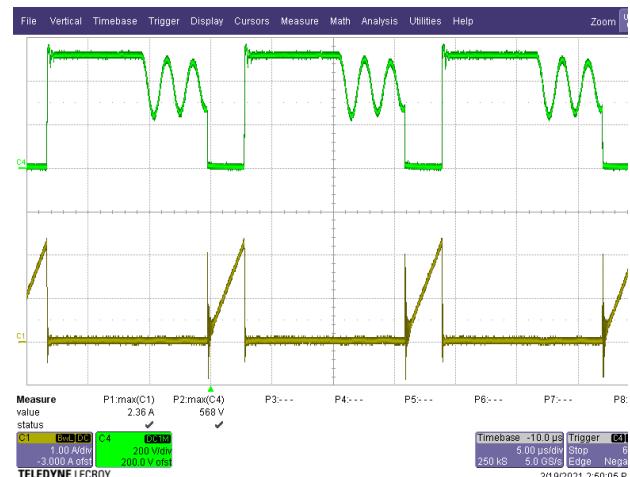
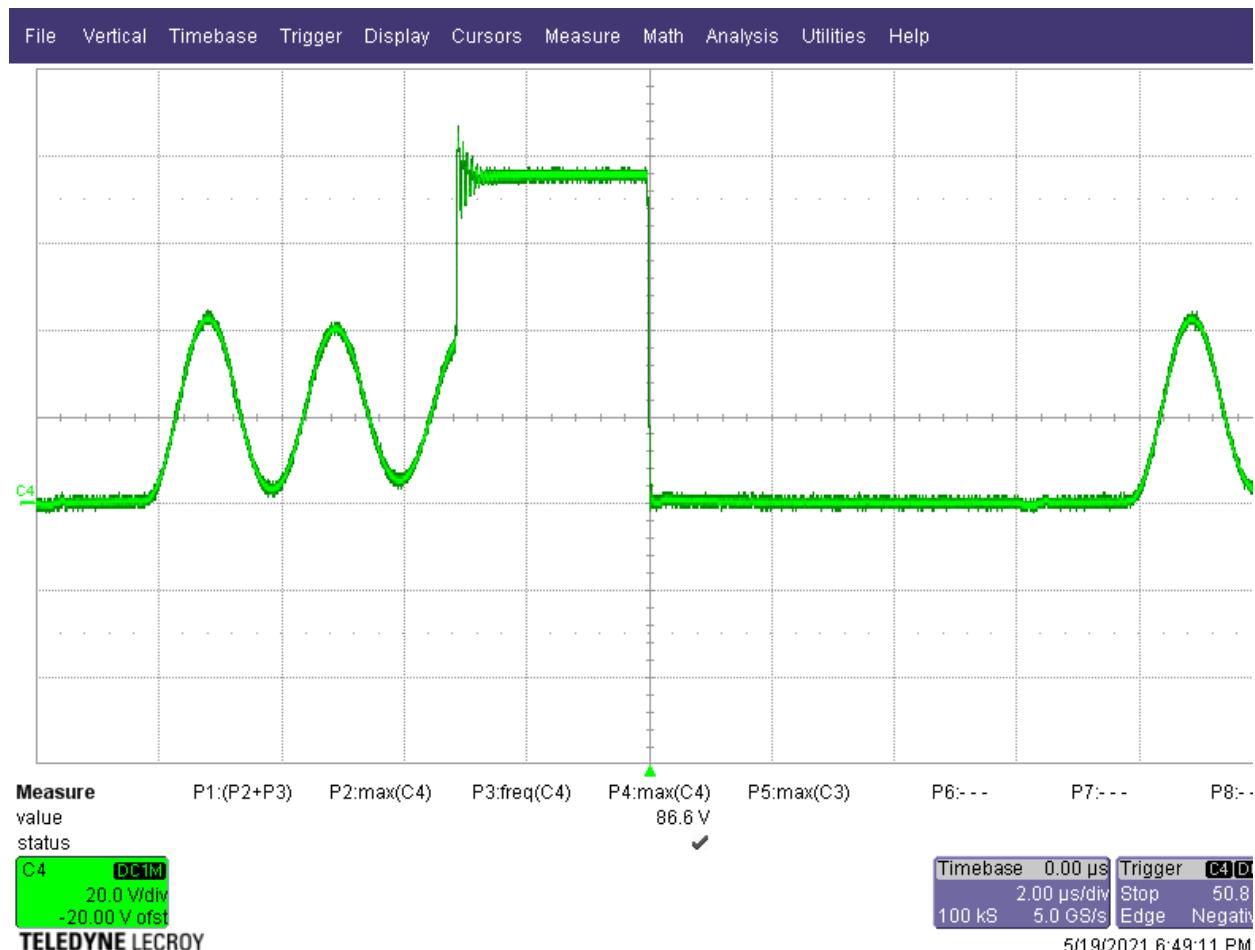


Figure 30 – Flyback Drain Voltage and Current, 264 VAC Input, 2 A Load.
Upper: Drain Voltage, 200 V / div.
Lower: Drain Current, 1 A, 5 μ s / div.



11.2.2 SR FET Voltage

The reading taken is at 264 VAC input, and is worst case, as the power supply runs in DCM over the entire 160-264 VAC input range.



**Figure 31 – SR FET V_{DS} , 264 VAC, 2 A Load.
GRN - SR_VDRAIN, 20 V, 2 μ s / div.**



11.2.3 Diode (D5) Voltage

The reading taken at 264 V represents a worst-case situation as the power supply runs in DCM over the entire 160-264 VAC input range.

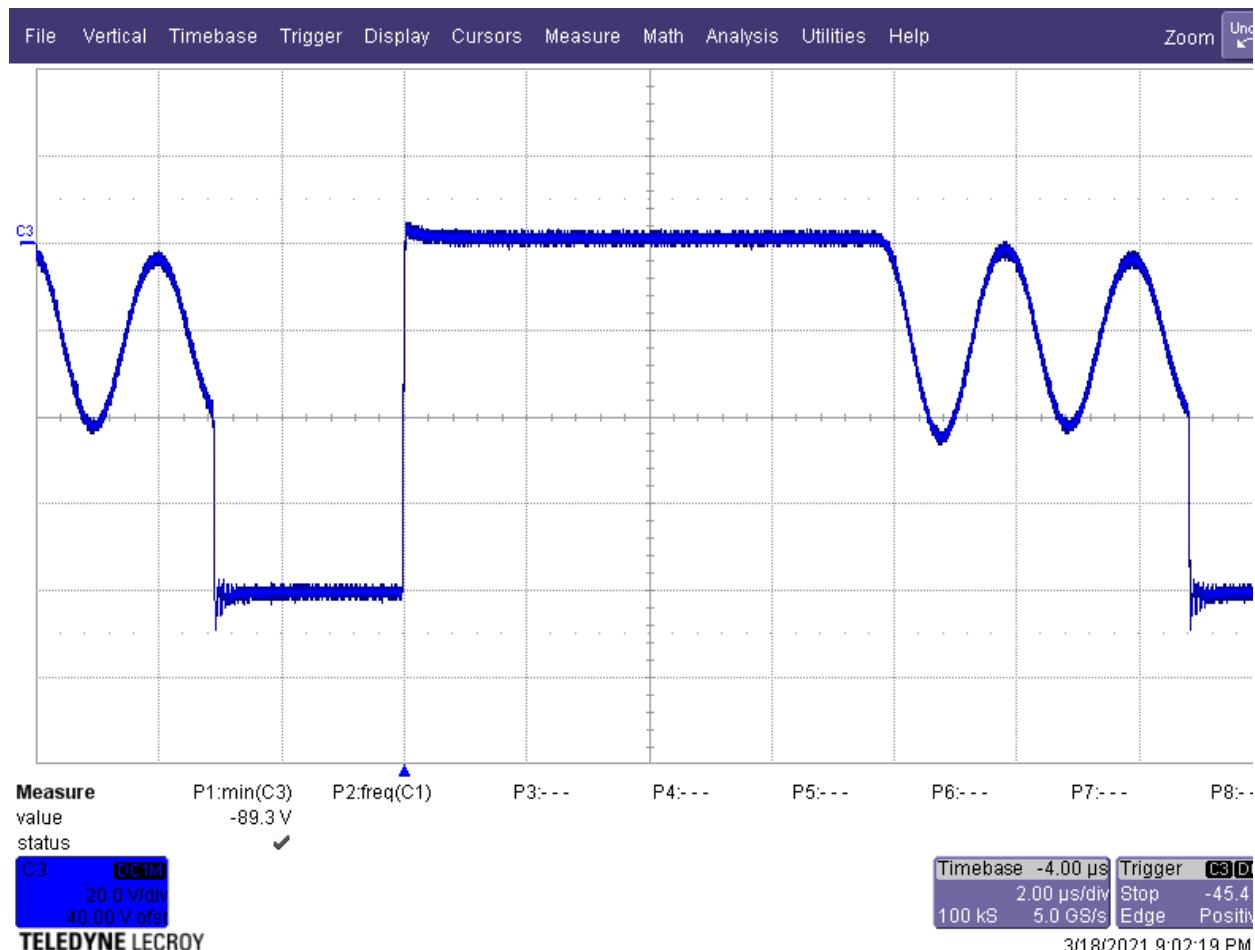


Figure 32 – D5 PIV, 264 VAC, 2 A Load.
Blu – D5 PIV, 20 V / 2 μ s / div.



11.2.4 Flyback Start-up Waveforms

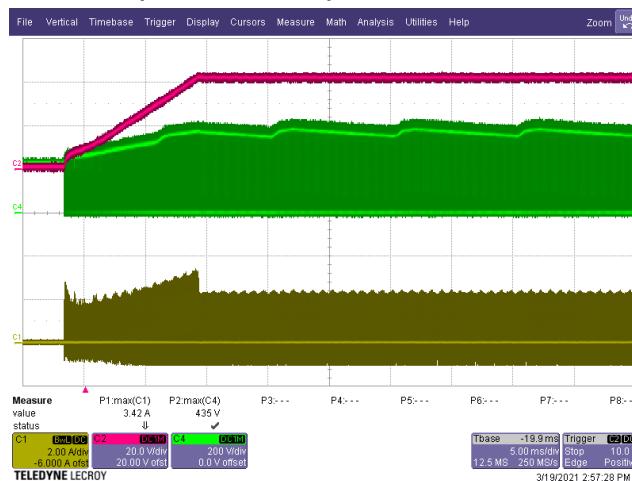


Figure 33 – Flyback Start-up Waveforms, 90 VAC Input, 2 A Load.

Red – V_{OUT} , 20 V / div.

Grn – $U_1 V_{DRAIN}$, 200 V / div.

Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.

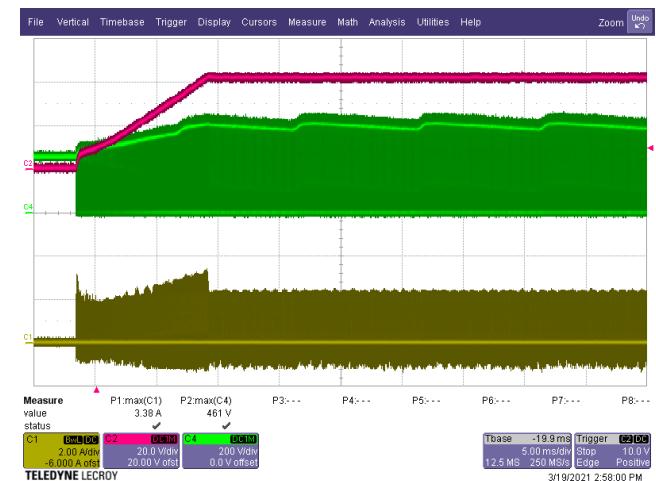


Figure 34 2 – Flyback Start-up Waveforms, 115 VAC Input, 2 A Load.

Red – V_{OUT} , 20 V / div.

Grn – $U_1 V_{DRAIN}$, 200 V / div.

Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.

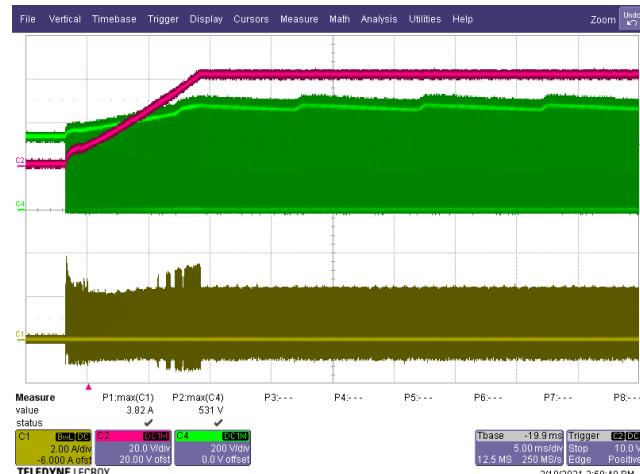


Figure 35 – Flyback Start-up Waveforms, 230 VAC Input, 2 A Load.

Red – V_{OUT} , 20 V / div.

Grn – $U_1 V_{DRAIN}$, 200 V / div.

Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.

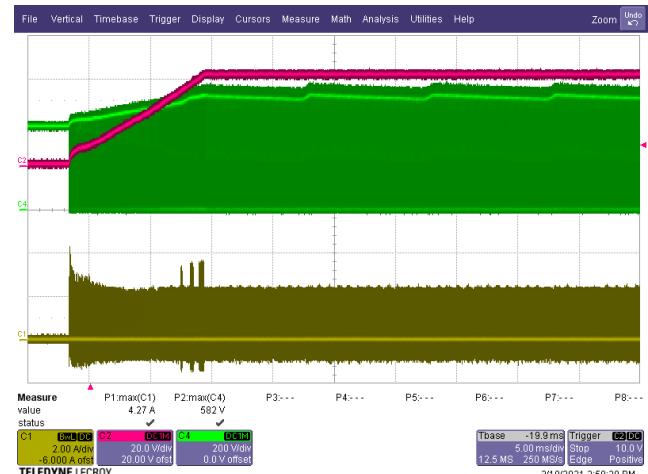


Figure 36 – Flyback Start-up Waveforms, 264 VAC Input, 2 A Load.

Red – V_{OUT} , 20 V / div.

Grn – $U_1 V_{DRAIN}$, 200 V / div.

Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.



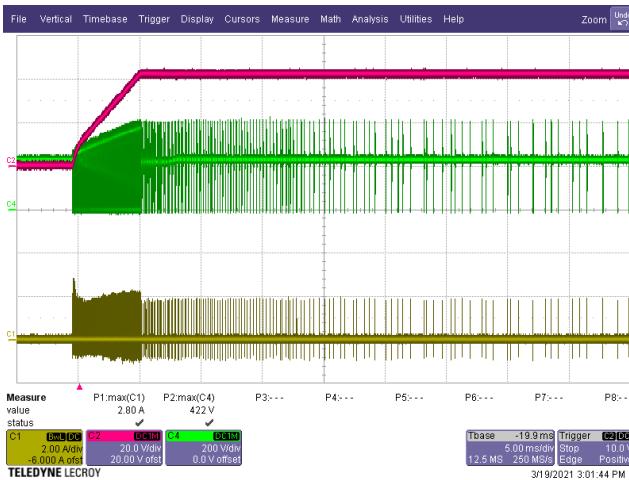


Figure 37 – Flyback Start-up Waveforms, 160 VAC Input, 0 A Load.
 Red – V_{OUT} , 20 V / div.
 Grn – $U_1 V_{DRAIN}$, 200 V / div.
 Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.

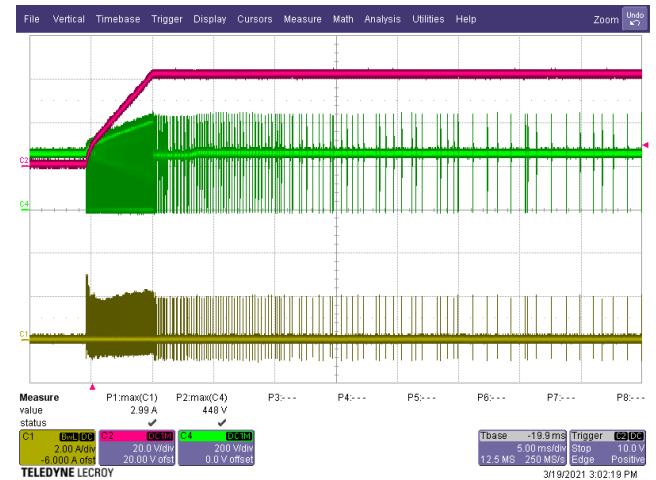


Figure 38 – Flyback Start-up Waveforms, 180 VAC Input, 0 A Load.
 Red – V_{OUT} , 20 V / div.
 Grn – $U_1 V_{DRAIN}$, 200 V / div.
 Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.

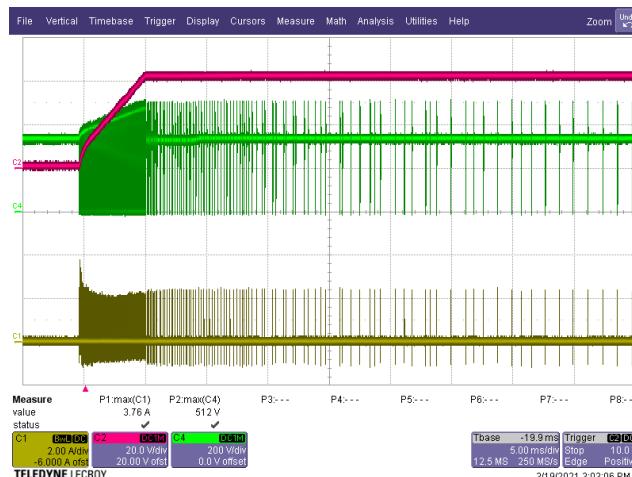


Figure 39 – Flyback Start-up Waveforms, 230 VAC Input, 0 A Load.
 Red – V_{OUT} , 20 V / div.
 Grn – $U_1 V_{DRAIN}$, 200 V / div.
 Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.

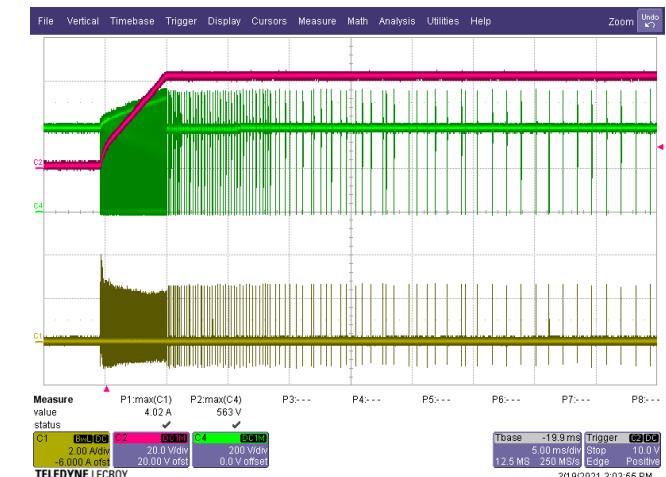


Figure 40 – Flyback Start-up Waveforms, 264 VAC Input, 0 A Load.
 Red – V_{OUT} , 20 V / div.
 Grn – $U_1 V_{DRAIN}$, 200 V / div.
 Yel – $U_1 I_{DRAIN}$, 2 A, 5 ms / div.



11.3 ***Output Ripple Measurements***

11.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF /50 V ceramic type and one (1) 47 μF /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

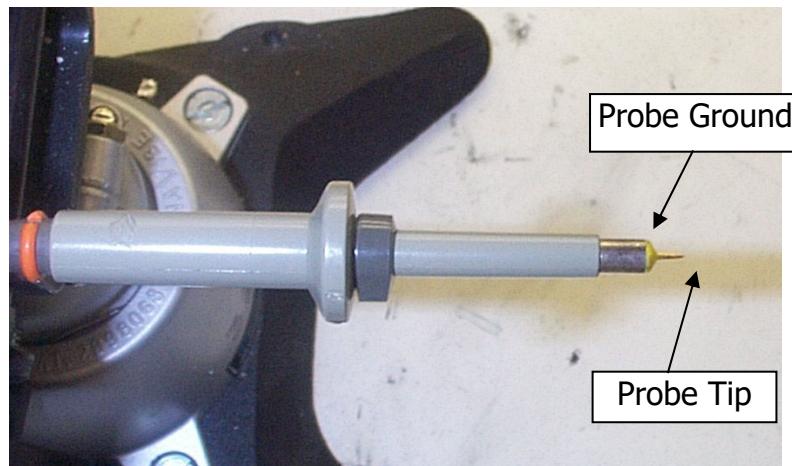


Figure 41 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

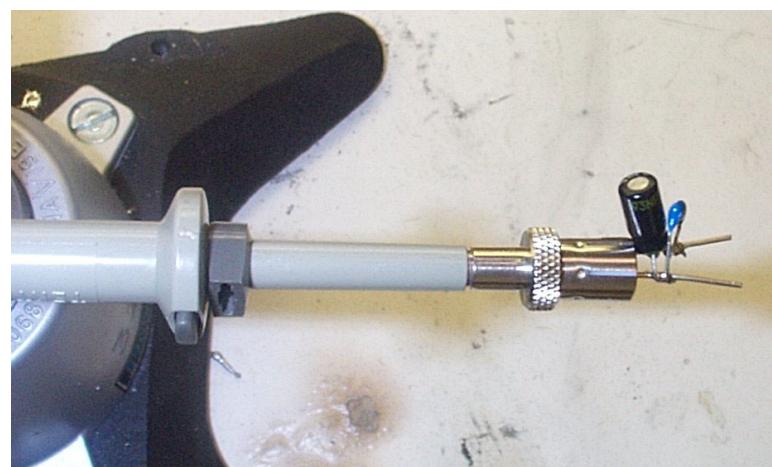
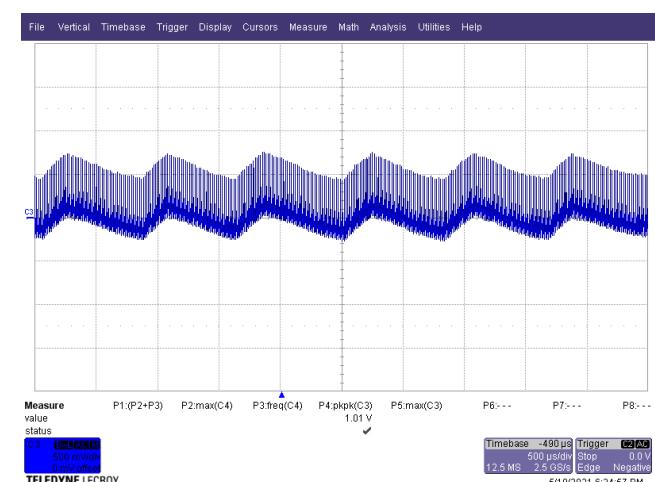
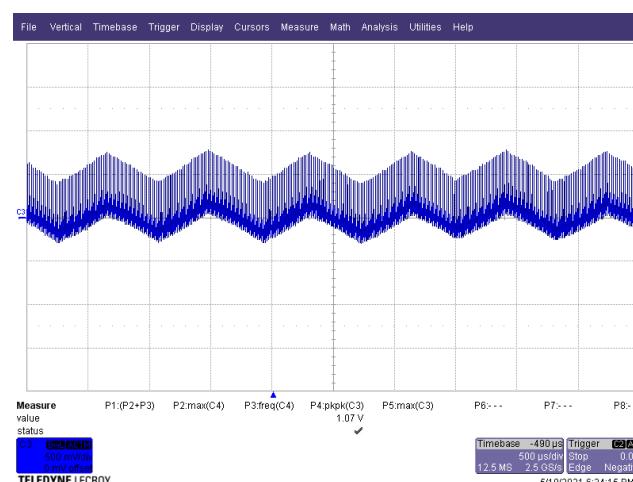
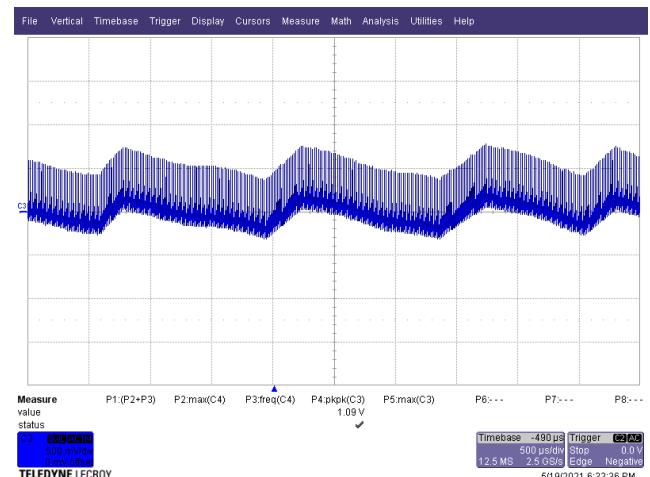
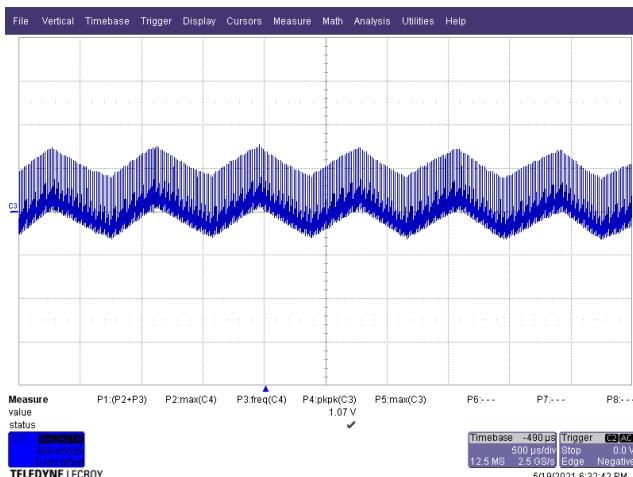


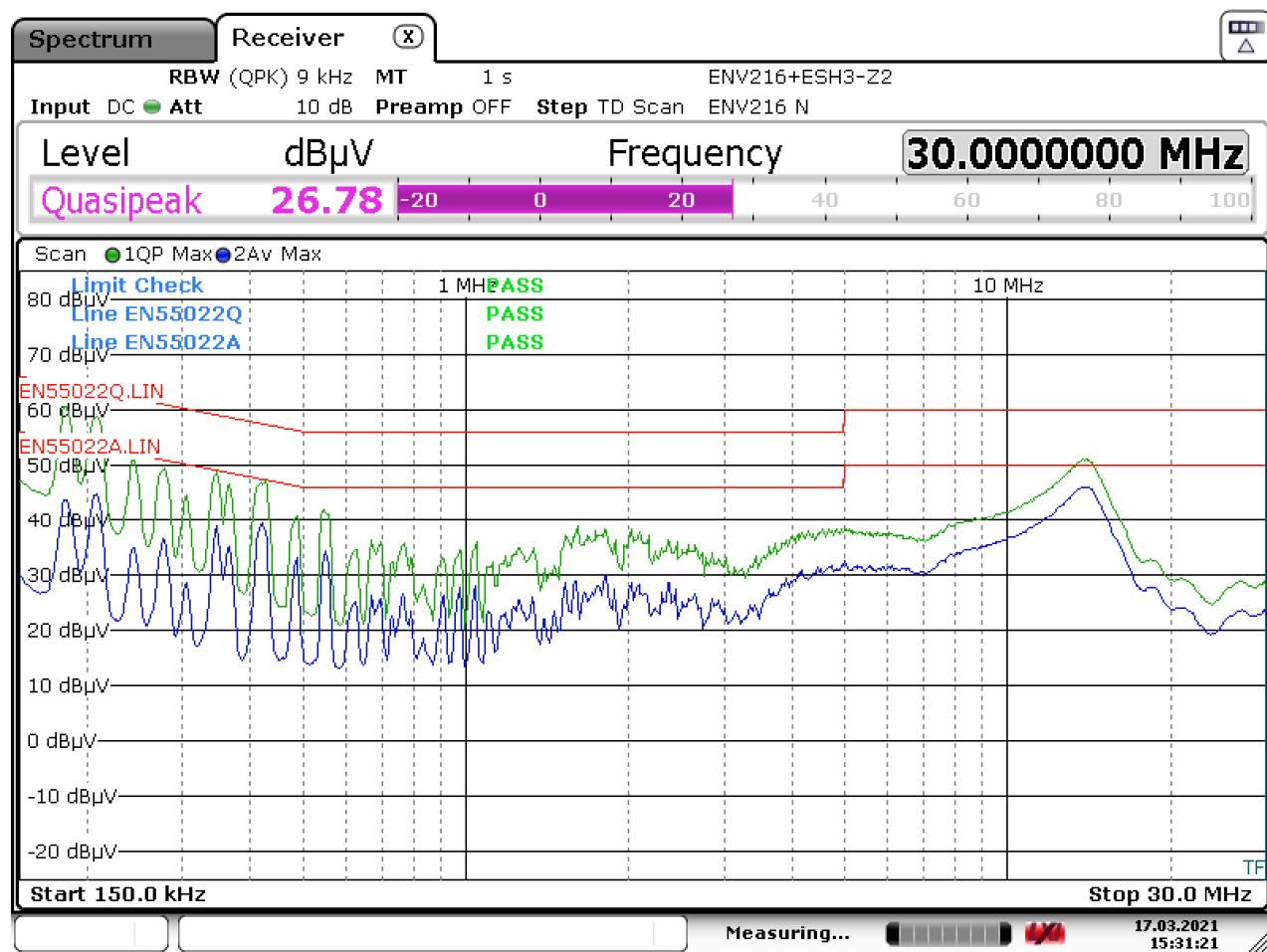
Figure 42 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter.
(Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.3.1.1 Output Ripple waveforms



12 Conducted EMI

EMI scans were made using an 21Ω resistive load, with the output return grounded to the LISN.



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Figure 47 – EMI, Full Load, 230 VAC, LISN Grounded to Secondary Return.



13 Line Surge

13.1 Combination Wave Differential Mode Test

Pass criterion is no output interruption.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+1	90	2	10	PASS
230	-1	90	2	10	PASS
230	+1	270	2	10	PASS
230	-1	270	2	10	PASS
230	+1	0	2	10	PASS
230	-1	0	2	10	PASS

13.2 Combination Wave Common Mode Test

PE grounded to secondary return - pass criterion is no output interruption.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS



14 ESD

Pass criterion is no permanent output interruption.

14.1 *Air Discharge*

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	+15	Output +	10	PASS
230	-15	Output +	10	PASS
230	+15	Output -	10	PASS
230	-15	Output -	10	PASS

14.2 *Contact Discharge*

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	+8.8	Output +	10	PASS
230	-8.8	Output +	10	PASS
230	+8.8	Output -	10	PASS
230	-8.8	Output -	10	PASS



15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
17-Mar-21	RH	1.0	Initial Release.	Apps & Mktg
23-Jul-21	KM	1.1	Minor Formatting Change	Mktg



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