Design Example Report

Title	***6 W Dual Output Power Supply with Low No-Load Input Power (<5 mW), Non-Isolated Flyback, Using InnoSwitch™3-TN INN3072M***
Specification	85 VAC – 265 VAC Input 5 V, 0.9 A and 12 V, 0.13 A Outputs
Application	Open Frame Appliance Power Supply
Author	Applications Engineering Department
Document Number	DER-959
Date	April 6, 2022
Revision	1.0

Summary and Features

- 6 W output from 85 VAC to 265 VAC
- Built in synchronous rectification for >84 % efficiency at nominal AC input
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- <5 mW no-load input power at 230 VAC input
- <200 mW standby input power at 5 V / 30 mA load
- Accurate thermal protection with hysteretic shutdown

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 0.9 A, 5 V and 0.13 A, 12 V non-isolated dual output embedded power supply utilizing INN3072M from the InnoSwitch3-TN family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

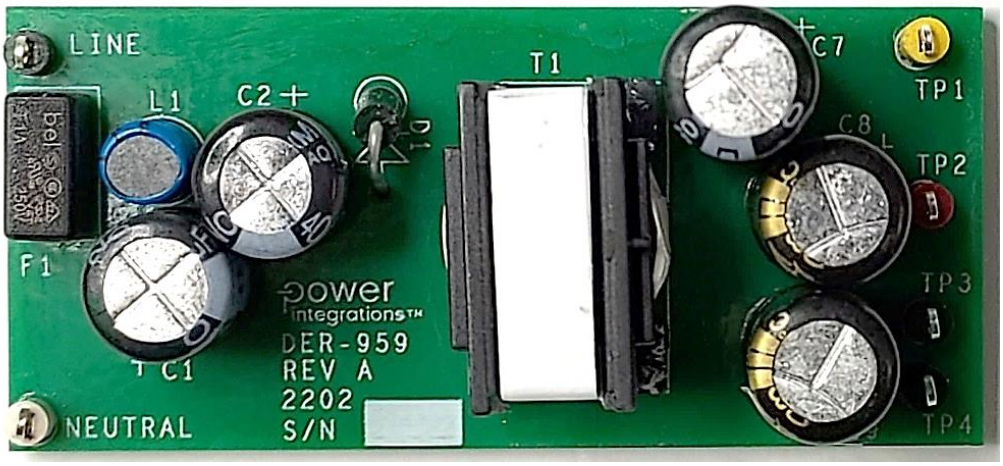


Figure 1 – Populated Circuit Board Photograph, Top.

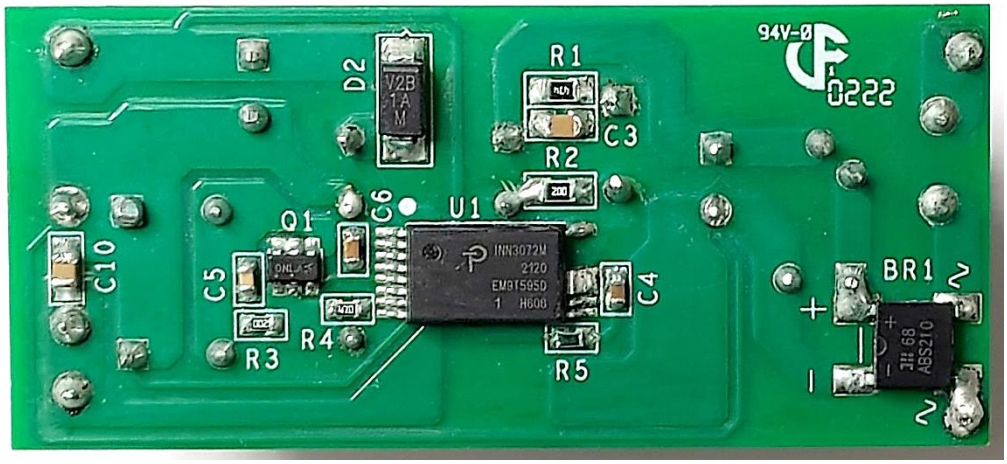


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115/230	265	VAC	2 Wire Input.
Frequency	f_{LINE}		50/60		Hz	
No-Load Input Power				5	mW	@ 230 VAC Input.
Standby Power (5 V / 30 mA)			200	300	mW	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5 %
Output Ripple Voltage 1	$V_{RIPPLE1}$			200	mV	20 MHz Bandwidth. <150 mV_{PP} at Room Temperature.
Output Current 1	I_{OUT1}	0	0.9		A	
Output Voltage 2	V_{OUT2}	9.6	12	14.4	V	±20 %,
Output Ripple Voltage 2	$V_{RIPPLE2}$			250	mV	20 MHz Bandwidth. <200 mV_{PP} at Room Temperature.
Output Current 2	I_{OUT2}	0	0.13		A	
Total Output Power						
Continuous Output Power	P_{OUT}			6	W	
Efficiency						
Average 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	85			%	Measured at 115 / 230 VAC, Room Temperature.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B Load Floating				Measured at 115 / 230 VAC
Safety		Designed to meet IEC950, UL1950 Class II				
Surge						
Differential		1			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω.
Ring Wave		6			kV	100 kHz Ring Wave, 12 Ω Common Mode.
EFT		4			kV	15 ms @ 5kHz. 0.75 ms @ 100kHz.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

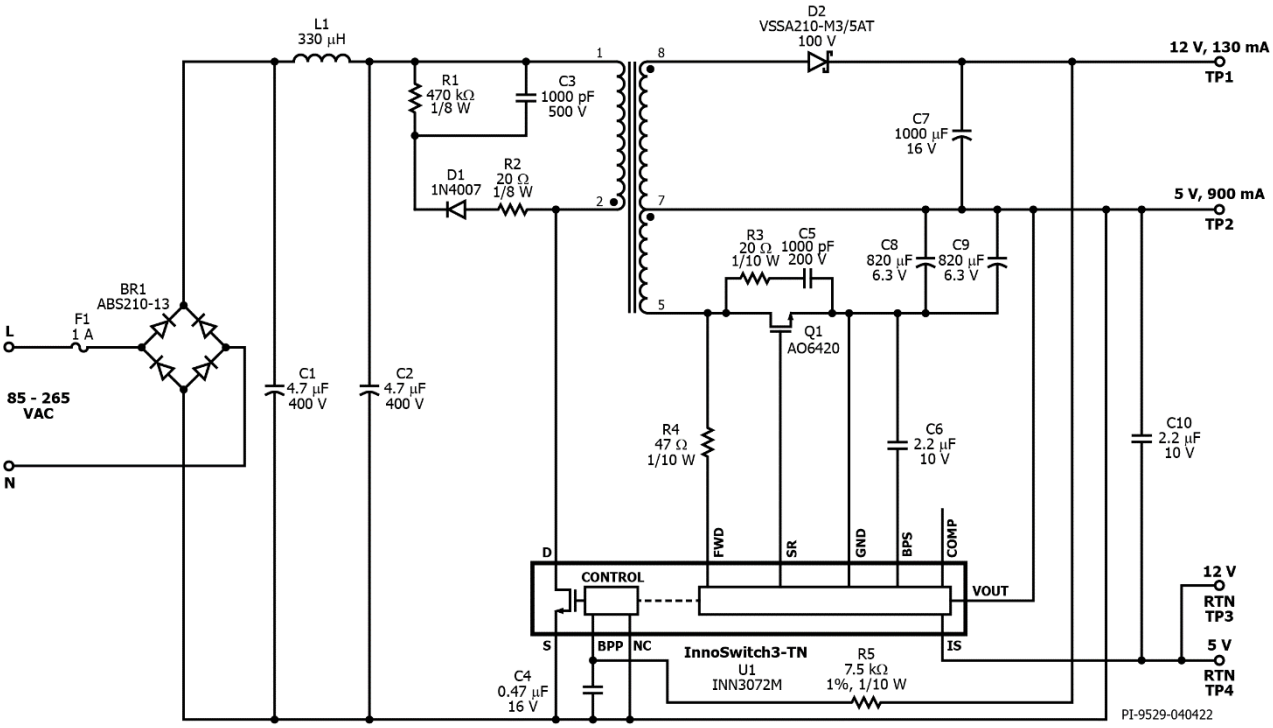


Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C1 and C2. The differential inductance of L1 with capacitors C1 and C2 provide differential noise filtering.

It is necessary to increase the size of both input capacitors, C1 and C2, to 15 μF and add thermistor RT1 to pass differential, ring wave and EFT surge tests.

4.2 *InnoSwitch3-TN Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the InnoSwitch3-TN IC (U1).

A low cost RCD clamp formed by D1, R2, R1, and C3 limits the peak drain voltage due to the effects of transformer leakage inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when AC is first applied. During normal operation the primary side block is powered from 12 V output. The 12 V output is fed in the BPP pin via current limiting resistor R5 with the primary Source connected to 5V output, the equivalent bias voltage is 7 V.

4.3 *InnoSwitch3-TN IC Secondary*

The secondary-side of the InnoSwitch3-TN IC provides output voltage, output current sensing and gate drive for a MOSFET providing synchronous rectification. For the secondary winding of the transformer, center-tapped configuration was used.

Output rectification for the 5 V output is provided by SR FET Q1. Low ESR capacitors C8, C9 and ceramic capacitor C10, provides filtering and significantly attenuates the high frequency ripple and noise at the 5 V output.

Output rectification for the 12 V output is provided by Schottky diode D2. Low ESR capacitor C7 provides filtering and significantly attenuates the high frequency ripple and noise at the 12 V output.

RC snubber network comprising R3 and C5 connected to MOSFET Q1 helps reduce high frequency ringing during switching transient, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gate of Q1 is turned on based on the winding voltage sensed via R4 and the FWD pin of the IC. In discontinuous mode the MOSFET is turned off when the voltage drop across

the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary-side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VOUT pin and charges the decoupling capacitor C6 and an internal regulator.

This IC regulates the output voltage to 5 V through VOUT pin and internal feedback divider network.

5 PCB Layout

PCB - 1 Layer BOTTOM, FR4, 2oz Copper, 0.062" Thickness unless otherwise stated.

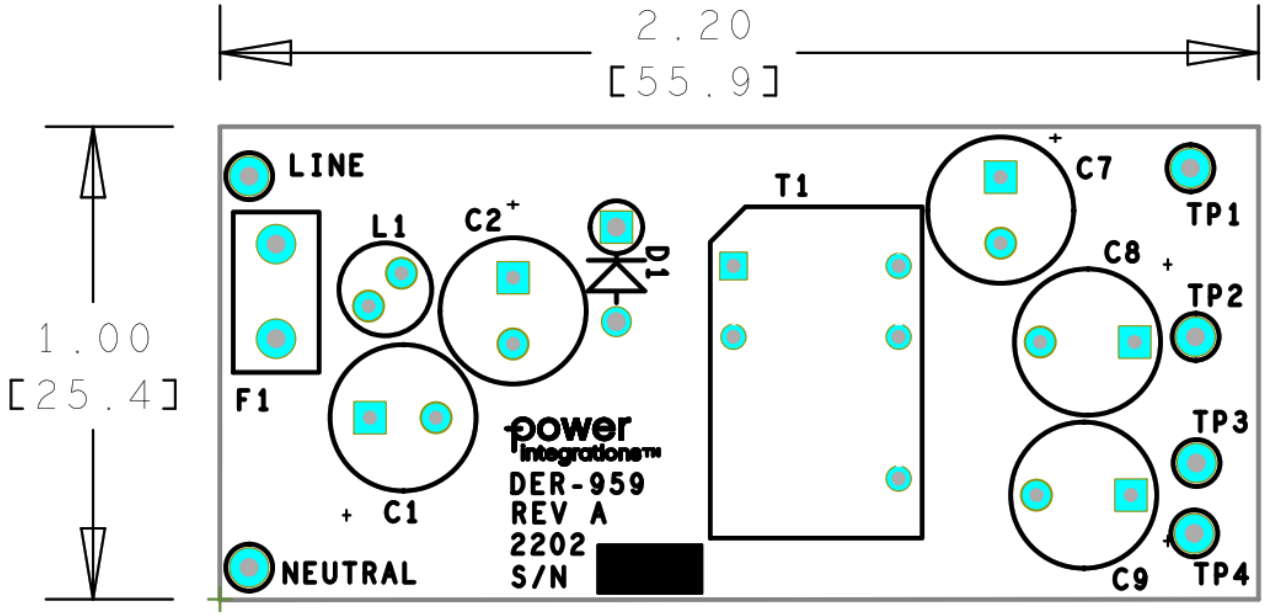


Figure 4 – Printed Circuit Layout, Top Side.

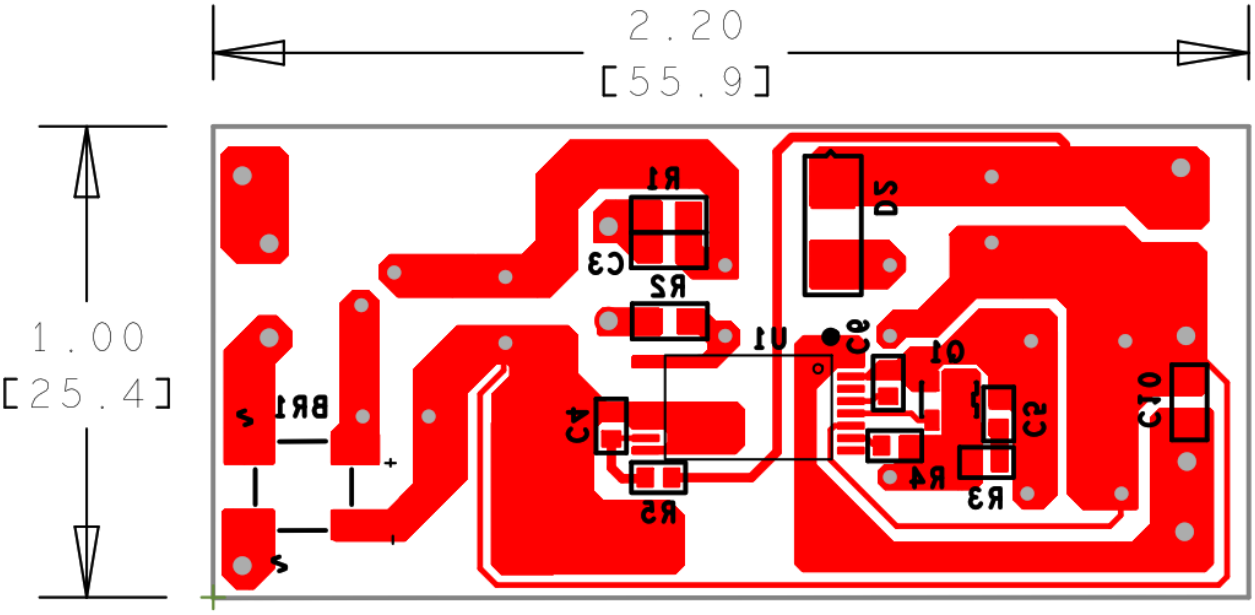


Figure 5 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	BRIDGE RECT, 1PH, 1 kV, 2 A, 4SOPA, SMD	ABS210-13	Diodes, Inc.
2	2	C1 C2	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G4R7MK0811MLL3	Taicon
3	1	C3	1000 pF, 10%, 500 V, Ceramic, X7R, 0805	C0805C102KCRACTU	Kemet
4	1	C4	0.47 μF, 10%, 16 V, X7R, 0603	GRM188R71C474KA88D	Murata
5	1	C5	1000 pF, 200 V, Ceramic, X7R, 0603	06032C102KAT2A	AVX
5 Alt.	1	C5 Alt.	1000 pF ±5% 200V Ceramic X7R 0603	06032C102JAT2A	AVX
6	1	C6	2.2 μF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
7	1	C7	1000 μF, 16 V, Electrolytic, Low ESR, (8 x 20)	EEU-FR1C102LB	Panasonic
8	2	C8 C9	820 μF, 6.3 V, Aluminum Electrolytic Radial, Can - 3000 Hrs @ 105 °C (8 x 16.5)	EEU-FM0J821L	Panasonic
9	1	C10	2.2 μF ±10% 25 V Ceramic X7R 0805	GCM21BR71E225KA73L	Murata
9 Alt.	1	C10 Alt.	2.2 μF ±10% 10 V Ceramic X7R 0805	C0805C225M8RACTU	Kemet
10	1	D1	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
10 Alt.	1	D1 Alt.	Diode Standard 1000 V 1A Through Hole DO-204AL (DO-41)	1N4007G A0G	Taiwan Semi
11	1	D2	Diode Schottky 100 V 1.7A SMT DO-214AC (SMA)	VSSA210-M3/5AT	Vishay
12	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
13	1	L1	330 μH, 0.34 A, 5.5 x 10.5 mm	SBC1-331-341	Tokin
14	3	LINE TP3 TP4	Test Point, BLK, Miniature TH MOUNT	5001	Keystone
15	1	NEUTRAL	Test Point, WHT, Miniature TH MOUNT	5002	Keystone
16	1	Q1	MOSFET, N-CH, 60 V, 4.2 A, 6TSOP	AO6420	Alpha & Omega Semi
17	1	R1	RES, 470 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ474V	Panasonic
18	1	R2	RES, 20 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ200V	Panasonic
19	1	R3	RES, 20 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ200V	Panasonic
20	1	R4	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
20 Alt.	1	R4 Alt.	RES, 47 Ω, ±1%, 1/10 W, Chip Resistor 0603, Moisture Resistant Thick Film	RC0603FR-0747RL	YAGEO
21	1	R5	RES, 7.5 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF7501V	Panasonic
22	1	T1	Bobbin,Vertical, EF16, 8 Pins, mates with core 99-00063-00	B66308W1108T001	TDK
23	1	TP1	Test Point, PC MINI, .040"(1.02 mm)D, YELLOW, TH MOUNT	5004	Keystone
24	1	TP2	Test Point, RED, Miniature TH MOUNT	5000	Keystone
25	1	U1	InnoSwitch3-TN, MinSOP-16	INN3072M	Power Integrations

7 Transformer Specification

7.1 *Electrical Diagram*

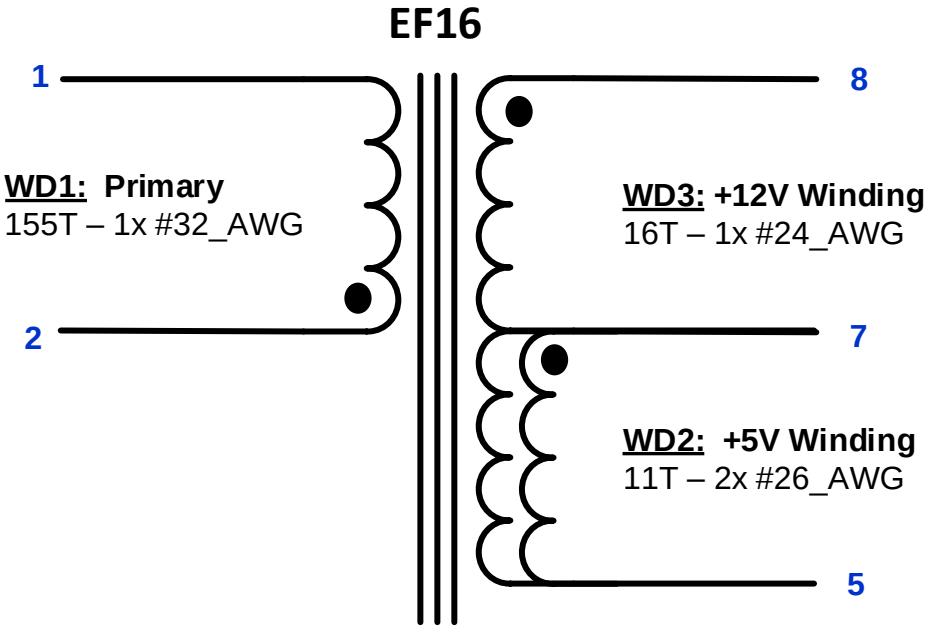


Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Specification
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	1731 µH ±5%
Primary Leakage Inductance	Between pin 1 and 2, with pins: 5, 7 & 8 shorted.	53 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EF16 – N87, PI#: 99-00063-00; or Equivalent.
[2]	Bobbin: EF16-Vert-8pins (4/4); PI#: 25-01138-00.
[3]	Magnet Wire: #32 AWG, Double Coated.
[4]	Magnet Wire: #26 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Double Coated.
[6]	Tape: 3M Scotch, Polyweb, 3.2 mm; or Equivalent.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 3.3 mm Width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 10.0 mm Width.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 4.5 mm Width.
[10]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

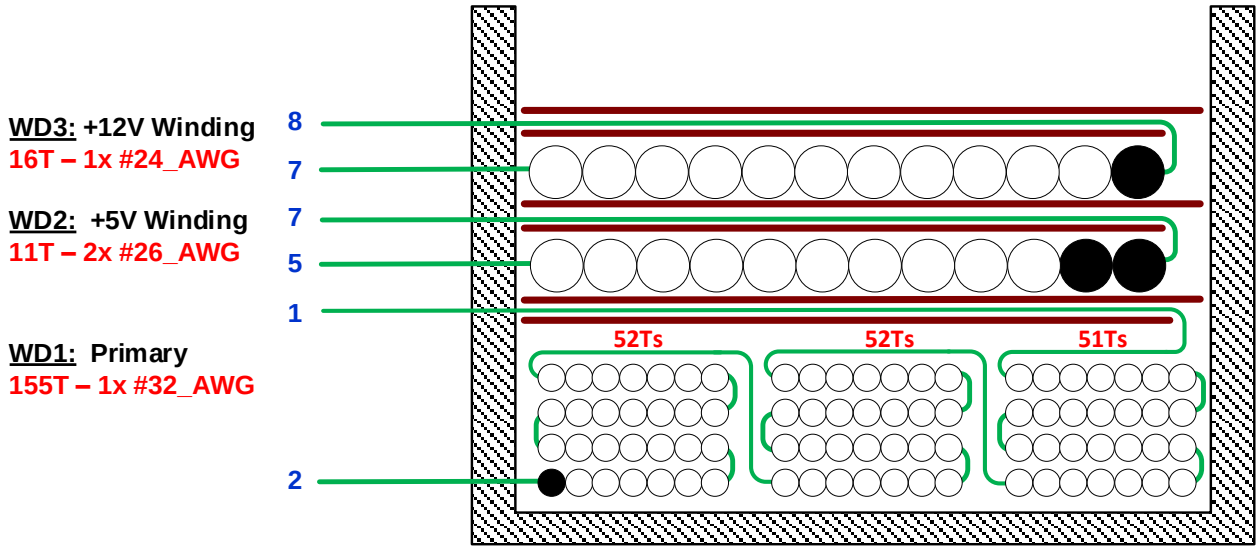
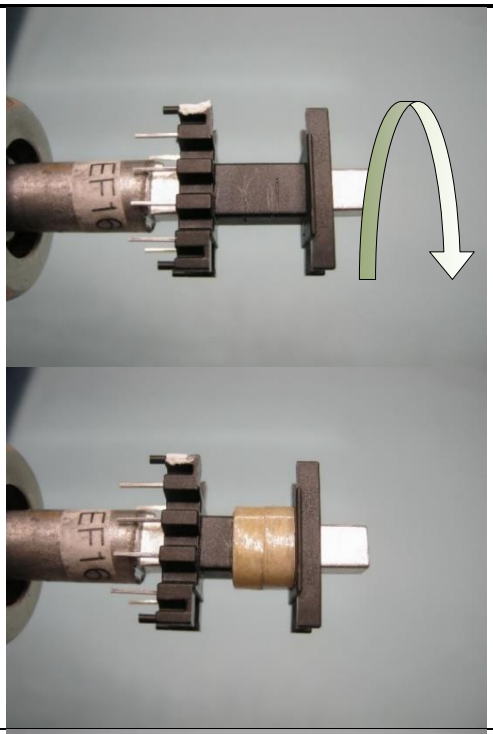
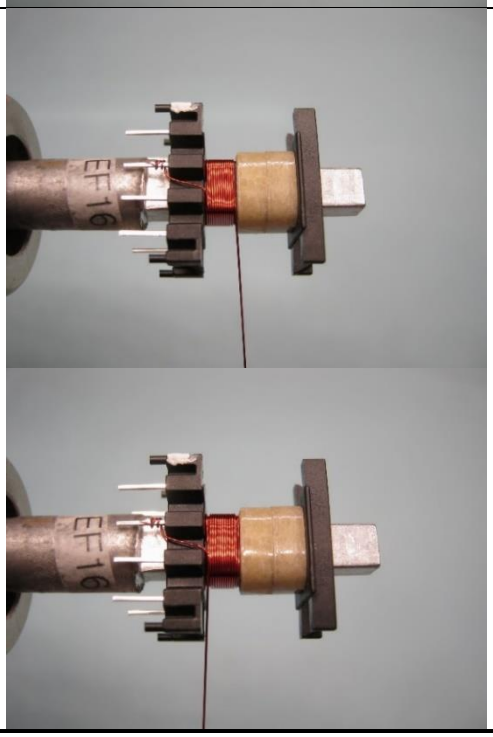


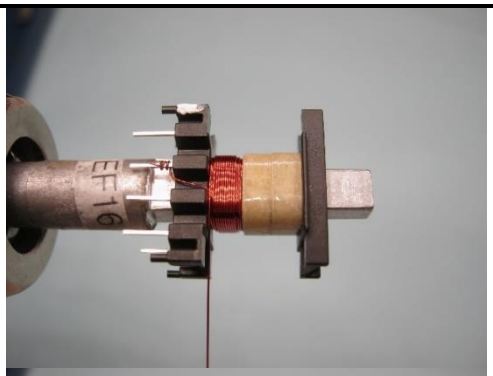
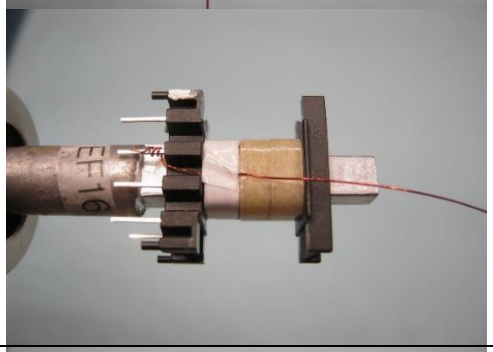
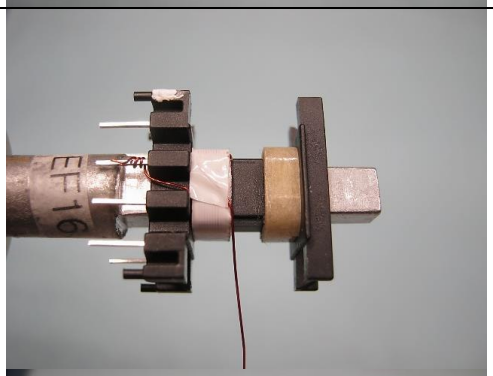
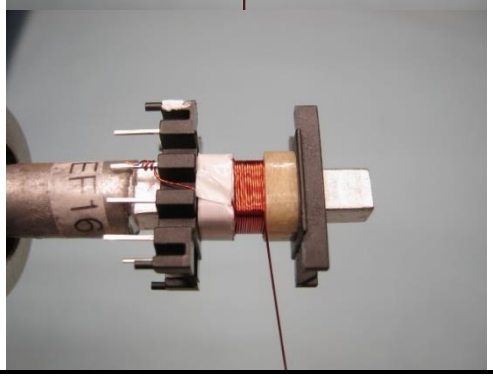
Figure 7 – Transformer Electrical Diagram.

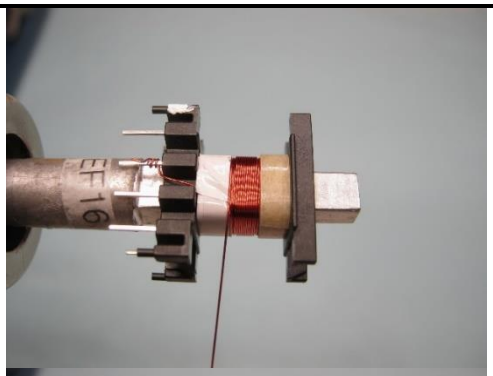
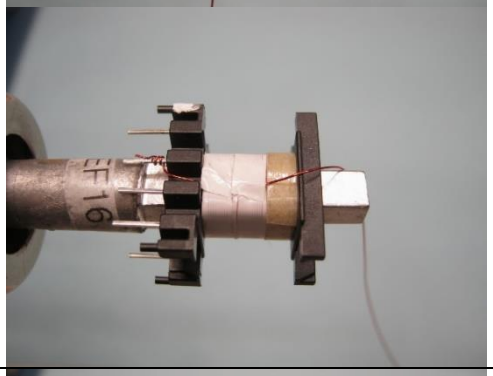
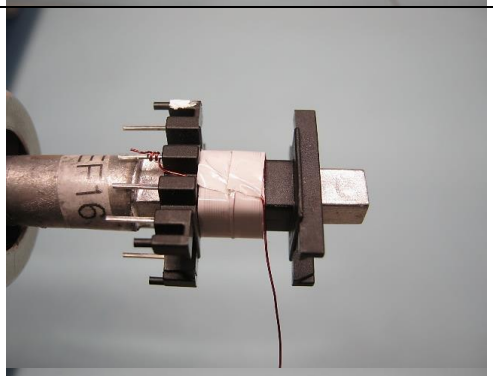
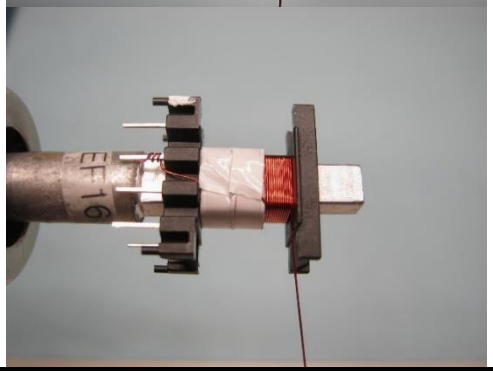
7.5 *Winding Instructions*

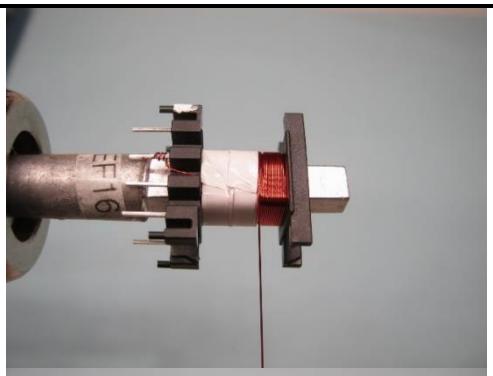
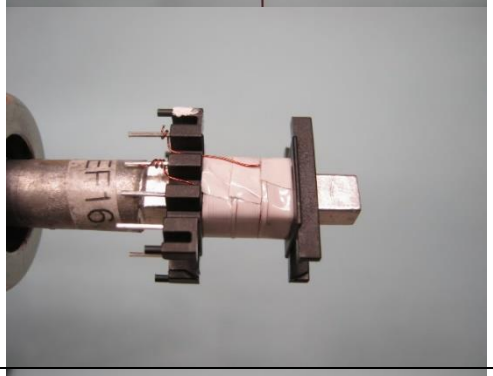
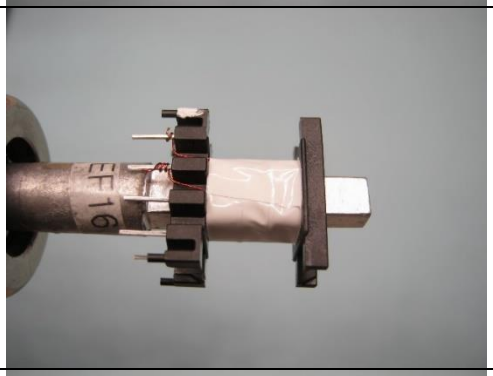
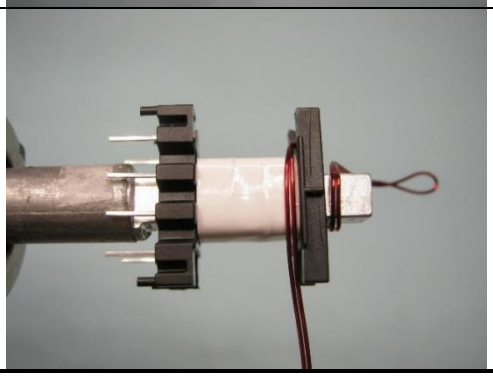
Winding Preparation	Position the bobbin Item [2] on the mandrel such that the pin-side of the bobbin is on the left side. Winding direction is clockwise direction. Make 2 stack of margin tape Item [6] on the right and the middle of bobbin width, so there is an empty chamber for the 1st winding of Primary winding (see pictures below).
WD1 Primary	Start at pin 2, for 1st winding of Primary winding, wind 52 turns of wire Item [3] in 4 layers, from left to right then right to left in the empty chamber. At the last turn, place 1 layer of tape Item [7] to hold this winding. Remove middle stack of margin tape, continue winding another 52 turns the same way as previous winding in the middle chamber, also place 1 layer of tape Item [7] to hold this winding – 2nd winding of Primary winding. Remove right stack of margin tape, repeat for another 51 turns for 3rd winding of Primary winding. At the last turn bring the wire back to left to terminate at pin 1 and 1 layer of tape Item [7] for this winding.
Insulation	1 layer of tape Item [8].
WD2: +5 V Winding	Use 2 wires Item [4] leaving 20 mm floating, start from the right of bobbin, wind 11 bi-filar turns to the left and terminate at pin 5 for the end of wires. Bring floating end of wires to the left to terminate at pin 7.
Insulation	1 layer of tape Item [8].
WD2: +12 V Winding	Use wire Item [5] leaving 20 mm floating, start from the right of bobbin, wind 16 turns to the left and terminate at pin 7 for the end of wire. Bring floating end of wire to the left to terminate at pin 8.
Insulation	2 layers of tape Item [8].
Finish	Gap core halves to get inductance 1731 μH. Secure the core with Item [9]. Varnish with Item [10].

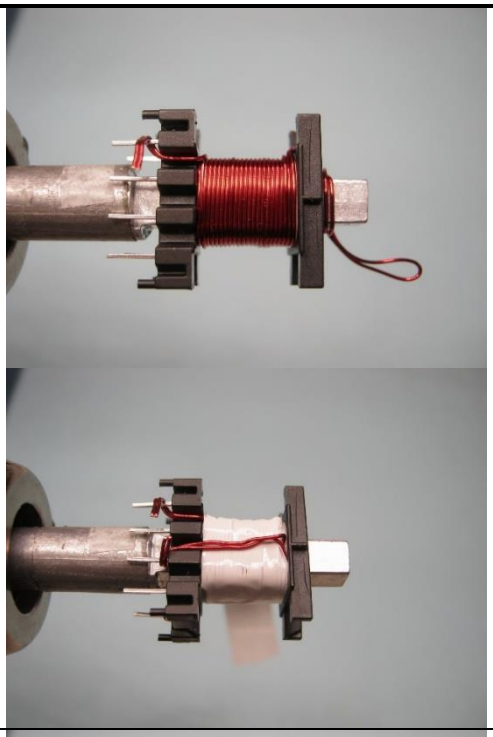
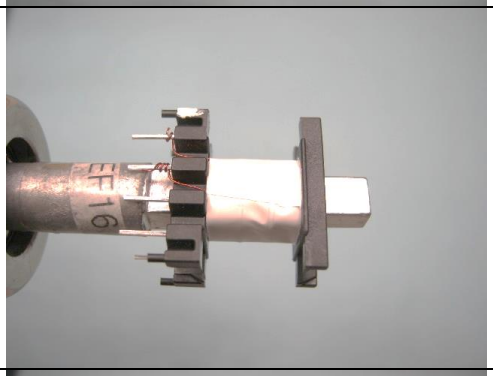
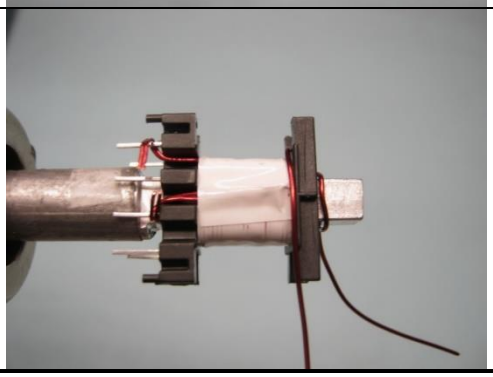
7.6 *Winding Illustrations*

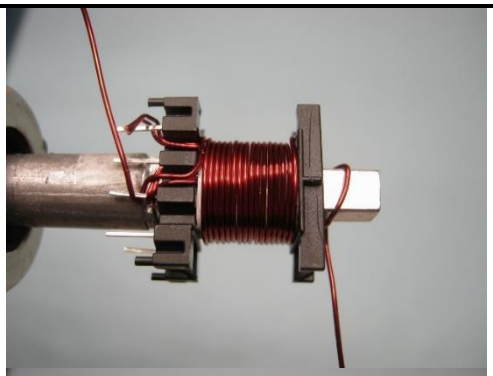
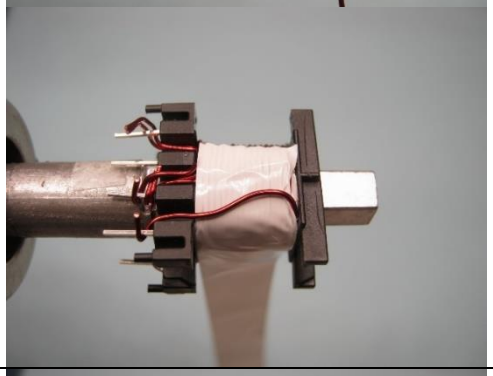
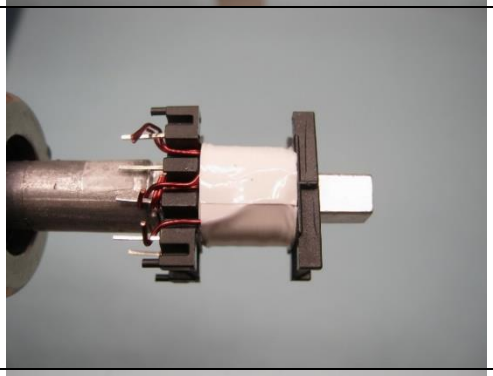
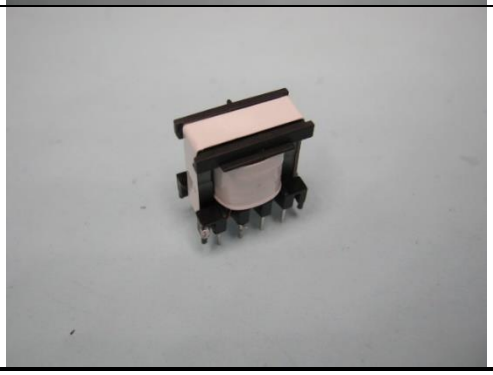
Winding Preparation		Position the bobbin Item [2] on the mandrel such that the pin-side of the bobbin is on the left side. Winding direction is clockwise direction. Make 2 stack of margin tape Item [6] on the right and the middle of bobbin width, so there is an empty chamber for the 1st winding of Primary winding.
WD1 **Primary – 1st winding**		Start at pin 2, for 1st winding of Primary winding, wind 52 turns of wire Item [3] in 4 layers, from left to right then right to left in the empty chamber. At the last turn, place 1 layer of tape Item [7] to hold this winding.

	 	
WD1 **Primary – 2nd winding**	 	Remove middle stack of margin tape, continue winding another 52 turns the same way as previous winding in the middle chamber, also place 1 layer of tape Item [7] to hold this winding – 2nd winding of Primary winding.

	 	
WD1 **Primary – 3rd winding**	 	Remove right stack of margin tape, repeat for another 51 turns for 3rd winding of Primary winding. At the last turn bring the wire back to left to terminate at pin 1 and 1 layer of tape Item [7] for this winding.

	 	
Insulation		1 layer of tape Item [7].
WD2: +5 V Winding		Use 2 wires Item [4] leaving 20 mm floating, start from the right of bobbin, wind 11 bi-filar turns to the left and terminate at pin 5 for the end of wires. Bring floating end of wires to the left to terminate at pin 7.

		
Insulation		1 layer of tape Item [8].
WD2: +12 V Winding		Use wire Item [5] leaving 20 mm floating, start from the right of bobbin, wind 16 turns to the left and terminate at pin 7 for the end of wire. Bring floating end of wire to the left to terminate at pin 8.

	 	
Insulation		2 layers of tape Item [8].
Finish		Gap core halves to get inductance 1731 μH. Secure the core with Item [9]. Varnish with Item [9].

8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-TN_Flyback_030222; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 TN Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VIN_MIN			85	V	Minimum AC input voltage
4	VIN_MAX			265	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT			12.1	uF	Input capacitor
8	VOUT			5.00	V	Output voltage at the board
9	CDC	0		0	mV	Cable drop compensation desired at full load
10	IOUT	1.212		1.212	A	Output current
11	POUT			6.06	W	Output power
12	EFFICIENCY	0.85		0.85		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE			OPEN FRAME		Power supply enclosure
18	**PRIMARY CONTROLLER SELECTION**					
19	DEVICE_GENERIC	AUTO		INN3072		Generic device code
20	DEVICE_CODE			INN3072M		Actual device code
21	POUT_MAX			10.0	W	Power capability of the device based on thermal performance
22	ICC_MIN			1.50	A	Minimum constant current regulation threshold of the device
23	ICC_TYP			1.70	A	Typical constant current regulation threshold of the device
24	ICC_MAX			1.90	A	Maximum constant current regulation threshold of the device
25	RDSON_100DEG			11.24	Ω	Primary switch on time drain resistance at 100 degC
26	ILIMIT_MIN			0.510	A	Minimum current limit of the primary switch
27	ILIMIT_TYP			0.550	A	Typical current limit of the primary switch
28	ILIMIT_MAX			0.590	A	Maximum current limit of the primary switch
29	VDRAIN_BREAKDOWN			725	V	Device breakdown voltage
30	VDRAIN_ON_PRSW			0.89	V	Primary switch on time drain voltage
31	VDRAIN_OFF_PRSW			514.9	V	Peak drain voltage on the primary switch during turn-off
35	**WORST CASE ELECTRICAL PARAMETERS**					
36	FSWITCHING_MAX	41300		41300	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
37	VOR	71.5		71.5	V	Secondary voltage reflected to the primary when the primary switch turns off
38	VMIN			84.48	V	Valley of the minimum input AC voltage at full load
39	KP			1.49		Measure of continuous/discontinuous mode of operation
40	MODE_OPERATION			DCM		Mode of operation
41	DUTYCYCLE			0.364		Primary switch duty cycle
42	TIME_ON			10.27	us	Primary switch on-time
43	TIME_OFF			15.55	us	Primary switch off-time
44	LPRIMARY_MIN			1643.4	uH	Minimum primary inductance

45	LPRIMARY_TYP			1729.9	uH	Typical primary inductance
46	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
47	LPRIMARY_MAX			1816.4	uH	Maximum primary inductance
49	**PRIMARY CURRENT**					
50	IPEAK_PRIMARY			0.483	A	Primary switch peak current
51	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
52	IAVG_PRIMARY			0.079	A	Primary switch average current
53	IRIPPLE_PRIMARY			0.483	A	Primary switch ripple current
54	IRMS_PRIMARY			0.159	A	Primary switch RMS current
56	**SECONDARY CURRENT**					
57	IPEAK_SECONDARY			6.802	A	Secondary winding peak current
58	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
59	IRMS_SECONDARY			2.428	A	Secondary winding RMS current
63	**TRANSFORMER CONSTRUCTION PARAMETERS**					
64	**CORE SELECTION**					
65	CORE	CUSTOM		CUSTOM		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
66	CORE CODE	N87EF16		N87EF16		Core code
67	AE	20.10		20.10	mm^2	Core cross sectional area
68	LE	37.60		37.60	mm	Core magnetic path length
69	AL	1000		1000	nH/turns^2	Ungapped core effective inductance
70	VE	756.0		756.0	mm^3	Core volume
71	BOBBIN	EF16-Vertical		EF16-Vertical		Bobbin
72	AW	22.30		22.30	mm^2	Window area of the bobbin
73	BW	10.00		10.00	mm	Bobbin width
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
76	**PRIMARY WINDING**					
77	NPRIMARY			155		Primary turns
78	BPEAK			3521	Gauss	Peak flux density
79	BMAX			2757	Gauss	Maximum flux density
80	BAC			1378	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			72	nH/turns^2	Typical gapped core effective inductance
82	LG			0.326	mm	Core gap length
84	**SECONDARY WINDING**					
85	NSECONDARY	11		11		Secondary turns
92	**PRIMARY COMPONENTS SELECTION**					
98	CBPP			0.47	uF	BPP pin capacitor
102	**SECONDARY COMPONENTS SELECTION**					
103	RFWD			47	Ω	Forward pin resistor
104	CBPS			2.2	uF	BPS pin capacitor
108	**MULTIPLE OUTPUT PARAMETERS**					
109	**OUTPUT 1**					
110	VOUT1			5.00	V	Output 1 voltage
111	IOUT1	0.90		0.90	A	Output 1 current
112	POUT1			4.50	W	Output 1 power
113	IRMS_SECONDARY1			1.803	A	Root mean squared value of the secondary current for output 1
114	IRIPPLE_CAP_OUTPUT1			1.562	A	Current ripple on the secondary waveform for output 1
115	NSECONDARY1			11		Number of turns for output 1
116	VREVERSE_RECTIFIER1			31.50	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
117	SRFET1	AUTO		AO6420		Secondary rectifier (Logic MOSFET) for output 1
118	VF_SRFET1			0.046	V	SRFET on-time drain voltage for output 1

119	VBREAKDOWN_SRFET1			60	V	SRFET breakdown voltage for output 1
120	RDSON_SRFET1			75.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
122	**OUTPUT 2**					
123	VOUT2	12.00		12.00	V	Output 2 voltage
124	IOUT2	0.130		0.130	A	Output 2 current
125	POUT2			1.56	W	Output 2 power
126	IRMS_SECONDARY2			0.260	A	Root mean squared value of the secondary current for output 2
127	IRIPPLE_CAP_OUTPUT2			0.226	A	Current ripple on the secondary waveform for output 2
128	NSECONDARY2			27		Number of turns for output 2
129	VREVERSE_DIODE2			77.04	V	Diode reverse voltage (not accounting parasitic voltage ring) for output 2
130	DIODE2	Auto		VSSA210-M3/5AT		Secondary rectifier (Diode) for output 2
131	VF_DIODE2			0.610	V	Diode forward voltage for output 2
132	VBREAKDOWN_DIODE2			100	V	Diode breakdown voltage for output 2
133	IFM_DIODE2			2.000	A	Diode maximum forward continuous current for output 2
134	TYPE_DIODE2			Schottky		Diode type for output 2
150	PO_TOTAL			6.06	W	Total power of all outputs
151	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

9 Performance Data

9.1 *Average Efficiency*

Requirement	
Average	69% (DOE6), 75% (CoC II)
10%	66%

9.1.1 115 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	115.07	151.13	7.05	4.96	0.90	12.27	0.12	5.982	84.875	
75%	115.08	120	5.24	4.97	0.67	12.25	0.09	4.475	85.401	
50%	115.07	81.93	3.45	4.98	0.45	12.21	0.06	2.972	86.245	
25%	115.08	43.78	1.67	4.98	0.23	12.14	0.03	1.445	86.631	**85.79**
10%	115.07	17.94	0.63	4.98	0.09	12.08	0.01	0.52	**83.14**	

9.1.2 230 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	230.24	91.62	7.0	4.96	0.90	12.29	0.12	5.995	85.68	
75%	230.24	71.08	5.20	4.97	0.67	12.27	0.09	4.48	86.12	
50%	230.24	49.88	3.43	4.97	0.45	12.22	0.06	2.967	86.43	
25%	230.25	27.81	1.69	4.98	0.23	12.15	0.03	1.451	85.71	**85.98**
10%	230.24	37.62	2.47	4.98	0.09	12.09	0.01	0.52	**81.53**	

9.2 *Full Load Efficiency vs. Line*

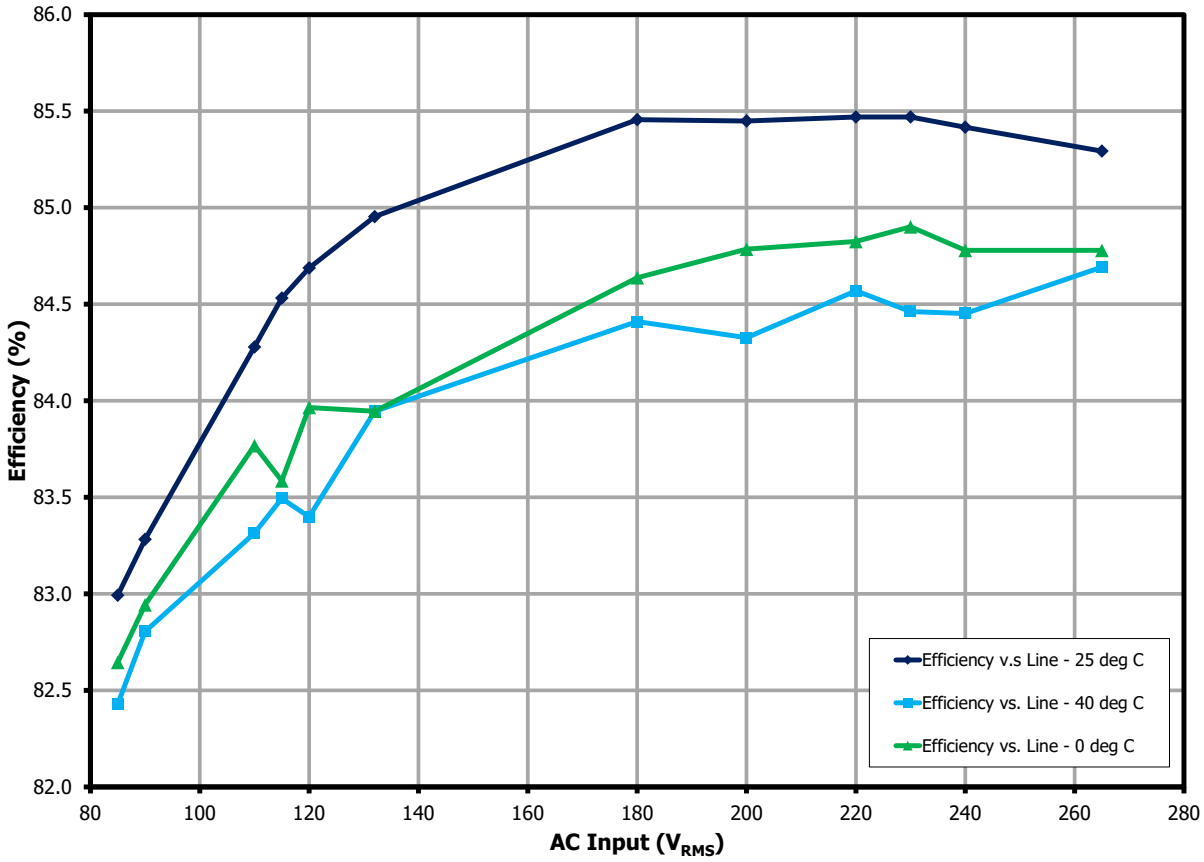


Figure 8 – Full load Efficiency vs. Line Voltage.

9.3 *Efficiency vs. Load*

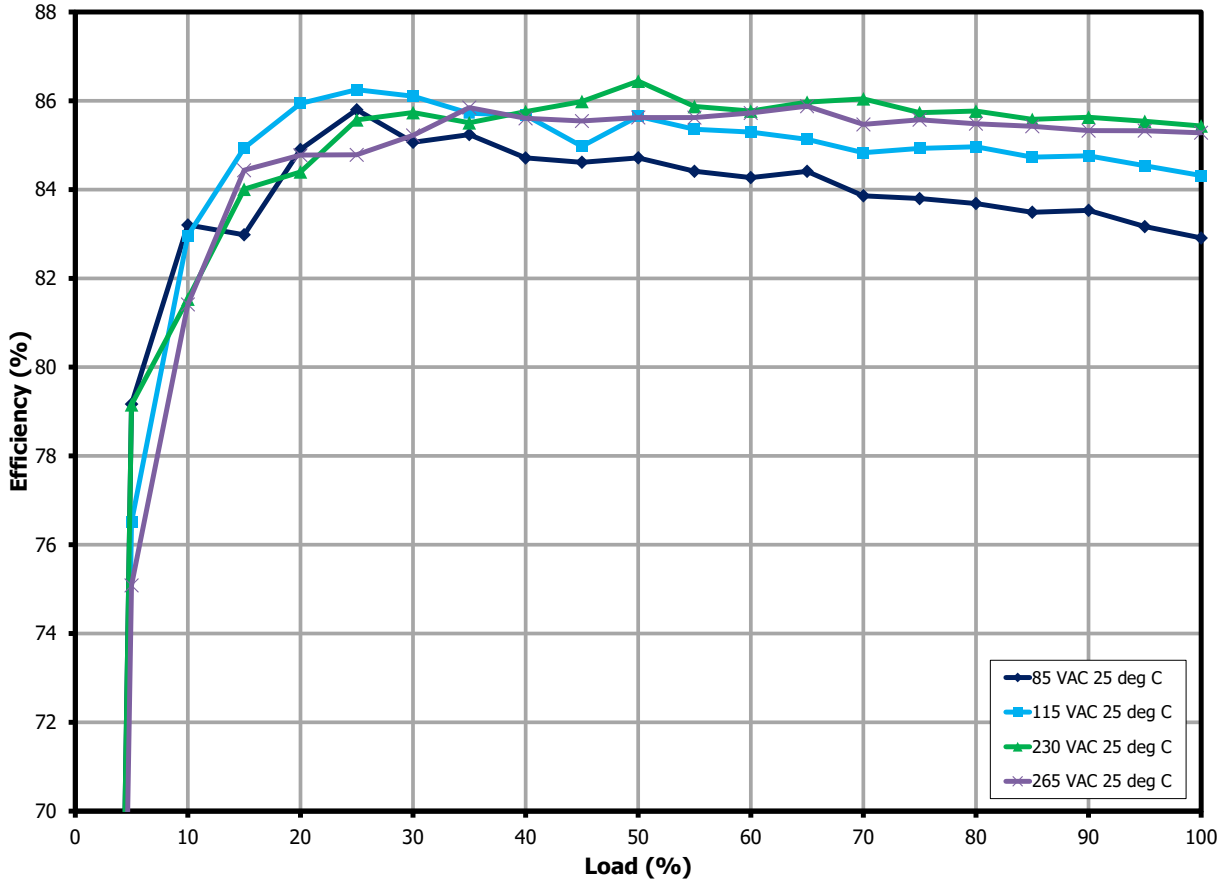


Figure 9 – Efficiency vs. Load, Room Ambient – 25 ºC Temperature.

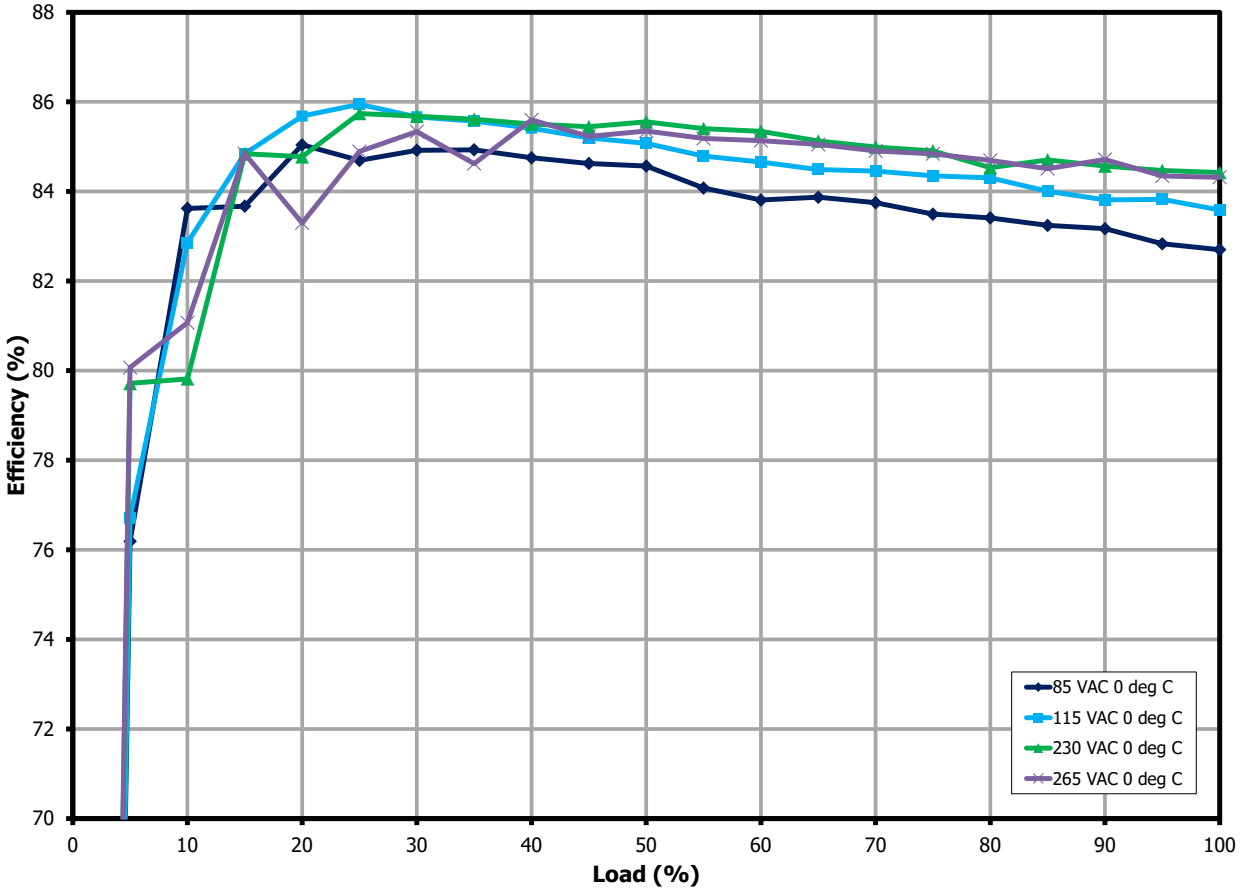


Figure 10 – Efficiency vs. Load, Cold Ambient – 0 ºC Temperature.

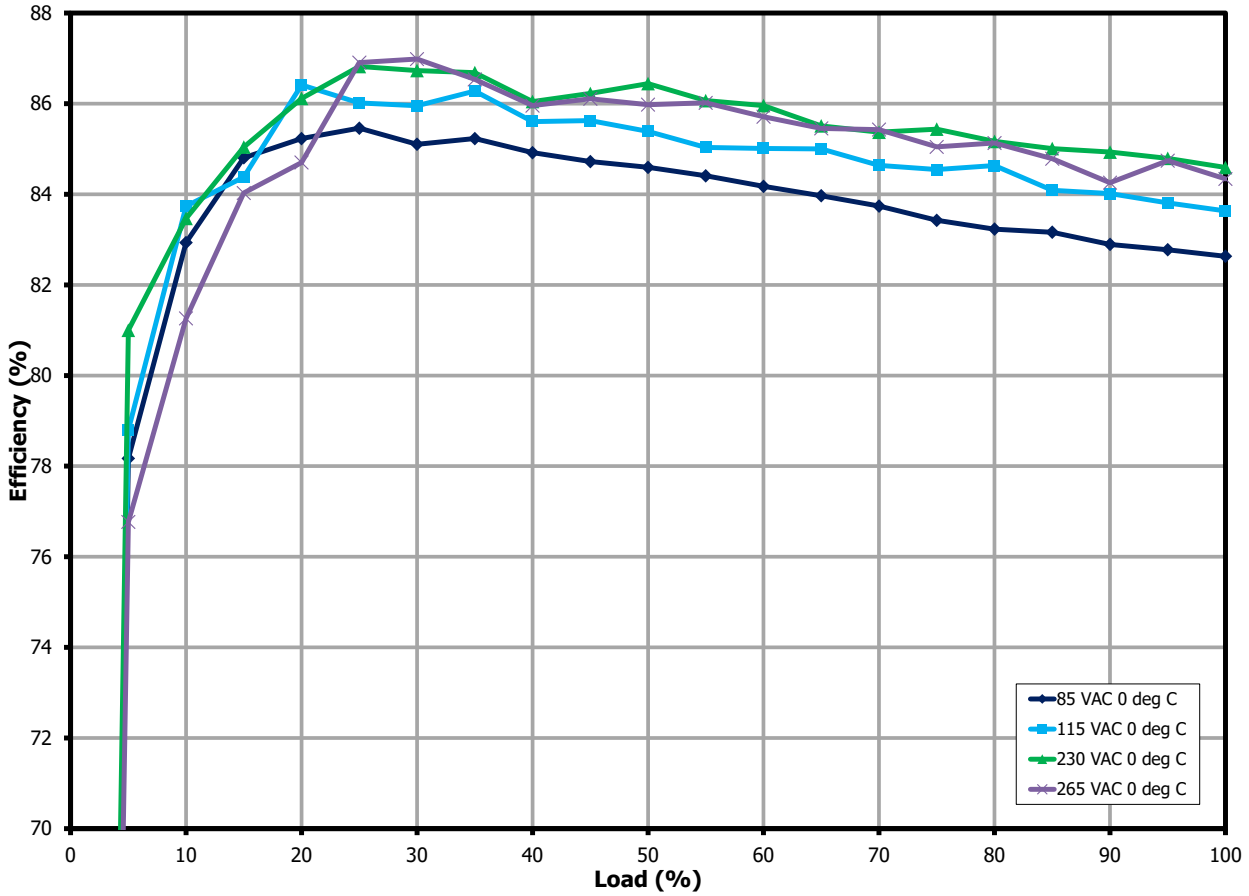


Figure 11 – Efficiency vs. Load, Hot Ambient – 40 ºC Temperature.

9.4 *No-Load Input Power*

Note: Soak for 30 minutes and integrate for 1 hour.

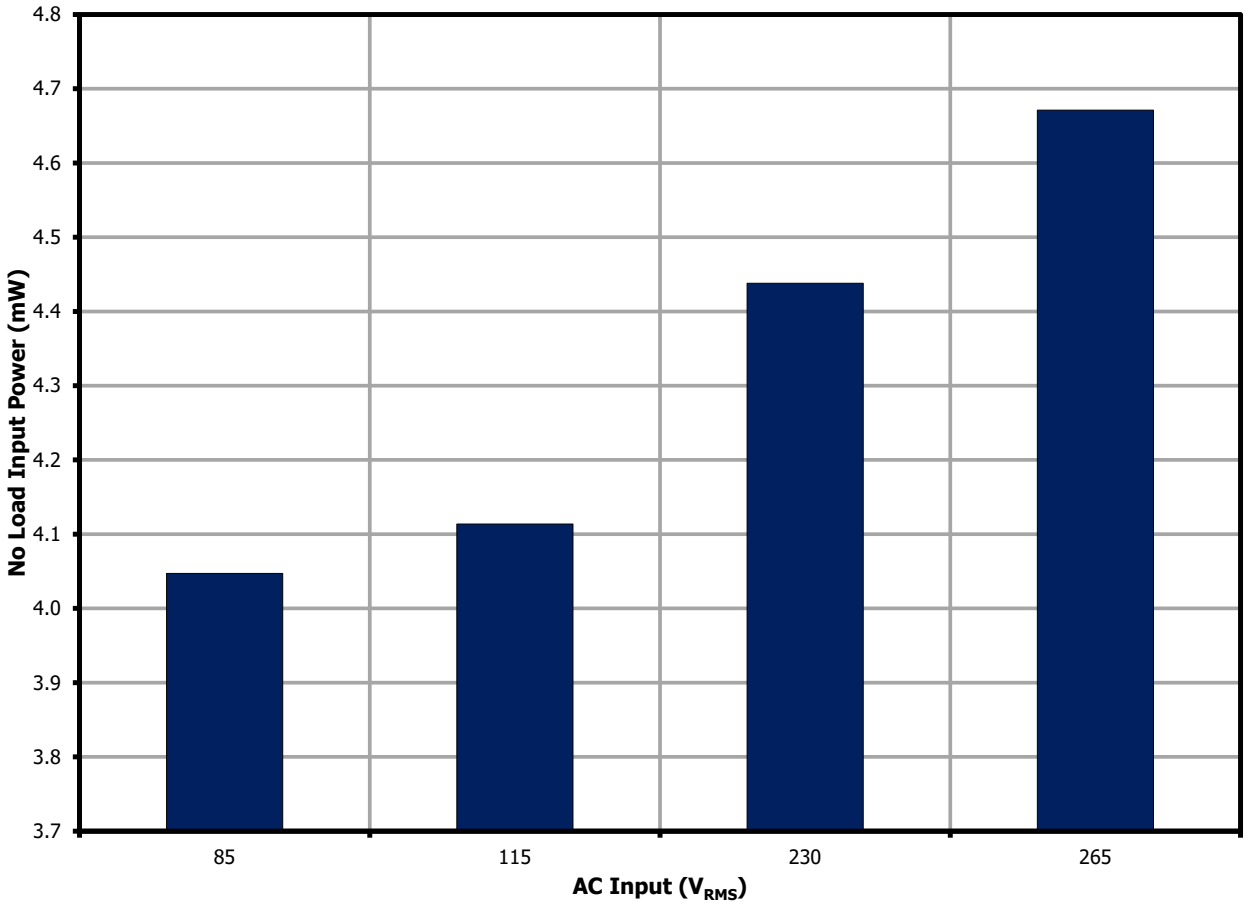


Figure 12 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

9.5 *Standby Power (5 V / 30 mA Load, 12 V No-Load)*

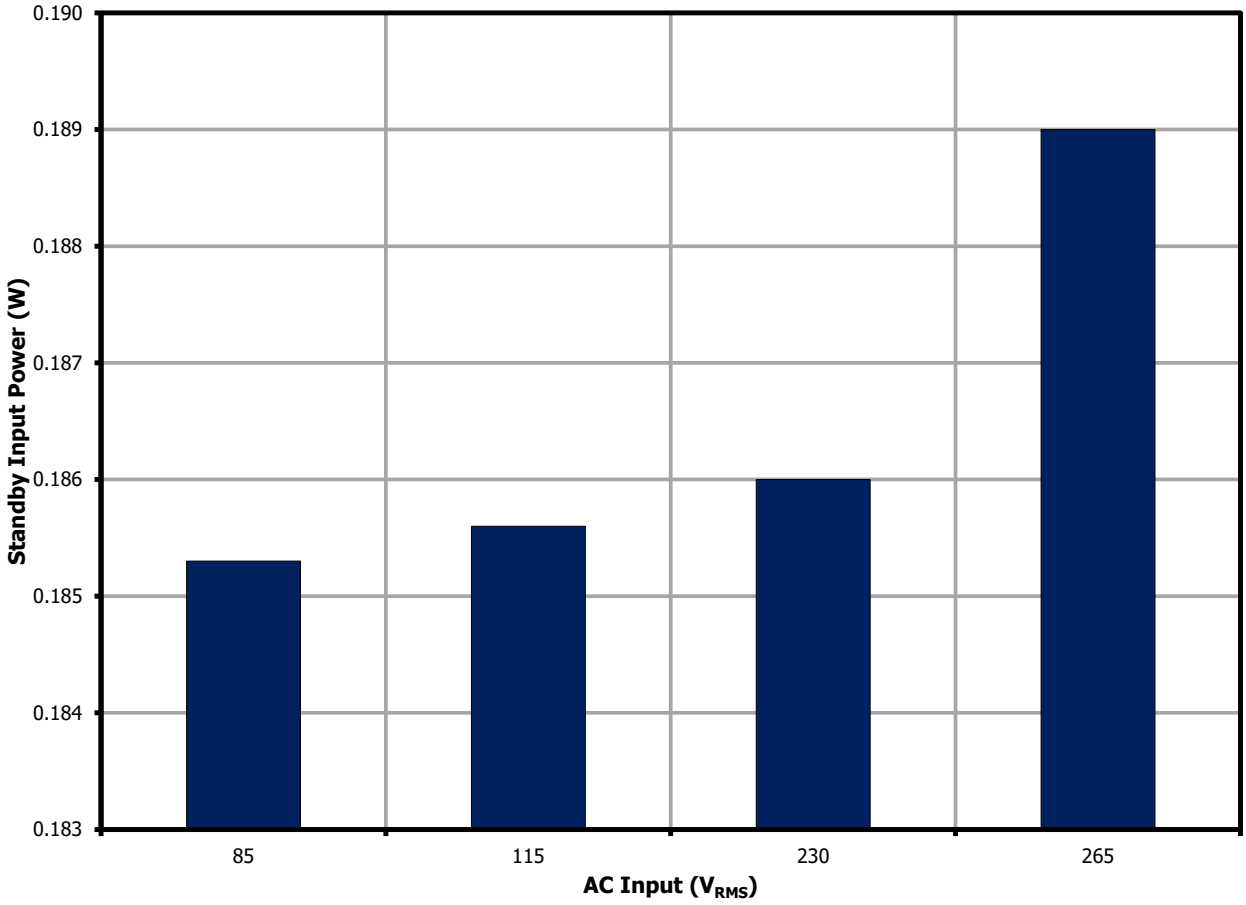


Figure 13 – Standby Power (5 V / 30 mA Load, 12 V No-Load).

9.6 *Line and Load Regulation*

9.6.1 Line Regulation (Full Load)

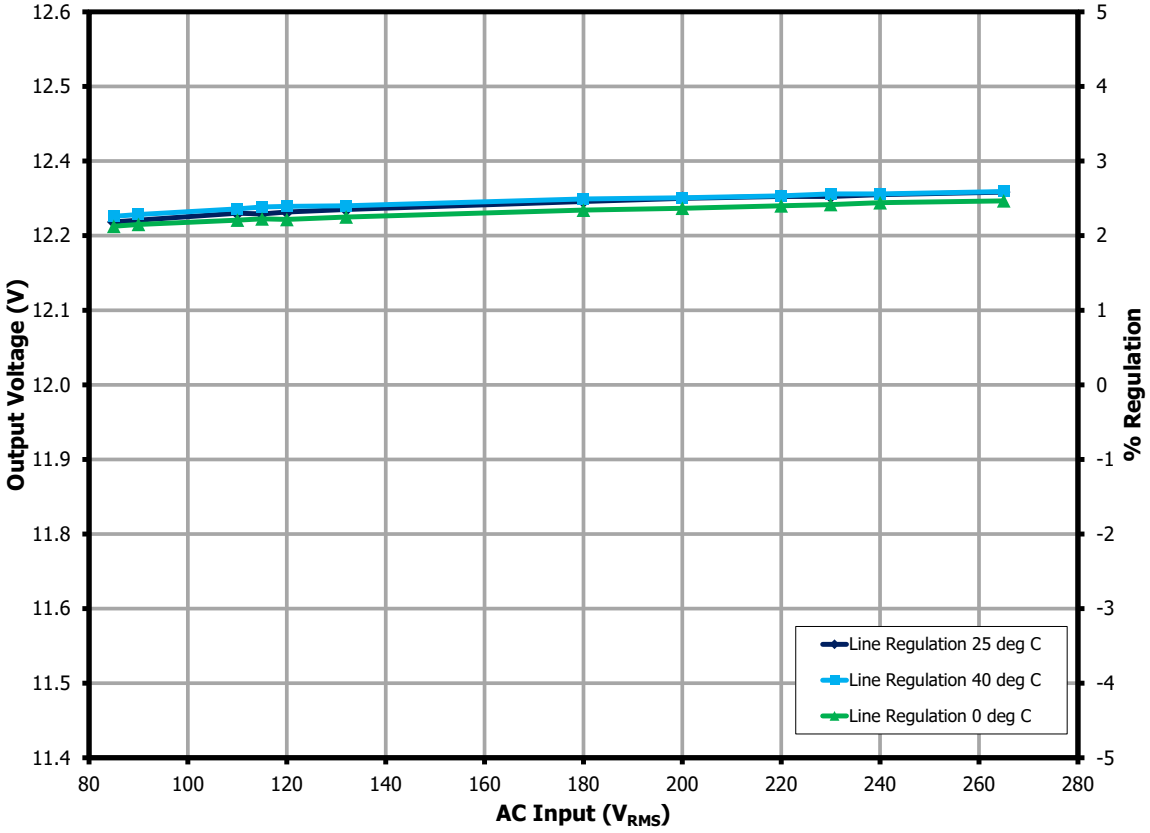


Figure 14 – 12 V Output Voltage vs. Input Line Voltage.

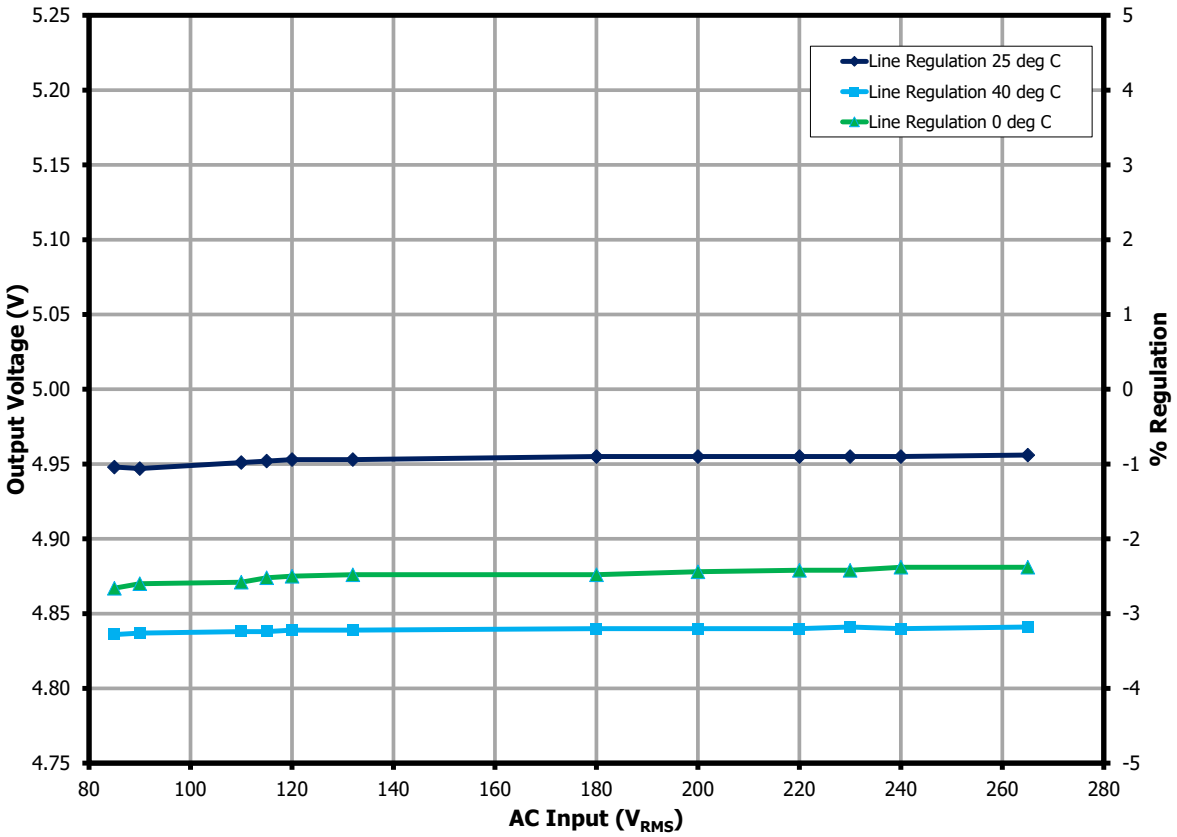


Figure 15 – 5 V Output Voltage vs. Input Line Voltage.

	5 V	12 V
Min.	4.84	12.27
Max.	4.96	12.31

9.6.2 5 V Load Regulation

Note: Both 5 V and 12 V outputs are loaded with the same percentage.

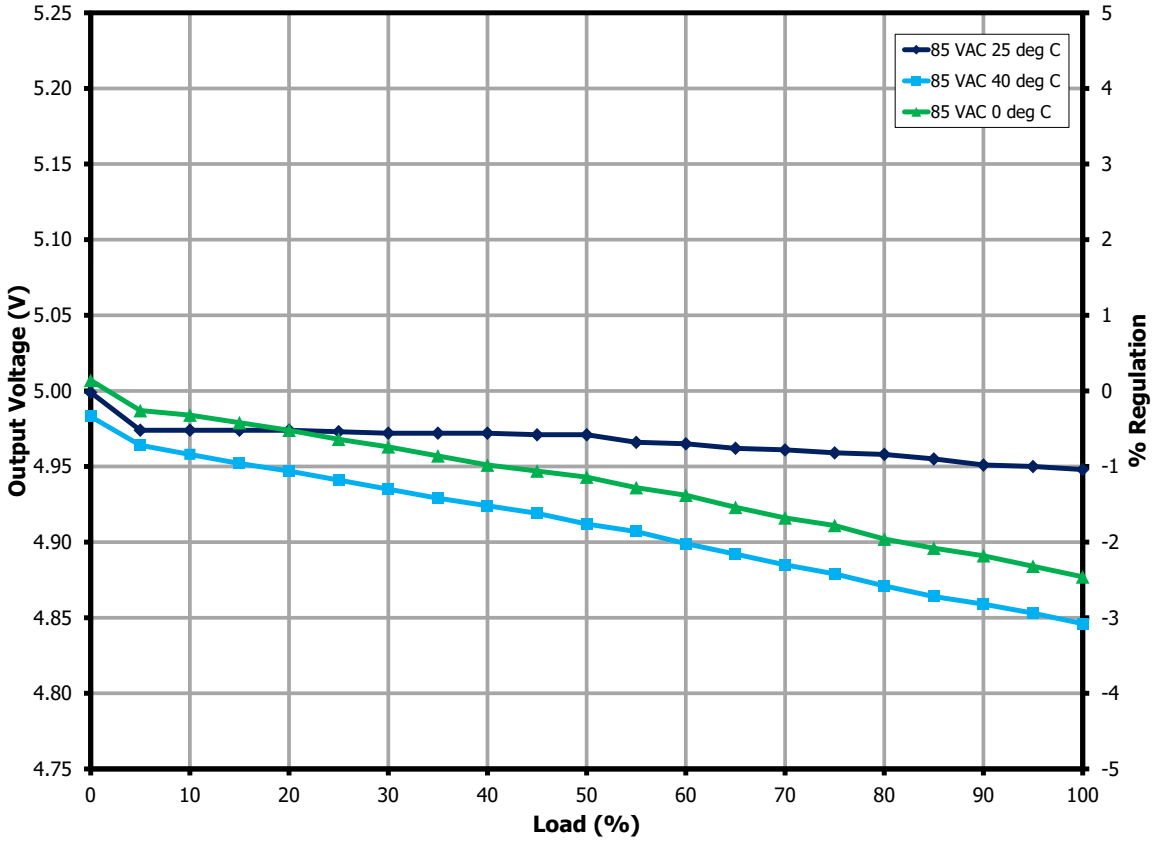


Figure 16 – 5 V Output Voltage vs. Load at 85 VAC.

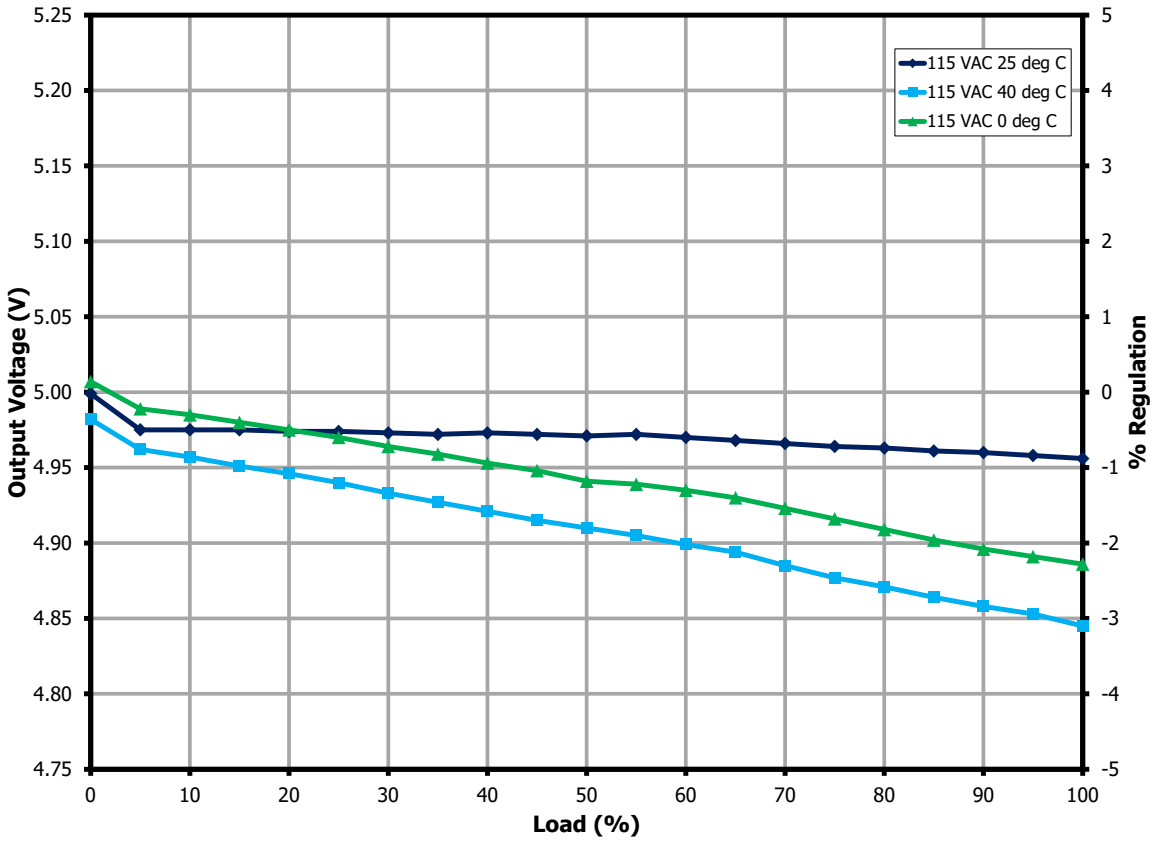


Figure 17 – 5 V Output Voltage vs. Load at 115 VAC.

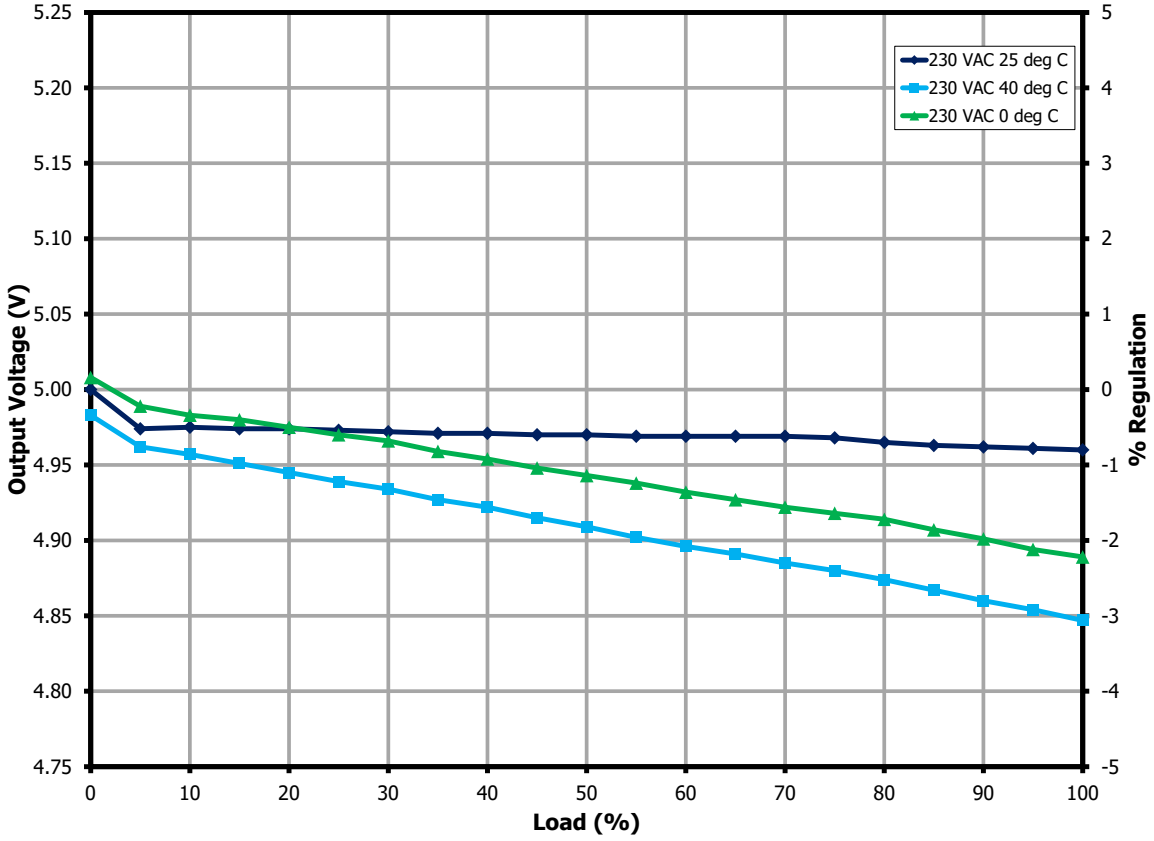


Figure 18 – 5 V Output Voltage vs. Load at 230 VAC.

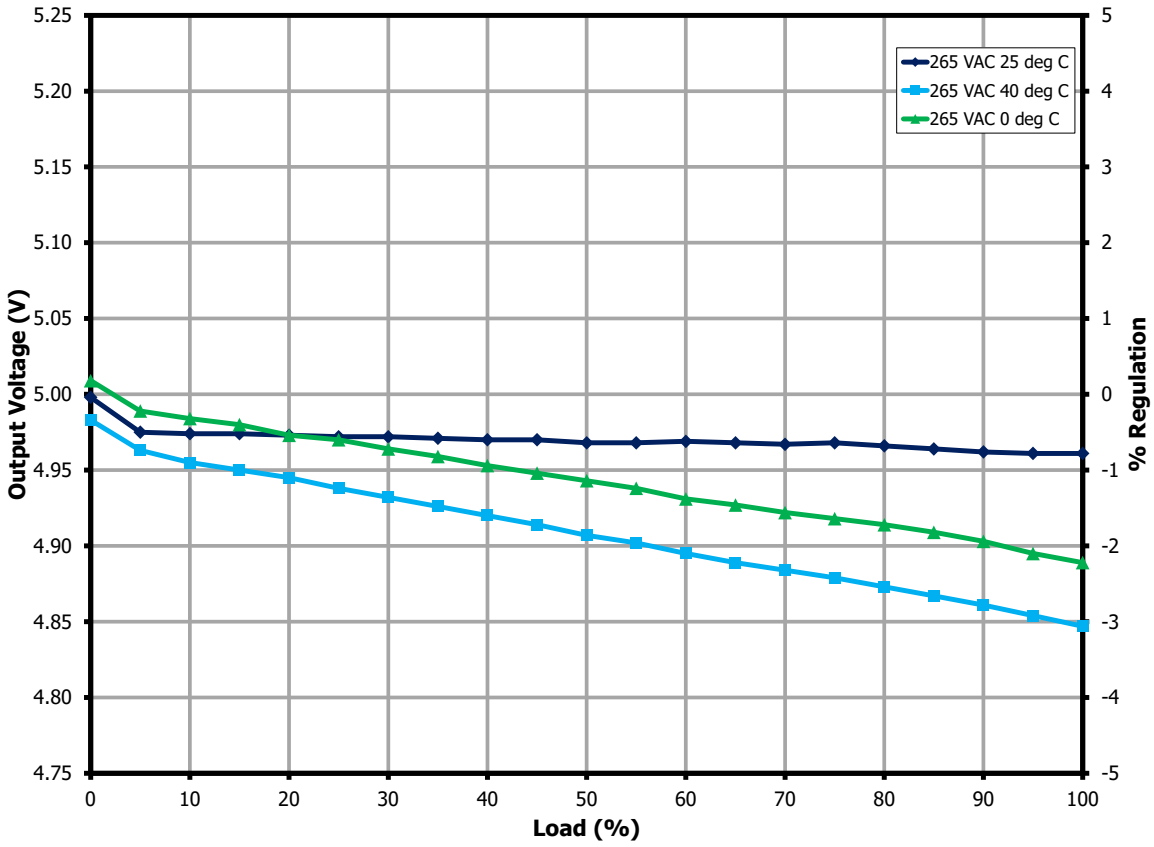


Figure 19 – 5 V Output Voltage vs. Load at 265 VAC.

9.6.3 12 V Load Regulation

Note: Both 5 V and 12 V outputs are loaded with the same percentage.

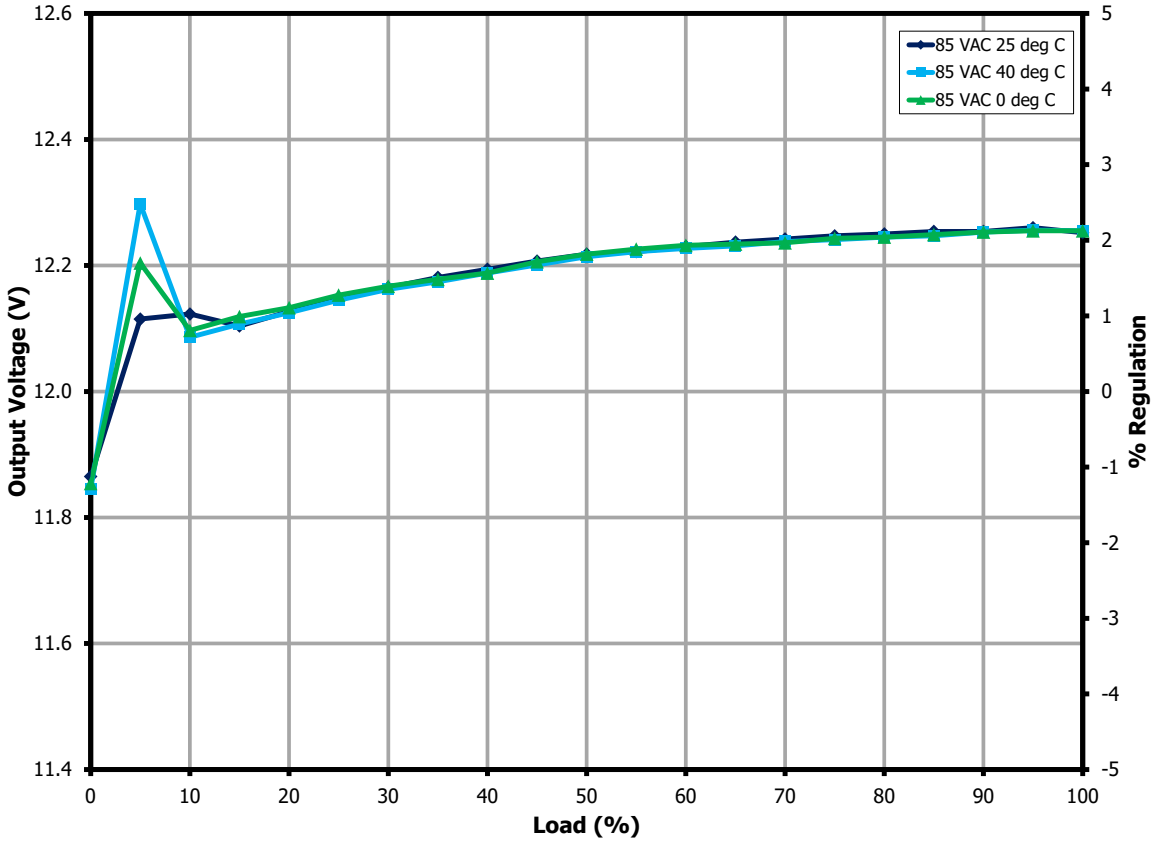


Figure 20 – 12 V Output Voltage vs. Load at 85 VAC.

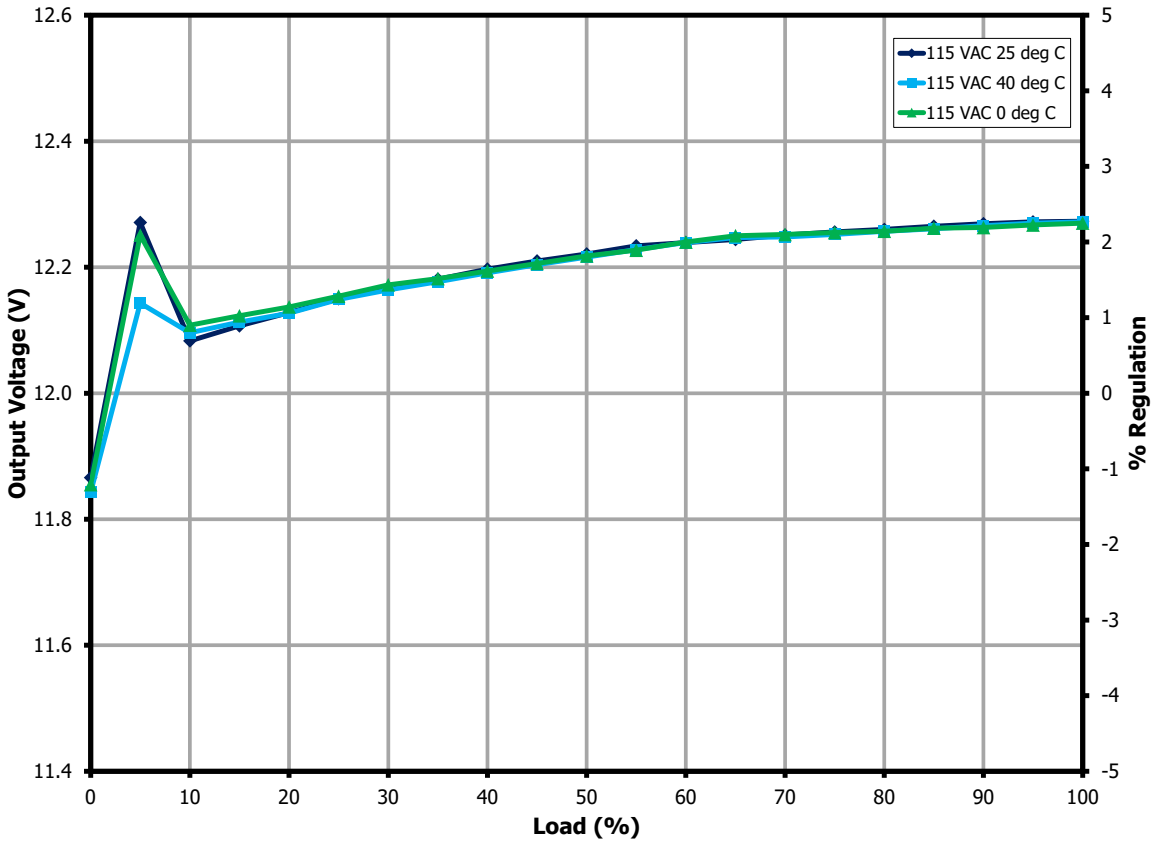


Figure 21 – 12 V Output Voltage vs. Load at 115 VAC.

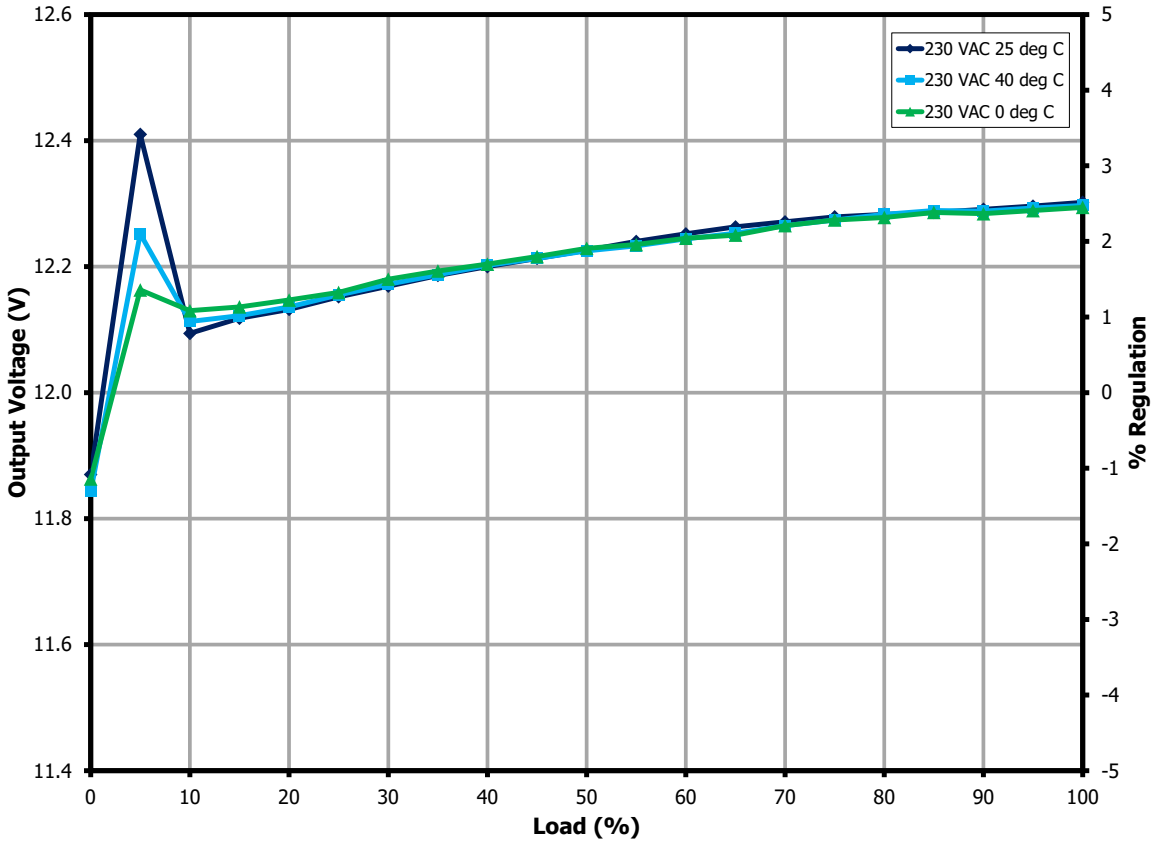


Figure 22 – 12 V Output Voltage vs. Load at 230 VAC.

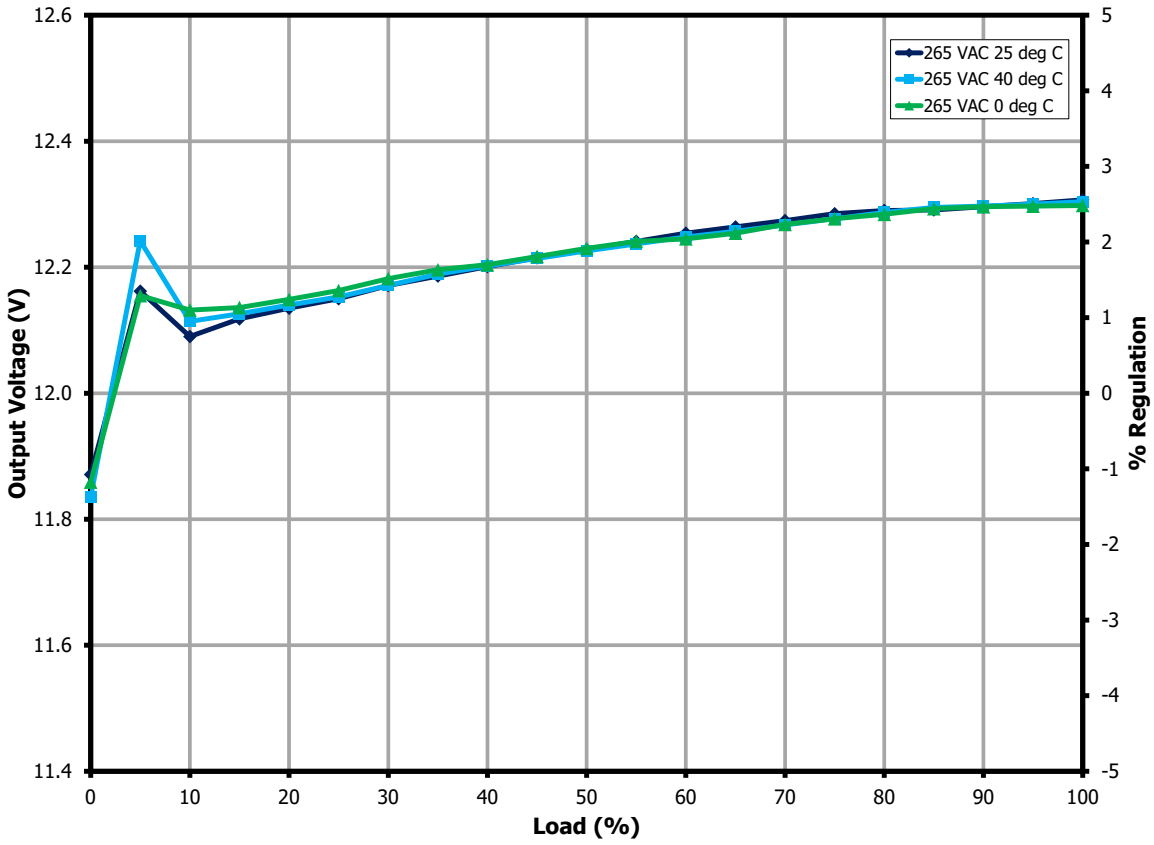


Figure 23 – 12 V Output Voltage vs. Load at 265 VAC.

9.7 *Cross Load Regulation*

9.7.1 12 V Load Change with Full Load on 5 V

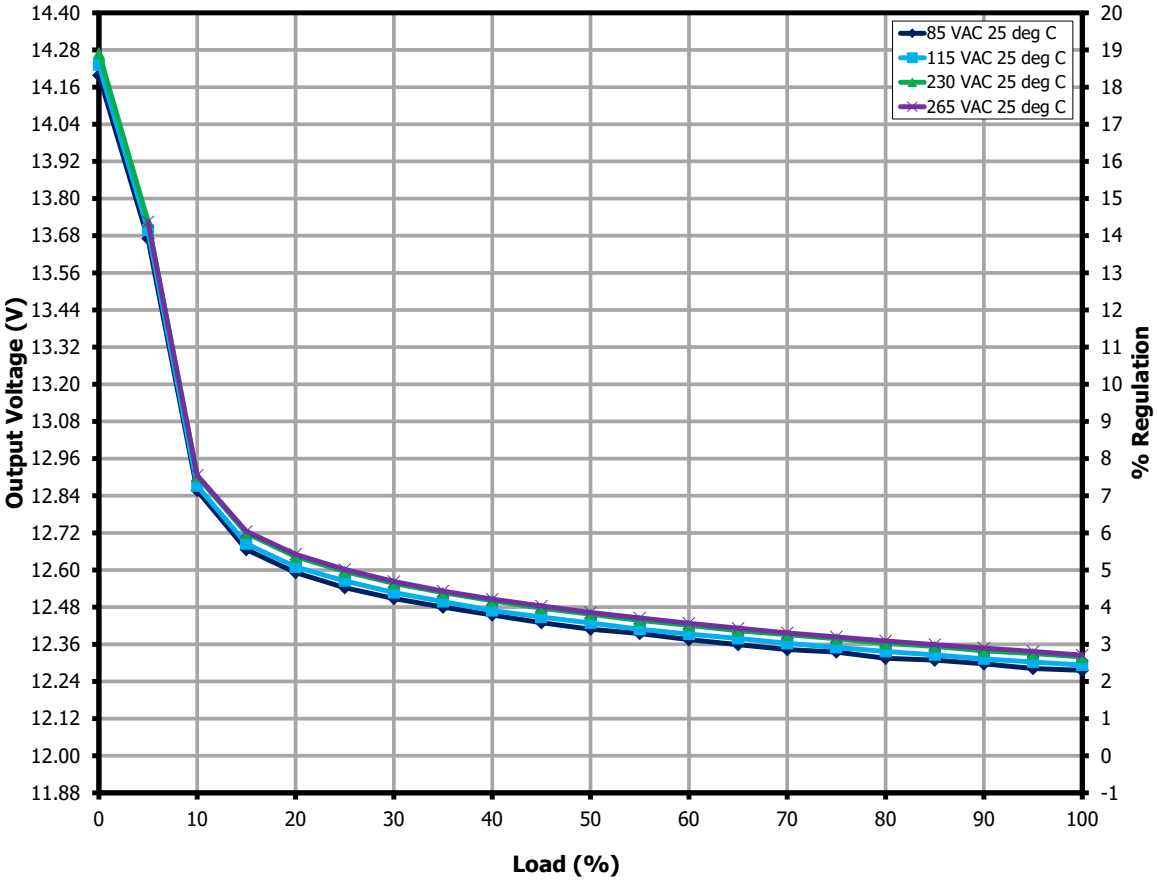


Figure 24 – 12 V Output Voltage vs. Output Load, Room Temperature.

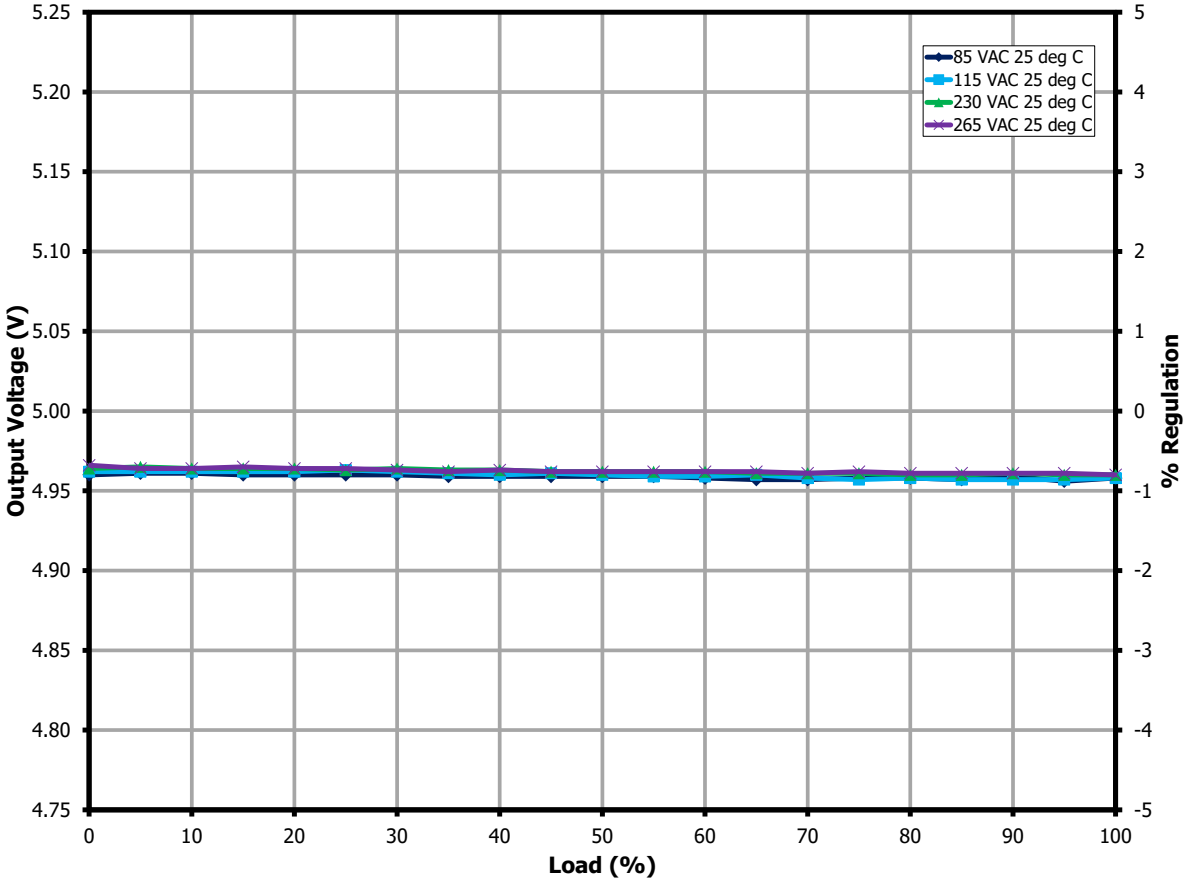


Figure 25 – 5 V Output Voltage Full Load, Room Temperature.

	5 V	12 V
Min.	4.96	12.28
Max.	4.97	14.27

9.7.2 12 V Load Change with No-Load on 5 V

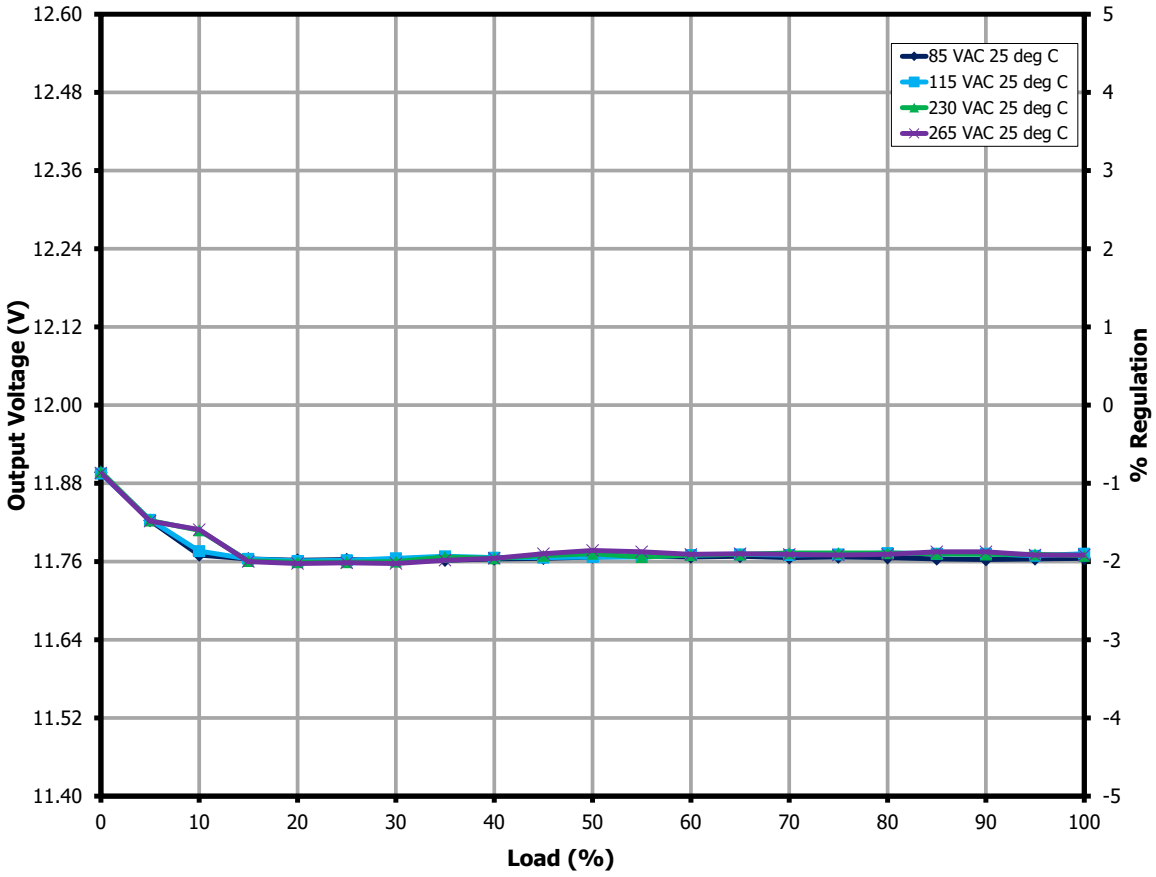


Figure 26 – 12 V Output Voltage vs. Output Load, Room Temperature.

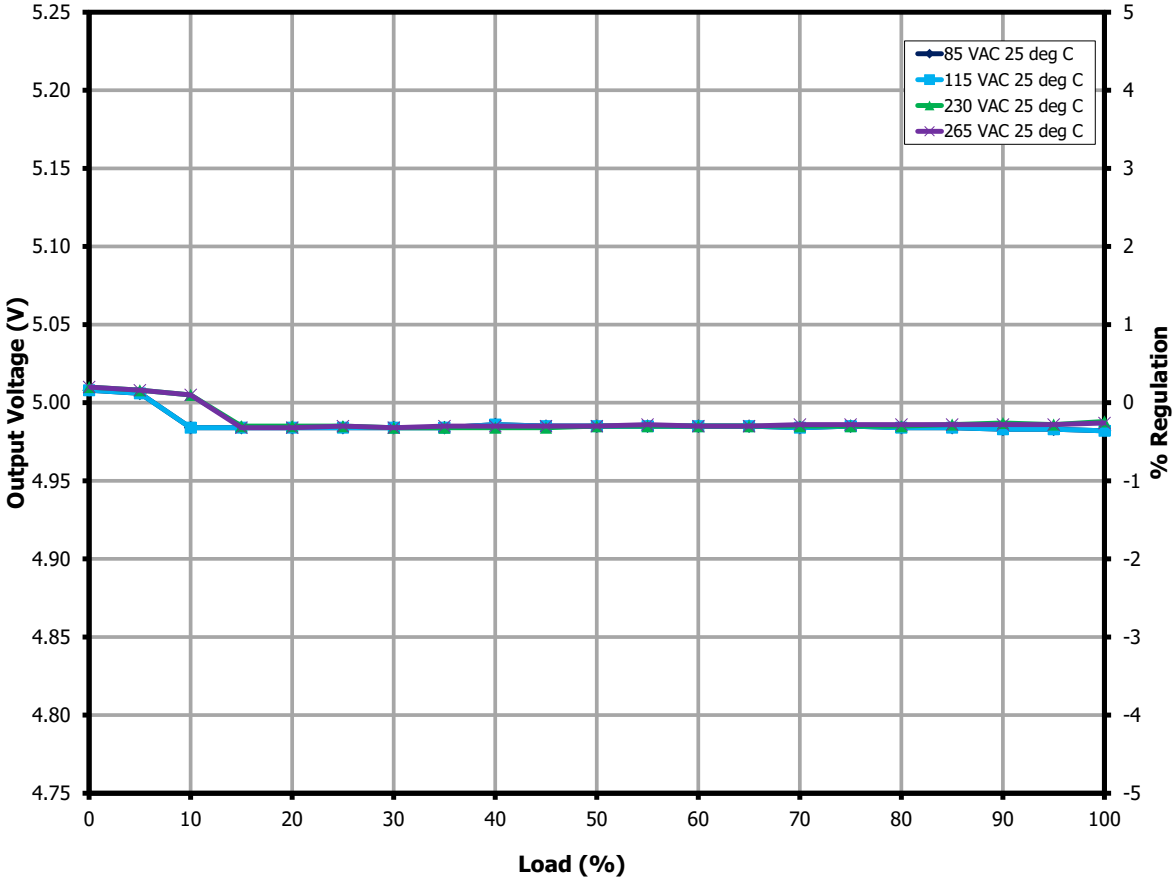


Figure 27 – 5 V Output Voltage No-Load, Room Temperature.

	5 V	12 V
Min.	4.98	11.76
Max.	5.01	11.90

9.7.3 5 V Load Change with Full Load on 12 V

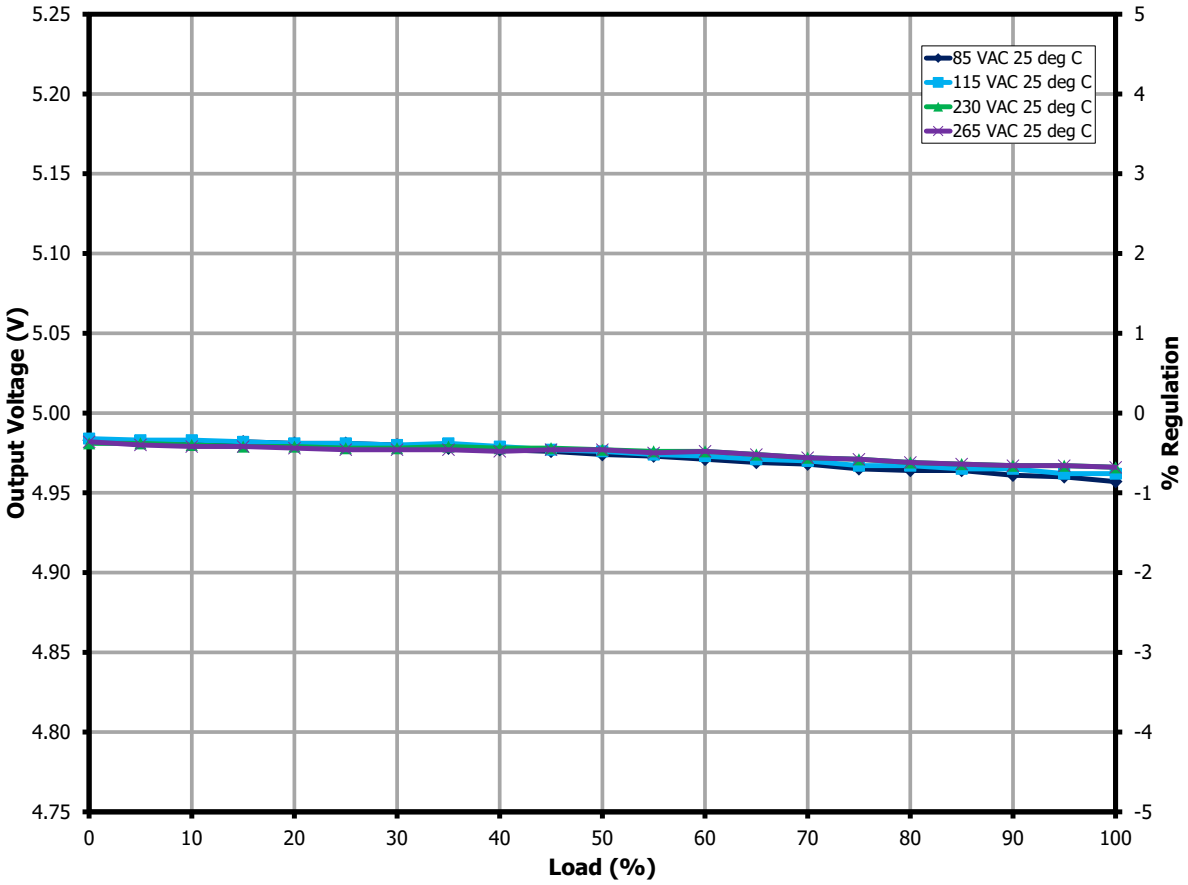


Figure 28 – 5 V Output Voltage vs. Output Load, Room Temperature.

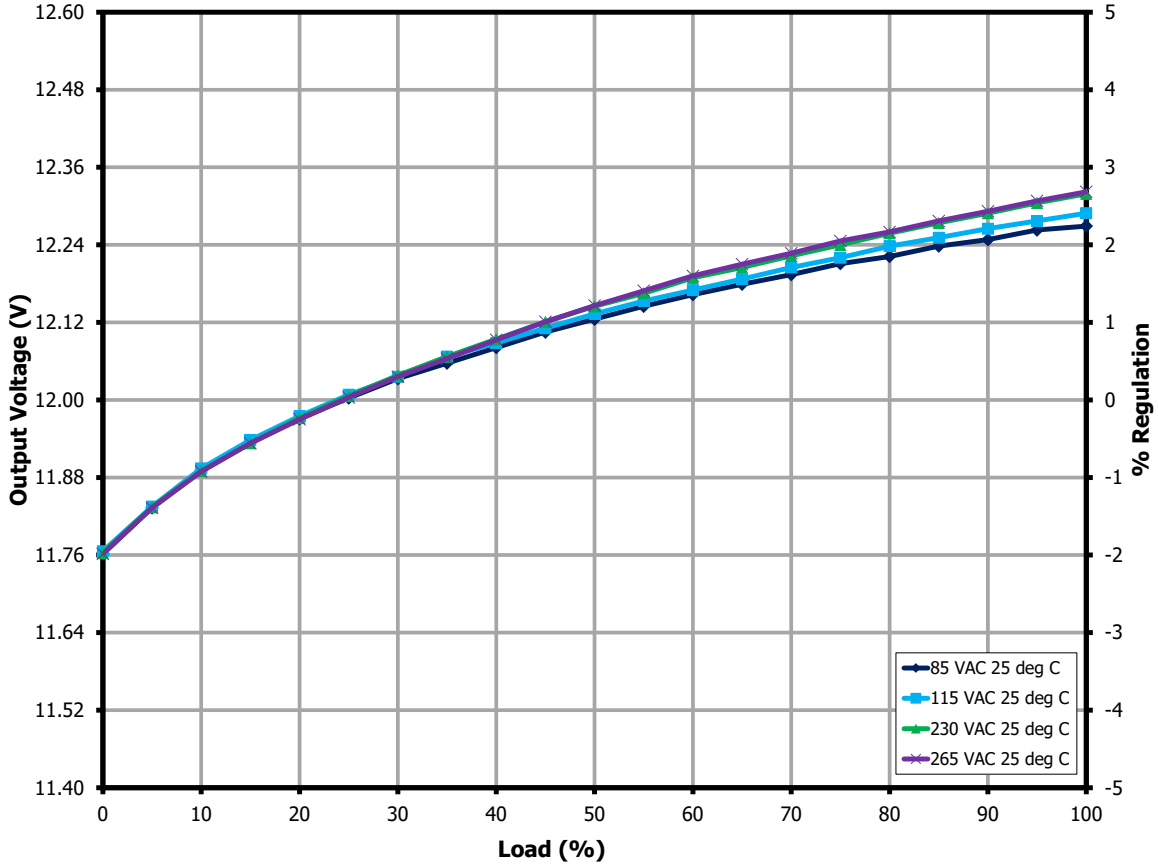


Figure 29 – 12 V Output Voltage Full Load, Room Temperature.

	5 V	12 V
Min.	4.96	11.76
Max.	4.98	12.32

9.7.4 5 V Load Change with No-Load on 12 V

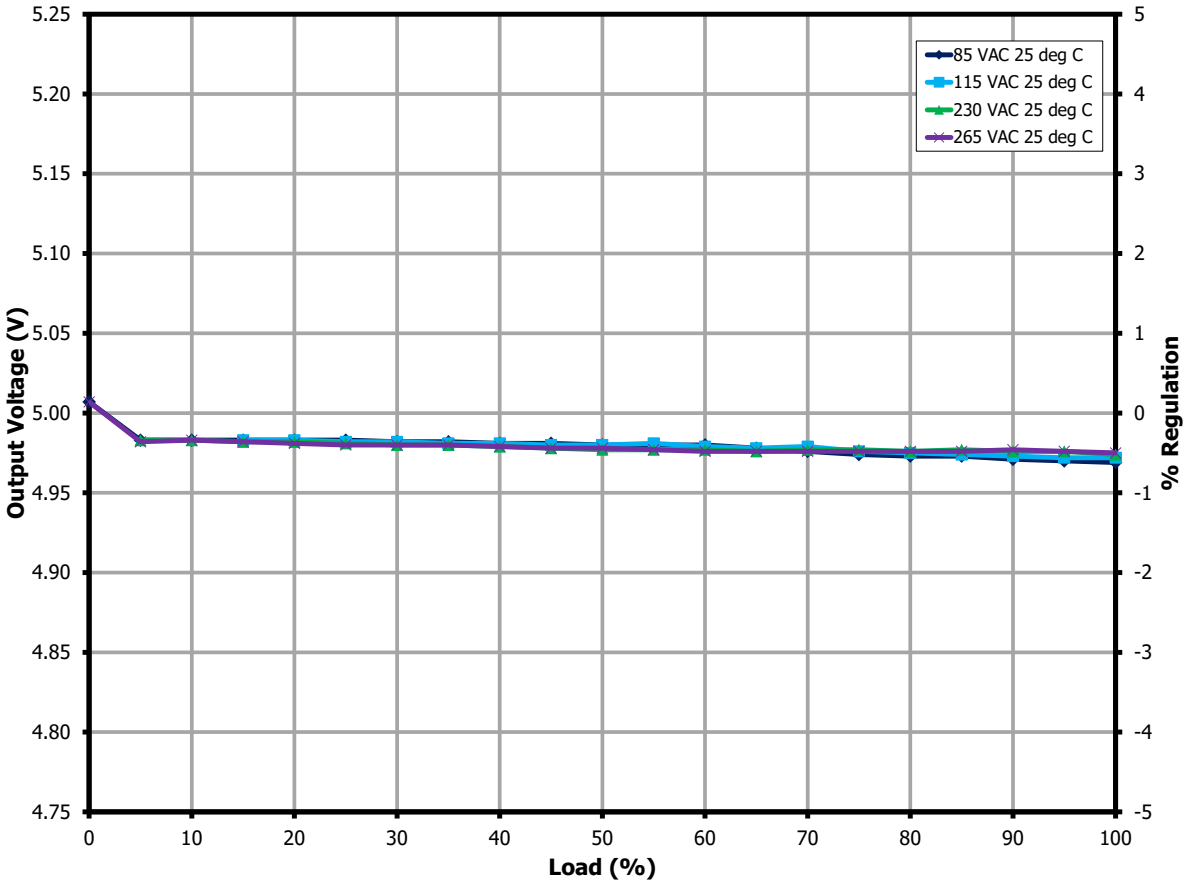


Figure 30 – 5 V Output Voltage vs. Output Load, Room Temperature**.**

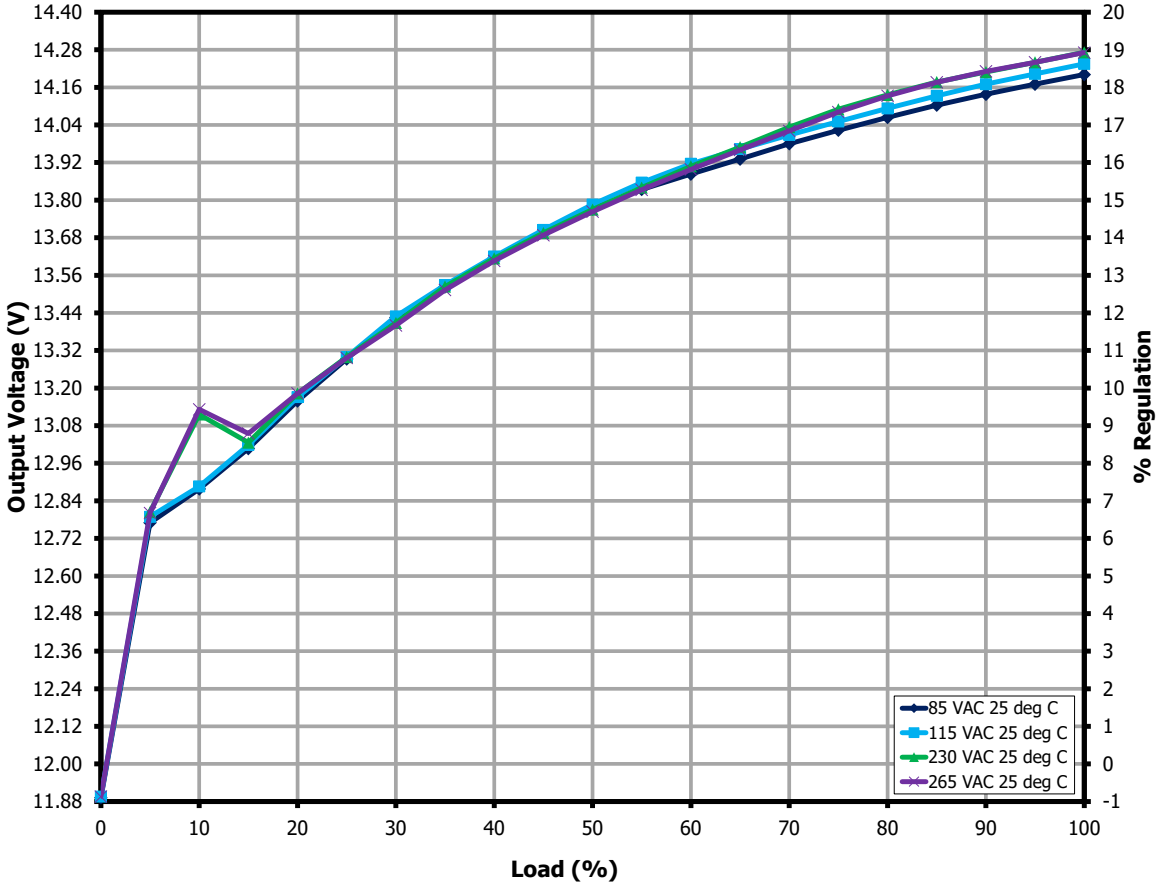


Figure 31 – 12 V Output Voltage No Load, Room Temperature**.**

	5 V	12 V
Min.	4.97	11.89
Max.	5.01	14.27

10 Thermal Performance

10.1 *85 VAC*

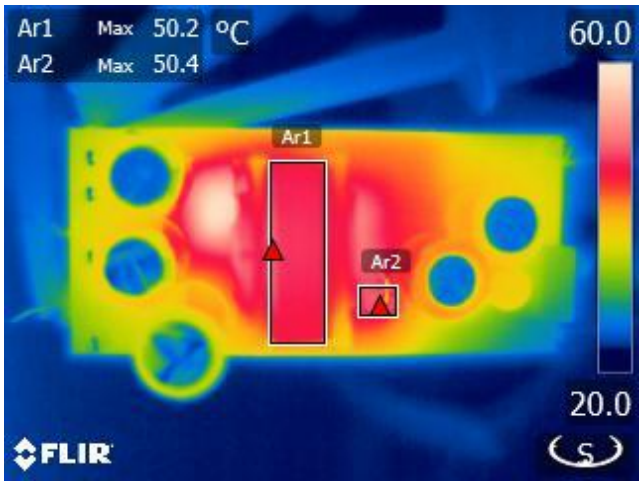


Figure 32 – Transformer Side. 85 VAC, Full Load.

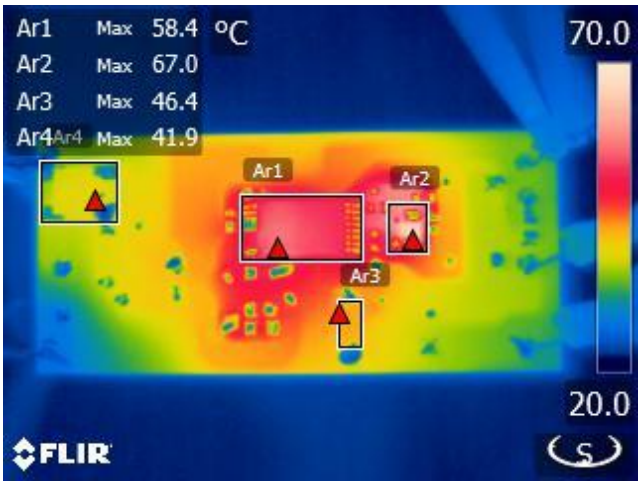


Figure 33 – InnoSwitch3-TN Side. 85 VAC, Full Load.

	Reference	°C
Ambient		22.6
Transformer	T1	50.2
Primary Snubber Diode	D1	50.4

	Reference	°C
Ambient		22.6
InnoSwitch3-TN	U1	58.4
SR FET Q1	Q1	67.0
Schottky D2	D2	46.4
Bridge Diode	BR1	41.9

10.2 ***265 VAC***

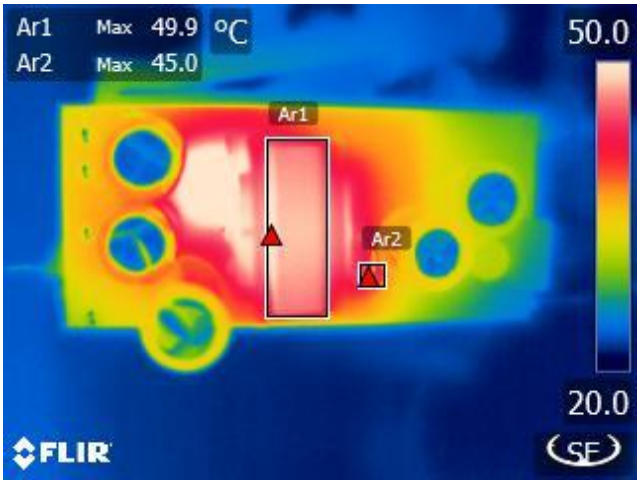


Figure 34 – Transformer Side. 265 VAC, Full Load.

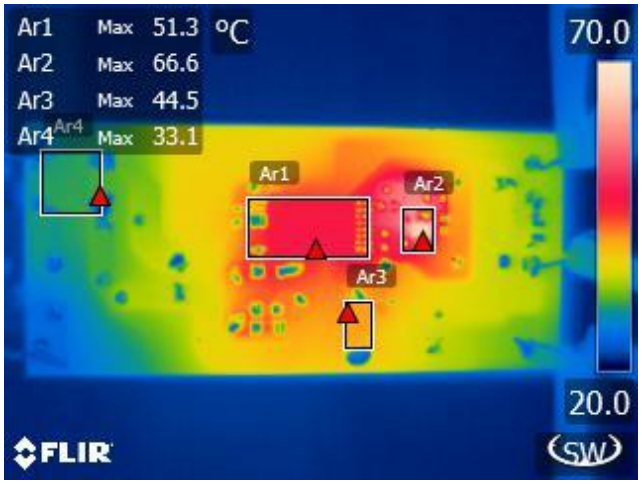


Figure 35 – InnoSwitch3-TN Side. 265 VAC, Full Load.

	Reference	°C
Ambient		21.8
Transformer	T1	49.9
Primary Snubber Diode	D1	45.0

	Reference	°C
Ambient		21.8
InnoSwitch3-TN	U1	51.3
SR FET Q1	Q1	66.6
Schottky D2	D2	44.5
Bridge Diode	BR1	33.1

11 Waveforms

11.1 *Load Transient Response*

11.1.1 12 V Load Transient – Full-Load at 5 V Output

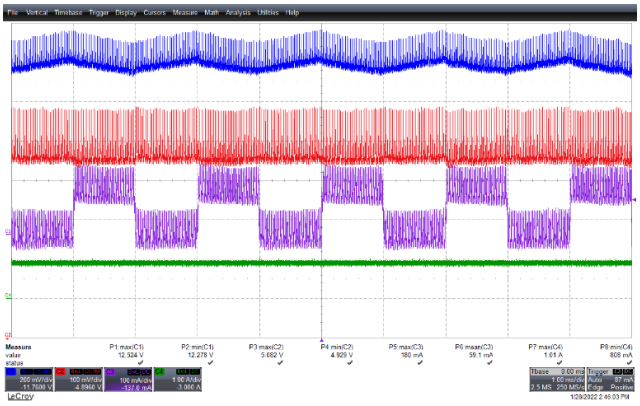


Figure 36 – 0 A – 0.13 A, 12 V Load Step Transient Response, 5 V 0.9 A, 85 VAC.
5 V_{MIN}: 4.93 V.; 5 V_{MAX}: 5.08 V.
12 V_{MIN}: 12.28 V. 12 V_{MAX}: 12.52 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

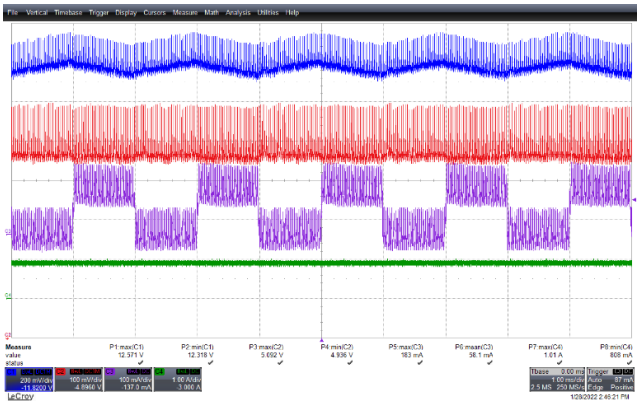


Figure 37 – 0 A – 0.13 A, 12 V Load Step Transient Response, 5 V 0.9 A, 265 VAC.
5 V_{MIN}: 4.94 V. 5 V_{MAX}: 5.09 V.
12 V_{MIN}: 12.32 V. 12 V_{MAX}: 12.57 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

11.1.2 12 V Load Transient – No-Load at 5 V Output

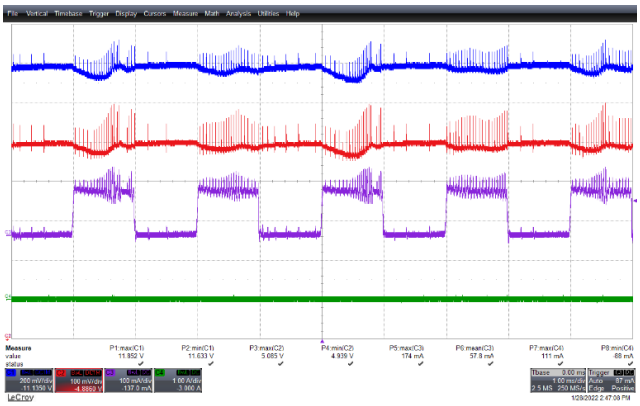


Figure 38 – 0 A – 0.13 A, 12 V Load Step Transient Response, 5 V 0 A, 85 VAC.
5 V_{MIN}: 5.09 V.; 5 V_{MAX}: 4.94 V.
12 V_{MIN}: 11.63 V. 12 V_{MAX}: 11.85 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 V I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

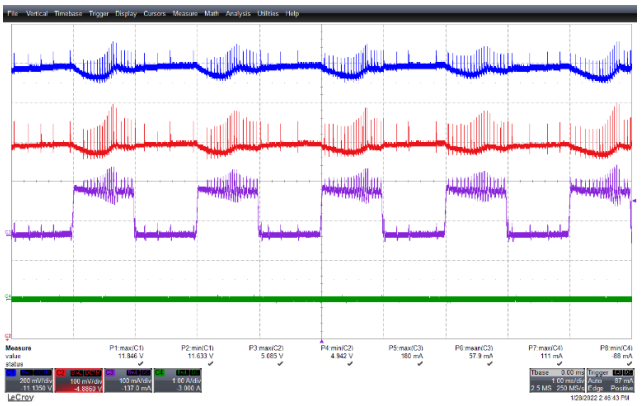


Figure 39 – 0 A – 0.13 A, 12 V Load Step Transient Response, 5 V 0 A, 265 VAC.
5 V_{MIN}: 4.94 V. 5 V_{MAX}: 5.09 V.
12 V_{MIN}: 11.63 V. 12 V_{MAX}: 11.85 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

11.1.3 5 V Load Transient – Full-Load at 12 V Output

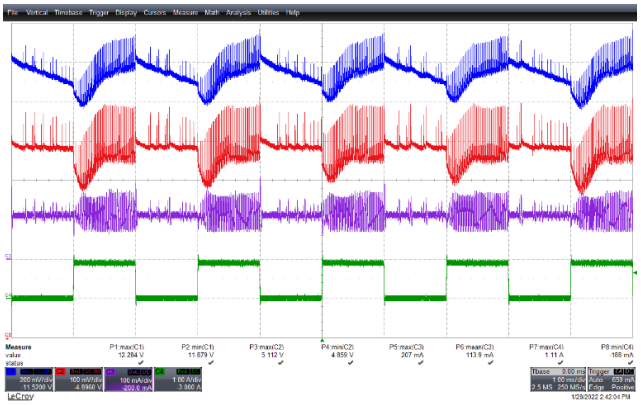


Figure 40 – 0 A – 0.9 A, 5 V Load Step Transient Response, 12 V 0.13 A, 85 VAC.
5 V_{MIN}: 4.86 V.; 5 V_{MAX}: 5.11 V.
12 V_{MIN}: 11.88 V. 12 V_{MAX}: 12.28 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

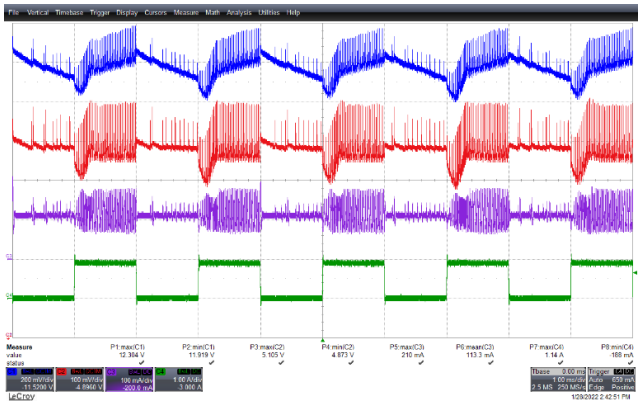


Figure 41 – 0 A – 0.9 A, 5 V Load Step Transient Response, 12 V 0.13 A, 265 VAC.
5 V_{MIN}: 4.87 V. 5 V_{MAX}: 5.11 V.
12 V_{MIN}: 11.92 V. 12 V_{MAX}: 12.30 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

11.1.4 5 V Load Transient – No-Load at 12 V Output

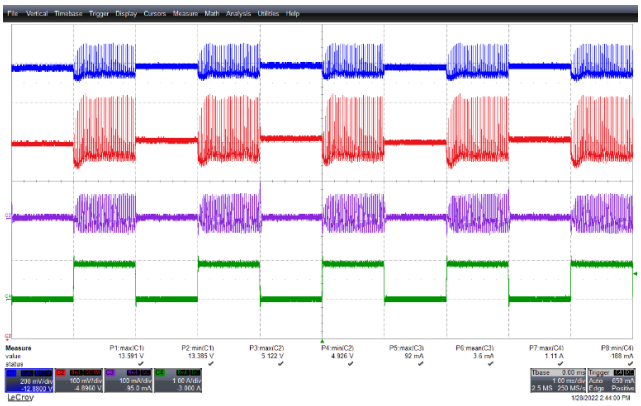


Figure 42 – 0 A – 0.9 A, 5 V Load Step Transient Response, 12 V 0 A, 85 VAC.
5 V_{MIN}: 4.93 V.; 5 V_{MAX}: 5.12 V.
12 V_{MIN}: 13.39 V. 12 V_{MAX}: 13.59 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

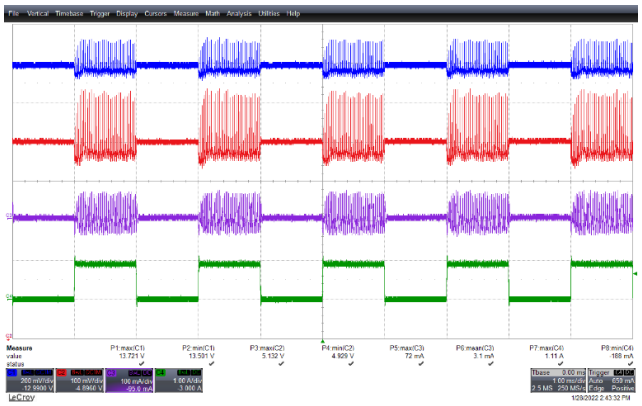


Figure 43 – 0 A – 0.9 A, 5 V Load Step Transient Response, 12 V 0 A, 265 VAC.
5 V_{MIN}: 4.93 V. 5 V_{MAX}: 5.13 V.
12 V_{MIN}: 13.50 V. 12 V_{MAX}: 13.72 V.
Upper: 12 V_{OUT}, 200 mV / div.
Upper Middle: 5 V_{OUT}, 100 mV / div.
Lower Middle: 12 I_{OUT}, 100 mA / div.
Lower: 5 I_{OUT}, 1 A / div., 1 ms / div.

11.2 *Switching Waveforms*

11.2.1 InnoSwitch3-TN Waveforms

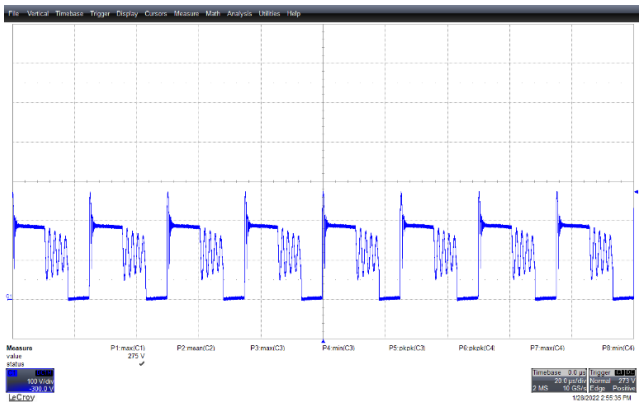


Figure 44 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
CH1: V_{DRAIN}, 100 V / div, 20 µs / div.

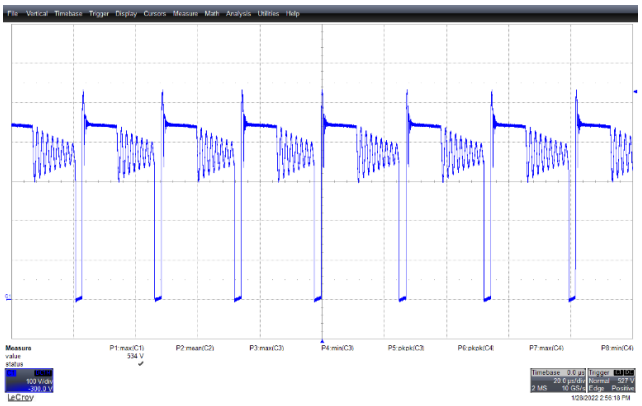


Figure 45 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (534 V_{MAX}).
CH1: V_{DRAIN}, 100 V / div, 20 µs / div.

11.2.2 InnoSwitch3-TN Drain Voltage and Current Waveforms During Start-Up

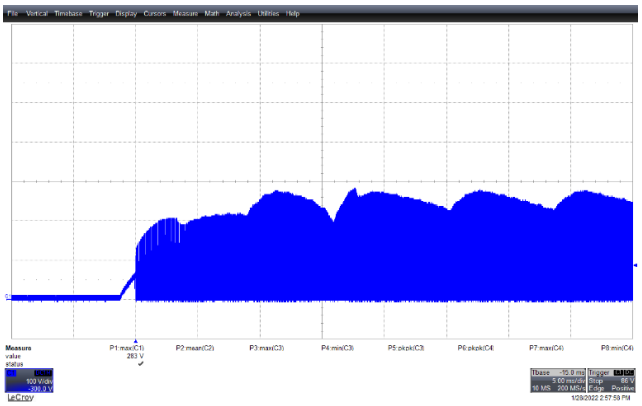


Figure 46 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
CH1: V_{DRAIN}, 100 V / div, 5 ms / div.

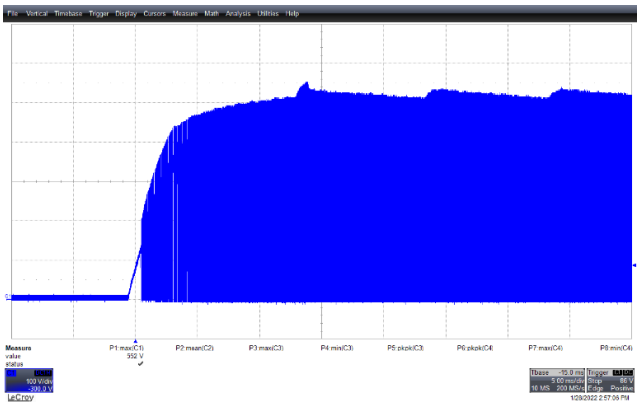


Figure 47 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (552 V_{MAX}).
CH1: V_{DRAIN}, 100 V / div, 5 ms / div.

11.2.3 InnoSwitch3-TN Drain Voltage and Current Waveforms During Output Short-Circuit

Note: 5 V output is shorted

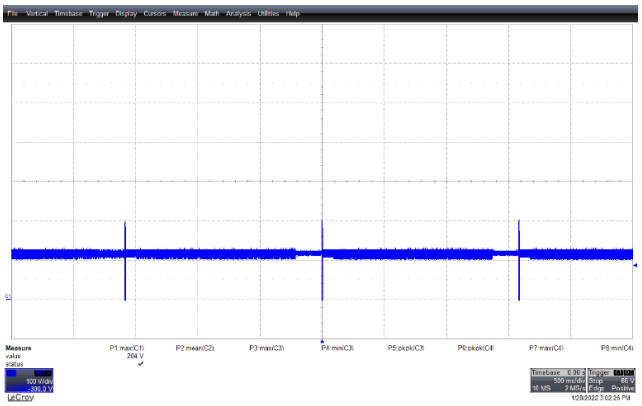


Figure 48 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
CH1: V_{DRAIN}, 100 V / div., 500 ms / div.

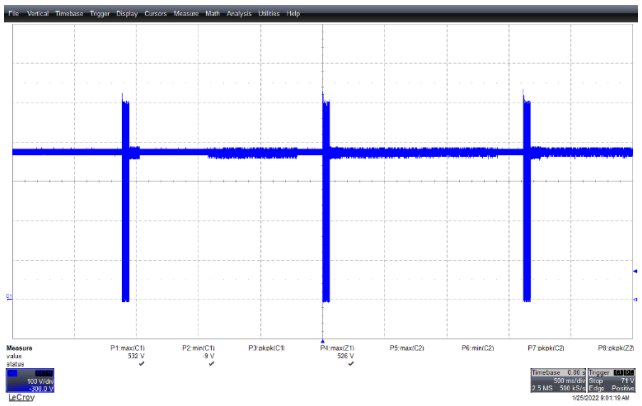


Figure 49 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (532 V_{MAX}).
CH1: V_{DRAIN}, 100 V / div., 500 ms / div.

11.2.4 5 V_{OUT} SR FET and 12 V_{OUT} Schottky Diode Waveforms

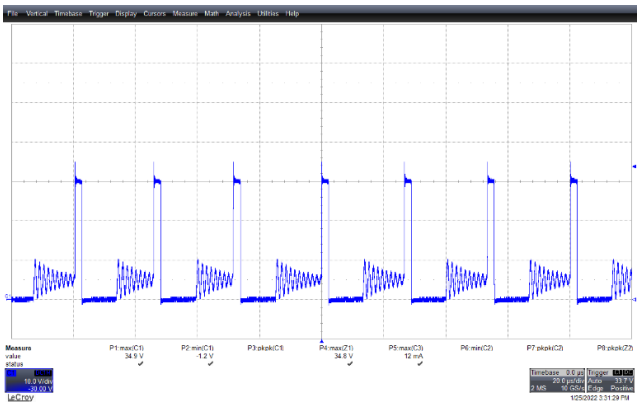


Figure 50 – 5 V SR FET Voltage Waveforms.
265 VAC Input, Full Load.
5 V_{MAX} = 34.9 V.
5 V SR FET V_{MAX}: 10 V / div.
20 µs / div.

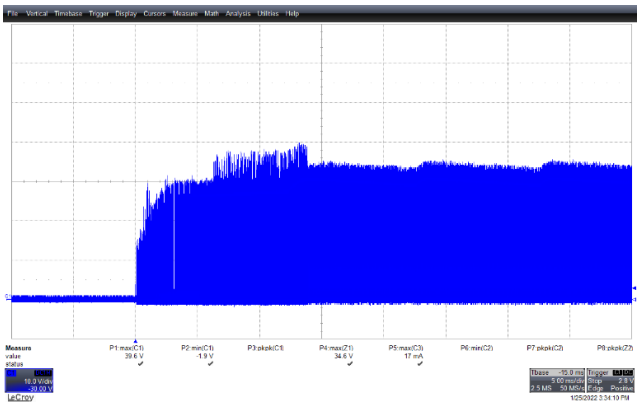


Figure 51 – 5 V FET Voltage Waveforms During Start-Up.
265 VAC Input, Full Load.
5 V_{MAX} = 39.6 V.
5 V SR FET V_{MAX}: 10 V / div.
20 µs / div.

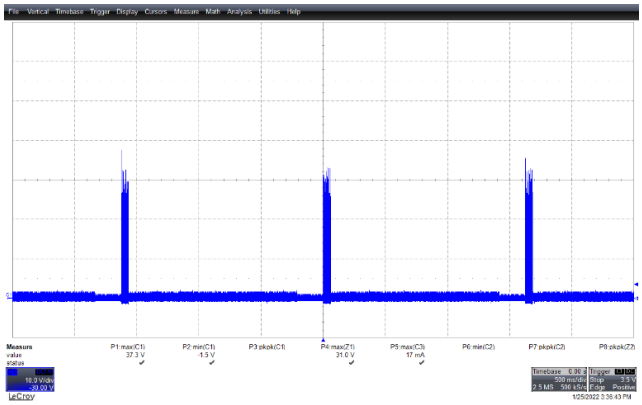


Figure 52 – 5 V SR FET Voltage Waveforms During Output Short-Circuit.
265 VAC Input, Full Load.
5 V_{MAX} = 37.3 V.
5 V SR FET V_{MAX}: 10 V / div.
500 ms / div.

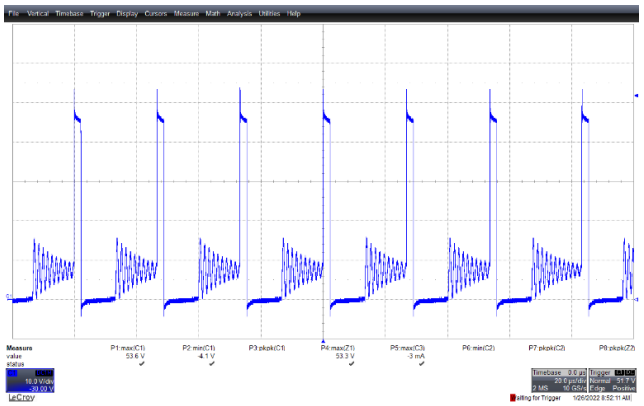


Figure 53 – 12 V Schottky Voltage Waveforms.
265 VAC Input, Full Load.
12 V_{MAX} = 53.6 V.
12 V Schottky V_{MAX}: 10 V / div.
20 µs / div.

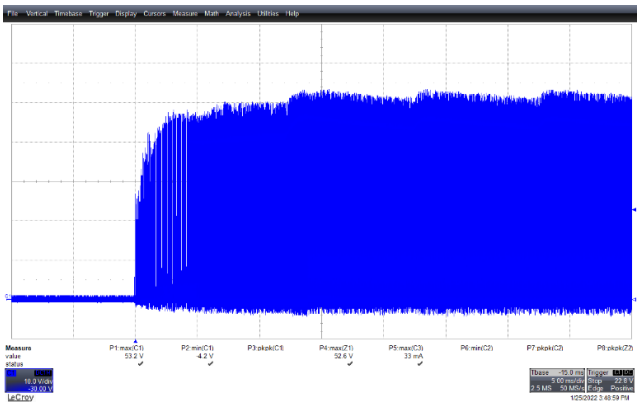


Figure 54 – 5 V Schottky Voltage Waveforms During Start-Up.
265 VAC Input, Full Load.
12 V_{MAX} = 53.2 V.
12 V Schottky V_{MAX}: 10 V / div.
5 ms / div.

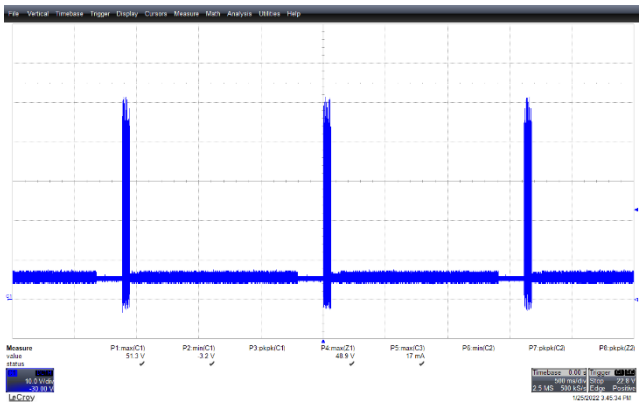


Figure 55 – 5 V Schottky Voltage Waveforms During Output Short-Circuit.
265 VAC Input, Full Load.
12 V_{MAX} = 51.3 V.
12 V Schottky V_{MAX}: 10 V / div.
500 ms / div.

11.2.5 Output Voltage and Current Waveforms During Start-Up

11.2.5.1 Full Load

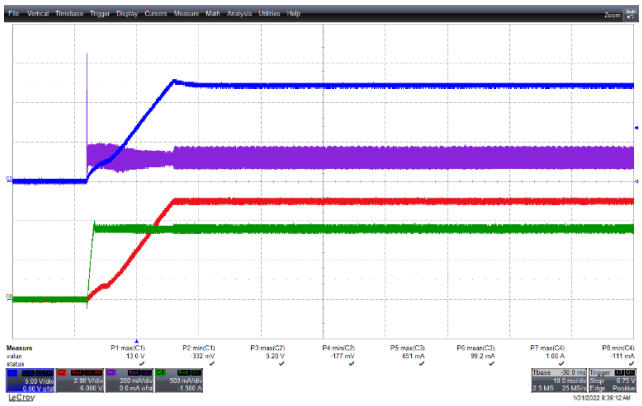


Figure 56 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: 12 V_{OUT}, 5 V / div.
Upper Middle: 12 I_{OUT}, 200 mA / div.
Lower Middle: 5 V_{OUT}, 4 V / div.
Lower: 12 I_{OUT}, 500 mA / div.
10 ms / div.

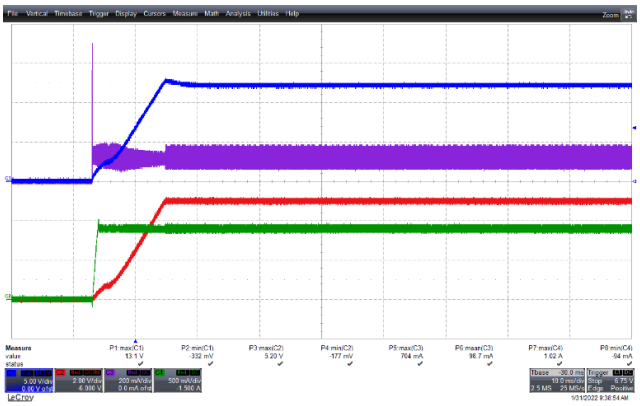


Figure 57 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 12 V_{OUT}, 5 V / div.
Upper Middle: 12 I_{OUT}, 200 mA / div.
Lower Middle: 5 V_{OUT}, 4 V / div.
Lower: 12 I_{OUT}, 500 mA / div.
10 ms / div.

11.3 *Output Ripple Measurements*

11.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 10 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

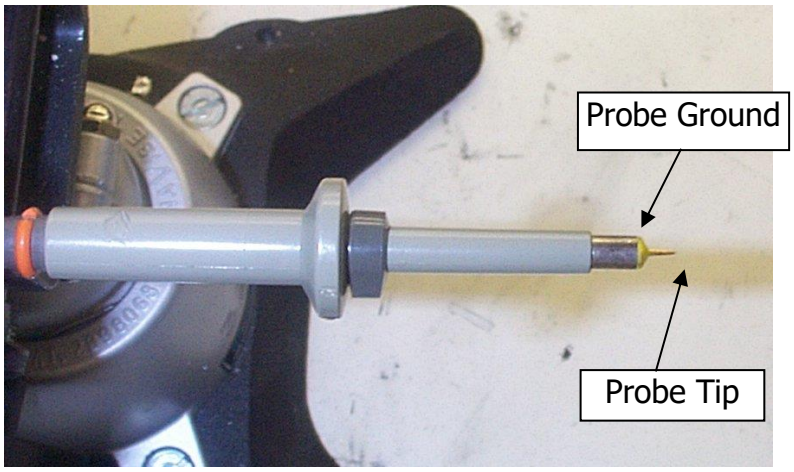


Figure 58 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

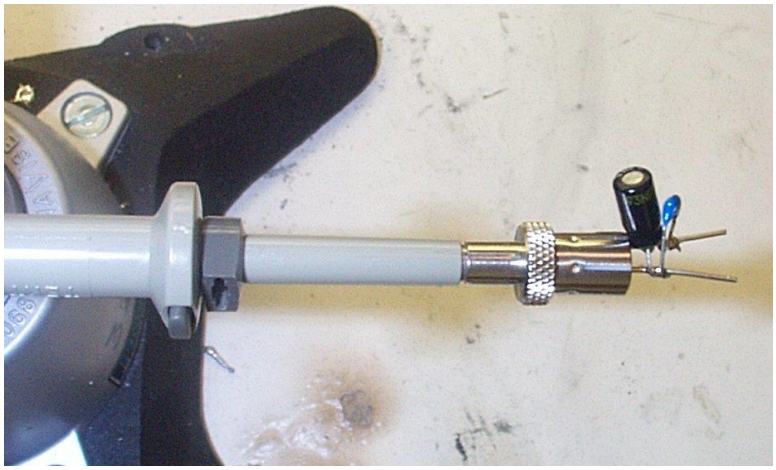


Figure 59 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.3.2 Ripple Voltage Waveforms

Note: Both 5 V and 12 V output are loaded with the same percentage.

11.3.2.1 0% Load

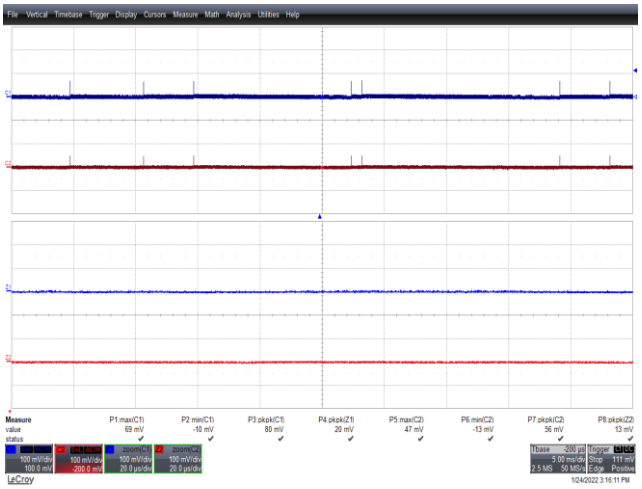


Figure 60 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 80 mV, 5 V_{PK-PK}: 56 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

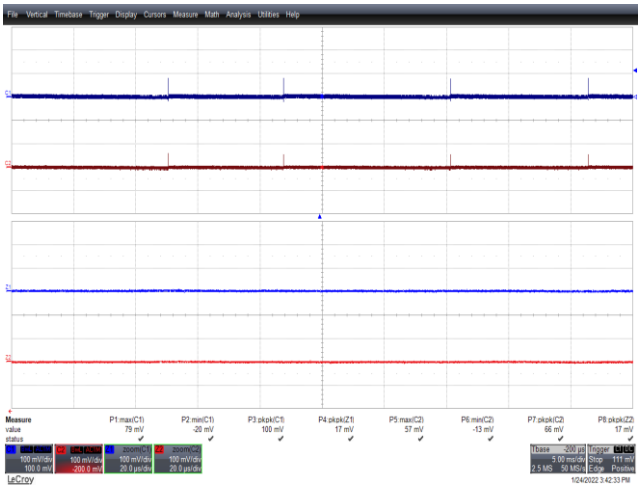


Figure 61 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 100 mV, 5 V_{PK-PK}: 66 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

11.3.2.2 25% Load

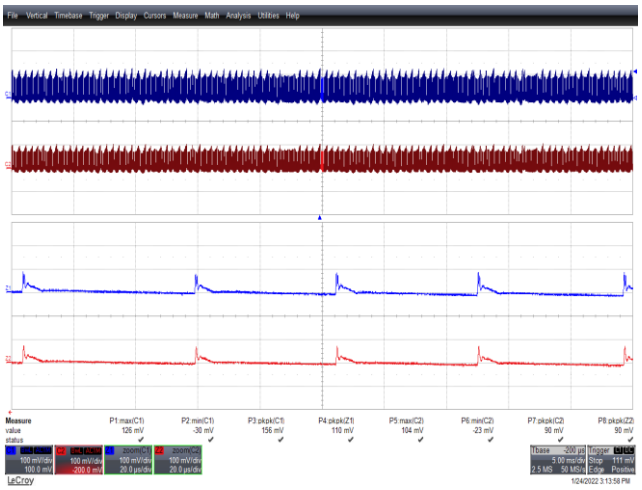


Figure 62 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 156 mV, 5 V_{PK-PK}: 90 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

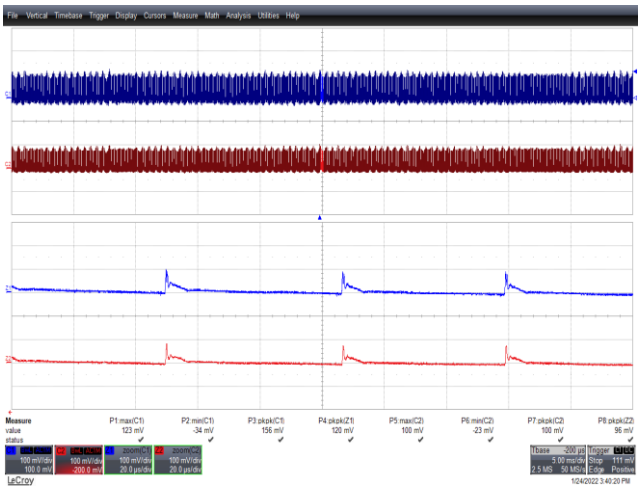


Figure 63 – Output Ripple Voltage Waveforms.
265 VAC Input.
12 V_{PK-PK}: 156 mV, 5 V_{PK-PK}: 100 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

11.3.2.3 50% Load

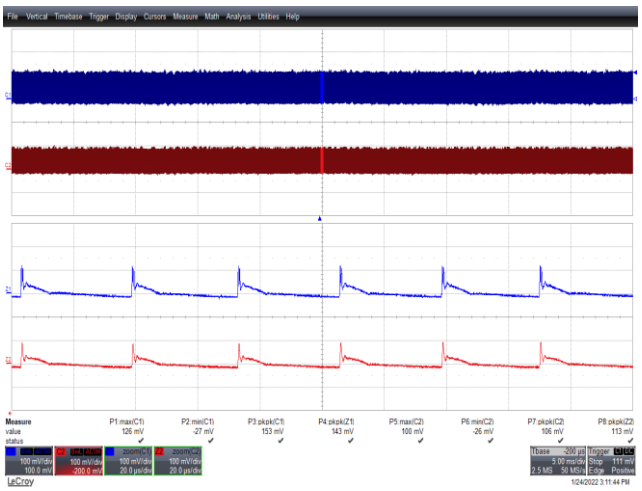


Figure 64 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 153 mV, 5 V_{PK-PK}: 106 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

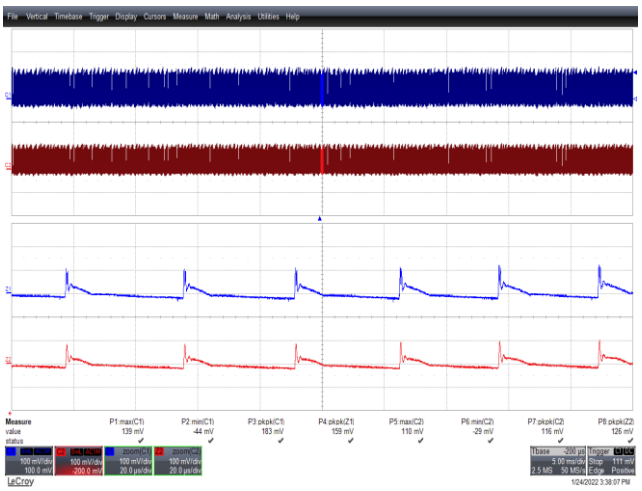


Figure 65 – Output Ripple Voltage Waveforms.
265 VAC Input.
12 V_{PK-PK}: 183 mV, 5 V_{PK-PK}: 116 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

11.3.2.4 75% Load

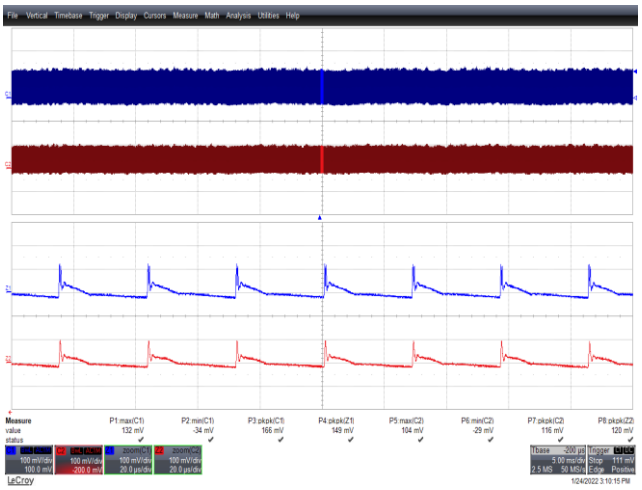


Figure 66 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 166 mV, 5 V_{PK-PK}: 116 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

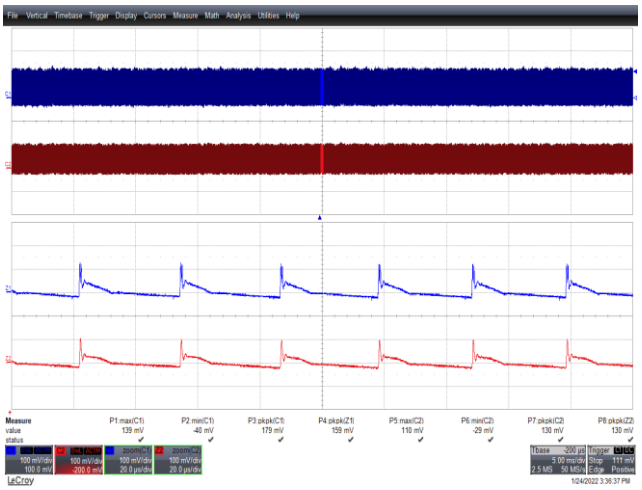


Figure 67 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 139 mV, 5 V_{PK-PK}: 130 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

11.3.2.5 100% Load

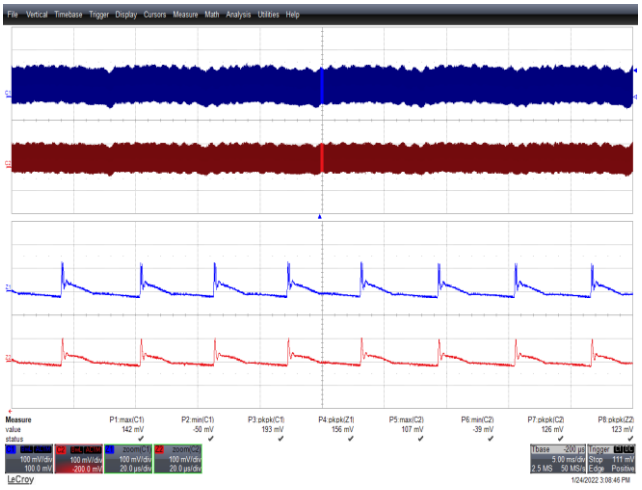


Figure 68 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 193 mV, 5 V_{PK-PK}: 126 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

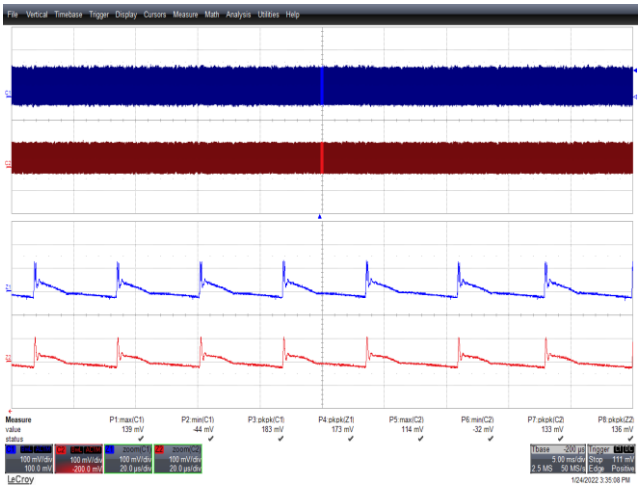


Figure 69 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 183 mV, 5 V_{PK-PK}: 133 mV.
Upper: 12 V_{OUT}, 100 mV / div., 5 ms / div.
Lower: 5 V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 20 µs / div.

11.3.3 Ripple (ATE Measurements)

Note: Both 5 V and 12 V output are loaded with the same percentage.

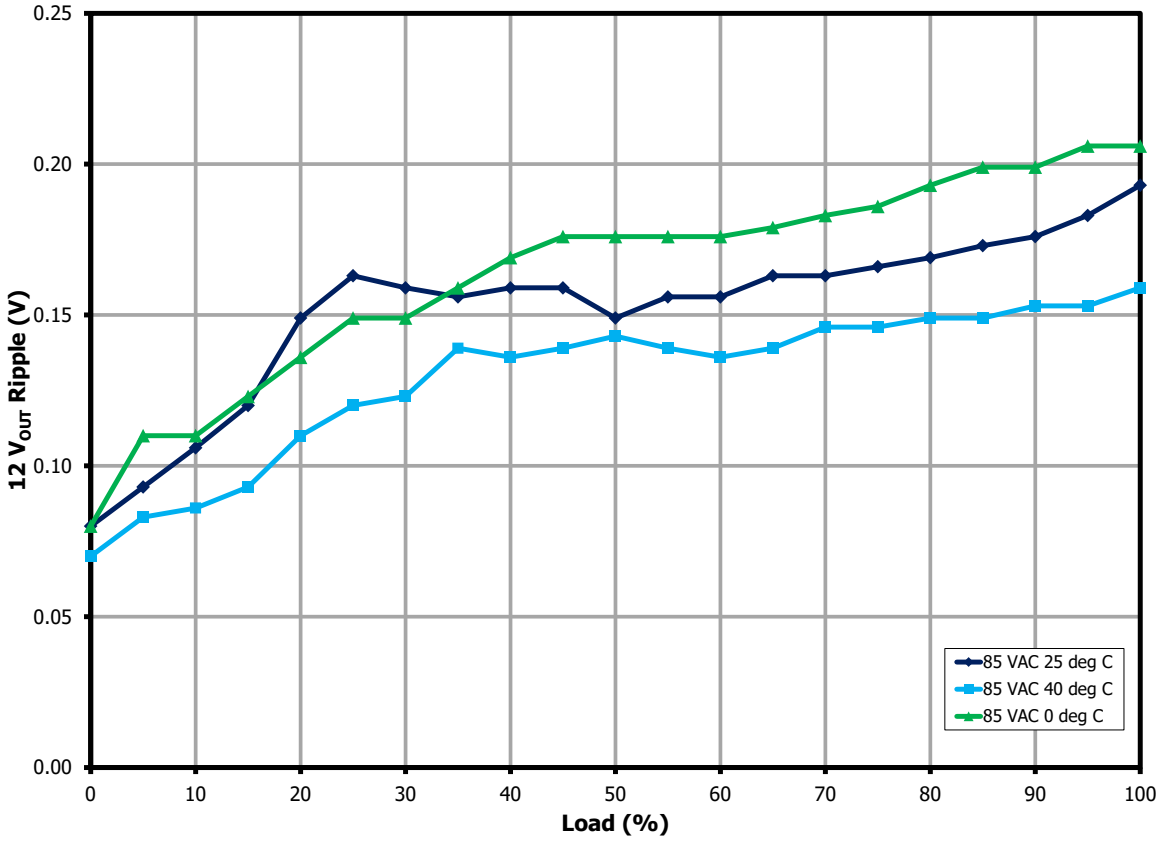


Figure 70 – 12 V Output Voltage Ripple vs. Output Load, 85 VAC Input.

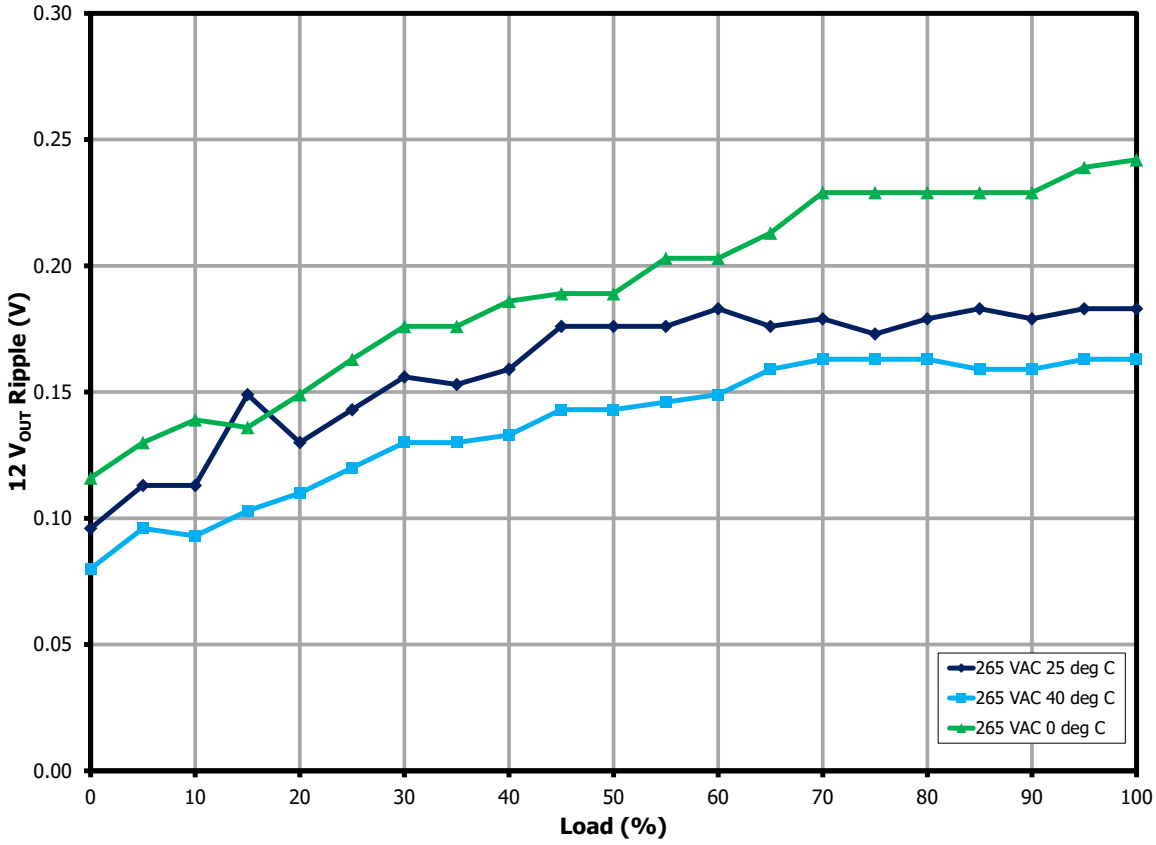


Figure 71 – 12 V Output Voltage Ripple vs. Output Load, 265 VAC Input.

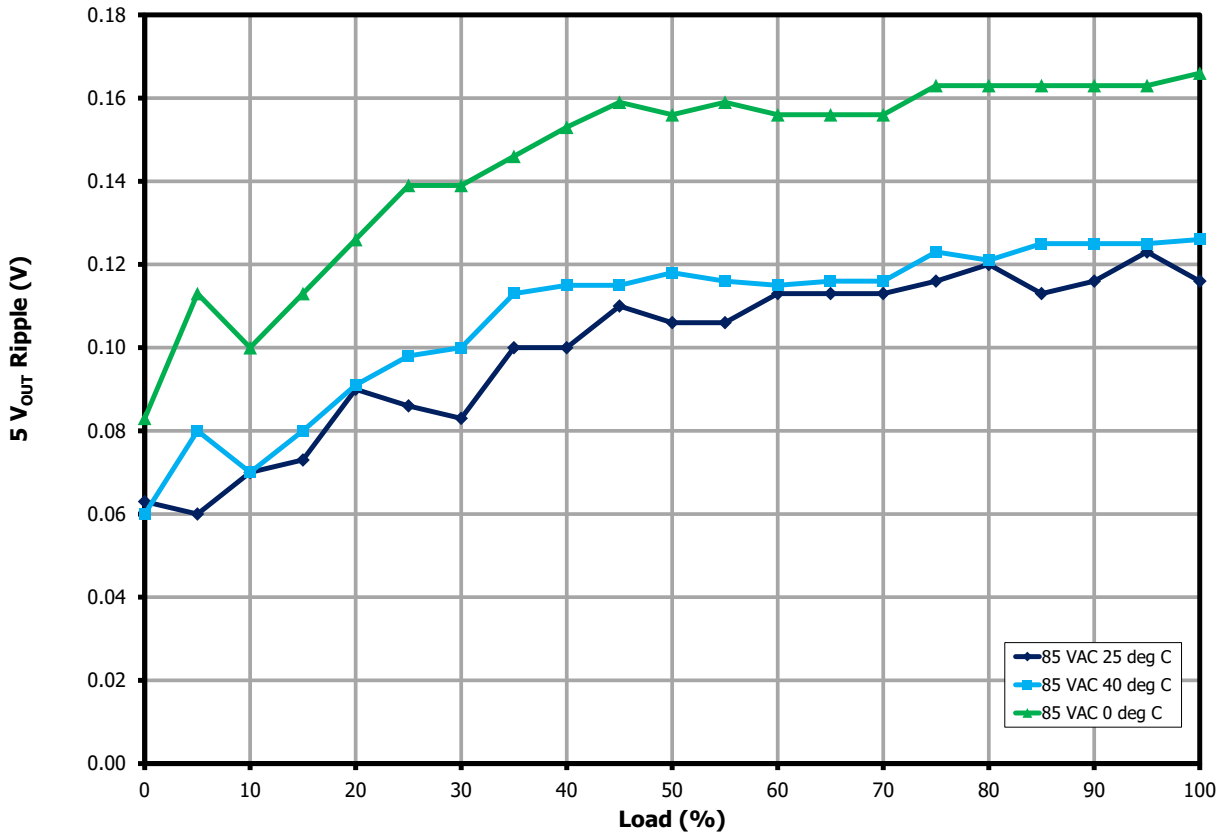


Figure 72 – 5 V Output Voltage Ripple vs. Output Load, 85 VAC Input.

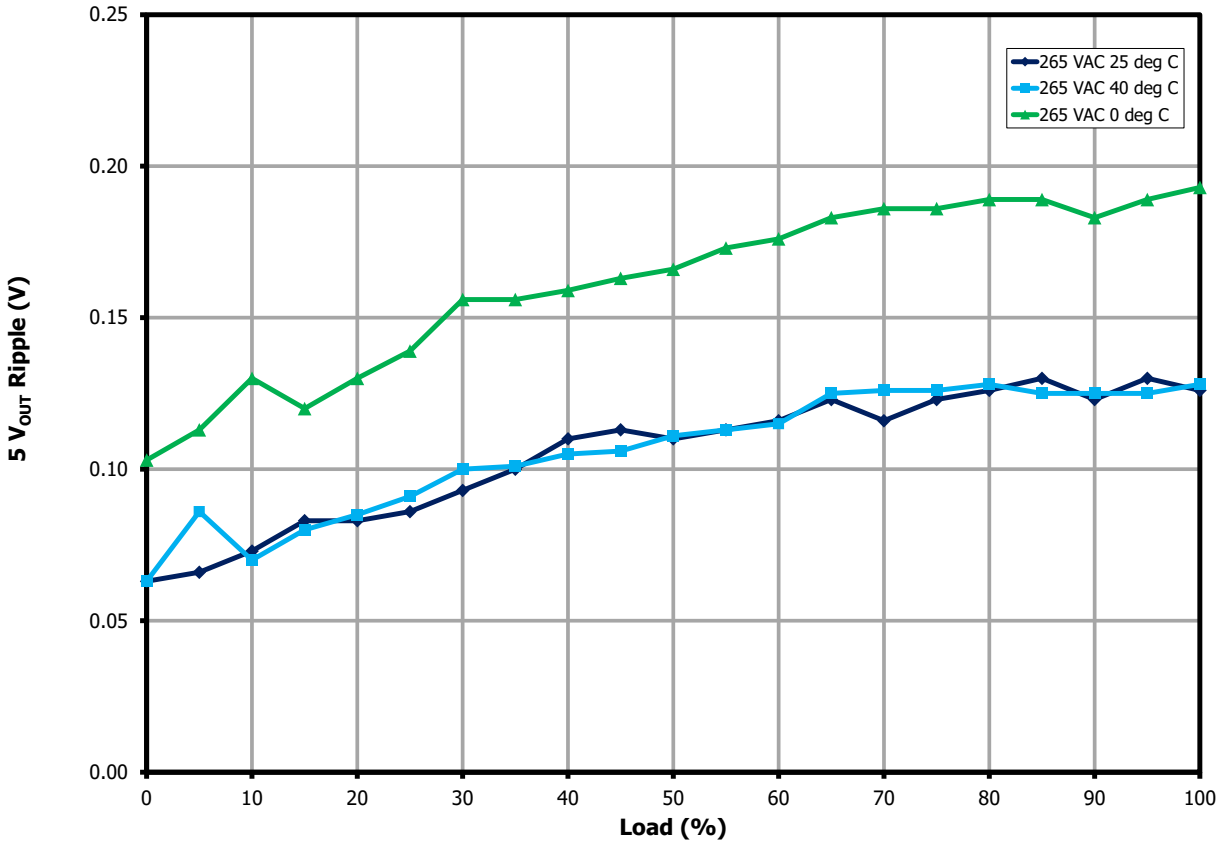


Figure 73 – 12 V Output Voltage Ripple vs. Output Load, 265 VAC Input.

12 EMI

12.1 *Conductive EMI*

12.1.1 Floating Output (QP / AV)

12.1.1.1 115 VAC Input

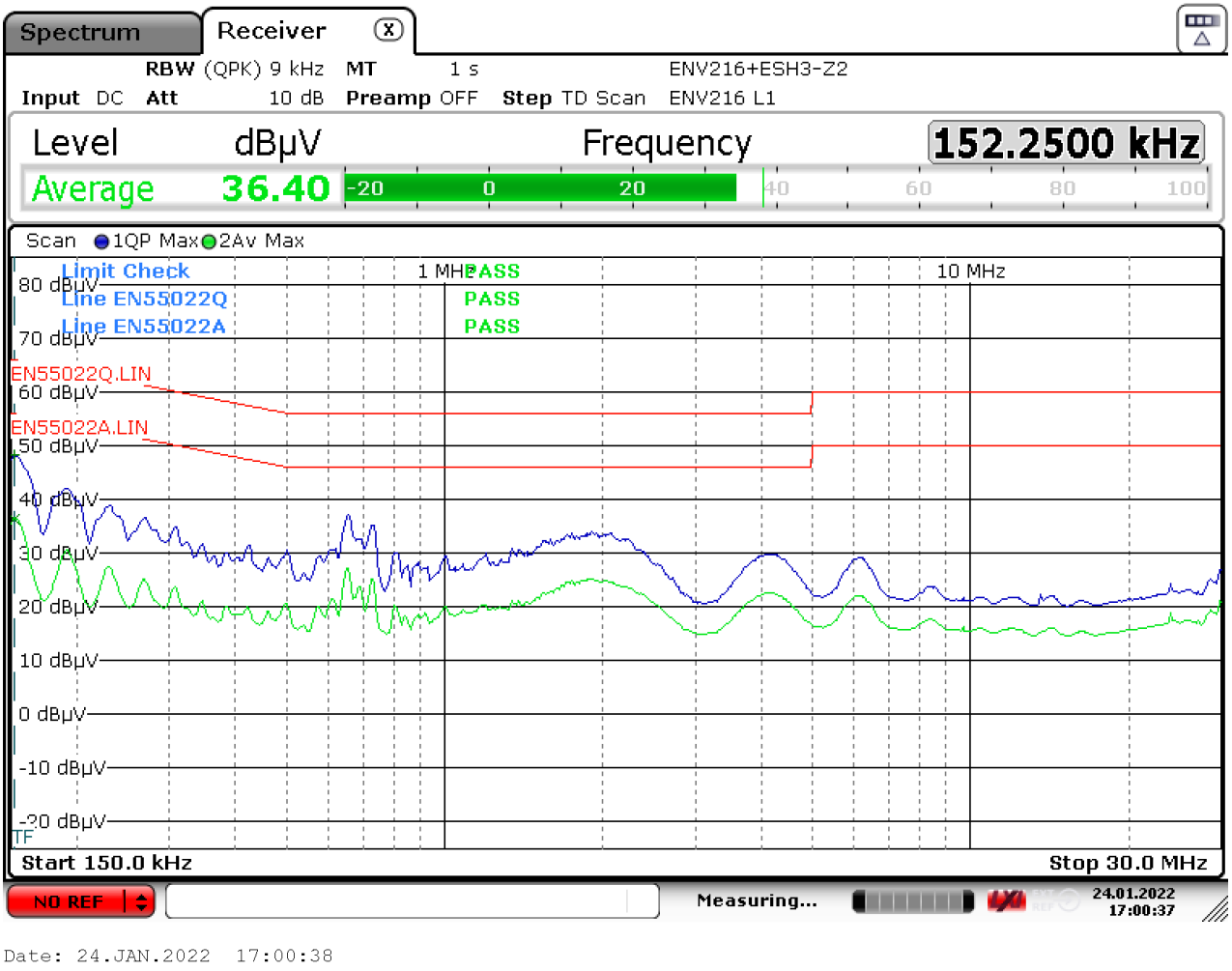
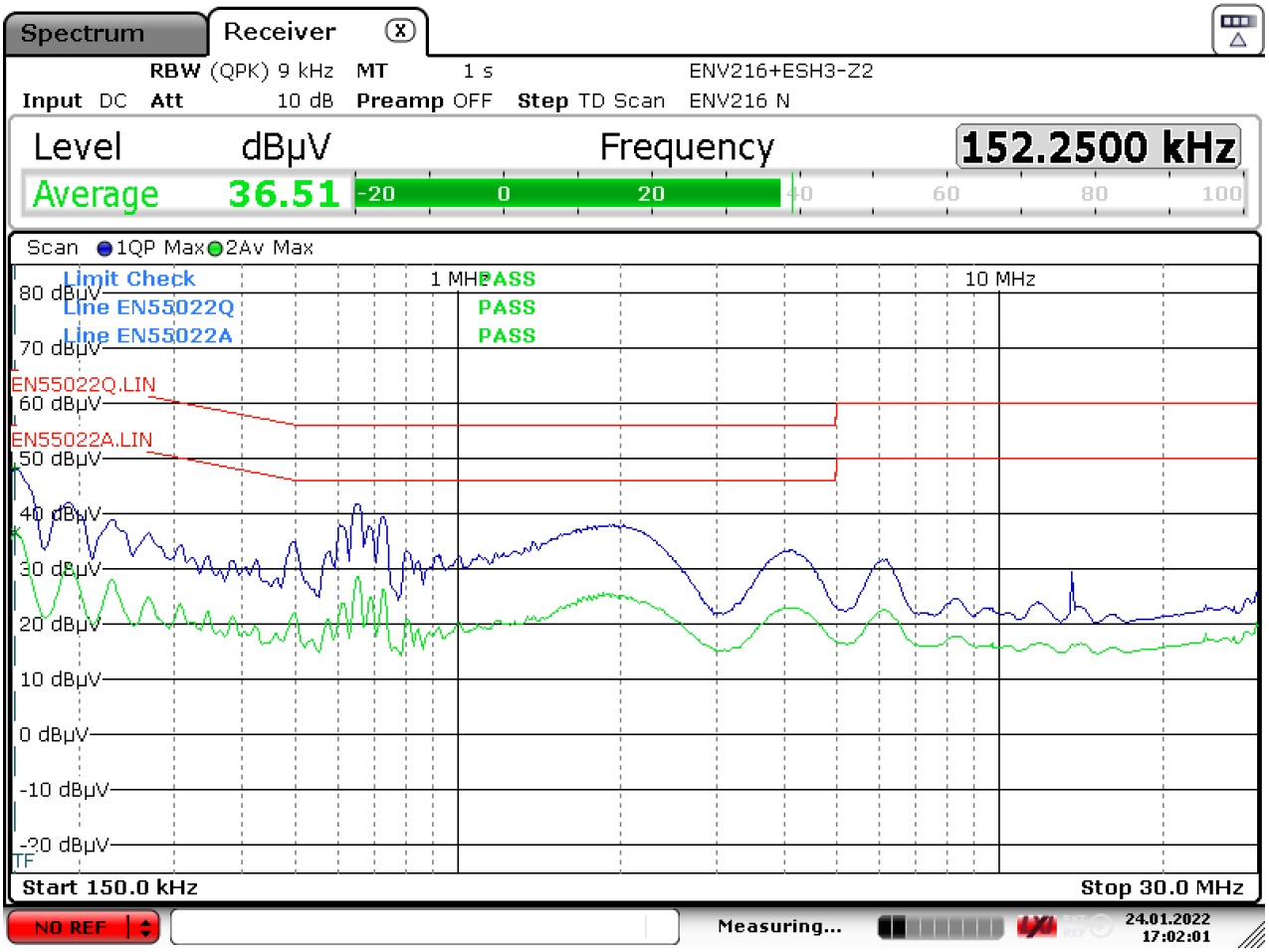


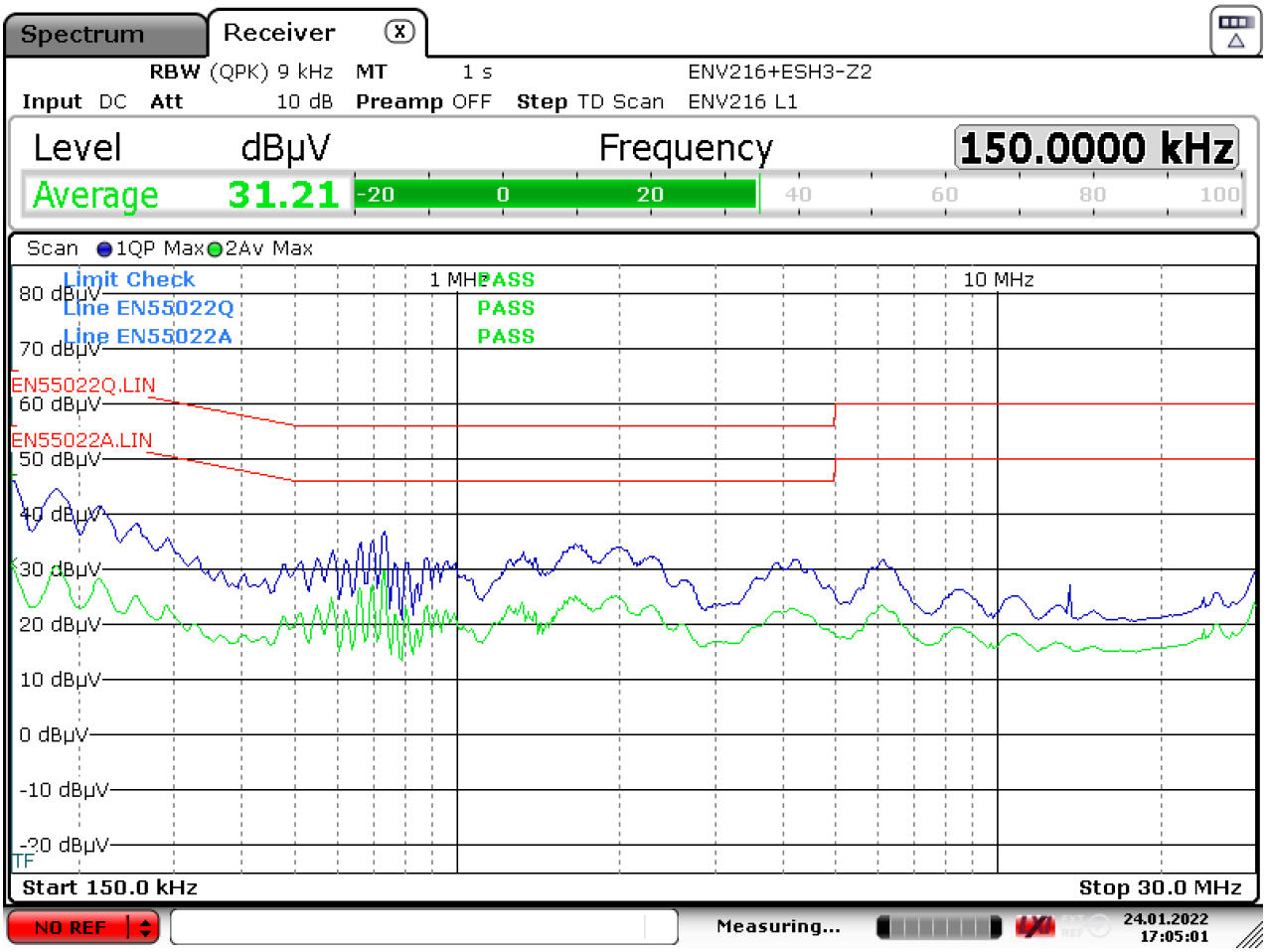
Figure 74 – Floating Ground - 115 VAC Line.



Date: 24.JAN.2022 17:02:02

Figure 75 – Floating Ground - 115 VAC Neutral.

12.1.1.2 230 VAC Input



Date: 24.JAN.2022 17:05:01

Figure 76 – Floating Ground - 230 VAC Line.

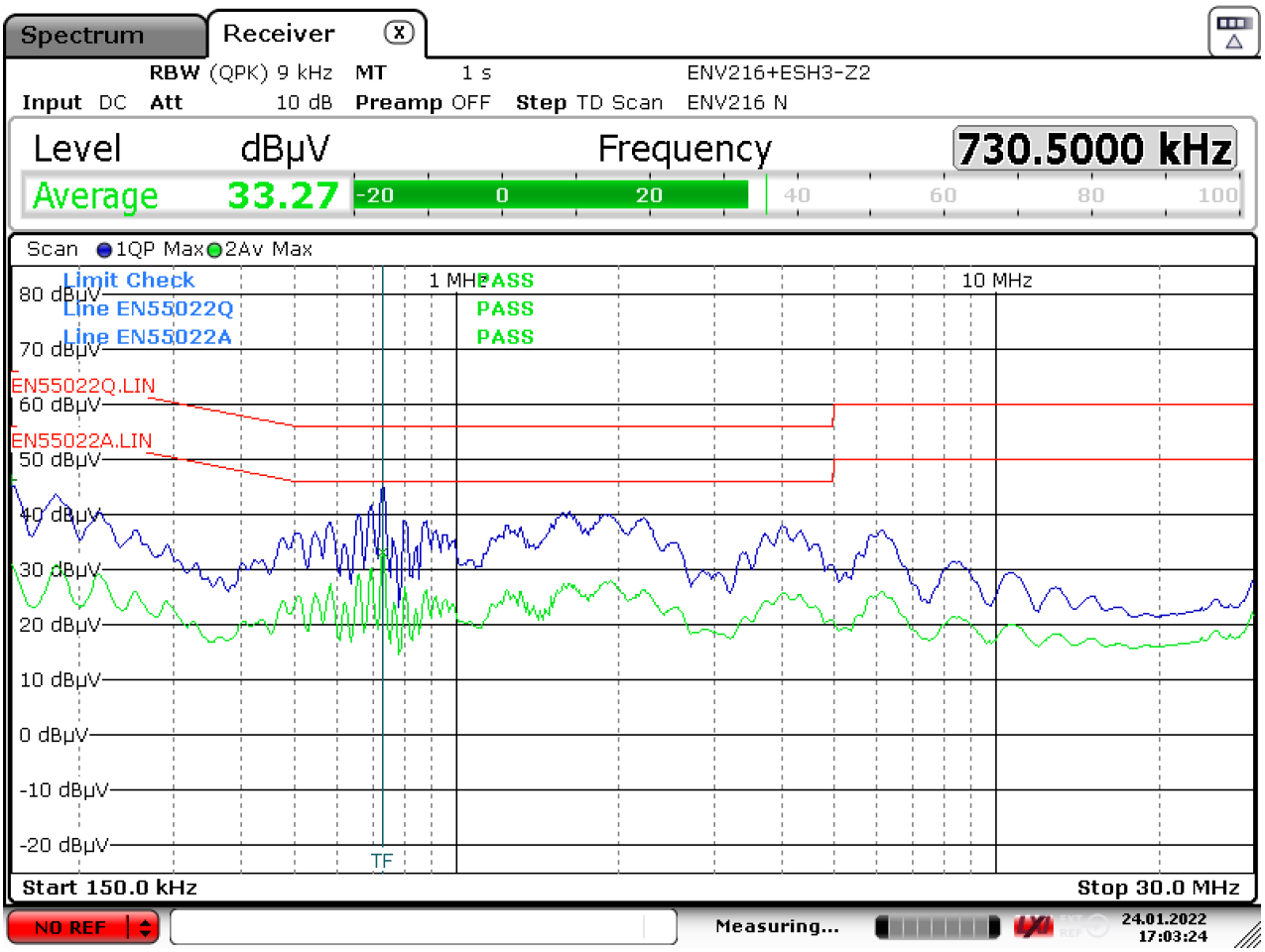


Figure 77 – Floating Ground - 230 VAC Neutral.

13 Lighting Surge Test

13.1 *Differential Surge Test*

Note: To pass 1 kV differential mode surge test the size of both input capacitors, C1 and C2, needs to be increased to 15 µF and add 10 Ω 0.7 A thermistor in series with Neutral Test Point.

Passed ±1 kV, 500 A surge test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
1	0	L, N	2	10	PASS (No AR)
-1	0	L, N	2	10	PASS (No AR)
1	90	L, N	2	10	PASS (No AR)
-1	90	L, N	2	10	PASS (No AR)
1	180	L, N	2	10	PASS (No AR)
-1	180	L, N	2	10	PASS (No AR)
1	270	L, N	2	10	PASS (No AR)
-1	270	L, N	2	10	PASS (No AR)

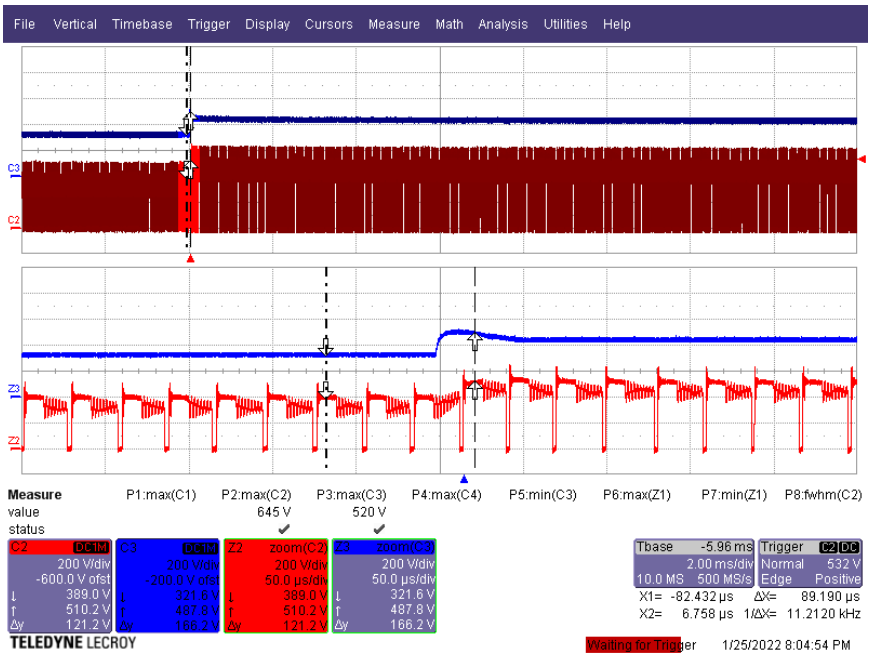


Figure 78 – 1 kV Differential Mode Surge Test.
InnoSwitch3-TN $V_{DS(MAX)}$: 645 V, $V_{BULK(MAX)}$: 520 V.
Upper: V_{BULK}, 200 V / div, 2 ms / div.
Lower: InnoSwitch3-TN V_{DS}, 200 V / div, 2 ms / div.
Zoom: 50 µs / div.

13.2 *Ring Wave Test*

Note: To pass 6 kV Ring Wave test the size of both input capacitors, C1 and C2, needs to be increased to 15 μF and add 10 Ω 0.7 A thermistor in series with Neutral Test point.

Passed ±6 kV Ring Wave Test

Ring Wave Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
4	0	L, N	12	10	PASS (No AR)
-4	0	L, N	12	10	PASS (No AR)
4	90	L, N	12	10	PASS (No AR)
-4	90	L, N	12	10	PASS (No AR)
4	180	L, N	12	10	PASS (No AR)
-4	180	L, N	12	10	PASS (No AR)
4	270	L, N	12	10	PASS (No AR)
-4	270	L, N	12	10	PASS (No AR)
5	0	L, N	12	10	PASS (No AR)
-5	0	L, N	12	10	PASS (No AR)
5	90	L, N	12	10	PASS (No AR)
-5	90	L, N	12	10	PASS (No AR)
5	180	L, N	12	10	PASS (No AR)
-5	180	L, N	12	10	PASS (No AR)
5	270	L, N	12	10	PASS (No AR)
-5	270	L, N	12	10	PASS (No AR)
6	0	L, N	12	10	PASS (No AR)
-6	0	L, N	12	10	PASS (No AR)
6	90	L, N	12	10	PASS (No AR)
-6	90	L, N	12	10	PASS (No AR)
6	180	L, N	12	10	PASS (No AR)
-6	180	L, N	12	10	PASS (No AR)
6	270	L, N	12	10	PASS (No AR)
-6	270	L, N	12	10	PASS (No AR)

Figure 79 – 6 kV Ring Wave Test.
InnoSwitch3-TN $V_{DS(MAX)}$: 478, $V_{BULK(MAX)}$: 393 V.
Upper: V_{BULK}, 200 V / div, 20 ms / div.
Lower: InnoSwitch3-TN V_{DS}, 100 V / div, 20 ms / div.
Zoom: 200 µs / div.

13.3 *EFT / Burst Test*

Note: To pass 4 kV EFT test the size of both input capacitors, C1 and C2, needs to be increased to 15 µF and add 10 Ω 0.7 A thermistor in series with Neutral Test point.

Passed ±4 kV EFT Test

EFT Voltage (kV)	Phase Angle (°)	Frequency (kHz)	T-Burst	T-Rep	Coupling	Test Result
4	0	5	15 ms	120 s	L, N	PASS (No AR)
-4	0	5	15 ms	120 s	L, N	PASS (No AR)
4	0	100	750 us	120 s	L, N	PASS (No AR)
-4	0	100	750 us	120 s	L, N	PASS (No AR)
4	90	5	15 ms	120 s	L, N	PASS (No AR)
-4	90	5	15 ms	120 s	L, N	PASS (No AR)
4	90	100	750 us	120 s	L, N	PASS (No AR)
-4	90	100	750 us	120 s	L, N	PASS (No AR)
4	180	5	15 ms	120 s	L, N	PASS (No AR)
-4	180	5	15 ms	120 s	L, N	PASS (No AR)
4	180	100	750 us	120 s	L, N	PASS (No AR)
-4	180	100	750 us	120 s	L, N	PASS (No AR)
4	270	5	15 ms	120 s	L, N	PASS (No AR)
-4	270	5	15 ms	120 s	L, N	PASS (No AR)
4	270	100	750 us	120 s	L, N	PASS (No AR)
-4	270	100	750 us	120 s	L, N	PASS (No AR)

Figure 80 – 4 kV EFT Test.
InnoSwitch3-TN $V_{DS(MAX)}$: 478, $V_{BULK(MAX)}$: 406 V.
Upper: V_{BULK}, 200 V / div, 20 ms / div.
Lower: InnoSwitch3-TN V_{DS}, 100 V / div, 20 ms / div.
Zoom: 200 µs / div.

14 Appendix

14.1 *Primary Winding – Conventional vs. Sectional Winding Comparison*

14.1.1 Transformer Construction Comparison

Note: Both transformers have identical transformer parameters, only the Primary winding construction are different.

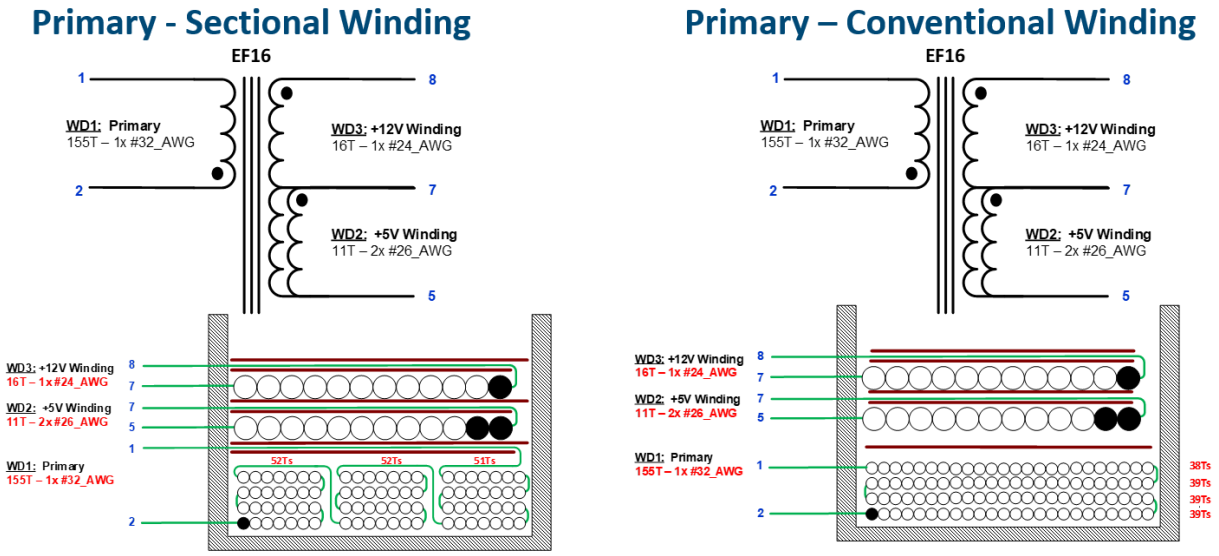
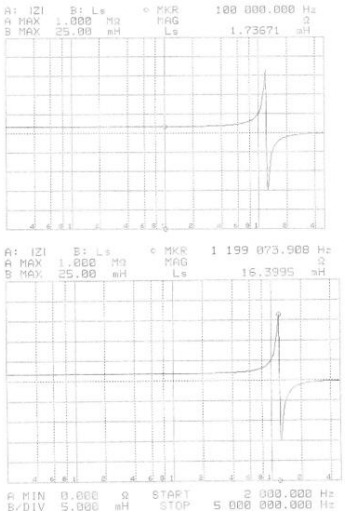


Figure 81 – Transformer Construction (Conventional vs. Sectional).

14.1.2 Transformer Electrical Parameters Comparison

Primary - Sectional Winding

Lp – 1.73mH
RSF – 1199kHz
Lk – 61.43uH



Primary – Conventional Winding

Lp – 1.77mH
RSF – 666kHz
Lk – 46.53uH

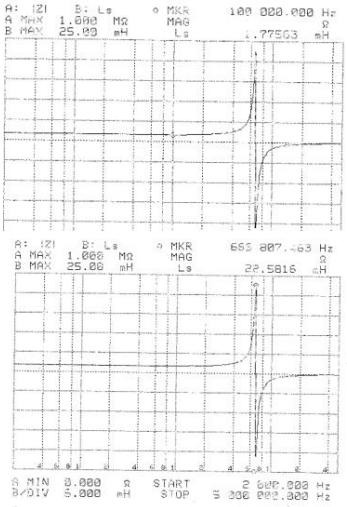


Figure 82 – Transformer Electrical Parameters Comparison.

Sectional Winding has greater resonant frequency, reducing the effective capacitance compared with the Conventional Winding.

14.1.3 Performance Comparison

14.1.3.1 Efficiency vs. Line

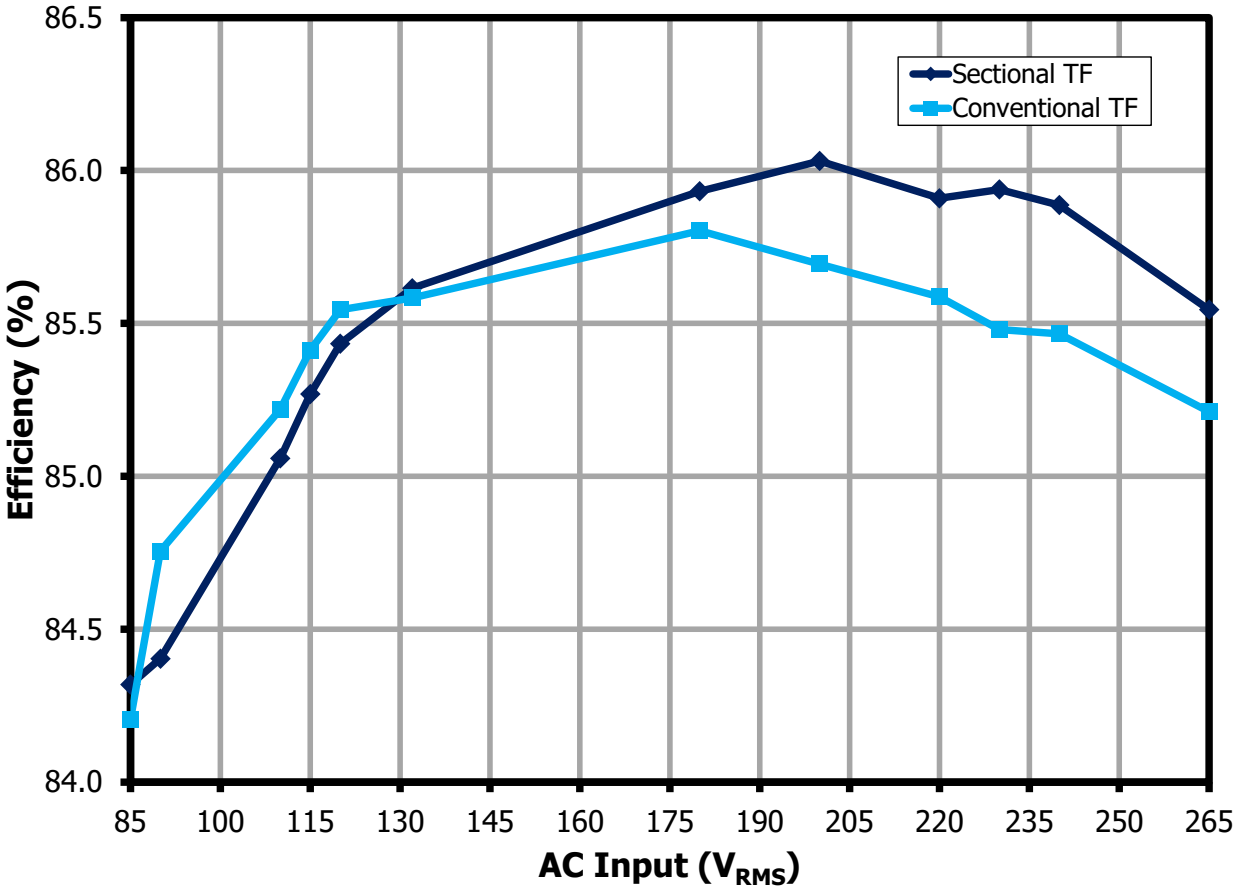


Figure 83 – Efficiency vs. Line.

14.1.3.2 Standby Efficiency vs. Line (5 V / 30 mA)

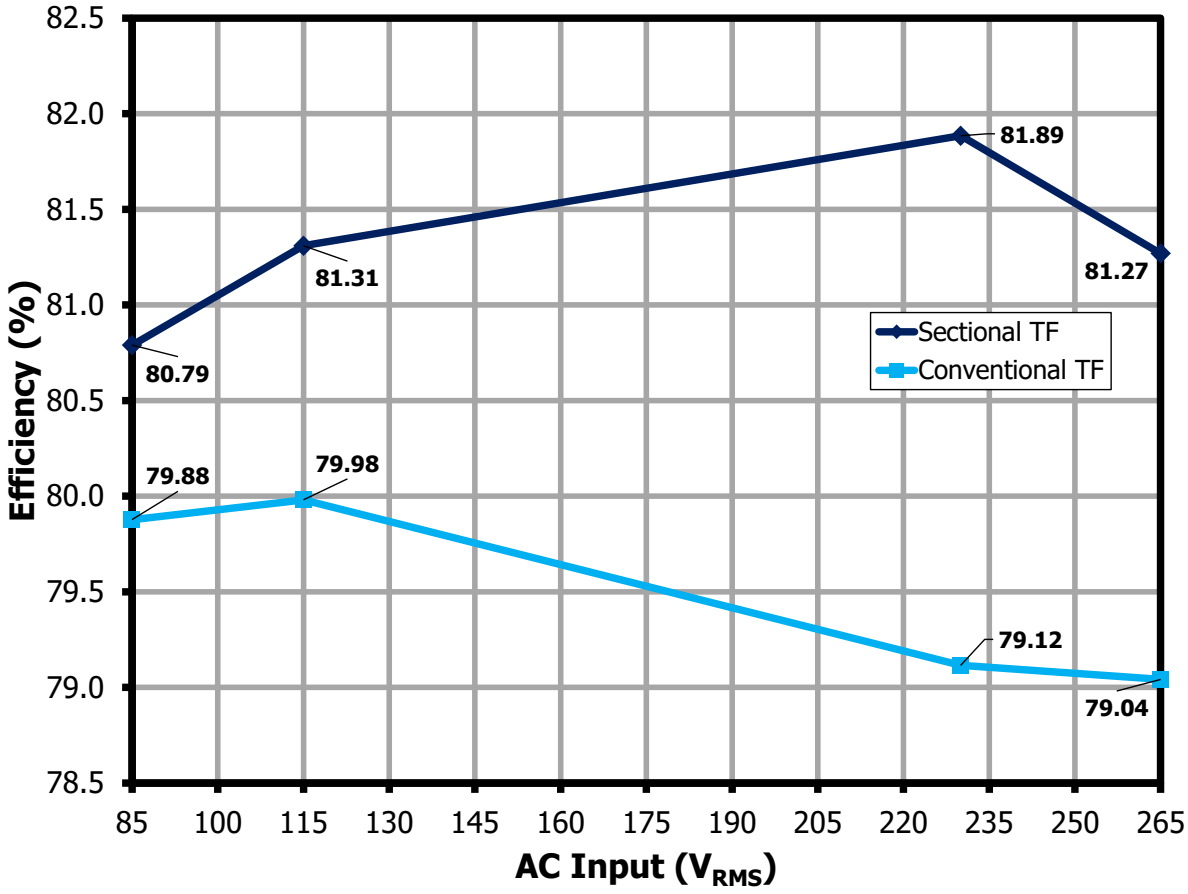


Figure 84 – Standby Efficiency vs. Line.

14.1.3.3 No-Load Input Power at 230 VAC Input

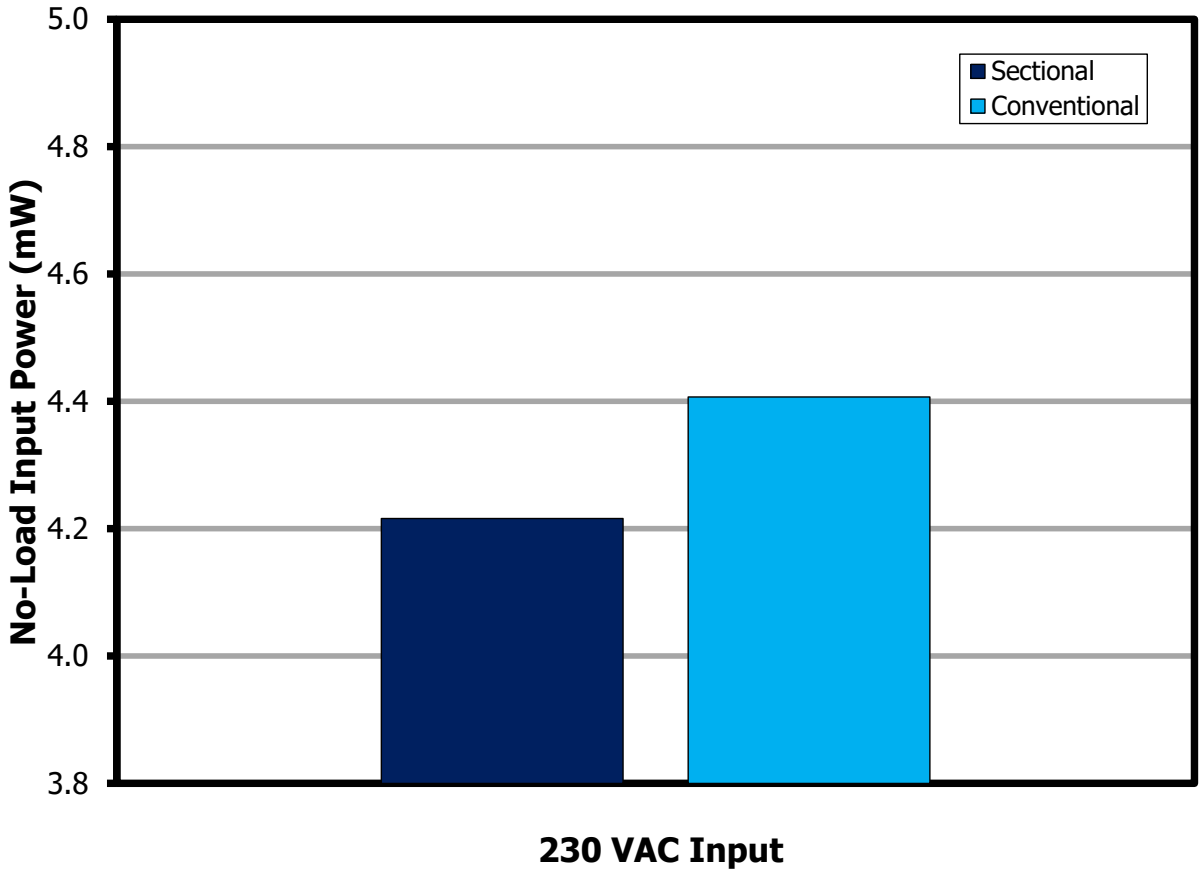


Figure 85 – No-Load Input Power.

14.1.3.4 Standby Input Power (5 V / 30 mA)

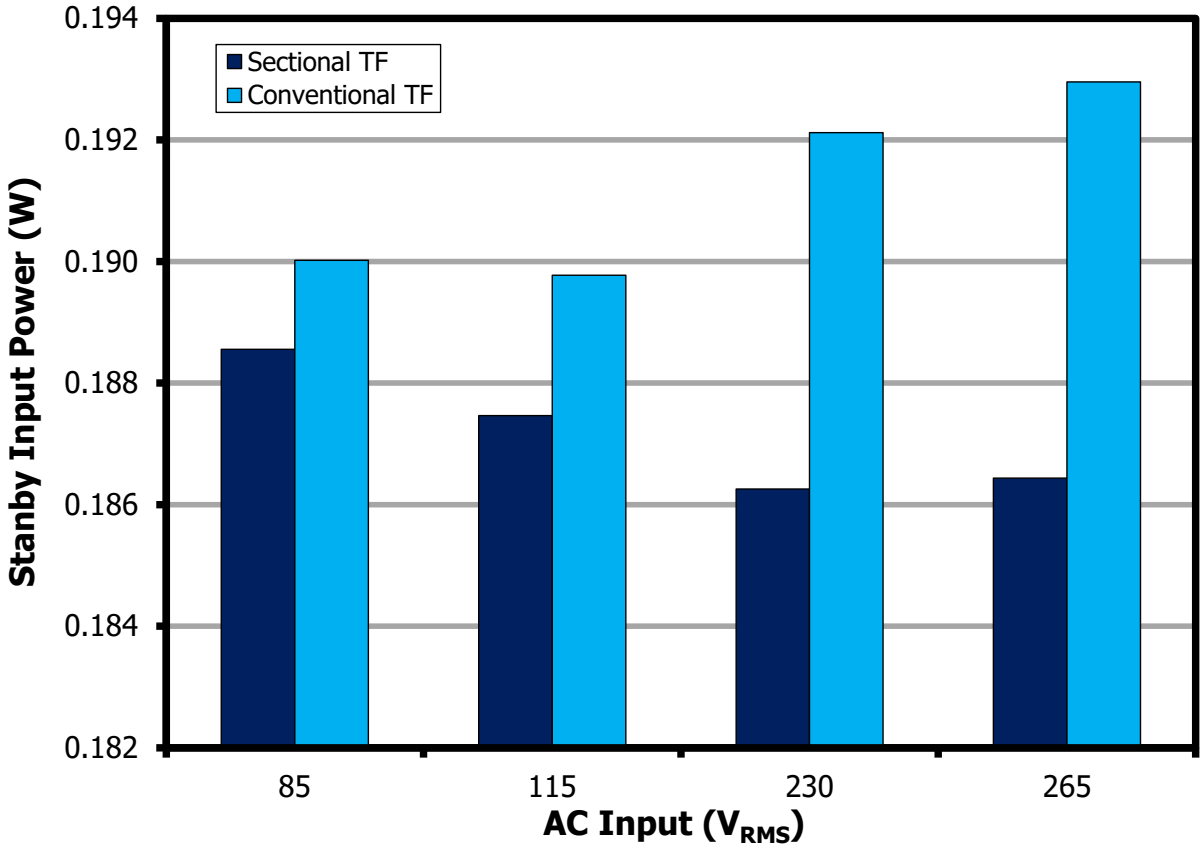


Figure 86 – Standby Input Power (5 V / 30 mA).

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
06-Apr-22	MA	1.0	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

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