Design Example Report

Title	***5 W Single Output Power Supply with Low No-Load Input Power (<5 mW), Isolated Flyback, Using InnoSwitch™3-TN INN3072M***
Specification	85 VAC – 265 VAC Input; 5 V, 1 A Output
Application	Open Frame Appliance Power Supply
Author	Applications Engineering Department
Document Number	DER-967
Date	June 21, 2022
Revision	1.0

Summary and Features

- 5 W output from 85 VAC to 265 VAC
- Built in synchronous rectification for >85 % efficiency at nominal AC input
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- <5 mW no-load input power at 230 VAC input
- <200 mW standby input power at 5 V / 30 mA load
- Accurate thermal protection with hysteretic shutdown

Power Integrations

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Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 1 A, 5 V isolated single output embedded power supply utilizing INN3072M from the InnoSwitch3-TN family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

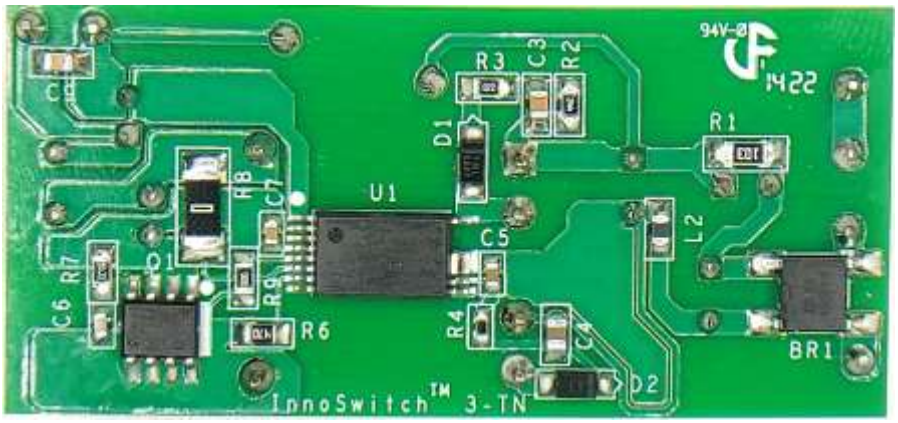


Figure 1 – Populated Circuit Board Photograph, Top.

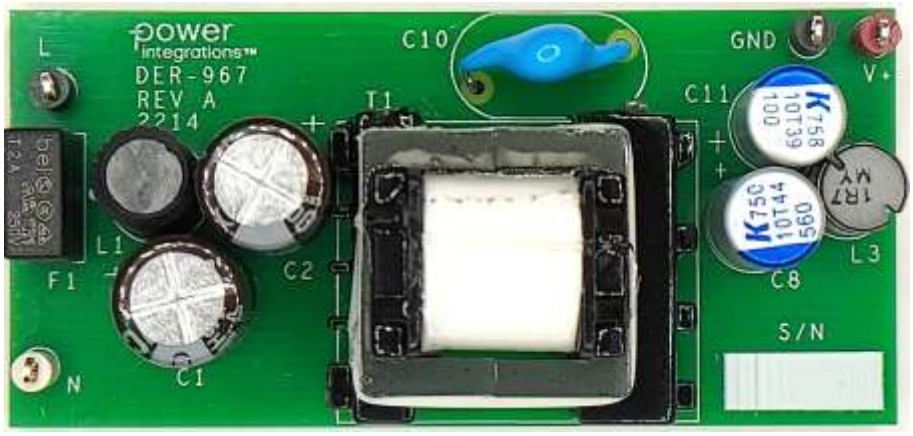


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115/230	265	VAC	2 Wire Input.
Frequency	f_{LINE}		50/60		Hz	
No-Load Input Power				5	mW	@ 230 VAC Input.
Standby Power (5 V / 30 mA)			200	300	mW	
Output						
Output Voltage	V_{OUT}	4.75	5	5.25	V	±5 %
Output Ripple Voltage	V_{RIPPLE}			50	mV	20 MHz Bandwidth. <50 mV_{PP} at Room Temperature.
Output Current	I_{OUT}	0	1		A	
Total Output Power						
Continuous Output Power	P_{OUT}			5	W	
Efficiency						
Average	$\eta_{AVE[BRD]}$	85			%	Measured at 115 / 230 VAC, Room Temperature.
25%, 50%, 75%, and 100%						
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B Load Floating				Measured at 115 / 230 VAC
Safety		Designed to meet IEC950, UL1950 Class II				
Surge						
Differential		1			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω.
Ring Wave		6			kV	100 kHz Ring Wave, 12 Ω Common Mode.
EFT		2			kV	15 ms @ 5 kHz. 0.75 ms @ 100 kHz.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

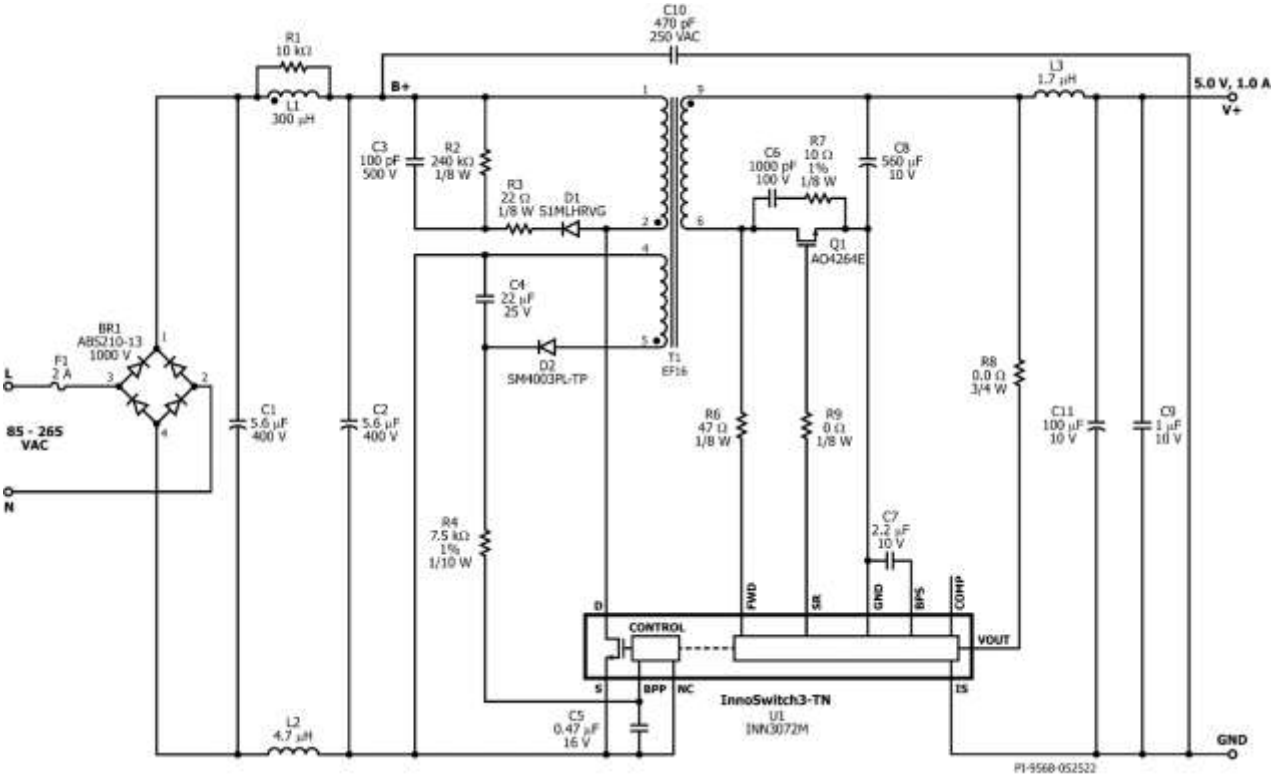


Figure 3 – Schematic.

4 Circuit Description

4.1 Input EMI Filtering

Fuse F1 isolates the circuit and provides protection from component failure.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C1 and C2. The differential inductors L1 and L2, with R1 are placed in between input capacitors provide differential noise filtering.

It is necessary to increase the size of both input capacitors, C1 and C2, to 10 μF and add thermistor RT1 to pass differential, ring wave and EFT surge tests.

4.2 InnoSwitch3-TN Primary

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the InnoSwitch3-TN IC (U1).

A low cost RCD clamp formed by D1, R2, R3, and C3 limits the peak drain voltage of U1 due to the effects of transformer leakage inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C5, when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C4, and fed in the BPP pin via current limiting resistor R4.

4.3 InnoSwitch3-TN IC Secondary

The secondary-side of the InnoSwitch3-TN IC provides output voltage, output current sensing and gate drive for a MOSFET providing synchronous rectification. Secondary winding of the transformer is rectified by MOSFET Q1 and filtered by capacitors C8, C9, C11 and inductor L3 which forms a π-filter configuration to achieve very low output voltage ripple.

RC snubber network comprising C6 and R7 connected to MOSFET Q1 helps reduce high frequency ringing during switching transient, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gate of Q1 is turned on based on the winding voltage sensed via R6 and the FWD pin of the IC.

In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary-side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VOUT pin and charges the decoupling capacitor C7 and an internal regulator.

Output current is sensed by monitoring the voltage drop between the IS and GND pins. Once the constant current threshold is exceeded, the device will enter into Auto-Restart feature until load current is reduced below the constant current threshold.

This IC regulates the output voltage to 5 V through VOUT pin and internal feedback divider network.

5 PCB Layout

PCB - 1 Layer BOTTOM, FR4, 2oz Copper, 0.062" Thickness unless otherwise stated.

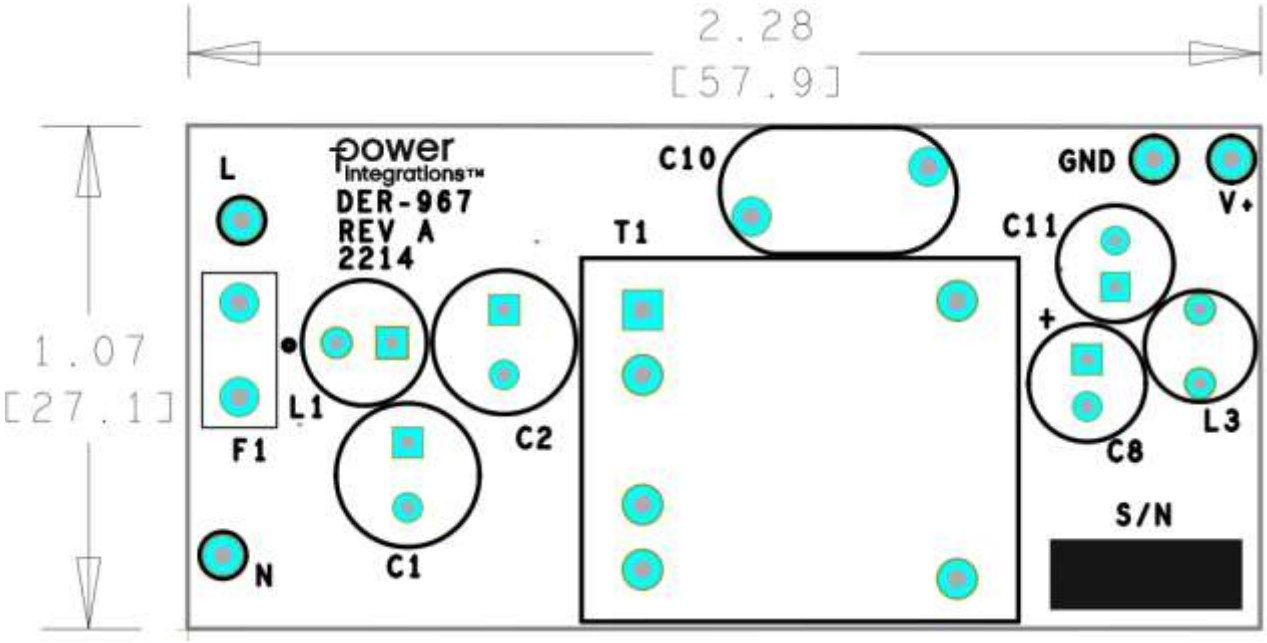


Figure 4 – Printed Circuit Layout, Top Side.

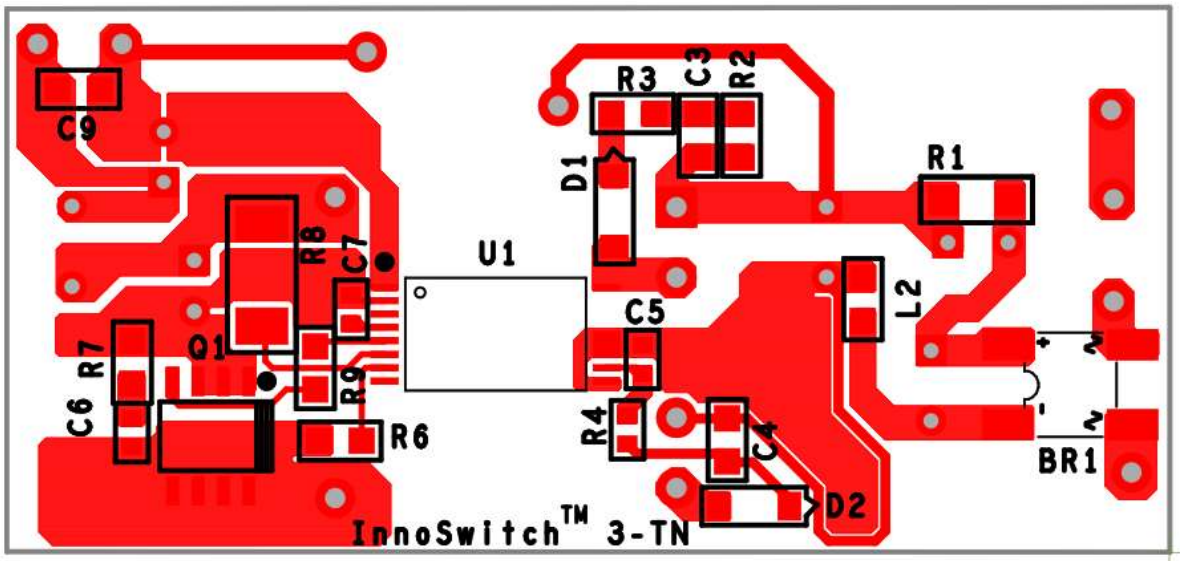


Figure 5 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

6.1 Electrical

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	BRIDGE RECT, 1PH, 1 kV, 2 A, 4SOPA, 4-SOPA, SOPA-4, SMD	ABS210-13	Diodes, Inc
2	2	C1 C2	ALUM, 5.6 µF, 20%, 400 V, RADIAL	UVC2G5R6MPD	Nichicon
3	1	C3	100 pF, ±10%, 500 V, Ceramic X7R, 0805	C0805X101KCRAC7800	Kemet
4	1	C4	22 µF, ±20%, 25 V, Ceramic X5R, 0805	GMC21X5R226M25NT	CAL-CHIP
5	1	C5	0.47 µF, 10%, 16 V, X7R, 0603	GRM188R71C474KA88D	Murata
6	1	C6	1000 pF, 100 V, Ceramic, NP0, 0603	C1608C0G2A102J	TDK
7	1	C7	2.2 µF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
8	1	C8	560 µF, 10 V, Aluminum - Polymer, Radial, Can 12 mΩ 2000 Hrs @ 105°C, (6.3 x 12)	A750EQ567M1AAAE012	KEMET
9	1	C9	CER, 1 µF, 10 V, X7R, 0805	CL21B105KPFNNNE	Samsung
10	1	C10	470 pF, ±10%, 250 VAC, Ceramic, Radial, Disc, X1, Y1	DE1B3RA471KN4AN01F	Murata
11	1	C11	100 µF, ±20%, 10 V, Aluminum Polymer, 2000 Hrs @ 105°C, (6.3 x 9)	A758EK107M1AAAE016	KEMET
12	1	D1	Diode, Standard, 1000 V, 1 A, SMT, Sub SMA	S1MLHRVG	TAIWAN SEMI
13	1	D2	200 V, 1 A, Standard Recovery, SOD-123FL	SM4003PL-TP	Micro Commercial
14	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
15	1	L1	330 µH, 0.300 A, 20%	RL-5480-2-330	Renco
16	1	L2	4.7 µH, 600 mA SMD INDUCTOR, MULTILAYER	MLZ2012N4R7LT000	TDK
17	1	L3	1.7 µH, Unshielded, Wirewound, Inductor, 3.52 A, 22.8 mΩ Max, Radial, 6.0 mm diam, 6.5 mm H, 4.0 mm LS	RCH664NP-1R7M	Sumida
18	1	Q1	N-Channel, 60 V, 13.5A (Ta), 3.1 W (Ta), SMT 8-SO, 8-SOP, PG-DSO-8, 8-SOIC (0.154", 3.90 mm Width)	AO4264E	Alpha & Omega Semi
19	1	R1	RES, 10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
20	1	R2	RES, 240 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ244V	Panasonic
21	1	R3	RES, 22 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ220V	Panasonic
22	1	R4	RES, 7.5 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF7501V	Panasonic
23	1	R6	RES, 47 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
24	1	R7	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
25	1	R8	0.0 Ω, Jumper, ¾ W, 2010, Moisture Resistant, Thick Film	RC2010JK-070RL	Yageo
26	1	R9	RES, 0 Ω, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole
27	1	T1	Bobbin, EF16, Horizontal, 9 pins (5x4)	YC-1635	Ying Chin
28	1	U1	InnoSwitch3-TN, MinSOP-16	INN3072M	Power Integrations

6.2 Mechanical

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	GND N	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
2	1	L	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
3	1	V+	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone

7 Transformer Specification

7.1 Electrical Diagram

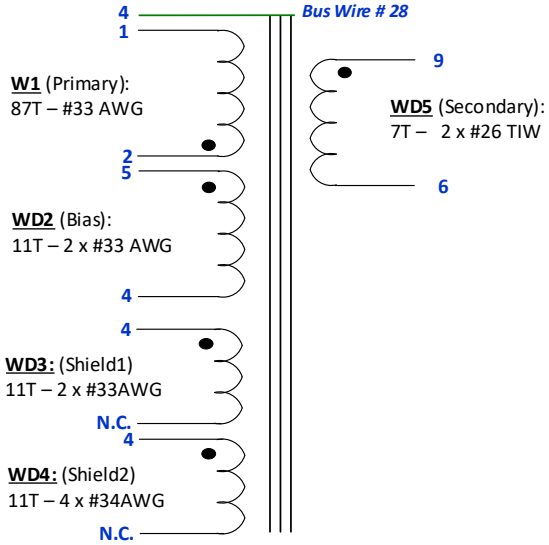


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Specification
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	967 µH ±5%
Resonant Frequency	Between pin 1 and 2, other windings open.	1400 kHz (Min.)
Primary Leakage Inductance	Between pin 1 and 2, with pins: 6 & 9 shorted.	36 µH (Max.)

7.3 Material List

Item	Description
[1]	Core: EF16 – N87, PI#: 99-00063-00; or Equivalent.
[2]	Bobbin: EF16-H-9pins (5/4); PI#: 25-01030-00. YingChin.
[3]	Magnet Wire: #33 AWG, Double Coated.
[4]	Magnet Wire: #26 AWG, Triple Insulated Wire.
[5]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[6]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 3.2 mm Width.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 9.5 mm Width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 4.5 mm Width
[9]	Tape: 3M Scotch, Polyweb, 3.2 mm Width or Equivalent.
[10]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

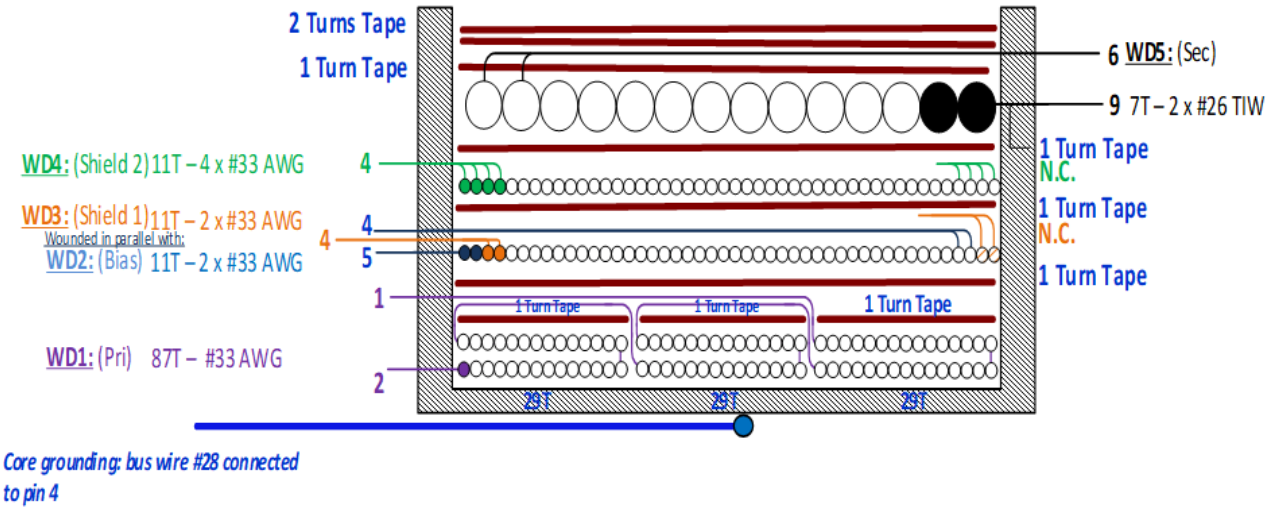
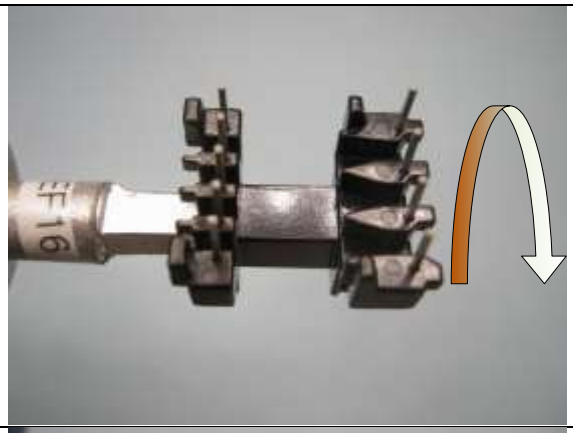


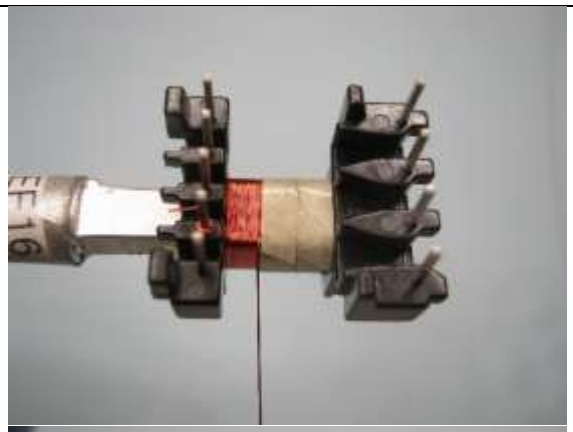
Figure 7 – Transformer Electrical Diagram.

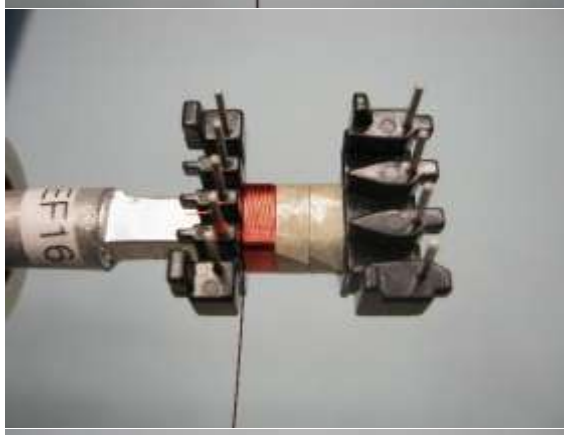
7.5 Winding Instructions

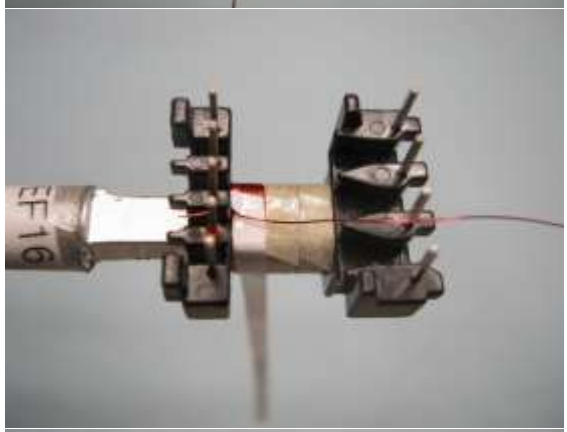
Winding Preparation	Position the bobbin Item [2] on the mandrel such that the pin-side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 Primary	Make 2 stacks of margin tape Item [9], 1 on the right and 1 at middle of bobbin width, so there is an empty chamber for the 1st winding of Primary winding (see pictures below). Start at pin 2, for 1st winding of Primary winding, wind 29 turns of wire Item [3] in 2 layers, from left to right then right to left in the empty chamber. At the last turn, place 1 layer of tape Item [6] to hold this winding. Remove middle stack of margin tape, continue winding another 29 turns for 2nd winding of Primary winding same way as previous winding in the middle chamber, also place 1 layer of tape Item [6] to hold this winding. Remove right stack of margin tape, repeat for another 29 turns for 3rd winding of Primary winding. At the last turn bring the wire back to left to terminate at pin 1 and 1 layer of tape Item [6] for this winding.
Insulation	1 layer of tape Item [7].
WD2 & WD3 Bias & Shield1	Start at pin 5, use 2 wires Item [3] for Bias winding and start at pin 4 also use 2 wires Item [3] for Shield1 winding, wind all 4 wires 11 turns. At the last turn, bring 2 wires of Bias winding to the left to terminate at pin 4 and cut short 2 wires of Shield1 winding as No-Connect (NC).
Insulation	1 layer of tape Item [7].
WD4 Shield2	Start at pin 4, wind 11 quad-filar turns of wires Item [3]. At the last turn cut short all wires as No-Connect (NC).
Insulation	1 layer of tape Item [7].
WD5 Secondary	Start pin 9, wind 7 bi-filar turns of wire Item [4] from right to left. At the last turn, bring 2 wires back to the right and terminate at pin 6.
Insulation	2 layers of tape Item [7].
Finish	Gap core halves to get inductance 967 µH. Use bus wire Item [5] solder to pin 4 and lean along the core halves then secure with tape Item [8]. Varnish with Item [10].

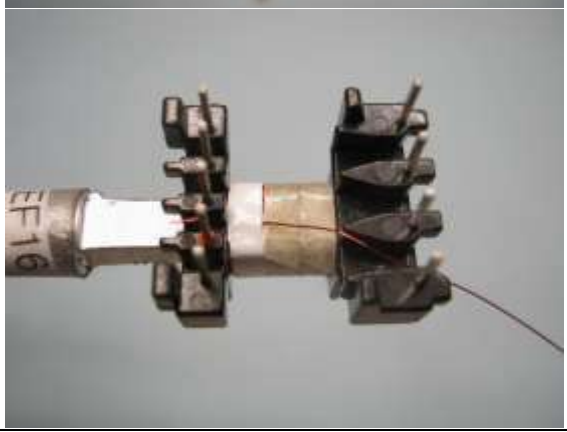
7.6 Winding Illustrations

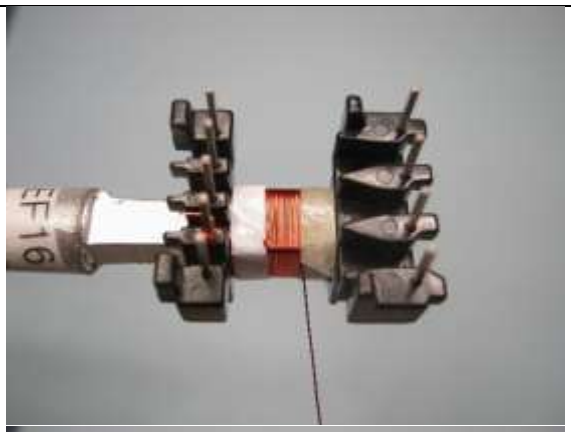
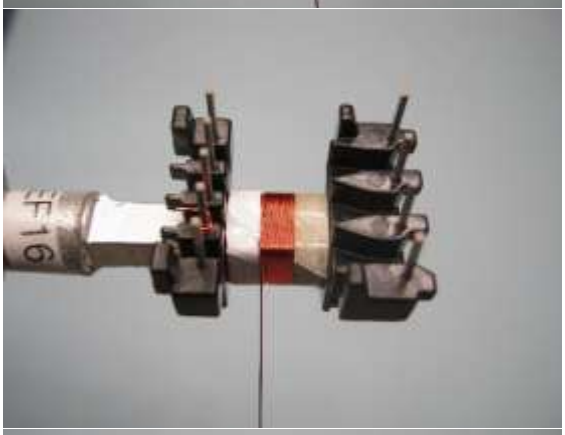
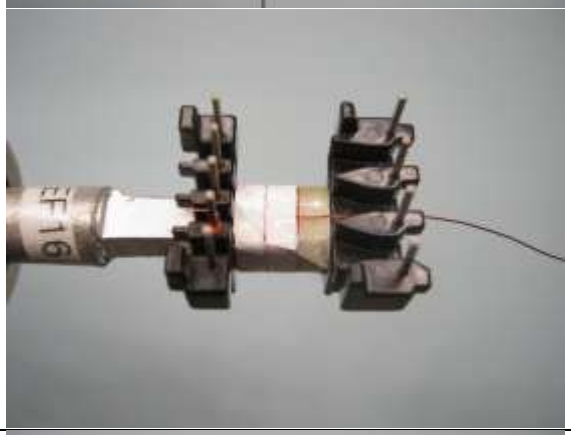
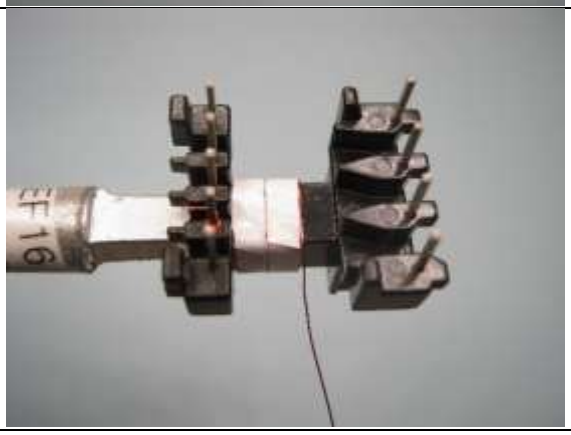
Winding Preparation		Position the bobbin Item [2] on the mandrel such that the pin-side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **Primary – 1st winding**	 	Make 2 stacks of margin tape Item [9], 1 on the right and 1 at middle of bobbin width, so there is an empty chamber for the 1st winding of Primary winding (see pictures beside). Start at pin 2, for 1st winding of Primary winding, wind 29 turns of wire Item [3] in 2 layers, from left to right then right to left in the empty chamber. At the last turn, place 1 layer of tape Item [6] to hold this winding.

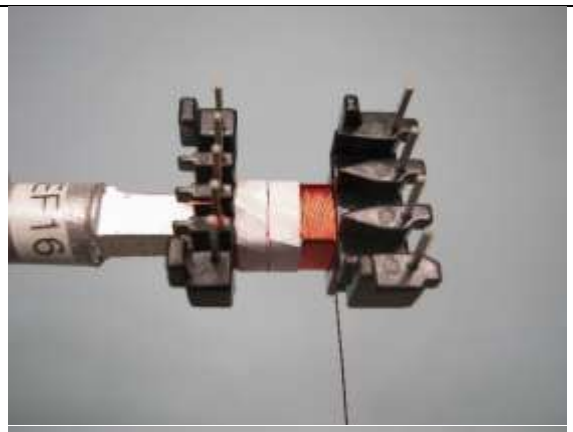

EF16

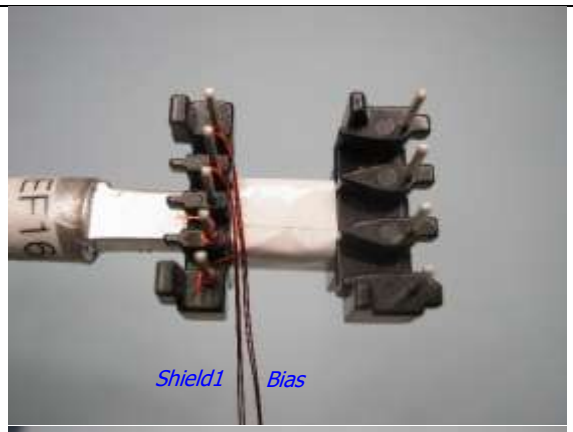
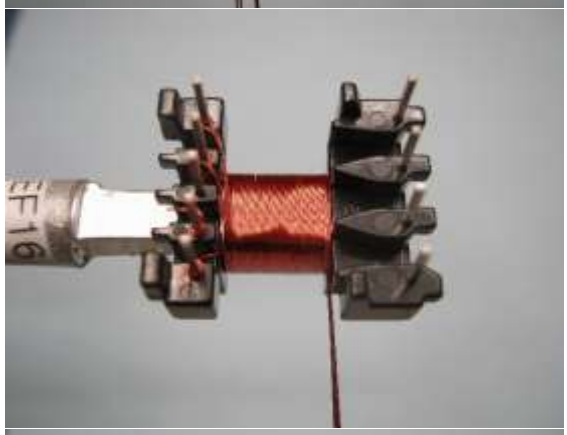
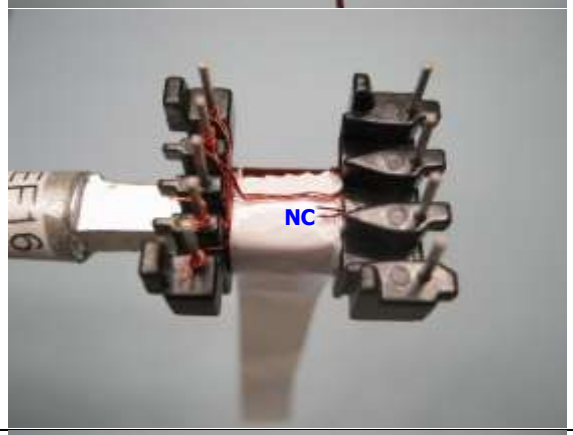

EF16

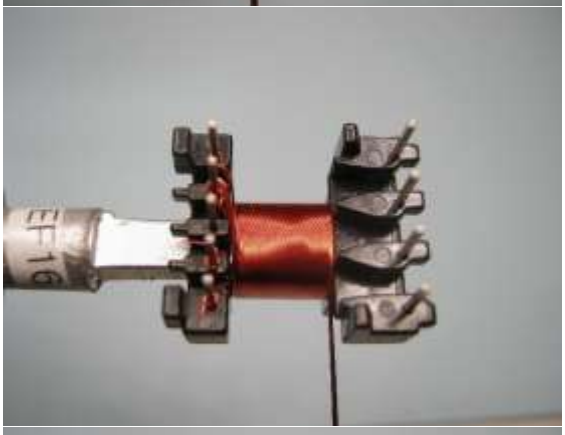
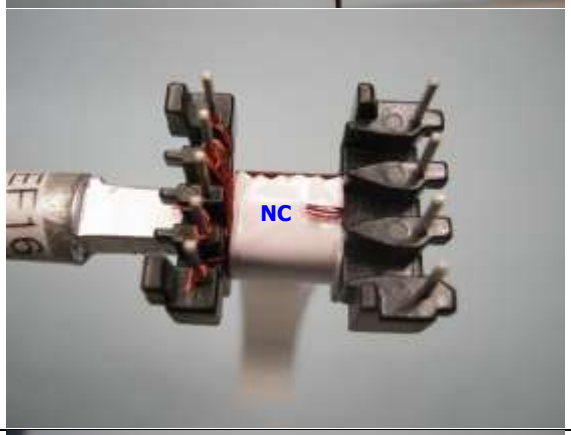

EF16

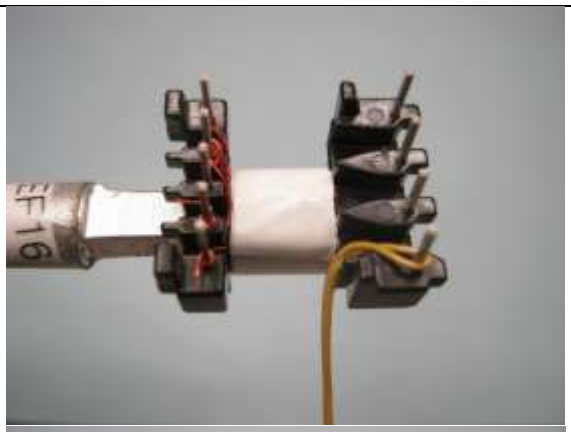

EF16

WD1 **Primary – 2nd winding**	  	Remove middle stack of margin tape, continue winding another 29 turns for 2nd winding of Primary winding same way as previous winding in the middle chamber, also place 1 layer of tape Item [6] to hold this winding.
WD1 **Primary – 3rd winding**		Remove right stack of margin tape, repeat for another 29 turns for 3rd winding of Primary winding. At the last turn bring the wire back to left to terminate at pin 1 and 1 layer of tape Item [6] for this winding.

	  	
Insulation		1 layer of tape Item [7].

WD2 & WD3 **Bias & Shield1**	  	Start at pin 5, use 2 wires Item [3] for Bias winding and start at pin 4 also use 2 wires Item [3] for Shield1 winding, wind all 4 wires 11 turns. At the last turn, bring 2 wires of Bias winding to the left to terminate at pin 4 and cut short 2 wires of Shield1 winding as No-Connect (NC).
Insulation		1 layer of tape Item [7].

WD4 **Shield2**	  	Start at pin 4, wind 11 quad-filar turns of wires Item [3]. At the last turn cut short all wires as No-Connect (NC).
Insulation		1 layer of tape Item [7].

WD5 **Secondary**	  	Start pin 9, wind 7 bi-filar turns of wire Item [4] from right to left. At the last turn, bring 2 wires back to the right and terminate at pin 6.
Insulation		2 layers of tape Item [7].

Finish	 	Gap core halves to get inductance 967 uH. Use bus wire Item [5] solder to pin 4 and lean along the core halves then secure with tape Item [7]. Varnish with Item [10].

8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-TN_Flyback_030222; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 TN Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VIN_MIN	85		85	V	Minimum AC input voltage
4	VIN_MAX	265		265	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	11.2		11.2	uF	Input capacitor
8	VOUT			5.00	V	Output voltage at the board
9	CDC	0		0	mV	Cable drop compensation desired at full load
10	IOUT	1.000		1.000	A	Output current
11	POUT			5.00	W	Output power
12	EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE			OPEN FRAME		Power supply enclosure
18	**PRIMARY CONTROLLER SELECTION**					
19	DEVICE_GENERIC	INN3072		INN3072		Generic device code
20	DEVICE_CODE			INN3072M		Actual device code
21	POUT_MAX			10.0	W	Power capability of the device based on thermal performance
22	ICC_MIN			1.50	A	Minimum constant current regulation threshold of the device
23	ICC_TYP			1.70	A	Typical constant current regulation threshold of the device
24	ICC_MAX			1.90	A	Maximum constant current regulation threshold of the device
25	RDSON_100DEG			11.24	Ω	Primary switch on time drain resistance at 100 degC
26	ILIMIT_MIN			0.510	A	Minimum current limit of the primary switch
27	ILIMIT_TYP			0.550	A	Typical current limit of the primary switch
28	ILIMIT_MAX			0.590	A	Maximum current limit of the primary switch
29	VDRAIN_BREAKDOWN			725	V	Device breakdown voltage
30	VDRAIN_ON_PRSW			0.70	V	Primary switch on time drain voltage
31	VDRAIN_OFF_PRSW			506.4	V	Peak drain voltage on the primary switch during turn-off
35	**WORST CASE ELECTRICAL PARAMETERS**					
36	FSWITCHING_MAX	53000		53000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
37	VOR	63.0		63.0	V	Secondary voltage reflected to the primary when the primary switch turns off
38	VMIN			86.09	V	Valley of the minimum input AC voltage at full load
39	KP			1.99		Measure of continuous/discontinuous mode of operation
40	MODE_OPERATION			DCM		Mode of operation
41	DUTYCYCLE			0.270		Primary switch duty cycle
42	TIME_ON			6.04	us	Primary switch on-time
43	TIME_OFF			13.84	us	Primary switch off-time
44	LPRIMARY_MIN			919.0	uH	Minimum primary inductance
45	LPRIMARY_TYP			967.4	uH	Typical primary inductance
46	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
47	LPRIMARY_MAX			1015.7	uH	Maximum primary inductance

49	**PRIMARY CURRENT**					
50	IPEAK_PRIMARY			0.516	A	Primary switch peak current
51	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
52	IAVG_PRIMARY			0.062	A	Primary switch average current
53	IRIPPLE_PRIMARY			0.516	A	Primary switch ripple current
54	IRMS_PRIMARY			0.146	A	Primary switch RMS current
56	**SECONDARY CURRENT**					
57	IPEAK_SECONDARY			6.418	A	Secondary winding peak current
58	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
59	IRMS_SECONDARY			2.117	A	Secondary winding RMS current
63	**TRANSFORMER CONSTRUCTION PARAMETERS**					
64	**CORE SELECTION**					
65	CORE	CUSTOM		CUSTOM		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
66	CORE CODE	N27EF16		N27EF16		Core code
67	AE	20.10		20.10	mm^2	Core cross sectional area
68	LE	37.60		37.60	mm	Core magnetic path length
69	AL	950		950	nH/turns^2	Ungapped core effective inductance
70	VE	756.0		756.0	mm^3	Core volume
71	BOBBIN	EF16-Horizontal		EF16-Horizontal		Bobbin
72	AW	30.40		30.40	mm^2	Window area of the bobbin
73	BW	9.50		9.50	mm	Bobbin width
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
76	**PRIMARY WINDING**					
77	NPRIMARY			87		Primary turns
78	BPEAK			3508	Gauss	Peak flux density
79	BMAX			2948	Gauss	Maximum flux density
80	BAC			1474	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			128	nH/turns^2	Typical gapped core effective inductance
82	LG			0.171	mm	Core gap length
84	**SECONDARY WINDING**					
85	NSECONDARY	7		7		Secondary turns
87	**BIAS WINDING**					
88	NBIAS			11		Bias Turns
92	**PRIMARY COMPONENTS SELECTION**					
94	VBIAS	7.0	Info	7.0	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 10V
95	VF_BIAS			0.70	V	Bias winding diode forward drop
96	VREVERSE_BIASDIODE			54.21	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
97	CBIAS			22	uF	Bias winding rectification capacitor
98	CBPP			4.70	uF	BPP pin capacitor
102	**SECONDARY COMPONENTS SELECTION**					
103	RFWD			47	Ω	Forward pin resistor
104	CBPS			2.2	uF	BPS pin capacitor
108	**MULTIPLE OUTPUT PARAMETERS**					
109	**OUTPUT 1**					
110	VOUT1			5.00	V	Output 1 voltage
111	IOUT1			1.00	A	Output 1 current
112	POUT1			5.00	W	Output 1 power
113	IRMS_SECONDARY1			2.117	A	Root mean squared value of the secondary current for output 1
114	IRIPPLE_CAP_OUTPUT1			1.866	A	Current ripple on the secondary waveform for output 1
115	NSECONDARY1			7		Number of turns for output 1
116	VREVERSE_RECTIFIER1			35.04	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1

117	SRFET1	AO4264E	Info	AO4264E		The voltage stress (including the parasitic ring) on the secondary MOSFET selected may exceed the device BVDSS: pick a MOSFET with a higher BVDSS
118	VF_SRFET1			0.012	V	SRFET on-time drain voltage for output 1
119	VBREAKDOWN_SRFET1			60	V	SRFET breakdown voltage for output 1
120	RDSON_SRFET1			13.5	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1

9 Performance Data

9.1 Average Efficiency

Requirement	
Average	**73.6% (DOE6), 73.7% (CoC II)**
10%	**64.5%**

9.1.1 115 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	115	96.54	5.75	4.96	1.00	4.95	86.07	
75	115	76.86	4.30	4.97	0.75	3.72	86.47	
50	115	55.77	2.86	4.98	0.50	2.48	86.69	
25	115	32.91	1.43	4.98	0.25	1.23	86.15	**86.35**
10	115	16.54	0.57	4.98	0.01	0.48	**83.88**	

9.1.2 230 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	230	63.01	5.76	4.96	1.00	4.95	86.05	
75	230	50.95	4.34	4.97	0.75	3.73	85.84	
50	230	37.87	2.90	4.98	0.50	2.48	85.26	
25	230	22.74	1.46	4.98	0.25	1.23	84.21	**85.34**
10	230	11.48	0.58	4.98	0.01	0.48	**83.30**	

9.2 Full Load Efficiency vs. Line

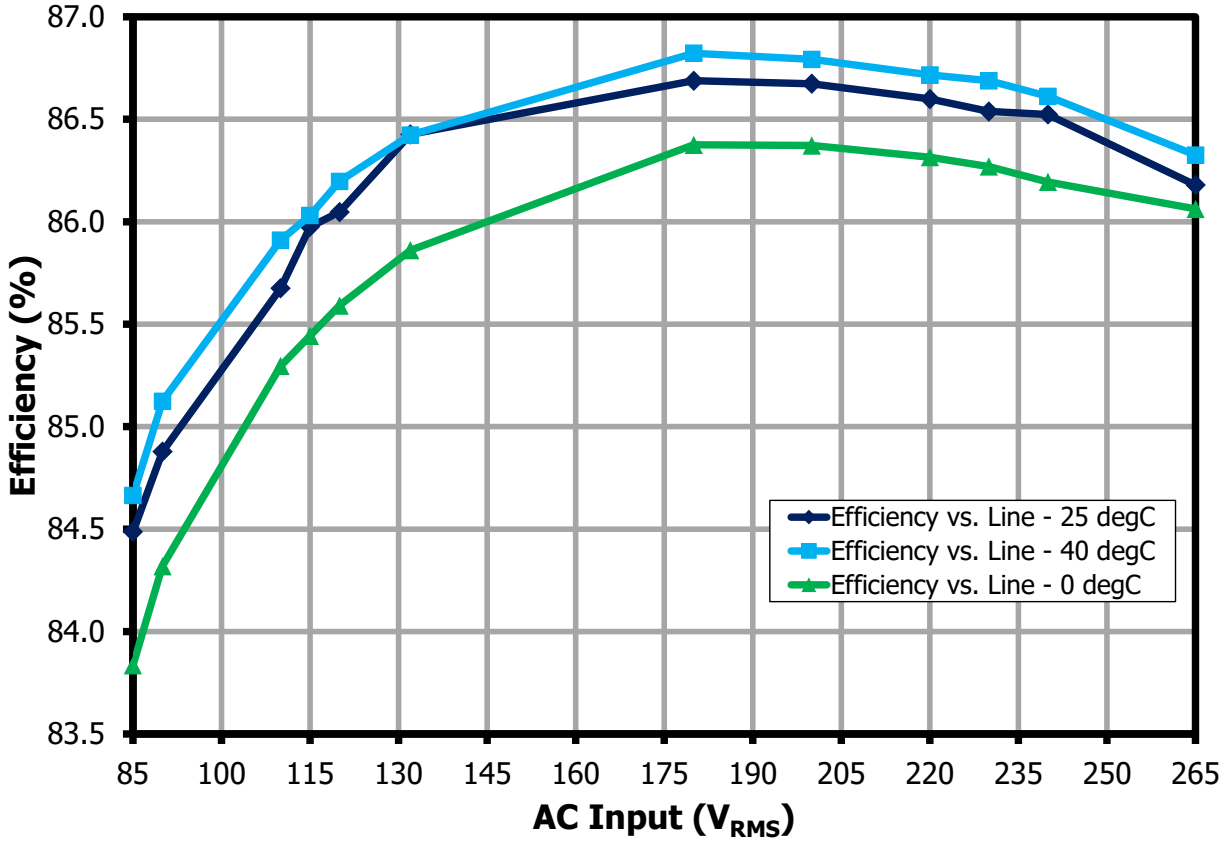


Figure 8 – Full load Efficiency vs. Line Voltage.

9.3 Efficiency vs. Load

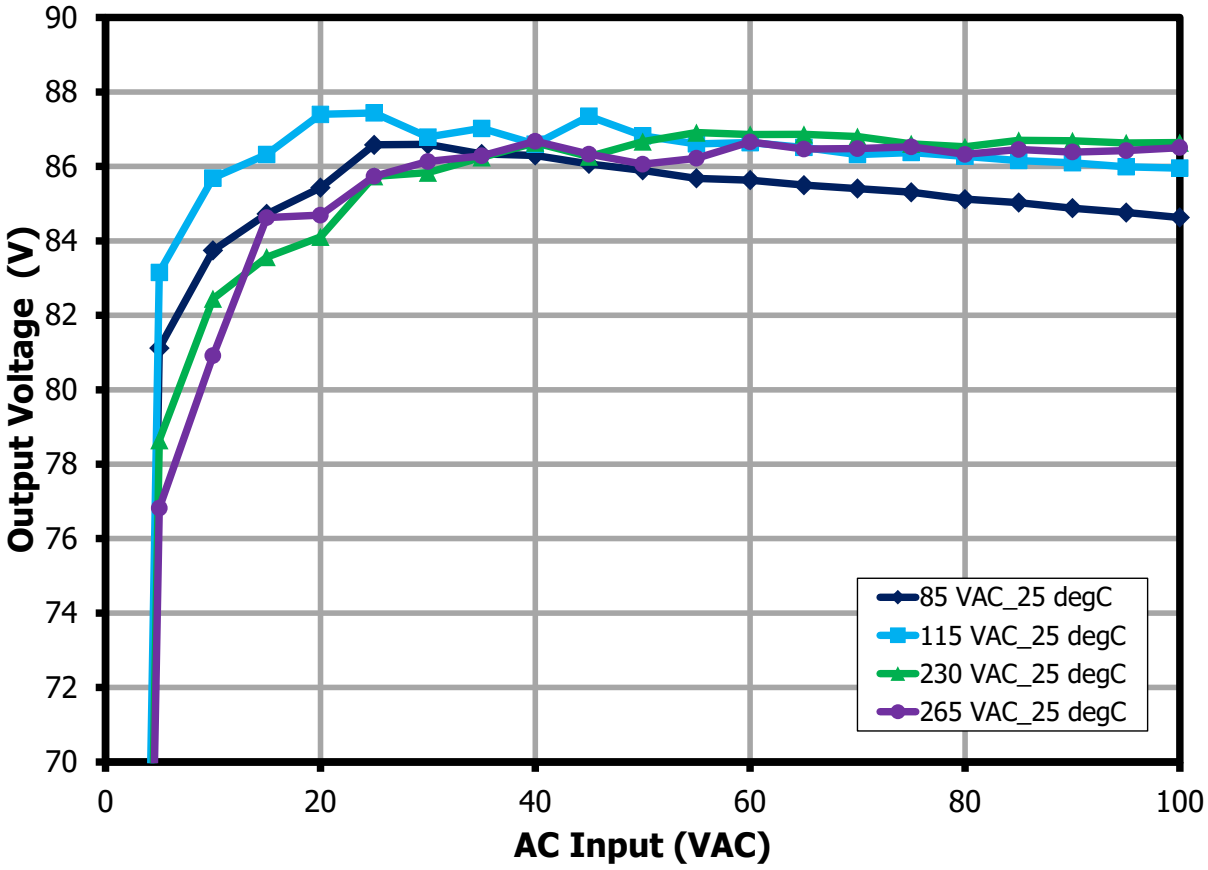


Figure 9 – Efficiency vs. Load, Room Ambient – 25 ºC Temperature.

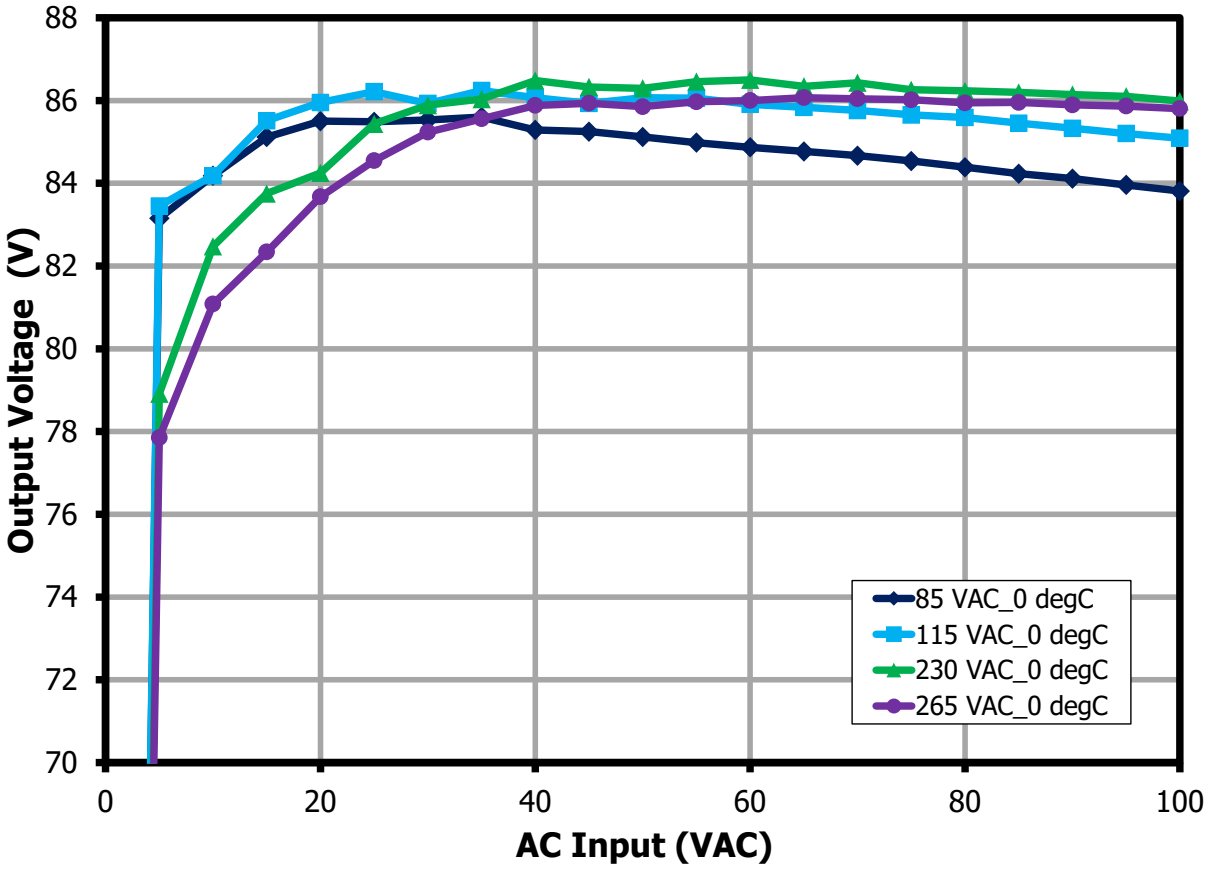


Figure 10 – Efficiency vs. Load, Cold Ambient – 0 ºC Temperature.

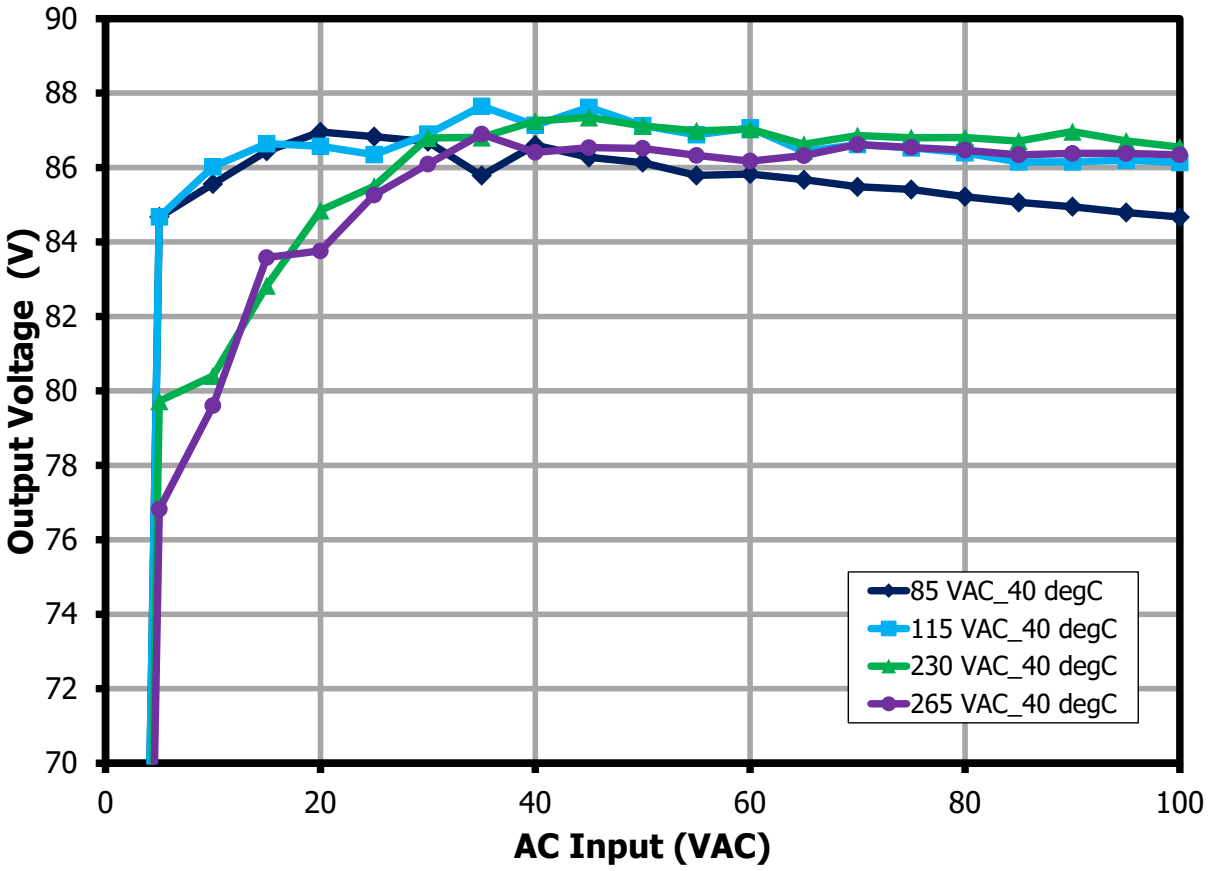


Figure 11 – Efficiency vs. Load, Hot Ambient – 40 ºC Temperature.

9.4 No-Load Input Power

Note: Soak for 30 minutes and integrate for 1 hour.

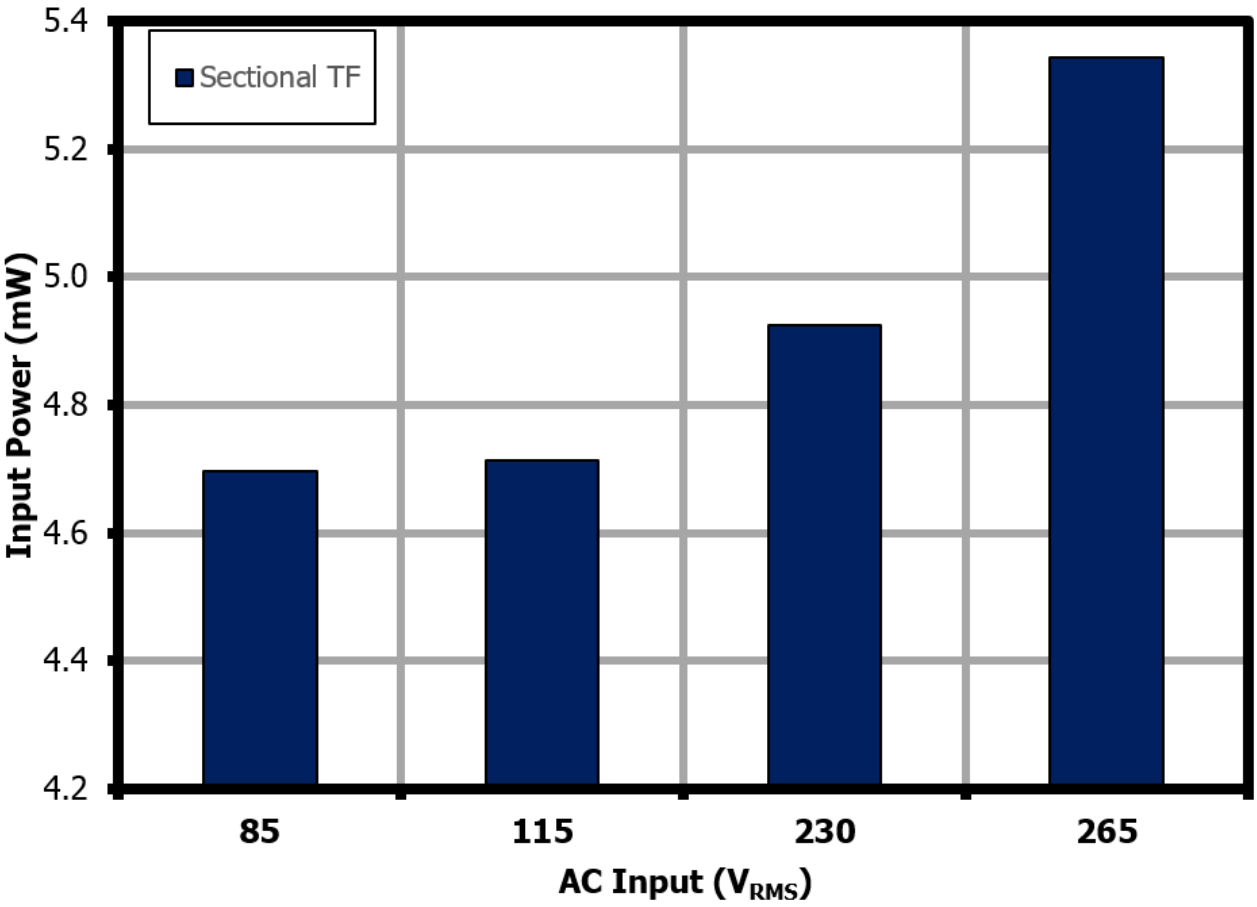


Figure 12 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

9.5 Standby Power (5 V / 30 mA Load)

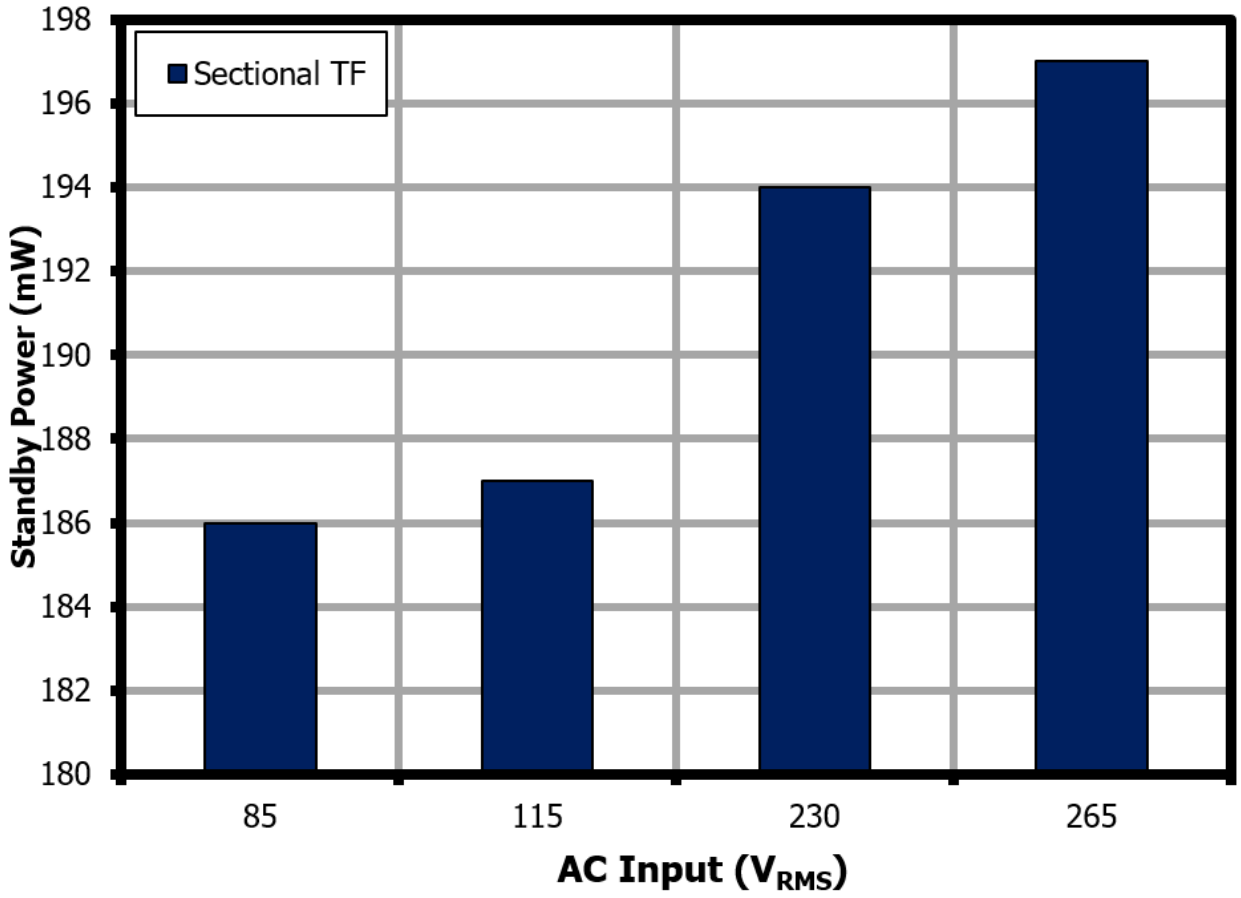


Figure 13 – Standby Power (5 V / 30 mA Load).

9.6 Line and Load Regulation

9.6.1 Line Regulation (Full Load)

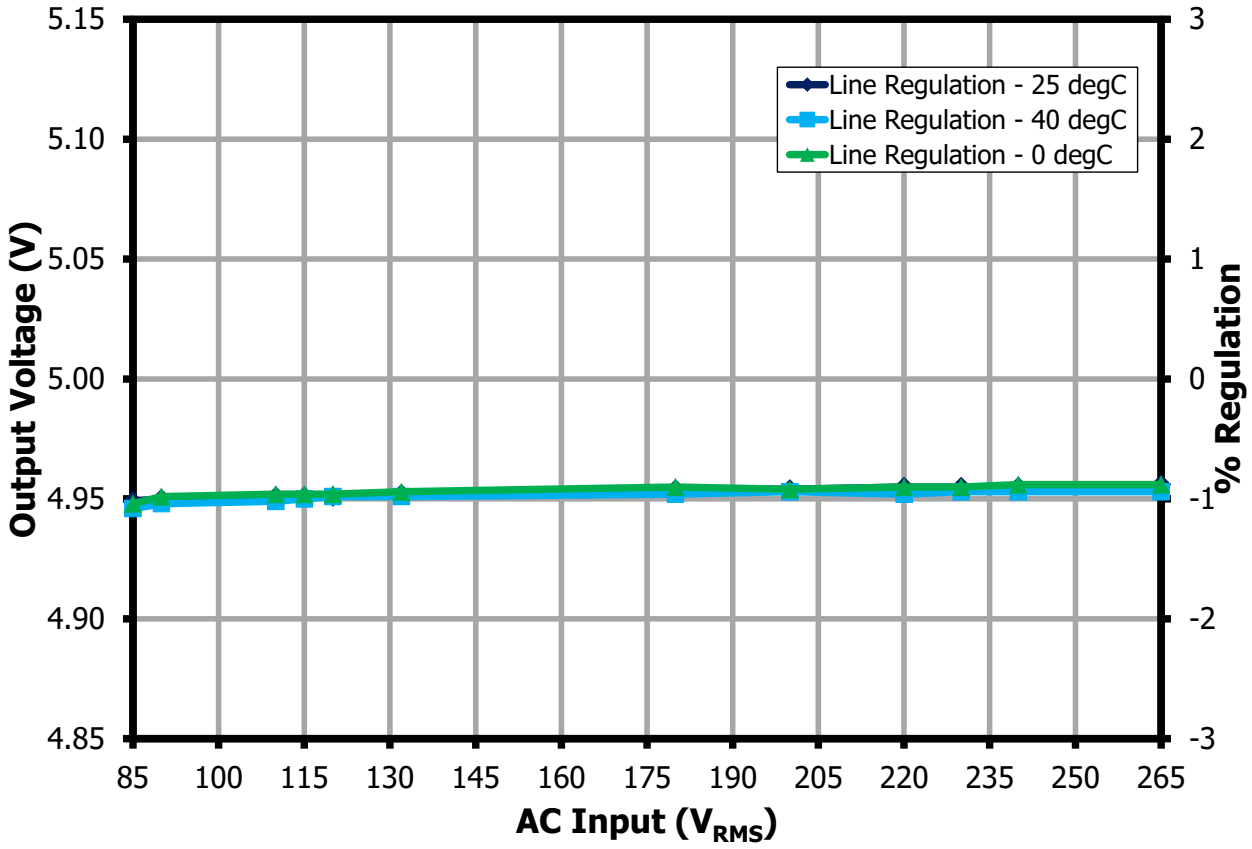


Figure 14 – 5 V Output Voltage vs. Input Line Voltage.

9.6.2 Load Regulation

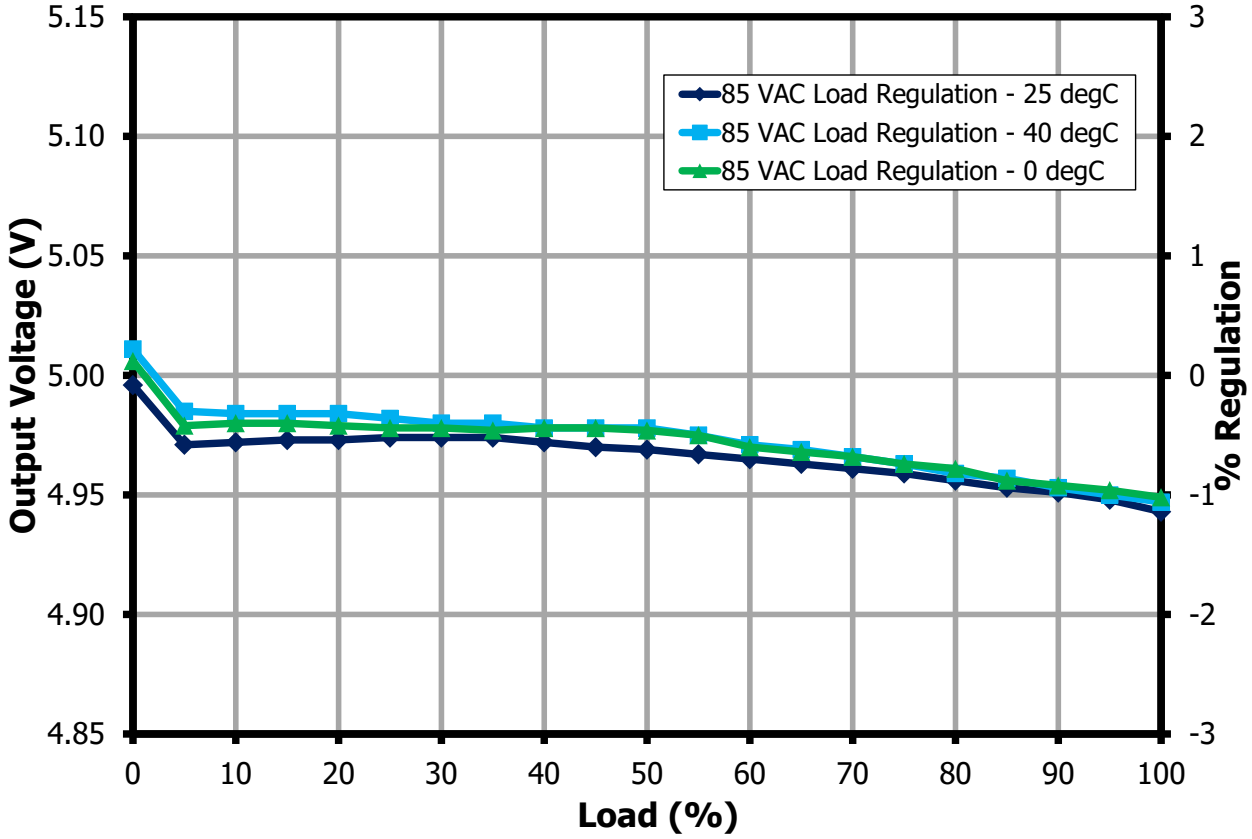


Figure 15 – 5 V Output Voltage vs. Load at 85 VAC.

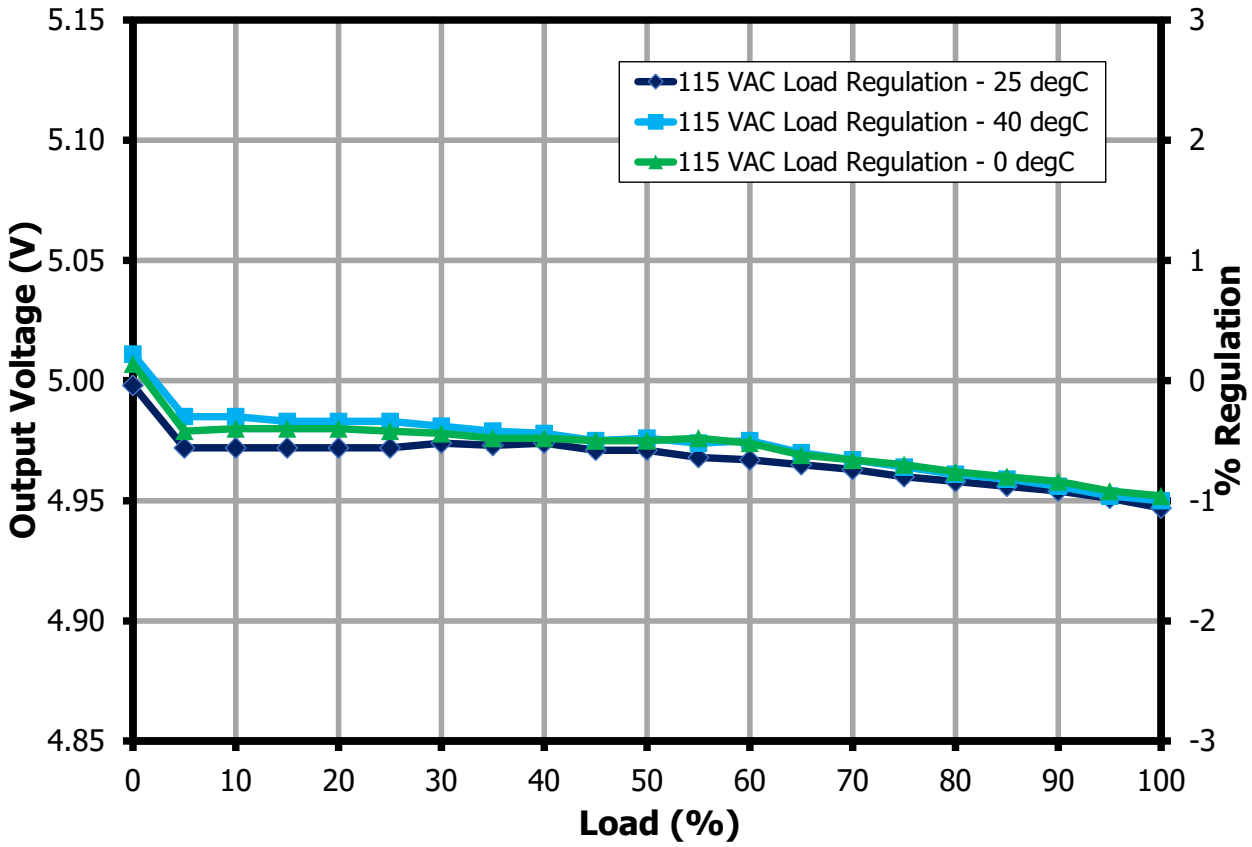


Figure 16 – 5 V Output Voltage vs. Load at 115 VAC.

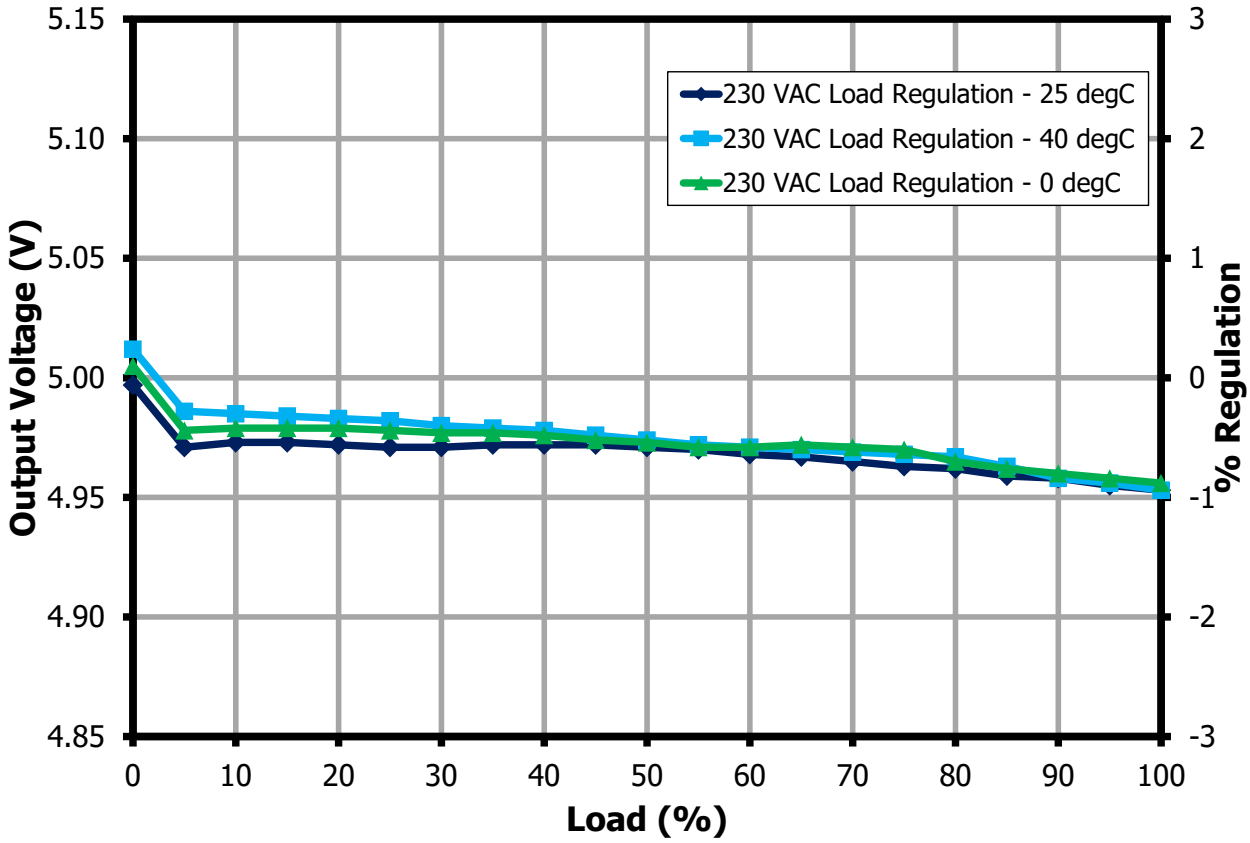


Figure 17 – 5 V Output Voltage vs. Load at 230 VAC.

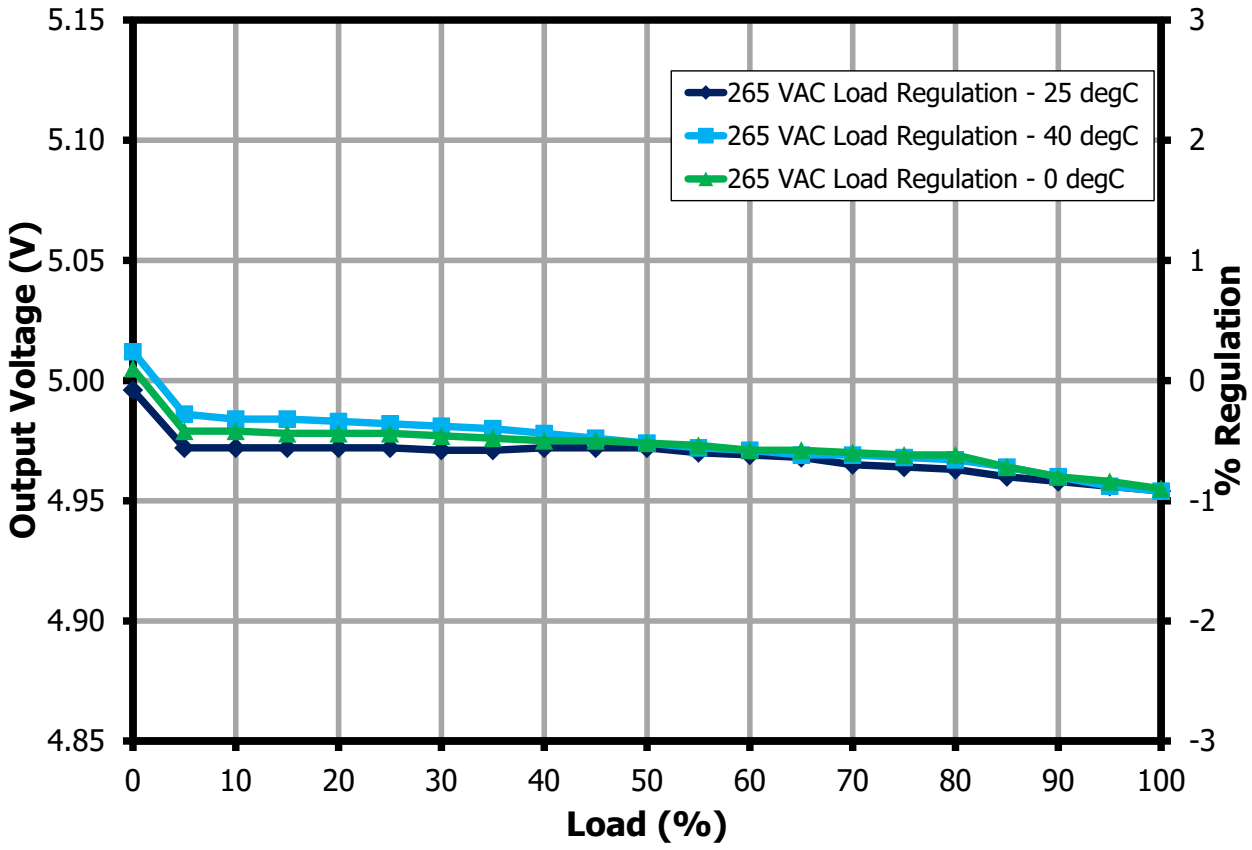


Figure 18 – 5 V Output Voltage vs. Load at 265 VAC.

10 Thermal Performance

10.1 85 VAC

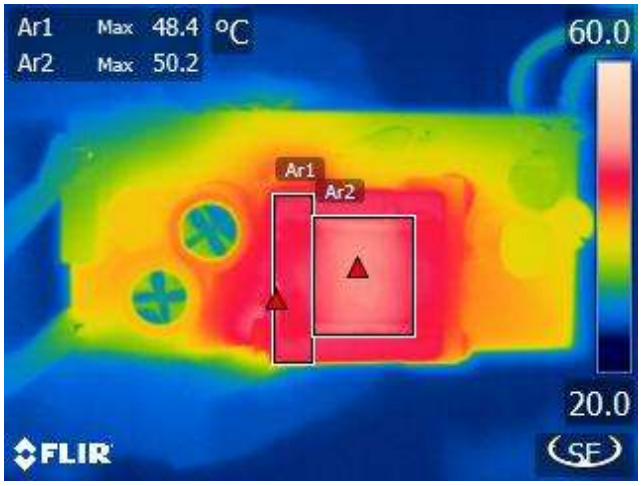


Figure 19 – Transformer Side. 85 VAC, Full Load.

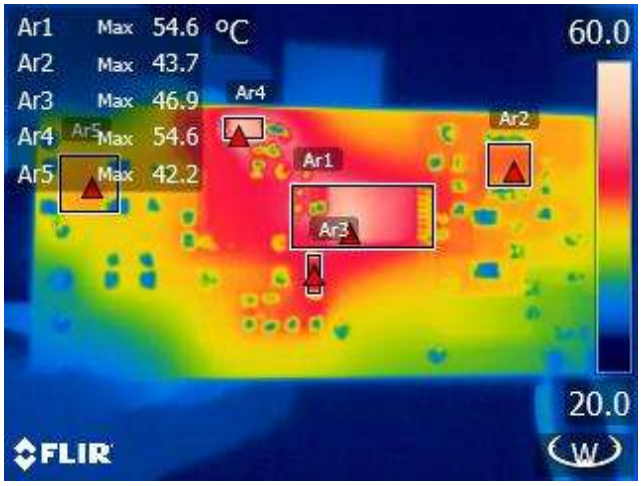


Figure 20 – InnoSwitch3-TN Side. 85 VAC, Full Load.

	Reference	°C
Ambient		25.4
Transformer Core	T1-Core (Ar1)	50.2
Transformer Winding	T1-Winding (Ar2)	48.4

	Reference	°C
Ambient		25.4
InnoSwitch3-TN	U1 (Ar1)	54.6
SR FET – AO4264E	Q1 (Ar2)	43.7
Primary Snubber Diode	D1 (Ar3)	46.9
Bias Diode	D2 (Ar4)	54.6
Bridge Rectifier	BR1 (Ar5)	42.2

10.2 265 VAC

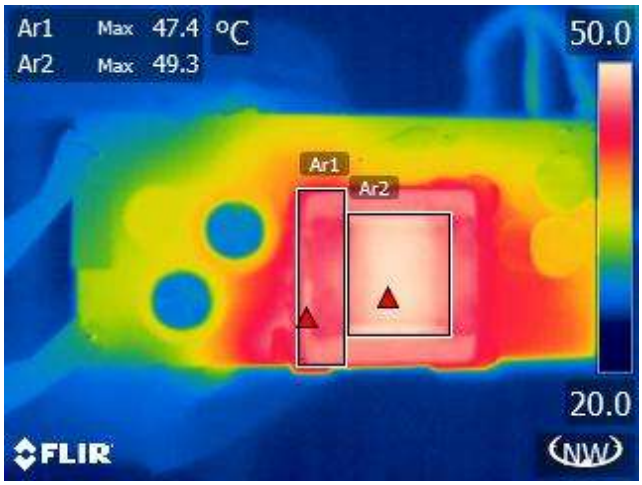


Figure 21 – Transformer Side. 265 VAC, Full Load.

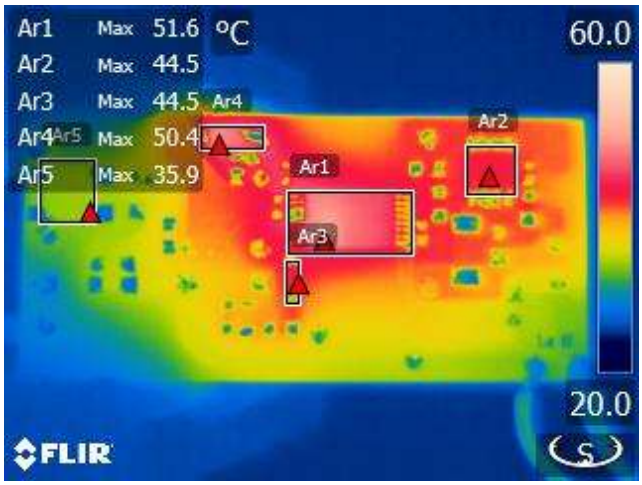


Figure 22 – InnoSwitch3-TN Side. 265 VAC, Full Load.

	Reference	°C
Ambient		25.9
Transformer Core	T1-Core (Ar1)	47.4
Transformer Winding	T1-Winding (Ar2)	49.3

	Reference	°C
Ambient		25.9
InnoSwitch3-TN	U1 (Ar1)	51.6
SR FET – AO4264E	Q1 (Ar2)	44.5
Primary Snubber Diode	D1 (Ar3)	44.5
Bias Diode	D2 (Ar4)	50.4
Bridge Rectifier	BR1 (Ar5)	35.9

11 Waveforms

11.1 Load Transient Response

11.1.1 5 V Load Transient – Full-Load to No-Load

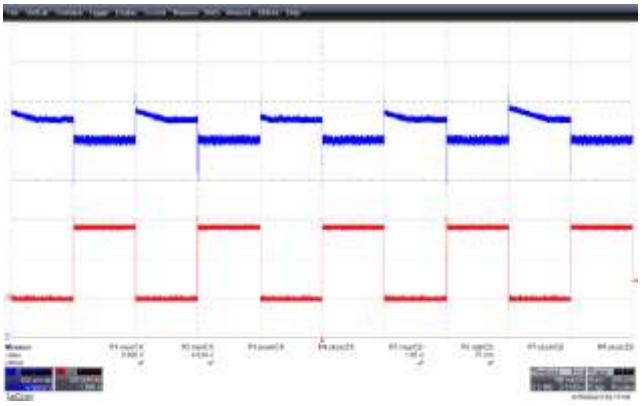


Figure 23 – 0 A – 1 A, 5 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 4.83 V.; 5 V_{MAX}: 5.08 V.
Upper: 5 V_{OUT}, 100 mV / div.
Lower: 5 I_{OUT}, 500 mA / div.

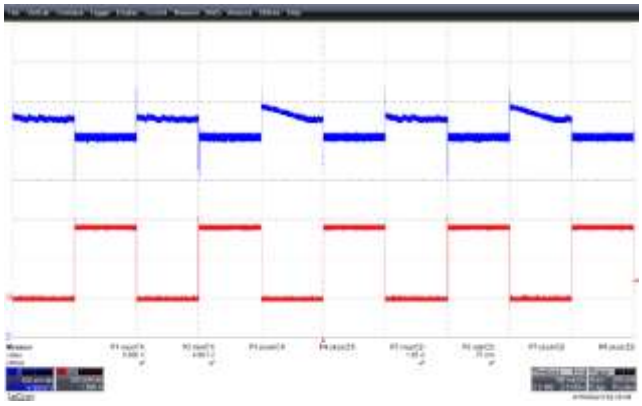


Figure 24 – 0 A – 1 A, 5 V Load Step Transient Response, 265 VAC.
5 V_{MIN}: 4.86 V.; 5 V_{MAX}: 5.08 V.
Upper: 5 V_{OUT}, 100 mV / div.
Lower: 5 I_{OUT}, 500 mA / div.

11.2 Switching Waveforms

11.2.1 InnoSwitch3-TN Waveforms

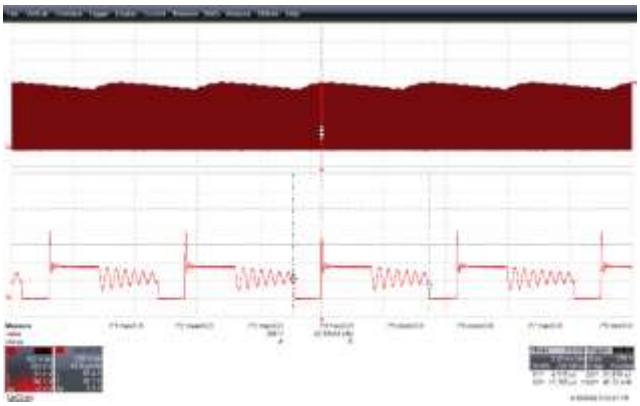


Figure 25 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
CH1: V_{DRAIN}, 100 V / div, 5 ms / div.
Zoom: 10 µs / div.

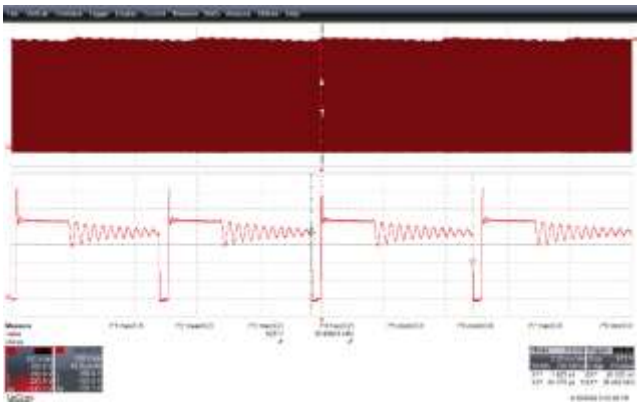


Figure 26 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (629 V_{MAX}).
CH1: V_{DRAIN}, 100 V / div, 5 ms / div.
Zoom: 10 µs / div.

11.2.2 InnoSwitch3-TN Drain Voltage and Current Waveforms During Start-Up

Figure 27 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
CH1: V_{DRAIN}, 100 V / div, 5 ms / div.

Figure 28 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (625 V_{MAX}).
CH1: V_{DRAIN}, 100 V / div, 5 ms / div.

11.2.3 InnoSwitch3-TN Drain Voltage and Current Waveforms During Output Short-Circuit

Note: 5 V output is shorted

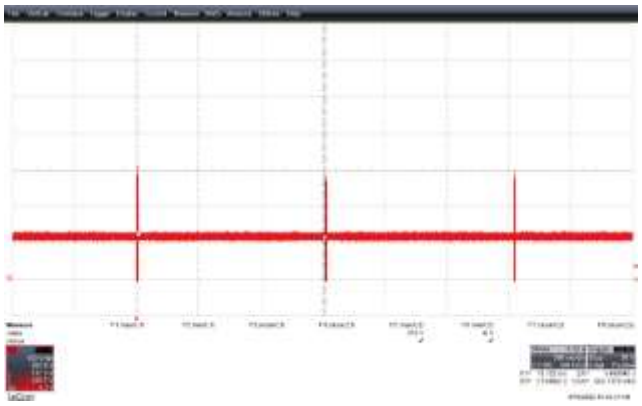


Figure 29 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
CH1: V_{DRAIN}, 100 V / div., 500 ms / div.

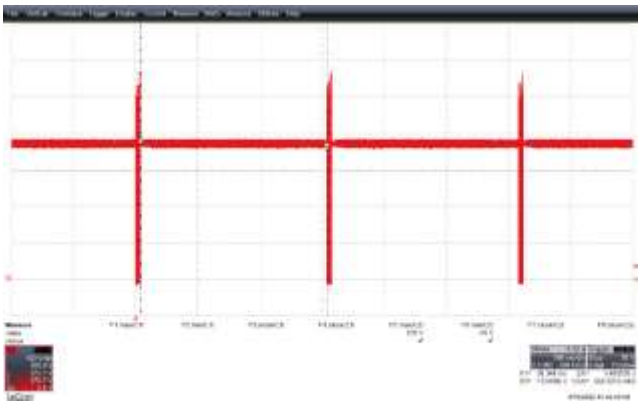


Figure 30 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (579 V_{MAX}).
CH1: V_{DRAIN}, 100 V / div., 500 ms / div.

11.2.4 SR FET Waveforms

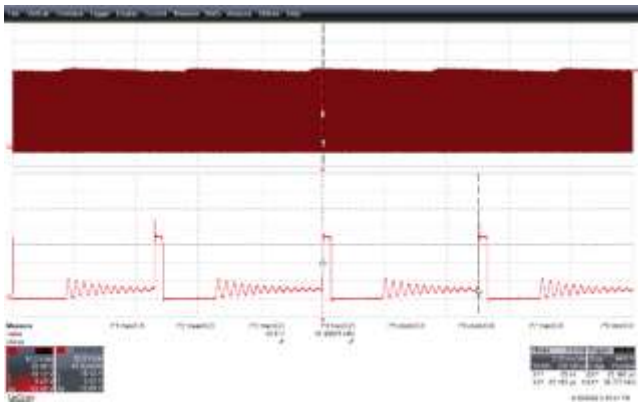


Figure 31 – SR FET Voltage Waveforms.
265 VAC Input, Full Load. (45.6 V_{MAX})
CH1: V_{DRAIN}, 10 V / div, 5 ms / div.
Zoom: 10 μs / div.

Figure 32 – SR FET Voltage Waveforms During Start-Up.
265 VAC Input, Full Load. (45.6V V_{MAX})
CH1: V_{DRAIN}, 10 V / div, 5 ms / div.

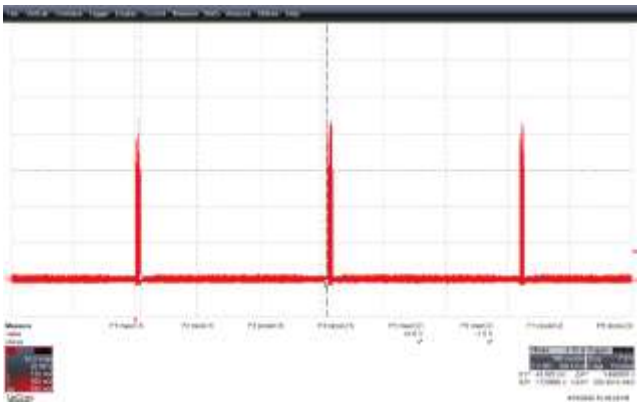


Figure 33 – 5 V SR FET Voltage Waveforms During Output Short-Circuit.
265 VAC Input, Full Load. (44.6V V_{MAX})
CH1: V_{DRAIN}, 10 V / div, 500 ms / div.

11.2.5 Output Voltage and Current Waveforms During Start-Up

11.2.5.1 Full Load

Figure 34 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: 5 V_{OUT}, 2 V / div.
Lower: 5 I_{OUT}, 500 mA / div.
2 ms / div.

Figure 35 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V_{OUT}, 2 V / div.
Lower: 5 I_{OUT}, 500 mA / div.
2 ms / div.

11.3 Output Ripple Measurements

11.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 10 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

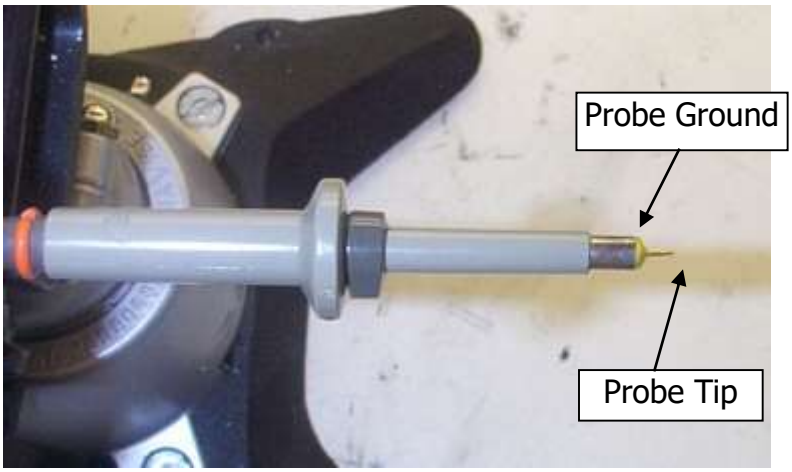


Figure 36 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

Figure 37 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

11.3.2 Ripple Voltage Waveforms

11.3.2.1 0% Load

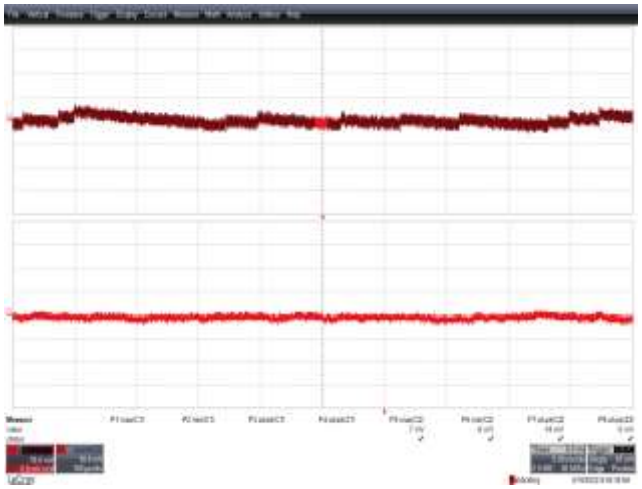


Figure 38 – Output Ripple Voltage Waveforms.
85 VAC Input. 5 V_{PK-PK}: 14 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

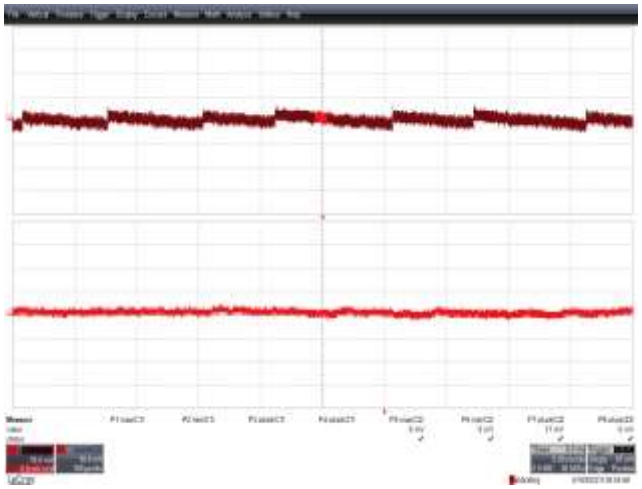


Figure 39 – Output Ripple Voltage Waveforms.
265 VAC Input. 5 V_{PK-PK}: 11 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

11.3.2.2 25% Load

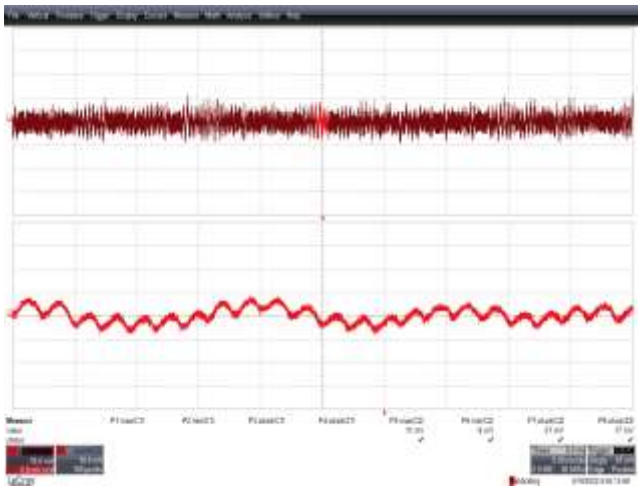


Figure 40 – Output Ripple Voltage Waveforms.
85 VAC Input. 5 V_{PK-PK}: 21 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

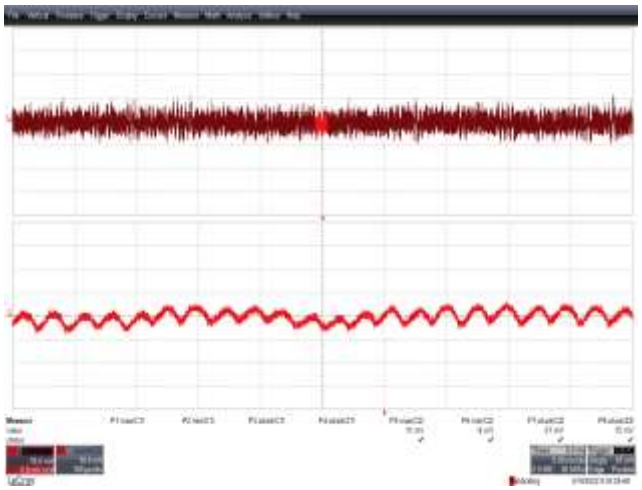


Figure 41 – Output Ripple Voltage Waveforms.
265 VAC Input. 5 V_{PK-PK}: 21 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

11.3.2.3 50% Load

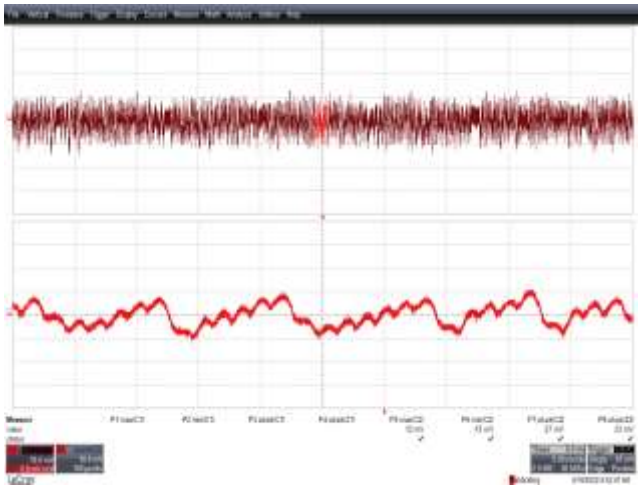


Figure 42 – Output Ripple Voltage Waveforms.
85 VAC Input. 5 V_{PK-PK}: 27 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

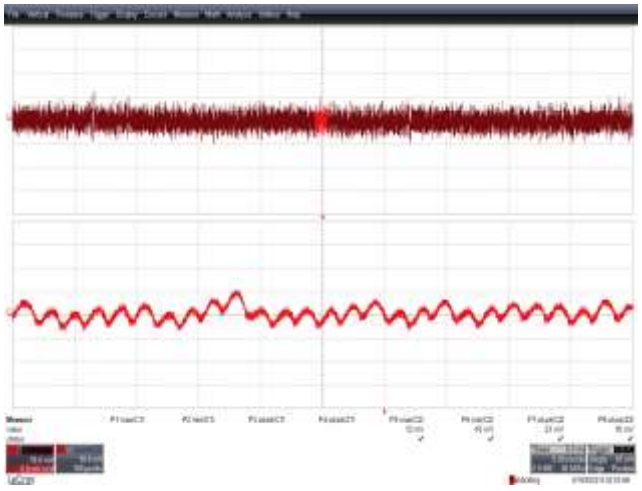


Figure 43 – Output Ripple Voltage Waveforms.
265 VAC Input. 5 V_{PK-PK}: 23 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

11.3.2.4 75% Load

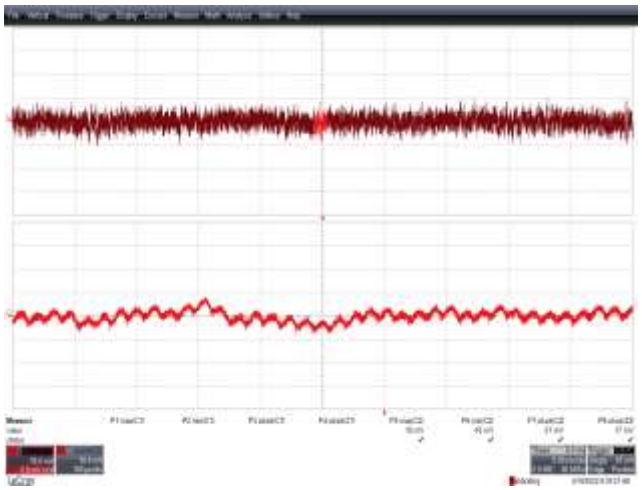


Figure 44 – Output Ripple Voltage Waveforms.
85 VAC Input. 5 V_{PK-PK}: 21 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

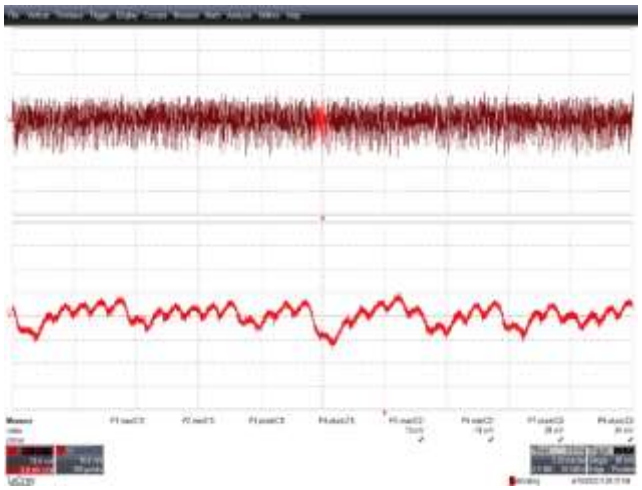


Figure 45 – Output Ripple Voltage Waveforms.
265 VAC Input. 5 V_{PK-PK}: 28 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

11.3.2.5 100% Load

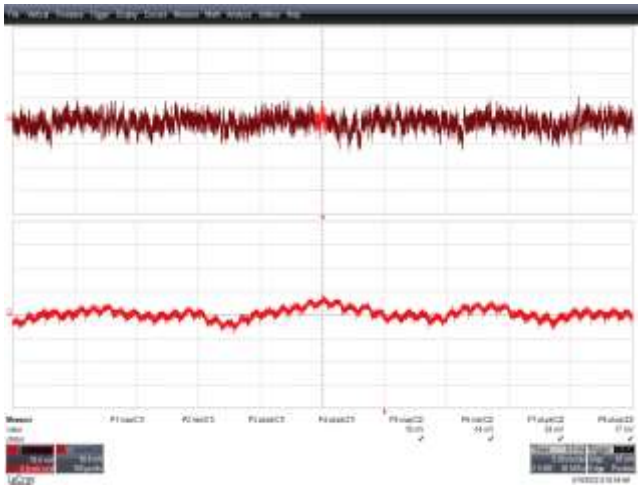


Figure 46 – Output Ripple Voltage Waveforms.
85 VAC Input. 5 V_{PK-PK}: 24 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

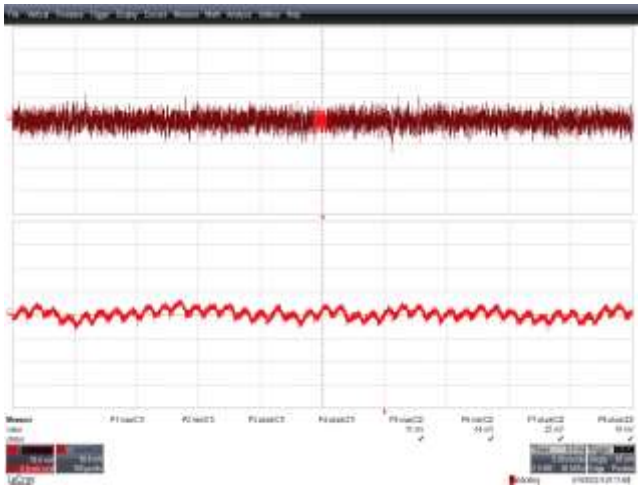


Figure 47 – Output Ripple Voltage Waveforms.
265 VAC Input. 5 V_{PK-PK}: 25 mV.
Upper: 5 V_{OUT}, 10 mV / div., 5 ms / div.
Zoom: 100 µs / div.

11.3.3 Ripple (ATE Measurements)

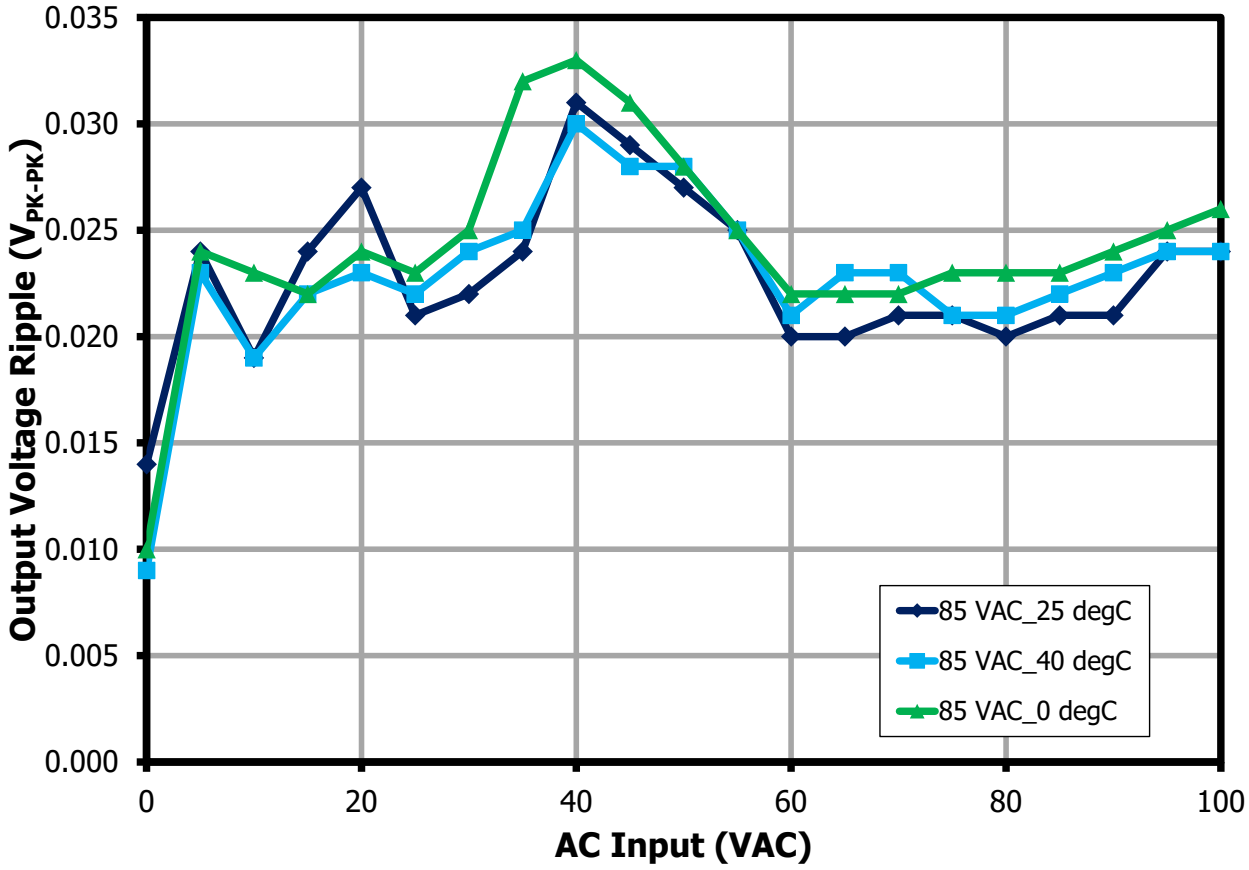


Figure 48 – 5 V Output Voltage Ripple vs. Output Load, 85 VAC Input.

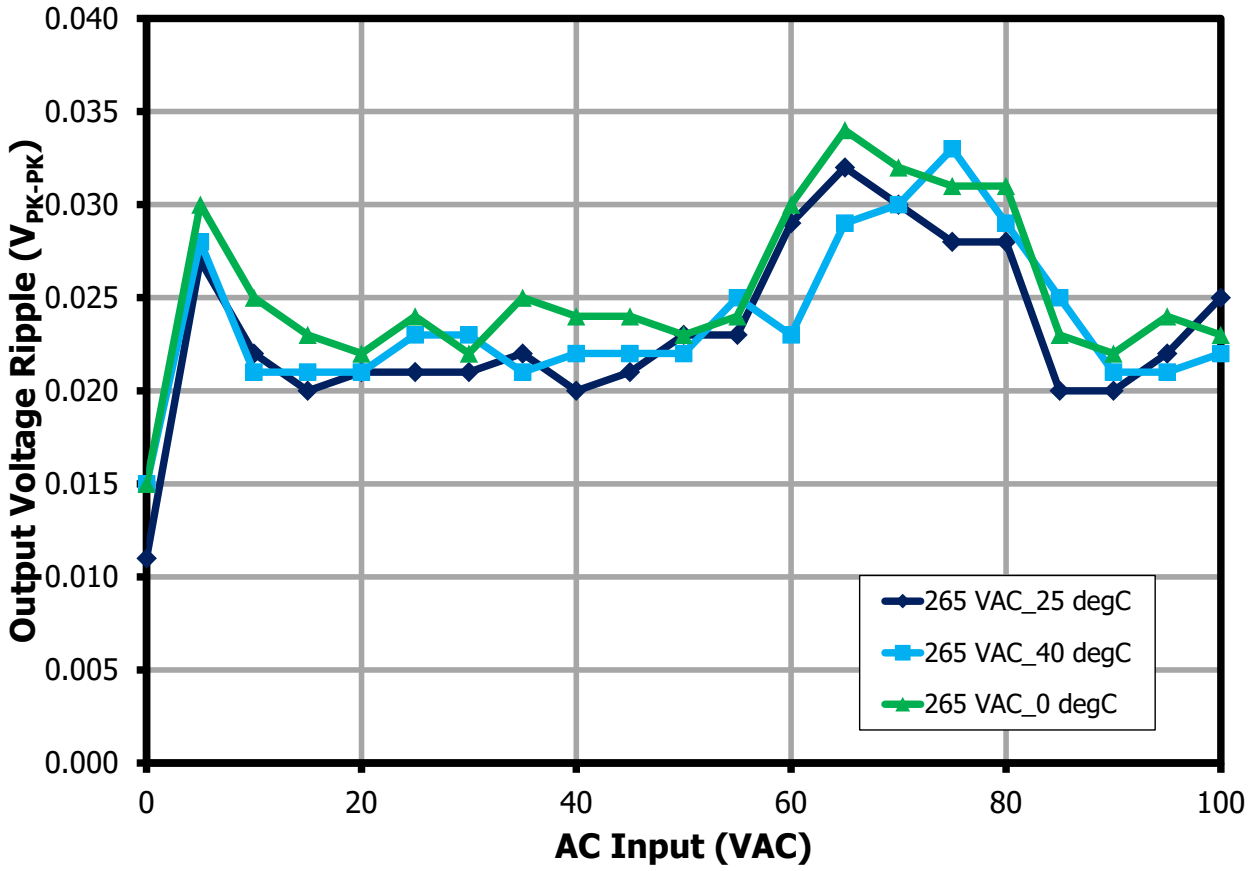


Figure 49 – 5 V Output Voltage Ripple vs. Output Load, 265 VAC Input.

12 EMI

12.1 Conductive EMI

12.1.1 Floating Output (QP / AV)

12.1.1.1 115 VAC Input

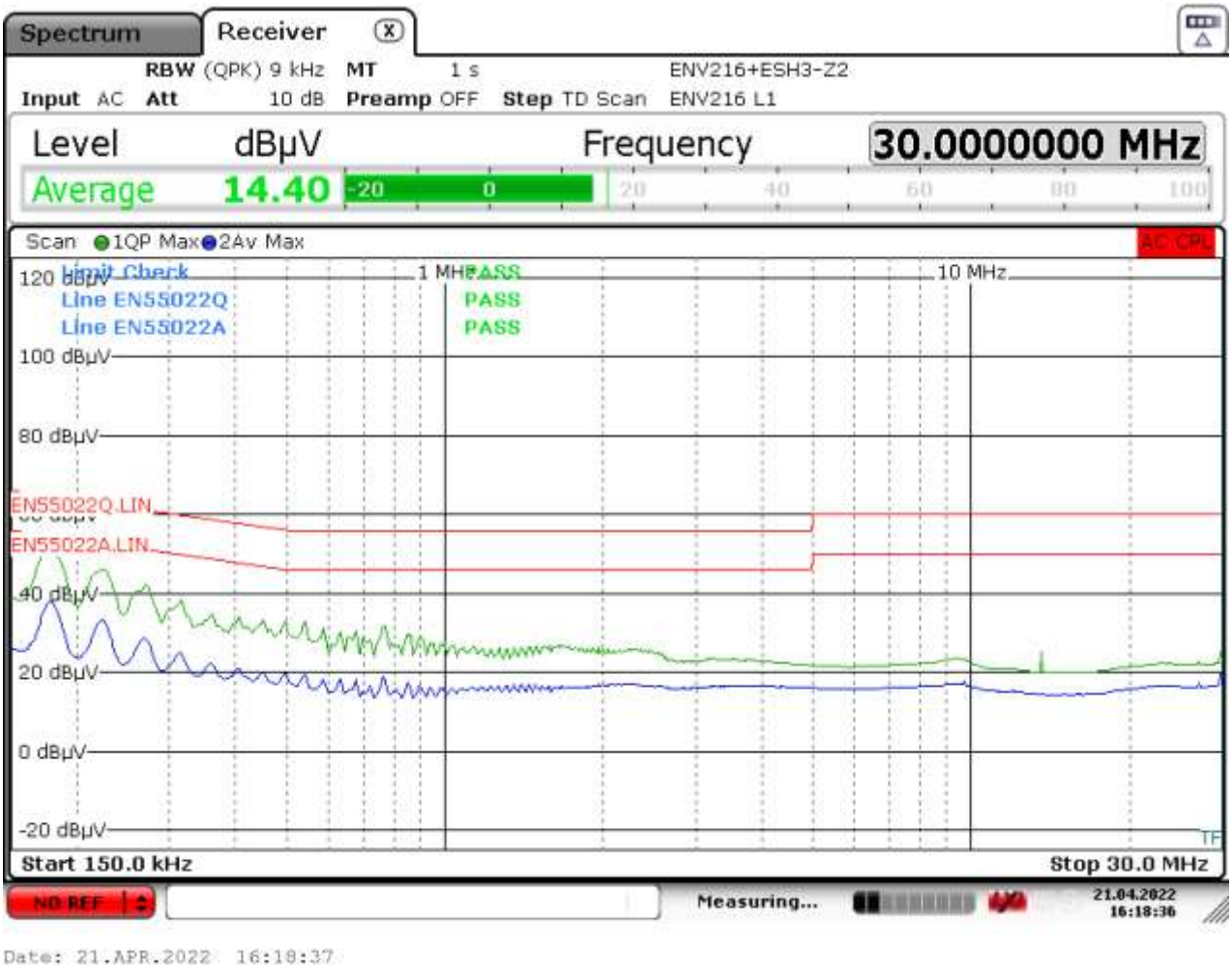


Figure 50 – Floating Ground - 115 VAC Line.

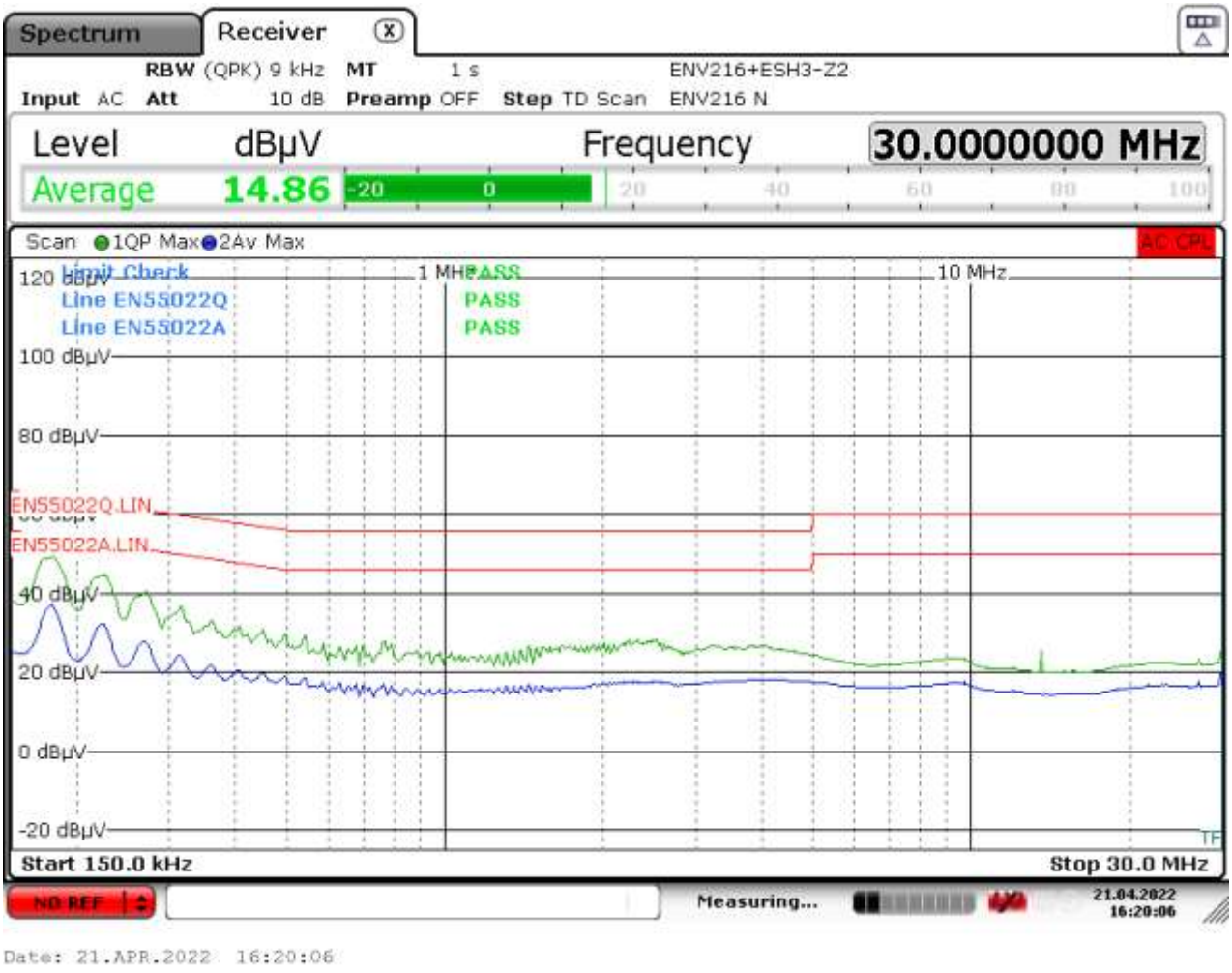


Figure 51 – Floating Ground - 115 VAC Neutral.

12.1.1.2 230 VAC Input

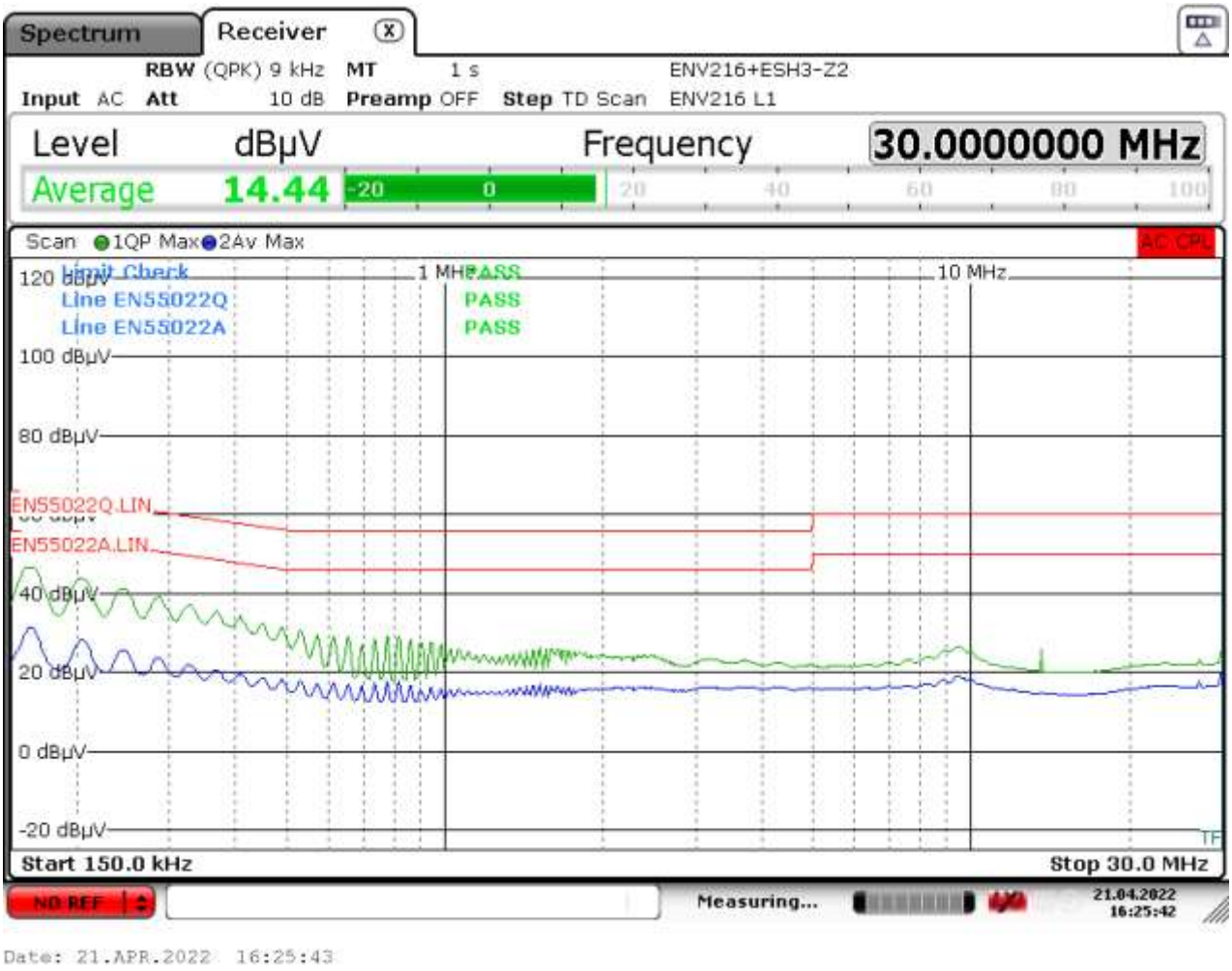


Figure 52 – Floating Ground - 230 VAC Line.

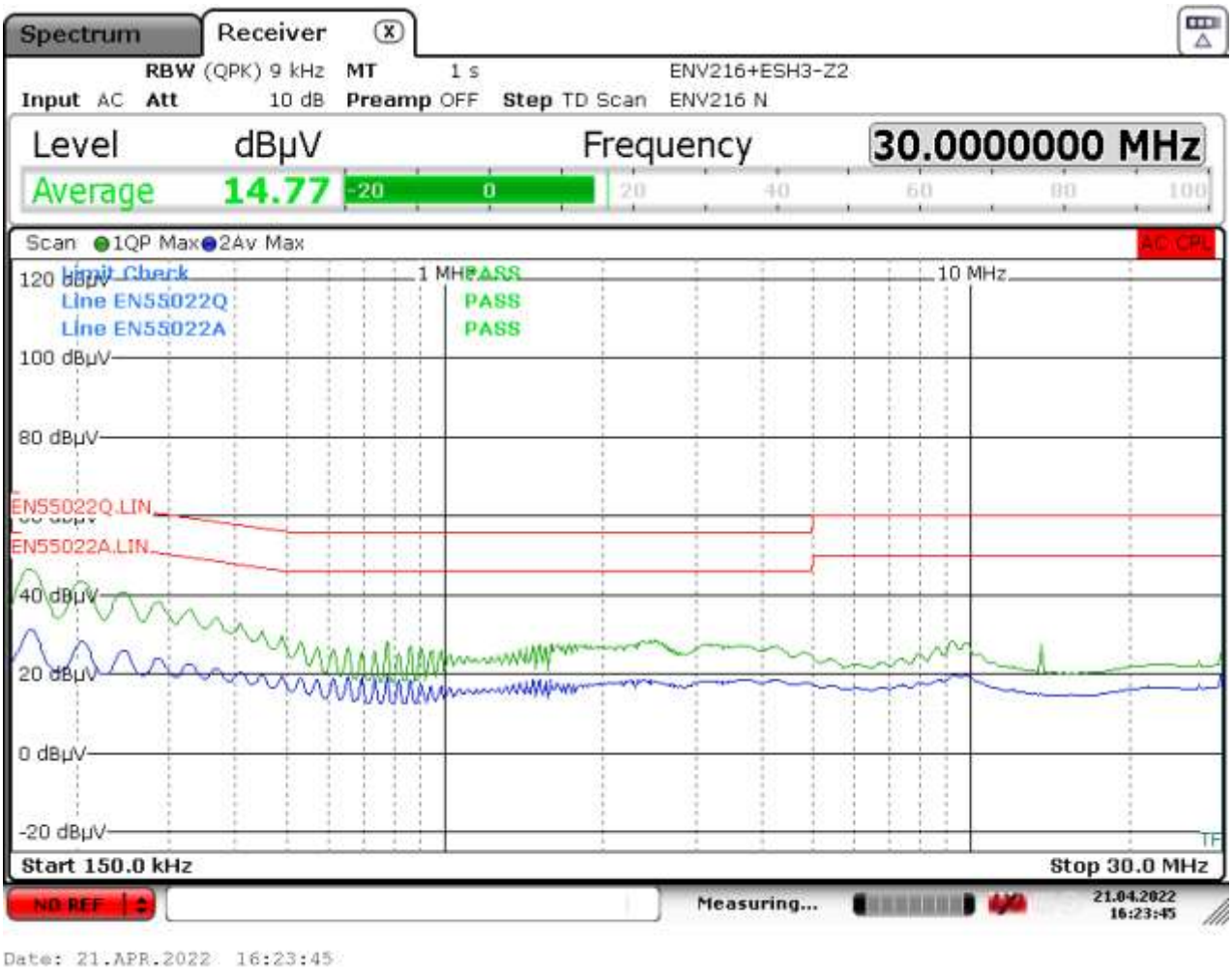


Figure 53 – Floating Ground - 230 VAC Neutral.

13 Lightning Surge Test

13.1 Differential Surge Test

Note: To pass 1 kV differential mode surge test the size of both input capacitors, C1 and C2, needs to be increased to 10 μF and add 10 Ω 0.7 A thermistor in series with Neutral Test Point.

Passed ±1 kV, 500 A surge test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
1	0	L, N	2	10	PASS (No AR)
-1	0	L, N	2	10	PASS (No AR)
1	90	L, N	2	10	PASS (No AR)
-1	90	L, N	2	10	PASS (No AR)
1	180	L, N	2	10	PASS (No AR)
-1	180	L, N	2	10	PASS (No AR)
1	270	L, N	2	10	PASS (No AR)
-1	270	L, N	2	10	PASS (No AR)

Figure 54 – 1 kV Differential Mode Surge Test.
InnoSwitch3-TN $V_{DS(MAX)}$: 651 V, $V_{BULK(MAX)}$: 472 V.
Upper: V_{BULK}, 200 V / div, 2 ms / div.
Lower: InnoSwitch3-TN V_{DS}, 200 V / div, 2 ms / div.
Zoom: 20 μs / div.

13.2 Ring Wave Test

Note: To pass 6 kV Ring Wave test the size of both input capacitors, C1 and C2, needs to be increased to 10 μF and add 10 Ω 0.7 A thermistor in series with Neutral Test point.

Passed ±6 kV Ring Wave Test

Ring Wave Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
4	0	L, N	12	10	PASS (1/10 AR)
-4	0	L, N	12	10	PASS (1/10 AR)
4	90	L, N	12	10	PASS (6/10 AR)
-4	90	L, N	12	10	PASS (No AR)
4	270	L, N	12	10	PASS (No AR)
-4	270	L, N	12	10	PASS (2/10 AR)
5	0	L, N	12	10	PASS (10/10 AR)
-5	0	L, N	12	10	PASS (4/10 AR)
5	90	L, N	12	10	PASS (8/10 AR)
-5	90	L, N	12	10	PASS (1/10 AR)
5	270	L, N	12	10	PASS (10/10 AR)
-5	270	L, N	12	10	PASS (2/10 AR)
6	0	L, N	12	10	PASS (10/10 AR)
-6	0	L, N	12	10	PASS (6/10 AR)
6	90	L, N	12	10	PASS (10/10 AR)
-6	90	L, N	12	10	PASS (2/10 AR)
6	270	L, N	12	10	PASS (6/10 AR)
-6	270	L, N	12	10	PASS (2/10 AR)

Figure 55 – 6 kV Ring Wave Test.
InnoSwitch3-TN $V_{DS(MAX)}$: 485 V, $V_{BULK(MAX)}$: 370 V.
Upper: V_{BULK}, 200 V / div, 2 ms / div.
Lower: InnoSwitch3-TN V_{DS}, 200 V / div, 2 ms / div.
Zoom: 20 μs / div.

13.3 EFT / Burst Test

Note: To pass 2 kV EFT test the size of both input capacitors, C1 and C2, needs to be increased to 10 μF and add 10 Ω 0.7 A thermistor in series with Neutral Test point.

Passed ±2 kV EFT Test

EFT Voltage (kV)	Phase Angle (°)	Frequency (kHz)	T-Burst	T-Rep	Coupling	Test Result
2	0	5	15 ms	120 s	L, N	PASS (No AR)
-2	0	5	15 ms	120 s	L, N	PASS (No AR)
2	0	100	750 us	120 s	L, N	PASS (No AR)
-2	0	100	750 us	120 s	L, N	PASS (No AR)
2	90	5	15 ms	120 s	L, N	PASS (No AR)
-2	90	5	15 ms	120 s	L, N	PASS (No AR)
2	90	100	750 us	120 s	L, N	PASS (No AR)
-2	90	100	750 us	120 s	L, N	PASS (No AR)
2	180	5	15 ms	120 s	L, N	PASS (No AR)
-2	180	5	15 ms	120 s	L, N	PASS (No AR)
2	180	100	750 us	120 s	L, N	PASS (No AR)
-2	180	100	750 us	120 s	L, N	PASS (No AR)
2	270	5	15 ms	120 s	L, N	PASS (No AR)
-2	270	5	15 ms	120 s	L, N	PASS (No AR)
2	270	100	750 us	120 s	L, N	PASS (No AR)
-2	270	100	750 us	120 s	L, N	PASS (No AR)

Figure 56 – 2 kV EFT Test.
InnoSwitch3-TN $V_{DS(MAX)}$: 517 V, $V_{BULK(MAX)}$: 363 V.
Upper: V_{BULK}, 200 V / div, 2 ms / div.
Lower: InnoSwitch3-TN V_{DS}, 200 V / div, 2 ms / div.
Zoom: 20 μs / div.

14 Appendix

14.1 Primary Winding – Conventional vs. Sectional Winding Comparison

14.1.1 Transformer Construction Comparison

Note: Both transformers have identical transformer parameters, only the Primary winding construction are different.

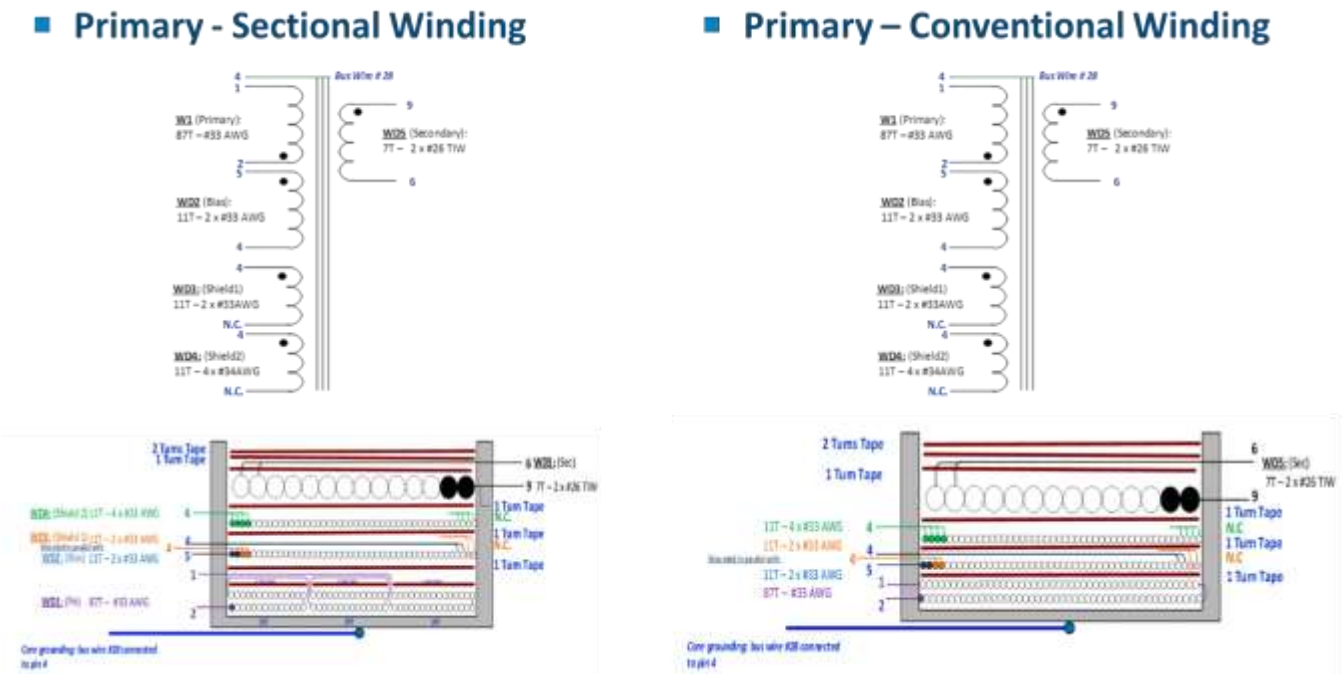


Figure 57 – Transformer Construction (Conventional vs. Sectional).

14.1.2 Transformer Electrical Parameters Comparison

Primary – Sectional Winding	Primary – Conventional Winding
Lp – 970 μH	Lp – 998 μH
RSF – 1429 kHz	RSF – 735 kHz
Lk – 38 μH	Lk – 35 μH

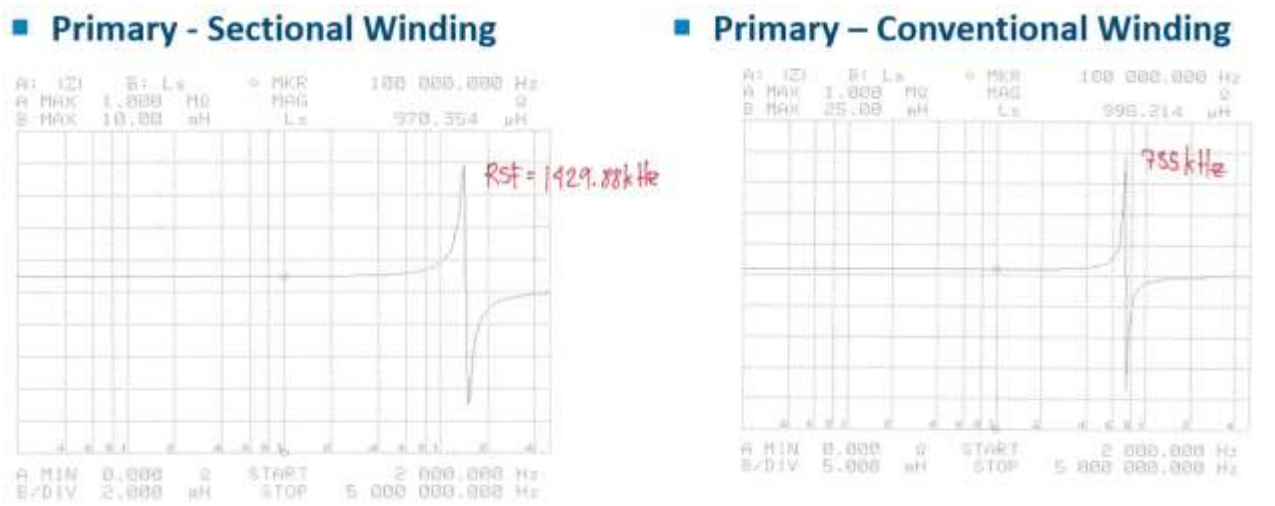


Figure 58 – Transformer Electrical Parameters Comparison.

Sectional Winding has greater resonant frequency, reducing the effective capacitance compared with the Conventional Winding.

14.1.3 Performance Comparison

14.1.3.1 Efficiency vs. Line

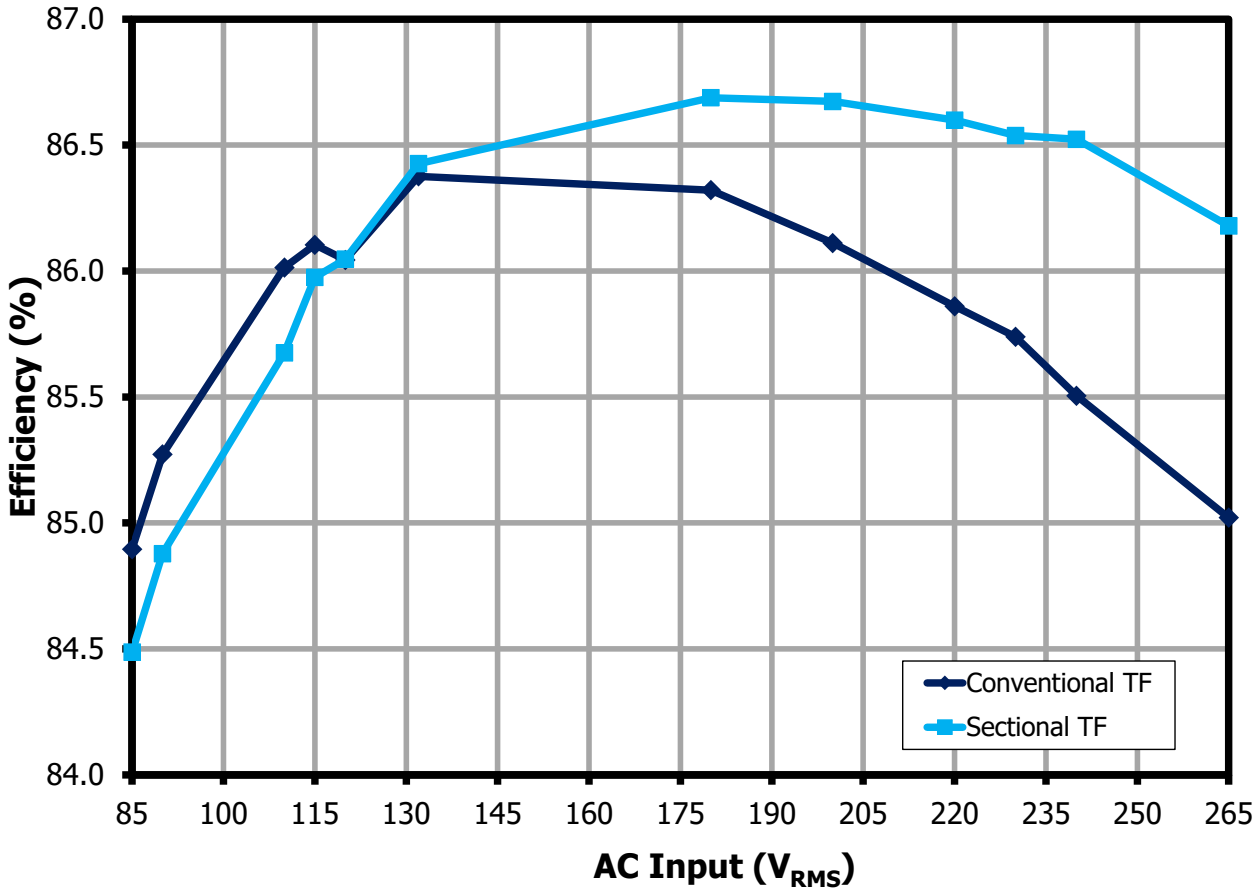


Figure 59 – Efficiency vs. Line.

14.1.3.2 Standby Efficiency vs. Line (5 V / 30 mA)

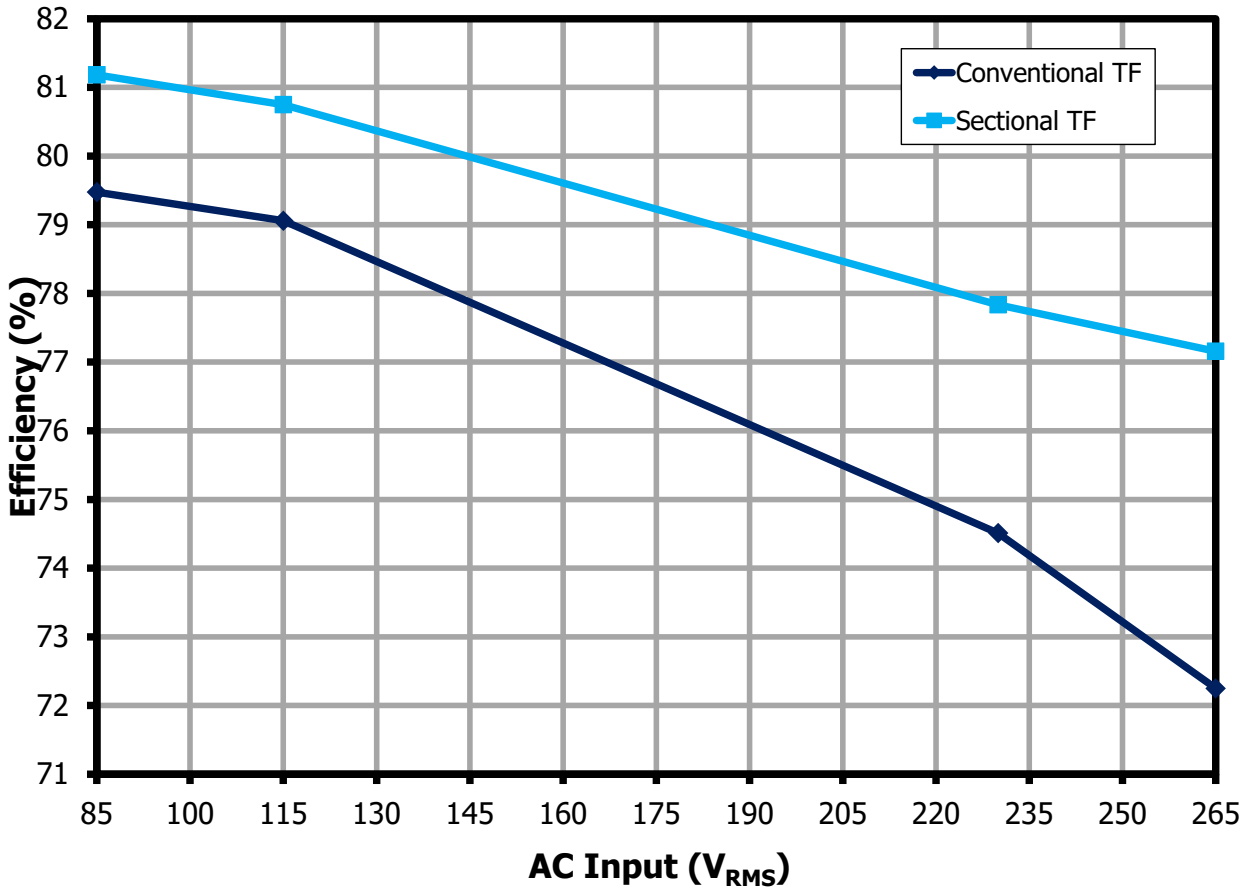


Figure 60 – Standby Efficiency vs. Line.

14.1.3.3 No-Load Input Power at 230 VAC Input

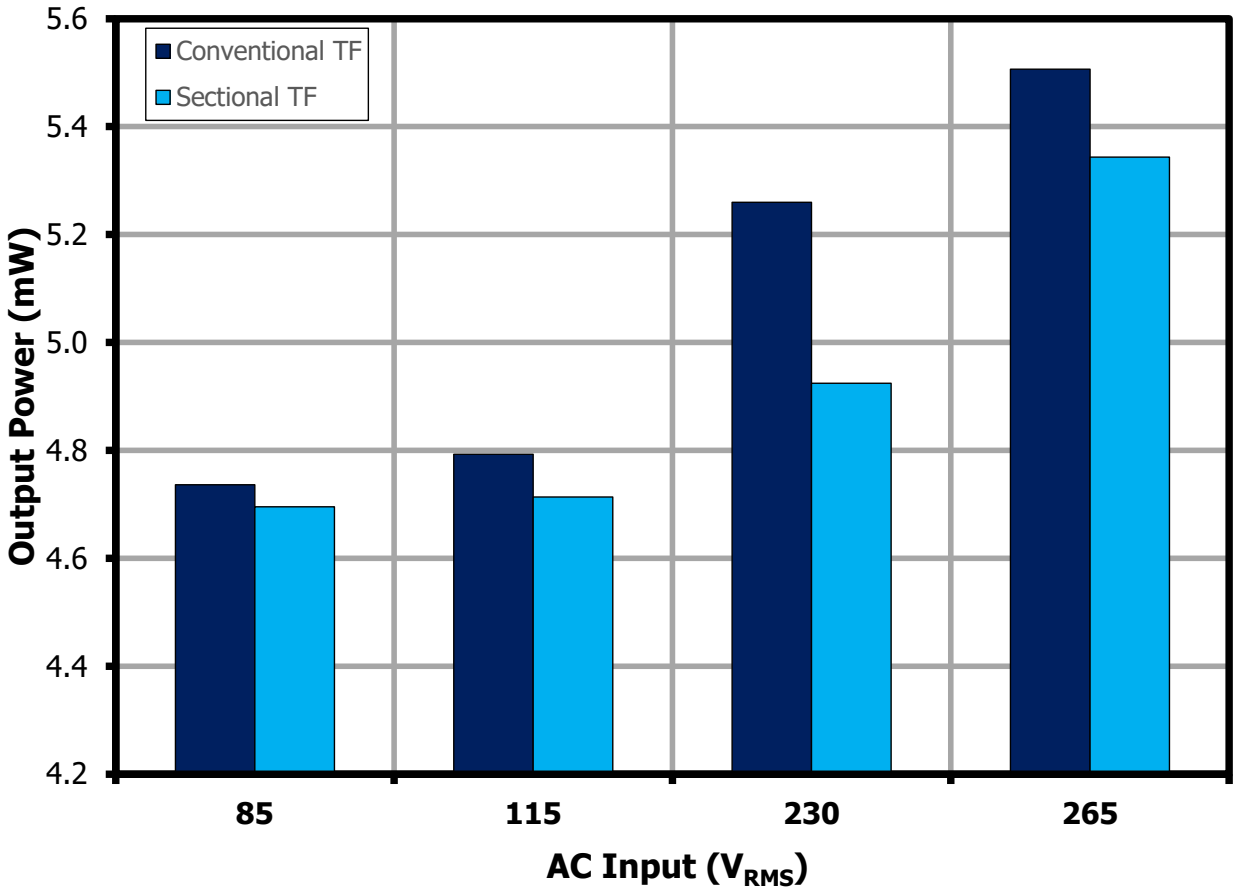


Figure 61 – No-Load Input Power.

14.1.3.4 Standby Input Power (5 V / 30 mA)

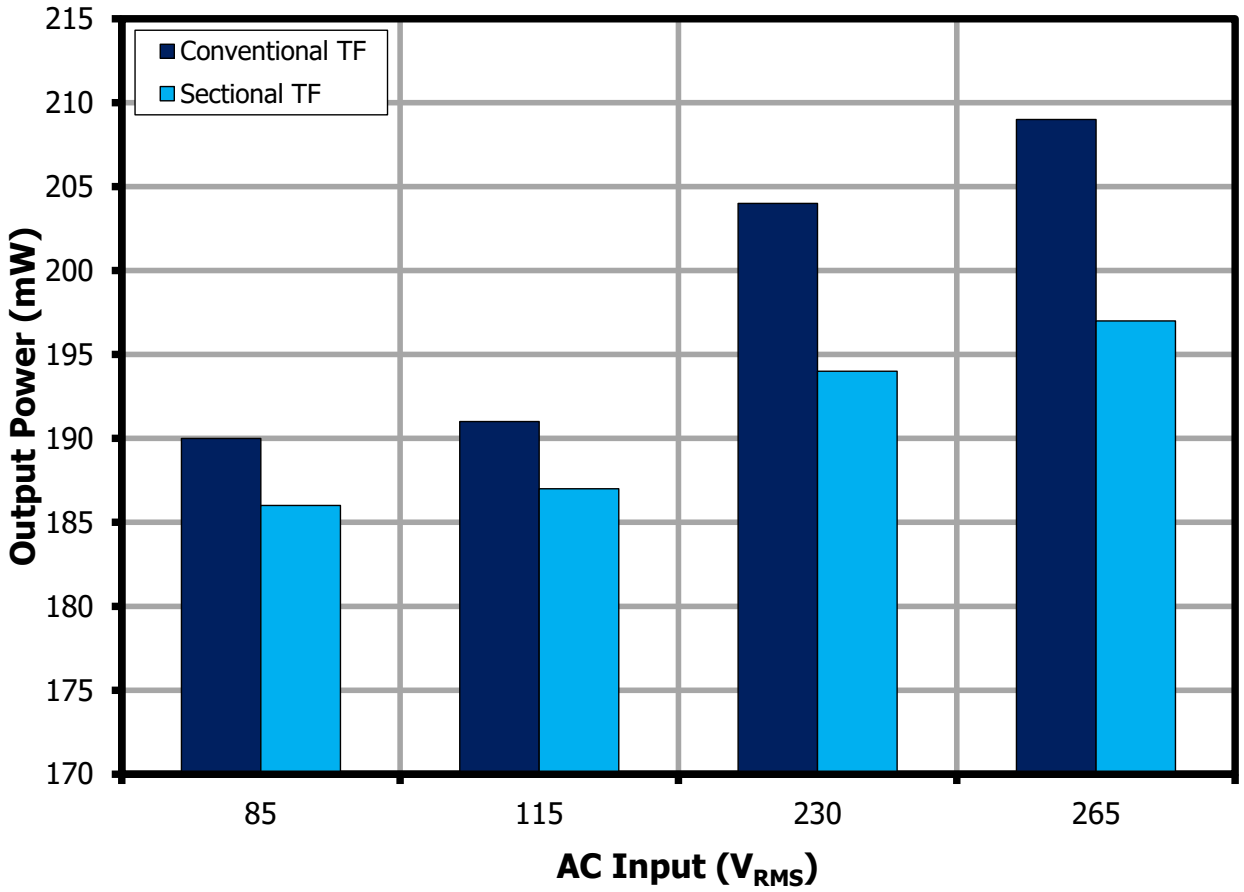


Figure 62 – Standby Input Power (5 V / 30 mA).

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
21-Jun-22	MA	1.0	Initial Release.	Apps & Mktg

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