Reference Design Report

Title	**35 W Automotive Power Supply for 800 V Systems Using InnoSwitch™3-AQ INN3947FQ**
Specification	200 VDC – 1000 VDC Input; 24.0 V / 1.46 A Output
Application	Gate Driver Power Supply for a Traction Inverter or Emergency Power Supply
Author	Automotive Systems Engineering Department
Document Number	RDR-994Q
Date	June 24, 2025
Revision	A

Summary and Features

- Ultra-compact design for 800 VDC automotive BEV applications
- Low component count (only 59 electrical components)
- Uses new InSOP28 (F) package for InnoSwitch3-AQ which provides 5 mm Drain to Source pin spacing (IEC-60664-1 compliant)
- Wide-range start-up and operating voltage from 200 VDC to 1000 VDC[1]
- Transformer provides reinforced isolation at 1000 V (IEC-60664-1 and IEC-60664-4 compliant)
- ≥85% full-load efficiency across the input voltage range
- Accurate secondary-side regulation without optocouplers
- Provides continuous 35 W power from -40 °C to 85 °C[2]
- Comprehensive fault protection, including output current limit and short-circuit
- Uses automotive-qualified AEC-Q surface mount (SMD) components[3]
- Low profile, only 18 mm high

[1] Derated power delivery for input below 200 VDC input.
[2] Derated power delivery beyond 85 °C ambient and a maximum limit of 105 °C.
[3] AEC-Q200 transformer qualification and input common-mode choke selection belongs to final design.

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Table of Contents

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1 Introduction

This engineering report describes a 35 W single-output automotive power supply for electric vehicles with an 800 V battery system. The design supports a wide input range of 200 VDC to 1000 VDC and uses the 1700 V rated INN3947FQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (low-voltage output) sides and meets creepage and clearance requirements described in IEC-60664 parts 1 and 4. The ≥5.0 mm Drain to Source pin spacing provided by the INN3947FQ IC in the F package also complies with primary-side creepage and clearance requirements (functional isolation for 2.5 kV transients).

This document contains the power supply specification, schematic, printed circuit board (PCB) layout, bill of materials (BOM), details of the magnetics, and comprehensive performance data.

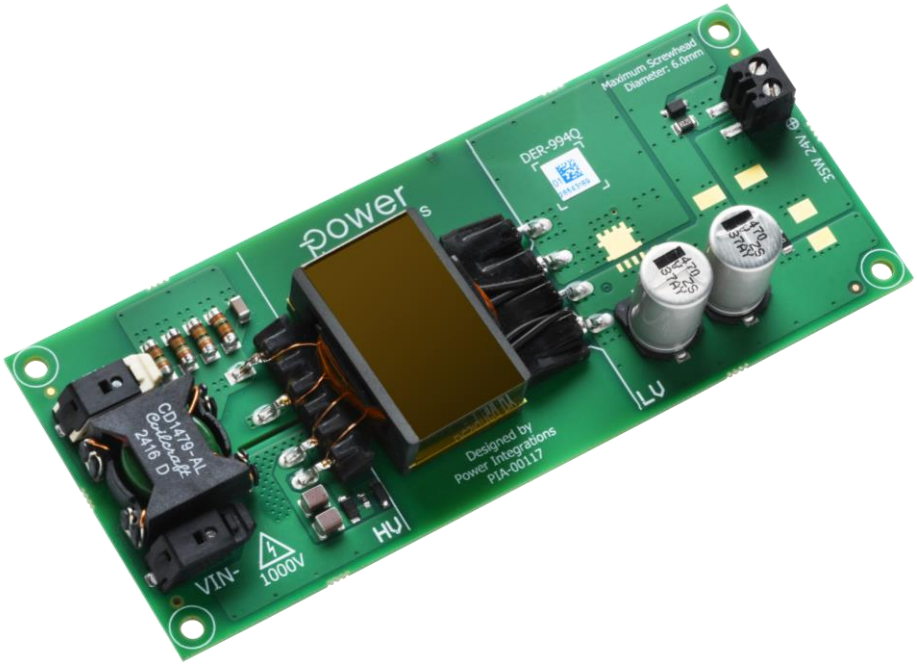


Figure 1 — Populated Circuit Board, Entire Assembly.

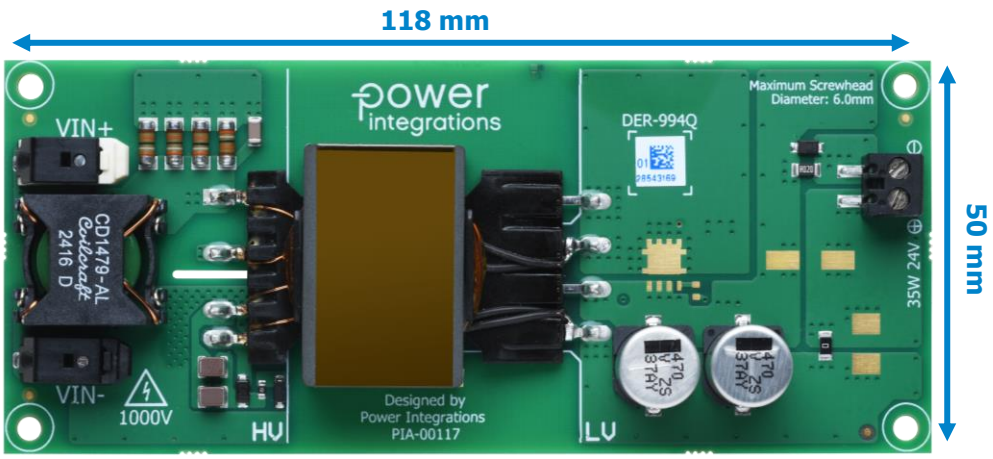


Figure 2 – Populated Circuit Board, Top.

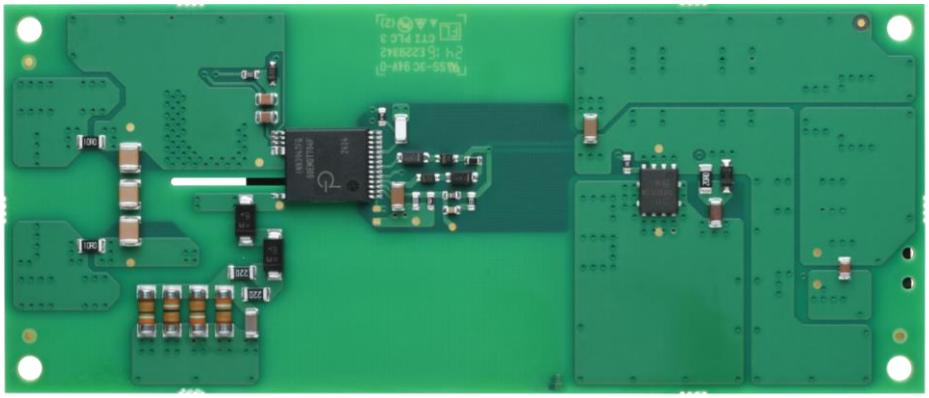


Figure 3 – Populated Circuit Board, Bottom.

Figure 4 – Populated Circuit Board, Side.

The design can deliver the full rated 35 W output power at 85 °C ambient from 200 VDC to 1000 VDC input, with derated output power beyond 85 °C up to a hard limit of 105 °C ambient. The 24 V output allows the power supply to act as traction inverter gate power supply or perform in the role of an emergency power supply. A summary of power delivery below 200 VDC input and thermal derating are provided in tables 14 and 15.

The InnoSwitch3-AQ IC maintains regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink™ magneto-inductive coupling. The secondary-side controller also provides drive for synchronous rectification improving overall efficiency (compared to a conventional diode rectifier) and eliminating heatsinks.

2 Design Specification

The following tables represent the minimum acceptable performance for the design. Actual performance is listed in the results section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV**	200	800	1000	VDC
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	V_{OUT}	22.8	24	25.2	VDC
Output Voltage Load and Line Regulation	V_{REG}	-5		+5	%
Ripple Voltage Measured on Board	V_{RIPPLE}		500		mV
Output Current Parameters					
Output Current	I_{OUT}		1460		mA
Output Power Parameters					
Continuous Output Power at 200 VDC – 1000 VDC Input	P_{OUT}		35[4]		W
Output Overshoot and Undershoot During Dynamic Load Condition	ΔV_{OUT}	-5		+5	%
Operating Parameters					
Operating Switching Frequency	f_{SW}	25		31.6	kHz

Table 1 – Electrical Specifications.

[4] From -40 °C to 85 °C ambient. For maximum output power capability at higher temperature, see Section 13.

2.2 Isolation

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3947FQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			1400	V
Working Voltage	$V_{WORKING}$			1000	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175			
Rated Impulse Voltage	$V_{IMPULSE}$			2.50	kV
Altitude Correction Factor for h_a	C_{ha}			1.59	
Basic Clearance Distance Requirement	CLR_{BASIC}	2.4			mm
Reinforced Clearance Distance Requirement	$CLR_{REINFORCED}$	4.8			mm
Basic Creepage Distance Requirement for PCB	$CPG_{BASIC(PCB)}$	5.0			mm
Reinforced Creepage Distance Requirement for PCB	$CPG_{REINFORCED(PCB)}$	10.0			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60 s	V_{ISO}	3540			V_{RMS}
Partial Discharge Test Voltage	V_{PD_TEST}	2100			V_{PK}

Table 2 – Isolation Coordination[5].

2.3 Environmental Specification

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		105	°C
Altitude of Operation	Ha			5500	m

Table 3 – Environmental Specifications.

[5] Clearance and creepage distances were calculated according to IEC 60664-1 and IEC 60664-4.

3 Schematic

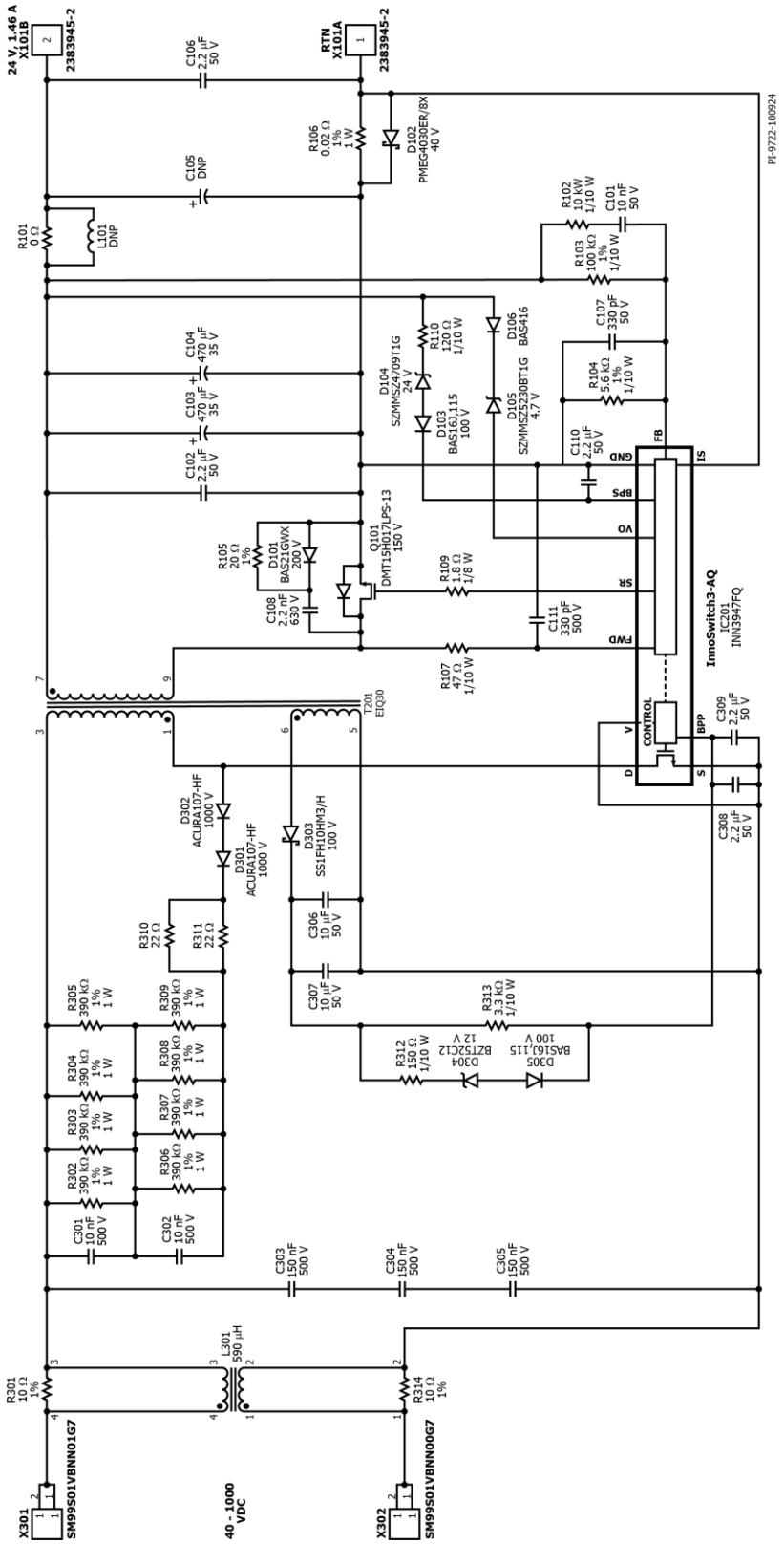


Figure 5 – RDR-994Q Schematic.

4 Circuit Description

4.1 Input Filter

The automotive inverter environment is harsh, characterized by high dv/dt and di/dt from the switching action of the power modules. These transient events can create high electrical noise levels that can interfere with the operation of the power supply. The input common mode choke, L301, together with capacitors C303 to C305, reduces the noise entering the power supply and prevents it from affecting performance.

Capacitors C303 to C305 minimize the primary-side current loop. The voltage rating of the capacitors was chosen so as not to exceed 65% of the maximum voltage rating even in worst case conditions. Capacitor case size was selected to ensure adequate pad separation for an automotive design that meets relevant creepage and clearance requirements. Resistors R301 and R314 provide damping to reduce the imposition of oscillation to the input voltage during each switching cycle.

4.2 High-Voltage Circuit

The power supply is a flyback converter topology that provides an isolated low-voltage output from the high-voltage input. The primary winding of flyback transformer T201 was connected between the high-voltage DC input and the drain pin of the 1700 V SiC power switch integrated into the InnoSwitch3-AQ IC (IC201).

An R2CD-type snubber circuit was placed across the primary winding to limit the drain-source voltage peak during turn-off. Two super-fast surface-mount, AEC-Q qualified diodes (D301 and D302), were placed in series to meet creepage and clearance requirements. This also ensures that the reverse voltage across the diodes will not exceed 70% of their maximum rating. Capacitors C301 and C302 store the energy from the leakage inductance of transformer T201. The capacitors were sized to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation through the switching cycle. Resistors R302 to R309 dissipate the energy stored by the snubber capacitors. The resistor values were selected so that their average voltage did not exceed 80% of their maximum rated voltage and to dissipate less than 50% of their power rating.

The auxiliary winding of transformer T201 provides power to the primary-side during normal operation. This improves efficiency and reduces heating of the InnoSwitch3-AQ IC. The output of the auxiliary winding is rectified and filtered by diode D303 and capacitors C306 and C307. The InnoSwitch3-AQ IC is self-starting, using an internal high-voltage current source to charge the BPP capacitors, C308 and C309. Current is injected into the BPP capacitors through resistor R313. Diodes D304, D305, and resistor R312 serve as a primary-sensed output overvoltage protection (primary OVP) circuit, which injects current to the BPP pin of InnoSwitch3-AQ IC during output overvoltage events, driving the IC to enter auto-restart (AR) as long as the fault is present.

In this design, input UV features were disabled by shorting the V pin to the SOURCE pin. This allows the design to operate at inputs as low as 40 VDC.

4.3 Low-Voltage Circuit

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR FET Q101 rectifies the voltage across the secondary winding of the transformer T201, which is then filtered by output capacitors C102, C103, and C104. An RCD-type snubber formed by resistor R105, diode D101, and capacitor C108 damps the high-frequency ringing across the Drain-Source nodes of the SR FET.

The secondary-side controller inside InnoSwitch3-AQ IC controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed by the FWD pin via resistor R107. Capacitor C111 and resistor R107 form a low-pass filter that reduces voltage spikes seen by the FWD pin and ensures that the maximum rating of 150 V is not exceeded. In continuous conduction mode operation, the SR MOSFET is turned off just before the secondary-side controller requests a new switching cycle from the primary. In discontinuous mode, the SR MOSFET is turned off when the voltage across it rises above $V_{SR(TH)}$. The secondary-side control of both SR MOSFET and primary-side switch prevents cross-conduction and ensures reliable SR operation.

The secondary-side of the InnoSwitch3-AQ IC is powered by either the secondary winding forward voltage (thru R107 and the FWD pin) or by the output voltage (thru the VOUT pin). In both cases, energy is used to charge the BPS capacitor C110 via an internal regulator. Diodes D105 and D106 introduce a voltage drop, which lowers the voltage seen by the VOUT pin and protects the pin in case of an output overvoltage event.

Diodes D103, D104, and resistor R110 comprise the secondary-side output overvoltage protection (secondary OVP) circuit. During output overvoltage events, current through these components will be injected into the BPS pin of InnoSwitch3-AQ IC, triggering AR.

The InnoSwitch3-AQ IC's FB pin has an internal 1.265 V reference. Resistors R103 and R104 form a voltage divider network. Capacitor C107 provides decoupling of high-frequency noise. C101 and R102 form a feedforward network to improve feedback response and lower output ripple. Resistor R101 is a default installation and is used to short inductor L101 when the output LC filter is not needed (if lower output ripple is required, remove R101 and install the appropriate inductor L101 and capacitor C105).

Output current is measured by monitoring the voltage drop across the resistor R106. A low internal current sense threshold of approximately 35 mV is used to reduce losses. Once the threshold is reached, InnoSwitch3-AQ IC will adjust the number of pulses to maintain a fixed output current (CC mode). The IC will enter auto-restart (AR) operation when the output voltage falls 10% below regulation during CC mode and recovers when the load current is reduced below the CC limit. Diode D101 limits the voltage across the IS pin to protect it during output short-circuits.

5 PCB Layout

Layers: Six (6)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 1 oz

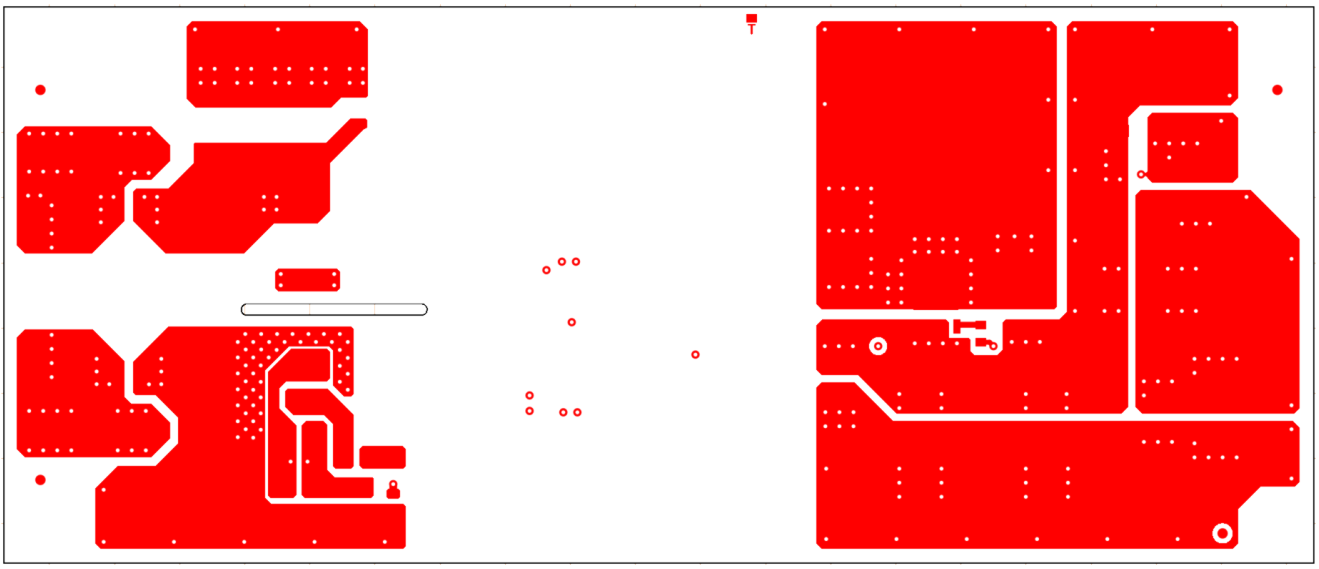


Figure 6 – RDR-994Q Top Layer PCB Layout.

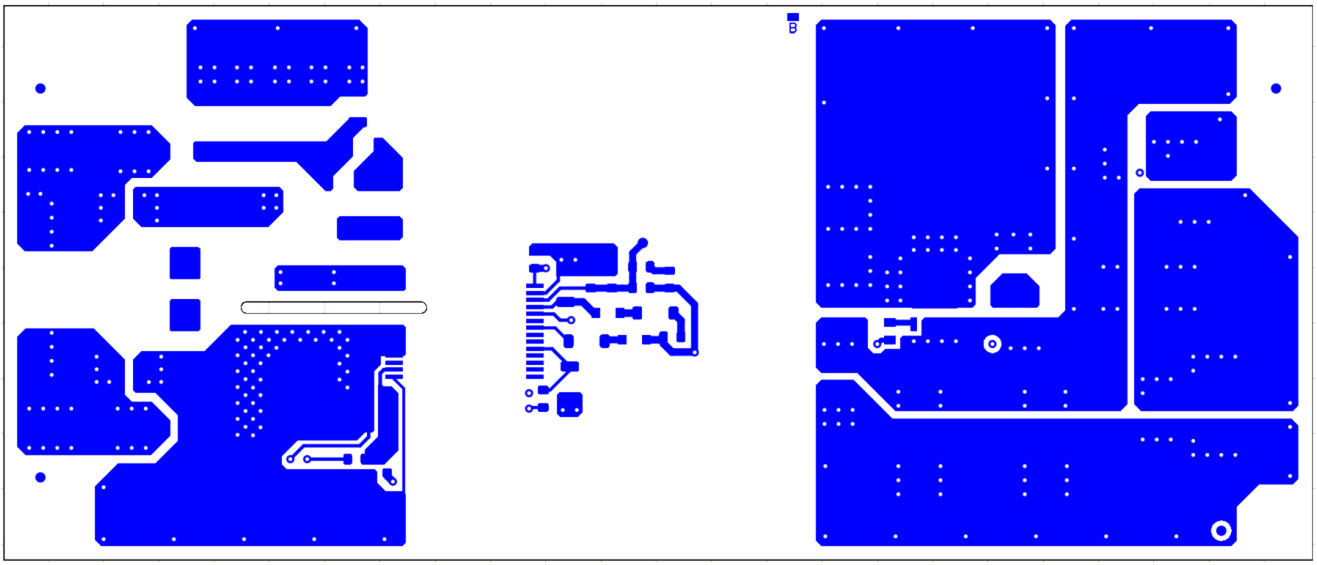


Figure 7 – RDR-994Q Bottom Layer PCB Layout.

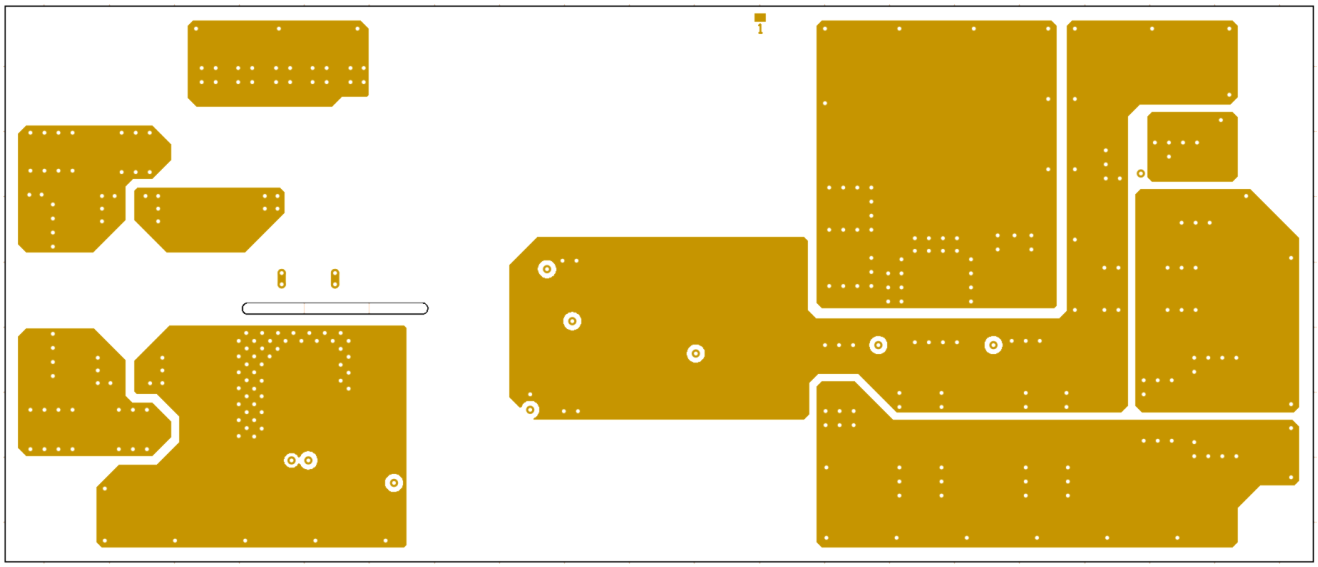


Figure 8 – RDR-994Q Mid-Layer 1 PCB Layout

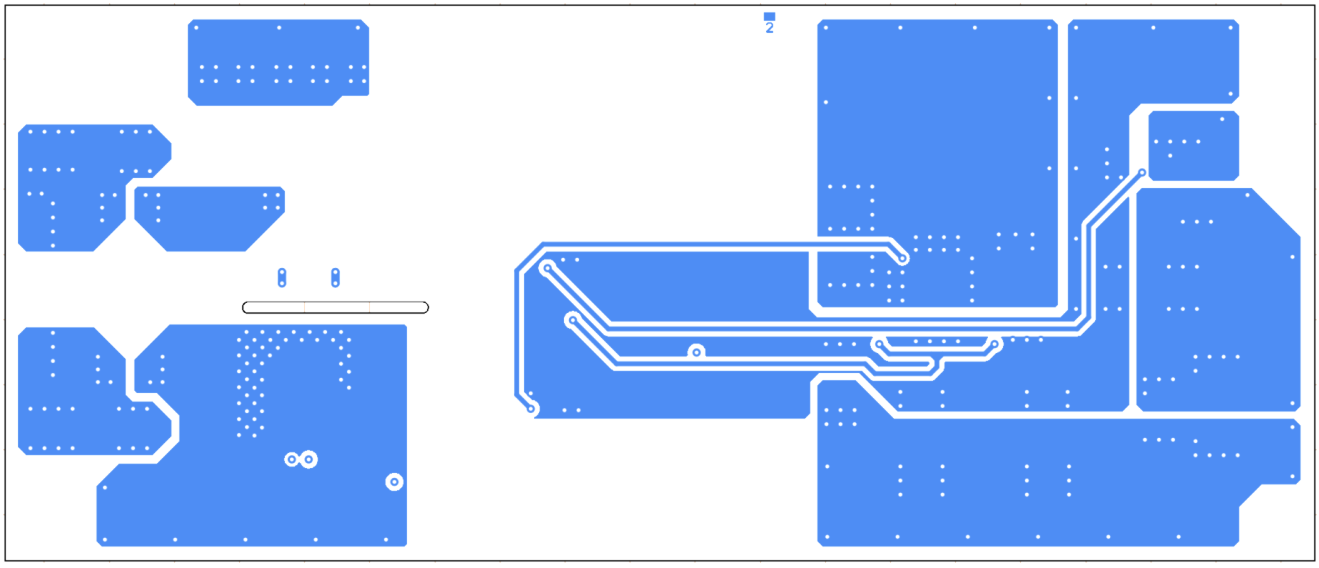


Figure 9 – RDR-994Q Mid-Layer 2 PCB Layout.

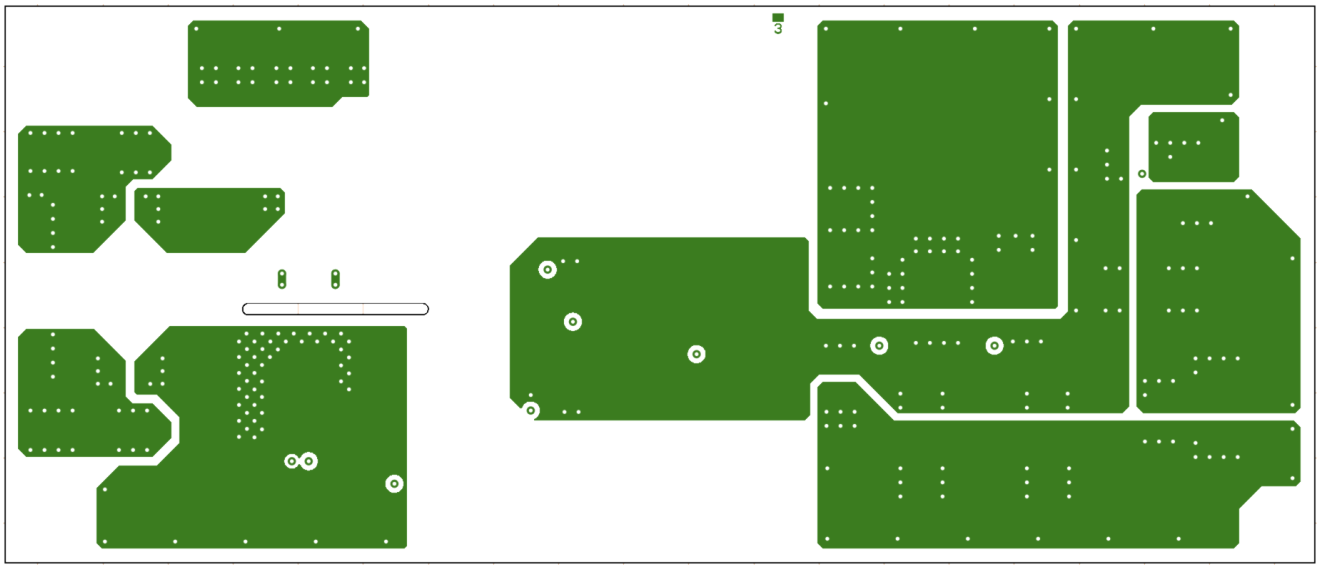


Figure 10 – RDR-994Q Mid-Layer 3 PCB Layout.

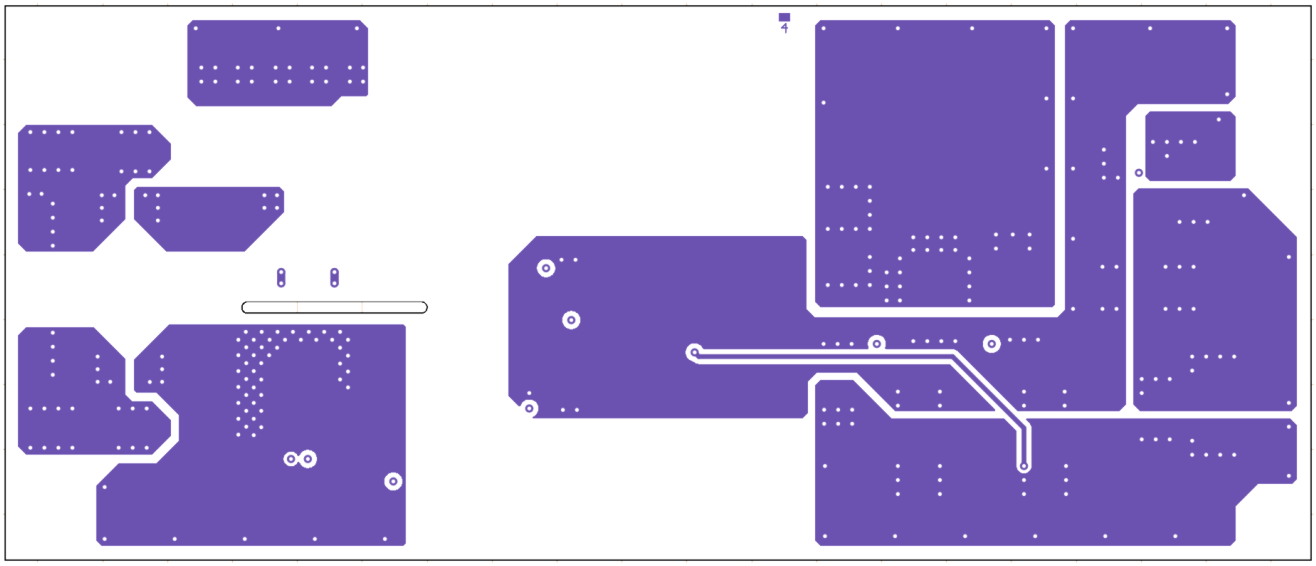


Figure 11 – RDR-994Q Mid-Layer 4 PCB Layout.

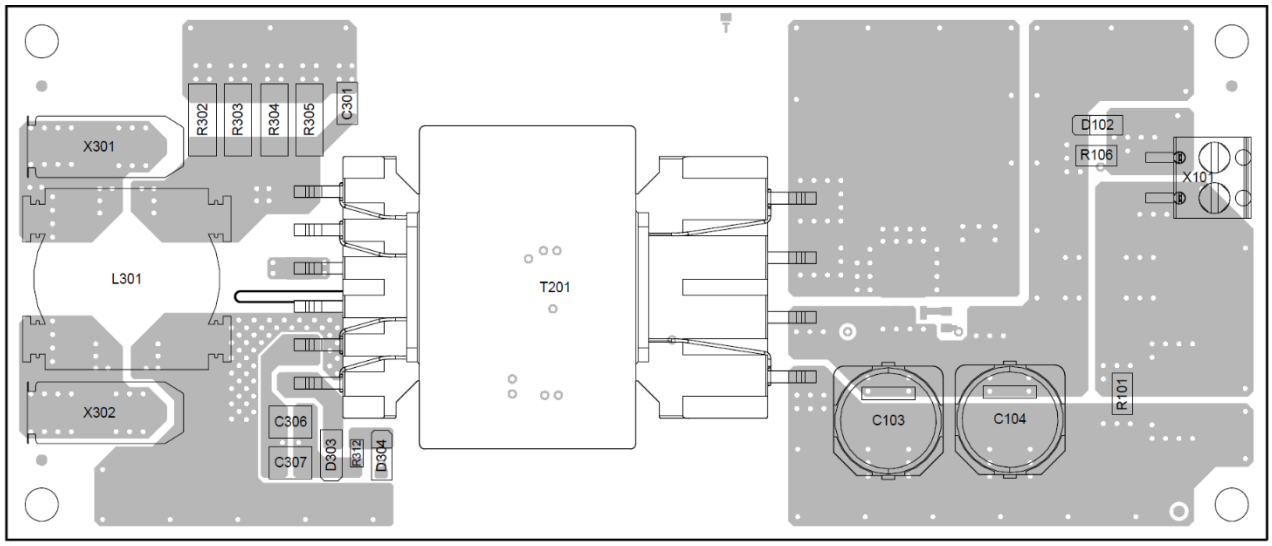
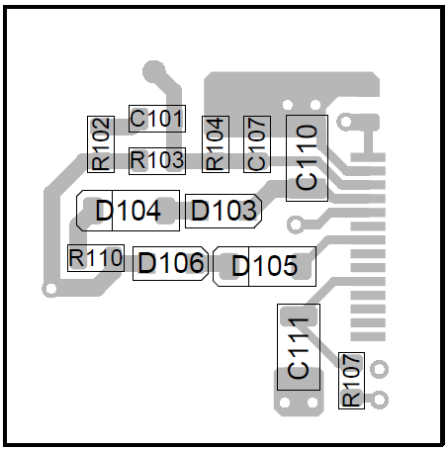


Figure 12 – RDR-994Q PCB Assembly (Top).



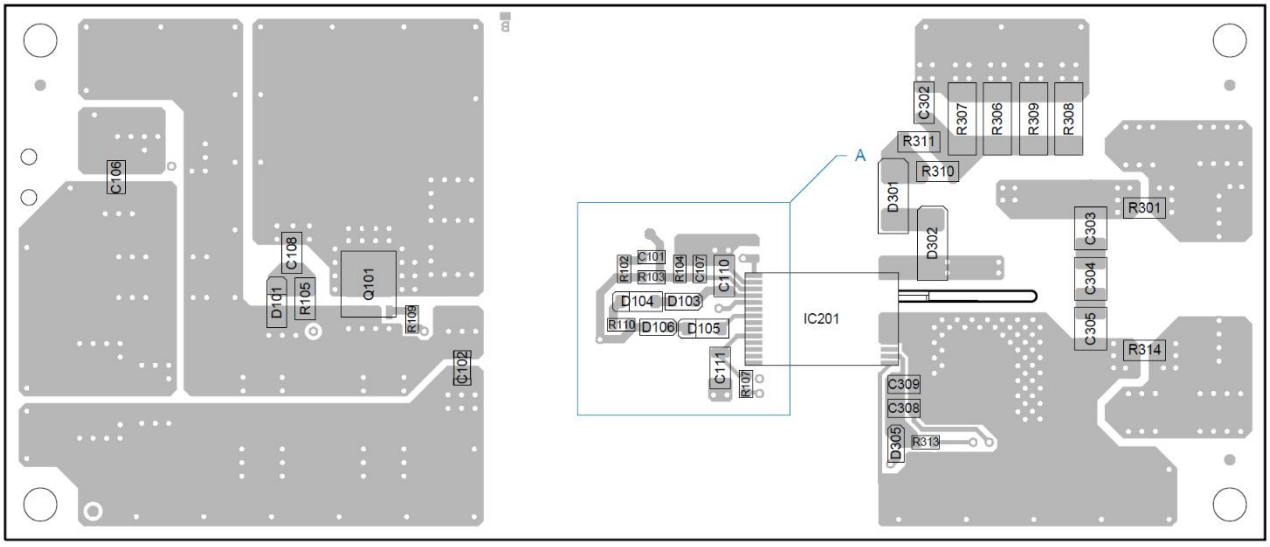


Figure 13 – RDR-994Q PCB Assembly (Bottom)

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	1	C101	10000 pF ±20% 50 V Ceramic Capacitor X7R 0603 (1608 Metric) AEC-Q200	C0603C103M5RACAUTO	KEMET
2	2	C102, C110	2.2 µF ±10% 50 V Ceramic Capacitor X7R 1206 (3216 Metric) AEC-Q200	GCM31CR71H225KA55K	Murata
3	2	C103, C104	470 µF 35 V Aluminum - Polymer Capacitors Radial, Can - SMD 11mOhm 4000 Hrs @ 125°C AEC-Q200	EEH-ZS1V471P	Panasonic
4	3	C106, C308, C309	2.2 µF ±10% 50 V Ceramic Capacitor X7R 0805 (2012 Metric) Soft Termination AEC-Q200	CGA4J3X7R1H225K125AE	TDK
5	1	C107	330 pF ±5% 50 V Ceramic Capacitor C0G, NP0 0603 (1608 Metric) AEC-Q200	C0603C331J5GACAUTO	KEMET
6	1	C108	2200 pF ±5% 630 V Ceramic Capacitor C0G, NP0 1206 (3216 Metric) AEC-Q200	GCM31B5C2J222JX01L	Murata
7	1	C111	330 pF ±10% 500 V Ceramic Capacitor C0G, NP0 1206 (3216 Metric) AEC-Q200	C1206C331KCGACAUTO	KEMET
8	2	C301, C302	10000 pF ±5% 500 V Ceramic Capacitor C0G, NP0 1206 (3216 Metric) AEC-Q200	C1206C103JCGACAUTO	KEMET
9	3	C303, C304, C305	0.15 µF ±10% 500 V Ceramic Capacitor X7R 1210 (3225 Metric) AEC-Q200	C1210X154KCRACAUTO	KEMET
10	2	C306, C307	10 µF ±10% 50 V Ceramic Capacitor X7R 1210 (3225 Metric) AEC-Q200	CNA6P1X7R1H106K250AE	TDK
11	1	D101	Diode 200 V 225 mA Surface Mount SOD-123 AEC-Q101	BAS21GWX	Nexperia
12	1	D102	Diode 40 V 3 A Surface Mount SOD-123W AEC-Q101	PMEG4030ER-QX	Nexperia
13	2	D103, D305	Diode Standard 100 V 250 mA SOD-323	BAS16J,115	Nexperia
14	1	D104	Zener Diode 24 V 500 mW ±5% Surface Mount SOD-123 AEC-Q101	SZMMSZ4709T1G	On Semi
15	1	D105	Zener Diode 4.7 V 500 mW ±5% Surface Mount SOD-123 AEC-Q101	SZMMSZ5230BT1G	Diodes, Inc.
16	1	D106	Diode 75 V 200 mA Surface Mount SOD-323 AEC-Q101	BAS416,115	Nexperia
17	2	D301, D302	Diode 1000 V 1 A Surface Mount DO-214AC (SMA) AEC-Q101	ACURA107-HF	Comchip
18	1	D303	Diode 100 V 1 A Surface Mount DO-219AB (SMF) AEC-Q101	SS1FH10HM3/H	Vishay
19	1	D304	Zener Diode 12 V 370 mW ±5.42% Surface Mount SOD-123	BZT52C12Q-13-F	Diodes
20	1	IC201	CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3947FQ	Power Integrations
21	1	L301	Input Common Mode Choke	CD1479-AL	Coilcraft
22	1	Q101	N-Channel 150 V 8 A (Ta), 50 A (Tc) 1.5 W (Ta), 107 W (Tc) Surface Mount, Wettable Flank PowerDI5060-8 (Type UX) AEC-Q101	DMTH15H017LPSWQ-13	Diodes, Inc.
23	1	R101	0 Ohms Jumper Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC1206JR-070RL	YAGEO
24	1	R102	10 kOhms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603JR-0710KL	YAGEO
25	1	R103	100 kOhms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RMCF0603FT100K	Stackpole

26	1	R104	5.6 kOhms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RMCF0603FT5K60	Stackpole
27	1	R105	20 Ohms ±1% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC1206FR-0720RL	Yageo
28	1	R106	20 mOhms ±1% 1 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Current Sense, Moisture Resistant Metal Element	CRF1206-FZ-R020ELF	Bourns
29	1	R107	47 Ohms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RMCF0603JT47R0	Stackpole
30	1	R109	1.8 Ohms ±5% 0.125 W, 1/8 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RK73B1JTTD1R8J	KOA
31	1	R110	120 Ohms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	CRCW0603120RJNEA	Vishay
32	2	R301, R314	10 Ohms ±1% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC1206FR-0710RL	YAGEO
33	8	R302, R303, R304, R305, R306, R307, R308, R309	390 kOhms ±1% 1 W Chip Resistor MELF, 0207 Anti-Sulfur, Automotive AEC-Q200 Thin Film	MMB02070C3903FB200	Vishay
34	2	R310, R311	22 Ohms ±5% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200 Thick Film	RK73B2BTTD220J	KOA
35	1	R312	150 Ohms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603JR-07150RL	YAGEO
36	1	R313	3.3 kOhms ±5% 0.1W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603JR-073K3L	YAGEO
37	1	T201	35 W Power Transformer	EIQ30	Power Integrations
38	1	T201-Core	3C96 Ferrite Core	EQ30 – 3C96	Ferroxcube
39	1	T201-Core	3C96 Ferrite Core	PLT30/20/3 – 3C96	Ferroxcube
40	1	T201-Bobbin	Customized Bobbin	MCT-EIQ3001 V4+6P	Power Integrations
41	1	X101	2 Position Wire to Board Terminal Block Horizontal with Board 0.150" (3.81mm) Surface Mount	2383945-2	TE
42	1	X301	1 Position Wire to Board Terminal Block Horizontal with Board Surface Mount	SM99S01VBNN01G7	METZ CONNECT
43	1	X302	1 Position Wire to Board Terminal Block Horizontal with Board Surface Mount	SM99S01VBNN00G7	METZ CONNECT
44	1	Z1	Printed Circuit Board, PIA-00117	PIA-00117-TL	Power Integrations

Table 4 – RDR-994Q Bill of Materials[6].

[6] All components are AEC-Q qualified except the connectors, input common mode choke, and transformer.

7 Transformer Specification (T201)

7.1 Electrical Diagram

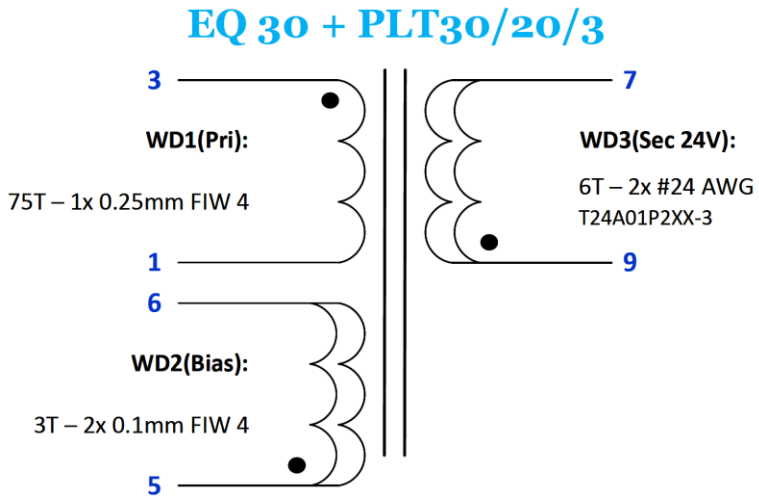


Figure 14 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			35	W
Input voltage VDC	Flyback topology	200	800	1000	V
Switching frequency	Flyback topology			31.6	kHz
Duty cycle	Flyback topology	5.50		28.9	%
Np:Ns			12.5		
Rdc	Primary-side		1.50		Ω
Rdc	Secondary-side		17.3		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 3 to pin 7, with pins 1 - 3 shorted and pins 7 - 12 shorted at 25 °C			52.0	pF
Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 3, with all other windings open at 25 °C		1480		µH
Part-to-part tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.			22.0	µH

Table 5 – Transformer (T201) Electrical Specifications.

7.3 Transformer Build Diagram

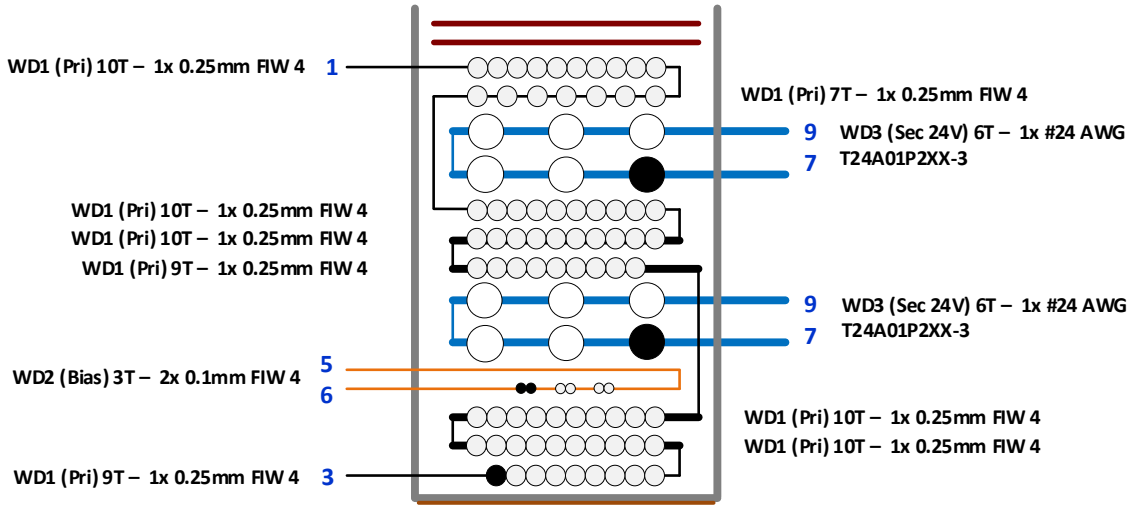


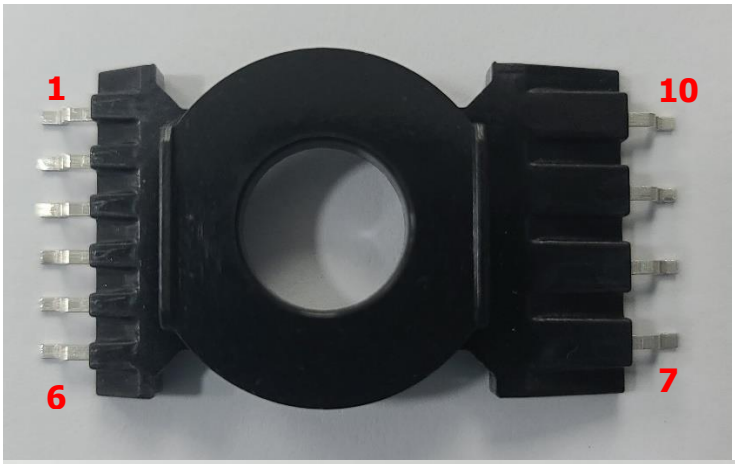
Figure 15 – Transformer Build Diagram.

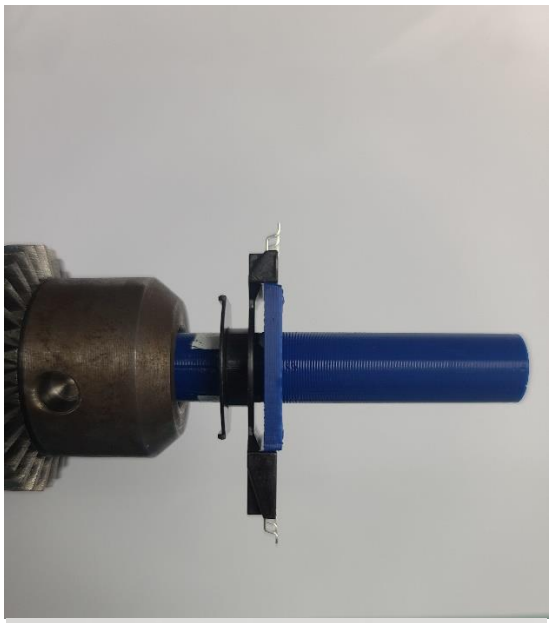
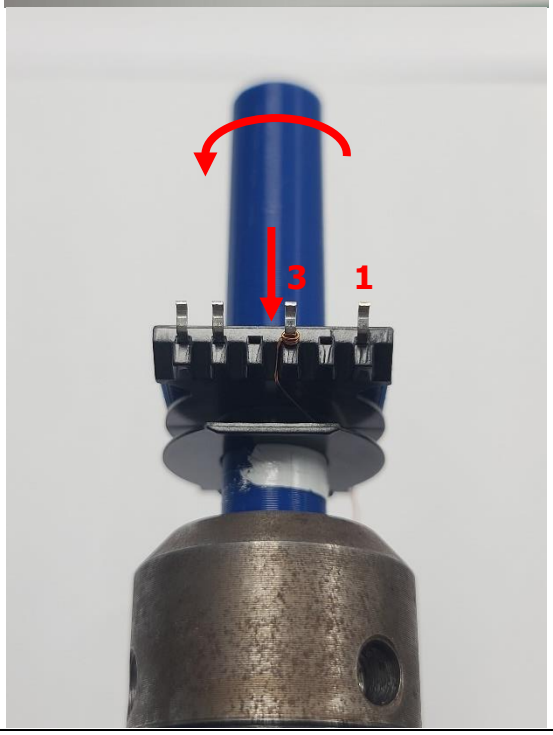
7.4 Material List

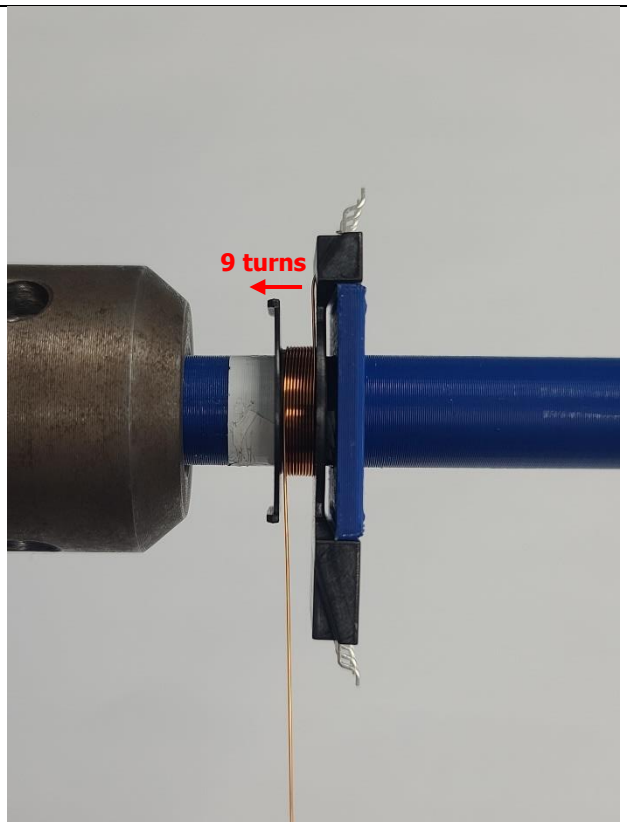
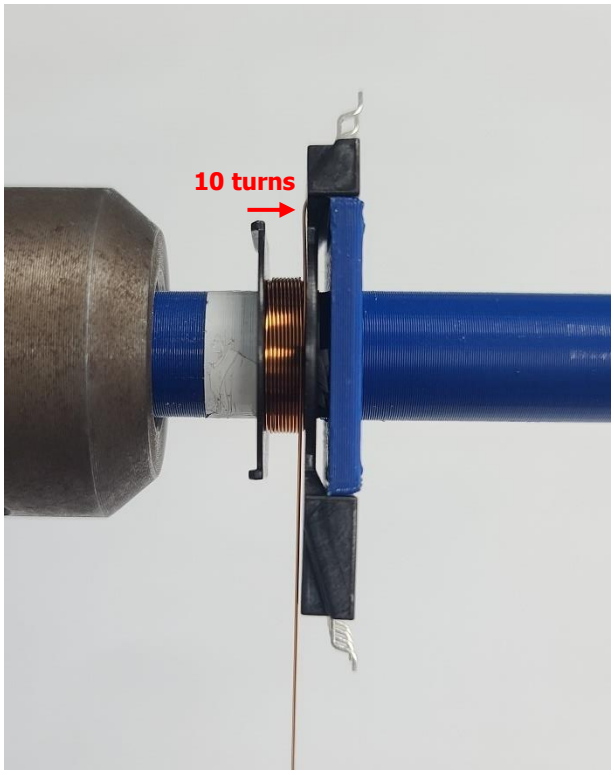
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: MCT-EIQ3001 V4+6P	1	PC	Phenolic	MyCoilTech
[2]	Core: EQ30	1	PC	3C96 (or equivalent)	Ferroxcube
[3]	Core: PLT30/20/3	1	PC	3C96 (or equivalent)	Ferroxcube
[4]	WD1 (Pri): 0.30 mm FIW 4, Class F	4295	mm	Copper Wire	Elektrisola
[5]	WD2 (Bias): 0.20 mm FIW 4, Class F	133	mm		Elektrisola
[6]	WD3 (VOUT): T24A01PXXX-3, AWG 22 PFA .003”		mm		Rubadue
[7]	3M Polyimide Film Tape 5413, width: 0.38 in (9.65 mm)		mm	3M 5413 0.38" X 36YD (or equivalent)	3M

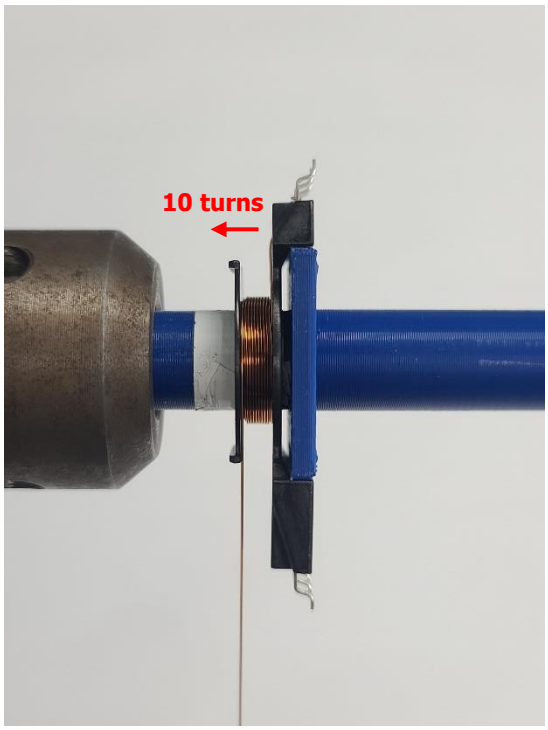
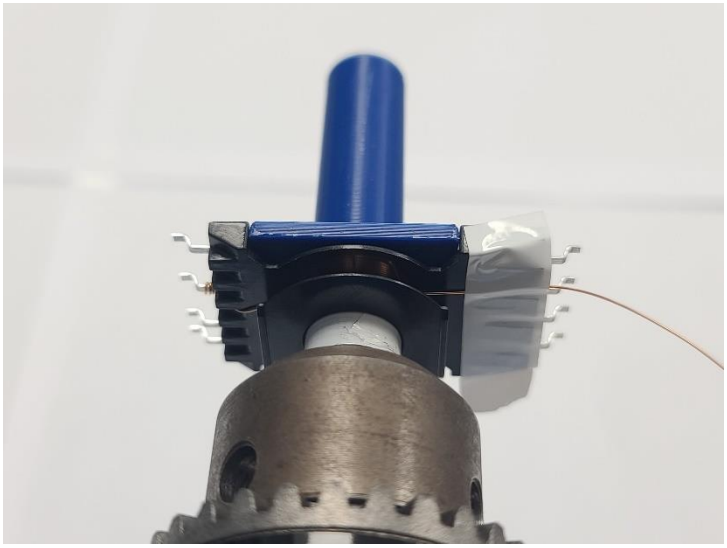
Table 6 – Transformer (T201) Material List.

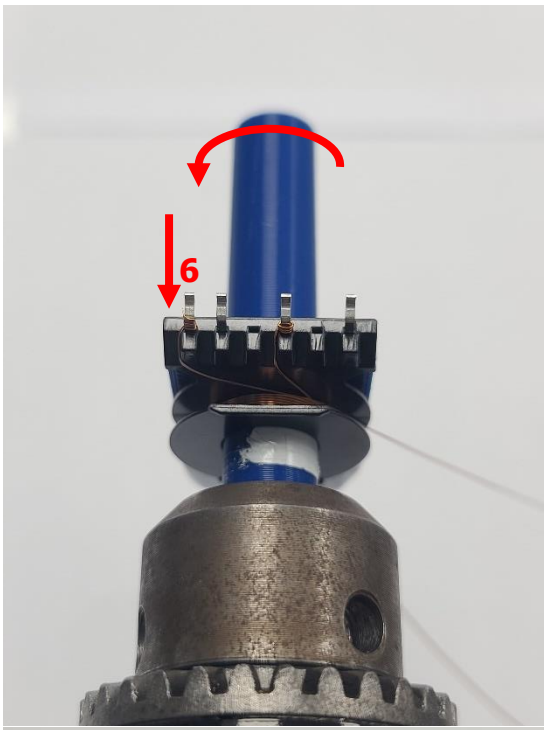
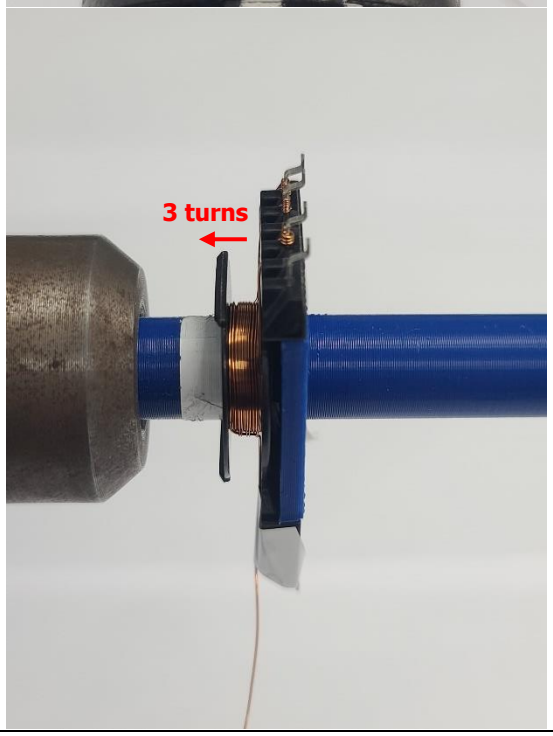
7.5 Winding Instructions

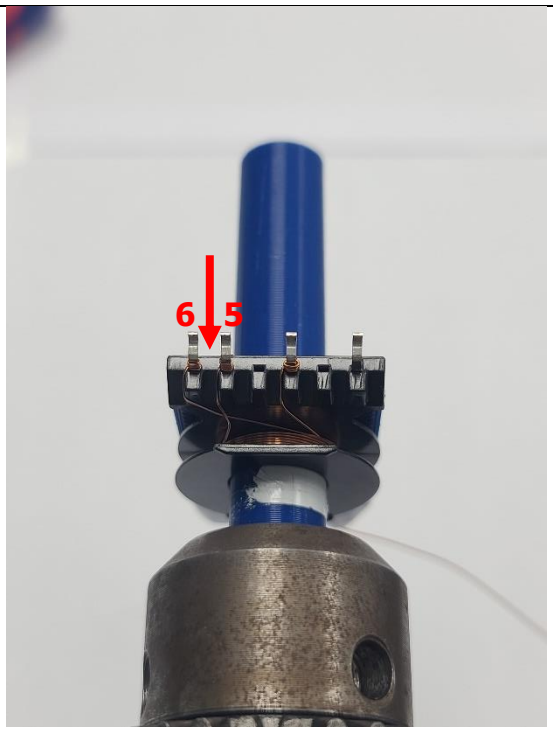
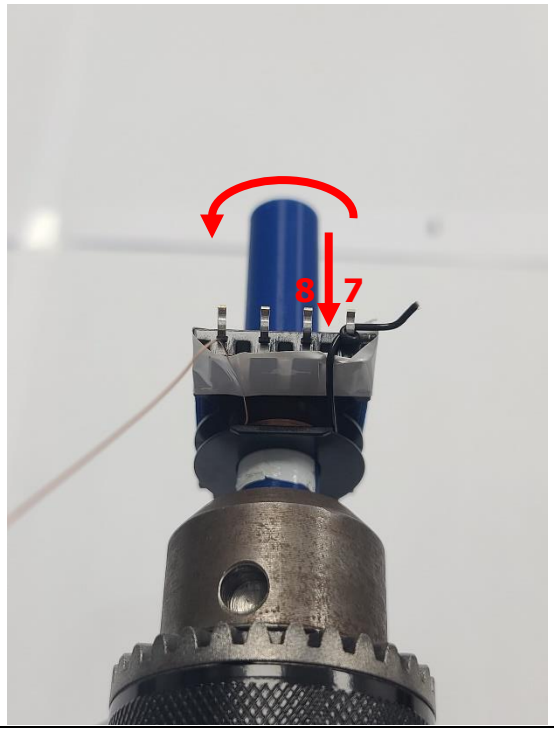
Starting	 	Remove pins 2 and 4.

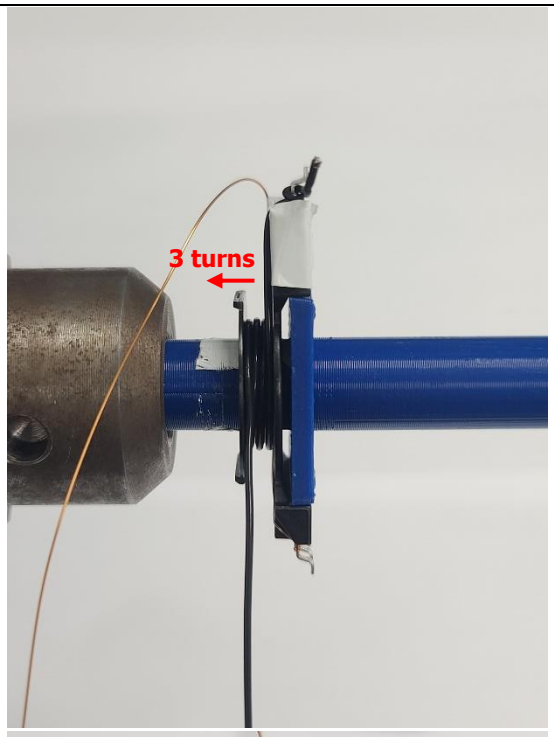
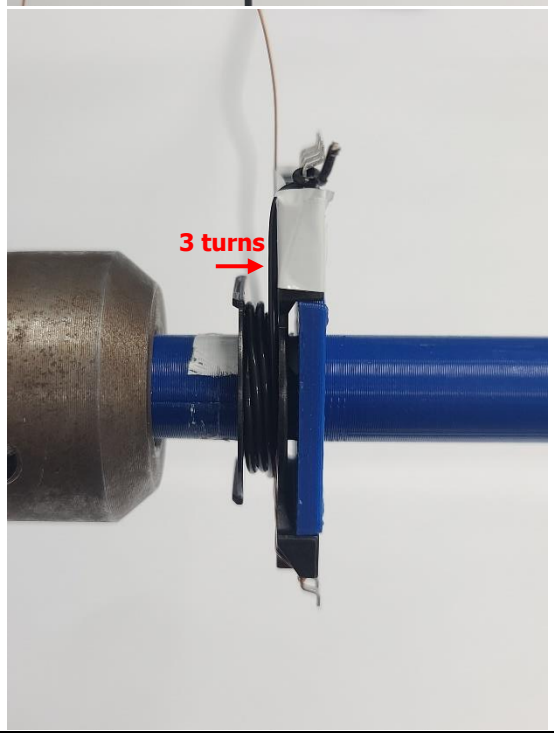
WD1 (Primary)		Place the bobbin on the mandrel.
		Use 0.25 mm FIW4 wire. Start on PIN 3. Route the wire in the slot between PIN 3 and the now removed PIN 4.

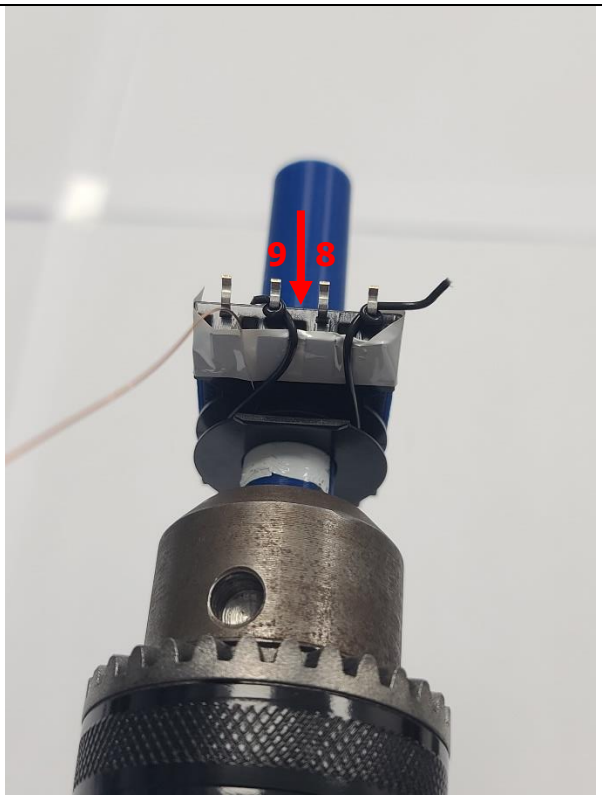
WD1 (Primary)	 	Start the first layer by winding 9 turns in the direction indicated. Begin the second layer by winding 10 turns in the direction indicated.

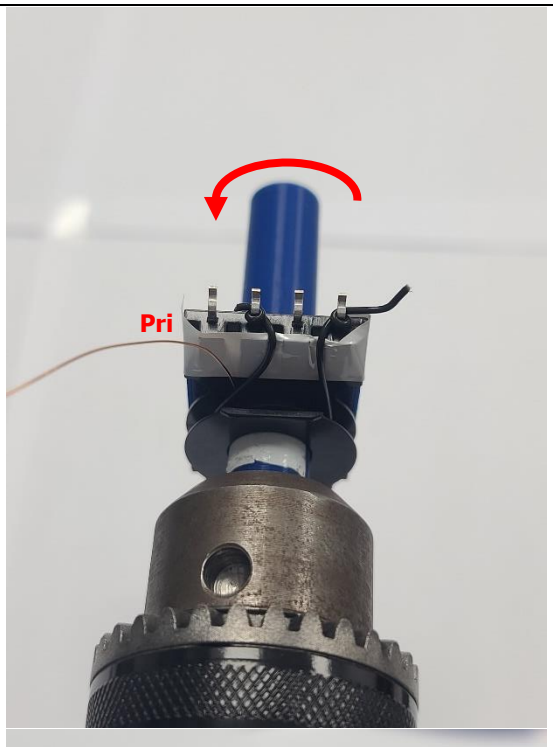
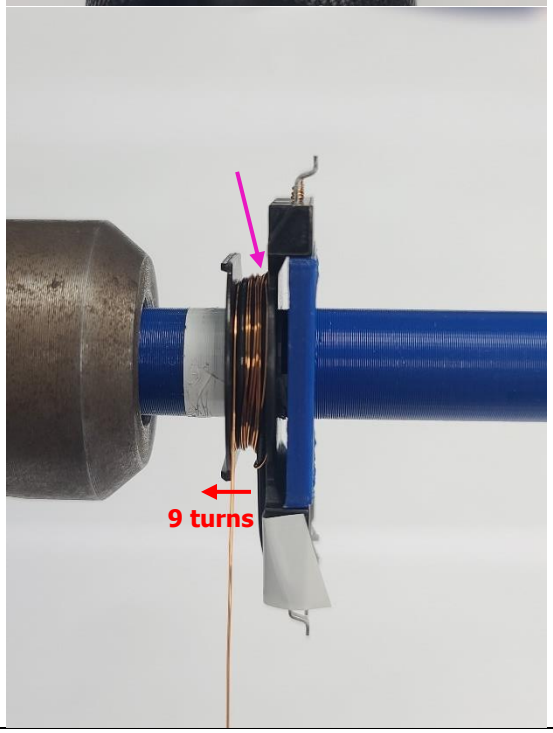
WD1 (Primary)		Finish the third layer by winding 10 turns in the direction indicated.
		Fasten the wire on the right end of the bobbin. Do not terminate yet.

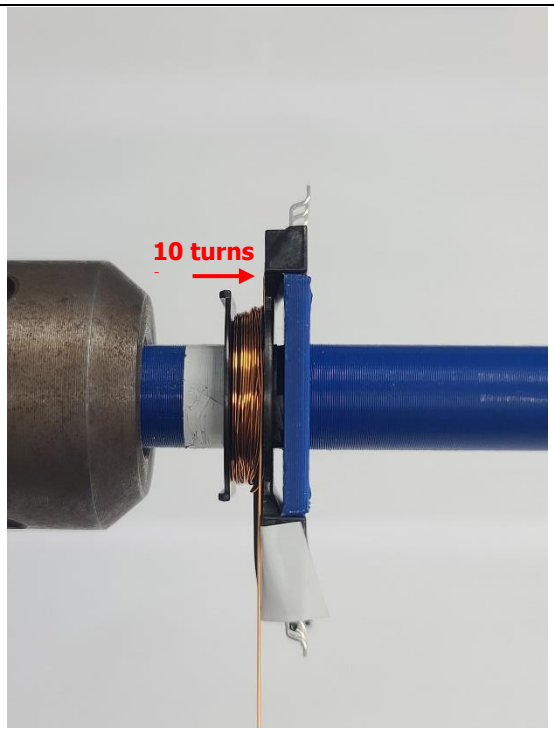
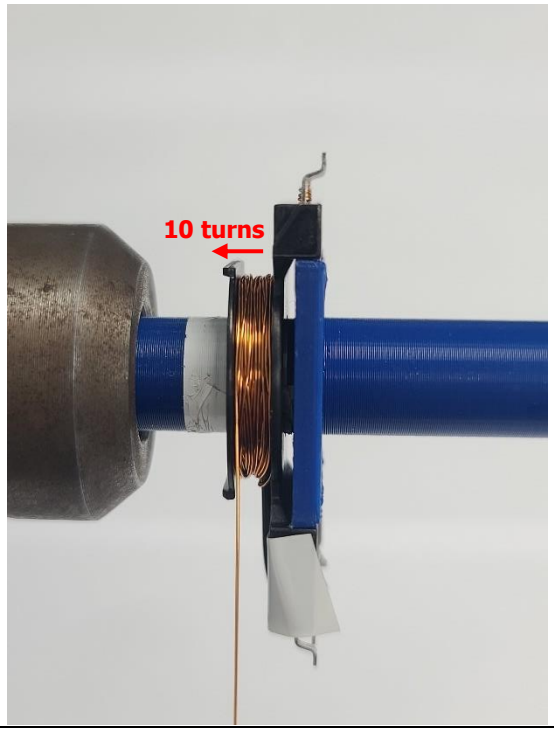
WD2 (Bias)	 	Use 2 x 0.1 mm FIW4 wire. Start on PIN 6. Route the wire on the slot on the left of PIN 6. Wind the 3 turns of the bias winding in the direction indicated. Place the bias wires between the primary winding's third layer wires.

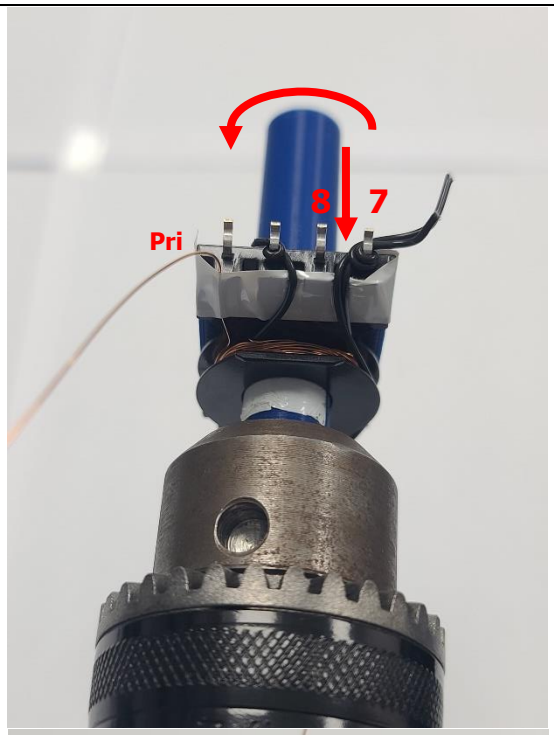
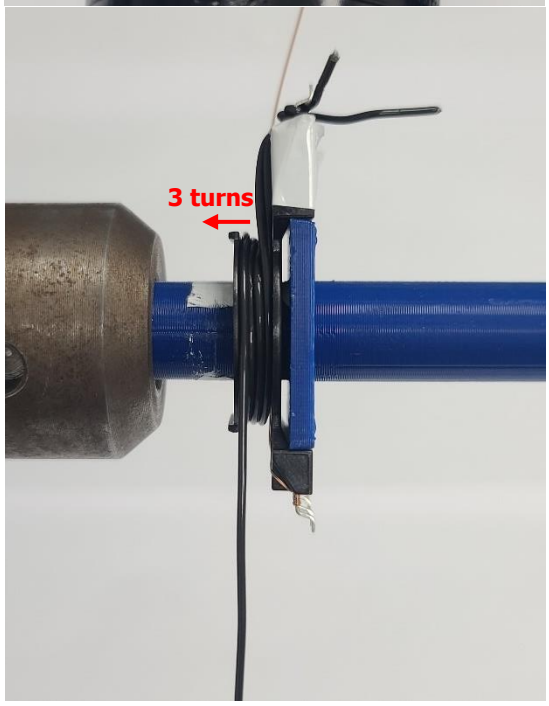
WD2 (Bias)		After three turns, route the wires in the slot between PIN 5 and PIN 6. Terminate the bias winding on PIN 5.
WD3 (Sec 24 V)		Use 1 x #24 AWG T24A01PXXX-3. Start the winding on PIN 7 and route the wire in the slot between PIN 7 and PIN 8.

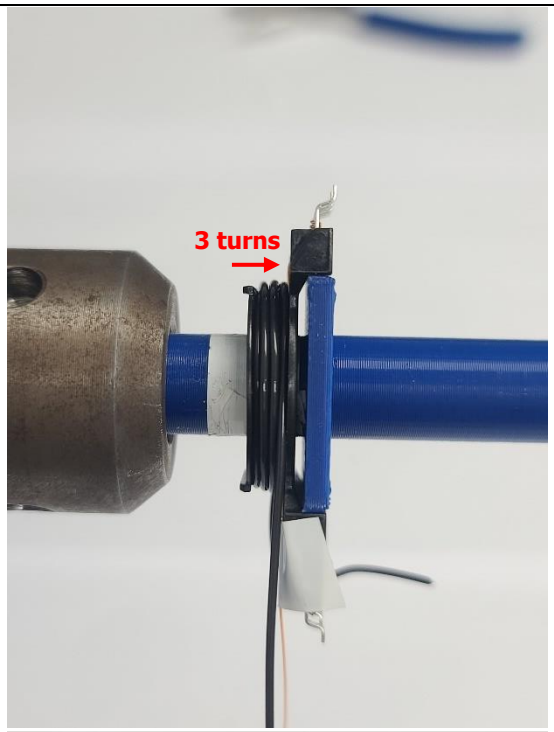
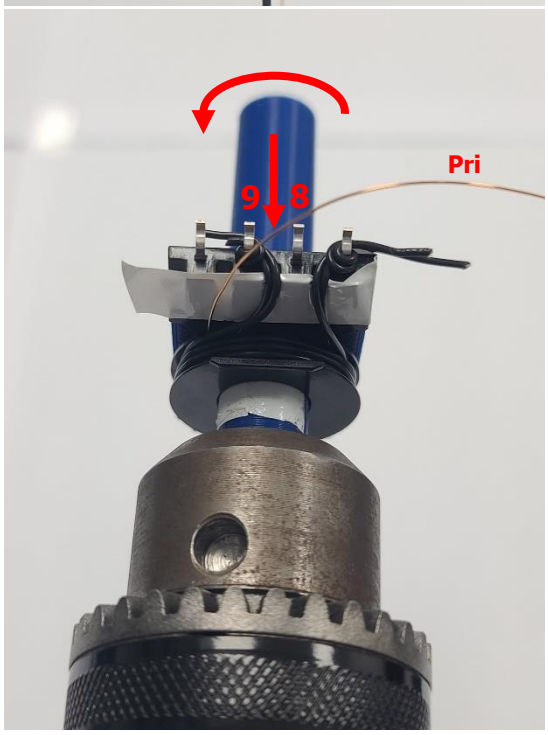
WD3 (Sec 24 V)	 	Begin by winding 3 turns in the direction indicated. Finish by winding the remaining 3 turns.

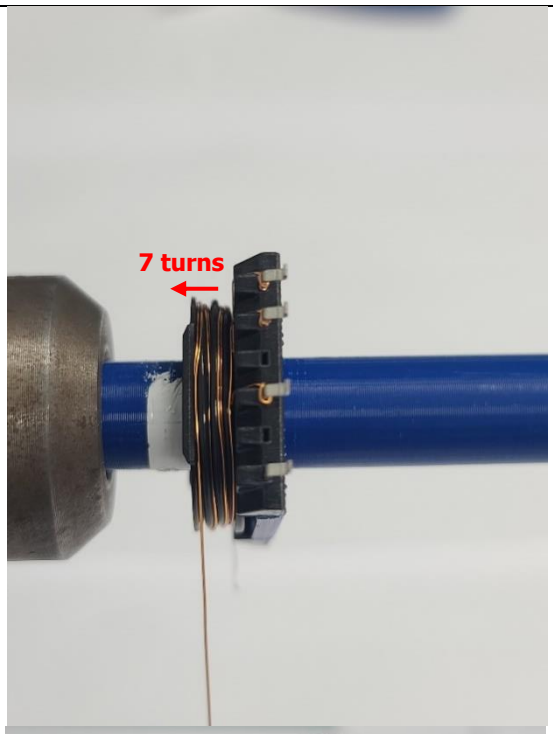
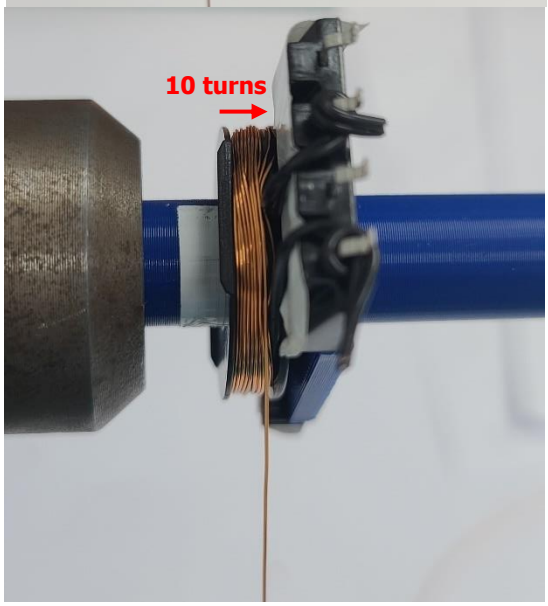
WD3 (Sec 24 V)		Route the wire in the slot between PIN 8 and PIN 9. Terminate the winding on PIN 9.

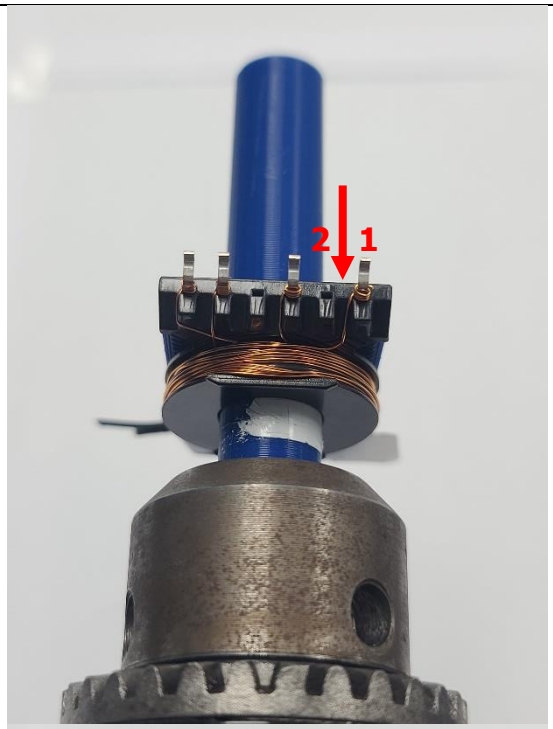
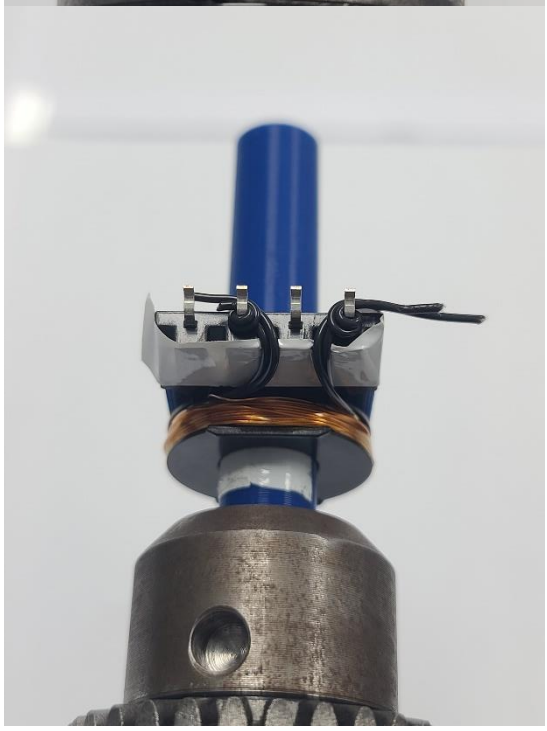
WD1 (Primary)	 	Release the primary winding from the tape, but do not remove the tape from the bobbin. Wind the next 3 turns on the space indicated by the pink arrow. Wind 2 turns on every space between the wires of the secondary winding. This makes a total of 9 turns for the fourth layer.

WD1 (Primary)	 	Continue winding 10 turns on the fifth layer. Finish the sixth layer by winding another 10 turns.

WD3 **(Sec 24 V)**	 	Place the wire under the tape it was removed from. Use 1 x #24 AWG T22A01PXXX-3. Start the winding on PIN 7 and route the wire in the slot between PIN 7 and PIN 8. Begin by winding 3 turns in the direction indicated.

WD3 **(Sec 24 V)**	 	Wind the 3 remaining turns. Route the wire on the slot between PIN 8 and PIN 9. Terminate the winding on PIN 9. Remove the primary winding from the tape.

WD1 (Primary)	 	Wind the next 7 turns in between the wires of the SEC winding. This should be the primary winding's seventh layer. Wind 10 turns on the eighth layer.

WD1 (Primary)	 	Route the wire on the slot between PIN 1 and the removed PIN 2. Terminate the winding on Pin 1. Put two layers of tape to hold the winding in place.

Finishing		Remove the bobbin from the mandrel, then cut and solder the excess wires.
		Mount the gapped core using glue (a 0.375” polyester film electrical tape can be used as an alternative).

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	24.00		24.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	1.500		1.500	A	Output current 1
7	POUT1			36.00	W	
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	200.00		200.00	V	Input DC voltage 2
13	IOUT2	1.500		1.500	A	Output current 2
14	POUT2			36.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	**PRIMARY CONTROLLER SELECTION**					
70	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
71	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X7		Device selection
73	DEVICE_CODE	INN3947FQ		INN3947FQ		Device code
74	PDEVICE_MAX			50	W	Device maximum power capability
75	RDSON_25DEG			1.53	Ω	Primary switch on-time resistance at 25°C
76	RDSON_125DEG			3.12	Ω	Primary switch on-time resistance at 125°C
77	ILIMIT_MIN			1.674	A	Primary switch minimum current limit
78	ILIMIT_TYP			1.800	A	Primary switch typical current limit
79	ILIMIT_MAX			1.926	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.61	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1330	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	31600		31600	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	300.0		300.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			3.468		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation

90	DUTYCYCLE			0.303		Primary switch duty cycle
91	TIME_ON_MIN			1.87	µs	Minimum primary switch on-time
92	TIME_ON_MAX			10.89	µs	Maximum primary switch on-time
93	TIME_OFF			22.28	µs	Primary switch off-time
94	LPRIMARY_MIN			1406.2	µH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			1480.2	µH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			1554.2	µH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			0.196	A	Primary switch average current
101	IPEAK_PRIMARY			1.432	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.432	A	Primary switch ripple current
104	IRMS_PRIMARY			0.433	A	Primary switch RMS current
108	**TRANSFORMER CONSTRUCTION PARAMETERS**					
109	**CORE SELECTION**					
110	CORE	CUSTOM		CUSTOM		Core selection
111	CORE NAME	EIQ30-3C96		EIQ30-3C96		Core Code
112	AE	108.0		108.0	mm^2	Core cross sectional area
113	LE	36.2		36.2	mm	Core magnetic path length
114	AL	6000		6000	nH	Ungapped core effective inductance per turns squared
115	VE	3910		3910	mm^3	Core volume
116	BOBBIN NAME	EIQ30-3C96		EIQ30-3C96		Bobbin name
117	AW	22.3		22.3	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW	3.60		3.60	mm	Bobbin width
119	BH			4.70	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
122	**PRIMARY WINDING**					
123	NPRIMARY			75		Primary winding number of turns
124	BPEAK			3782	Gauss	Peak flux density
125	BMAX			2681	Gauss	Maximum flux density
126	BAC			1341	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			263	nH	Typical gapped core effective inductance per turns squared
128	LG			0.493	mm	Core gap length
130	**SECONDARY WINDING**					
131	NSECONDARY	6		6		Secondary winding number of turns
133	**BIAS WINDING**					
134	NBIAS			3		Bias winding number of turns

138	**PRIMARY COMPONENTS SELECTION**					
139	**LINE UNDERVOLTAGE/OVERVOLTAGE[7]**					
140	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
141	**UNDERVOLTAGE PARAMETERS**					
142	BROWN-IN REQUIRED	30.00		30.00	V	Required DC bus brown-in voltage threshold
143	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
144	VZ			9.10	V	Zener diode reverse voltage
145	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
146	ILKG			2.00	μA	Zener diode maximum reverse leakage current
147	BROWN-IN ACTUAL			22.99 - 29.55	V	Actual brown-in voltage range using standard resistors
148	BROWN-OUT ACTUAL			19.76 - 26.44	V	Actual brown-out voltage range using standard resistors
149	**OVERVOLTAGE PARAMETERS**					
150	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
151	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
152	VF				V	OV diode forward voltage
153	VRRM				V	OV diode reverse voltage
154	PIV				V	OV diode peak inverse voltage
155	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
156	**DC BUS SENSE RESISTORS**					
157	RLS_H			0.70	MΩ	Connect five 140 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
158	RLS_L			261	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
161	**BIAS WINDING**					
162	VBIAS	9.00		9.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			49.00	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	μF	Bias winding rectification capacitor
166	CBPP			4.70	μF	BPP pin capacitor
170	**SECONDARY COMPONENTS SELECTION**					
171	**FEEDBACK COMPONENTS**					
172	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
173	RFB_LOWER			5.62	kΩ	Lower feedback resistor
174	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
178	**MULTIPLE OUTPUT PARAMETERS**					
179	**OUTPUT 1**					
180	VOUT1			24.00	V	Output 1 voltage
181	IOUT1	1.500		1.500	A	Output 1 current

[7] Input UV and OV is not applicable for this design.

182	POUT1			36.00	W	Output 1 power
183	IRMS_SECONDARY1			4.414	A	Root mean squared value of the secondary current for output 1
184	IRIPPLE_CAP_OUTPUT1			4.151	A	Current ripple on the secondary waveform for output 1
185	NSECONDARY1			6		Number of turns for output 1
186	VREVERSE_RECTIFIER1			104.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
187	SRFET1	DMT15H017LPS-13		DMT15H017LPS-13[8]		Secondary rectifier (Logic MOSFET) for output 1
188	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
189	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
190	RDSON_SRFET1			26	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
218	PO_TOTAL			36.00	W	Total power of all outputs
223	**INPUT VOLTAGE SET-POINTS ANALYSIS**					
224	**TOLERANCE CORNER**					
225	USER_VINDC	800		800	V	Input DC voltage corner to be evaluated
226	USER_ILIMIT	TYP		1.800	A	Current limit corner to be evaluated
227	USER_LPRIMARY	TYP		1480.2	µH	Primary inductance corner to be evaluated
229	**OPERATING CONDITION SELECTION**					
230	POUT	35.00		35.00	W	Output power to be evaluated
231	EFFICIENCY			0.85		Converter efficiency to be evaluated
232	Z FACTOR			0.50		Z-factor to be evaluated
233	FSWITCHING			27956	Hz	Maximum switching frequency at the output power to be evaluated
234	KP			4.968		Measure of continuous/discontinuous mode of operation
235	MODE_OPERATION			DCM		Mode of operation
236	DUTYCYCLE			0.070		Primary switch duty cycle
237	TIME_ON			2.511	µs	Primary switch on-time
238	TIME_OFF			33.260	µs	Primary switch off-time
240	**PRIMARY CURRENT**					
241	IAVG_PRIMARY			0.048	A	Primary switch average current
242	IPEAK_PRIMARY			1.357	A	Primary switch peak current
243	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
244	IRIPPLE_PRIMARY			1.357	A	Primary switch ripple current
245	IRMS_PRIMARY			0.208	A	Primary switch RMS current
247	**MAGNETIC FLUX DENSITY**					
248	BPEAK			3367	Gauss	Peak flux density
249	BMAX			2479	Gauss	Maximum flux density
250	BAC			1240	Gauss	AC flux density (0.5 x Peak to Peak)

Table 7 – RDR-994Q PIXls Spreadsheet.

[8] The AEC-Q qualified version of the SR FET (MFR Part Number: DMTH15H017LPSWQ) was used for the design.

9 Performance data

Note: 1. Measurements were taken with the unit under test positioned inside a thermal chamber in a high-voltage (HV) safety room.

Figure 16 – Set-up for High-Voltage Test.

Figure 17 – Set-up for Test Inside the High-Voltage Room.

2. The RDR-994Q board was placed inside a box within the thermal chamber to eliminate the effects of airflow.

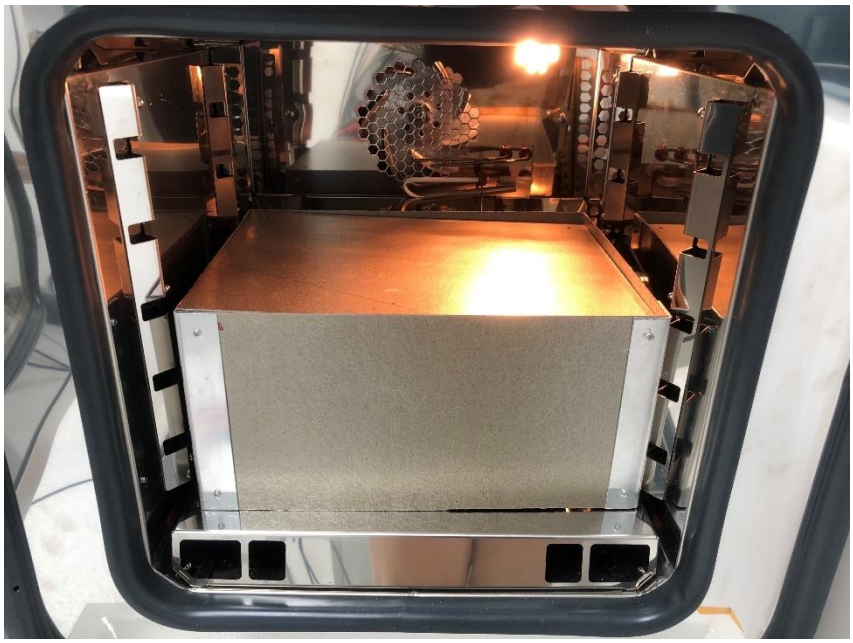


Figure 18 – Unit under test placed inside a box to eliminate the effect of airflow.

3. The RDR board was allowed to settle for 5 minutes at full load at the start of each test sequence. The board was allowed to stabilize for at least 1 minute before measurements were taken at each load conditon.

9.1 No-Load Input Power

F shows the schematic diagram for no-load input power measurement. The voltmeter is placed before the ammeter; this is done to prevent the voltmeter bias current from affecting the input current measurement. A Chroma Digital Power Meter 66205 was used to measure both the current and voltage.

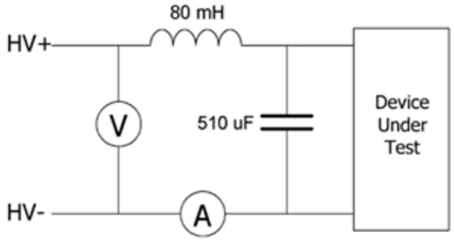


Figure 19 – No-Load Input Power Measurement Diagram.

The unit was soaked for ten minutes for every change in input voltage before starting data averaging. The leakage current of the DC-Link capacitor was also measured before testing and was subtracted from the no-load input current measurement. The average voltage across the inductor is assumed to be negligible due to the inductor's very low DCR (40m ohms) and average input current. AC losses in the inductor are also assumed to be negligible since the input current is expected to be DC.

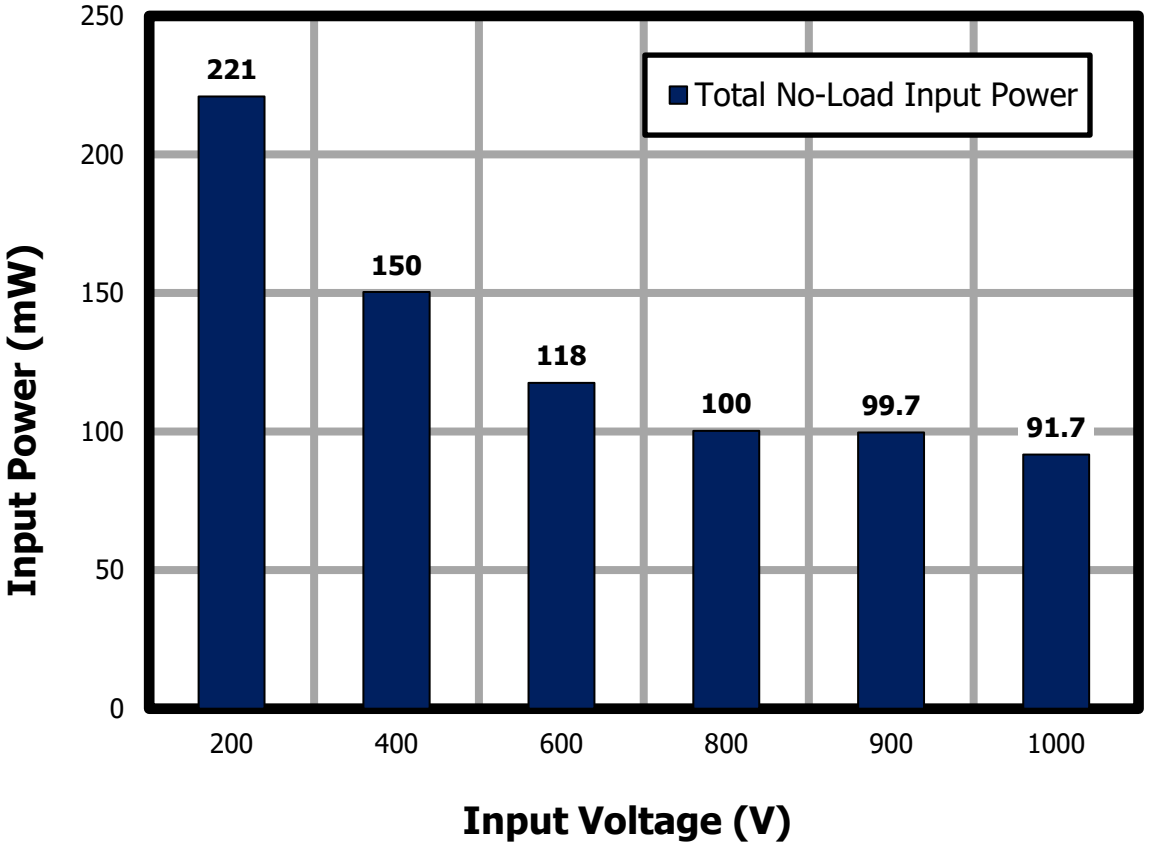


Figure 20 – No-Load Input Power vs. Input Voltage (25 C Ambient).

9.2 Efficiency

9.2.1 Efficiency Across Line

Efficiency across line describes how input voltage affects the unit's overall efficiency. The points in the graph were taken at 100% load conditions. 100% load was 1.46 A output current.

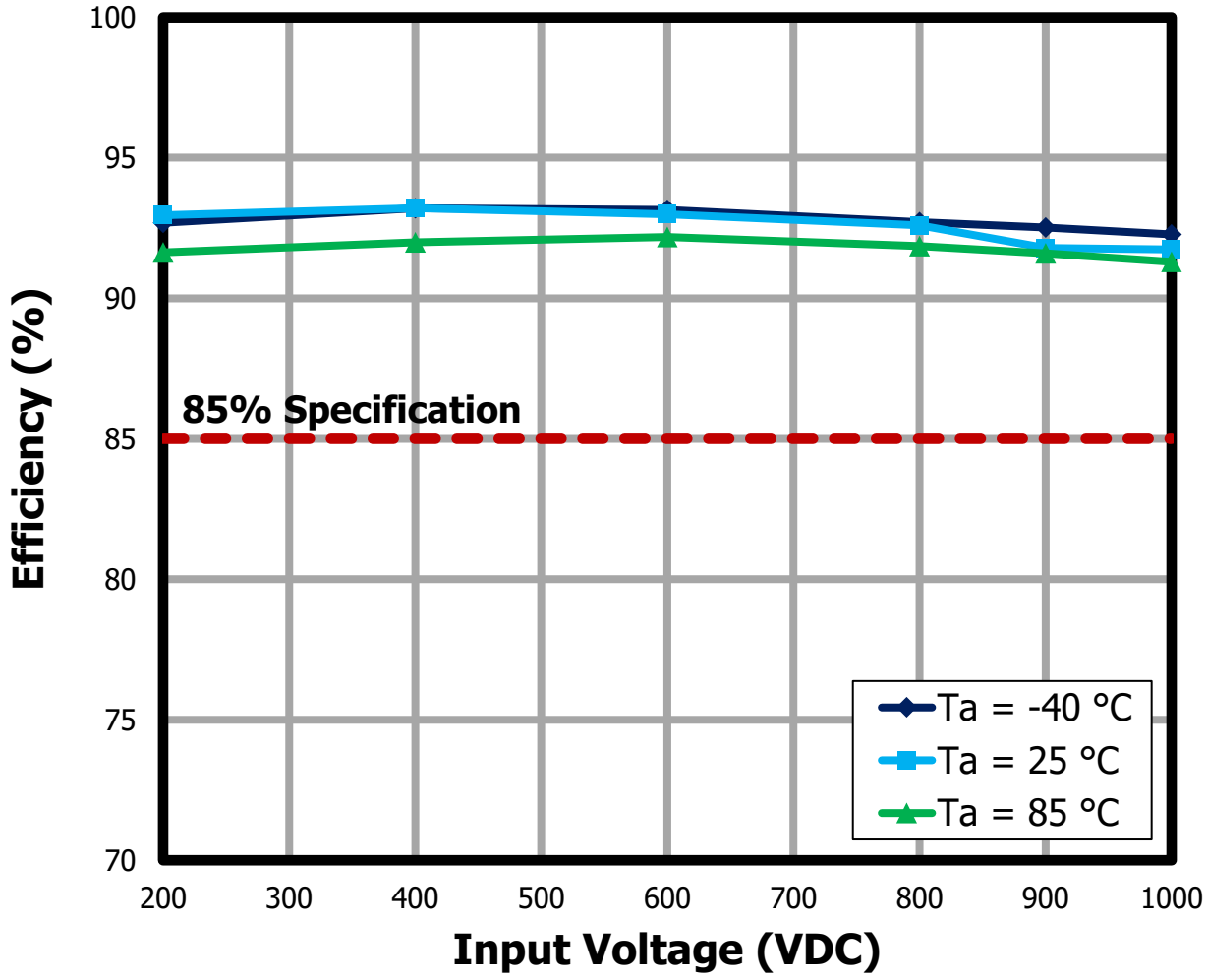


Figure 21 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Efficiency Across Load

Efficiency across load describes how the change in output loading conditions affects the unit's overall efficiency.

9.2.2.1 Efficiency Across Load at 85 °C Ambient

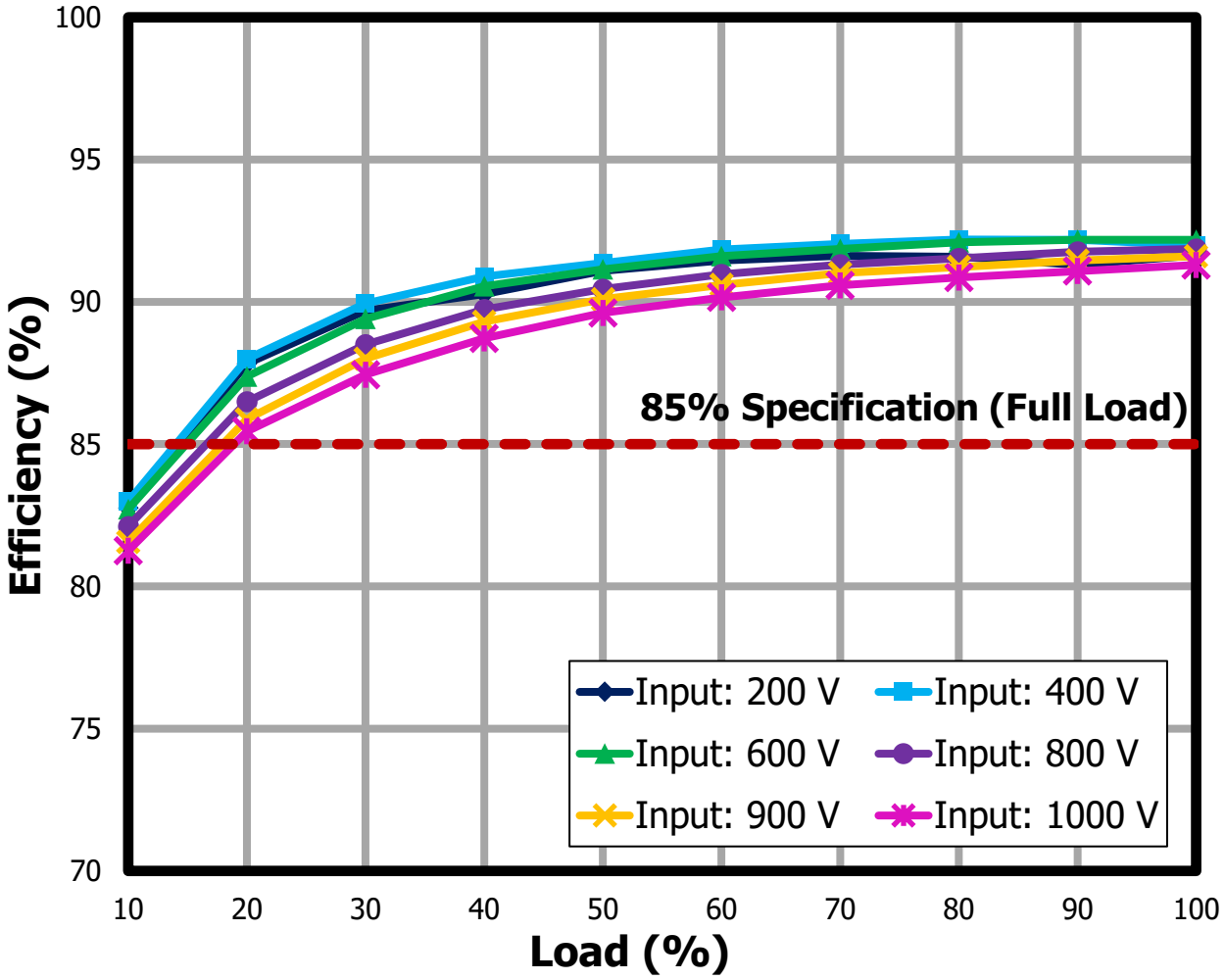


Figure 22 – Efficiency vs. Load across Input Voltage (85 °C Ambient).

9.2.2.2 Efficiency Across Load at 25 °C Ambient

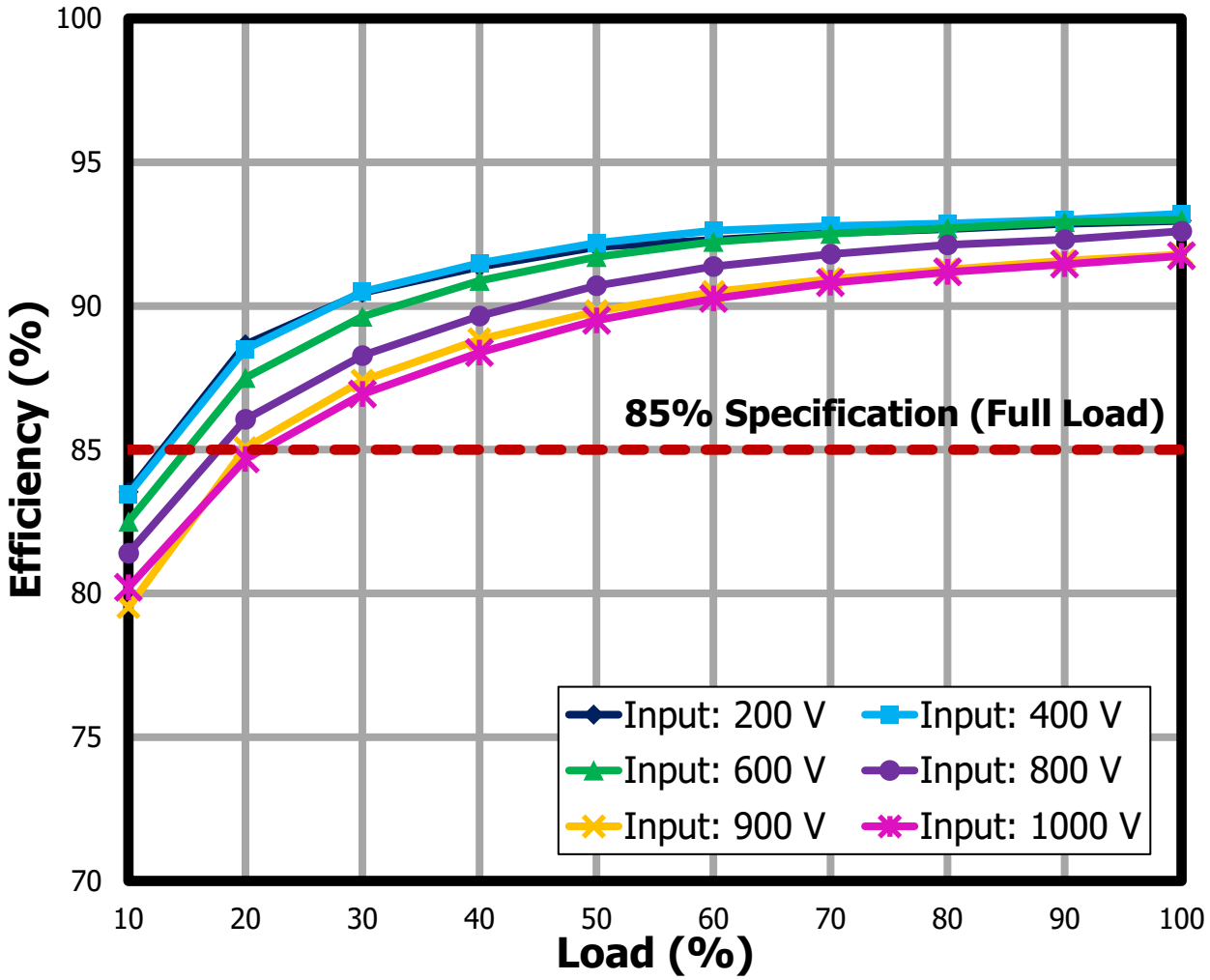


Figure 23 – Efficiency vs. Load across Input Voltage (25 °C Ambient).

9.2.2.3 Efficiency Across Load at -40 °C Ambient

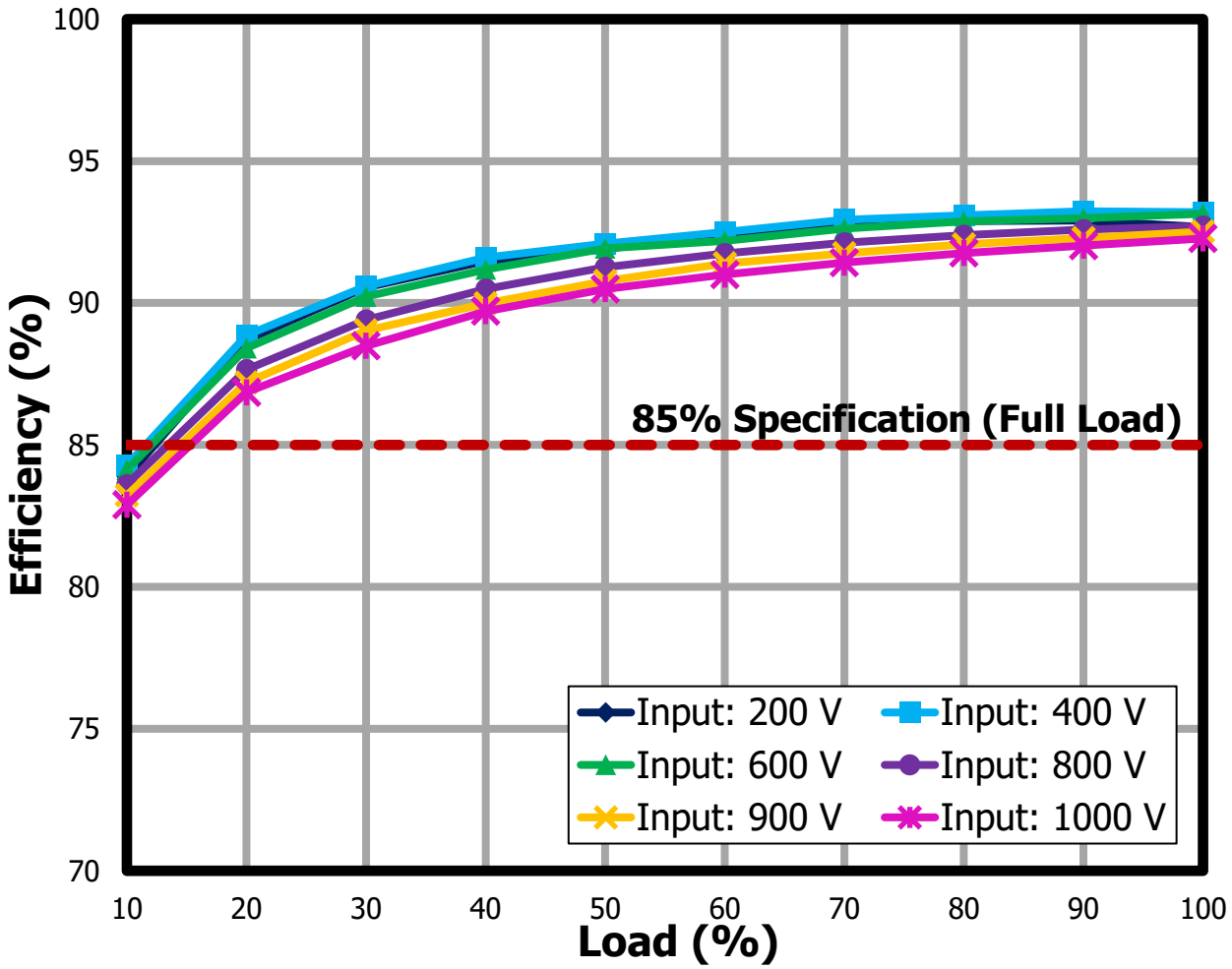


Figure 24 – Efficiency vs. Load across Input Voltage (-40 °C Ambient).

9.2.2.4 Efficiency Across Load at 105 °C Ambient

At 105 °C ambient, output power is derated to 20 W for 200 V ≤ VDC ≤ 800 V, 18 W for 900 V, and 16 W for 1000 V[9].

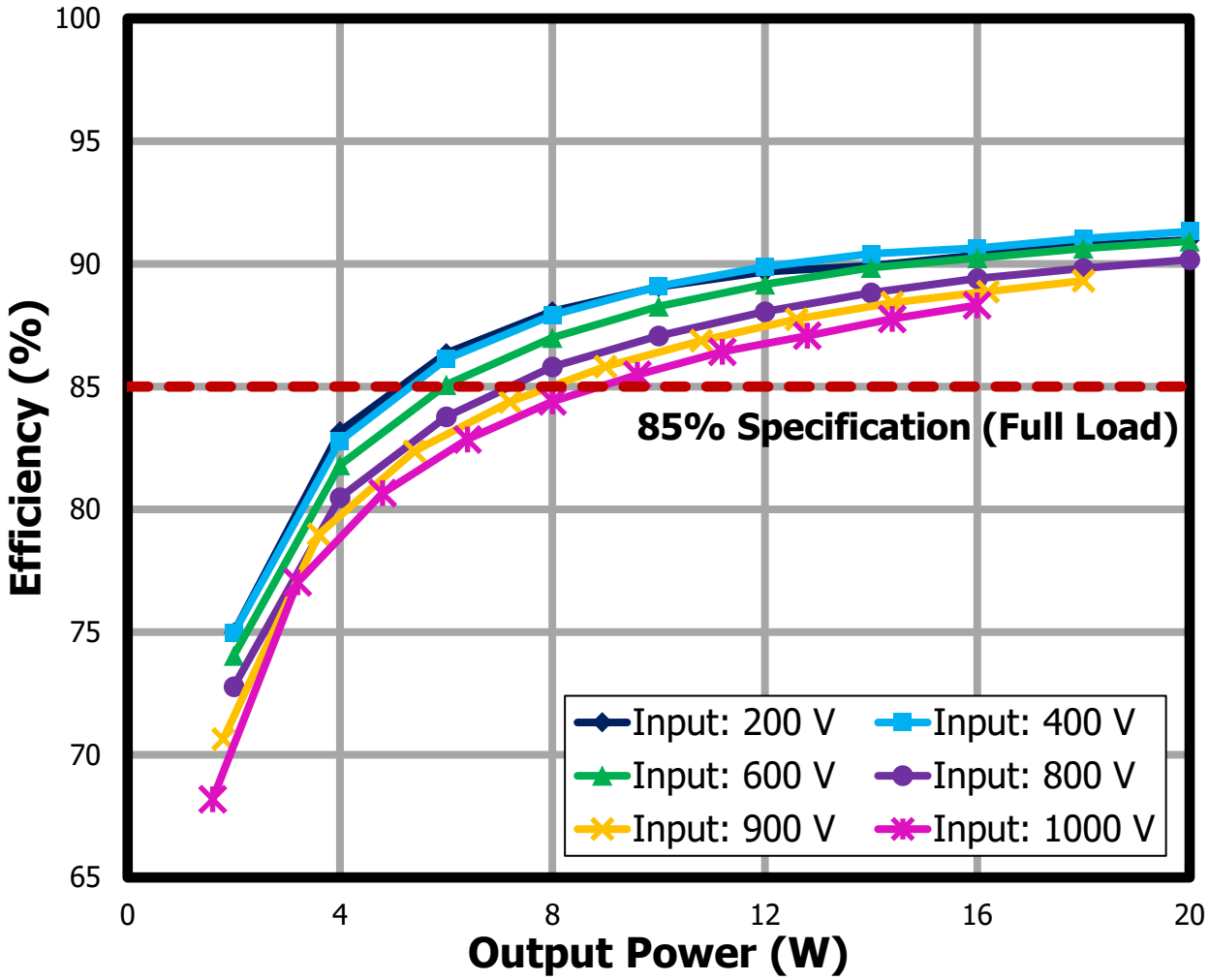


Figure 25 – Efficiency vs. Load at Different Input Voltages (105 °C Ambient).

[9] See Section 13 for power derating curve at 105 °C ambient.

9.3 Line and Load Regulation

9.3.1 Load Regulation

Load regulation describes how the change in load affects output voltage.

9.3.1.1 Load Regulation at 85 °C Ambient

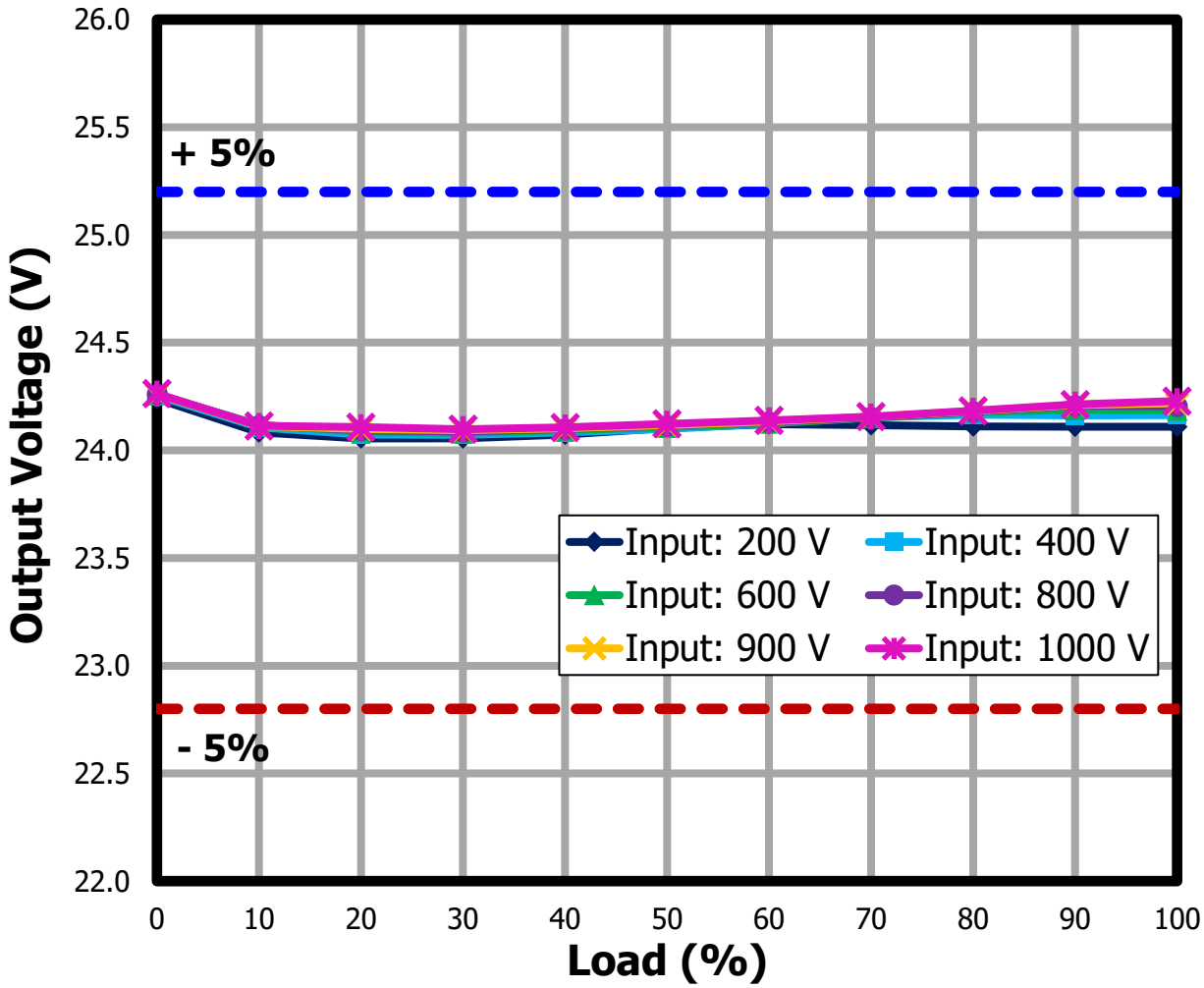


Figure 26 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).

9.3.1.2 Load Regulation at 25 °C Ambient

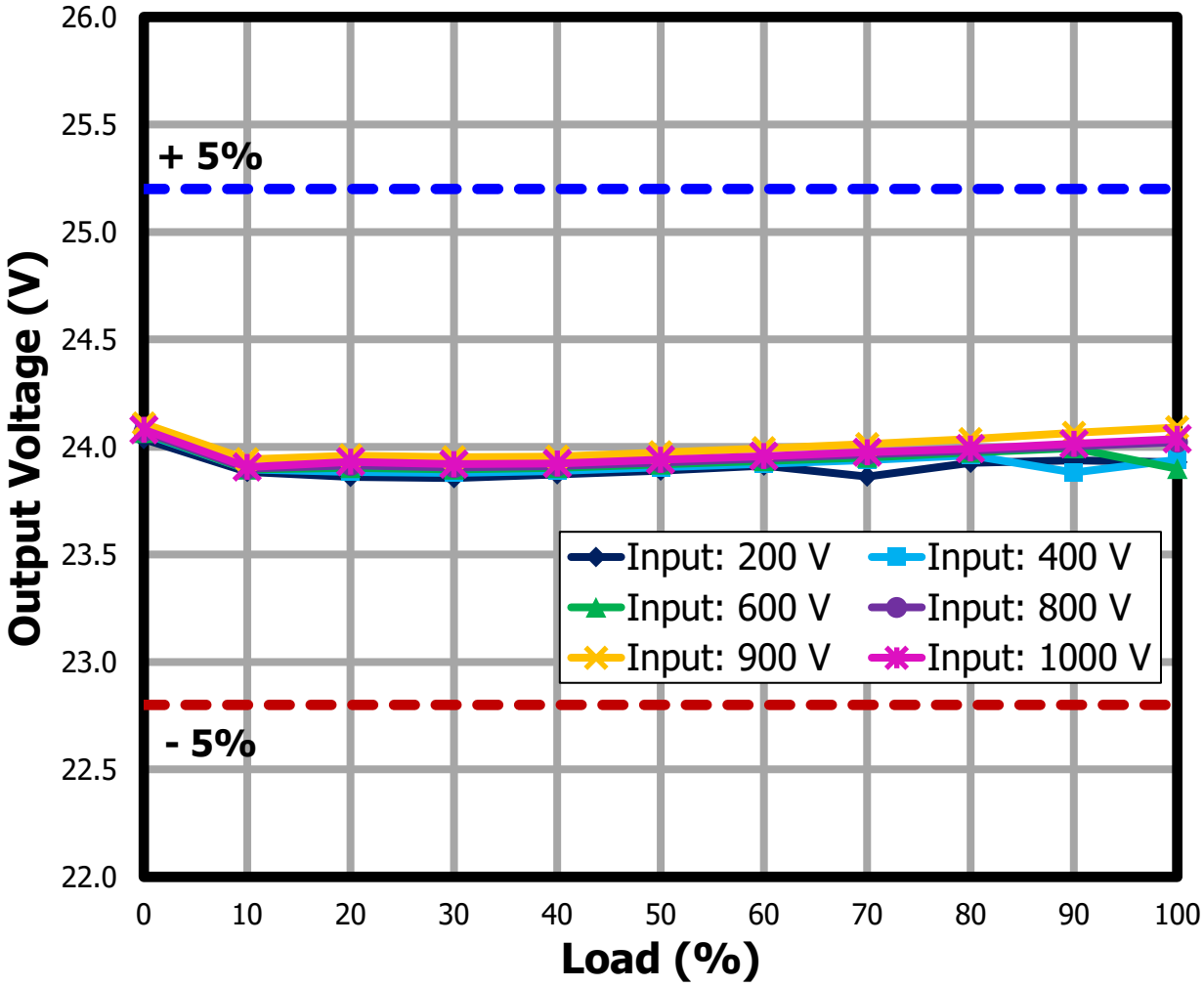


Figure 27 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).

9.3.1.3 Load Regulation at -40 °C Ambient

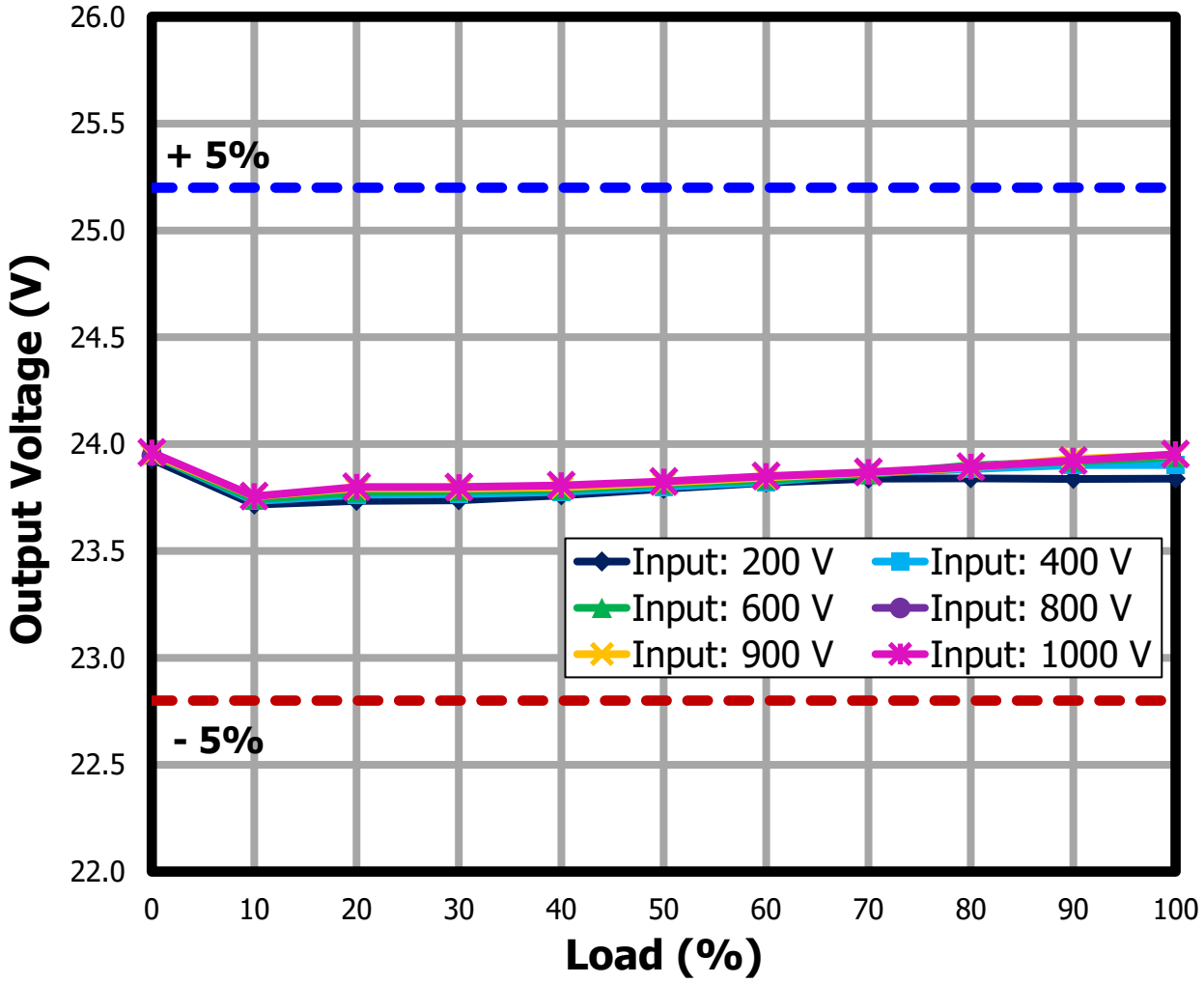


Figure 28 – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).

9.3.1.4 Load Regulation at 105 °C Ambient

At 105 °C ambient, output power is derated to 20 W for 200 V ≤ VDC ≤ 800 V, 18 W for 900 V, and 16 W for 1000 V[10].

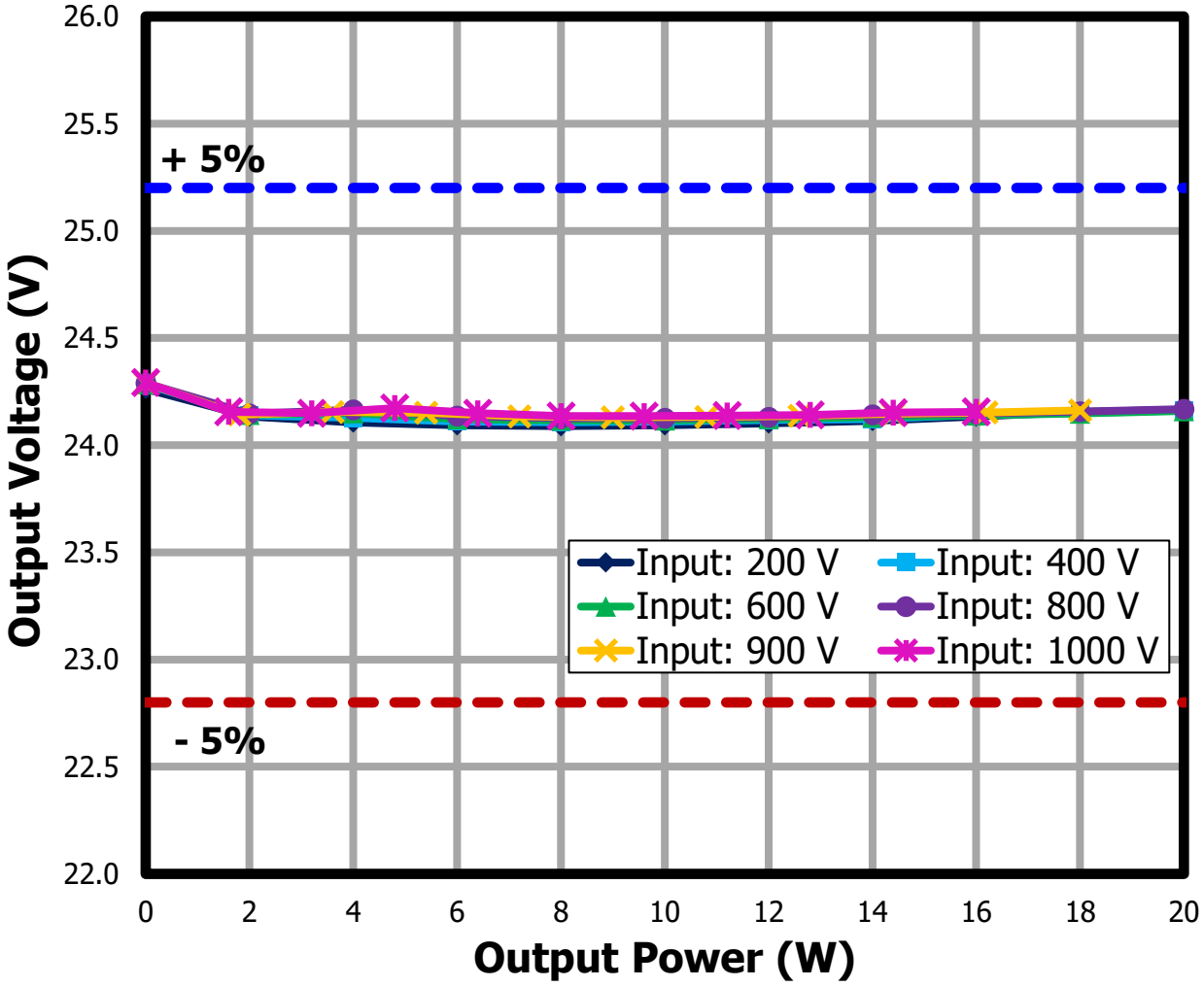


Figure 29 – Output Regulation vs. Load at Different Input Voltages (105 °C Ambient).

[10] See Section 13 for power derating curve at 105 °C ambient.

9.3.2 Line Regulation

Line regulation describes how the change in input voltage affects the output voltage. Tests were performed at full load. 100% load was 1.46 A output current.

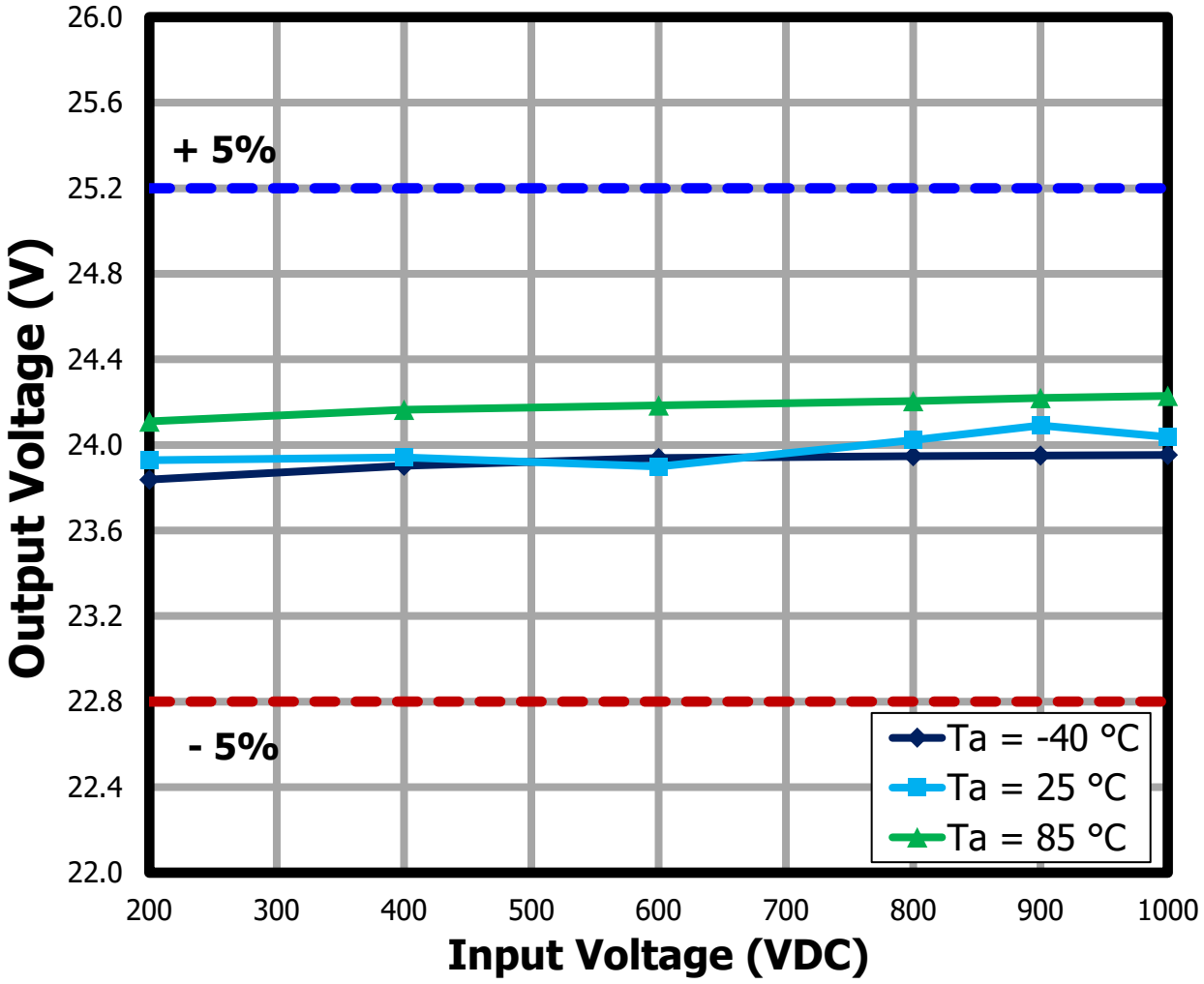


Figure 30 – Output Voltage vs Input Voltage at Full Load (1.46 A).

10 Thermal Performance

10.1 Thermal Data at 85 °C Ambient

The unit was placed inside a thermal chamber, powered up, and allowed to stabilize at 100% load for at least 1 hour prior to testing. The 85 °C ambient setting inside the enclosure increased to 87 °C due to the self-heating effect of the unit. Figure 18 shows the set-up for thermal measurements.

Critical Components	Temperature (°C)				
	200 V	400 V	800 V	900 V	1000 V
INN3947FQ (IC201)	115	109	113	115	118
Primary Snubber Resistor (R307)	113	113	113	114	112
Transformer Winding (T201)	111	107	109	109	111
Transformer Core (T201)	106	104	106	107	108
SR MOSFET (Q101)	100	97.7	98.6	98.9	104
Secondary Snubber Resistor (R104)	98.1	94.5	95.2	95.4	109
Output Capacitor (C104)	95.0	93.1	93.6	93.9	97.1
Current Sense Resistor (R107)	95.0	92.6	92.9	93.1	97.0
Ambient Temperature	87.2	86.4	86.5	86.6	87.3

Table 8 – Thermal Data at 90 °C at Different Input Voltages (V).

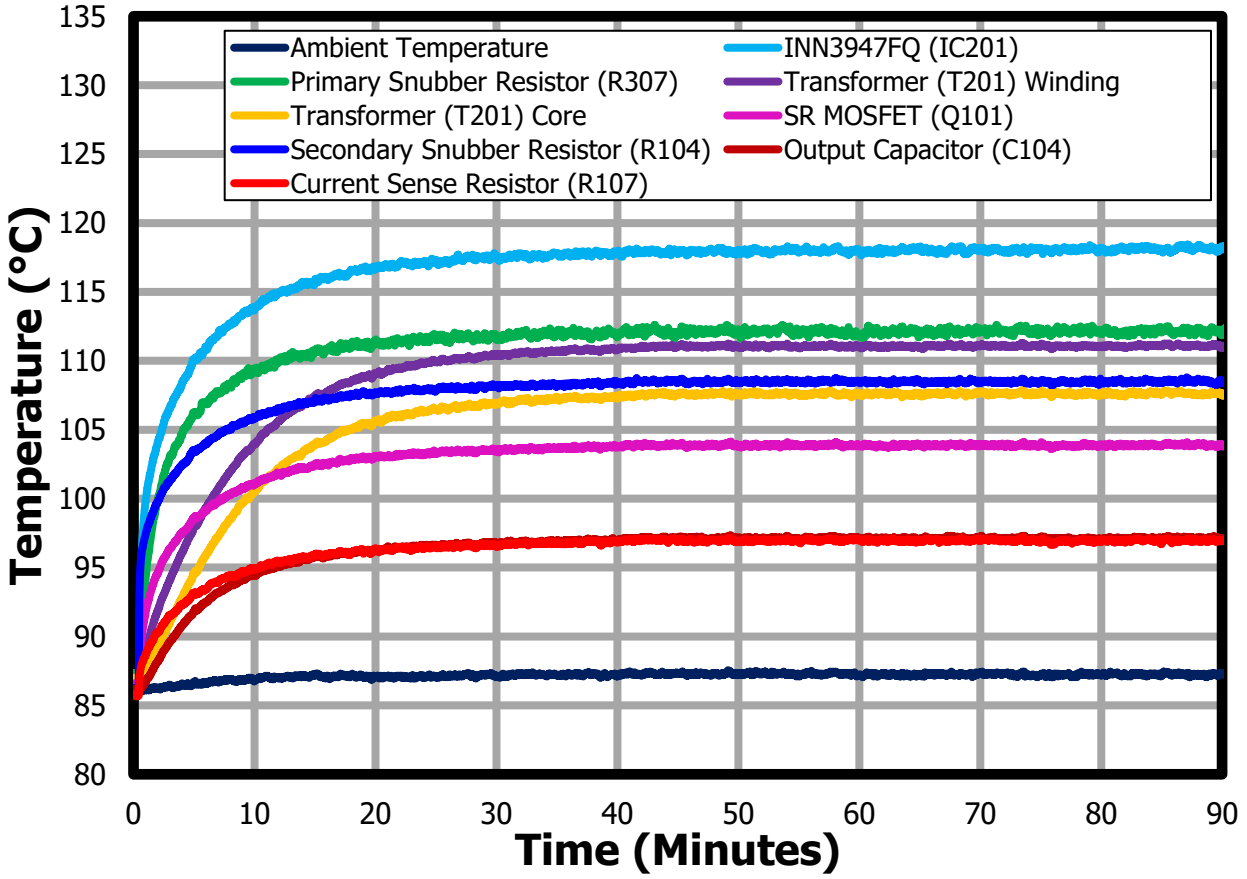


Figure 31 – Component Temperature settling time at 87 °C Inside the Enclosure, 1000 V Input.

10.2 Thermal Image Data at 22 °C Ambient

The following thermal scans were captured using a Fluke thermal imager after allowing the power supply to settle for 1 hour in an enclosure to ensure thermal equilibrium and minimize the effect of airflow.

Critical Components	Temperature (°C)			
	200 V	400 V	900 V	1000 V
INN3947FQ (IC201)	53.2	48.2	54.3	60.4
Primary Snubber Resistors	59.3	56.2	53.2	57.8
Transformer (T201)	50.8	47.6	48.4	50.8
SR MOSFET (Q101)	37.9	37.3	39.7	41.5
Current Sense Resistor (R107)	32.6	33.5	35.7	35.6
Secondary Snubber Resistor	36.7	36.9	48.4	49.6
Output Capacitor (C102)	32.2	32.9	34.7	36.0

Table 9 – Thermal Data at 22 °C at Different Input Voltages (V).

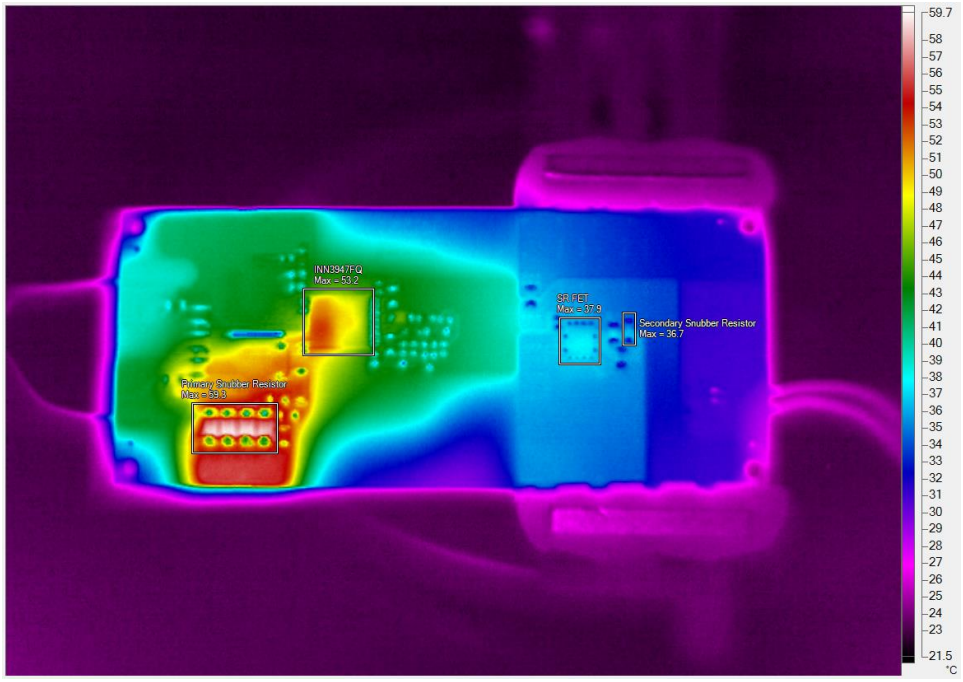


Figure 32 –Thermal Scan of the Bottom of the PCB at 200 V Input.

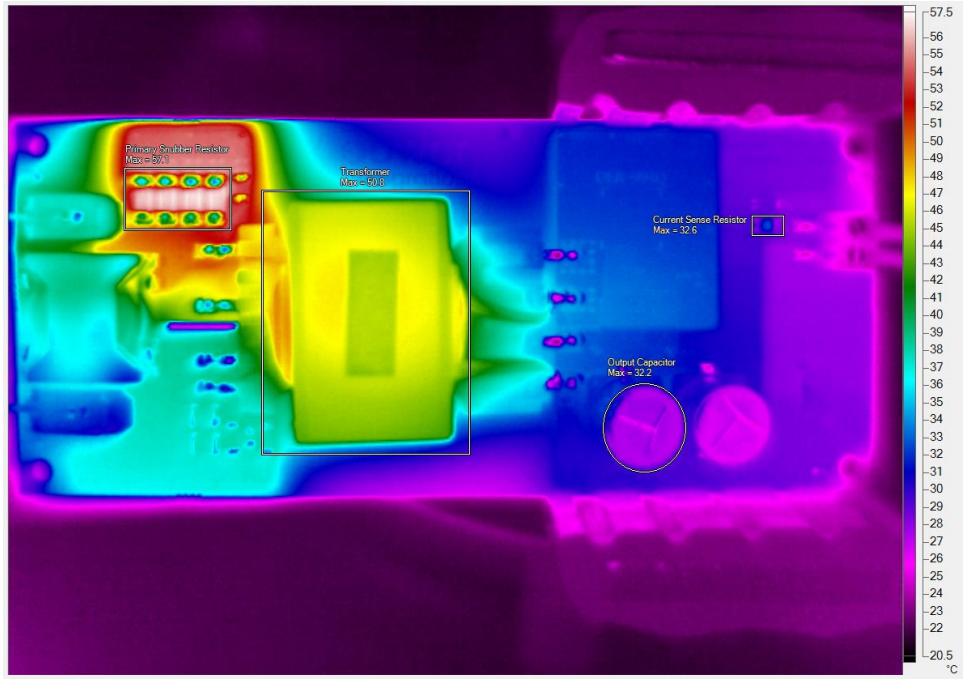


Figure 33 –Thermal Scan of the Top of the PCB at 200 V Input.

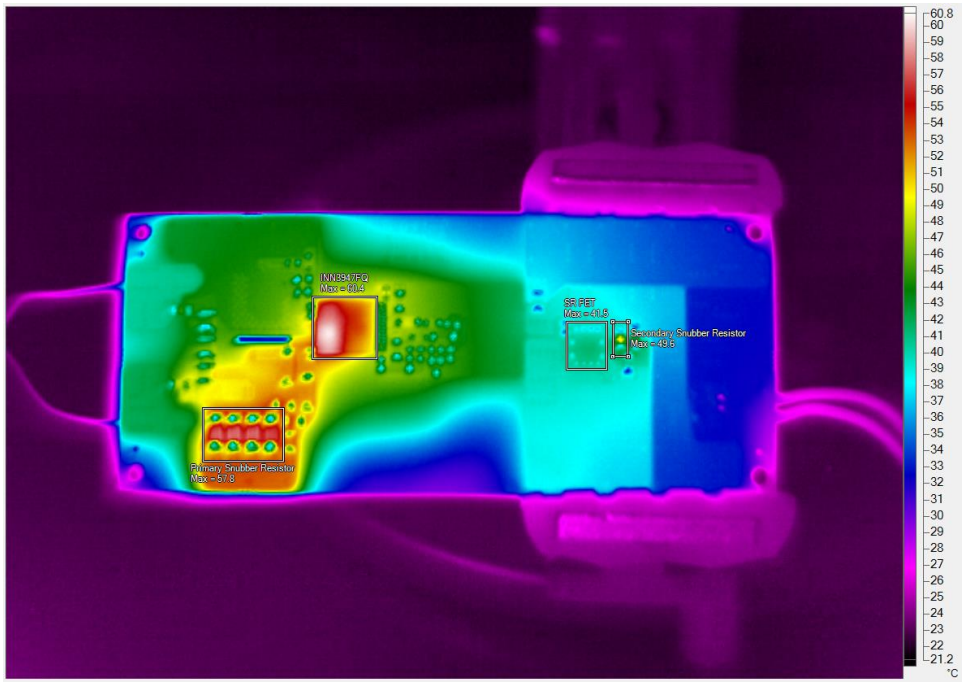


Figure 34 –Thermal Scan of the Bottom of the PCB at 1000 V Input.

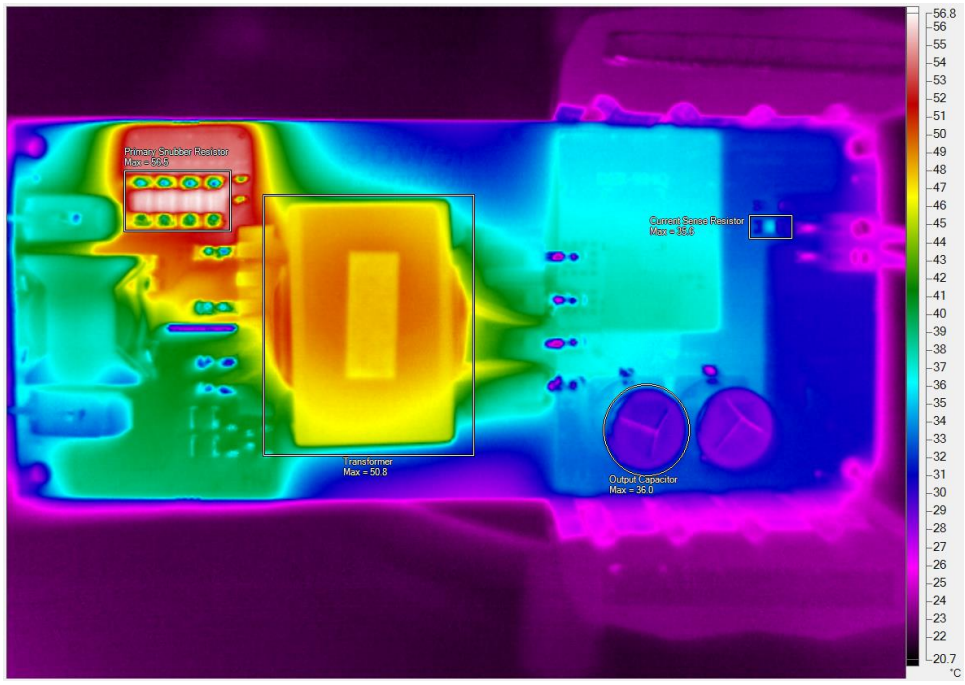


Figure 35 –Thermal Scan of the Top of the PCB at 1000 V Input.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by connecting the unit into a fully charged DC-link capacitor[11] at different input voltages. A constant resistance load configuration was used for all start-up tests.

11.1.1 Output Voltage and Current at 25 °C Ambient[12]

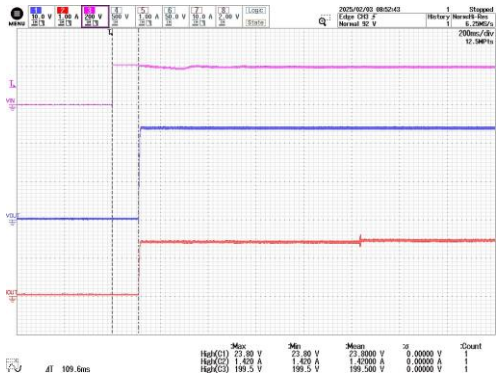


Figure 36 – Output Voltage and Current.
200 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 200 V / div.
Time: 200 ms / div.

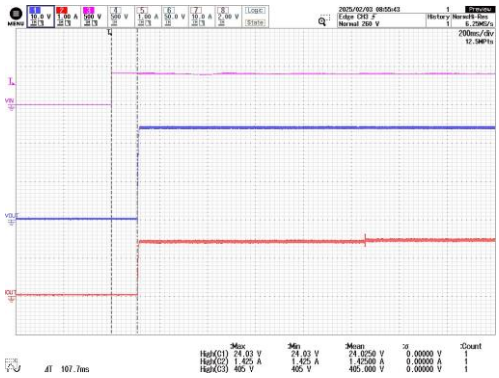


Figure 37 – Output Voltage and Current.
400 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

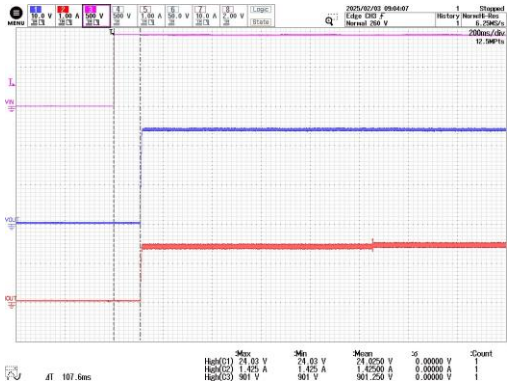


Figure 38 – Output Voltage and Current.
900 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

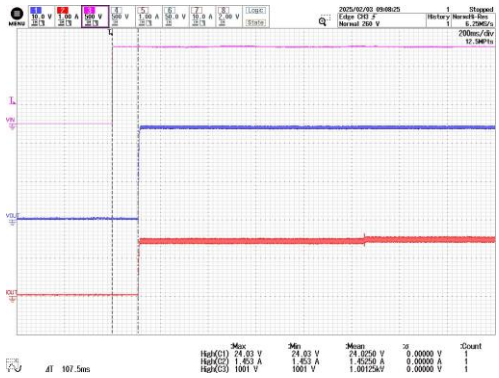


Figure 39 – Output Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[11] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[12] Current waveforms were measured using a Yokogawa current probe.

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient[13,14]

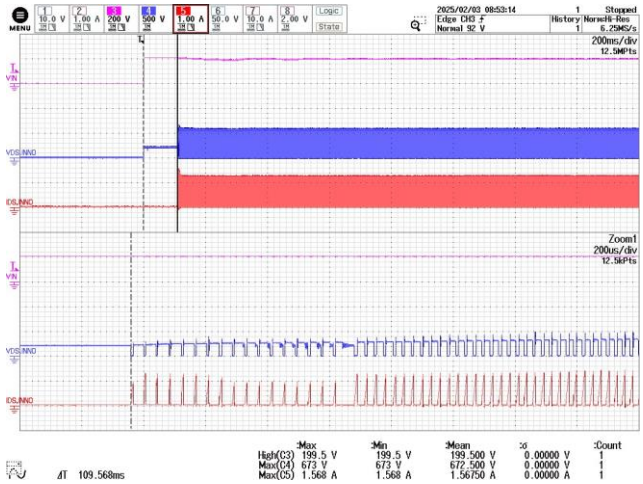


Figure 40 – INN3947FQ Drain Voltage and Current.
200 VDC, 16.3 Ω Load.
CH3: V_{IN}, 200 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

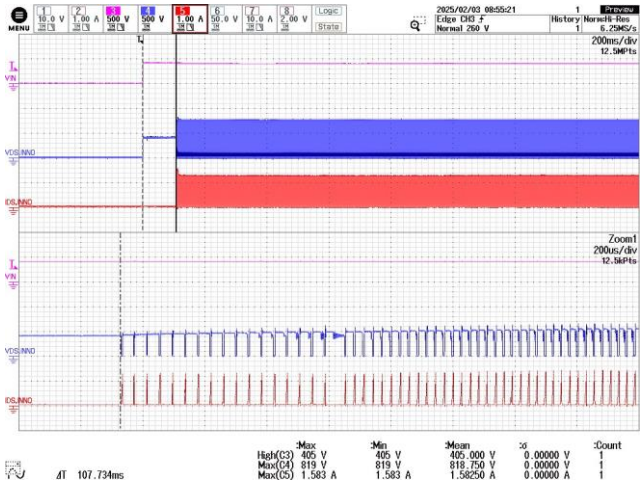


Figure 41 – INN3947FQ Drain Voltage and Current.
400 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

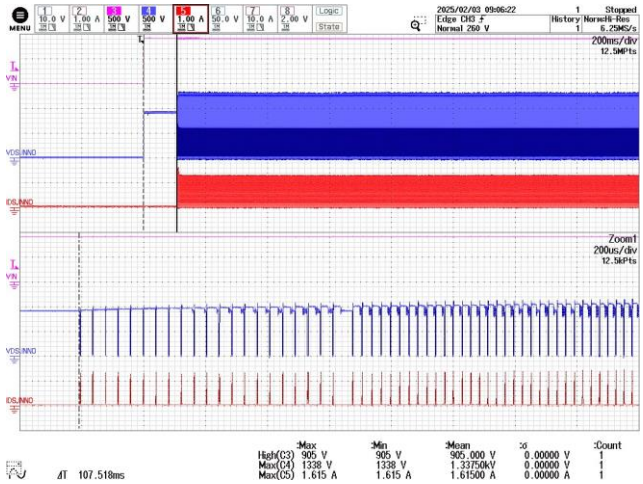


Figure 42 – INN3947FQ Drain Voltage and Current.
900 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

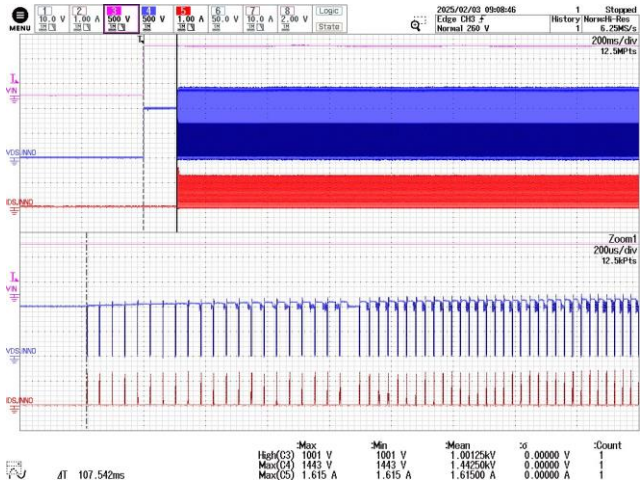


Figure 43 – INN3947FQ Drain Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

[13] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[14] Current waveforms were measured using a Rogowski coil.

11.1.3 SR FET Drain Voltage and Current at 25 °C Ambient[15,16]

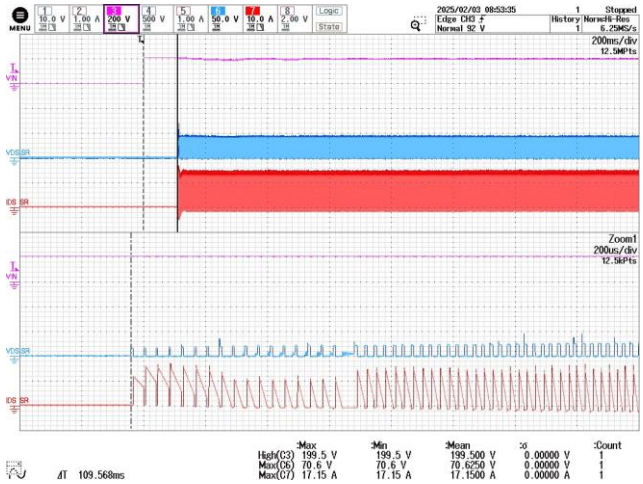


Figure 44 – SR FET Drain Voltage and Current.
200 VDC, 16.3 Ω Load.
CH3: V_{IN}, 200 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

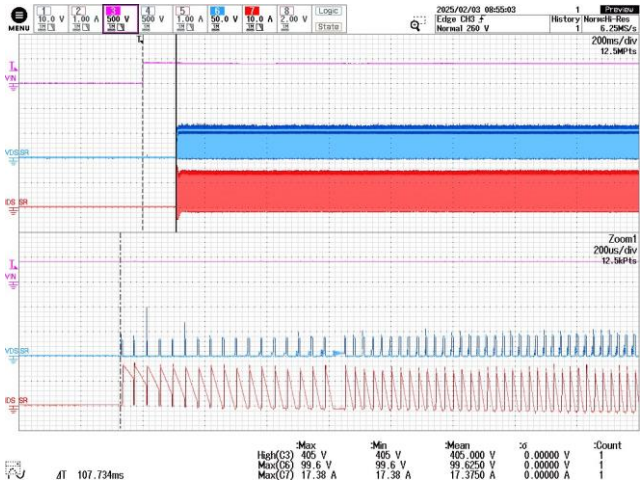


Figure 45 – SR FET Drain Voltage and Current.
400 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

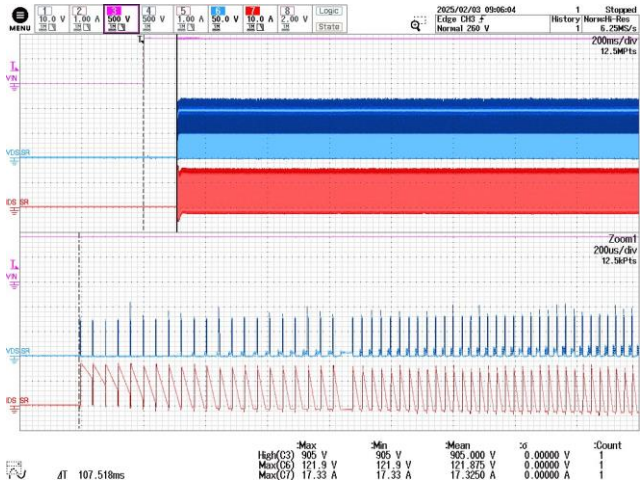


Figure 46 – SR FET Drain Voltage and Current.
900 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

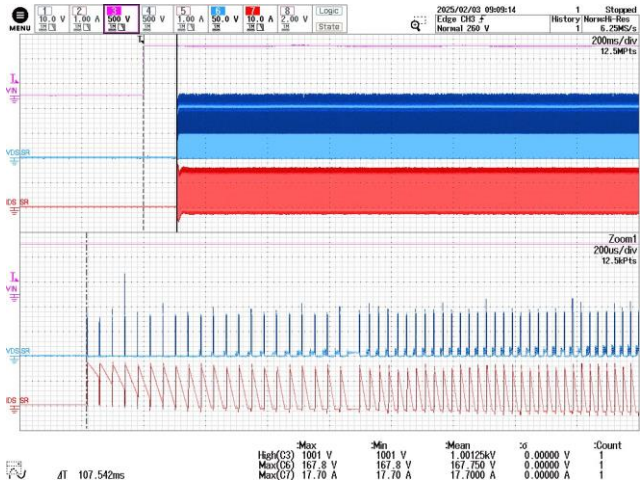


Figure 47 – SR FET Drain Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

[15] The time between when V_{IN} turned on and the SR FET starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[16] Current waveforms were measured using a Rogowski coil.

11.1.4 Output Voltage and Current at 85 °C Ambient[17]

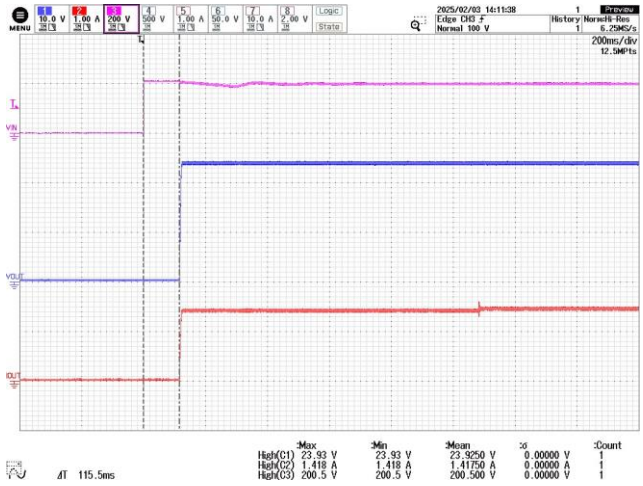


Figure 48 – Output Voltage and Current.
200 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 200 V / div.
Time: 200 ms / div.

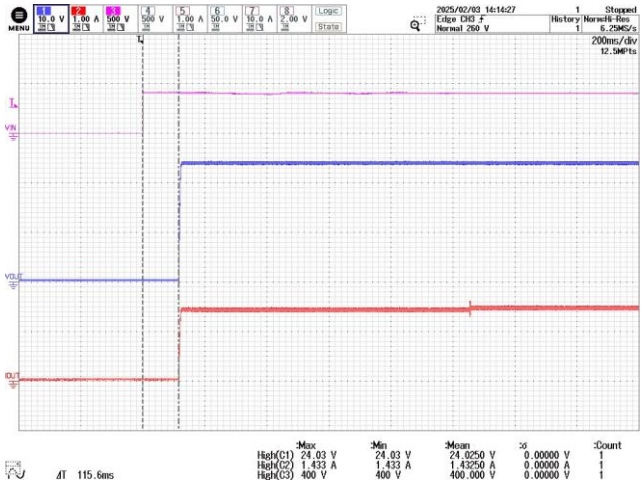


Figure 49 – Output Voltage and Current.
400 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

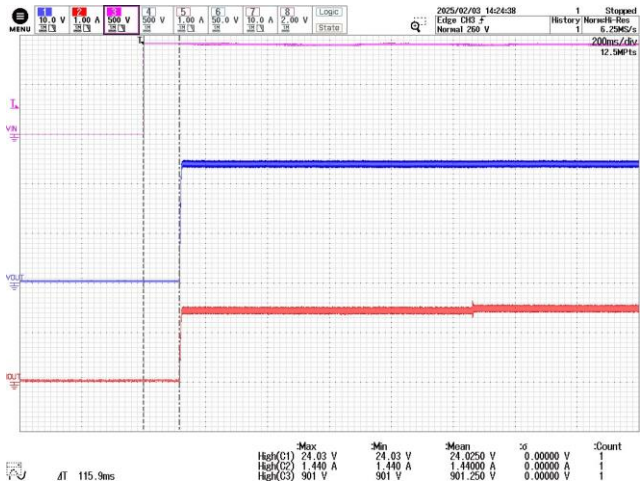


Figure 50 – Output Voltage and Current.
900 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

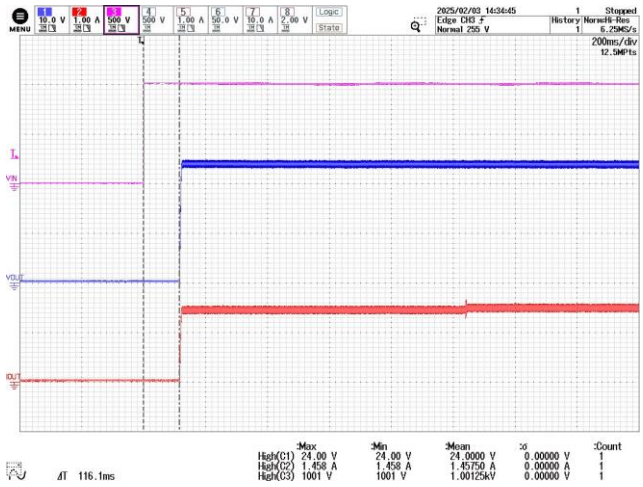


Figure 51 – Output Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[17] Current waveforms were measured using a Yokogawa current probe.

11.1.5 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient[18,19]

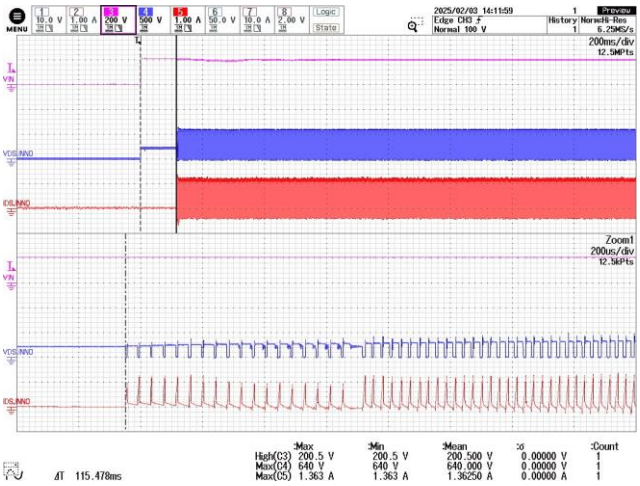


Figure 52 – INN3947FQ Drain Voltage and Current.
200 VDC, 16.3 Ω Load.
CH3: V_{IN}, 200 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

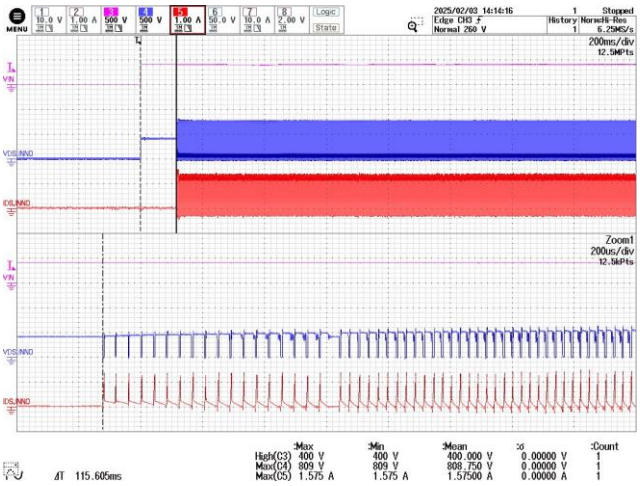


Figure 53 – INN3947FQ Drain Voltage and Current.
400 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

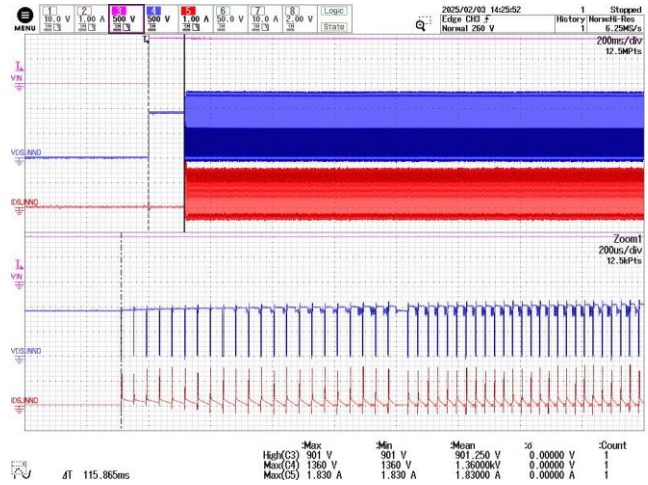


Figure 54 – INN3947FQ Drain Voltage and Current.
900 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

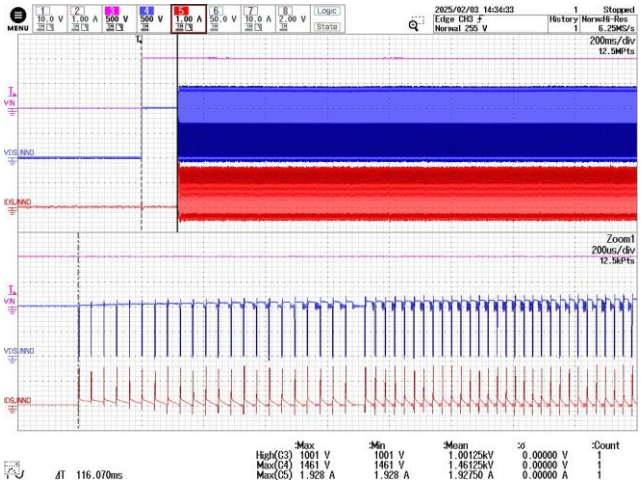


Figure 55 – INN397FQ Drain Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

[18] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[19] Current waveforms were measured using a Rogowski coil.

11.1.6 SR FET Drain Voltage and Current at 85 °C Ambient[20,21]

Figure 56 – SR FET Drain Voltage and Current.
200 VDC_C, 16.3 Ω Load.
CH3: V_{IN}, 200 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

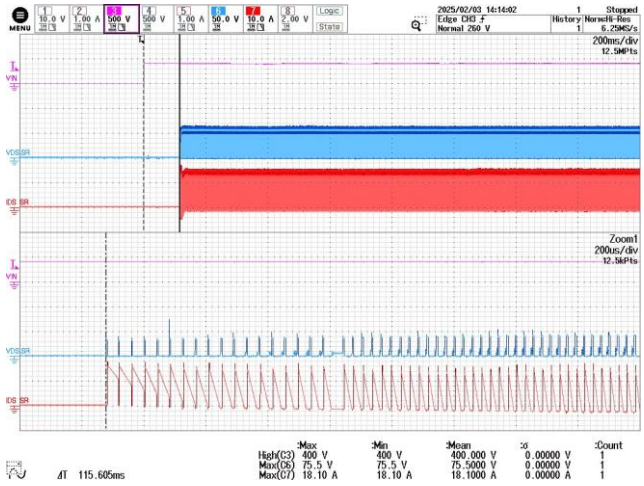


Figure 57 – SR FET Drain Voltage and Current.
400 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

Figure 58 – SR FET Drain Voltage and Current.
900 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

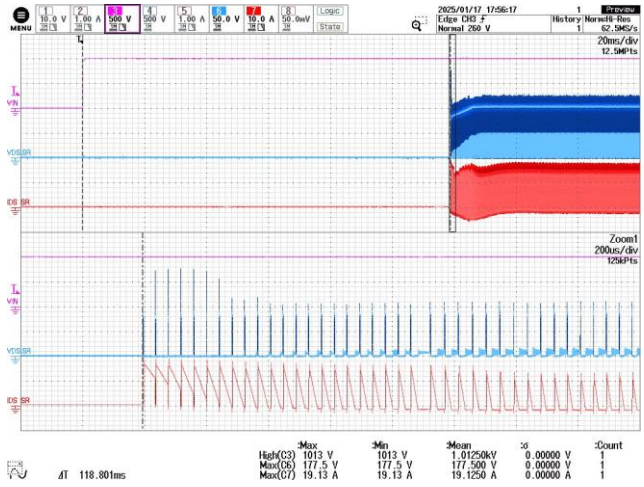


Figure 59 – SR FET Drain Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

[20] The time between when V_{IN} turned on and the SR FET starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[21] Current waveforms were measured using a Rogowski coil.

11.1.7 Output Voltage and Current at -40 °C Ambient[22]

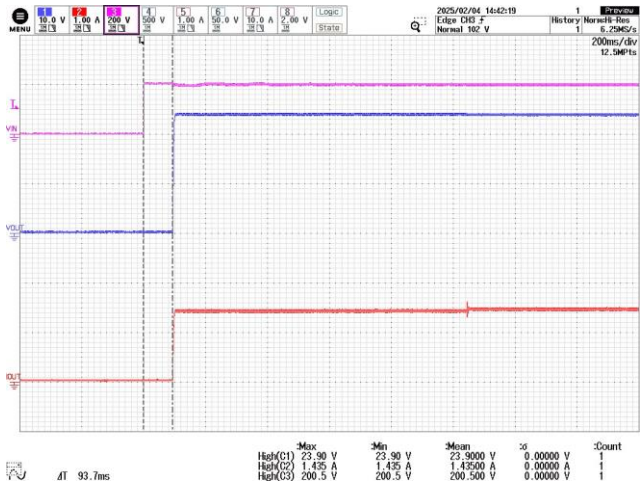


Figure 60 – Output Voltage and Current.
200 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 200 V / div.
Time: 200 ms / div.

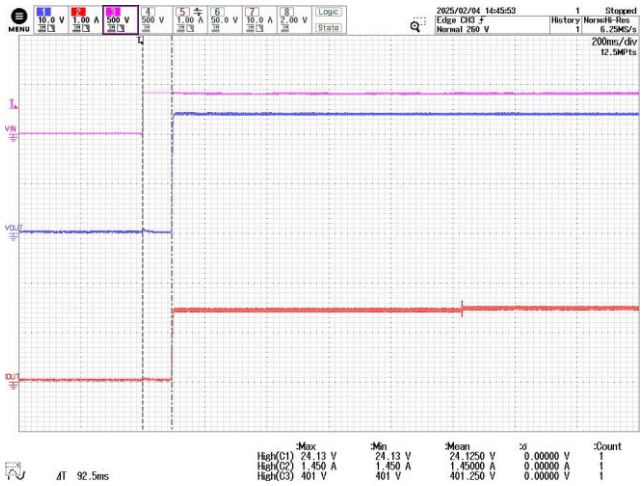


Figure 61 – Output Voltage and Current.
400 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

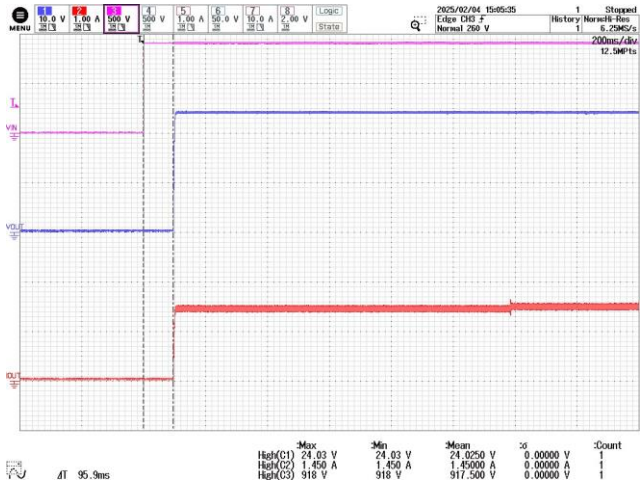


Figure 62 – Output Voltage and Current.
900 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

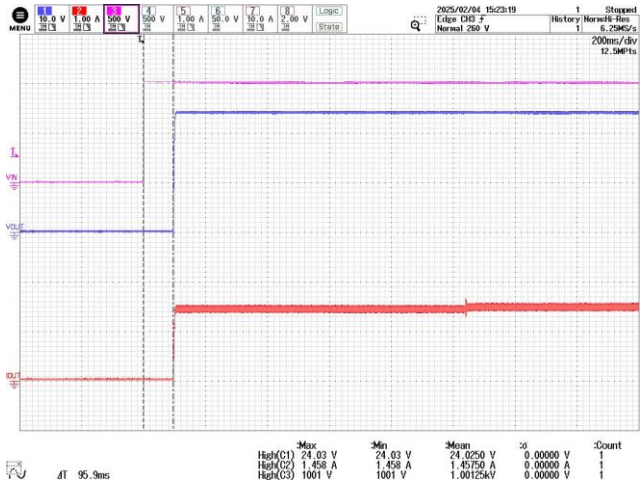


Figure 63 – Output Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH1: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[22] Current waveforms were measured using a Yokogawa current probe.

11.1.8 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient[23,24]

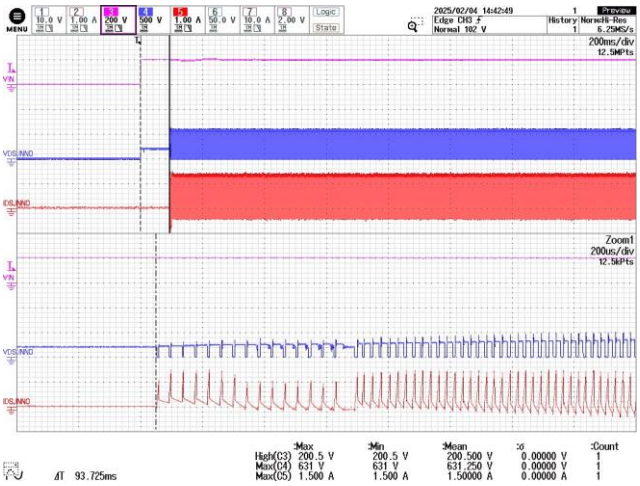


Figure 64 – INN3947FQ Drain Voltage and Current.
200 VDC, 16.3 Ω Load.
CH3: V_{IN}, 200 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

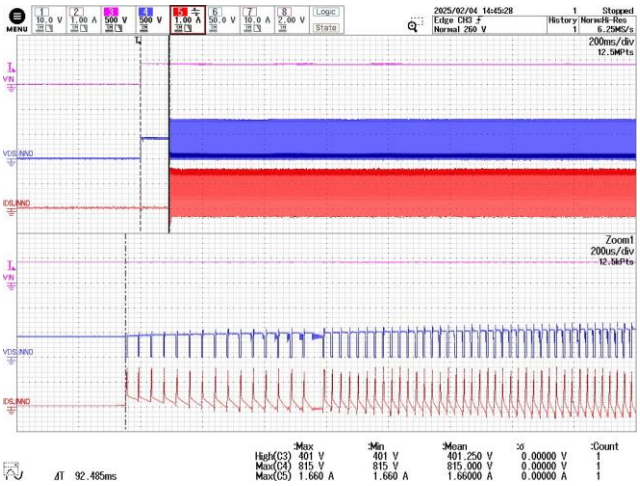


Figure 65 – INN3947FQ Drain Voltage and Current.
400 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

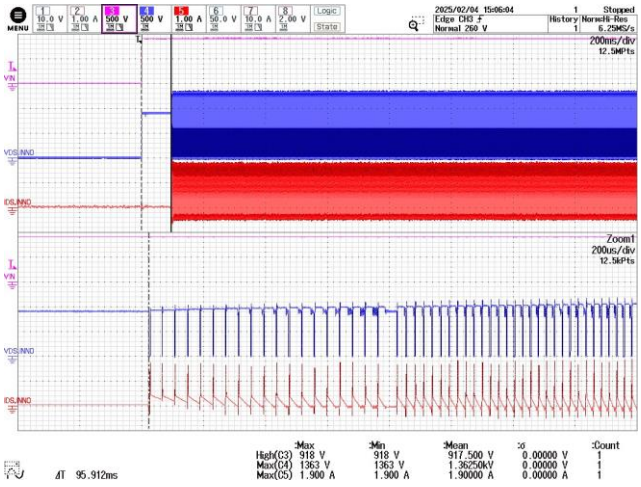


Figure 66 – INN3947FQ Drain Voltage and Current.
900 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

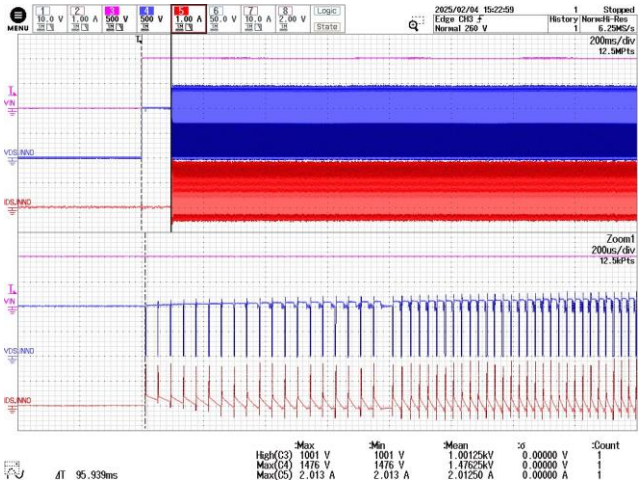


Figure 67 – INN3947FQ Drain Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 200 ms / div.

[23] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[24] Current waveforms were measured using a Rogowski coil.

11.1.9 SR FET Drain Voltage and Current at -40 °C Ambient[25,26]

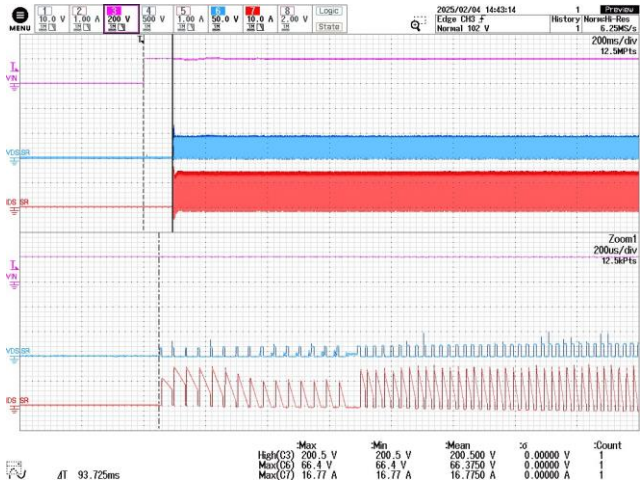


Figure 68 – SR FET Drain Voltage and Current.
200 VDC, 16.3 Ω Load.
CH3: V_{IN}, 200 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

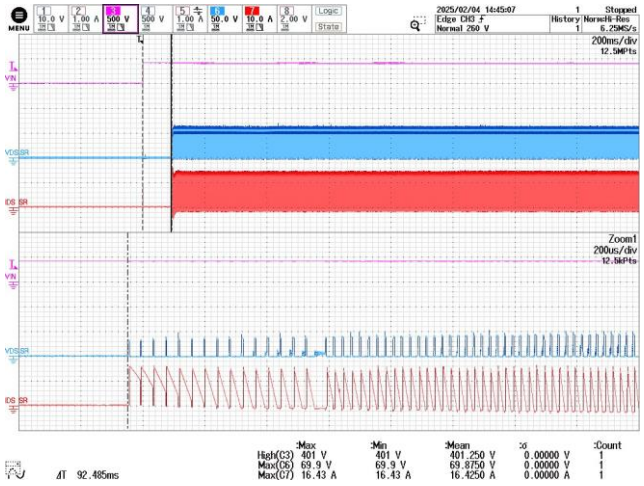


Figure 69 – SR FET Drain Voltage and Current.
400 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

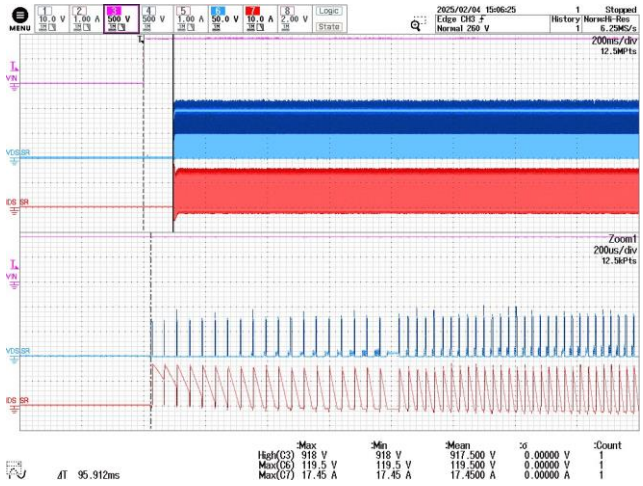


Figure 70 – SR FET Drain Voltage and Current.
900 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

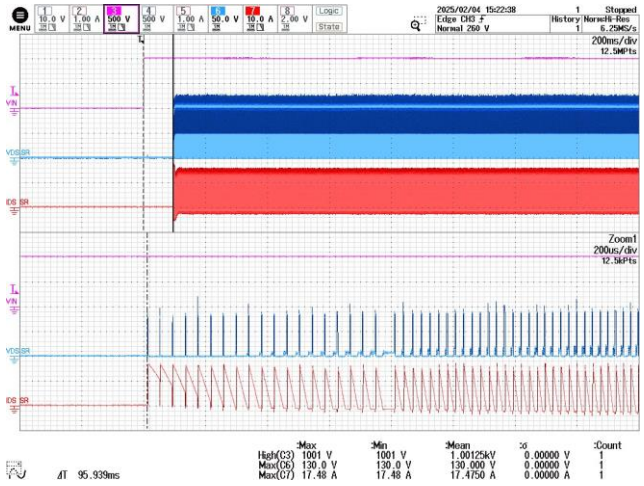


Figure 71 – SR FET Drain Voltage and Current.
1000 VDC, 16.3 Ω Load.
CH3: V_{IN}, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 200 ms / div.

[25] The time between when V_{IN} turned on and the SR FET starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[26] Current waveforms were measured using a Rogowski coil.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 85 °C Ambient

11.2.1.1 Component Stress in Normal Operation

Input	Steady-State Switching Waveforms 85 °C Ambient, Full Load					
	INN3947FQ			SR FET		
V_{IN} (V)	I_D (A)	V_{DS} (V)	V_{STRESS} (%)	I_D (A)	V_{DS} (V)	V_{STRESS} (%)
200	1.35	628	36.9	15.2	46.5	31.0
400	1.52	805	47.4	14.6	67.9	45.3
900	1.41	1358	79.9	15.1	120	80.0
1000	1.37	1466	86.2	15.1	131	87.0

Table 10 – Summary of Critical Component Voltage Stresses at 85 °C Ambient.

11.2.1.1 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient[27]

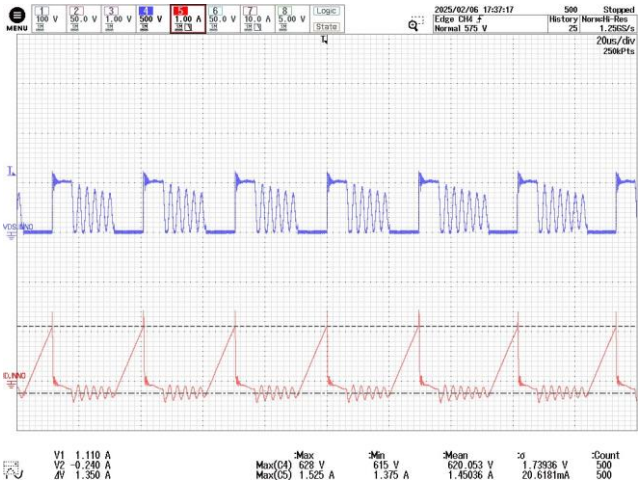


Figure 72 – InnoSwitch3-AQ and SR FET Drain Voltage.
200 VDC, 1.46 A Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

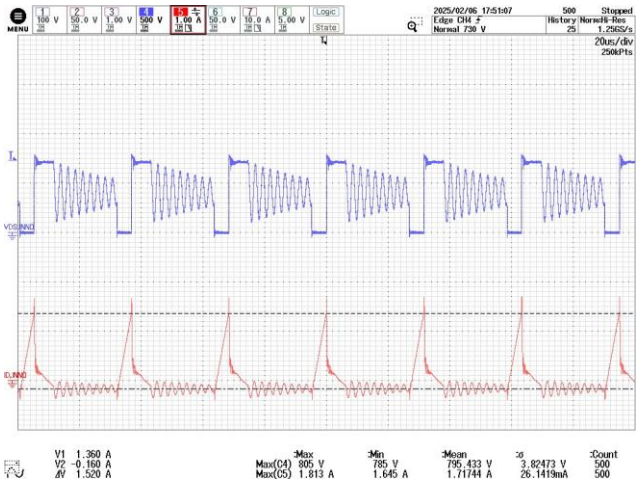


Figure 73 – InnoSwitch3-AQ and SR FET Drain Voltage.
400 VDC, 1.46 A Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

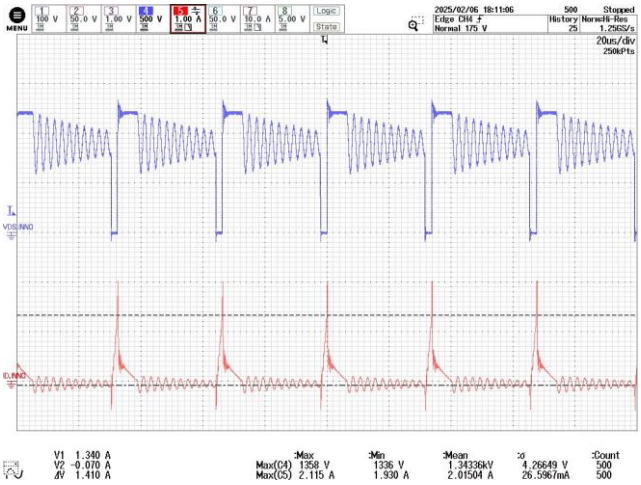


Figure 74 – InnoSwitch3-AQ and SR FET Drain Voltage.
900 VDC, 1.46 A Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

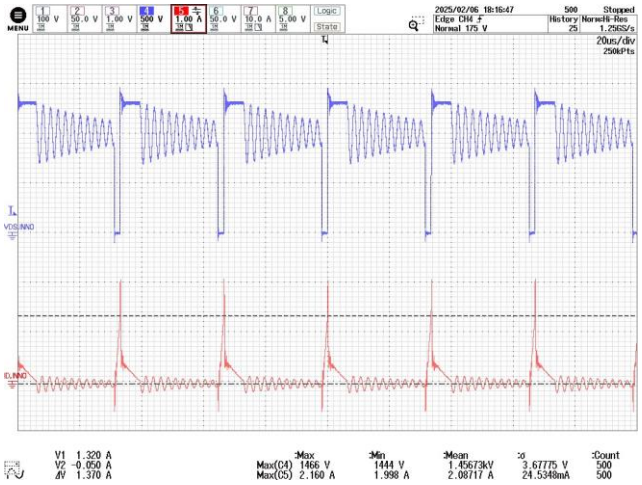


Figure 75 – InnoSwitch3-AQ and SR FET Drain Voltage.
1000 VDC, 1.46 A Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

[27] Current waveforms were measured using a Rogowski coil.

11.2.1.2 SR FET Drain Voltage and Current at 85 °C Ambient[28]

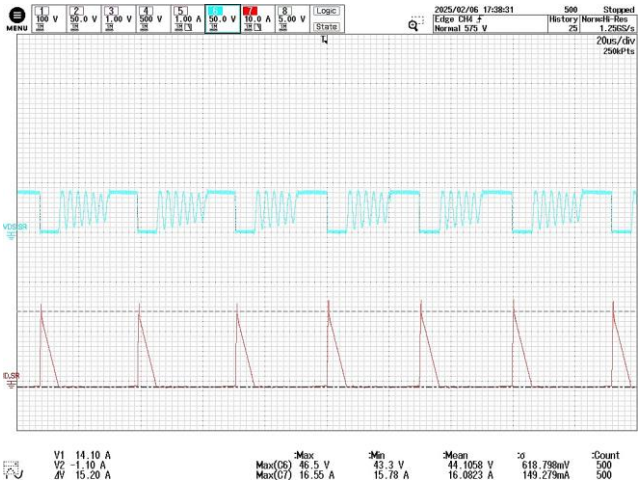


Figure 76 – InnoSwitch3-AQ and SR FET Drain Voltage.
200 VDC, 1.46 A Load, 85 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 1 A / div.
Time: 20 μs / div.

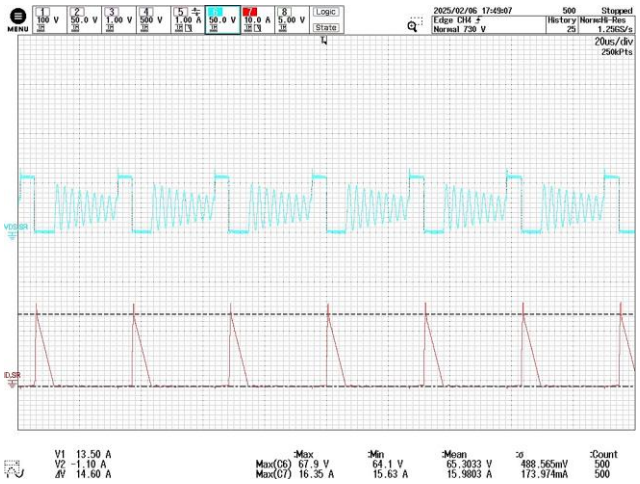


Figure 77 – InnoSwitch3-AQ and SR FET Drain Voltage.
400 VDC, 1.46 A Load, 85 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 1 A / div.
Time: 20 μs / div.

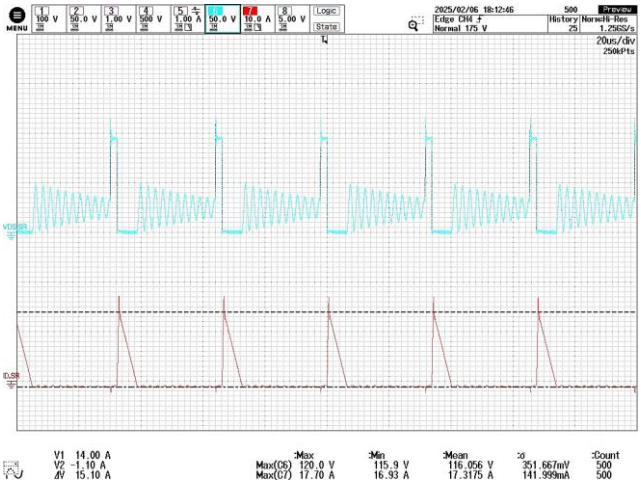


Figure 78 – InnoSwitch3-AQ and SR FET Drain Voltage.
900 VDC, 1.46 A Load, 85 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 1 A / div.
Time: 20 μs / div.

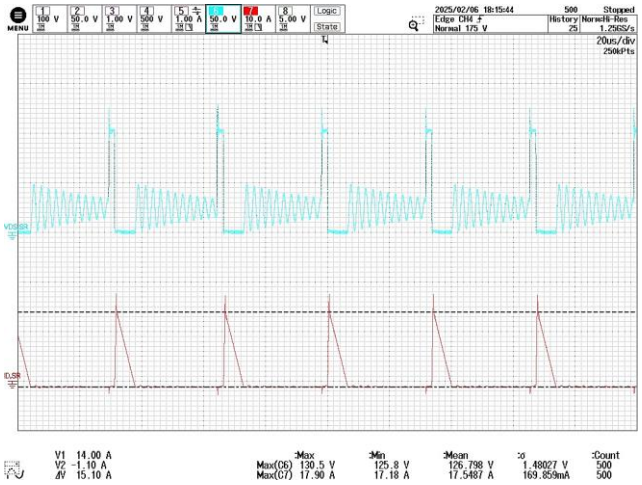


Figure 79 – InnoSwitch3-AQ and SR FET Drain Voltage.
1000 VDC, 1.46 A Load, 85 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 1 A / div.
Time: 20 μs / div.

[28] Current waveforms were measured using a Rogowski coil.

11.2.1.3 Short-Circuit Response

The unit was tested by applying an output short-circuit during normal operation and then removing the short-circuit to determine whether the unit will recover and operate normally. The expected response during short-circuit is for the unit to enter auto-restart (AR) mode and attempt to recover every 1.7 - 2.11 seconds. Full-load test configuration was set to 16.3 ohms constant resistance for this test.

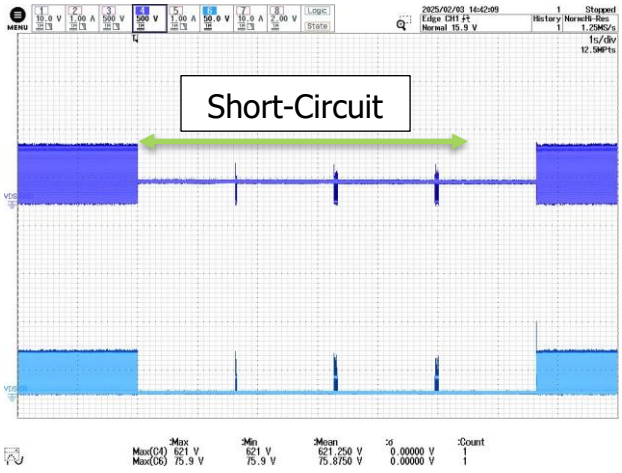


Figure 80 – InnoSwitch3-AQ and SR FET Drain Voltage. 200 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
Time: 1 s / div.

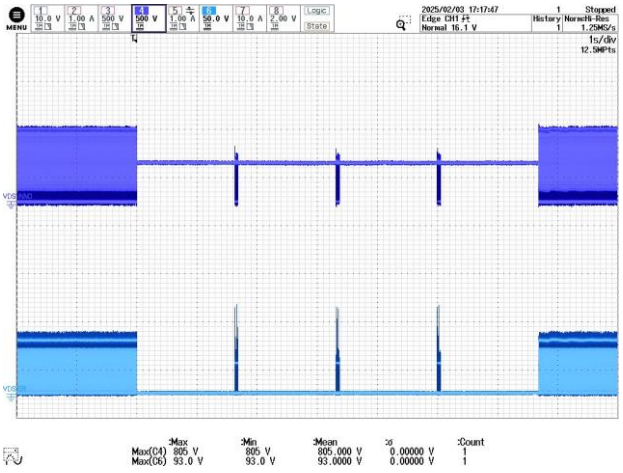


Figure 81 – InnoSwitch3-AQ and SR FET Drain Voltage. 400 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
Time: 1 s / div.

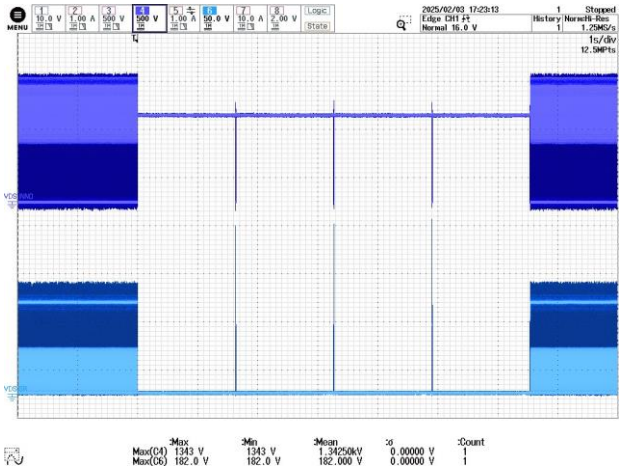


Figure 82 – InnoSwitch3-AQ and SR FET Drain voltage. 900 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
Time: 1 s / div.

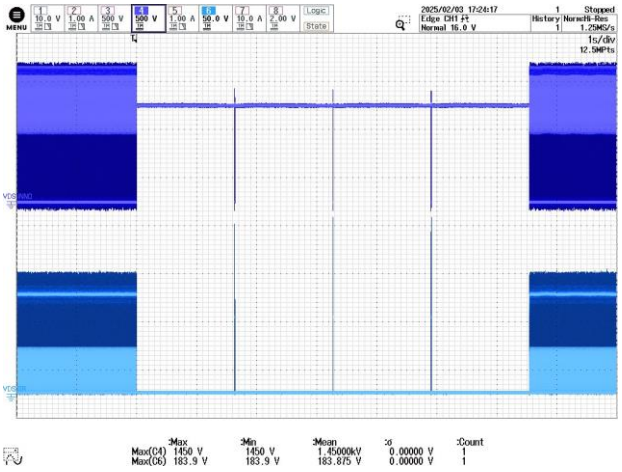


Figure 83 – InnoSwitch3-AQ and SR FET Drain voltage. 1000 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH6: $V_{DS,SRFET}$, 50 V / div.
Time: 1 s / div.

11.2.2 Switching Waveforms at 25 °C Ambient

11.2.2.1 Component Stress in Normal Operation

Input	Steady-State Switching Waveforms 25 °C Ambient, Full Load					
	INN3947FQ			SR FET		
V_{IN} (V)	I_D (A)	V_{DS} (V)	V_{STRESS} (%)	I_D (A)	V_{DS} (V)	V_{STRESS} (%)
200	1.33	625	36.8	14.0	44.5	29.7
400	1.34	804	47.3	14.2	66.4	44.3
900	1.17	1360	80.0	14.7	122	81.3
1000	1.14	1480	87.1	14.5	132	88.0

Table 11 – Summary of Voltage Stresses on Critical Components at 25 °C Ambient.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient[29]

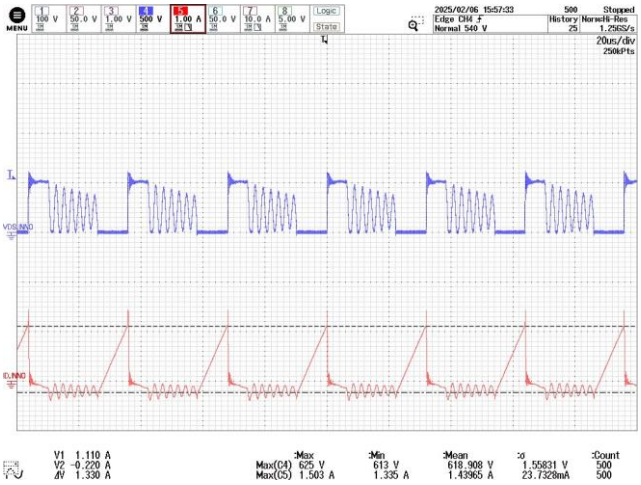


Figure 84 – InnoSwitch3-AQ Drain Voltage and Current.
200 VDC, 1.46 A Load, 25 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

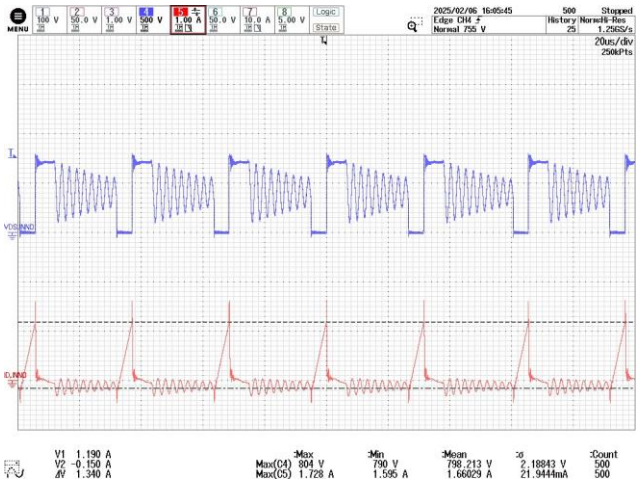


Figure 85 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 1.46 A Load, 25 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

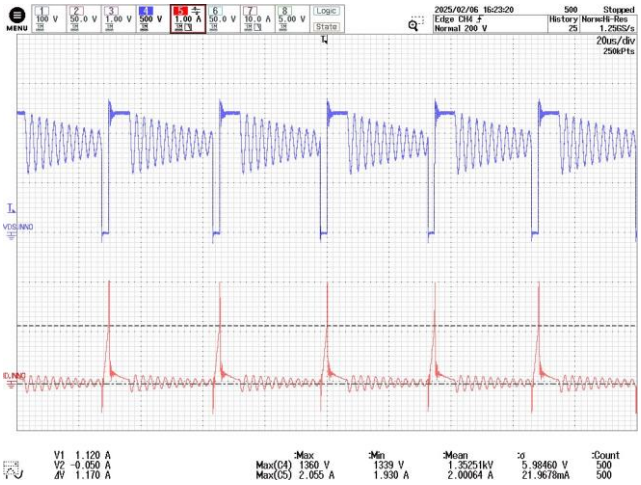


Figure 86 – InnoSwitch3-AQ Drain Voltage and Current.
900 VDC, 1.46 A Load, 25 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

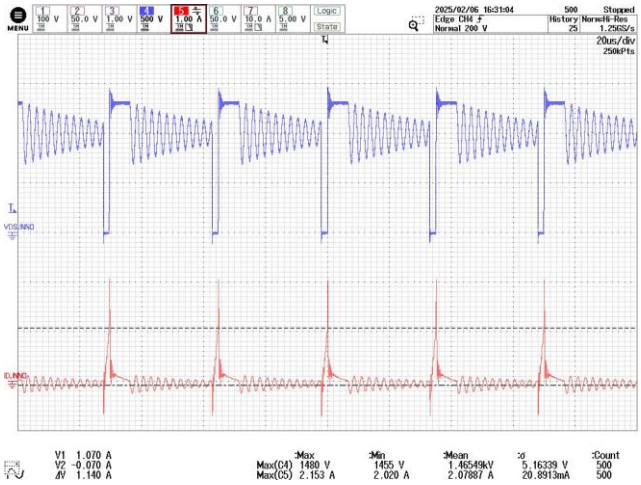


Figure 87 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 1.46 A Load, 25 °C Ambient.
CH4: $V_{DS,INNO}$, 500 V / div.
CH5: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

[29] Current waveforms were measured using a Rogowski coil.

11.2.2.3 SR FET Drain Voltage and Current at 25 °C Ambient[30]

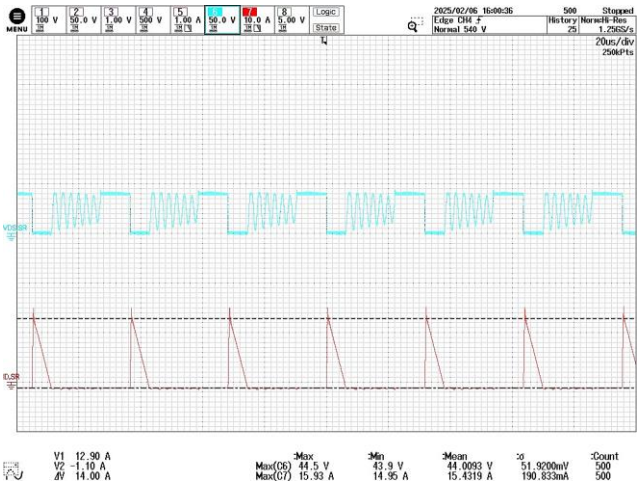


Figure 88 – SR FET Drain Voltage and Current.
200 VDC, 1.46 A Load, 25 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

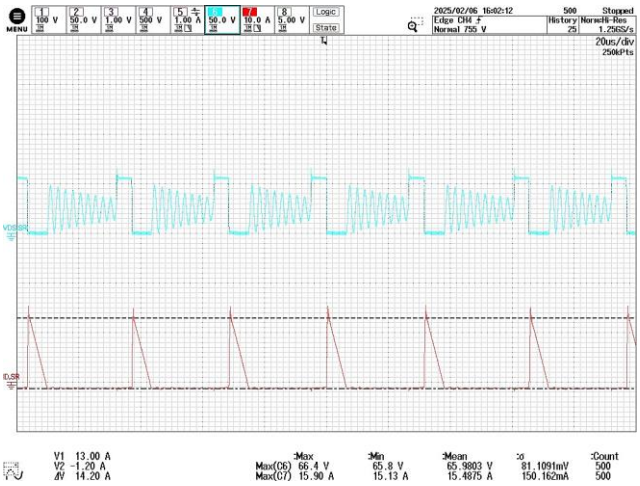


Figure 89 – SR FET Drain Voltage and Current.
400 VDC, 1.46 A Load, 25 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

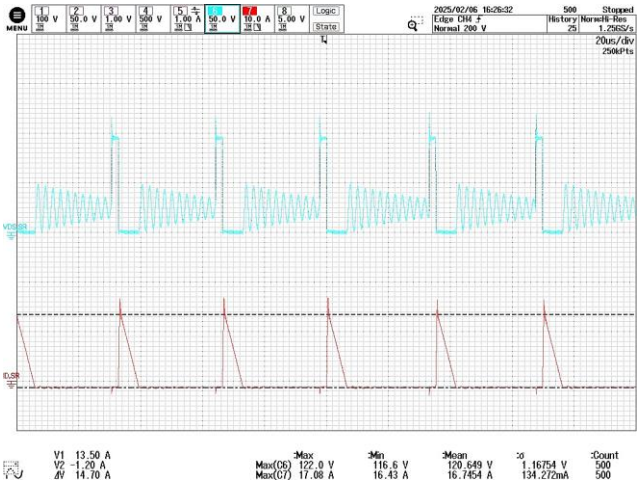


Figure 90 – SR FET Drain Voltage and Current.
800 VDC, 1.46 A Load, 25 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

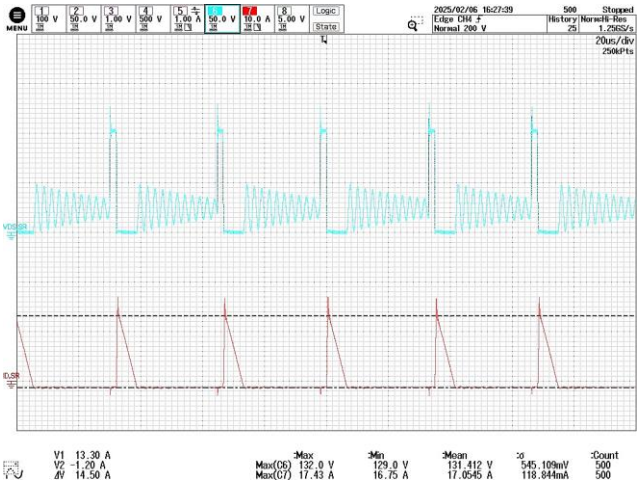


Figure 91 – SR FET Drain Voltage and Current.
1000 VDC, 1.46 A Load, 25 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

[30] Current waveforms were measured using a Rogowski coil.

11.2.3 Switching Waveforms at -40 °C Ambient

11.2.3.1 Component Stress in Normal Operation

Input	Steady-State Switching Waveforms -40 °C Ambient, Full Load					
	INN3947FQ			SR FETs		
V_{IN} (V)	I_D (A)	V_{DS} (V)	V_{STRESS} (%)	I_D (A)	V_{DS} (V)	V_{STRESS} (%)
200	1.46	630	37.1	14.3	45.9	30.6
400	1.44	810	47.6	14.5	65.1	43.4
900	1.36	1378	81.1	15.1	122	81.3
1000	1.35	1485	87.4	14.7	133	88.7

Table 12 – Summary of Voltage Stresses on Critical Components at -40 °C Ambient.

11.2.3.2 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient[31]

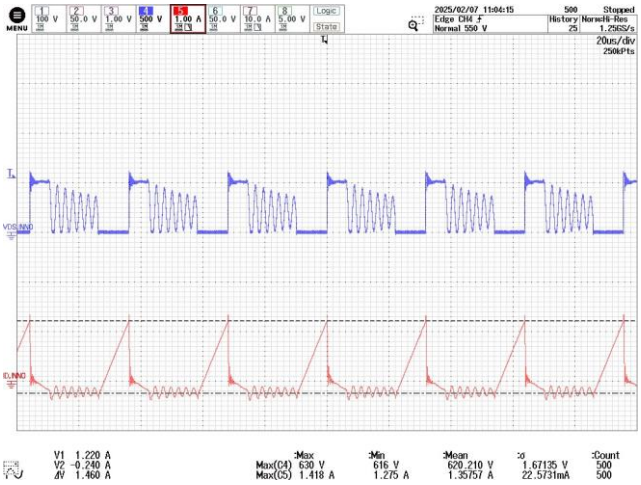


Figure 92 – InnoSwitch3-AQ Drain Voltage and Current.
200 VDC, 1.46 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

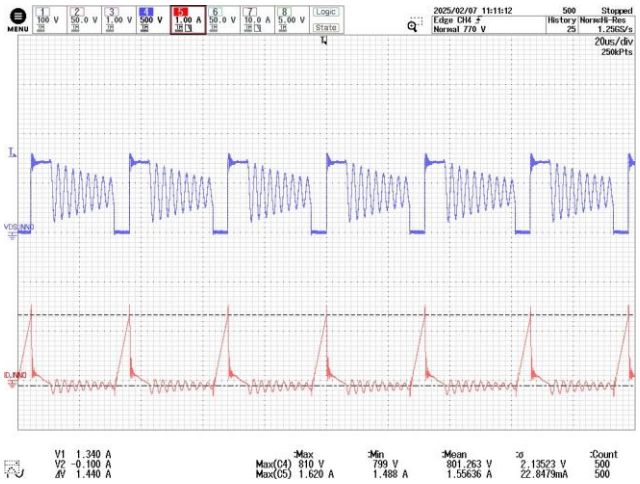


Figure 93 – InnoSwitch3-AQ Drain Voltage and Current.
400 VDC, 1.46 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

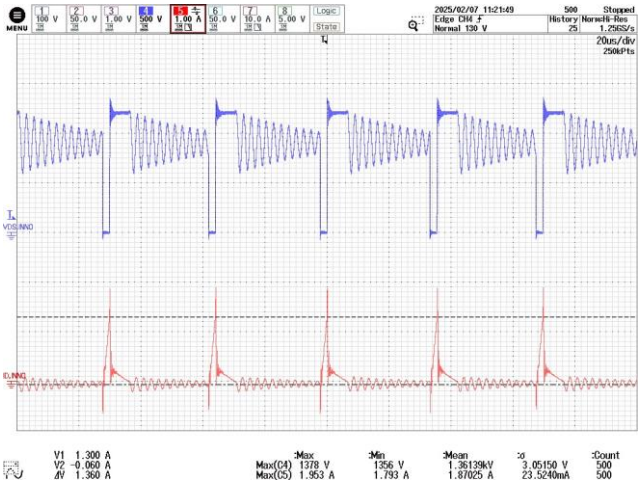


Figure 94 – InnoSwitch3-AQ Drain Voltage and Current.
900 VDC, 1.46 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

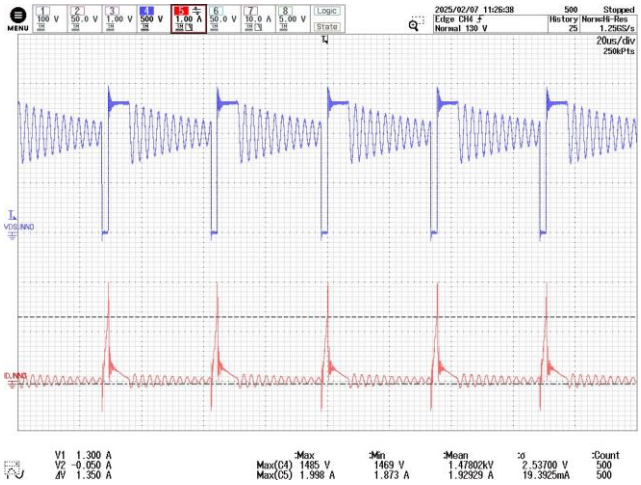


Figure 95 – InnoSwitch3-AQ Drain Voltage and Current.
1000 VDC, 1.46 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1 A / div.
Time: 20 μs / div.

[31] Current waveforms were measured using a Rogowski coil.

11.2.3.3 SR FET Drain Voltage and Current at -40 °C Ambient[32]

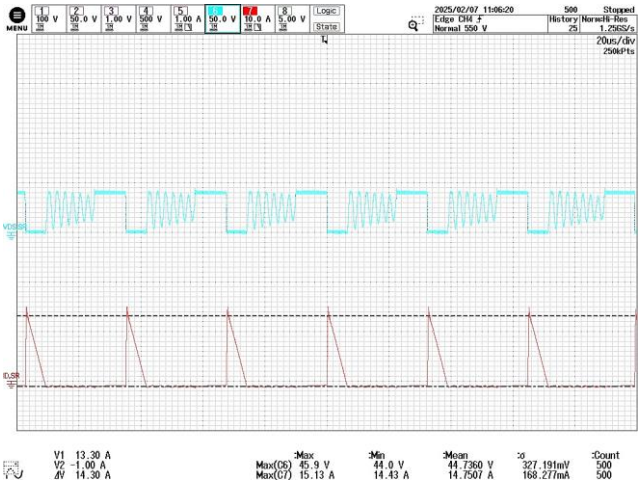


Figure 96 – SR FET Drain Voltage and Current.
200 VDC, 1.46 A Load, -40 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

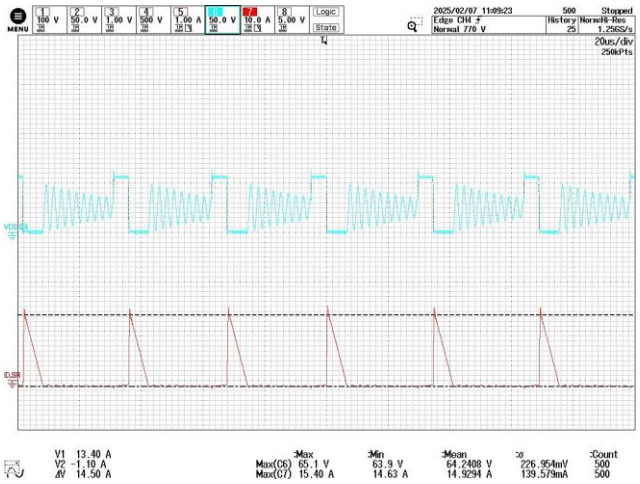


Figure 97 – SR FET Drain Voltage and Current.
400 VDC, 1.46 A Load, -40 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

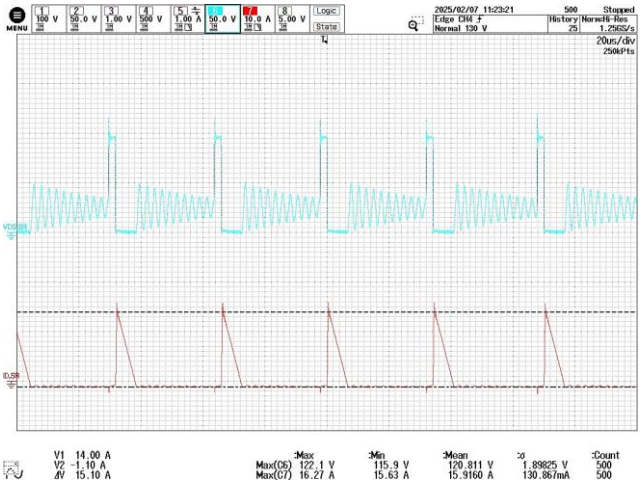


Figure 98 – SR FET Drain Voltage and Current.
900 VDC, 1.46 A Load, -40 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

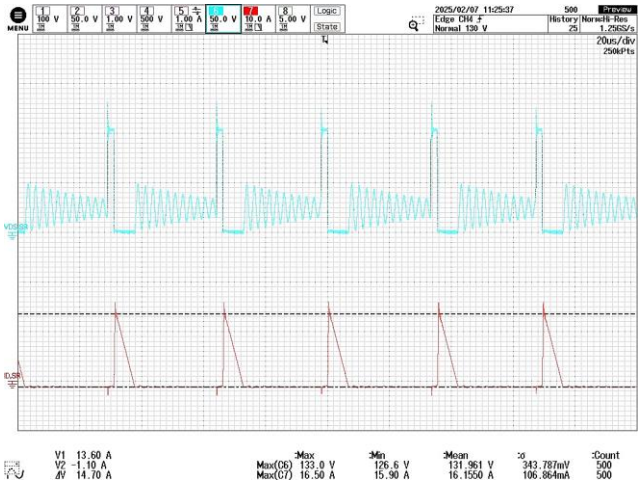


Figure 99 – SR FET Drain Voltage and Current.
1000 VDC, -40 A Load, 85 °C Ambient.
CH6: $V_{DS,SRFET}$, 50 V / div.
CH7: $I_{D,SRFET}$, 10 A / div.
Time: 20 μs / div.

[32] Current waveforms were measured using a Rogowski coil.

11.3 Load Transient Response

Output voltage waveforms were captured when subjected to a dynamic load-transient from 0% to 50%, 50% to 100%, and 10% to 90%. The time duration for the load at each state was set to 100 ms with a load slew rate of 100 mA / μs. The test was performed at 85 °C ambient.

Dynamic Load Settings	V_{IN} (V)	$V_{OVERSHOOT(MAX)}$ (mV)	$V_{UNDERSHOOT(MIN)}$ (mV)
0% to 50% (0 A to 0.73 A)	200	152	167
	400	168	178
	900	174	226
	1000	182	214
50% to 100% (0.73 A to 1.46 A)	200	257	141
	400	273	151
	900	300	236
	1000	305	257
10% to 90% (0.146 A to 1.31 A)	200	263	267
	400	261	223
	900	286	340
	1000	288	342

Table 13 – Load Transient Response.

11.3.1 Output Voltage Ripple with 0% to 50% Transient Load at 85 °C Ambient

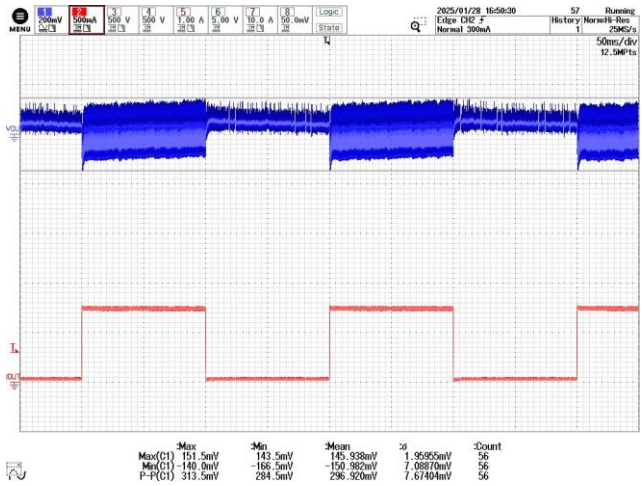


Figure 100 – Output Voltage and Current.
200 VDC, 0 A to 0.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

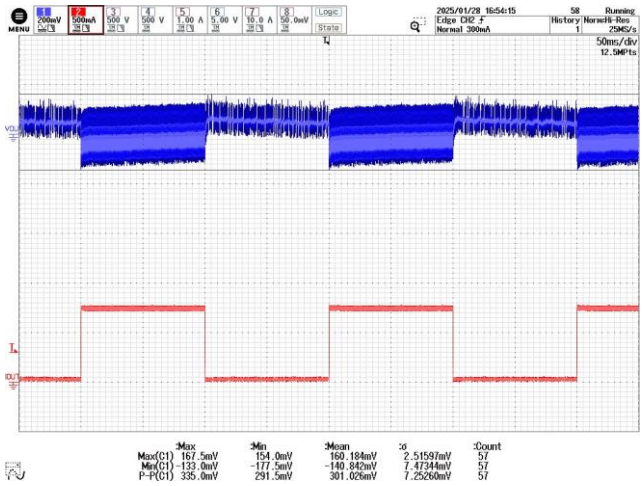


Figure 101 – Output Voltage and Current.
400 VDC, 0 A to 0.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

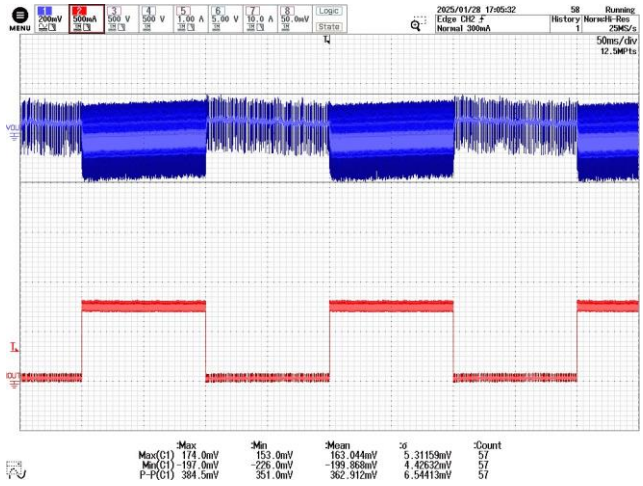


Figure 102 – Output Voltage and Current.
900 VDC, 0 A to 0.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

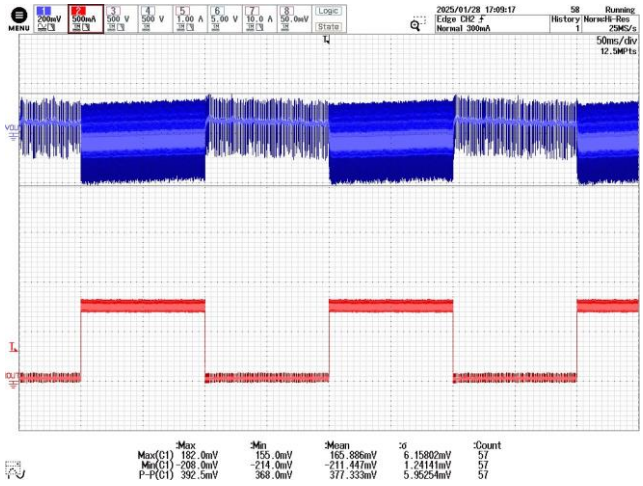


Figure 103 – Output Voltage and Current.
1000 VDC, 0 A to 0.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

11.3.2 Output Voltage Ripple with 50% to 100% Transient Load at 85 °C Ambient

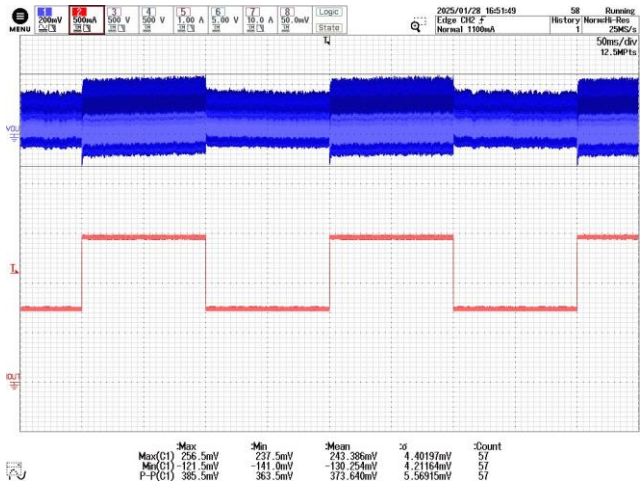


Figure 104 – Output Voltage and Current.
200 VDC,
0.73 A to 1.46 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

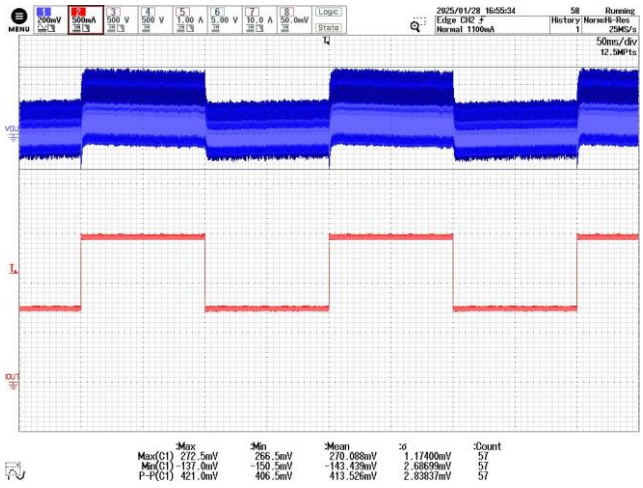


Figure 105 – Output Voltage and Current.
400 VDC,
0.73 A to 1.46 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

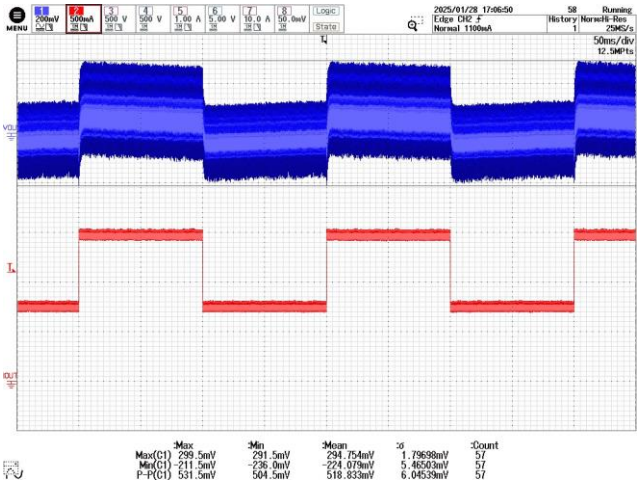


Figure 106 – Output Voltage and Current.
900 VDC,
0.73 A to 1.46 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

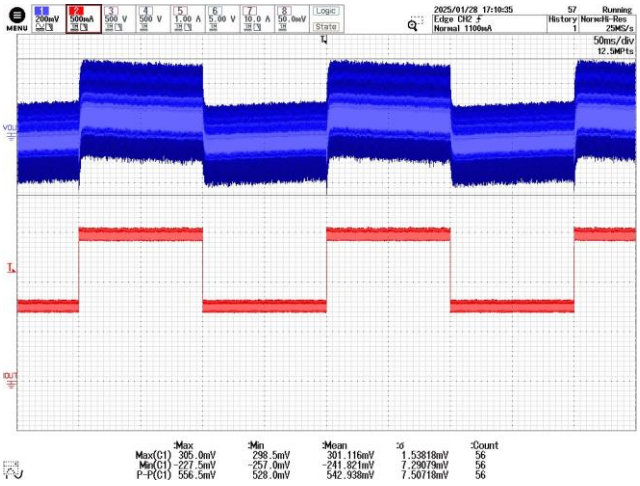


Figure 107 – Output Voltage and Current.
1000 VDC,
0.73 A to 1.46 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

11.3.3 Output Voltage Ripple with 10% to 90% Transient Load at 85 °C Ambient

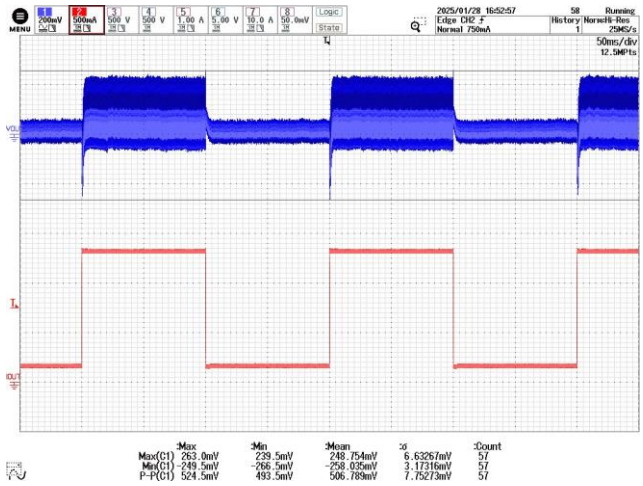


Figure 108 – Output Voltage and Current.
200 VDC,
146 mA to 1.31 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

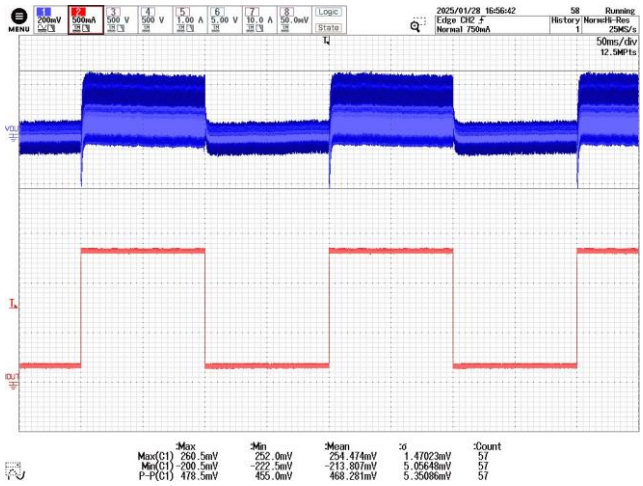


Figure 109 – Output Voltage and Current.
400 VDC,
146 mA to 1.31 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

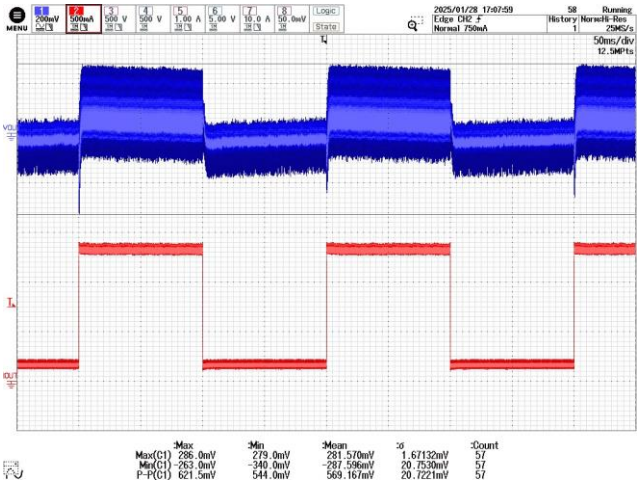


Figure 110 – Output Voltage and Current.
900 VDC,
146 mA to 1.31 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

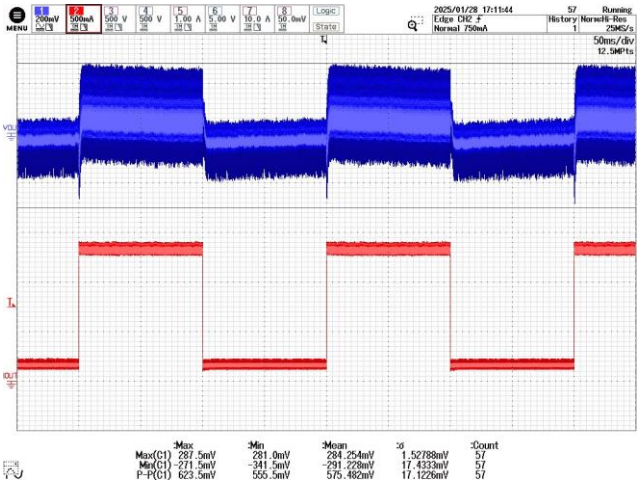


Figure 111 – Output Voltage and Current.
1000 VDC,
146 mA to 1.31 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 500 mA / div.
Time: 50 ms / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

A modified oscilloscope test probe was used for output voltage ripple measurements to reduce spurious signals due to pick-up. Details of the probe modification are provided in Figure 112 and Figure 113 below.

A CT2708 probe adapter was affixed with a 1 μF / 50 V ceramic capacitor placed in parallel between the probe tip and GND terminal. A twisted pair of wires, kept as short as possible, was soldered directly between the probe and the output terminals.

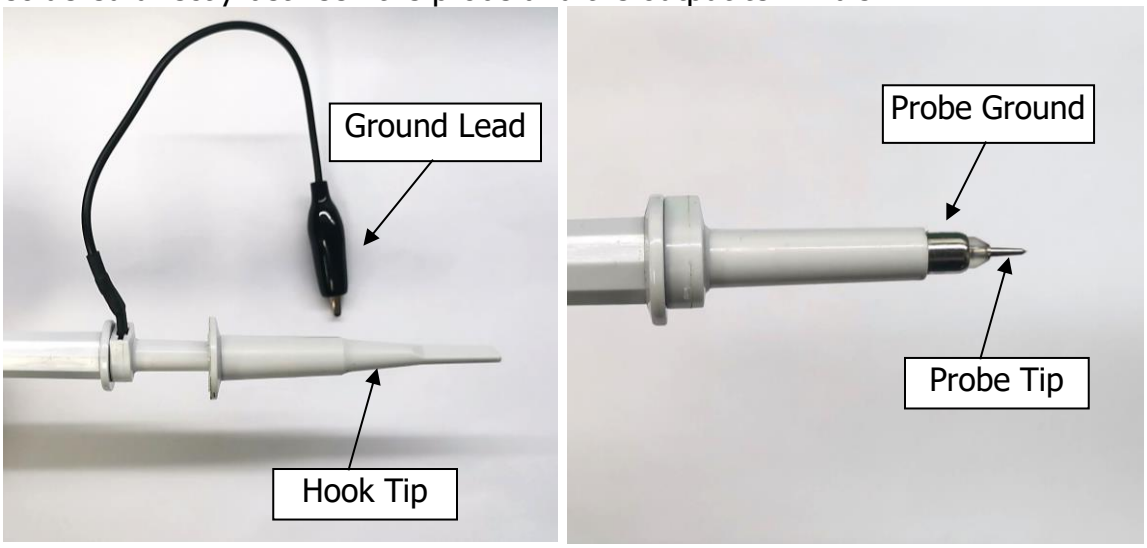


Figure 112 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

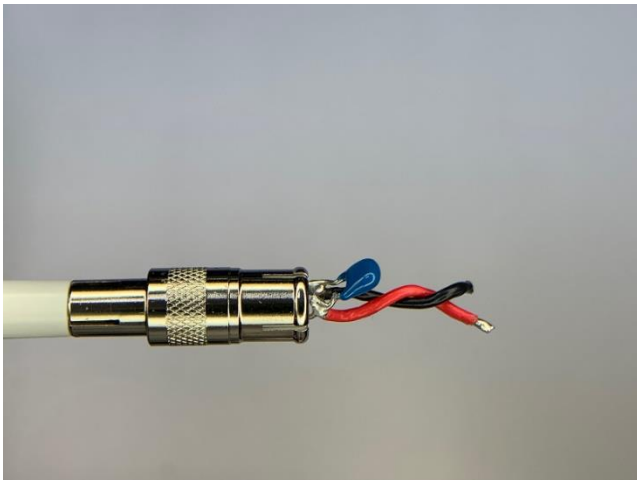


Figure 113 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

The output voltage ripple waveform was recorded at the output terminals at full load using the ripple measurement probe with a decoupling capacitor.

11.4.2.1 Output Voltage Ripple at 85 °C Ambient with Constant Full Load[33]

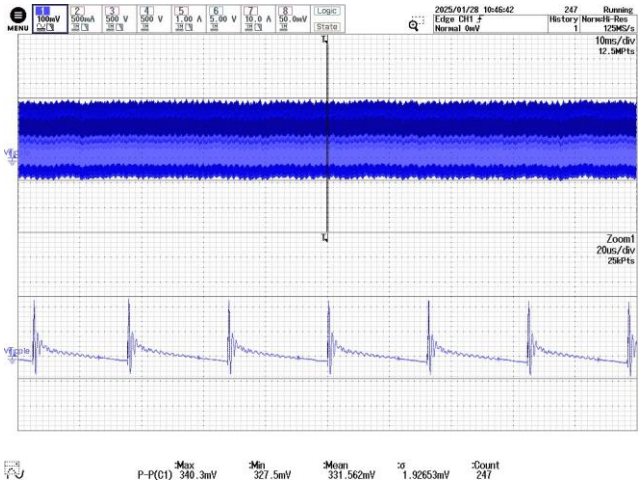


Figure 114 – Output Voltage Ripple.
200 VDC, 1.46 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 340 mV.

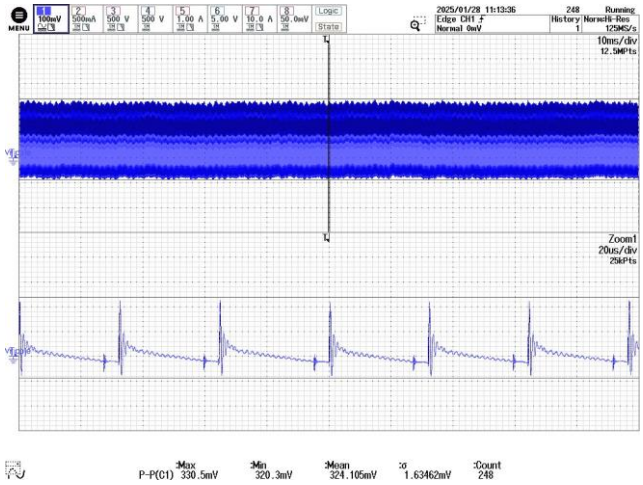


Figure 115 – Output Voltage Ripple.
400 VDC, 1.46 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 382 mV.

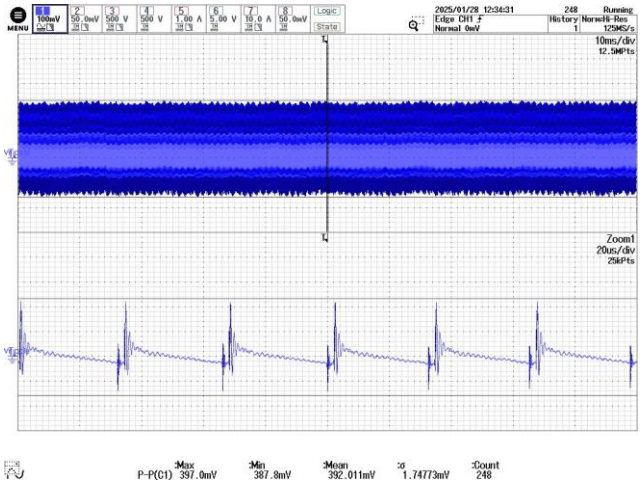


Figure 116 – Output Voltage Ripple.
900 VDC, 1.46 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 397 mV.

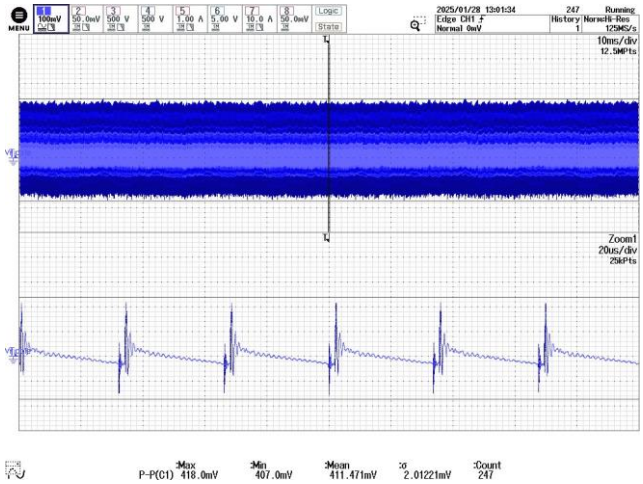


Figure 117 – Output Voltage Ripple.
1000 VDC, 1.46 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 418 mV.

[33] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at 25 °C Ambient with Constant Full Load[34]

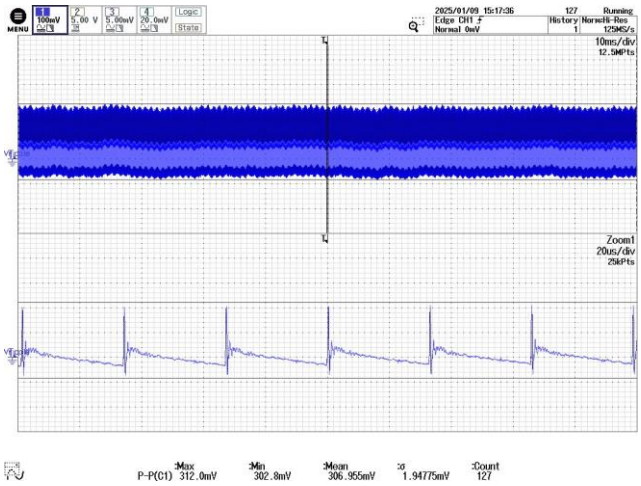


Figure 118 – Output Voltage Ripple.
200 VDC, 1.46 A Load, 25 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 312 mV.

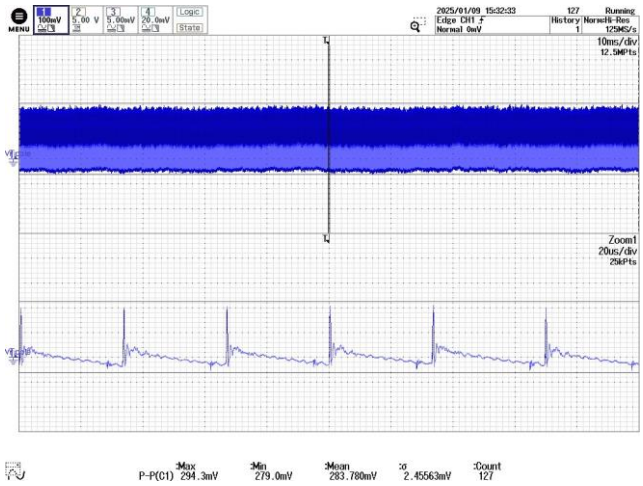


Figure 119 – Output Voltage Ripple.
400 VDC, 1.46 A Load, 25 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 308 mV.

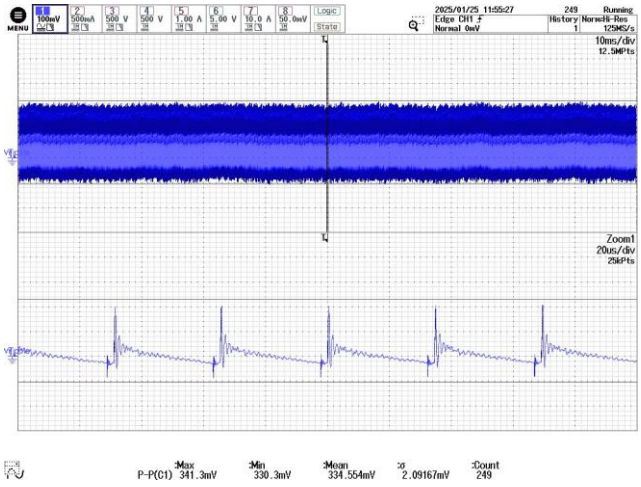


Figure 120 – Output Voltage Ripple.
900 VDC, 1.46 A Load, 25 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 341 mV.

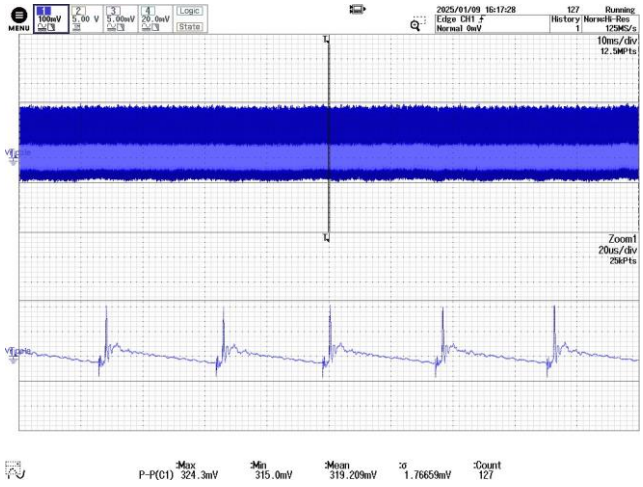


Figure 121 – Output Voltage Ripple.
1000 VDC, 1.46 A Load, 25 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 324 mV.

[34] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at -40 °C Ambient with Constant Full Load[35]

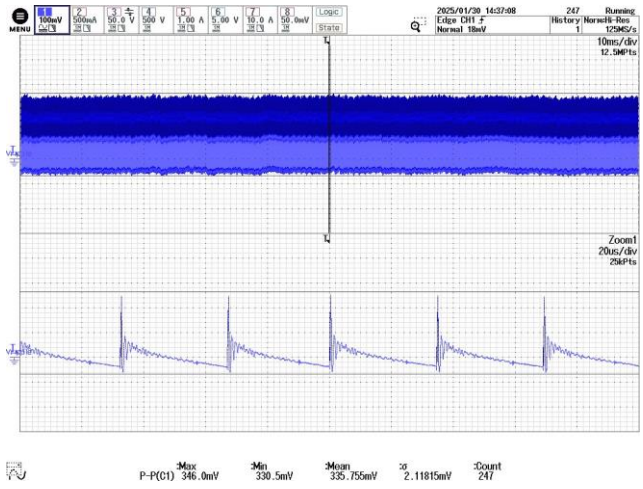


Figure 122 – Output Voltage Ripple.
200 VDC, 1.46 A Load, -40 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 346 mV.

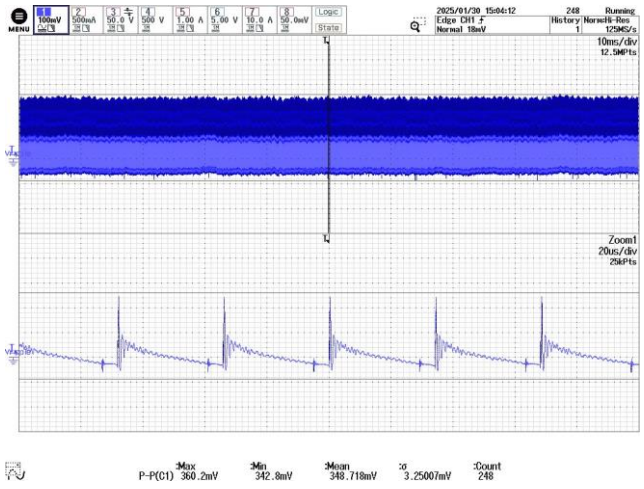


Figure 123– Output Voltage Ripple.
400 VDC, 1.46 A Load, -40 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 426 mV.

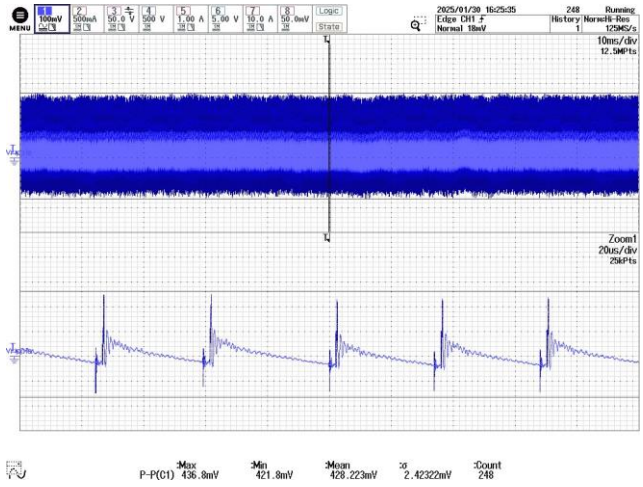


Figure 124 – Output Voltage Ripple.
900 VDC, 1.46 A Load, -40 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 437 mV.

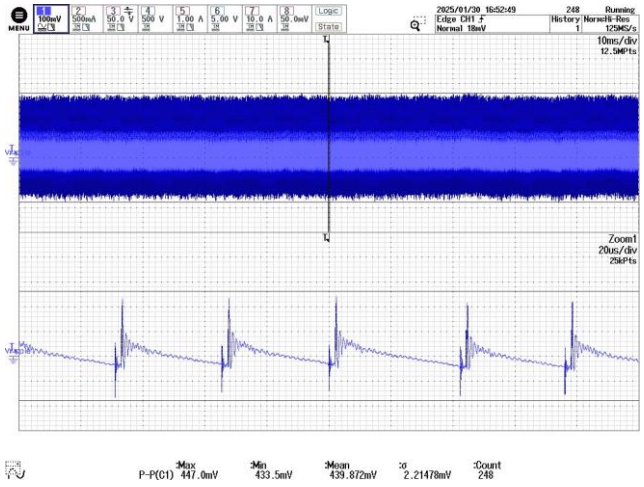


Figure 125 – Output Voltage Ripple.
1000 VDC, 1.46 A Load, -40 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 447 mV.

[35] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C Ambient

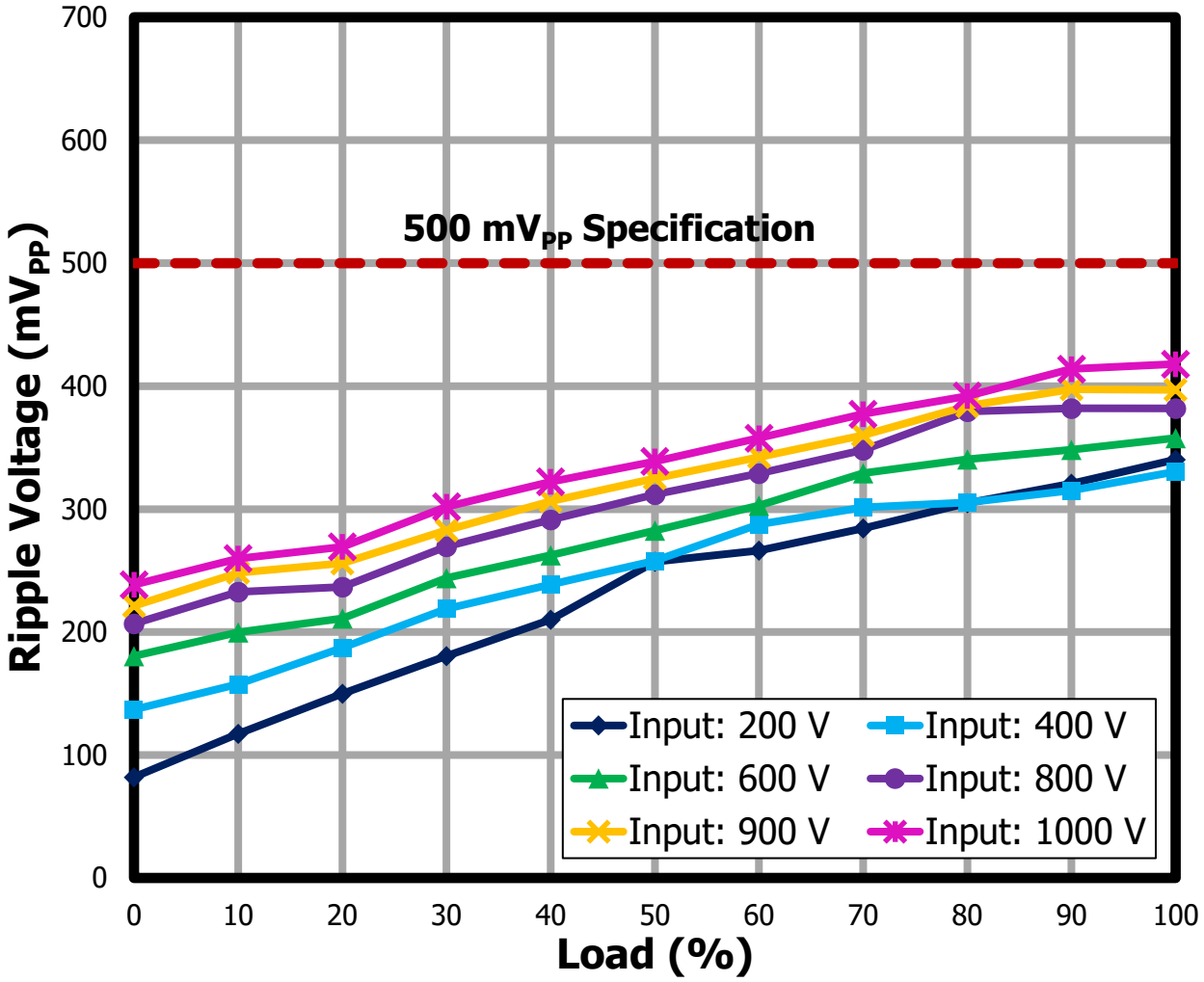


Figure 126 – Output Ripple Voltage Across Load Range (85 °C Ambient).

11.4.3.2 Output Ripple at 25 °C Ambient

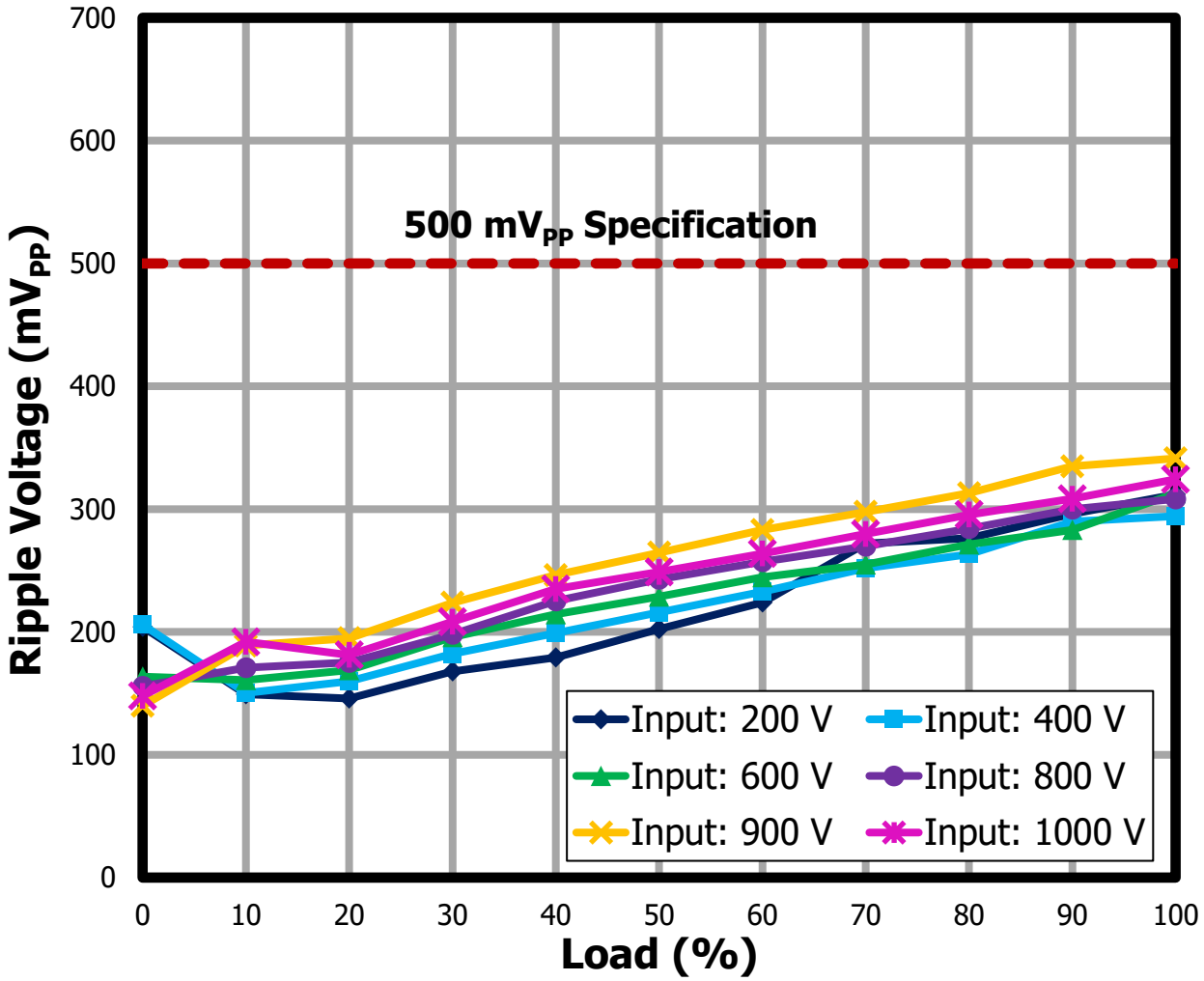


Figure 127 – Output Ripple Voltage Across Load Range (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C Ambient

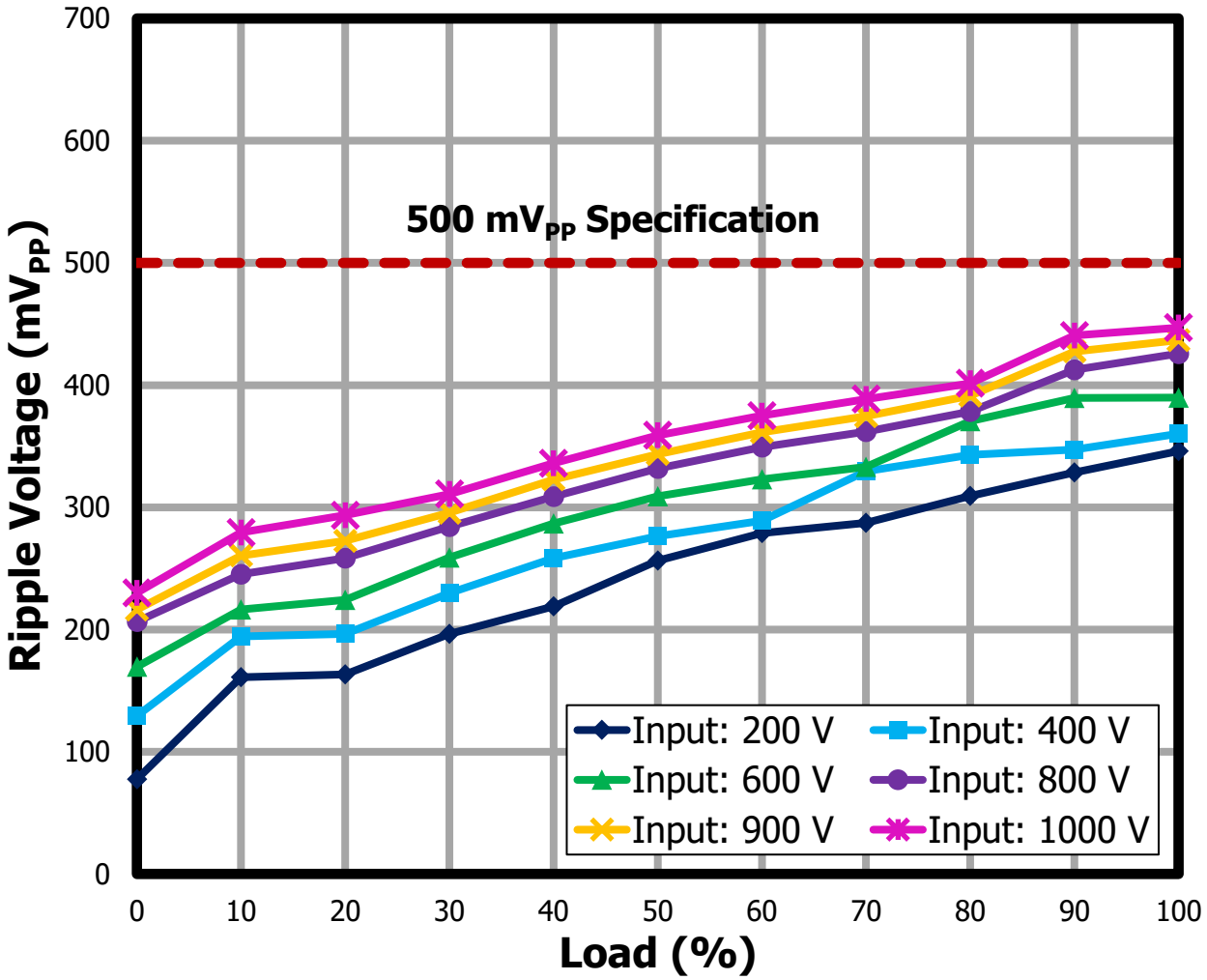


Figure 128 – Output Ripple Voltage Across Load Range (-40 °C Ambient).

12 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before turning on the power supply.The unit was allowed to stabilize for 20 minutes after each change in input voltage. For each load condition, the power supply was allowed to settle for 60 seconds before voltage and current measurements were taken.

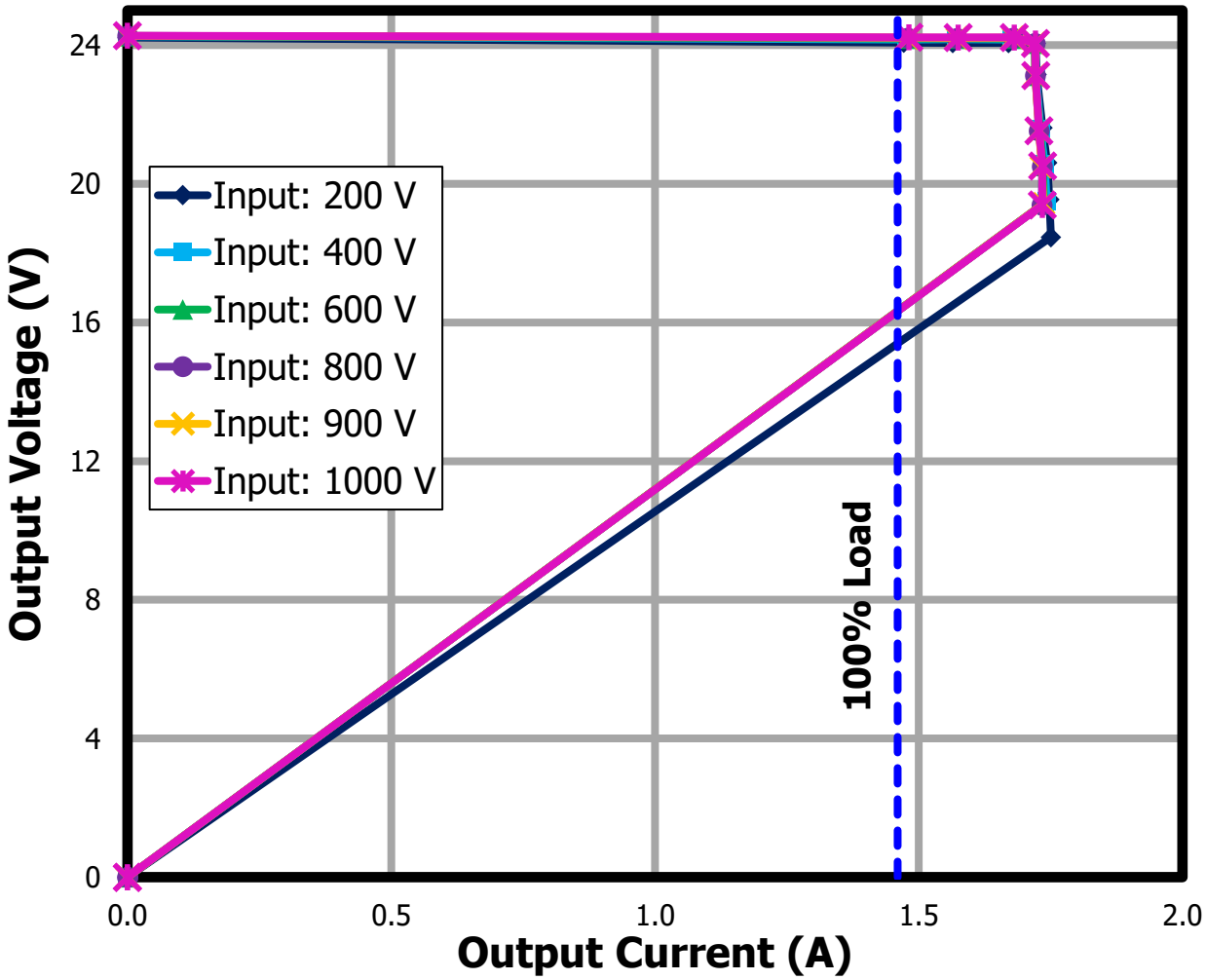


Figure 129 – Output Overload Curve at 85 °C Ambient.

13 Maximum Output Power

13.1 Maximum Output Power at 105 °C Ambient

The power supply was placed in a thermal chamber. The chamber was pre-heated to 105 °C and allowed to stabilize for 30 minutes before the power supply was turned on. To allow component temperatures to settle, the power supply was loaded for 30 minutes before each test. Maximum output power at each given input voltage was determined by finding the maximum loading condition at which the unit did not enter auto-restart (AR) or trigger over-temperature protection. The case temperature of critical components was also monitored.

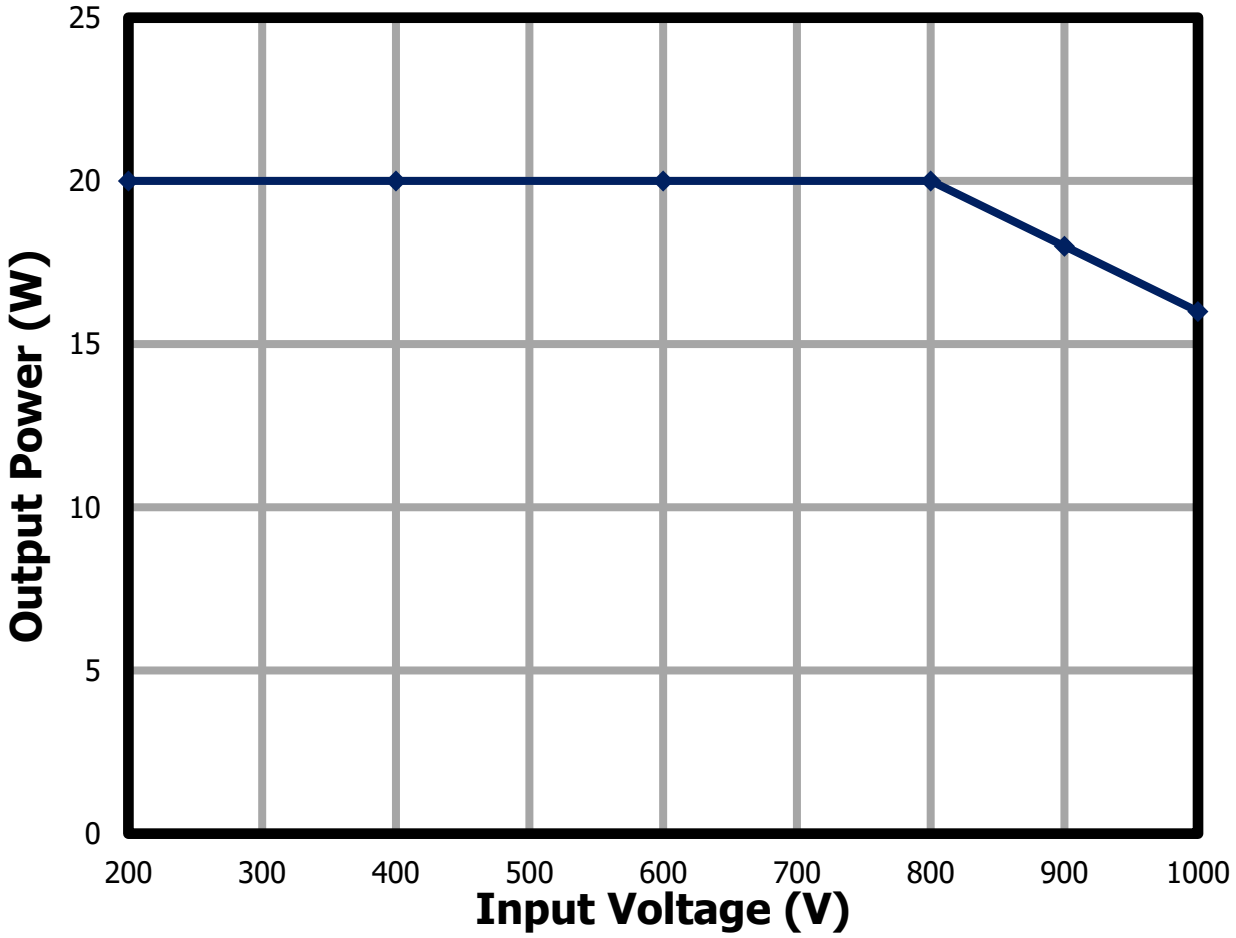


Figure 130 – Maximum Output Power Curve at 105 °C Ambient.

Input Voltage	Maximum Output Power	Limiting Factor	Value
200 V to 800 V	20 W	Primary Snubber Temperature	> 125 °C
900 V	18 W	Primary Snubber Temperature	> 125 °C
1000 V	16 W	InnoSwitch3-AQ Overtemperature Protection	> 125 °C

Table 14 – Limiting factors on Maximum Output Power.

13.2 Maximum Output Power at Low Input Voltage at 105 °C Ambient

The test procedure in Section 13.1 was repeated, but with the ambient temperature set to 85 °C. The maximum output power was measured at voltages lower than 200 V. The maximum output power at each input voltage was defined if the power supply can startup at the load condition without triggering auto-restart (AR), and if the power supply can operate at steady state without triggering AR and overtemperature protection.

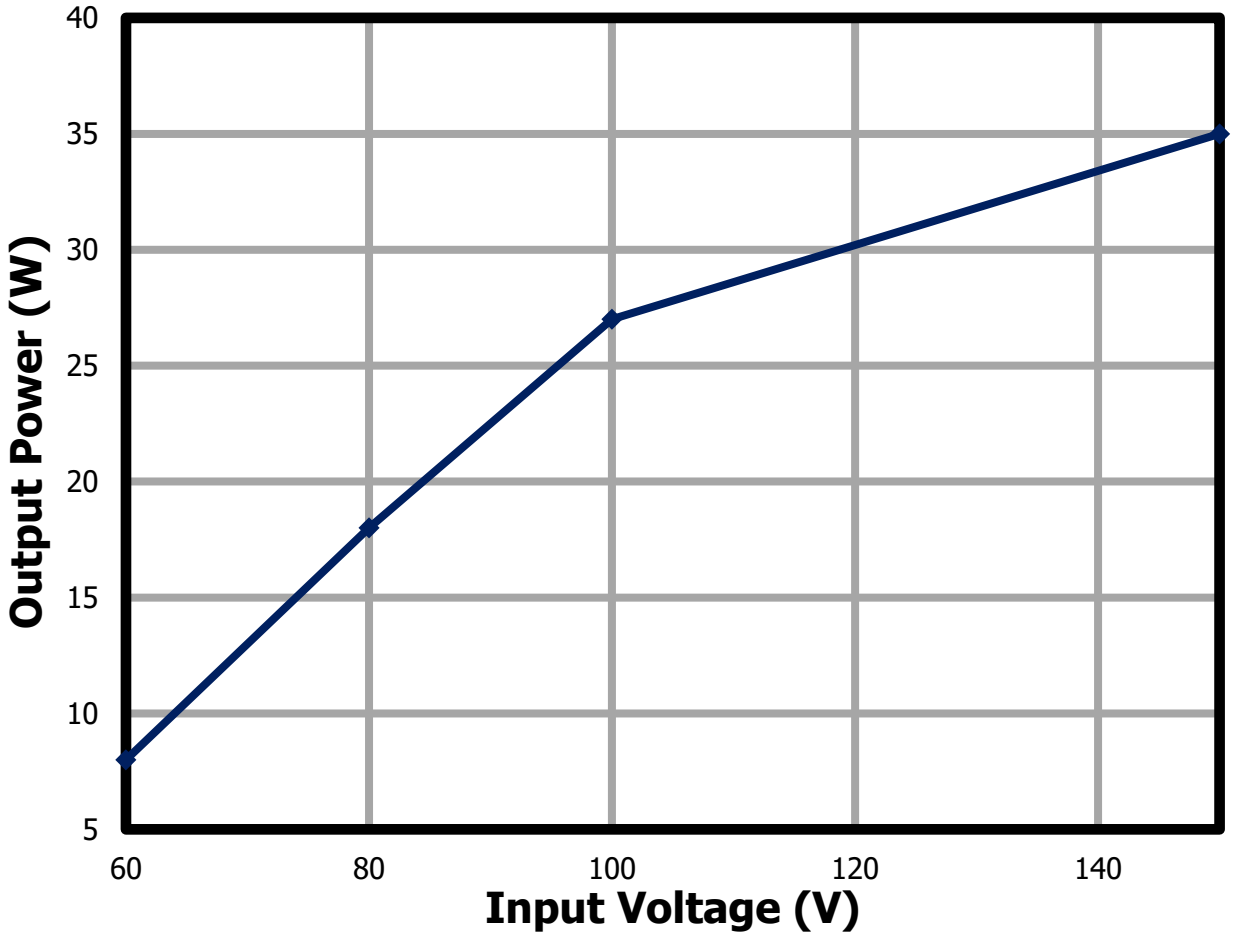


Figure 131– Maximum Output Power Curve Low Input Voltage at 85 °C Ambient.

Input Voltage	Maximum Output Power	Limiting Factor
150 V	35 W	-
100 V	27 W	Full Load Startup
80 V	18 W	Full Load Startup
60 V	8 W	Full Load Startup

Table 15 – Limiting factors on Maximum Output Power.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
24-June-25	VG	A	Initial Release.	Apps & Mktg

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