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## Design Example Report

<b>Title</b>	<i>12 W or 6 W Selectable Output Voltage, 12 V or 6 V, with 1 A Output Current Using LinkSwitch™-XT2SR LNK3773D</i>
<b>Specification</b>	90 VAC – 265 VAC Input; 12 V, 1 A or 6 V, 1 A Output
<b>Application</b>	Single Output Open Frame Appliance Power Supply
<b>Author</b>	Applications Engineering Department
<b>Document Number</b>	DER-998
<b>Date</b>	October 12, 2023
<b>Revision</b>	1.1

### **Summary and Features**

- 12 W or 6 W output from 90 VAC to 265 VAC
- Very low component count switcher solution with SR driver and integrated 3.3 V LDO (uVCC)
- Built-in synchronous rectification for 90% efficiency at nominal AC input
- <5 mW no-load input power at 6 V output 230 VAC
- <190 mW standby input power at 6 V / 30 mA load
- Accurate thermal protection with hysteretic shutdown
- Simple two-winding transformer

### **PATENT INFORMATION**

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.power.com](http://www.power.com). Power Integrations grants its customers a license under certain patent rights as set forth at <https://www.power.com/company/intellectual-property-licensing/>.

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**Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



## 1 Introduction

This engineering report describes a 1 A, 12 V or 1 A, 6 V non-isolated selectable single output embedded power supply utilizing LNK3773D from the LinkSwitch-XT2SR family of ICs.

This design shows the high-power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

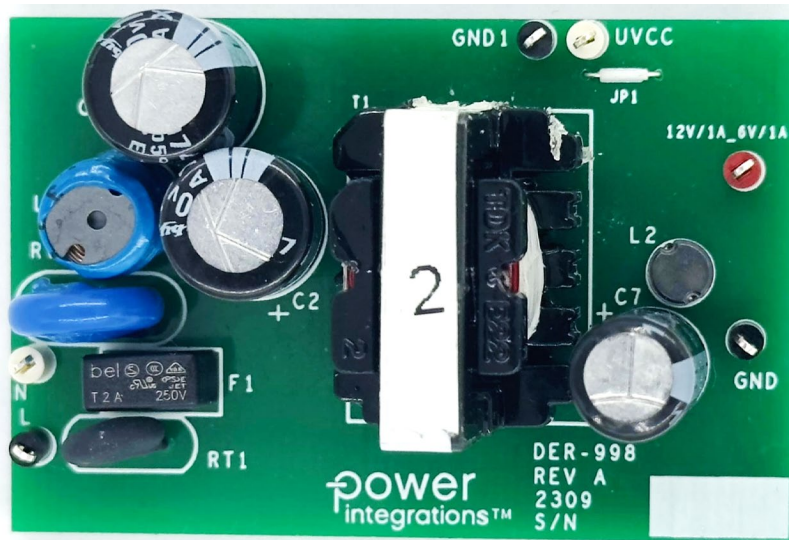


Figure 1 – Populated Circuit Board Photograph, Top.

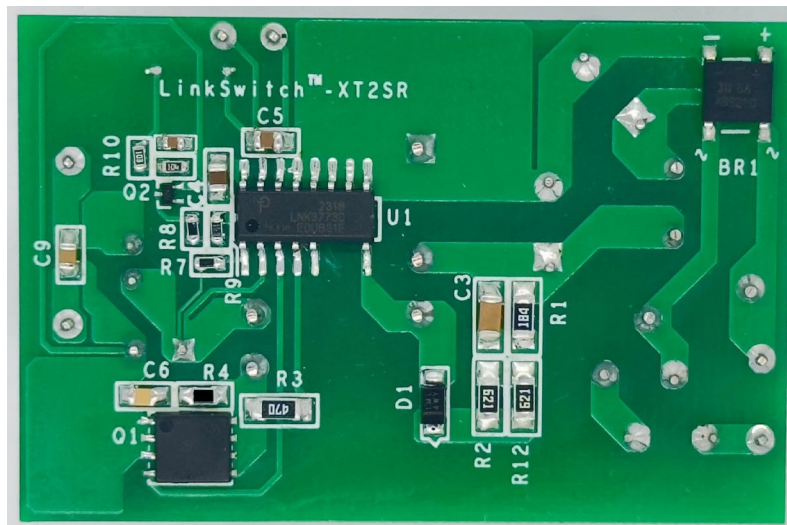


Figure 2 – Populated Circuit Board Photograph, Bottom.

## 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
<b>Input</b>						
Voltage	$V_{IN}$	90	115/230	265	VAC	2 Wire Input.
Frequency	$f_{LINE}$		50/60		Hz	
No-Load Input Power			5		mW	At 6 V Output, 230 VAC Input
Standby Power (6 V / 30 mA)				190	mW	
<b>12 V Output</b>						
Output Voltage 1	$V_{OUT1}$	11.4	12	12.6	V	±5 %
Output Ripple Voltage 1	$V_{RIPPLE1}$		120		mV	Measured at Full load, 20 MHz Bandwidth.
Output Current 1	$I_{OUT1}$	0	1		A	
<b>6 V Output</b>						
Output Voltage 2	$V_{OUT2}$	5.7	6	6.3	V	±5 %,
Output Ripple Voltage 2	$V_{RIPPLE2}$		120		mV	Measured at Full load, 20 MHz Bandwidth.
Output Current 2	$I_{OUT2}$	0	1		A	
<b>uVCC</b>						
uVCC Voltage	$V_{UVCC}$		3.3		V	
uVCC Current	$I_{UVCC}$			20	mA	
<b>Total Output Power</b>						
Continuous Output Power	$P_{OUT}$			12 / 6	W	
<b>Efficiency</b>						
Average	$\eta_{AVE[BRD]}$		90		%	Measured at 115 / 230 VAC, $P_{OUT}$ 25 °C. $V_{IN}$ at 230 VAC.
25%, 50%, 75%, and 100%						
<b>Environmental</b>						
Conducted EMI			Meets CISPR22B / EN55022B Load Floating			
Safety			Designed to meet IEC950, UL1950 Class II			
Surge						
Differential		1			kV	1.2/50 $\mu$ s surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 $\Omega$ .
Common mode Ring Wave		6			kV	100 kHz Ring Wave, 12 $\Omega$ Common Mode.
EFT		2			kV	5 kHz, 15 ms burst time, 120s repetition time, 12 $\Omega$ EFT
						100 kHz, 750 $\mu$ s burst time, 120s repetition time, 12 $\Omega$ EFT
Ambient Temperature	$T_{AMB}$	0		40	°C	Free Convection, Sea Level.



### 3 Schematic

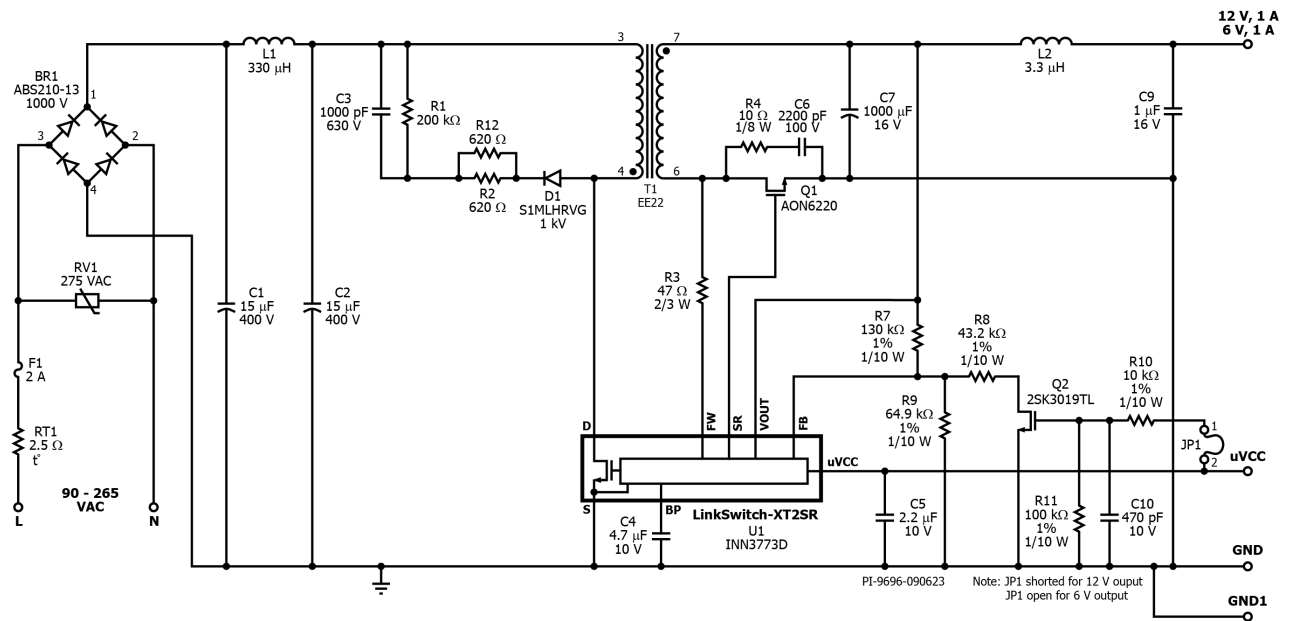


Figure 3 – Schematic.



## 4 Circuit Description

This circuit is a non-isolated single output flyback power supply for appliances using the LinkSwitch-XT2SR IC (U1). Using the optional external feedback pin for the single output design, features a highly efficient design satisfying regulation requirements without a post regulator. This circuit makes use of the synchronous rectifier to improve efficiency.

### 4.1 Input EMI Filtering

Input Fuse F1 isolates the circuit and provides protection against excess input current resulting from catastrophic failure of any of the components in the power supply.

Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of capacitors C1 and C2. The differential inductance of L1 is connected between C1 and C2, forms a pi-filter to attenuate differential mode EMI.

### 4.2 LinkSwitch-XT2SR Primary-Side Circuit

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the LinkSwitch-XT2SR IC (U1)

A low cost R2CD clamp circuit formed by D1, R1, R2, R12 and C3 limits the peak drain voltage at the instant of turn-off of the switch inside U1. The clamp circuit helps to dissipate the energy stored in the leakage inductance of transformer T1 and output traces.

The LinkSwitch-XT2SR IC is self-starting, using an internal high-voltage current source to charge the BP pin capacitor, C4 when AC is first applied. During normal operation the BP regulator is powered from VOUT. The minimum drain voltage at start-up before the IC starts switching is 50 VDC, and VOUT will be used to charge BP when VOUT voltage reaches 0.2 V higher than BP voltage.

### 4.3 LinkSwitch-XT2SR Secondary-Side Circuit

The controller of the LinkSwitch-XT2SR IC provides output voltage sensing and drives to a switch providing synchronous rectification.

The secondary winding of the transformer is rectified by SR FET Q1. Very Low ESR capacitor C7 and ceramic capacitor C9 with L2, provide filtering and significantly attenuates high frequency ripple and noise. RC snubber network comprising of R4 and C6 damp high frequency ringing across the SR FET during switching transients that would otherwise create radiated EMI.

Synchronous rectification (SR) is provided by switch Q1. Switch Q1 is turned on by the controller inside IC U1, based on the winding voltage sensed via resistor R3 and current fed into FORWARD pin of the IC.

In continuous conduction mode operation, the SR FET is turned off just prior to the controller commanding a new switching cycle. In discontinuous mode the SR FET is turned off when the voltage drop across the MOSFET falls below a threshold ( $V_{SR(TH)}$ ). The controller ensures that it is never on simultaneously with the synchronous rectification MOSFET.

External feedback circuit consisting of components R7, R8, R9, R10, R11, C10 and Q2 allows to select either 12 V or 6 V output voltage. Resistors R7, R8 and R9 form an external voltage divider network that senses the output voltage for better cross-regulation. Output voltage selector circuit comprising of Q2, R10, R11 and C10 adjust the effective value of the lower feedback resistor depending on the connection of JP1. When JP1 is connected to  $\mu$ VCC, the effective lower feedback resistance will be the equivalent resistance of R8 & R9 resistors in parallel and the output voltage will be 12 V. When JP1 is disconnected to  $\mu$ VCC, the effective lower feedback resistance will be R9, and the output voltage will be 6 V. The LinkSwitch-XT2SR IC has an internal reference of 2.0 V.

There is a 3.3 V  $\mu$ VCC output with C5 decoupling capacitor, which can deliver up to 20 mA maximum current.

## 5 PCB Layout

Layers: One (1)  
 Board Material: FR4  
 Board Thickness: 0.062"  
 Copper Weight: 2 oz (2.8 mils / 71 μm) unless otherwise stated.

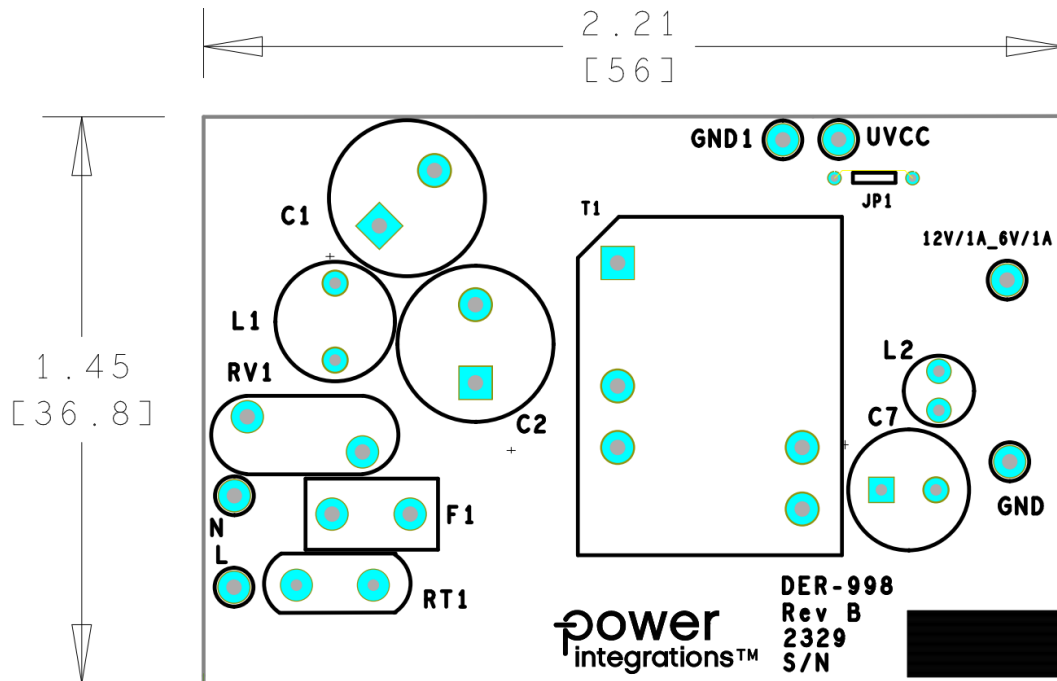


Figure 4 – Printed Circuit Layout, Top.

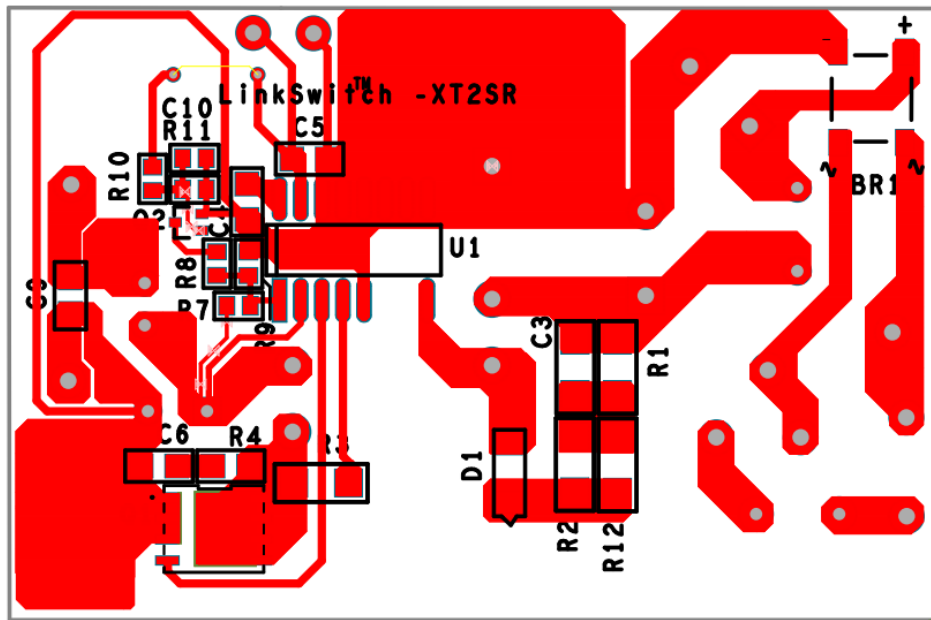


Figure 5 – Printed Circuit Layout, Bottom.

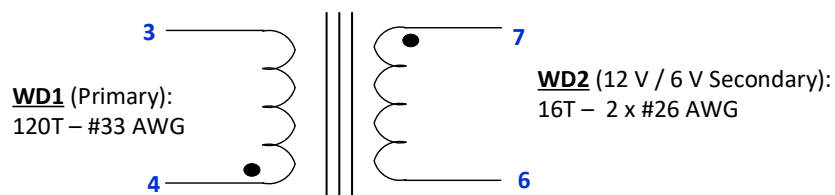
## 6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 2 A, Bridge Rectifier, SMD, 4SOPA	ABS210-13	Diodes, Inc.
2	2	C1 C2	15 $\mu$ F, $\pm$ 20%, 400 V, Electrolytic, (10 x 16)	UVC2G150MPD	Nichicon
3	1	C3	1000 pF, $\pm$ 10%, 630 V, Ceramic, X7R, 1206	C1206C102KBRACU	Kemet
4	1	C4	4.7 $\mu$ F, $\pm$ 10%, 10 V, Ceramic, X7R 0805	LMK212B7475KGHT	Taiyo Yuden
5	1	C5	2.2 $\mu$ F, $\pm$ 20%, 10 V, Ceramic, X7R, 0805	C0805C225M8RACTU	Kemet
6	1	C6	2200 pF, $\pm$ 10%, 100V, Ceramic X7R, 0805	CC0805KRX7R0BB222	Yageo
7	1	C7	1000 $\mu$ F, $\pm$ 20%, 16 V, Electrolytic, Low ESR, (8 x 20)	EEU-FR1C102LB	Panasonic
8	1	C9	1 $\mu$ F, $\pm$ 10%, 16V, X7R, 0805	GRM21BR71C105KA01K	Murata
9	2	C10	470 pF, $\pm$ 10%, 25V, Ceramic Capacitor, X7R, 0603	885012206057	Würth
10	1	D1	1000 V, 1 A, Diode, General Purpose, SMT, SUB SMA	S1MLHRVG	Taiwan Semi
11	1	F1	2 A, 250 V, Fuse, Slow, Long Time Lag, RST	RST 2	Belfuse
12	1	L1	330 $\mu$ H, Unshielded Drum Core, Wirewound Inductor, 0.55 A, 720 m $\Omega$ Max, Radial 9 x 11.5 mm	SBC3-331-551	Tokin
13	1	L2	3.3 $\mu$ H, Unshielded Drum Core, Wirewound Inductor, 2.3 A, 37 m $\Omega$ Max, Radial, Vertical Cylinder (Open)	SBCP-47HY3R3B	Kemet
14	1	Q1	MOSFET, N-CH, 100V, 48A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
15	1	Q2	MOSFET, N-CH, 30 V, .1 A, SOT416	2SK3019TL	Rohm Semi
16	1	R1	RES, 200 k $\Omega$ , 5%, 2/3 W, Thick Film, 1206	ERJ-P08J204V	Panasonic
17	1	R2 R12	RES, 620 $\Omega$ , 5%, 2/3 W, Thick Film, 1206	ERJ-P08J621V	Panasonic
18	1	R3	RES, 47 $\Omega$ , 5%, 2/3 W, Thick Film, 1206	ERJ-P08J470V	Panasonic
19	1	R4	RES, 10 $\Omega$ , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
20	1	R7	RES, 130 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1303V	Panasonic
21	1	R8	RES, 43.2 k $\Omega$ , 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF4322V	Panasonic
22	1	R9	RES, 64.9 k $\Omega$ , 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF6492V	Panasonic
23	1	R10	RES, 10 k $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
24	1	R11	RES, 100 k $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
25	1	RT1	NTC Thermistor, 2.5 $\Omega$ , 3 A	SL08 2R503	Ametherm
26	1	RV1	275 Vac, 43 J, 10 mm, RADIAL	S10K275	Epcos
27	1	T1	Bobbin, EE22. Vertical, 10 pins	BE-22-1110CPFR	TDK
28	1	U1	LinkSwitch-XT2SR2, SO-16B, High voltage	LNK3773D	Power Integrations
29	1	12V/1A_6 V/1A	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
30	1	GND GND1 L	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
31	1	JP1	Wire Jumper, Insulated, 28 AWG, 0.2 in	2842/1 WH005	Alpha Wire
32	4	N UVCC	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone



## 7 Transformer (T1) Specification

### 7.1 Electrical Diagram



**Figure 6** – Transformer Electrical Diagram.

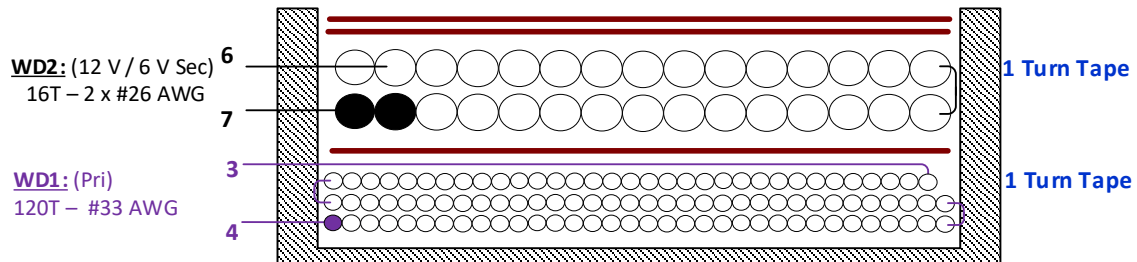
### 7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V <sub>PK-PK</sub> , 100 kHz switching frequency, between pin 3 and 4, with all other windings open.	2393 $\mu$ H $\pm$ 10%
Primary Leakage Inductance	Between pin 3 and 4, with secondary pins: 6 & 7 shorted.	16 $\mu$ H (Max).

### 7.3 Material List

Item	Description
[1]	Core: EE22, 3F3 or Equivalent, Gapped
[2]	Bobbin: EE22-V-10 pins
[3]	Magnet Wire: #33 AWG, Double Coated.
[4]	Magnet Wire: #26 AWG, Double Coated.
[5]	Barrier Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 8.4 mm Width.
[6]	Barrier Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 5.0 mm Width.
[7]	Varnish: Dolph BC-359.

## 7.4 Transformer Build Diagram

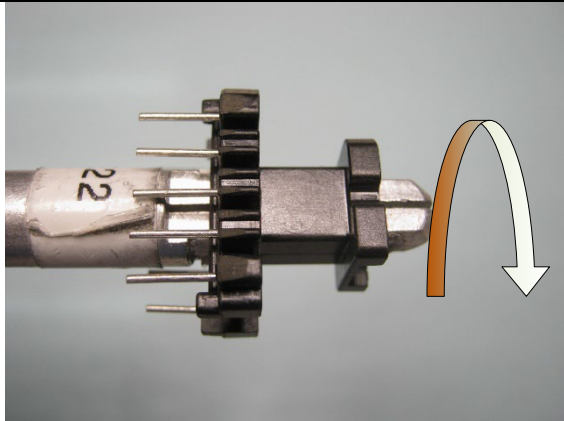
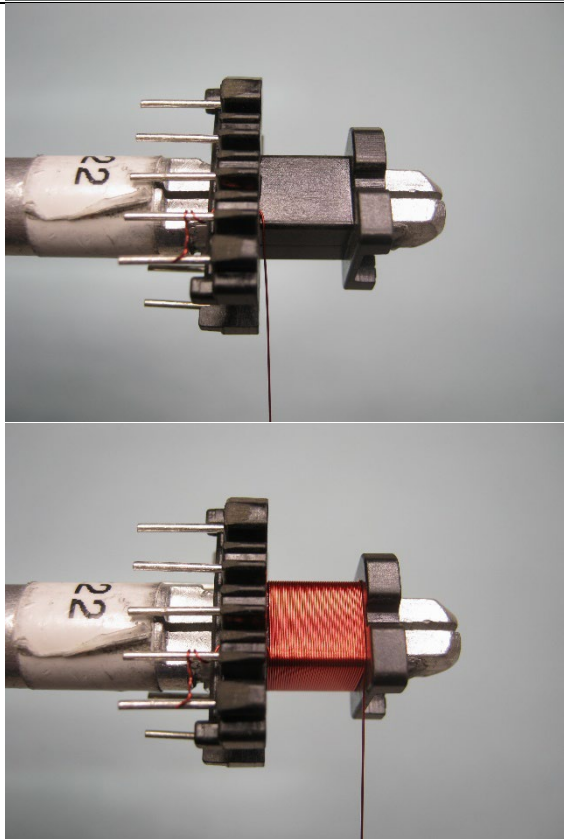


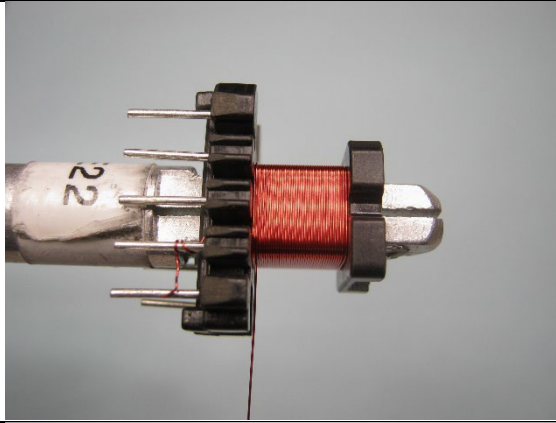
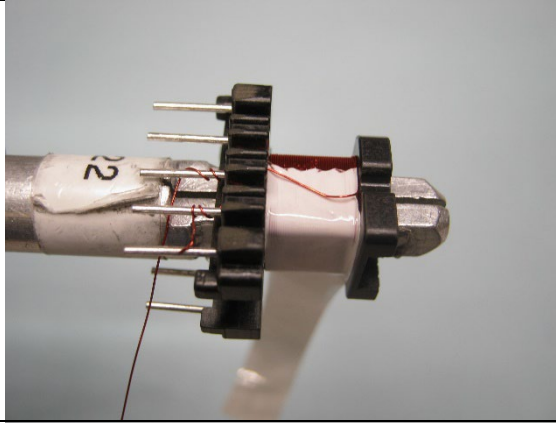
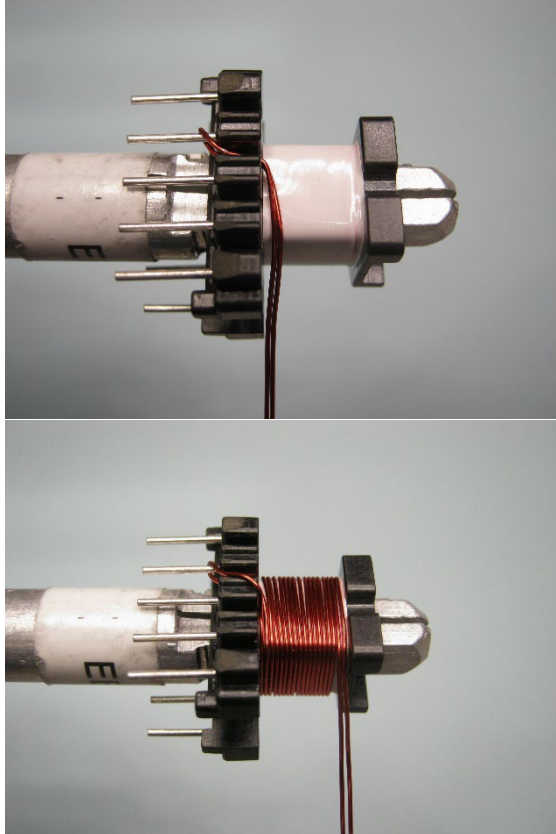
**Figure 7 – Transformer Electrical Diagram.**

## 7.5 Winding Instructions

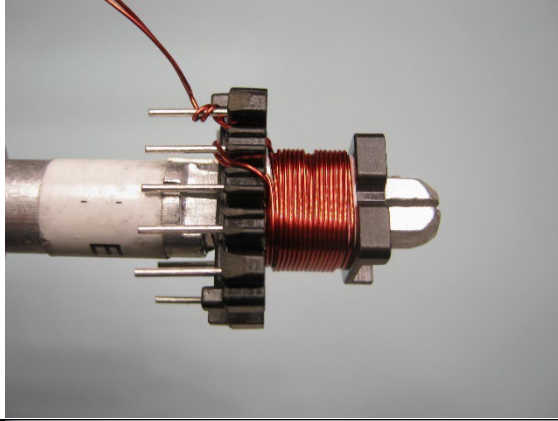
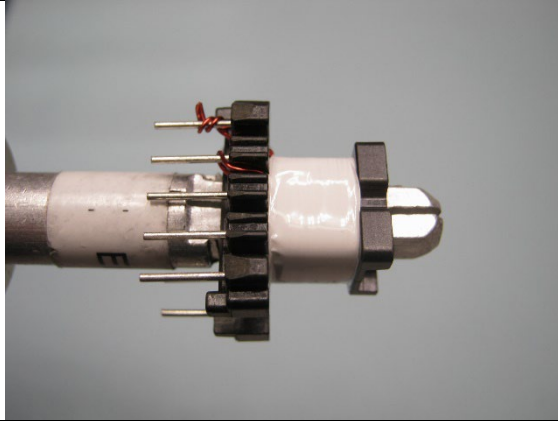
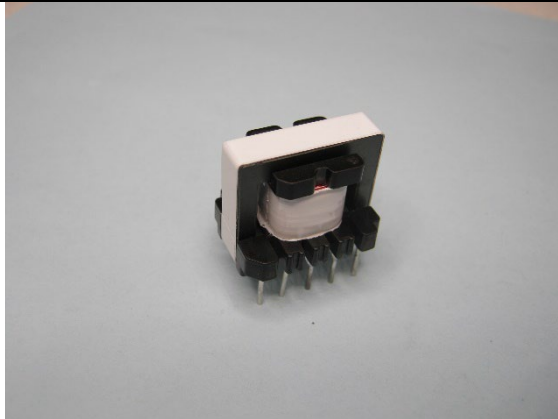
<b>Winding Preparation</b>	Position the bobbin Item [2] on the mandrel such that the primary-side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
<b>WD1 Primary</b>	Start at pin 4, wind 120 turns of wire Item [3] in 3 layers, with tight tension, from left to right and right to left. At the last turn, terminate the wire at pin 3.
<b>Insulation</b>	1 layer of tape Item [5].
<b>WD2 Secondary</b>	Start from pin 7, use 2 wires Item [4], wind 16 bifilar turns from right to left and right to left. At the last turn, terminate at pin 6.
<b>Insulation</b>	2 layer of tape Item [5] to secure all windings
<b>Finish</b>	Gap core halves to get 2393 $\mu$ H and secure with tape Item [6]. Varnish with Item [7].

**7.7 Winding Illustrations**

<p><b>Winding Preparation</b></p>		<p>Position the bobbin Item [2] on the mandrel such that the primary-side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.</p>
<p><b>WD1 Primary</b></p>		<p>Start at pin 4, wind 120 turns of wire Item [3] in 3 layers, with tight tension, from left to right and right to left. At the last turn, terminate the wire at pin 3.</p>

		
<p><b>`Insulation</b></p>		<p>1 layer of tape Item [5].</p>
<p><b>WD2 Secondary</b></p>		<p>Start from pin 7, use 2 wires Item [4], wind 16 bifilar turns from right to left and right to left. At the last turn, terminate at pin 6.</p>



		
<p><b>Insulation</b></p>		<p>2 layer of tape Item [5] to secures all windings</p>
<p><b>Finish</b></p>		<p>Gap core halves to get 2393 <math>\mu</math>H and secure with tape Item [6]. Varnish with Item [7].</p>

## 7.8 Transformer Design Spreadsheet

ACDC_LinkSwitchXT2SR_Flyback_081623; Rev.1.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch-XT2SR Flyback Design Spreadsheet
<b>APPLICATION VARIABLES</b>					
LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
VACMIN			90.00	V	Minimum AC line voltage
VACMAX			265.00	V	Maximum AC line voltage
fL			60.00	Hz	AC mains frequency
LINE RECTIFICATION TYPE	F		F		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
VOUT	12.00		12.00	V	Output voltage
IOUT	1.000		1.000	A	Average output current
EFFICIENCY (User Estimate)			0.80		Overall efficiency estimate
LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the primary switch off-state to the total system losses
POUT			12.00	W	Continuous output power
CIN	30.00		30.00	uF	Input capacitor
VMIN			99.77	V	Valley voltage of the rectified minimum AC line voltage
VMAX			374.77	V	Peak voltage of the maximum AC line voltage
FEEDBACK	EXTERNAL		EXTERNAL		Feedback type: select either "INTERNAL" or "EXTERNAL"
INPUT STAGE RESISTANCE			10.0	Ohms	Input stage resistance (includes thermistor, filtering components, etc)
PLOSS_INPUTSTAGE			0.226	W	Maximum input stage power loss
<b>LINKSWITCH-XT2 VARIABLES</b>					
DEVICE SERIES	LNK3773D		LNK3773D		Generic LinkSwitch-XT2SR device code
POUT_MAX			12	W	Power capability of the device based on thermal performance
ILIMITMIN			0.478	A	Minimum current limit of the device
ILIMITTYP			0.514	A	Typical current limit of the device
ILIMITMAX			0.550	A	Maximum current limit of the device
RDSON			6.85	Ohms	Switch on-state drain-to-source resistance at 100 degC
FSMIN			62000	Hz	Minimum switching frequency
FSTYP			66000	Hz	Typical switching frequency
FSMAX			70000	Hz	Maximum switching frequency
BVDSS			725	V	Device breakdown voltage
<b>PRIMARY WAVEFORM PARAMETERS</b>					
OPERATION MODE			CCM		Continuous mode of operation
VOR	90.0		90.0	V	Voltage reflected across the primary winding when the primary switch is off
VDSON			2.00	V	Primary switch on-time drain-to-source voltage
VDSOFF			534.8	V	Primary switch off-time drain-to-source voltage stress
KRP/KDP			0.661		Degree on how much the operation tend to be continuous or discontinuous
KP_TRANSIENT			0.302		KP value under transient conditions
DUTY			0.479		Maximum duty cycle
TIME_ON_MIN			2.762	us	Primary switch minimum on-time
IPEAK_PRIMARY			0.550	A	Maximum primary peak current
IPED_PRIMARY			0.162	A	Maximum primary pedestal current
IAVG_PRIMARY			0.153	A	Maximum primary average current
IRMS_PRIMARY			0.240	A	Maximum root-mean-squared value of the primary current
PLOSS_SWITCH			0.511	W	Maximum primary switch power loss



THERMAL RESISTANCE OF SWITCH			95	degC/W	Net thermal resistance of primary switch
T_RISE_SWITCH			48.5	degC	Maximum temperature rise of the switch in degrees Celsius
LPRIMARY_MIN			2154	uH	Minimum primary inductance
LPRIMARY_TYP			2393	uH	Typical primary inductance
LPRIMARY_MAX			2633	uH	Maximum primary inductance
LPRIMARY_TOL			10	%	Primary inductance tolerance
<b>SECONDARY WAVEFORM PARAMETERS</b>					
IPEAK_SECONDARY			4.125	A	Peak secondary current
IRMS_SECONDARY			1.875	A	Maximum root-mean-squared value of the secondary current
IRIPPLE_SECONDARY			4.125	A	Maximum ripple value of the secondary current
PIV_SECONDARY			61.7	V	Peak inverse voltage of the secondary rectifier
VF_SECONDARY	0.10		0.10	V	Forward voltage drop of the secondary rectifier
<b>TRANSFORMER CONSTRUCTION PARAMETERS</b>					
CORE	EE22		EE22		Select the transformer core
CODE CODE			PC40EE22-Z		Core code
BOBBIN			B-EE22-H		Core code
AE			41.00	mm <sup>2</sup>	Cross-sectional area of the core
LE			39.60	mm	Effective magnetic path length of the core
AL			1610.0	nH/(T <sup>2</sup> )	Ungapped effective inductance of the core
VE			1620.0	mm <sup>3</sup>	Effective volume of the core
AW			20.00	mm <sup>2</sup>	Window area of the bobbin
BW			8.45	mm	Width of the bobbin
MLT			32.40	mm	Mean length per turn of the bobbin
MARGIN			0.00	mm	Safety margin
Primary Winding					
NPRIMARY			120	turns	Primary winding number of turns
BMAX			2943	Gauss	Actual value of magnetic flux density (BMAX_TARGET = 3000 Gauss)
BAC			1471	Gauss	AC flux density
ALG			166	nH/(T <sup>2</sup> )	Gapped core effective inductance
LG			0.278	mm	Core gap length
Secondary Winding					
NSECONDARY	16		16	turns	Secondary winding number of turns
<b>FEEDBACK PARAMETERS</b>					
VFBRATIO			1.00		Output voltage feedback priority ratio. Eg. Ratio of 0.8 implies that VOUT1 has an 80% feedback priority.
RUPPER1			130000	Ohms	FB pin upper resistor connected to VOUT1
RUPPER2			N/A	Ohms	FB pin upper resistor connected to VOUT2
RLOWER	25936		25936	Ohms	FB pin (Lower) Resistor
<b>MULTIPLE OUTPUT PARAMETERS</b>					
Output 1 (SRFET)					
VOUT1			12.00	V	Output voltage 1
IOUT1	1.000		1.000	A	Output current 1
POUT1			12.00	W	Output power 1
VD1			0.70	V	Forward voltage drop of SRFET for output 1
NS1			17	turns	Number of turns for output 1
ISPEAK1			3.88	A	Instantaneous peak value of the secondary current for output 1



ISRMS1			1.875	A	Root-mean-squared value of the secondary current for output 1
ISRIPPLE1			3.882	A	Current ripple on the secondary current waveform for output 1
PIV1			81.0	V	Computed peak inverse voltage stress on the secondary SRFET for output 1
OUTPUT_RECTIFIER1	AON6220		AON6220		Selected SRFET for output 1
VRRM1			100	V	Maximum repetitive peak reverse voltage of the SRFET for output 1
TRR1			32	ns	Reverse recovery time of the SRFET for output 1
IFM1			48.00	A	Maximum forward continuous current of the SRFET of output 1
PLOSS_SRFET1			0.511	W	Maximum SRFET power loss for output 1
VOUT1_RIPPLE			120	mV	Output voltage ripple for output 1
ESR_COUT1			31	mOhms	Equivalent series resistance of the output capacitor for output 1
IRMS_COUT1			1.586	A	Root-mean-squared value of the output capacitor current for output 1
PLOSS_COUT1			0.078	W	Maximum output capacitor power loss for output 1



## 8 Performance Data

### 8.1 Average Efficiency

Note: Measured across PCB output terminals.

#### 8.1.1 12 V Output

Requirement	
Average	<b>82.96% (DOE6) 83.26% (CoC II)</b>
10%	<b>73.26% (CoC II)</b>

##### 8.1.1.1 115 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

% Load	$P_{\text{IN}}$ (W)	$12V_{\text{OUT}}$ (V <sub>DC</sub> )	$12I_{\text{OUT}}$ (A <sub>DC</sub> )	$12P_{\text{OUT}}$ (W)	Efficiency (%)	Average Efficiency (%)
100%	13.19	11.88	1.0	11.87	90.00	
75%	9.80	11.90	0.75	8.91	90.98	
50%	6.54	11.92	0.5	5.94	90.84	
25%	3.26	11.91	0.25	2.95	90.27	<b>90.12</b>
10%	1.29	11.96	0.1	1.15	<b>89.29</b>	

##### 8.1.1.2 230 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

% Load	$P_{\text{IN}}$ (W)	$12V_{\text{OUT}}$ (V <sub>DC</sub> )	$12I_{\text{OUT}}$ (A <sub>DC</sub> )	$12P_{\text{OUT}}$ (W)	Efficiency (%)	Average Efficiency (%)
100%	13.08	11.89	1.0	11.88	90.85	
75%	9.74	11.92	0.75	8.93	91.70	
50%	6.53	11.92	0.5	5.93	90.92	
25%	3.32	11.95	0.25	2.96	89.17	<b>90.27</b>
10%	1.31	11.96	0.1	1.15	<b>87.83</b>	

##### 8.1.1.3 115 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

% Load	$P_{\text{IN}}$ (W)	$12V_{\text{OUT}}$ (V <sub>DC</sub> )	$12I_{\text{OUT}}$ (A <sub>DC</sub> )	$12P_{\text{OUT}}$ (W)	$3.3V_{\text{OUT}}$ (V <sub>DC</sub> )	$3.3P_{\text{OUT}}$ (W)	$P_{\text{OUT-Total}}$ (W)	Eff (%)	Ave Eff (%)
100%	13.48	11.87	1.0	11.86	3.26	0.067	11.93	88.49	
75%	10.08	11.89	0.75	8.91	3.26	0.067	8.98	89.03	
50%	6.79	11.92	0.5	5.93	3.26	0.067	6.00	88.42	
25%	3.54	11.90	0.25	2.94	3.26	0.067	3.01	85.05	<b>87.75</b>
10%	1.57	11.96	0.1	1.15	3.26	0.067	1.22	<b>77.54</b>	

8.1.1.4 230 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

% Load	$P_{\text{IN}}$ (W)	$12V_{\text{OUT}}$ (V <sub>DC</sub> )	$12I_{\text{OUT}}$ (A <sub>DC</sub> )	$12P_{\text{OUT}}$ (W)	$3.3V_{\text{OUT}}$ (V <sub>DC</sub> )	$3.3P_{\text{OUT}}$ (W)	$P_{\text{OUT-Total}}$ (W)	Eff (%)	Ave Eff (%)
100%	13.38	11.89	1.0	11.88	3.26	0.067	11.95	89.32	
75%	10.02	11.91	0.75	8.92	3.26	0.067	8.99	89.77	
50%	6.81	11.93	0.5	5.94	3.26	0.067	6.01	88.27	
25%	3.60	11.94	0.25	2.96	3.26	0.067	3.02	83.92	<b>87.82</b>
10%	1.61	11.95	0.1	1.15	3.26	0.067	1.22	<b>75.99</b>	

## 8.1.2 6 V Output

Requirement	
Average	<b>75% (DOE6) 75.83% (CoC II)</b>
10%	<b>65.98% (CoC II)</b>

8.1.2.1 115 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

% Load	$P_{\text{IN}}$ (W)	$6V_{\text{OUT}}$ (V <sub>DC</sub> )	$6I_{\text{OUT}}$ (A <sub>DC</sub> )	$6P_{\text{OUT}}$ (W)	Efficiency (%)	Average Efficiency (%)
100%	6.56	5.91	1.0	5.91	90.06	
75%	4.89	5.93	0.75	4.44	90.83	
50%	3.25	5.94	0.5	2.96	91.02	
25%	1.62	5.97	0.25	1.48	90.90	<b>90.70</b>
10%	0.64	5.97	0.1	0.58	90.55	

8.1.2.2 230 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

% Load	$P_{\text{IN}}$ (W)	$6V_{\text{OUT}}$ (V <sub>DC</sub> )	$6I_{\text{OUT}}$ (A <sub>DC</sub> )	$6P_{\text{OUT}}$ (W)	Efficiency (%)	Average Efficiency (%)
100%	6.566	5.92	1.0	5.92	90.15	
75%	4.942	5.95	0.75	4.46	90.16	
50%	3.334	5.95	0.5	2.96	88.84	
25%	1.668	5.97	0.25	1.48	88.54	<b>89.42</b>
10%	0.655	5.97	0.1	0.58	87.85	

8.1.2.3 115 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

% Load	$P_{\text{IN}}$ (W)	$6V_{\text{OUT}}$ (V <sub>DC</sub> )	$6I_{\text{OUT}}$ (A <sub>DC</sub> )	$6P_{\text{OUT}}$ (W)	$3.3V_{\text{OUT}}$ (V <sub>DC</sub> )	$3.3P_{\text{OUT}}$ (W)	$P_{\text{OUT-Total}}$ (W)	Eff (%)	Ave Eff (%)
100%	6.72	5.92	1.0	5.91	3.26	0.067	5.98	88.92	
75%	5.04	5.93	0.75	4.44	3.26	0.067	4.51	89.53	
50%	3.39	5.94	0.5	2.96	3.26	0.067	3.02	89.09	
25%	1.77	5.97	0.25	1.48	3.26	0.067	1.54	87.41	<b>88.74</b>
10%	0.78	5.97	0.1	0.58	3.26	0.067	0.64	82.82	



8.1.2.4 230 VAC Input ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

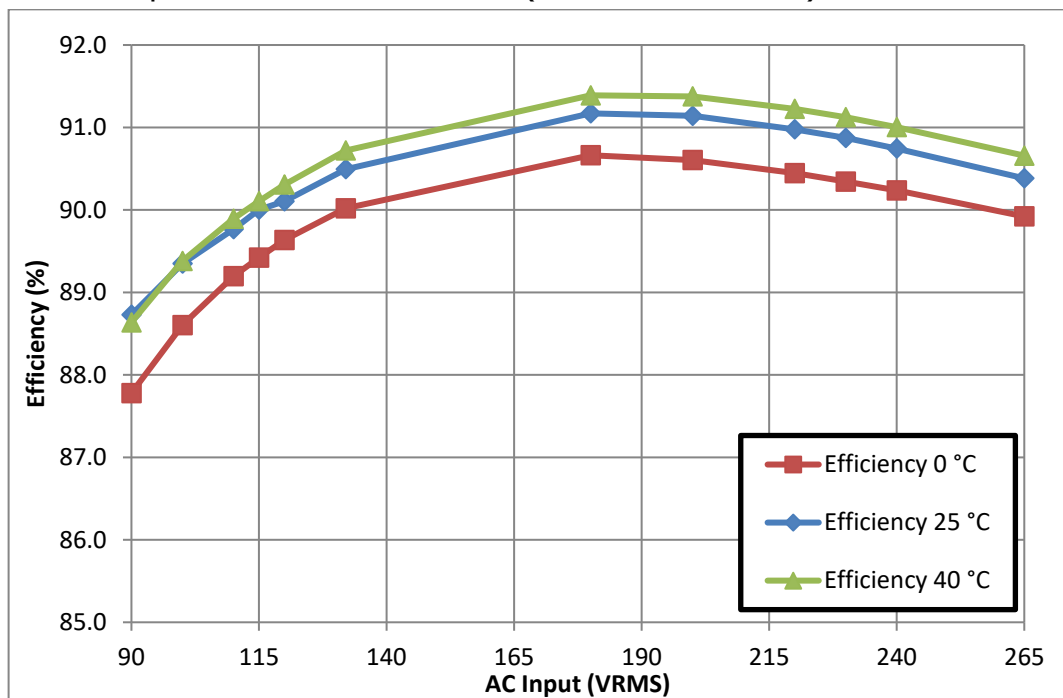
% Load	$P_{\text{IN}}$ (W)	$6V_{\text{OUT}}$ (V <sub>DC</sub> )	$6I_{\text{OUT}}$ (A <sub>DC</sub> )	$6P_{\text{OUT}}$ (W)	$3.3V_{\text{OUT}}$ (V <sub>DC</sub> )	$3.3P_{\text{OUT}}$ (W)	$P_{\text{OUT-Total}}$ (W)	Eff (%)	Ave Eff (%)
100%	6.71	5.92	1.0	5.91	3.26	0.067	5.98	89.20	
75%	5.08	5.94	0.75	4.45	3.26	0.067	4.52	88.94	
50%	3.48	5.95	0.5	2.96	3.26	0.067	3.03	87.11	
25%	1.82	5.97	0.25	1.48	3.26	0.067	1.54	85.09	<b>87.59</b>
10%	0.80	5.97	0.1	0.58	3.26	0.067	0.64	80.21	

## 8.2 Full Load Efficiency vs. Line

Note: A thermal chamber is used to increase/decrease the ambient temperature. Unit is placed inside a box to prevent air flow.

Test Condition: Soak for 15 minutes and 5 minutes for each line / step. Measured across PCB output terminals.

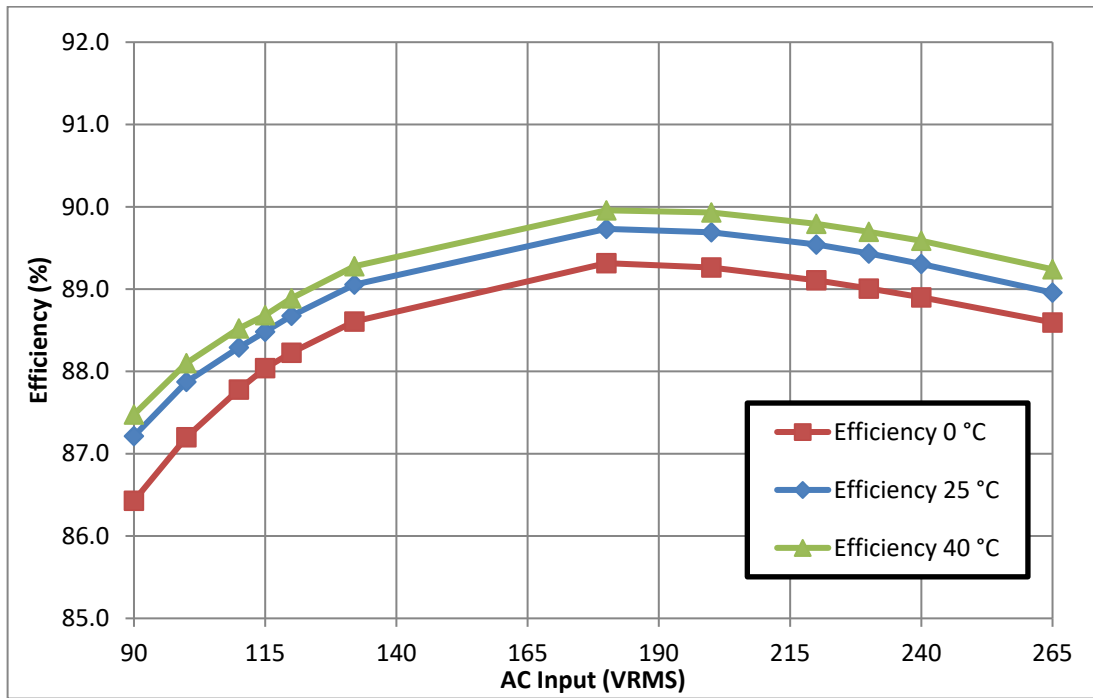
### 8.2.1 12 V Output at Full Load Condition ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )



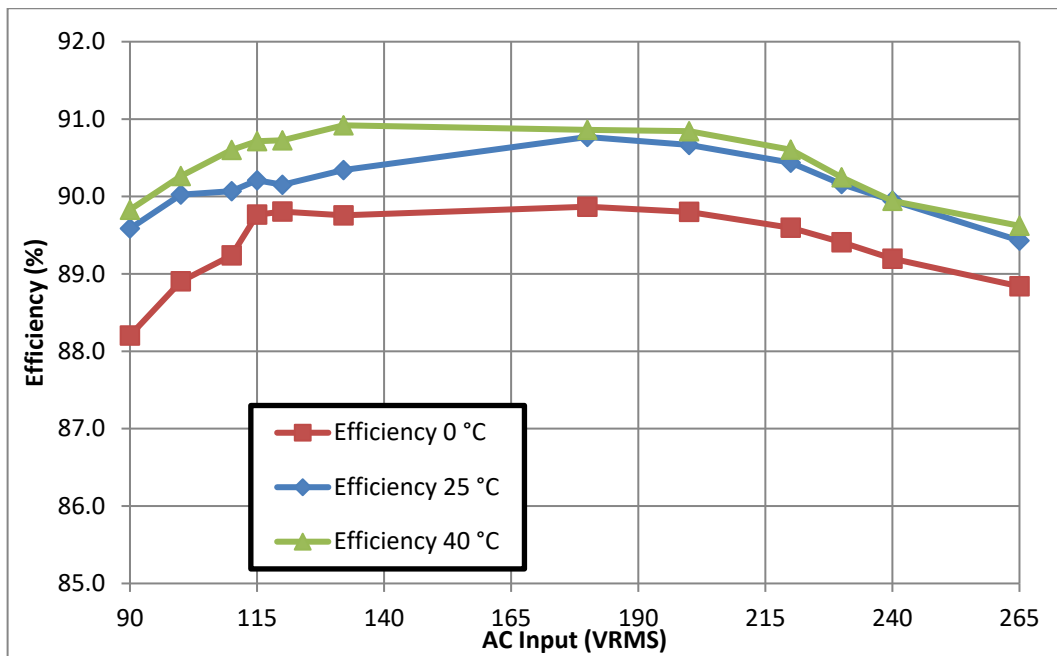
**Figure 8** – Full load Efficiency vs. Line Voltage. ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )



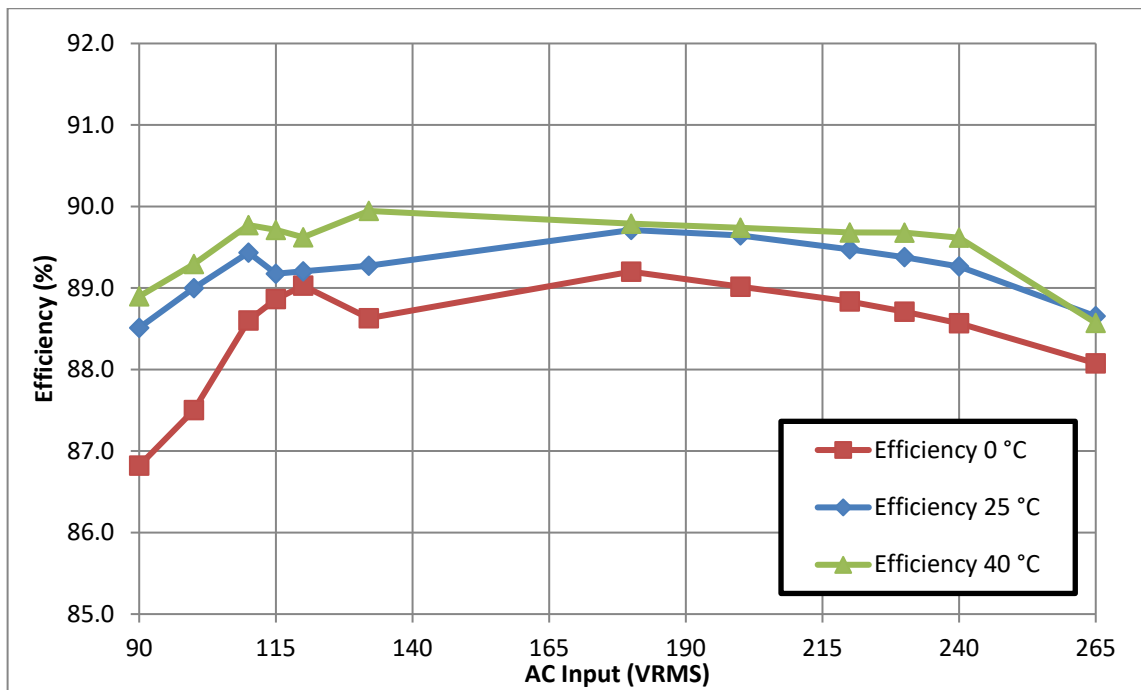
8.2.2 12 V Output at Full Load Condition ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )



**Figure 9** – Full load Efficiency vs. Line Voltage. ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

8.2.3 6 V Output at Full Load Condition ( $uVCC = 3.3\text{ V} / 0\text{ A}$ )

**Figure 10** – Full load Efficiency vs. Line Voltage. ( $uVCC = 3.3\text{ V} / 0\text{ A}$ )

8.2.4 6 V Output at Full Load Condition ( $uVCC = 3.3 \text{ V} / 20 \text{ mA}$ )

**Figure 11** – Full load Efficiency vs. Line Voltage. ( $uVCC = 3.3 \text{ V} / 20 \text{ mA}$ )

### 8.3 Efficiency vs. Load

Note: A thermal chamber is used to increase/decrease the ambient temperature. Unit is placed inside a box to prevent air flow.

Test Condition: Soak for 15 minutes and 2 minutes for each line/step. Measured across PCB output terminals.

#### 8.3.1 12 V Output Efficiency vs. Load ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

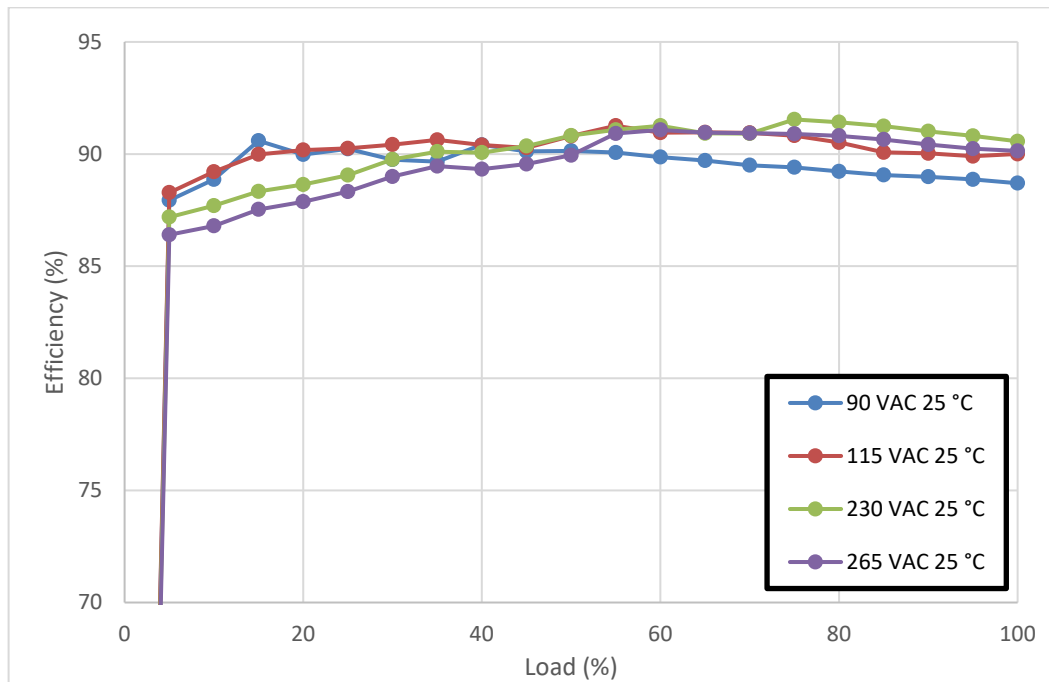
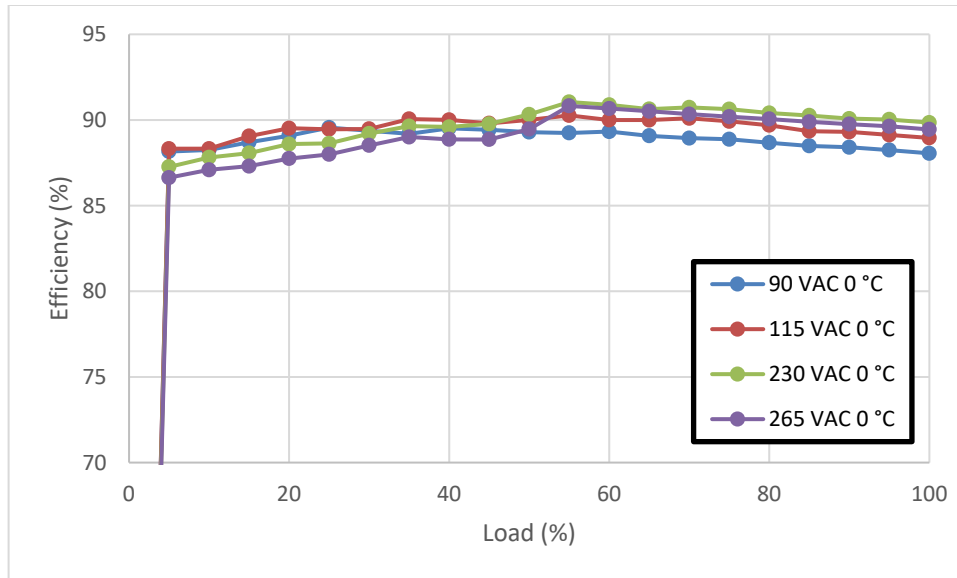
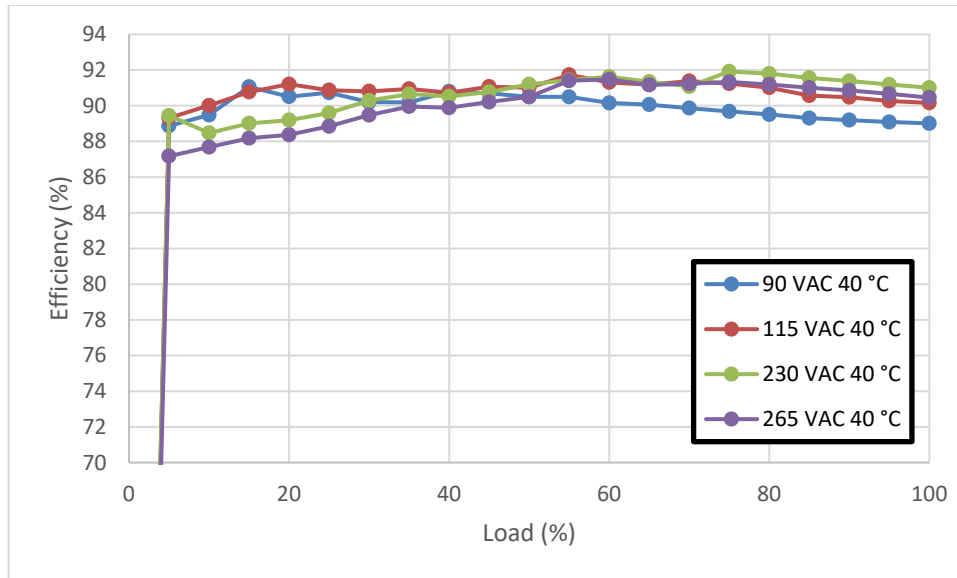


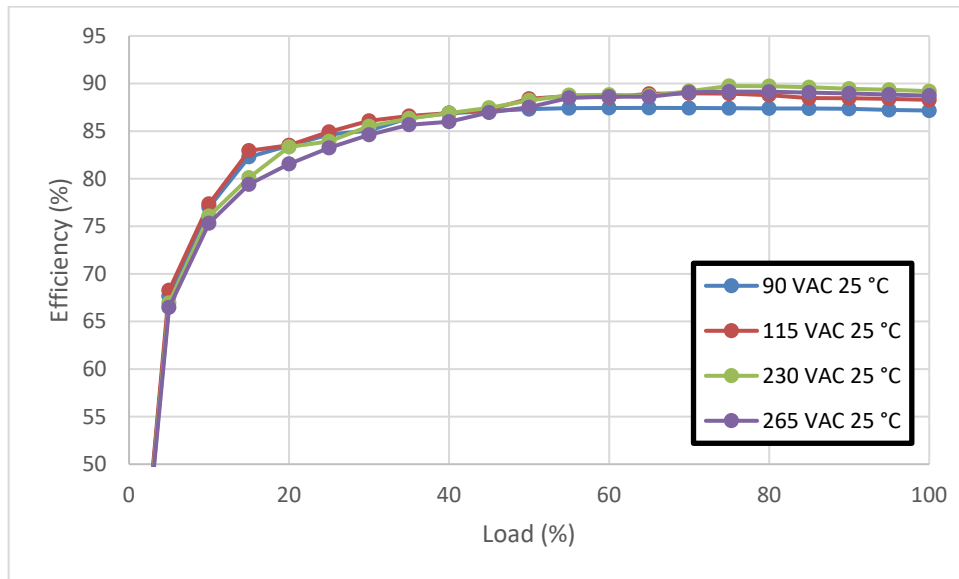
Figure 12 – Efficiency vs. Load, Room Ambient – 25 °C Temperature.



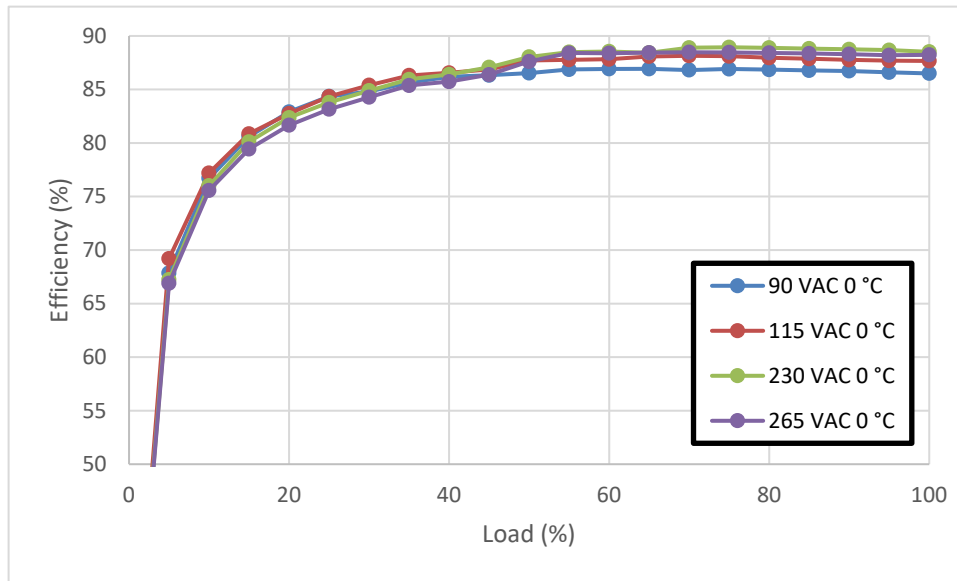
**Figure 13** – Efficiency vs. Load, Cold Ambient – 0 °C Temperature.



**Figure 14** – Efficiency vs. Load, Hot Ambient - 40°C Temperature.

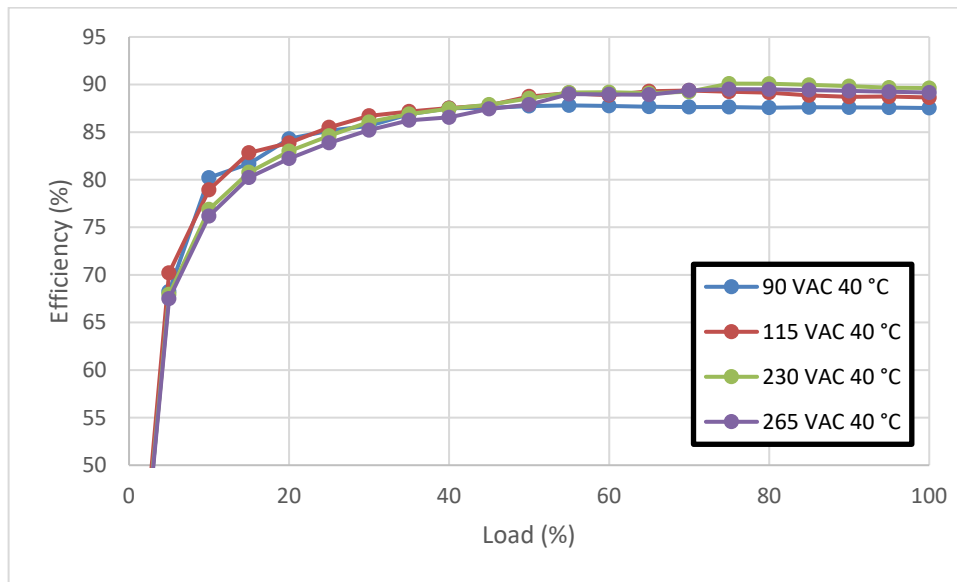
8.3.2 12 V Output Efficiency vs. Load ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

**Figure 15** – Efficiency vs. Load, Room Ambient – 25 °C Temperature.



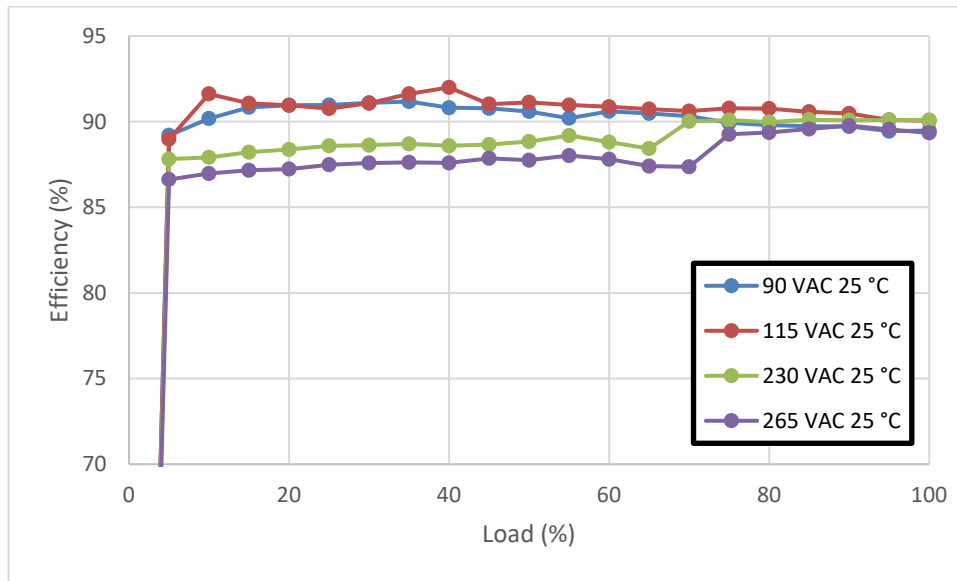
**Figure 16** – Efficiency vs. Load, Cold Ambient – 0 °C Temperature.



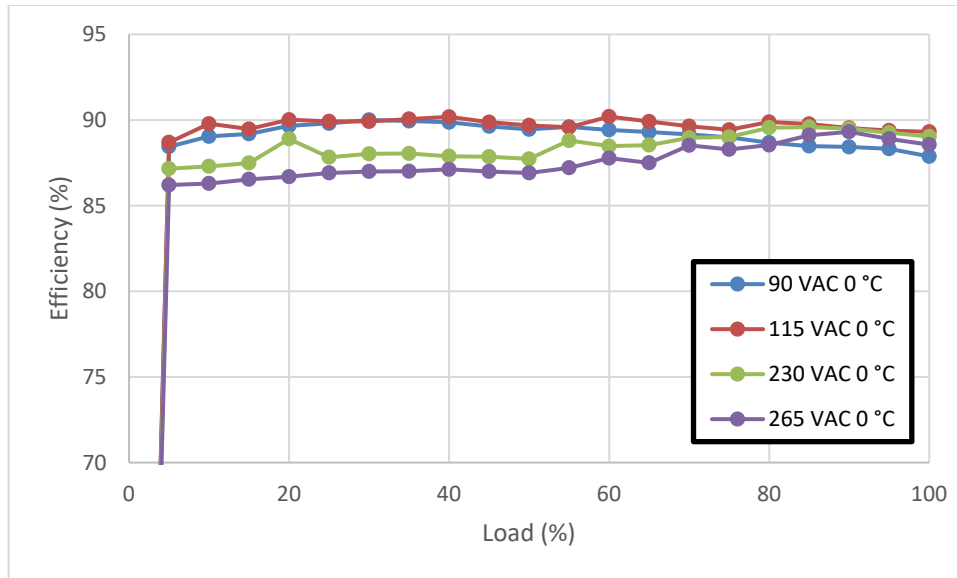


**Figure 17** – Efficiency vs. Load, Hot Ambient - 40°C Temperature.

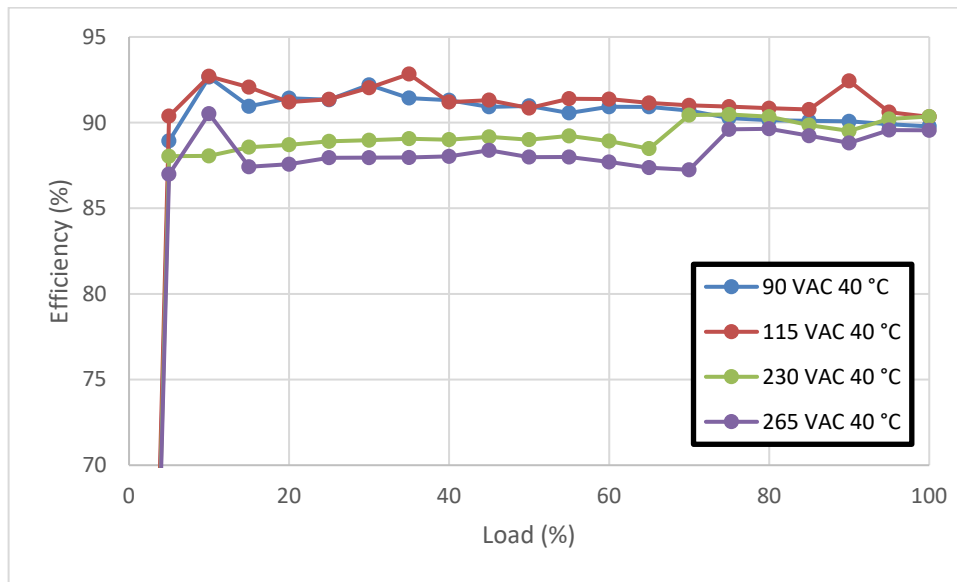
8.3.3 6 V Output Efficiency vs. Load ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )



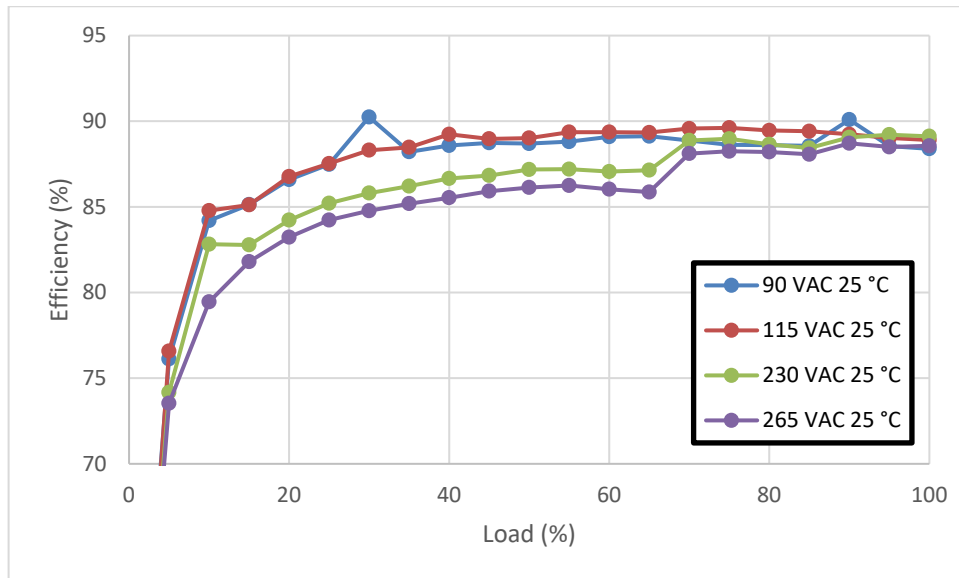
**Figure 18** – Efficiency vs. Load, Room Ambient – 25 °C Temperature.



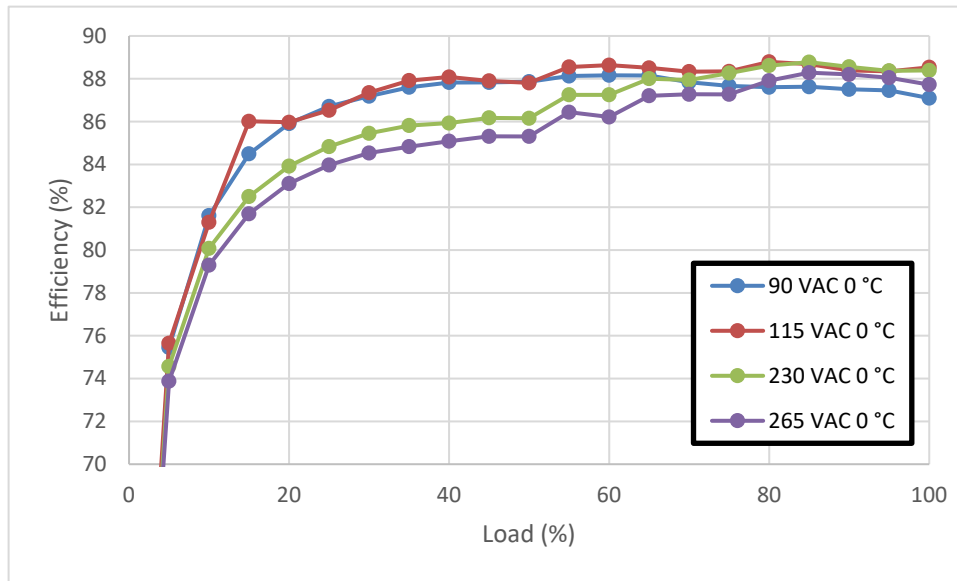
**Figure 19** – Efficiency vs. Load, Cold Ambient – 0 °C Temperature.



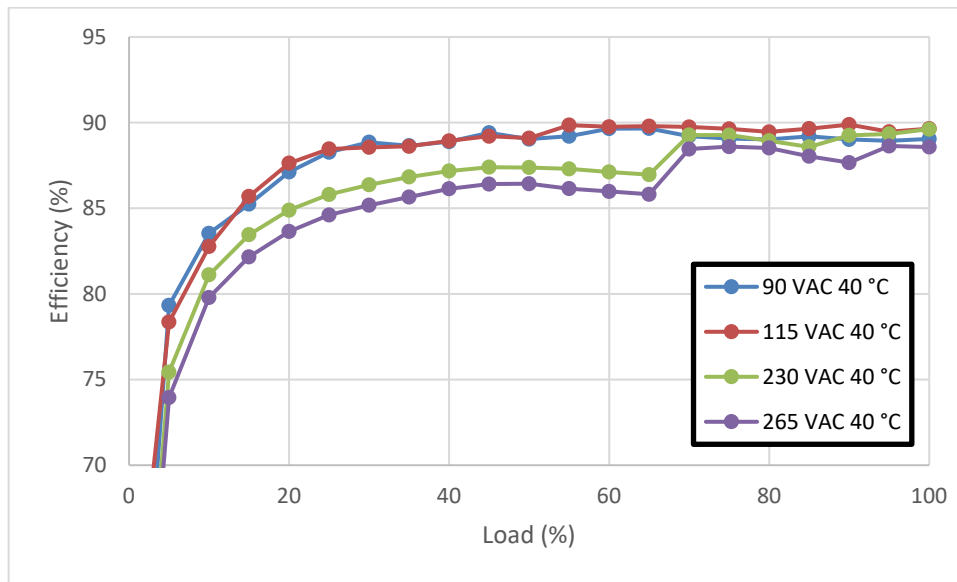
**Figure 20** – Efficiency vs. Load, Hot Ambient - 40°C Temperature.

8.3.4 6 V Output Efficiency vs. Load ( $uVCC = 3.3 \text{ V} / 20 \text{ mA}$ )

**Figure 21** – Efficiency vs. Load, Room Ambient – 25 °C Temperature.



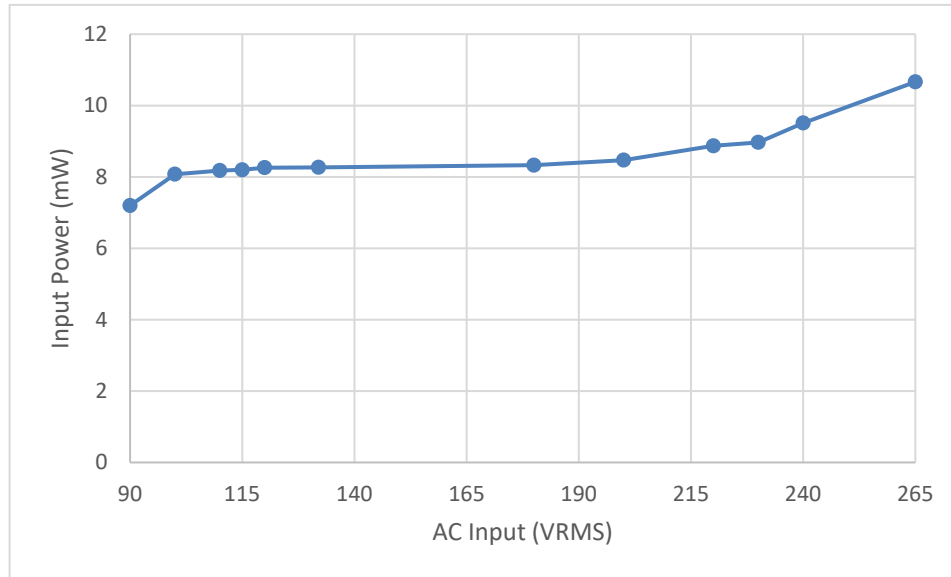
**Figure 22** – Efficiency vs. Load, Cold Ambient – 0 °C Temperature.



**Figure 23** – Efficiency vs. Load, Hot Ambient - 40°C Temperature.

## 8.4 No-Load Input Power

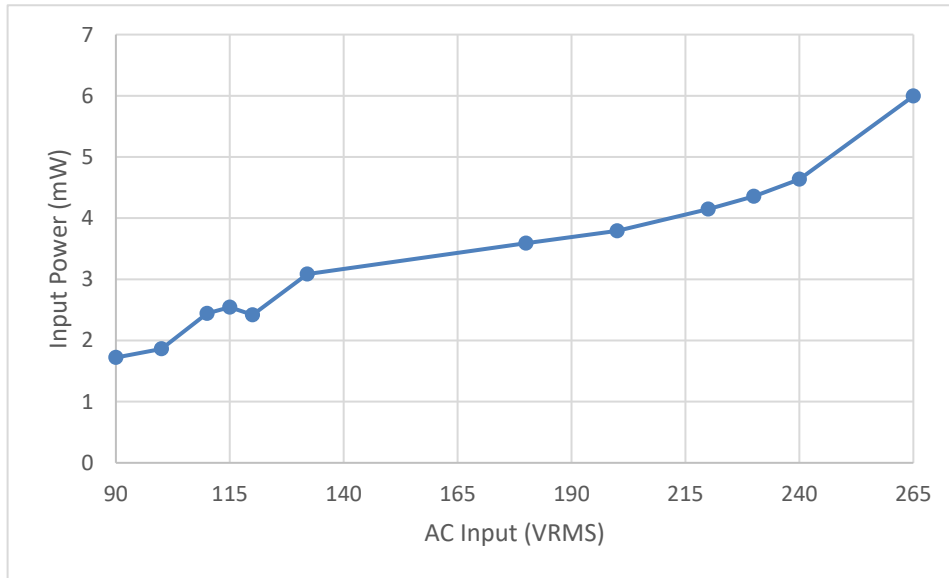
### 8.4.1 12 V Output – No-Load Input



**Figure 24** – No-Load Input Power vs. Input Line Voltage, Room Temperature.



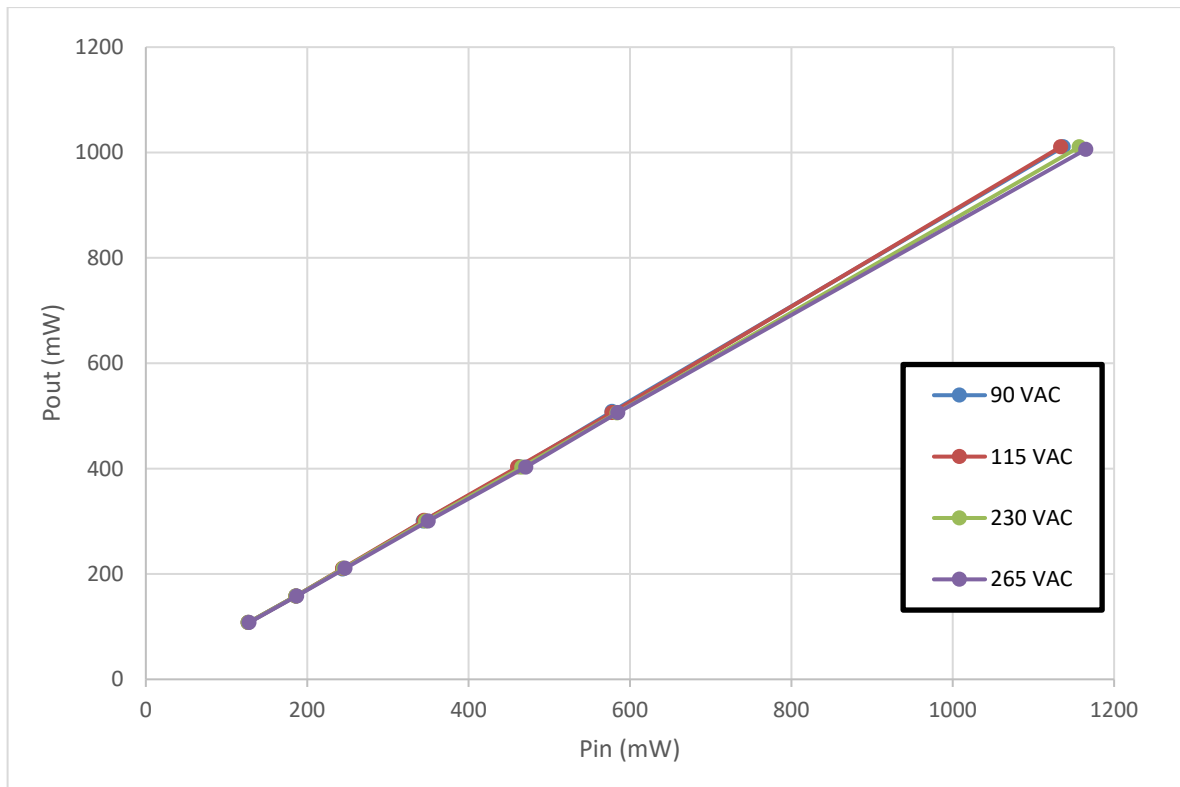
## 8.4.2 6 V Output – No-Load Input



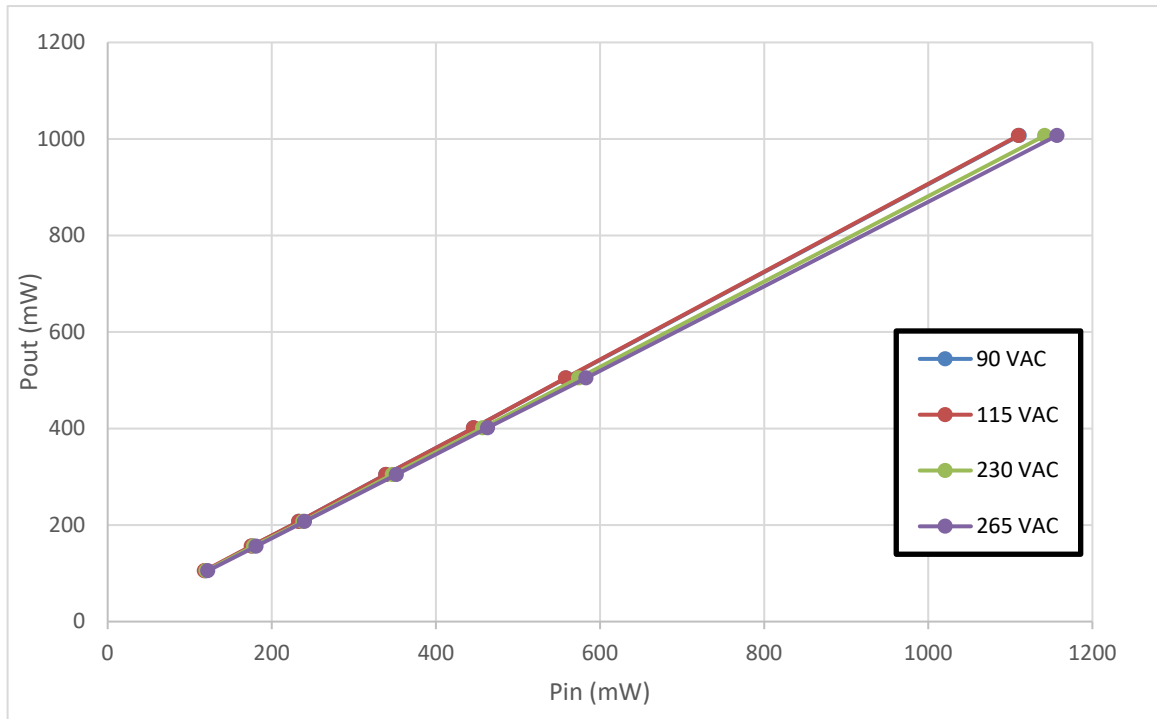
**Figure 25** – No-Load Input Power vs. Input Line Voltage, Room Temperature.

### 8.5 Standby Input Power

Test Condition: Soak at full load for 5 minutes and decrease the load to standby mode for 5 minutes each line step.



**Figure 26** – 12 V Standby Input Power vs Output Power.



**Figure 27** – 6 V Standby Input Power vs Output Power.

## 8.5.1 Standby Efficiency

## 8.5.1.1 90 VAC

## 12 V Output

V <sub>in</sub> (V <sub>RMS</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	12V <sub>OUT</sub> (V <sub>DC</sub> )	12I <sub>OUT</sub> (mA <sub>DC</sub> )	12P <sub>OUT</sub> (mW)	Efficiency (%)
90	24.91	1137	11.96	84.50	1010.79	88.90
90	13.89	578	11.97	42.50	508.56	87.99
90	11.24	463	11.97	33.70	403.22	87.09
90	8.49	344	11.97	25.10	300.40	87.32
90	6.16	244	11.97	17.50	209.42	85.83
90	4.52	186	11.97	13.20	158.00	84.95
90	3.40	127	11.97	9.00	107.73	84.83

## 6 V Output

V <sub>in</sub> (V <sub>RMS</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	6V <sub>OUT</sub> (V <sub>DC</sub> )	6I <sub>OUT</sub> (mA <sub>DC</sub> )	6P <sub>OUT</sub> (mW)	Efficiency (%)
90	26.01	1111	5.97	168.70	1006.97	90.64
90	13.47	559	5.97	84.50	504.55	90.26
90	10.86	446	5.97	67.20	401.32	89.98
90	8.27	339	5.97	51.00	304.57	89.84
90	5.89	233	5.97	34.70	207.30	88.97
90	4.54	176	5.97	26.20	156.52	88.93
90	3.17	119	5.97	17.60	105.07	88.30

## 8.5.1.2 115 VAC

## 12 V Output

V <sub>in</sub> (V <sub>RMS</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	12V <sub>OUT</sub> (V <sub>DC</sub> )	12I <sub>OUT</sub> (mA <sub>DC</sub> )	12P <sub>OUT</sub> (mW)	Efficiency (%)
115	19.77	1134	11.96	84.50	1010.87	89.14
115	11.10	578	11.97	42.30	506.16	87.57
115	8.98	461	11.97	33.70	403.25	87.47
115	6.83	345	11.97	25.20	301.62	87.43
115	4.94	244	11.97	17.60	210.62	86.32
115	3.60	186	11.97	13.20	158.00	84.95
115	2.72	127	11.97	9.00	107.73	84.83

## 6 V Output

V <sub>in</sub> (V <sub>RMS</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	6V <sub>OUT</sub> (V <sub>DC</sub> )	6I <sub>OUT</sub> (mA <sub>DC</sub> )	6P <sub>OUT</sub> (mW)	Efficiency (%)
115	20.77	1110	5.97	168.70	1007.14	90.73
115	10.73	558	5.97	84.50	504.63	90.44
115	8.69	446	5.97	67.20	401.32	89.98
115	6.66	339	5.97	51.00	304.62	89.86
115	4.74	233	5.97	34.70	207.26	88.95
115	3.64	175	5.97	26.20	156.49	89.42
115	2.54	118	5.97	17.60	105.14	89.10



## 8.5.1.3 230 VAC

## 12 V Output

V <sub>in</sub> (V <sub>rms</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	12V <sub>OUT</sub> (V <sub>DC</sub> )	12I <sub>OUT</sub> (mA <sub>DC</sub> )	12P <sub>out</sub> (mW)	Efficiency (%)
230	11.30	1157	11.96	84.50	1010.62	87.35
230	5.90	584	11.97	42.27	505.80	86.61
230	4.81	466	11.97	33.65	402.72	86.42
230	3.64	347	11.97	25.10	300.45	86.58
230	2.63	245	11.97	17.60	210.67	85.99
230	1.89	186	11.97	13.20	158.02	84.96
230	1.42	127	11.97	9.00	107.75	84.84

## 6 V Output

V <sub>in</sub> (V <sub>rms</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	12V <sub>OUT</sub> (V <sub>DC</sub> )	12I <sub>OUT</sub> (mA <sub>DC</sub> )	12P <sub>out</sub> (mW)	Efficiency (%)
230	11.16	1142	5.97	168.70	1006.97	88.18
230	5.81	574	5.97	84.50	504.63	87.92
230	4.71	457	5.97	67.20	401.32	87.82
230	3.61	347	5.97	51.00	304.62	87.79
230	2.57	238	5.97	34.70	207.26	87.09
230	1.96	178	5.97	26.20	156.52	87.93
230	1.35	120	5.98	17.60	105.16	87.63

## 8.5.1.4 265 VAC

## 12 V Output

V <sub>in</sub> (V <sub>rms</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	12V <sub>OUT</sub> (V <sub>DC</sub> )	12I <sub>OUT</sub> (A <sub>DC</sub> )	12P <sub>out</sub> (W)	Efficiency (%)
265	9.95	1165	11.91	84.50	1005.97	86.35
265	5.20	585	11.97	42.30	506.25	86.54
265	4.22	471	11.97	33.65	402.76	85.51
265	3.20	350	11.97	25.10	300.50	85.86
265	2.32	247	11.97	17.60	210.69	85.30
265	1.65	187	11.97	13.20	158.04	84.52
265	1.24	128	11.97	9.00	107.74	84.17

## 6 V Output

V <sub>in</sub> (V <sub>rms</sub> )	I <sub>in</sub> (mA)	P <sub>IN</sub> (mW)	12V <sub>OUT</sub> (V <sub>DC</sub> )	12I <sub>OUT</sub> (A <sub>DC</sub> )	12P <sub>out</sub> (W)	Efficiency (%)
265	9.89	1157	5.97	168.70	1007.14	87.05
265	5.15	583	5.97	84.50	504.63	86.56
265	4.17	463	5.97	67.20	401.39	86.69
265	3.23	352	5.97	51.00	304.62	86.54
265	2.29	240	5.97	34.70	207.30	86.37
265	1.73	181	5.96	26.20	156.05	86.21
265	1.20	122	5.97	17.60	105.14	86.18

8.5.2 Available Standby Output Power

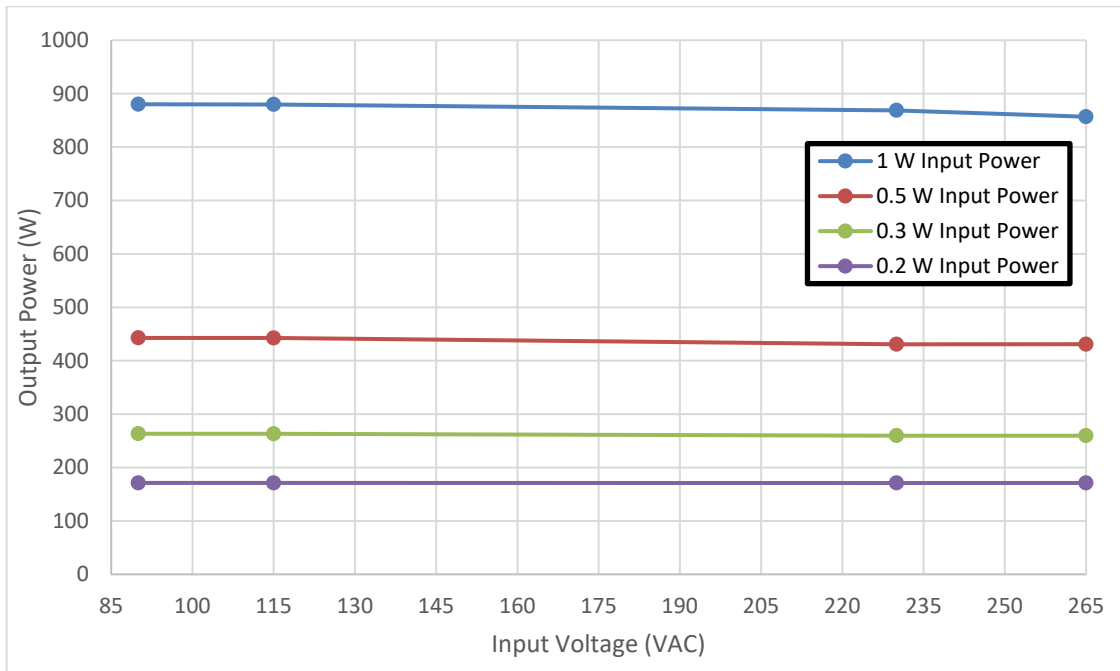


Figure 28 - 12 V Available Standby Output Power for 0.2 W, 0.3 W, 0.5 W and 1 W Input Power.

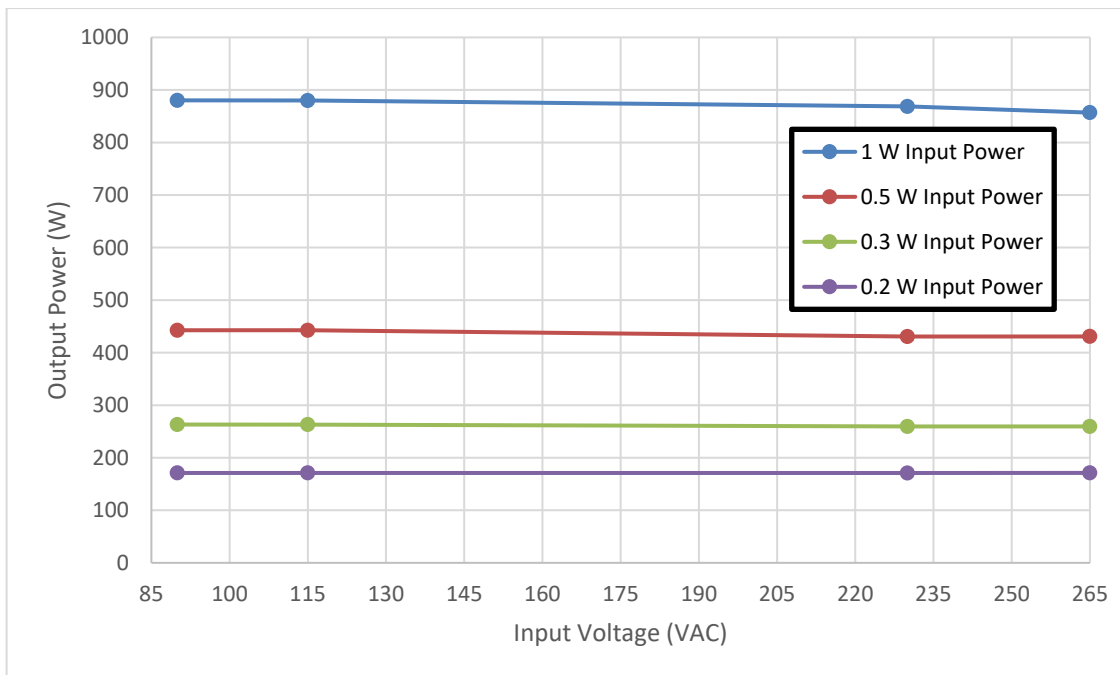


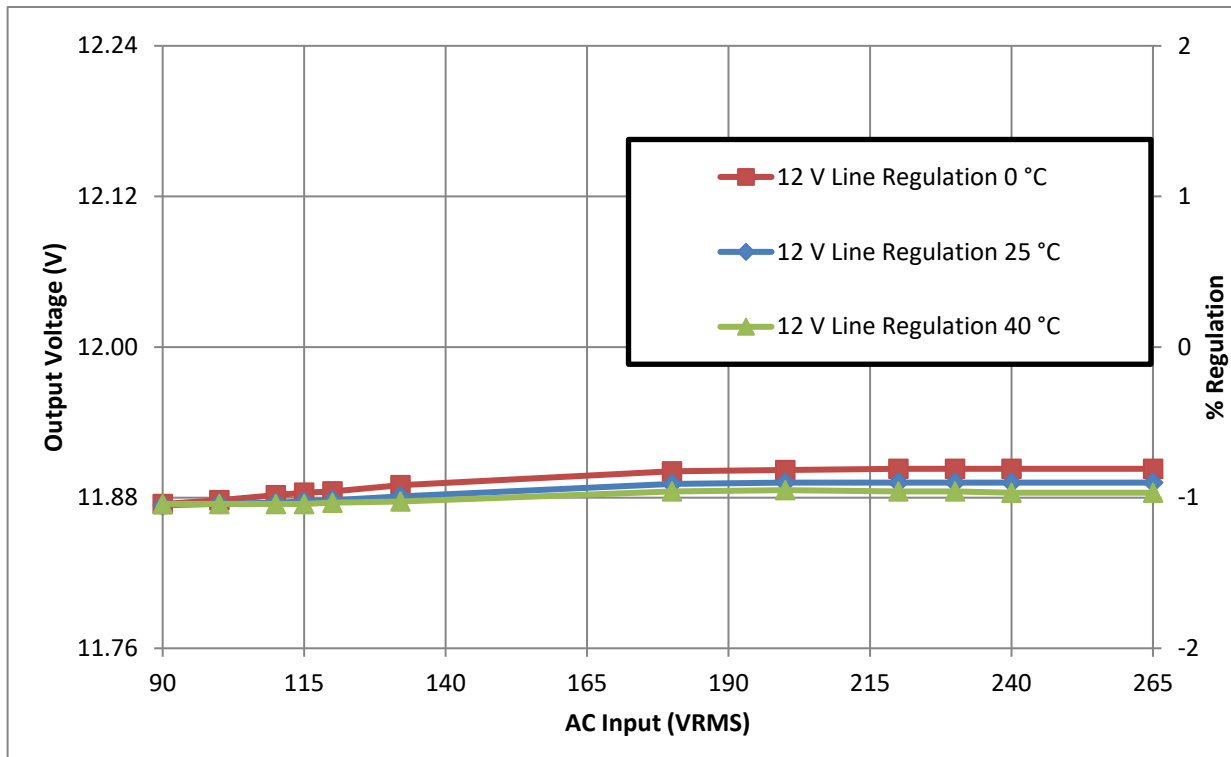
Figure 29 - 6 V Available Standby Output Power for 0.2 W, 0.3 W, 0.5 W and 1 W Input Power.

### 8.6 Line and Load Regulation

Note: A thermal chamber is used to increase/decrease the ambient temperature. Unit is placed inside a box to prevent air flow.

Test Condition: Soak for 15 minutes and 5 minutes for each line/step. Measured across PCB output terminals.

#### 8.6.1 Line Regulation at Full Load Condition ( $uVCC = 3.3\text{ V} / 0\text{ A}$ )



**Figure 30** – 12 V Output Voltage vs. Input Line Voltage.

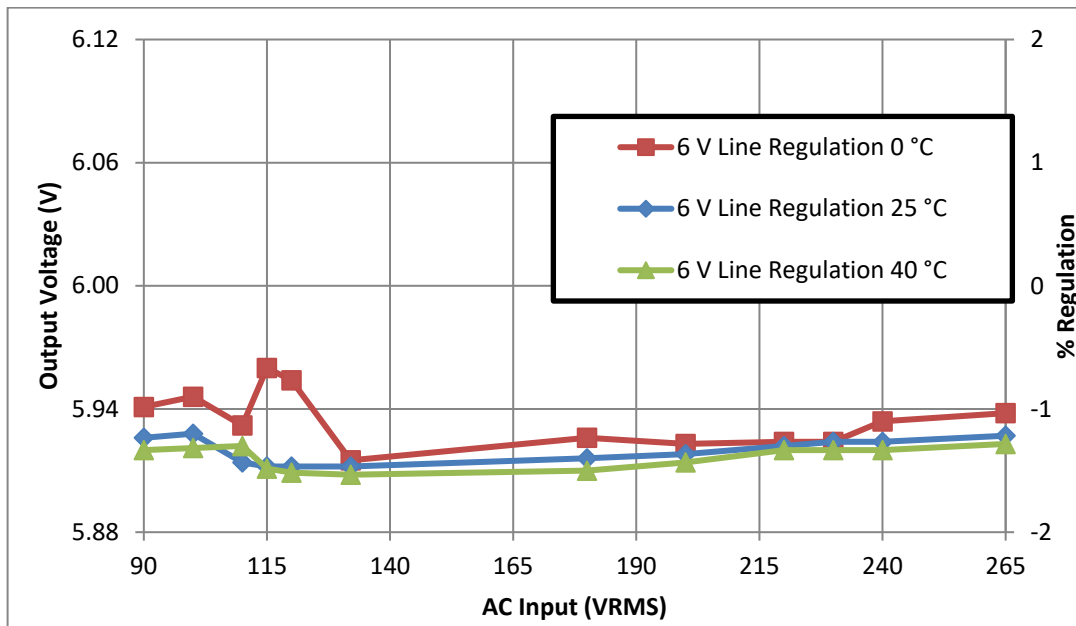


Figure 31 – 6 V Output Voltage vs. Input Line Voltage.

	12 V	6 V
<b>Min.</b>	11.88 V	5.91 V
<b>Max.</b>	11.89 V	5.96 V



8.6.2 Line Regulation at Full Load Condition (uVCC = 3.3 V / 20 mA)

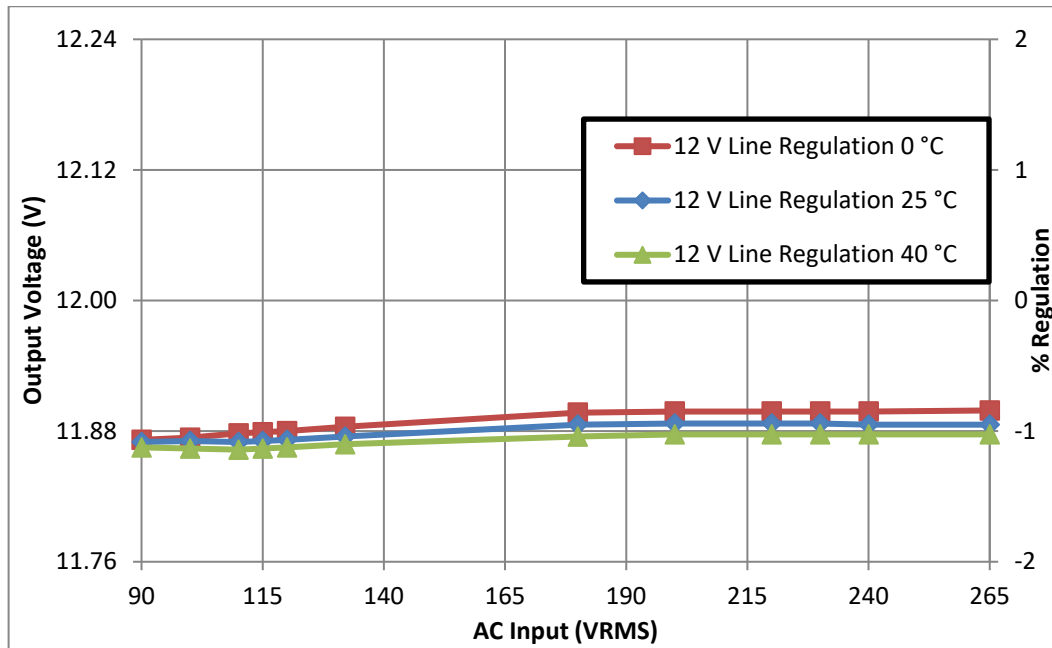


Figure 32 – 12 V Output Voltage vs. Input Line Voltage.

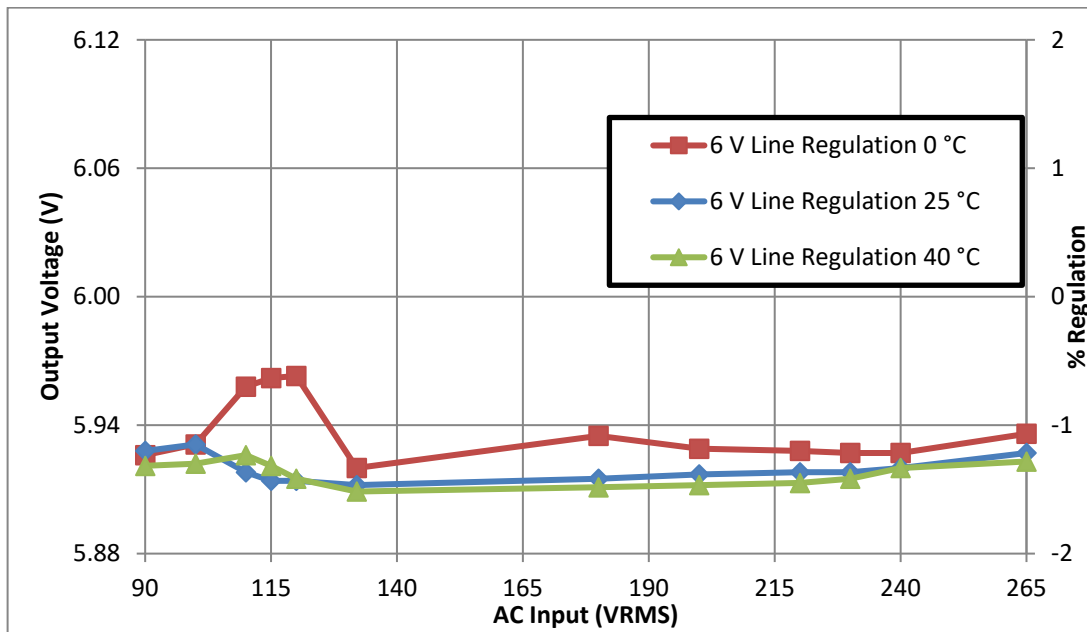
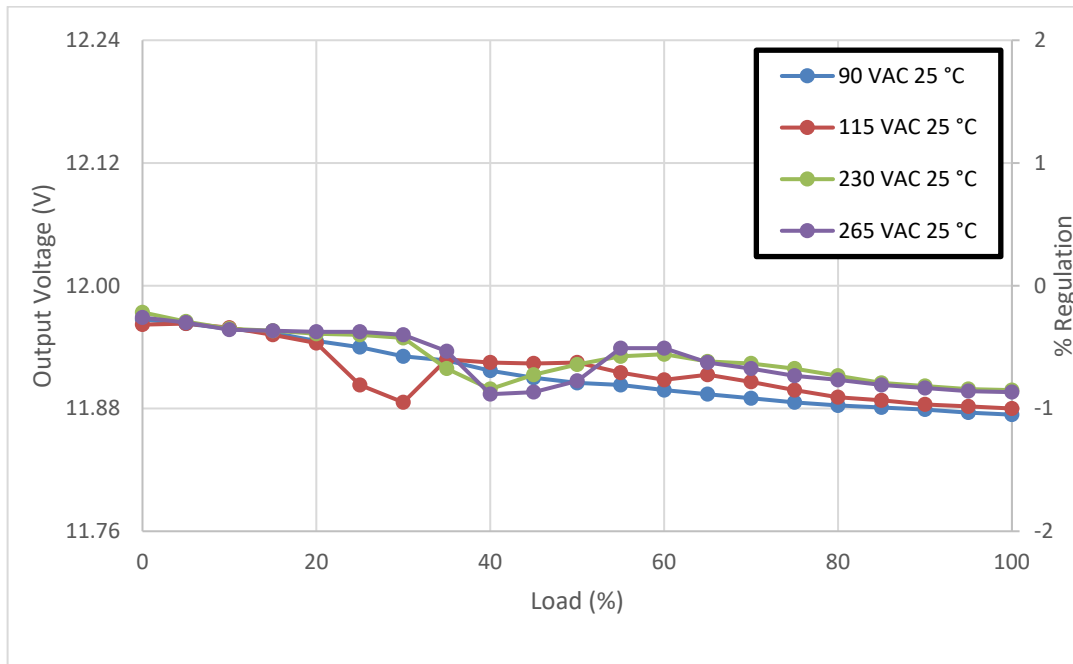
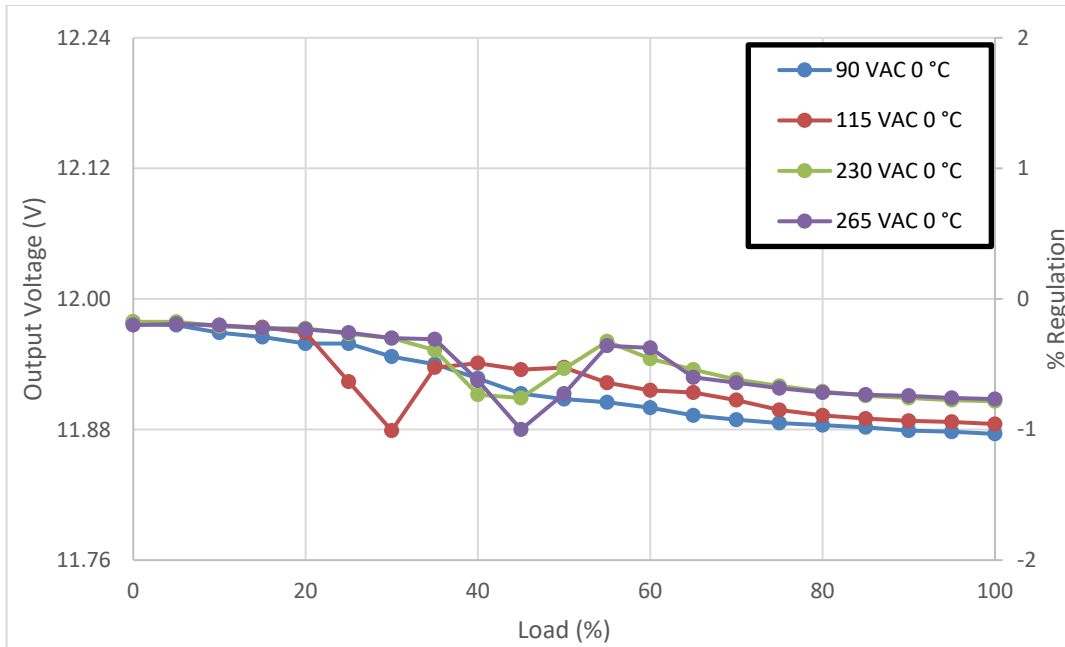


Figure 33 – 6 V Output Voltage vs. Input Line Voltage.

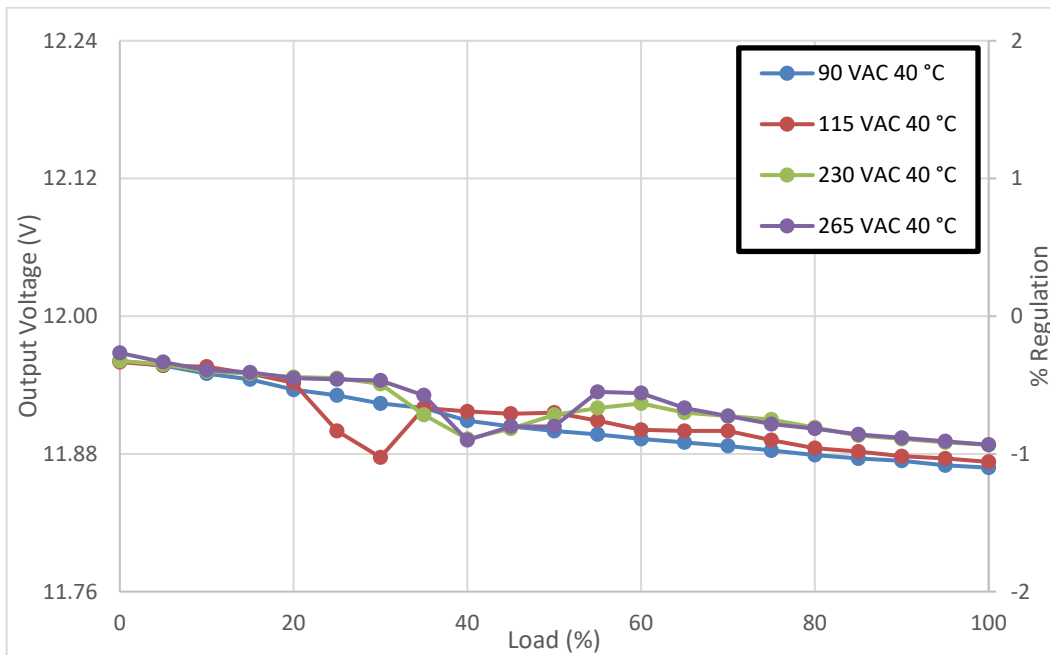
	12 V	6 V
<b>Min.</b>	11.86 V	5.91 V
<b>Max.</b>	11.90 V	5.96 V

8.6.3 12 V Load Regulation ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

**Figure 34** – 12 V Output Voltage vs. Load, Room Ambient – 25 °C Temperature.

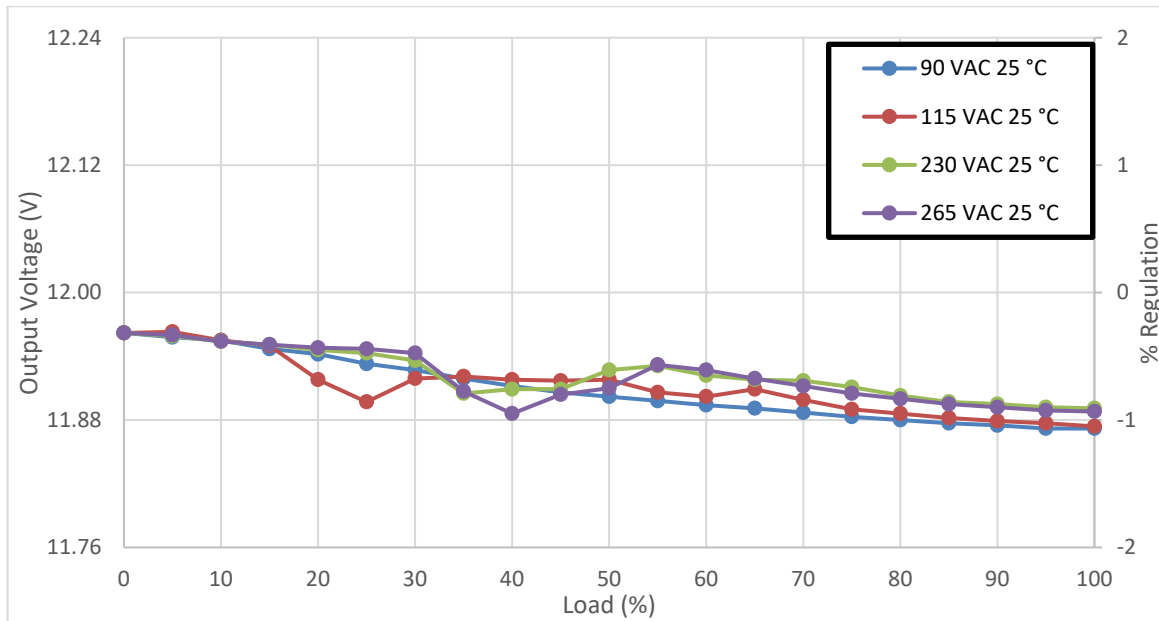


**Figure 35** – 12 V Output Voltage vs. Load, Cold Ambient – 0 °C Temperature.

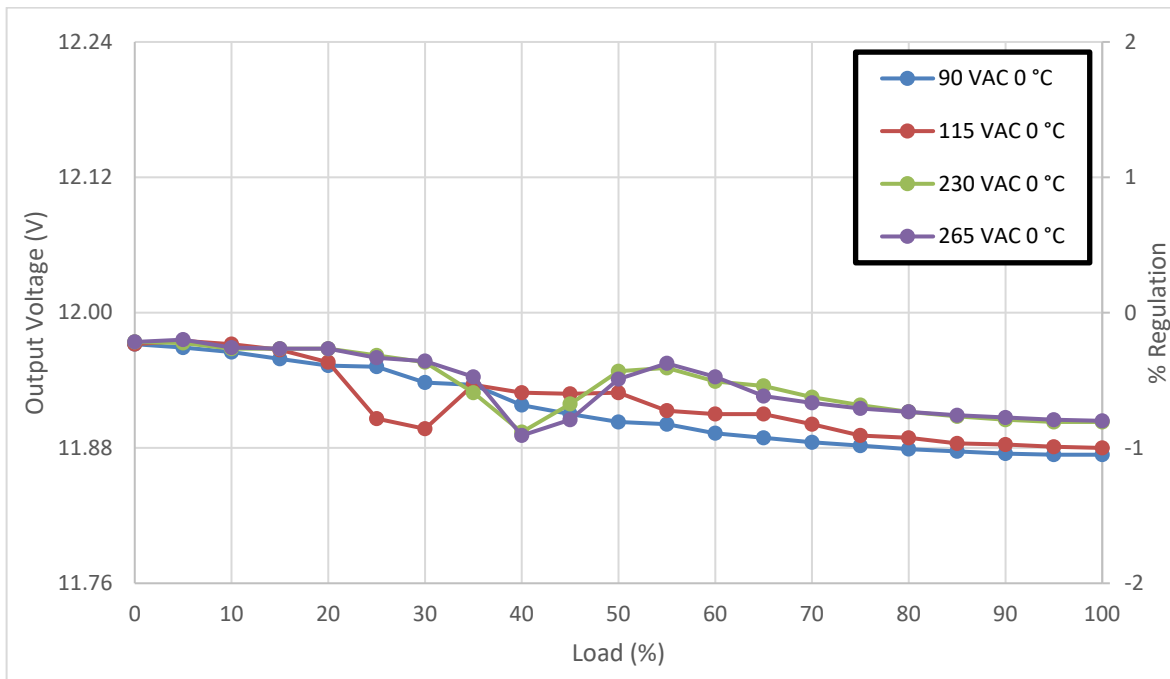


**Figure 36 – 12 V Output Voltage vs. Load, Hot Ambient – 40 °C Temperature.**

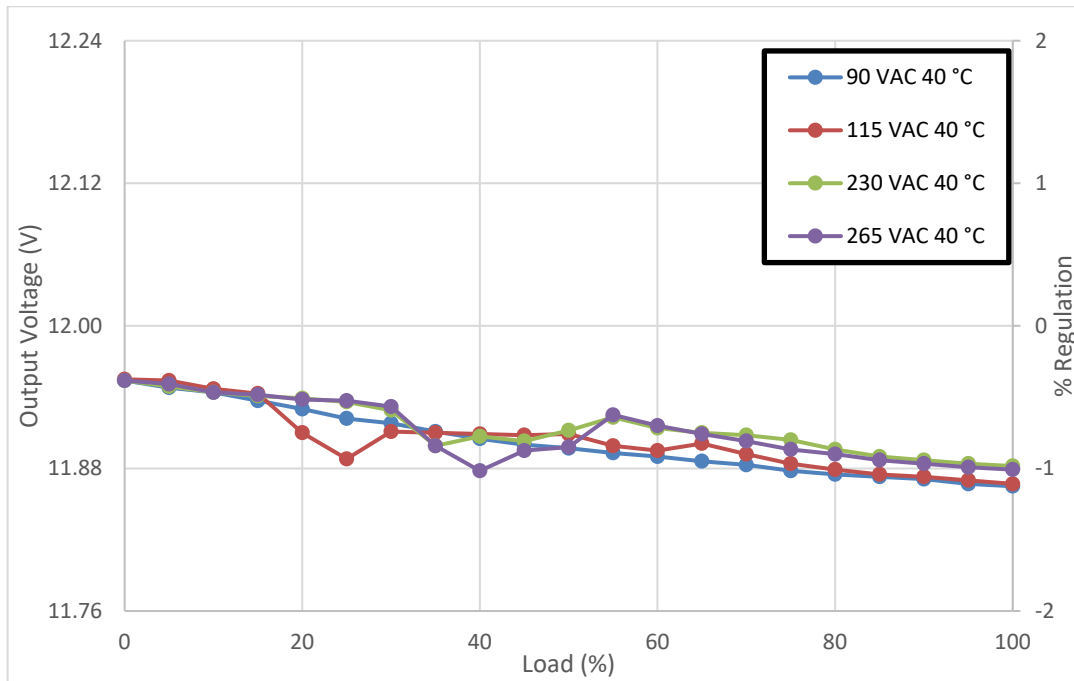
8.6.4 12 V Load Regulation ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )



**Figure 37** – 12 V Output Voltage vs. Load, Room Ambient – 25 °C Temperature.

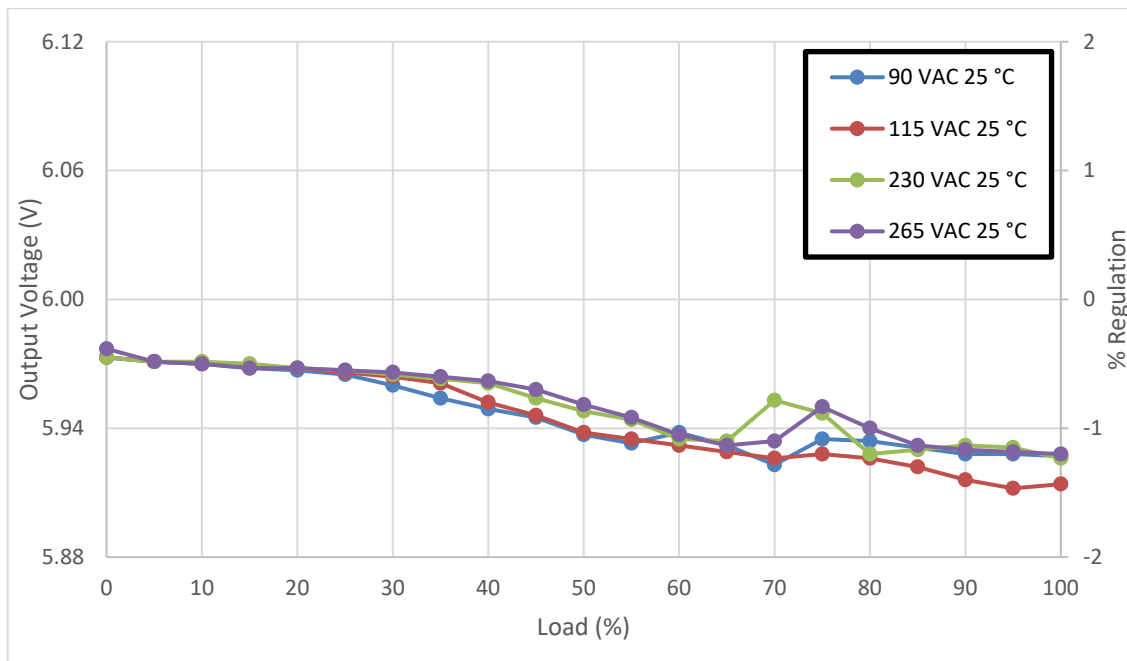


**Figure 38** – 12 V Output Voltage vs. Load, Cold Ambient – 0 °C Temperature.

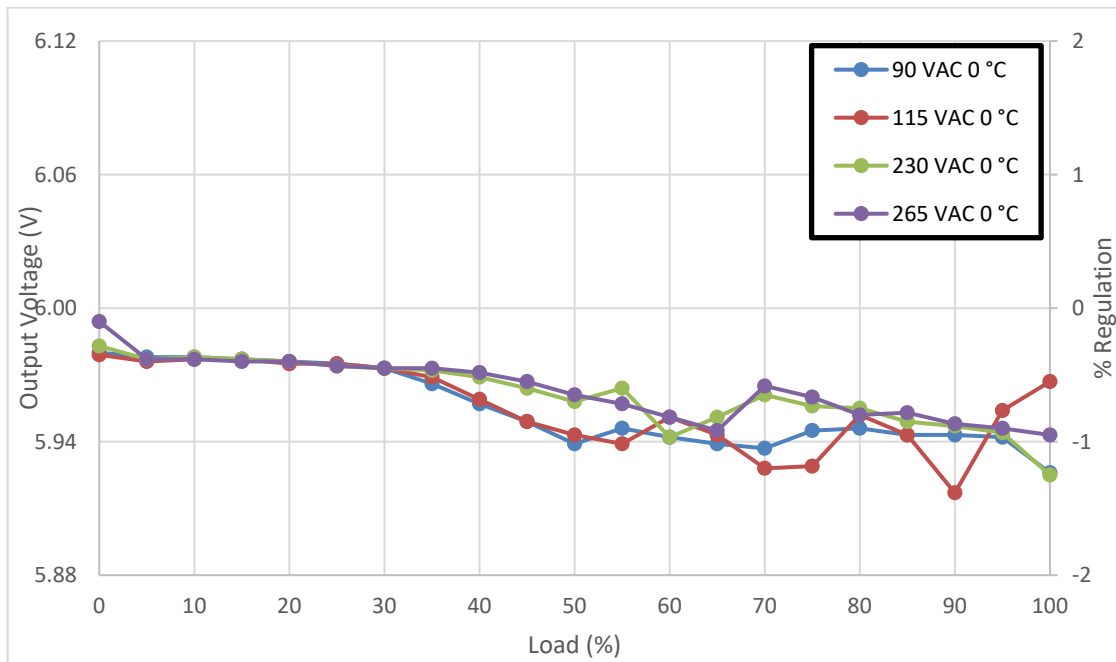


**Figure 39** – 12 V Output Voltage vs. Load, Hot Ambient – 40 °C Temperature.

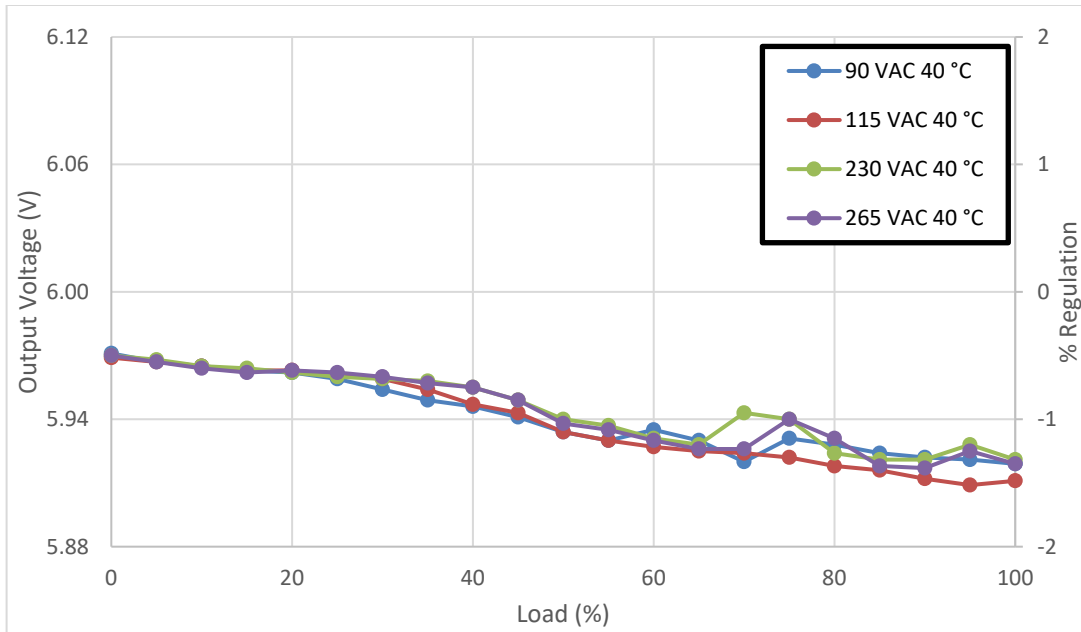


8.6.5 6 V Load Regulation ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

**Figure 40** – 6 V Output Voltage vs. Load, Room Ambient – 25 °C Temperature.

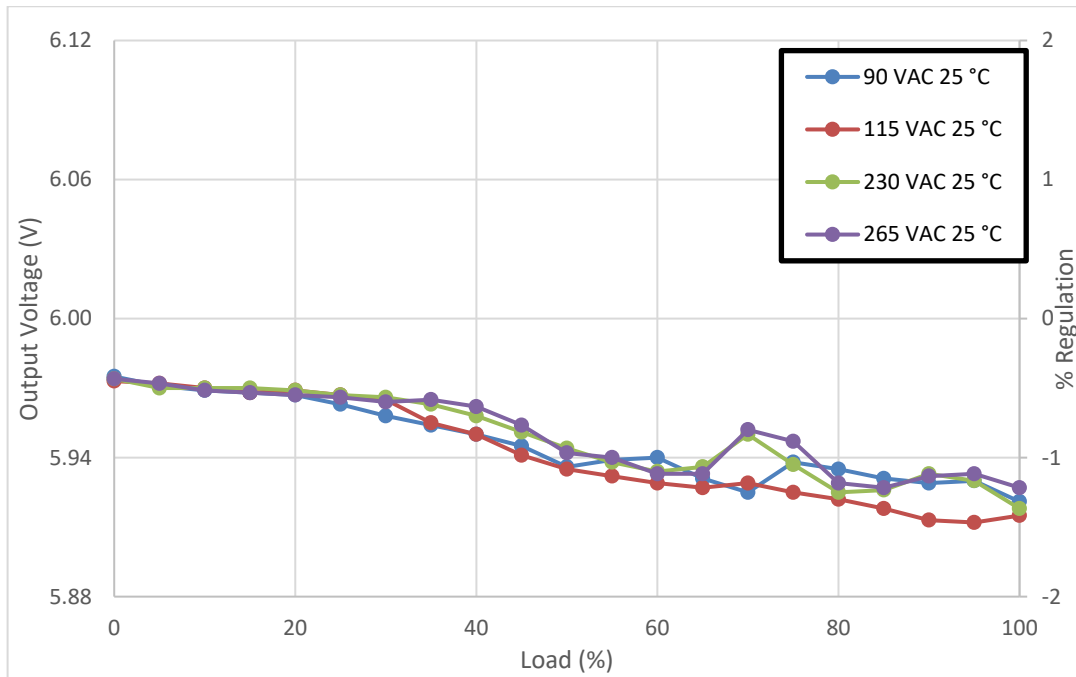


**Figure 41** – 6 V Output Voltage vs. Load, Cold Ambient – 0 °C Temperature.

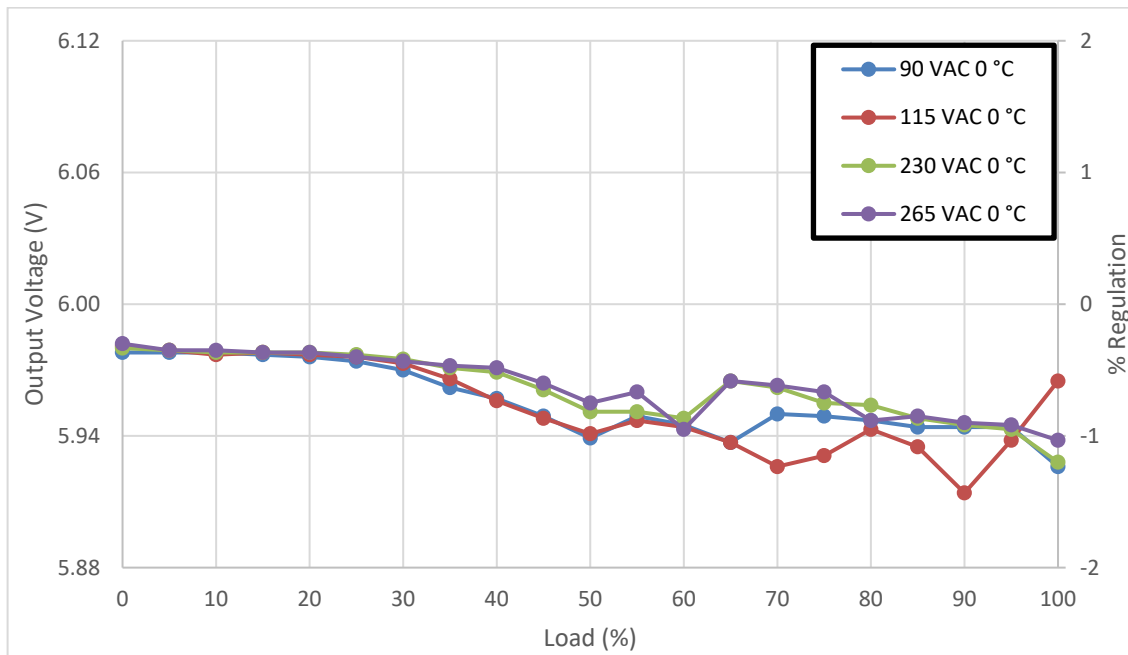


**Figure 42** – 12 V Output Voltage vs. Load, Hot Ambient – 40 °C Temperature.

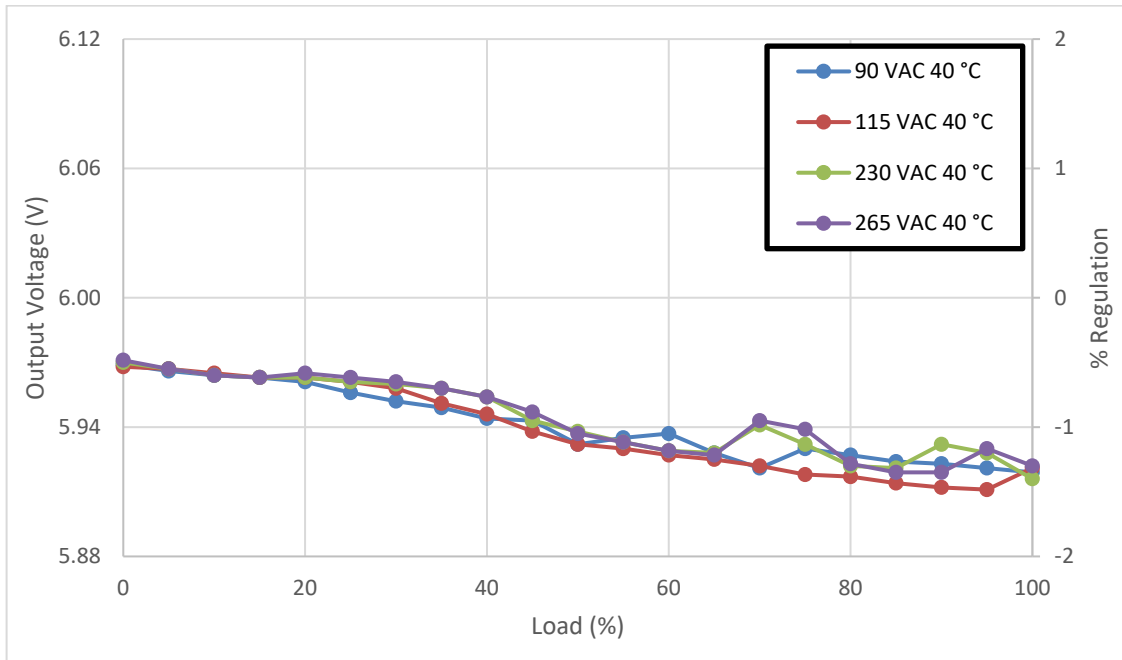
8.6.6 6 V Load Regulation ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )



**Figure 43** – 6 V Output Voltage vs. Load, Room Ambient – 25 °C Temperature.



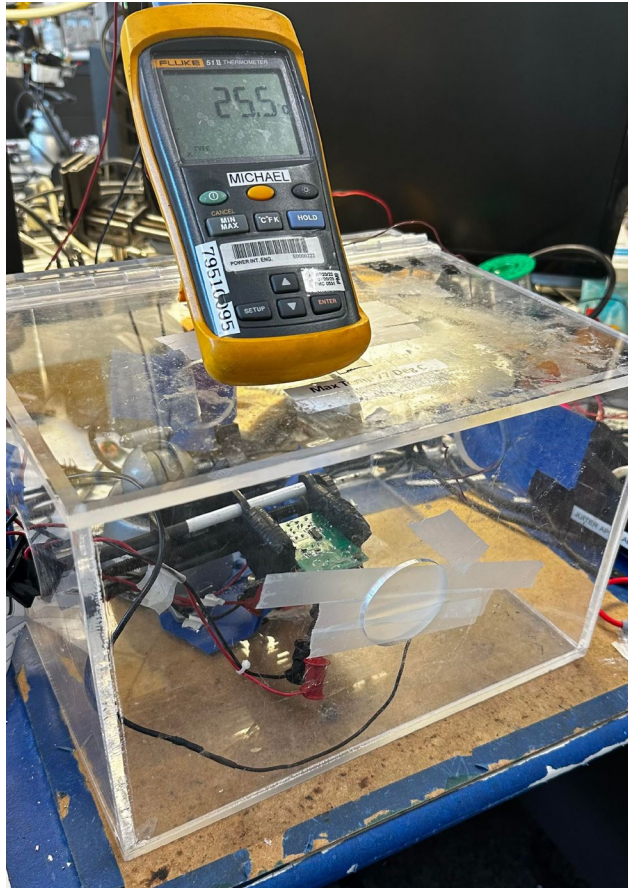
**Figure 44** – 6 V Output Voltage vs. Load, Cold Ambient – 0 °C Temperature.



**Figure 45** – 6 V Output Voltage vs. Load, Hot Ambient – 40 °C Temperature.

## 9 Thermal Performance

Note: Tested using an IR Camera.



**Figure 46** - Test Set-up.

9.1 90 VAC Input, 12 V / 1 A Output ( $v_{VCC} = 3.3 V / 20 mA$ )

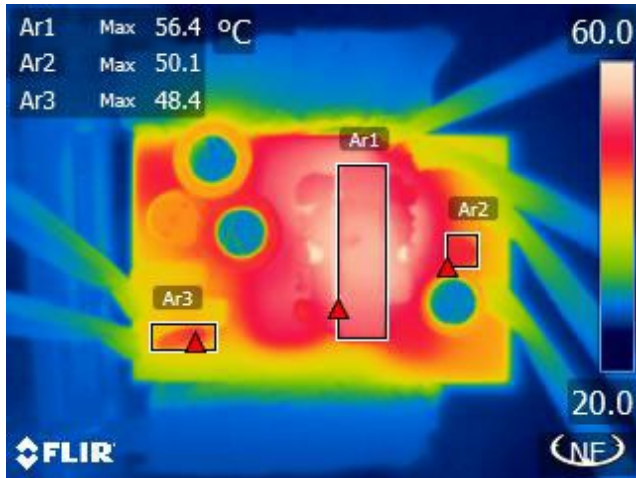


Figure 47 – Transformer Side. 90 VAC, Full Load.

	Reference	°C
Ambient		26.2
Transformer Core (T1)	Ar1	56.4
Output Filter Inductor (L2)	Ar2	50.1
Thermistor (RT1)	Ar3	48.4

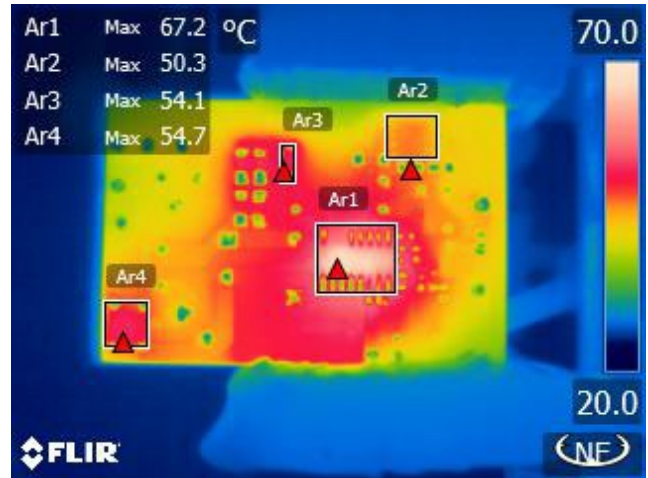


Figure 48 – LinkSwitch-XT2SR Side. 90 VAC, Full Load.

	Reference	°C
Ambient		26.2
LinkSwitch-XT2SR (U1)	Ar1	67.2
SR FET (Q1)	Ar2	50.8
Snubber Diode (D1)	Ar3	54.1
Bridge Diode (BR1)	Ar4	54.7



9.2 265 VAC Input, 12 V / 1 A Output ( $v_{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

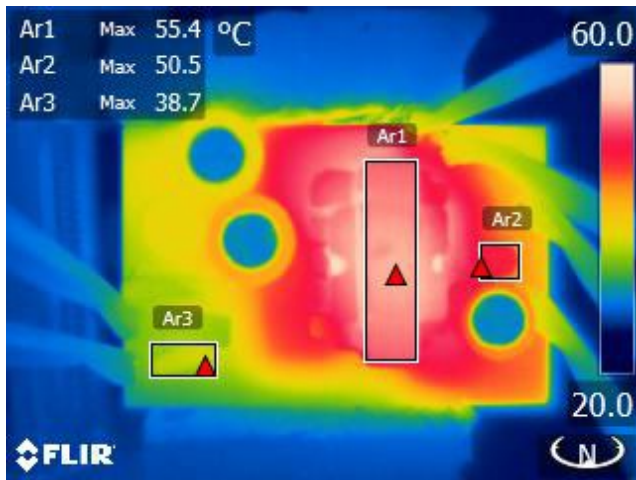


Figure 49 – Transformer Side. 265 VAC, Full Load.

	Reference	°C
Ambient		26.2
Transformer Core (T1)	Ar1	55.4
Output Filter Inductor (L2)	Ar2	50.5
Thermistor (RT1)	Ar3	38.7

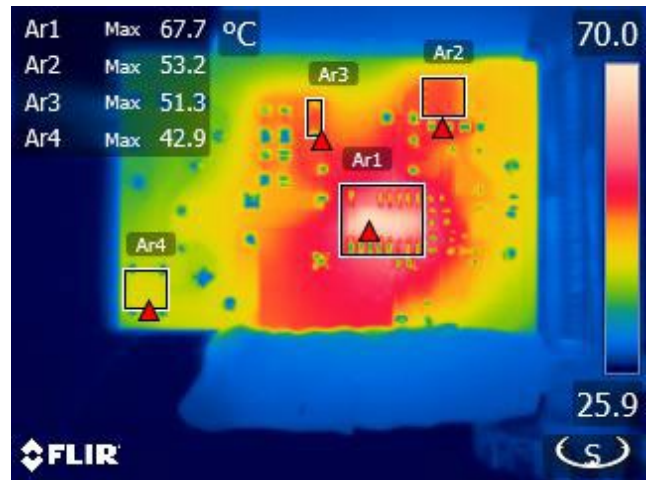


Figure 50 – LinkSwitch-XT2SR Side. 265 VAC, Full Load.

	Reference	°C
Ambient		26.2
LinkSwitch-XT2SR (U1)	Ar1	67.7
SR FET (Q1)	Ar2	53.2
Snubber Diode (D1)	Ar3	51.3
Bridge Diode (BR1)	Ar4	42.9

9.3 90 VAC Input, 6 V / 1 A Output ( $uVCC = 3.3 V / 20 mA$ )

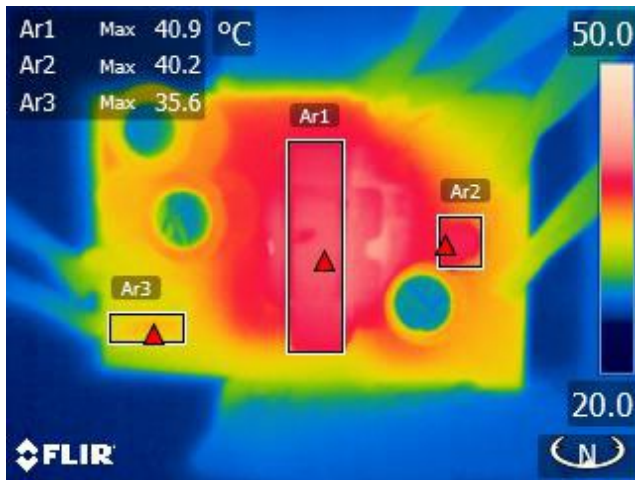


Figure 51 – Transformer Side. 90 VAC, Full Load.

	Reference	°C
<b>Ambient</b>		26.0
<b>Transformer Core (T1)</b>	Ar1	40.9
<b>Output Filter Inductor (L2)</b>	Ar2	40.2
<b>Thermistor (RT1)</b>	Ar3	35.6

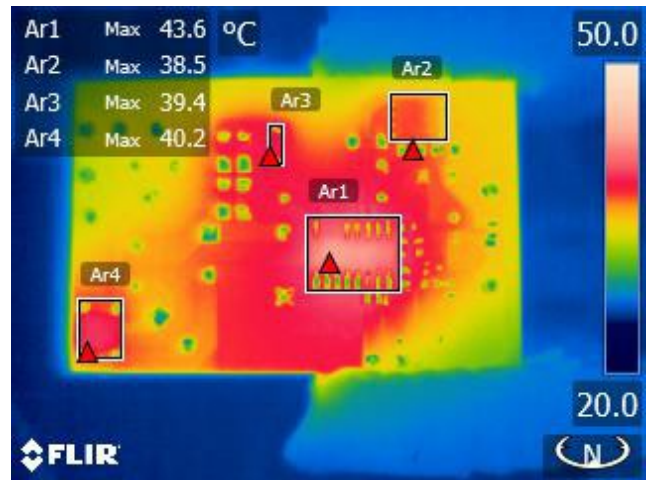


Figure 52 – LinkSwitch-XT2SR Side. 90 VAC, Full Load.

	Reference	°C
<b>Ambient</b>		26.0
<b>LinkSwitch-XT2SR (U1)</b>	Ar1	43.6
<b>SR FET (Q1)</b>	Ar2	38.5
<b>Snubber Diode (D1)</b>	Ar3	39.4
<b>Bridge Diode (BR1)</b>	Ar4	40.2

9.4 265 VAC Input, 6 V / 1 A Output ( $v_{VCC} = 3.3 V / 20 mA$ )

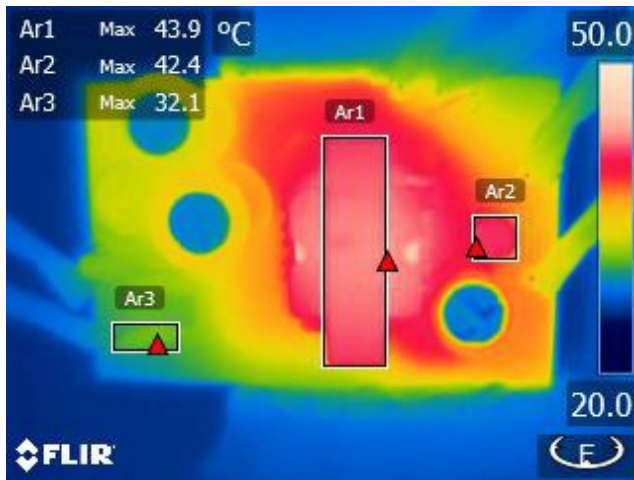


Figure 53 – Transformer Side. 265 VAC, Full Load.

	Reference	°C
Ambient		26.2
Transformer Core (T1)	Ar1	43.9
Output Filter Inductor (L2)	Ar2	42.4
Thermistor (RT1)	Ar3	32.1

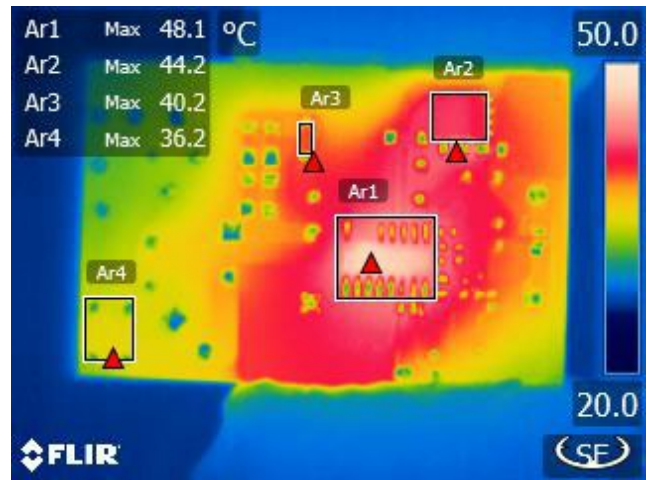


Figure 54 – LinkSwitch-XT2SR Side. 265 VAC, Full Load.

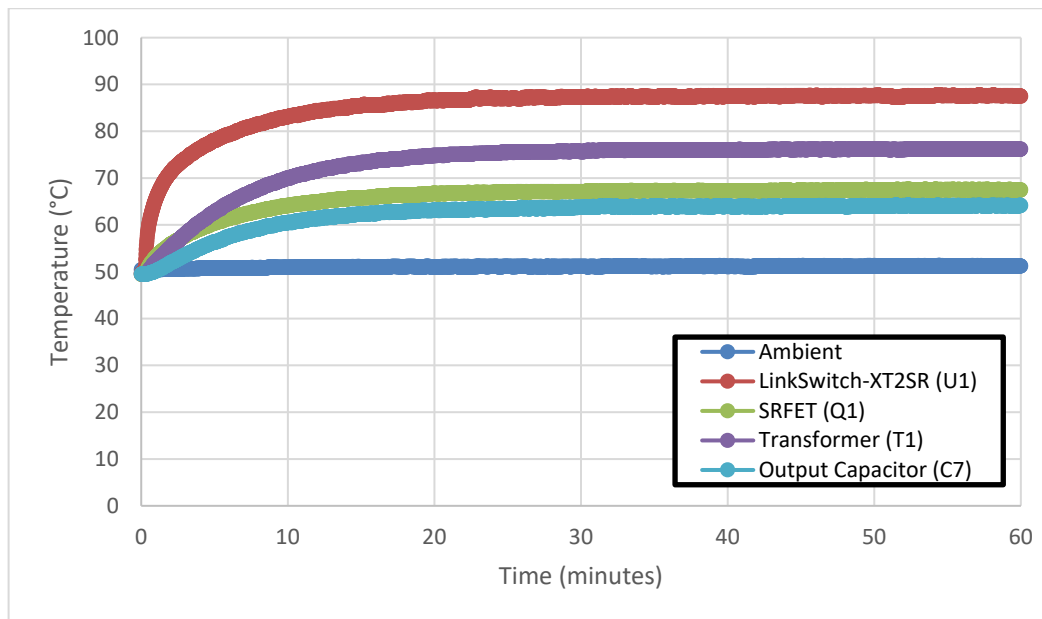
	Reference	°C
Ambient		26.2
LinkSwitch-XT2SR (U1)	Ar1	48.1
SR FET (Q1)	Ar2	44.2
Snubber Diode (D1)	Ar3	40.2
Bridge Diode (BR1)	Ar4	36.2

## 10 Thermal Performance at 50 °C Ambient

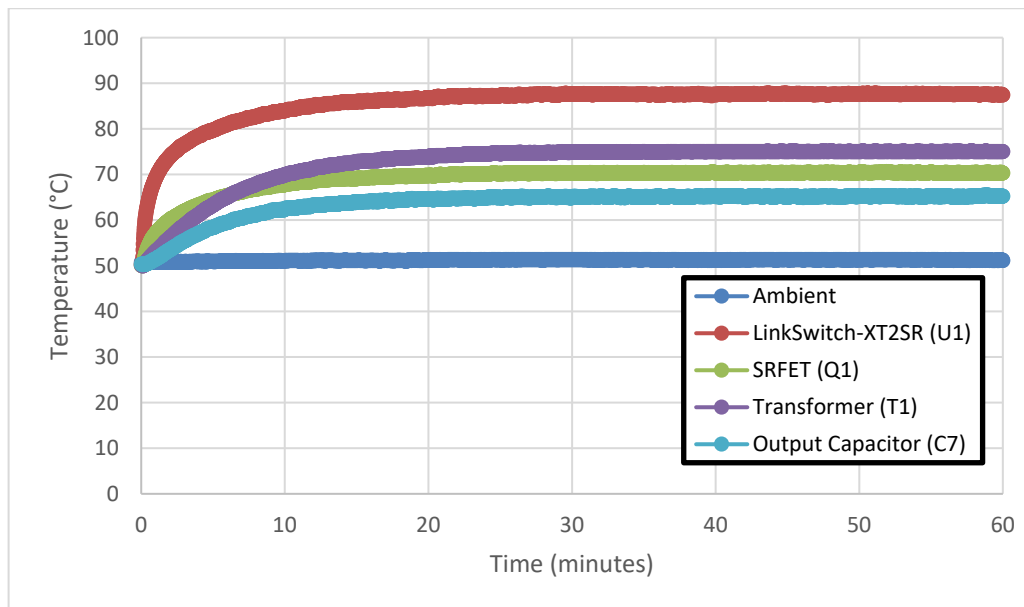
Note: A thermal chamber is used to increase the ambient temperature up to 50 °C. Unit is placed inside a box to prevent air flow. Soak for 1 hour.



**Figure 55** – Thermal Chamber Test Set-up.

**10.1 90 VAC Input, 12 V / 1 A Output ( $v_{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )****Figure 56** – Thermal Profile at 90 VAC Input, Ambient = 50 °C.

	Maximum Temperature °C
<b>Ambient</b>	51.3
<b>LinkSwitch-XT2SR (U1)</b>	87.5
<b>SRFET (Q1)</b>	67.6
<b>Transformer (T1)</b>	76.2
<b>Output Capacitor (C10)</b>	64.2

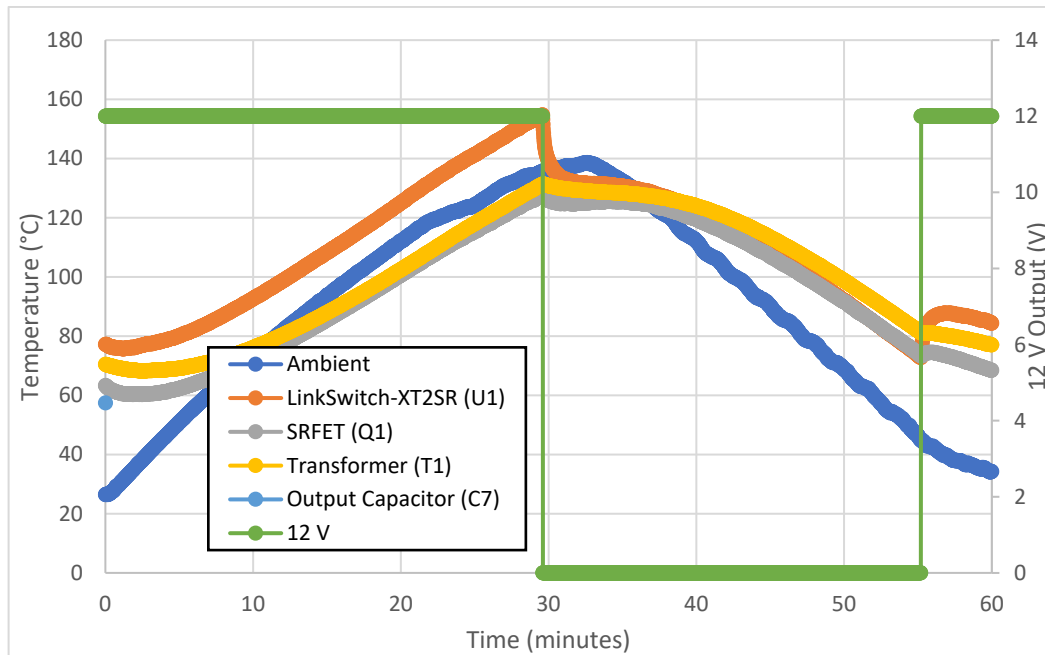
**10.2 265 VAC Input, 12 V / 1 A Output ( $v_{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )****Figure 57** – Thermal Profile at 265 VAC Input, Ambient = 50 °C.

	Maximum Temperature °C
<b>Ambient</b>	51.3
<b>LinkSwitch-XT2SR (U1)</b>	87.8
<b>SRFET (Q1)</b>	70.6
<b>Transformer (T1)</b>	75.1
<b>Output Capacitor (C10)</b>	65.4

## 11 Thermal Shutdown Performance

Note: A thermal chamber is used to increase the ambient temperature until unit goes to thermal shutdown. Unit is placed inside a box to prevent air flow.

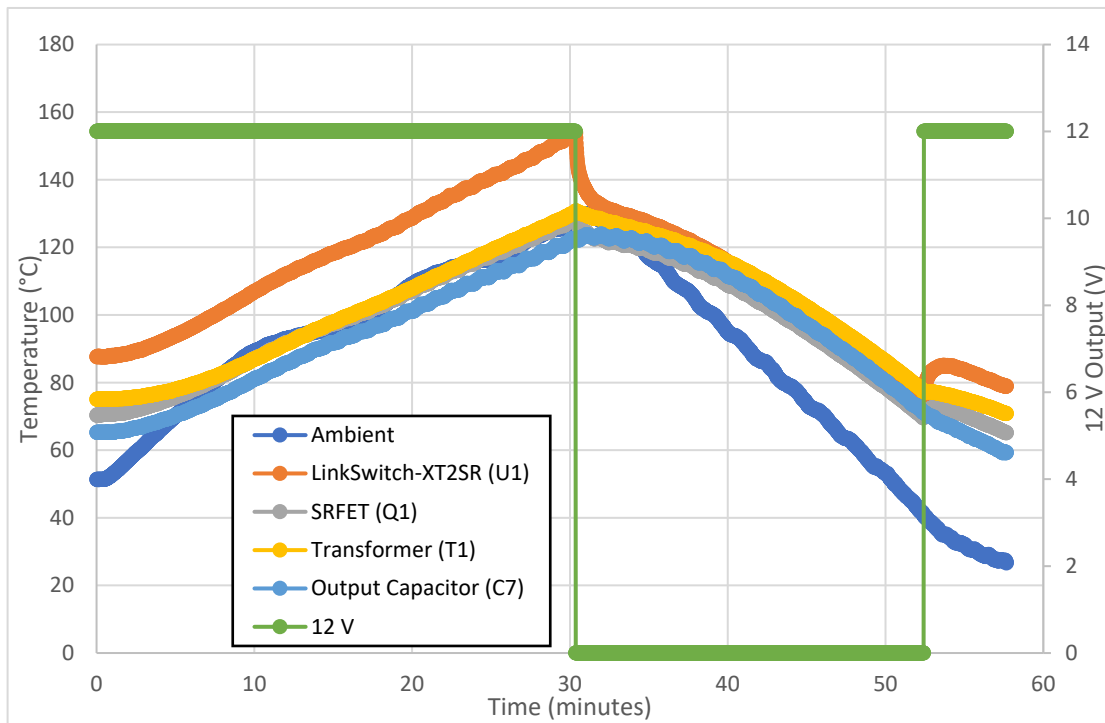
### 11.1 90 VAC Input, 12 V / 1 A Output ( $v_{VCC} = 3.3\text{ V} / 20\text{ mA}$ )



**Figure 58** – Thermal Shutdown Performance at 90 VAC Input.

AC Input	T <sub>SHUTDOWN</sub> (°C)	T <sub>RECOVERY</sub> (°C)	T <sub>HYSTERISIS</sub> (°C)
90 VAC	154.7	75.4	79.3

**11.2 265 VAC Input, 12 V / 1 A Output ( $v_{VCC} = 3.3 V / 20 mA$ )**



**Figure 59 - Thermal Shutdown Performance at 90 VAC Input.**

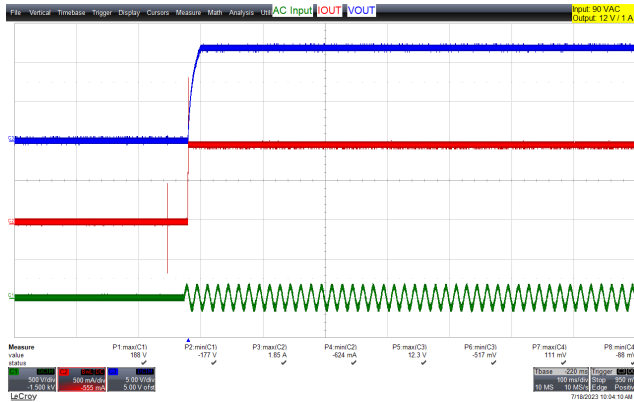
AC Input	T <sub>SHUTDOWN</sub> (°C)	T <sub>RECOVERY</sub> (°C)	T <sub>HYSTERISIS</sub> (°C)
265 VAC	154	75.9	78.1



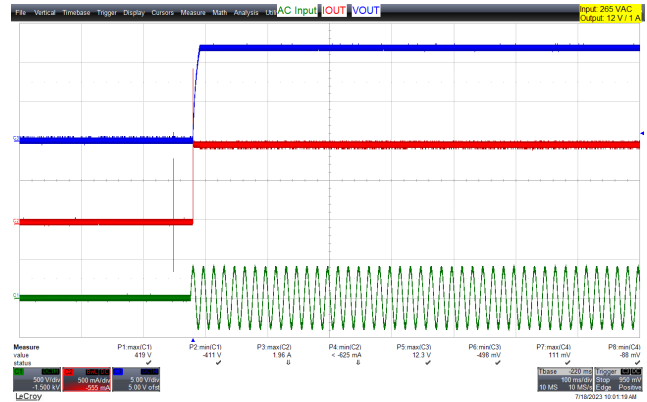
## 12 Waveforms

### 12.1 Output Waveforms During Start-up – CC Load ( $V_{CC} = 3.3\text{ V} / 0\text{ A}$ )

#### 12.1.1 12 V at Full Load Condition

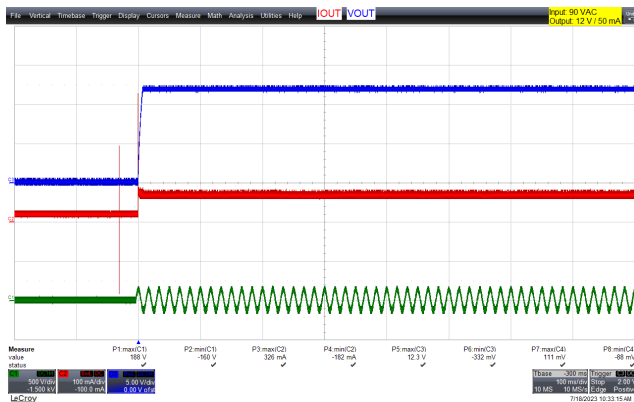


**Figure 60** – Output Voltage and Current Waveforms. 90 VAC Input.  
 Upper: 12  $V_{OUT}$ . 5 V / div.  
 Middle: 12  $I_{OUT}$ , 500 mA / div.  
 Lower: AC Input, 500 V / div.  
 100 ms / div.

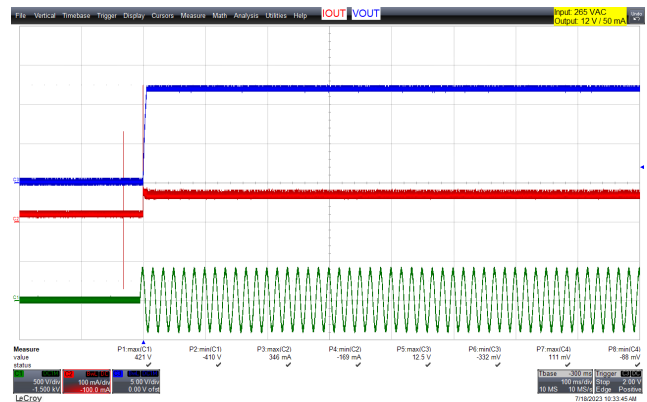


**Figure 61** – Output Voltage and Current Waveforms. 265 VAC Input.  
 Upper: 12  $V_{OUT}$ . 5 V / div.  
 Middle: 12  $I_{OUT}$ , 500 mA / div.  
 Lower: AC Input, 500 V / div.  
 100 ms / div.

#### 12.1.2 12 V at 50 mA Load Condition

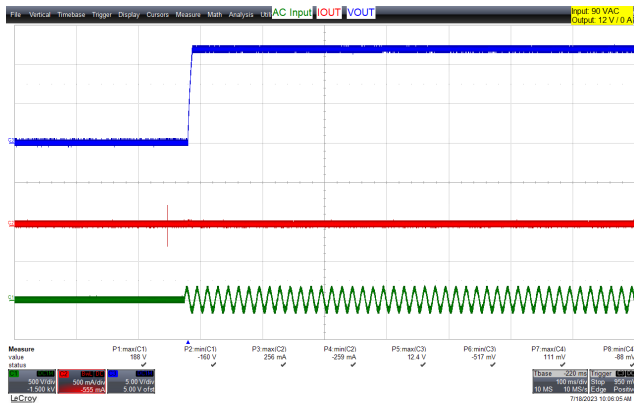


**Figure 62** – Output Voltage and Current Waveforms. 90 VAC Input.  
 Upper: 12  $V_{OUT}$ . 5 V / div.  
 Middle: 12  $I_{OUT}$ , 100 mA / div.  
 Lower: AC Input, 500 V / div.  
 100 ms / div.

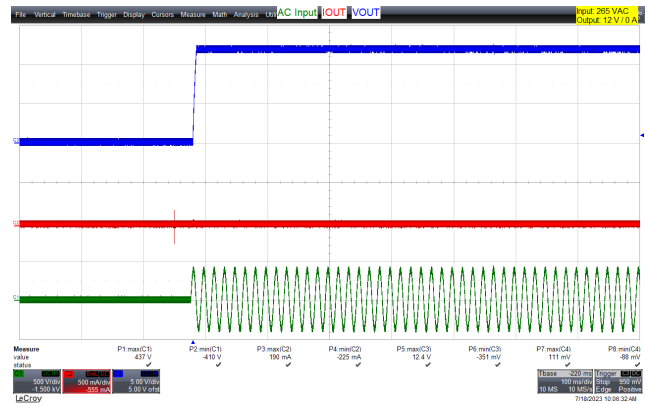


**Figure 63** – Output Voltage and Current Waveforms. 265 VAC Input.  
 Upper: 12  $V_{OUT}$ . 5 V / div.  
 Middle: 12  $I_{OUT}$ , 100 mA / div.  
 Lower: AC Input, 500 V / div.  
 100 ms / div.

### 12.1.3 12 V at No-Load Condition

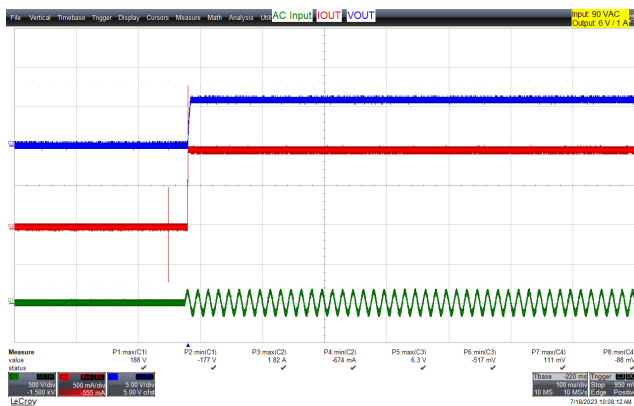


**Figure 64** – Output Voltage and Current Waveforms.  
90 VAC Input.  
Upper: 12  $V_{OUT}$ , 5 V / div.  
Middle: 12  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

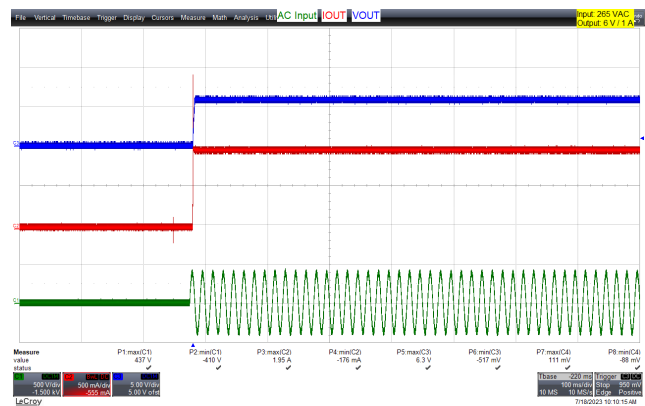


**Figure 65** – Output Voltage and Current Waveforms.  
265 VAC Input.  
Upper: 12  $V_{OUT}$ , 5 V / div.  
Middle: 12  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

### 12.1.4 6 V at Full Load Condition

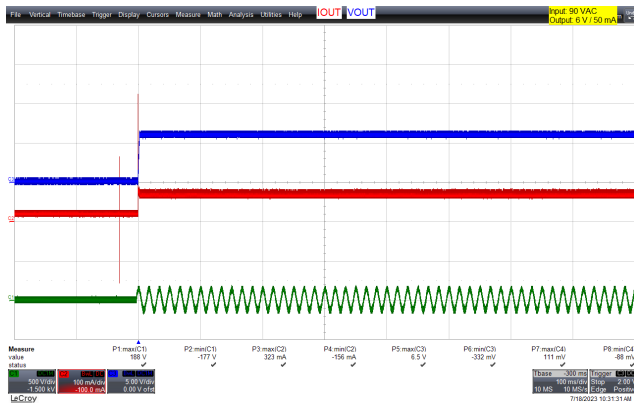


**Figure 66** – Output Voltage and Current Waveforms.  
90 VAC Input.  
Upper: 6  $V_{OUT}$ , 5 V / div.  
Middle: 6  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

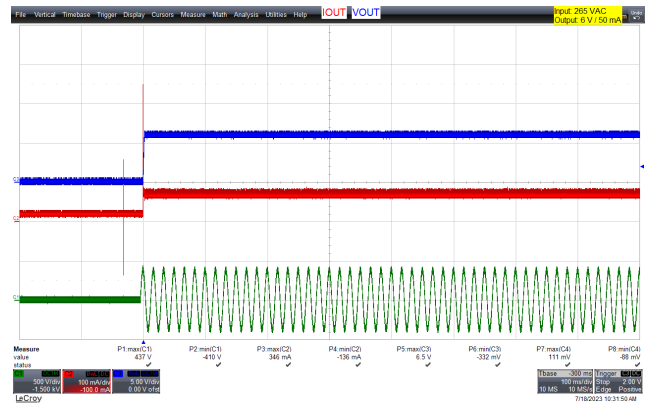


**Figure 67** – Output Voltage and Current Waveforms.  
265 VAC Input.  
Upper: 6  $V_{OUT}$ , 5 V / div.  
Middle: 6  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

### 12.1.5 6 V at 50 mA Load Condition

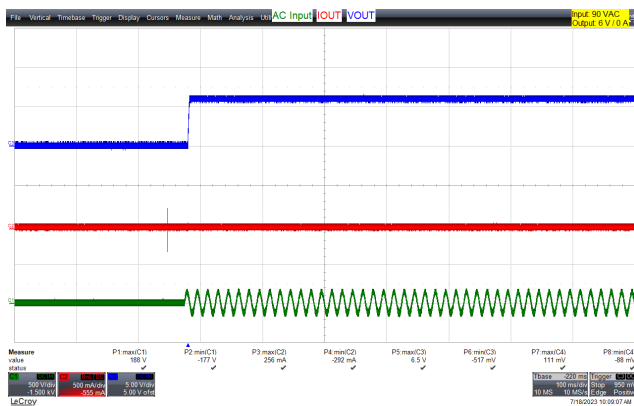


**Figure 68** – Output Voltage and Current Waveforms.  
90 VAC Input.  
Upper: 6  $V_{OUT}$ . 5 V / div.  
Middle: 6  $I_{OUT}$ , 100 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

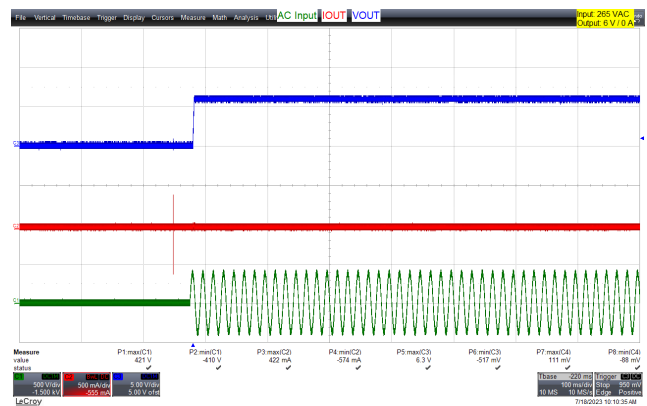


**Figure 69** – Output Voltage and Current Waveforms.  
265 VAC Input.  
Upper: 6  $V_{OUT}$ . 5 V / div.  
Middle: 6  $I_{OUT}$ , 100 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

### 12.1.6 6 V at No-Load Condition



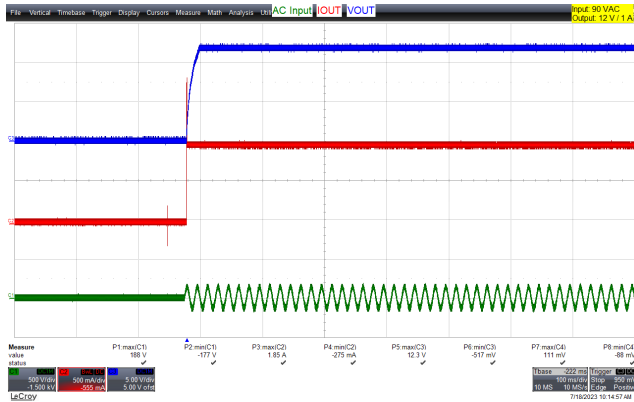
**Figure 70** – Output Voltage and Current Waveforms.  
90 VAC Input.  
Upper: 6  $V_{OUT}$ . 5 V / div.  
Middle: 6  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.



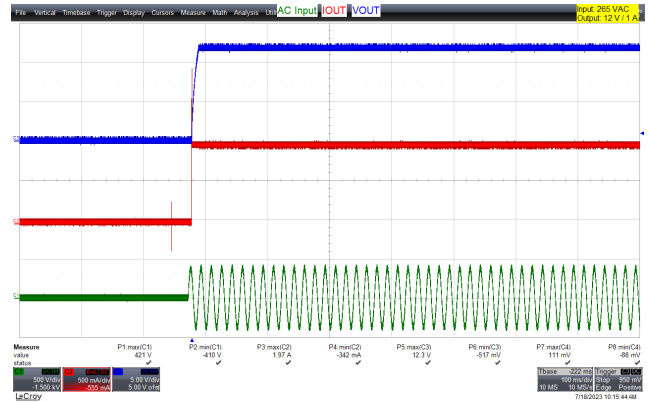
**Figure 71** – Output Voltage and Current Waveforms.  
265 VAC Input.  
Upper: 6  $V_{OUT}$ . 5 V / div.  
Middle: 6  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

## 12.2 Output Waveforms During Start-up – CC Load ( $v_{VCC} = 3.3 \text{ V}/20 \text{ mA}$ )

### 12.2.1 12 V at Full Load Condition

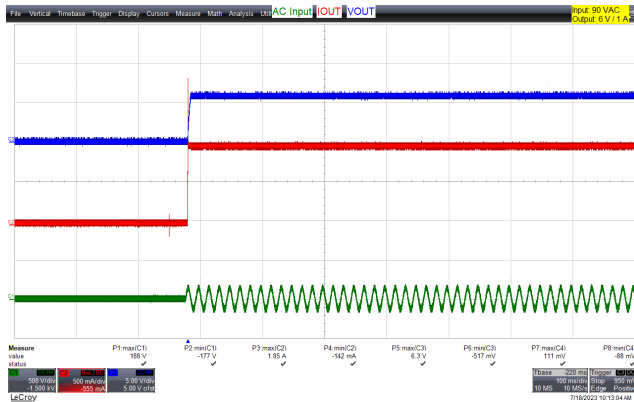


**Figure 72** – Output Voltage and Current Waveforms.  
90 VAC Input.  
Upper: 12  $V_{OUT}$ . 5 V / div.  
Middle: 12  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

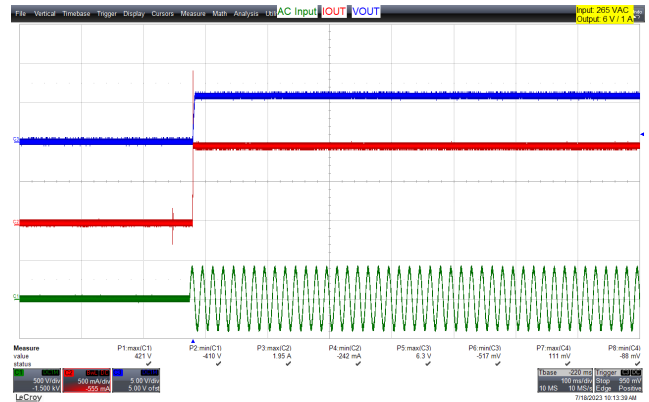


**Figure 73** – Output Voltage and Current Waveforms.  
265 VAC Input.  
Upper: 12  $V_{OUT}$ . 5 V / div.  
Middle: 12  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

### 12.2.2 6 V at Full Load Condition



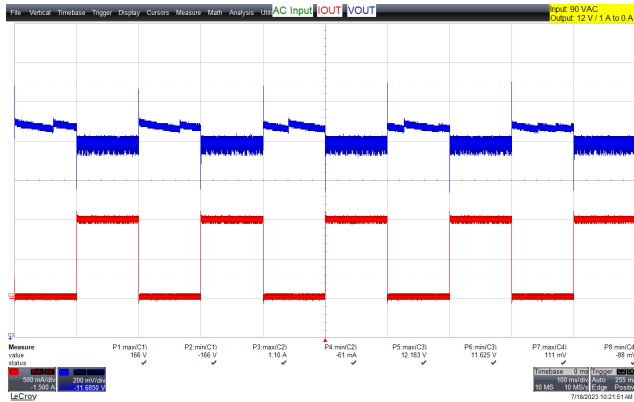
**Figure 74** – Output Voltage and Current Waveforms.  
90 VAC Input.  
Upper: 6  $V_{OUT}$ . 5 V / div.  
Middle: 6  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.



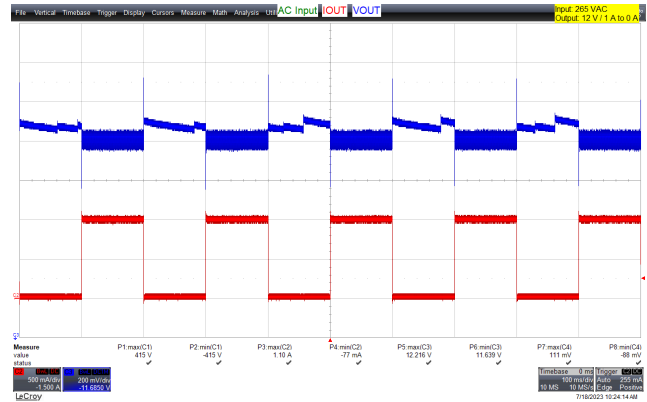
**Figure 75** – Output Voltage and Current Waveforms.  
265 VAC Input.  
Upper: 6  $V_{OUT}$ . 5 V / div.  
Middle: 6  $I_{OUT}$ , 500 mA / div.  
Lower: AC Input, 500 V / div.  
100 ms / div.

## 12.3 Load Transient Response

### 12.3.1 12 V Load Transient



**Figure 76** – 0 A – 1 A, 12 V Load Step Transient Response, 90 VAC.  
 12 V<sub>MAX</sub>: 12.18 V. 12 V<sub>MIN</sub>: 11.63 V.  
 Upper: 12 V<sub>OUT</sub>. 200 mV / div.  
 Lower: 12 I<sub>OUT</sub>, 500 mA / div.  
 100 ms / div.

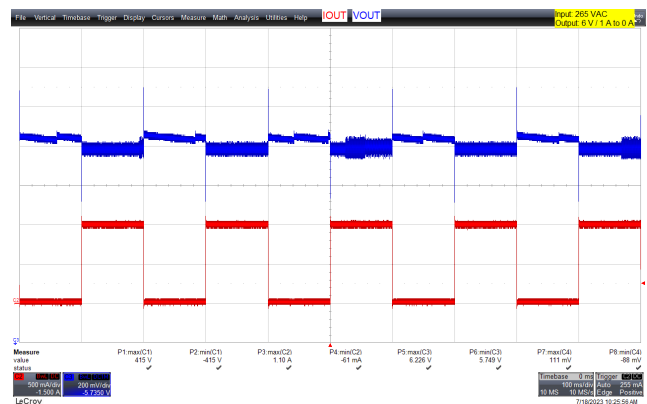


**Figure 77** – 0 A – 1 A, 12 V Load Step Transient Response. 265 VAC.  
 12 V<sub>MAX</sub>: 12.22 V. 12 V<sub>MIN</sub>: 11.64 V.  
 Upper: 12 V<sub>OUT</sub>. 200 mV / div.  
 Lower: 12 I<sub>OUT</sub>, 500 mA / div.  
 100 ms / div.

### 12.3.2 6 V Load Transient



**Figure 78** – 0 A – 1 A, 6 V Load Step Transient Response, 90 VAC.  
 6 V<sub>MAX</sub>: 6.23 V.; 6 V<sub>MIN</sub>: 5.75 V.  
 Upper: 12 V<sub>OUT</sub>. 200 mV / div.  
 Lower: 12 I<sub>OUT</sub>, 500 mA / div.  
 100 ms / div.

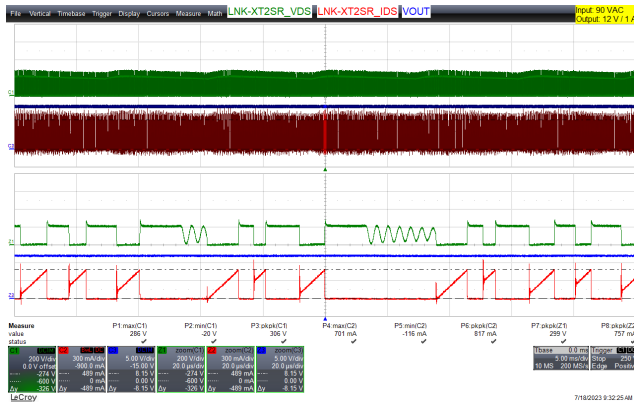


**Figure 79** – 0 A – 1 A, 6 V Load Step Transient Response. 265 VAC.  
 6 V<sub>MAX</sub>: 6.23 V.; 6 V<sub>MIN</sub>: 5.75 V.  
 Upper: 12 V<sub>OUT</sub>. 200 mV / div.  
 Lower: 12 I<sub>OUT</sub>, 500 mA / div.  
 100 ms / div.

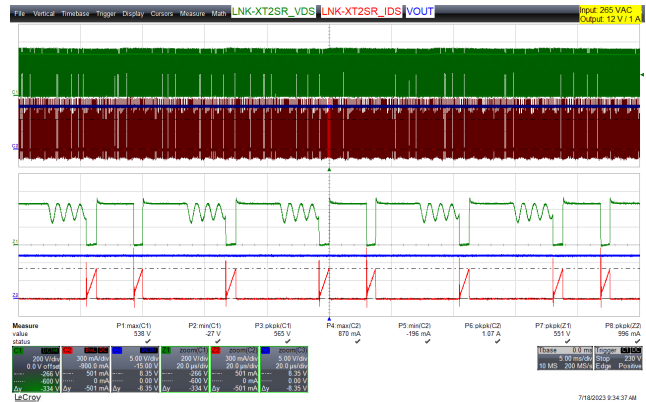
## 12.4 Switching Waveforms

### 12.4.1 LinkSwitch-XT2SR Waveforms During Normal Operation

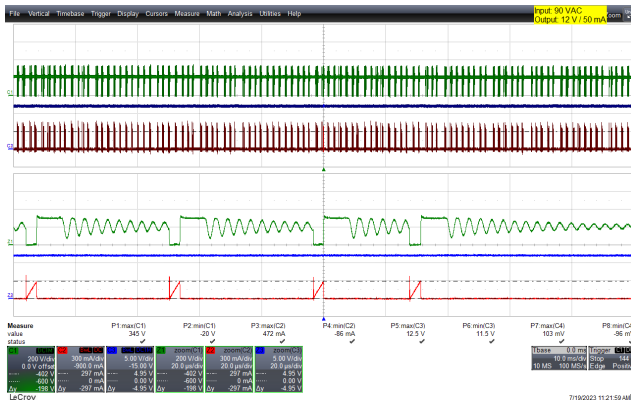
#### 12.4.1.1 12 V Output



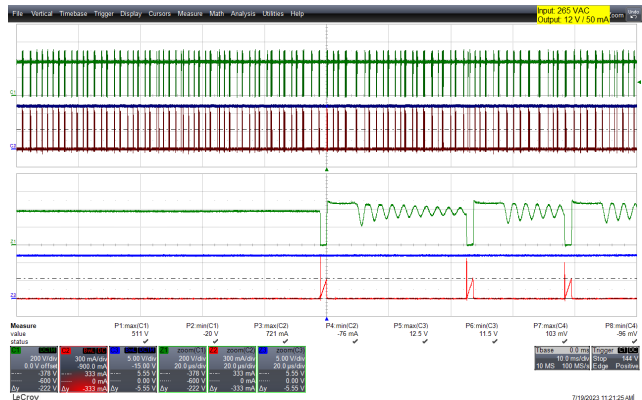
**Figure 80** – Drain Voltage and Current Waveforms. 90 VAC Input, Full Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.



**Figure 81** – Drain Voltage and Current Waveforms. 265 VAC Input, Full Load, (538 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.



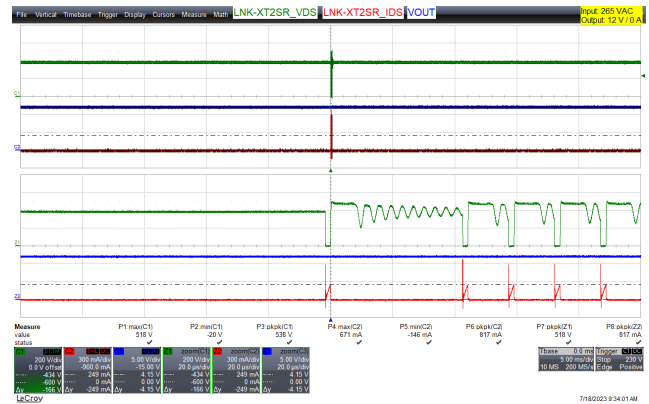
**Figure 82** – Drain Voltage and Current Waveforms. 90 VAC Input, 50 mA Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.



**Figure 83** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (511 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.

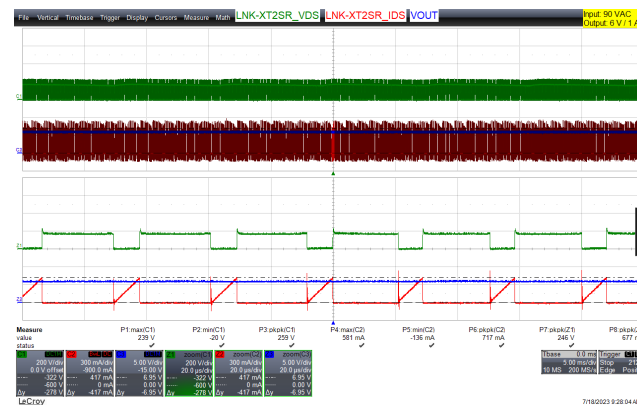


**Figure 84** – Drain Voltage and Current Waveforms. 90 VAC Input, No-Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.

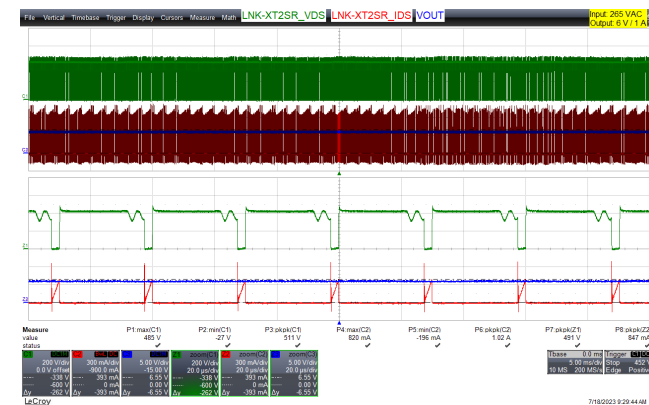


**Figure 85** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (518 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.

### 12.4.1.2 6 V Output

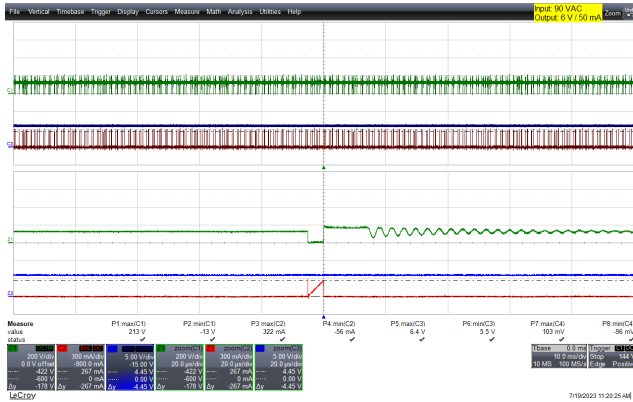


**Figure 86** – Drain Voltage and Current Waveforms. 90 VAC Input, Full Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.

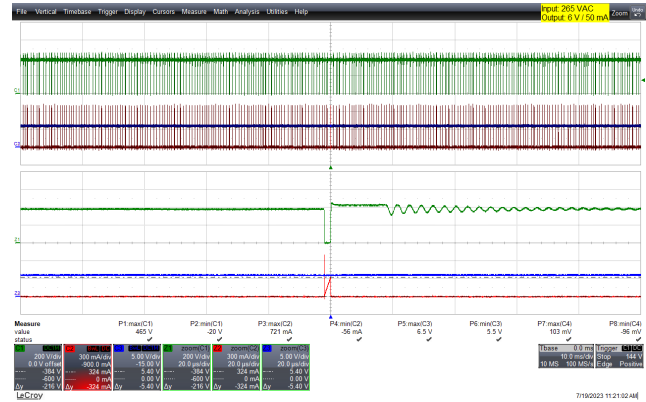


**Figure 87** – Drain Voltage and Current Waveforms. 265 VAC Input, Full Load, (485 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.

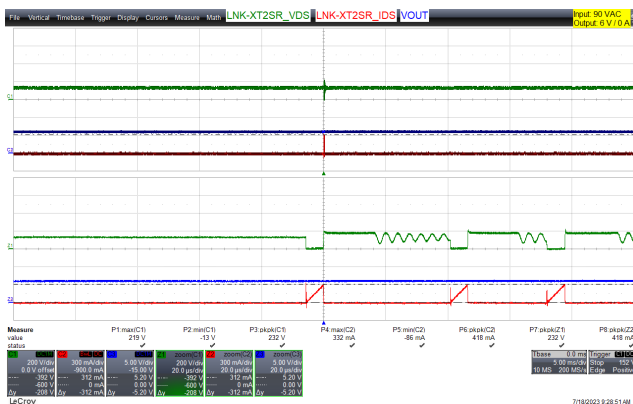




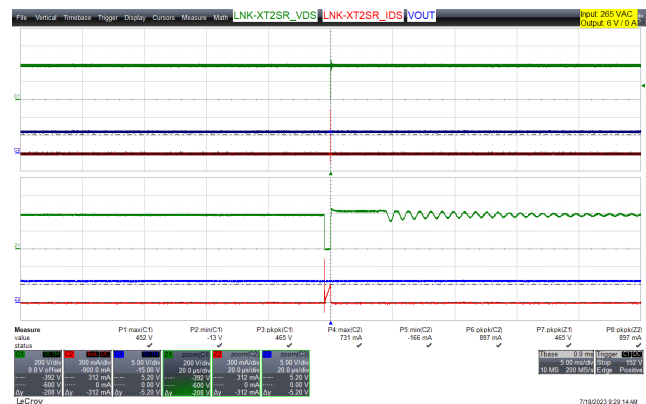
**Figure 88** – Drain Voltage and Current Waveforms. 90 VAC Input, 50 mA Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.



**Figure 89** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (465 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.



**Figure 90** – Drain Voltage and Current Waveforms. 90 VAC Input, No-Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.

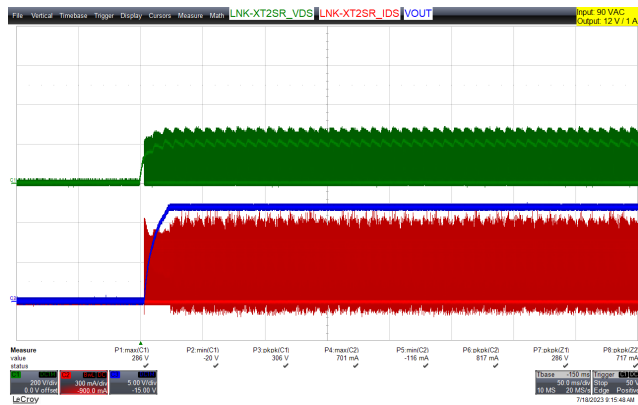


**Figure 91** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (452 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 20 μs / div.

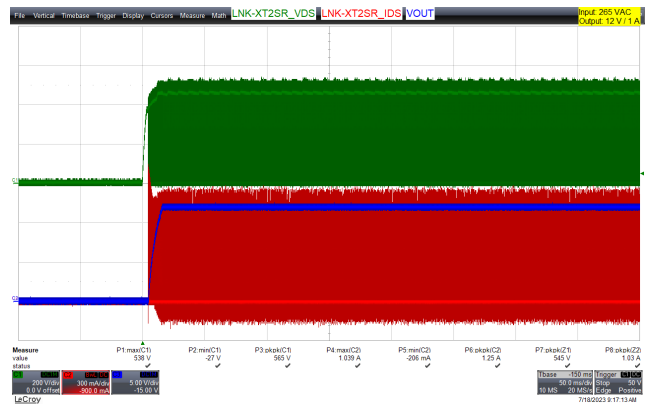


## 12.4.2 LinkSwitch-XT2SR Waveforms During Start-up

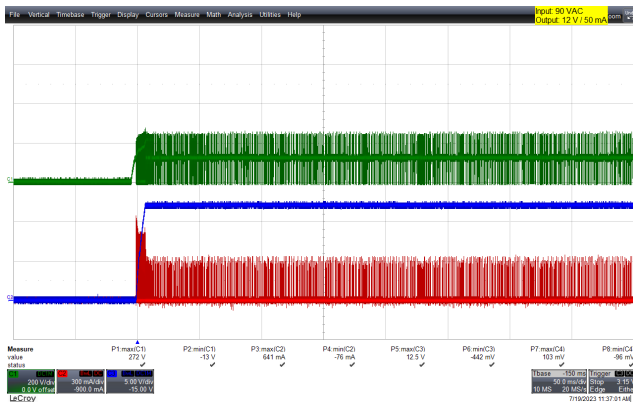
### 12.4.2.1 12 V Output



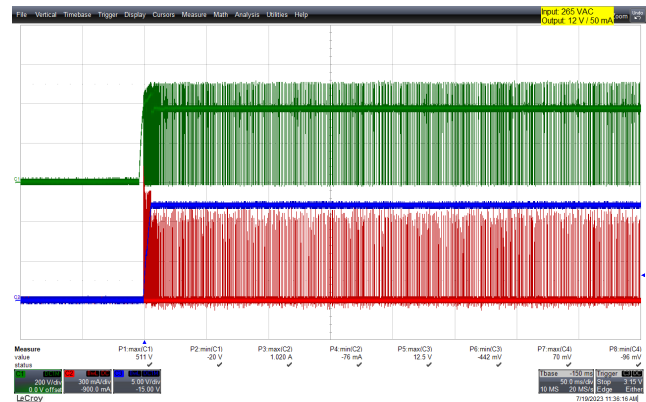
**Figure 92** – Drain Voltage and Current Waveforms. 90 VAC Input, Full Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div.



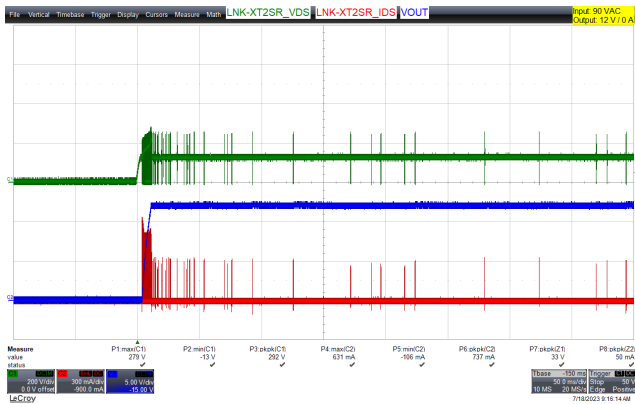
**Figure 93** – Drain Voltage and Current Waveforms. 265 VAC Input, Full Load, (538 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div.



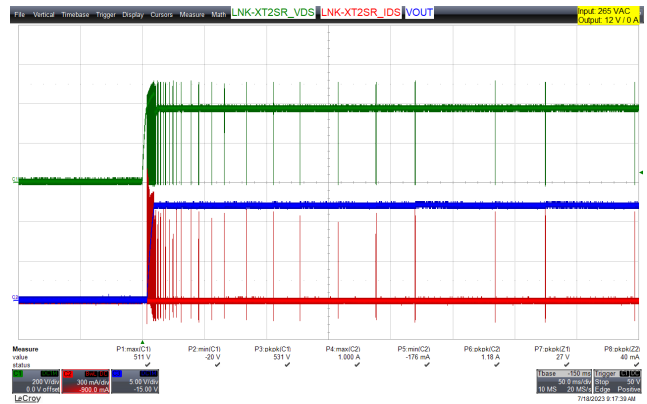
**Figure 94** – Drain Voltage and Current Waveforms. 90 VAC Input, 50 mA Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div.



**Figure 95** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (511 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div..

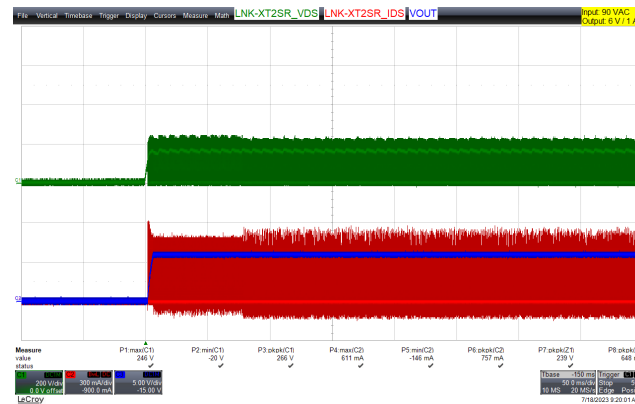


**Figure 96** – Drain Voltage and Current Waveforms. 90 VAC Input, No-Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>, 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 50 ms / div.

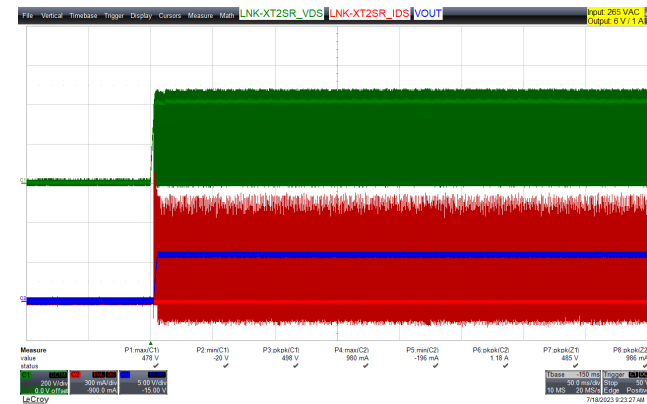


**Figure 97** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (511 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>, 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 50 ms / div.

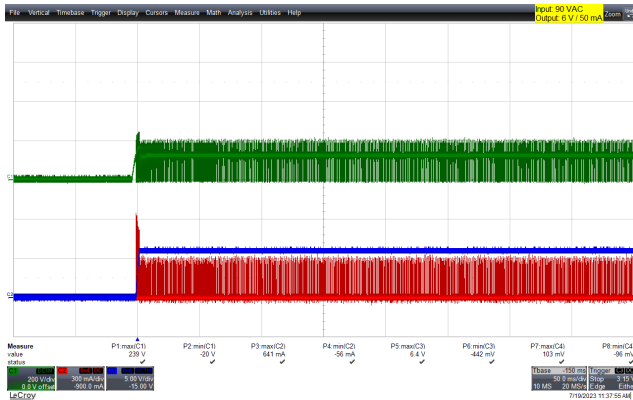
### 12.4.2.2 6 V Output



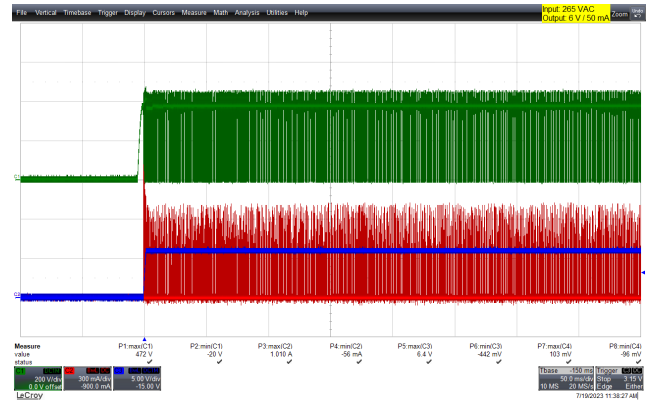
**Figure 98** – Drain Voltage and Current Waveforms. 90 VAC Input, Full Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>, 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 50 ms / div.



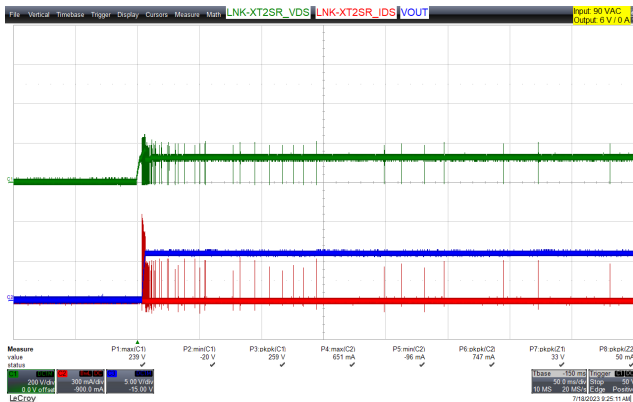
**Figure 99** – Drain Voltage and Current Waveforms. 265 VAC Input, Full Load, (478 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>, 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 50 ms / div.



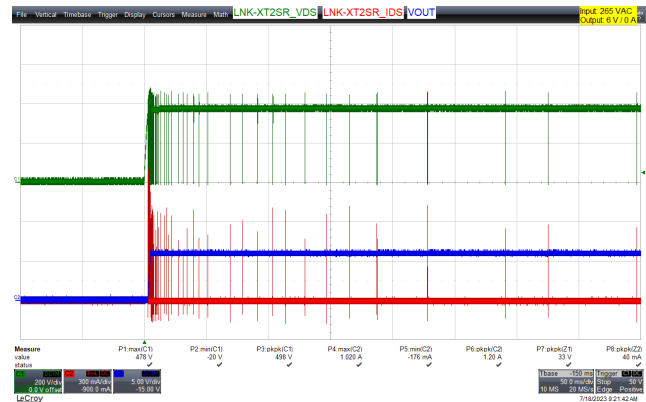
**Figure 100** – Drain Voltage and Current Waveforms. 90 VAC Input, 50 mA Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div.



**Figure 101** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (472 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div..



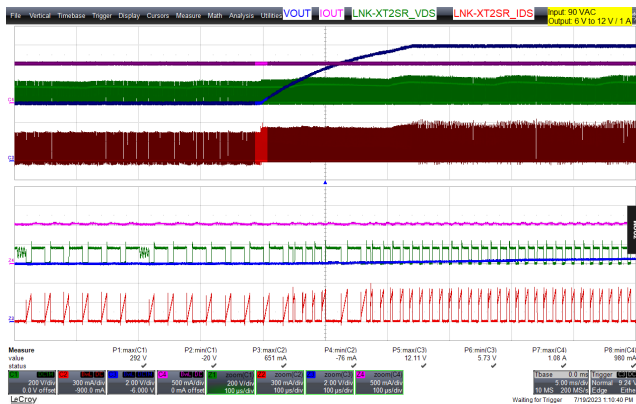
**Figure 102** – Drain Voltage and Current Waveforms. 90 VAC Input, No-Load.  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div.



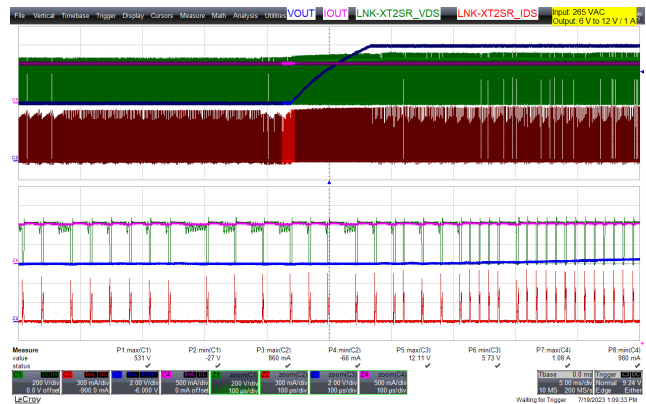
**Figure 103** – Drain Voltage and Current Waveforms. 265 VAC Input, No-Load, (478 V<sub>MAX</sub>).  
 Upper: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div. 50 ms / div.

### 12.4.3 LinkSwitch-XT2SR Waveforms During Output Voltage Transient

#### 12.4.3.1 6 to 12 V Output Full Load



**Figure 104** – Output Voltage Transient Waveforms.  
90 VAC Input, Full Load.  
Upper:  $V_{OUT}$ , 2 V / div.  
Upper Middle:  $I_{OUT}$ , 500 mA / div.  
Lower Middle: LNK-XT2SR\_  $V_{DS}$ . 200 V / div.  
Lower: LNK-XT2SR\_  $I_{DS}$ , 300 mA / div.  
5 ms / div.  
Zoom: 100  $\mu$ s / div.

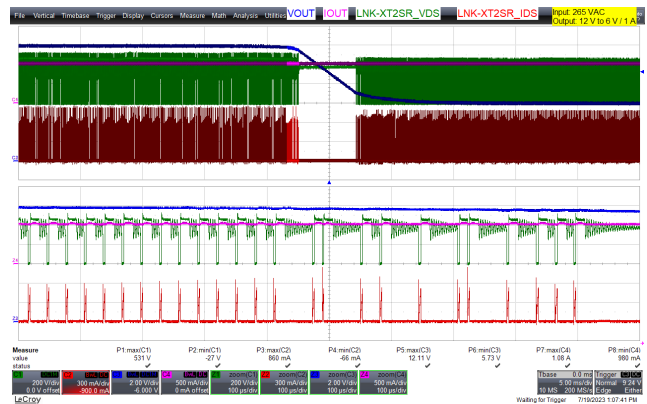


**Figure 105** – Output Voltage Transient Waveforms  
265 VAC Input, Full Load.  
Upper:  $V_{OUT}$ , 2 V / div.  
Upper Middle:  $I_{OUT}$ , 500 mA / div.  
Lower Middle: LNK-XT2SR\_  $V_{DS}$ . 200 V / div.  
Lower: LNK-XT2SR\_  $I_{DS}$ , 300 mA / div.  
5 ms / div.  
Zoom: 100  $\mu$ s / div.

12.4.3.2 12 to 6 V Output Full Load

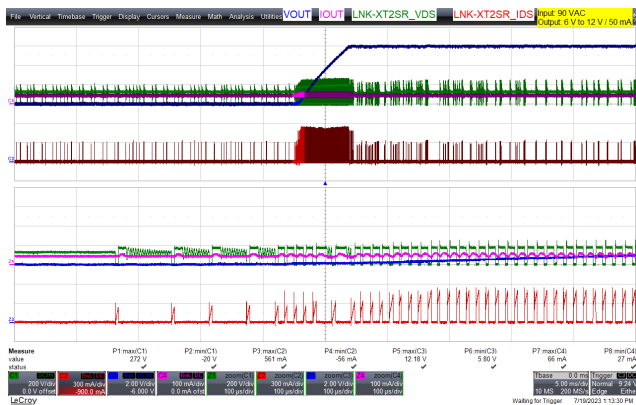


**Figure 106** – Output Voltage Transient Waveforms. 90 VAC Input, Full Load.  
 Upper: V<sub>OUT</sub>, 2 V / div.  
 Upper Middle: I<sub>OUT</sub>, 500 mA / div.  
 Lower Middle: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 100 μs / div.

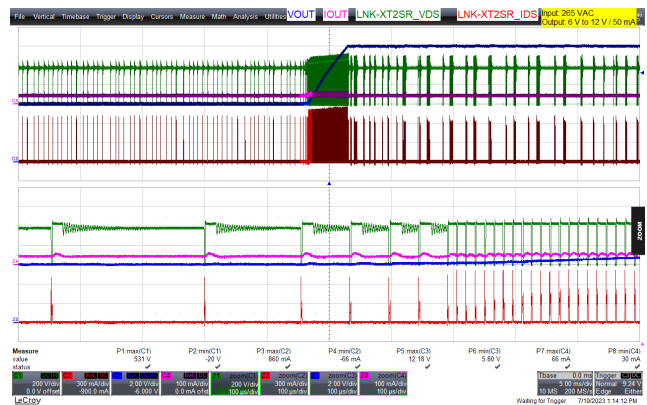


**Figure 107** – Output Voltage Transient Waveforms 265 VAC Input, Full Load.  
 Upper: V<sub>OUT</sub>, 2 V / div.  
 Upper Middle: I<sub>OUT</sub>, 500 mA / div.  
 Lower Middle: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 100 μs / div.

12.4.3.3 6 to 12 V Output 50 mA Load



**Figure 108** – Output Voltage Transient Waveforms. 90 VAC Input, Full Load.  
 Upper: V<sub>OUT</sub>, 2 V / div.  
 Upper Middle: I<sub>OUT</sub>, 100 mA / div.  
 Lower Middle: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 100 μs / div.

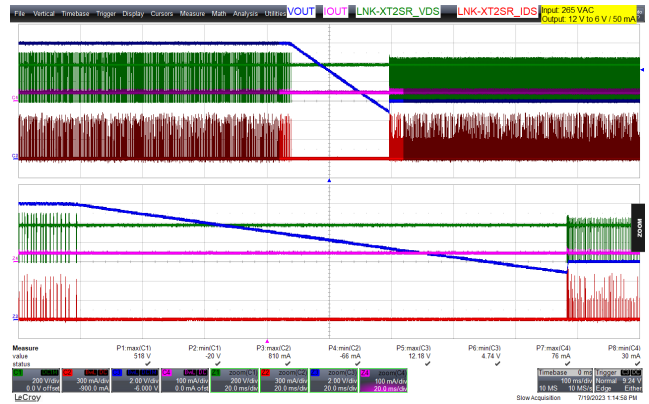


**Figure 109** – Output Voltage Transient Waveforms 265 VAC Input, Full Load.  
 Upper: V<sub>OUT</sub>, 2 V / div.  
 Upper Middle: I<sub>OUT</sub>, 100 mA / div.  
 Lower Middle: LNK-XT2SR\_V<sub>DS</sub>. 200 V / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 5 ms / div.  
 Zoom: 100 μs / div.

12.4.3.4 12 to 6 V Output 50 mA Load



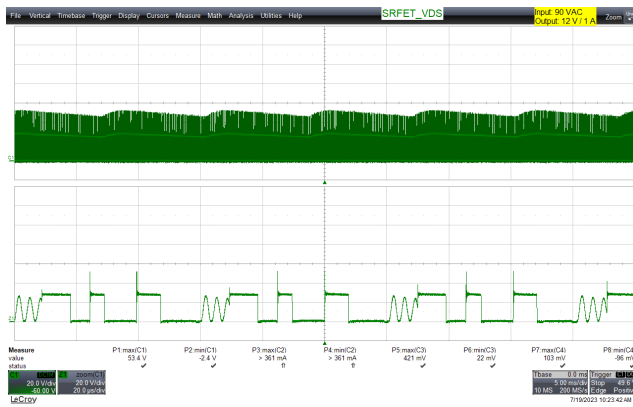
**Figure 110** – Output Voltage Transient Waveforms.  
 90 VAC Input, Full Load.  
 Upper:  $V_{OUT}$ , 2 V / div.  
 Upper Middle:  $I_{OUT}$ , 100 mA / div.  
 Lower Middle: LNK-XT2SR\_  $V_{DS}$ . 200 V / div.  
 Lower: LNK-XT2SR\_  $I_{DS}$ , 300 mA / div.  
 100 ms / div.  
 Zoom: 20 ms / div.



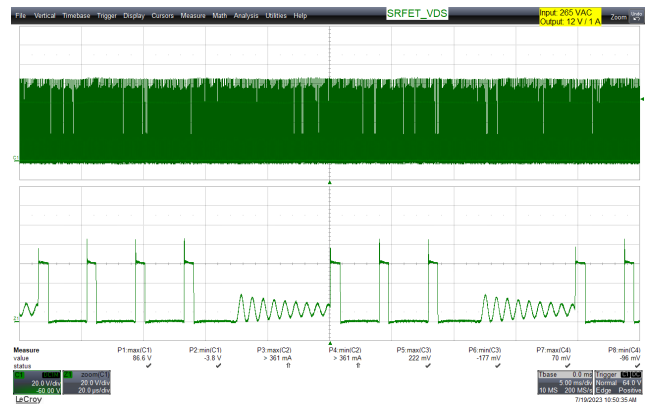
**Figure 111** – Output Voltage Transient Waveforms  
 265 VAC Input, Full Load.  
 Upper:  $V_{OUT}$ , 2 V / div.  
 Upper Middle:  $I_{OUT}$ , 100 mA / div.  
 Lower Middle: LNK-XT2SR\_  $V_{DS}$ . 200 V / div.  
 Lower: LNK-XT2SR\_  $I_{DS}$ , 300 mA / div.  
 100 ms / div.  
 Zoom: 20 ms / div.

### 12.4.4 SRFET Waveforms During Normal Operation

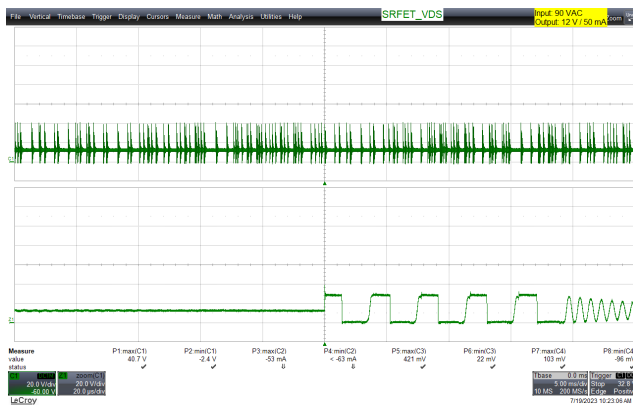
#### 12.4.4.1 12 V Output



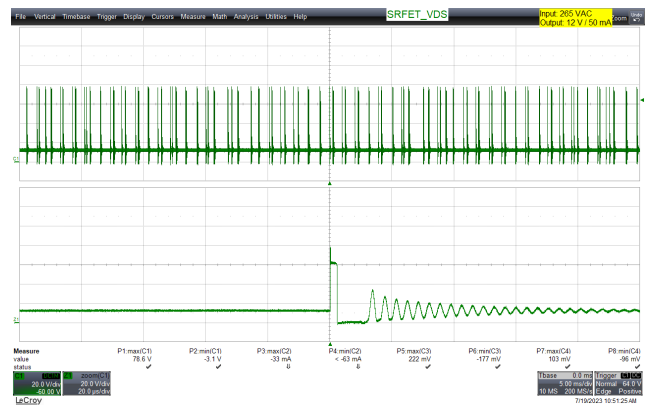
**Figure 112** – SRFET Voltage Waveforms.  
 90 VAC Input, Full Load.  
 Upper: SRFET\_V<sub>DS</sub>. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



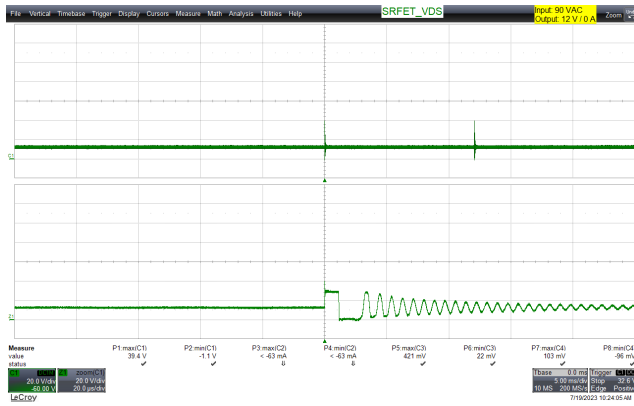
**Figure 113** – SRFET Voltage Waveforms.  
 265 VAC Input, Full Load (86.6 V<sub>MAX</sub>).  
 Upper: SRFET\_V<sub>DS</sub>. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



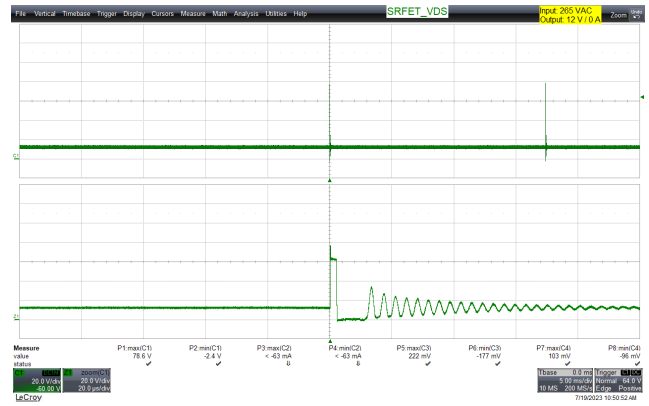
**Figure 114** – SRFET Voltage Waveforms.  
 90 VAC Input, 50 mA Load.  
 Upper: SRFET\_V<sub>DS</sub>. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



**Figure 115** – SRFET Voltage Waveforms.  
 265 VAC Input, 50 mA Load (78.6 V<sub>MAX</sub>).  
 Upper: SRFET\_V<sub>DS</sub>. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.

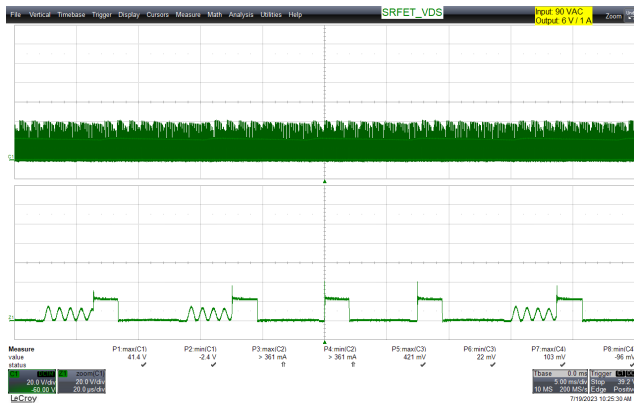


**Figure 116** – SRFET Voltage Waveforms.  
 90 VAC Input, No-Load.  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



**Figure 117** – SRFET Voltage Waveforms.  
 265 VAC Input, No-Load (78.6 V<sub>MAX</sub>).  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.

### 12.4.4.2 6 V Output

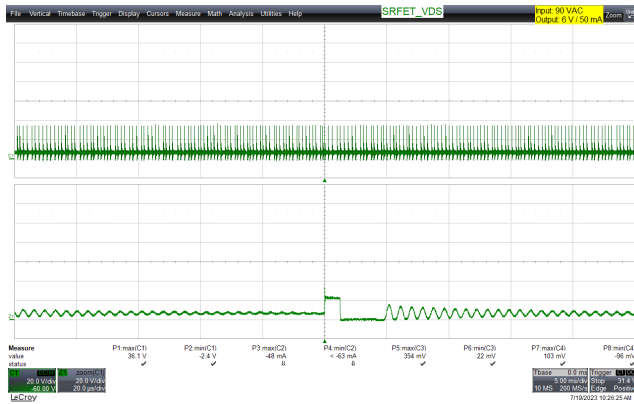


**Figure 118** – SRFET Voltage Waveforms.  
 90 VAC Input, Full Load.  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



**Figure 119** – SRFET Voltage Waveforms.  
 265 VAC Input, Full Load (77.3 V<sub>MAX</sub>).  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.

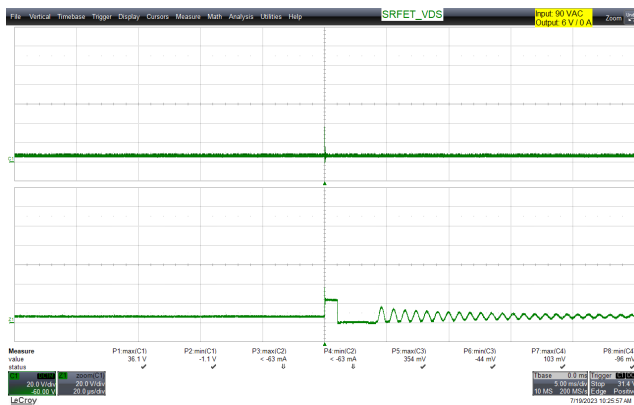




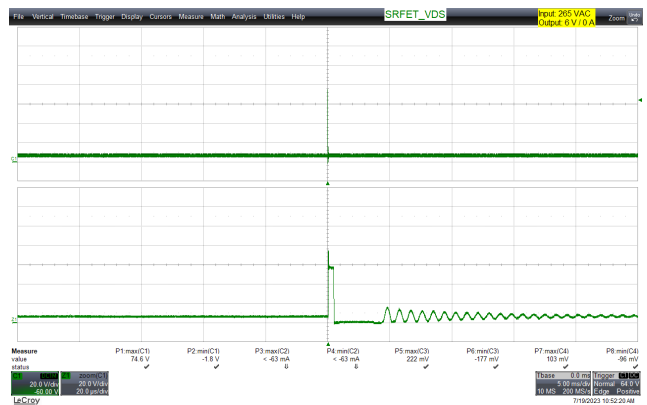
**Figure 120** – SRFET Voltage Waveforms.  
 90 VAC Input, 50 mA Load.  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



**Figure 121** – SRFET Voltage Waveforms.  
 265 VAC Input, 50 mA Load (74.6 V<sub>MAX</sub>).  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



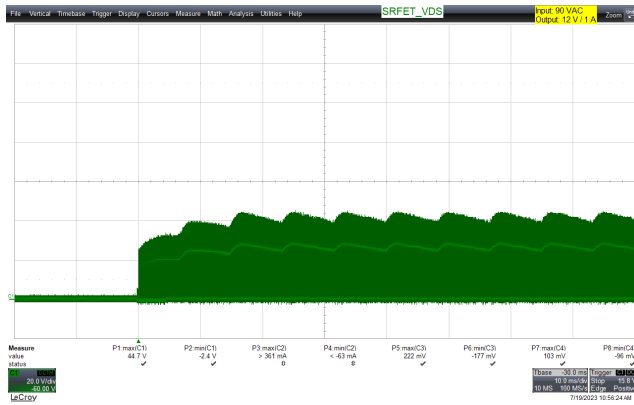
**Figure 122** – SRFET Voltage Waveforms.  
 90 VAC Input, No-Load.  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.



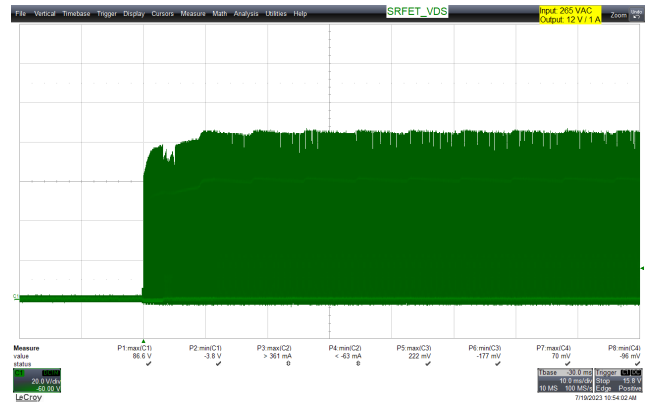
**Figure 123** – SRFET Voltage Waveforms.  
 265 VAC Input, No-Load (74.6 V<sub>MAX</sub>).  
 Upper: SRFET\_Vds. 20 V / div.  
 5 ms / div.  
 Zoom: 20 us / div.

### 12.4.5 SRFET Waveforms During Start-up Operation

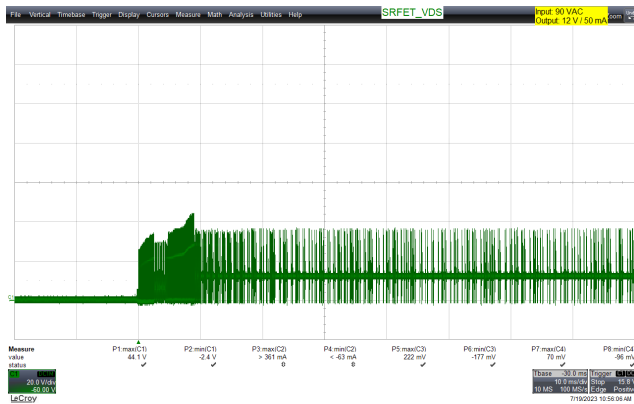
#### 12.4.5.1 12 V Output



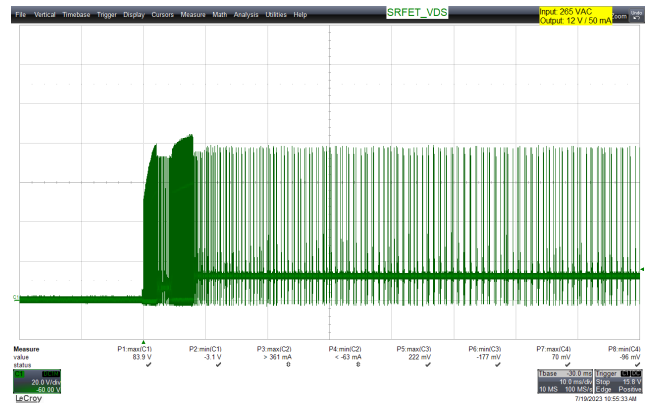
**Figure 124** – SRFET Voltage Waveforms.  
90 VAC Input, Full Load.  
Upper: SRFET\_VDS. 20 V / div.  
10 ms / div.



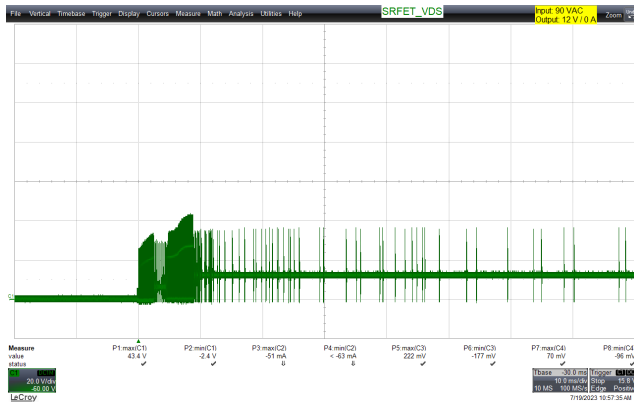
**Figure 125** – SRFET Voltage Waveforms.  
265 VAC Input, Full Load (86.6 V<sub>MAX</sub>).  
Upper: SRFET\_VDS. 20 V / div.  
10 ms / div.



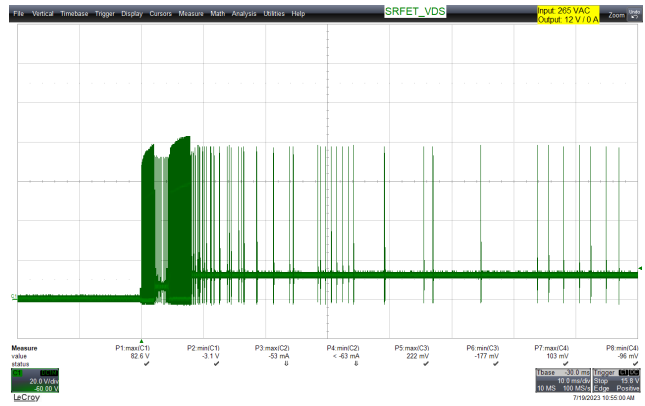
**Figure 126** – SRFET Voltage Waveforms.  
90 VAC Input, 50 mA Load.  
Upper: SRFET\_VDS. 20 V / div.  
10 ms / div.



**Figure 127** – SRFET Voltage Waveforms.  
265 VAC Input, 50 mA Load (83.9 V<sub>MAX</sub>).  
Upper: SRFET\_VDS. 20 V / div.  
10 ms / div.

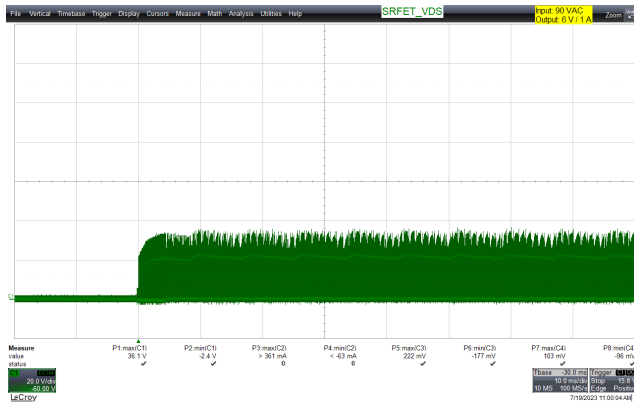


**Figure 128** – SRFET Voltage Waveforms.  
 90 VAC Input, No-Load.  
 Upper: SRFET\_V<sub>DS</sub>. 20 V / div.  
 10 ms / div.

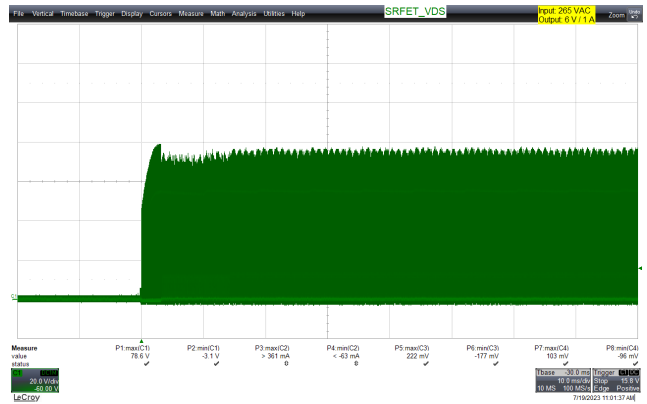


**Figure 129** – SRFET Voltage Waveforms.  
 265 VAC Input, No-Load (82.6 V<sub>MAX</sub>).  
 Upper: SRFET\_V<sub>DS</sub>. 20 V / div.  
 10 ms / div.

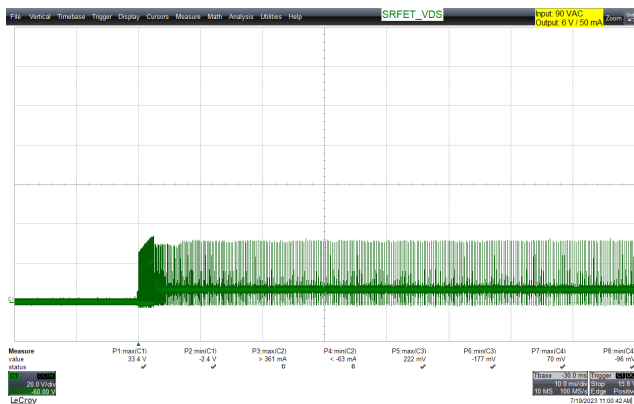
### 12.4.5.2 6 V Output



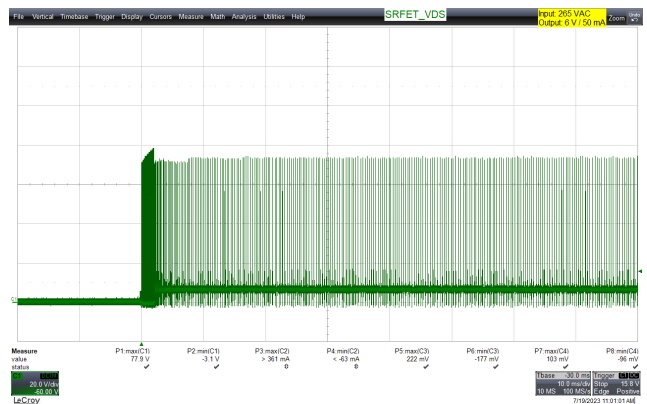
**Figure 130** – SRFET Voltage Waveforms.  
90 VAC Input, Full Load.  
Upper: SRFET\_Vds. 20 V / div.  
10 ms / div.



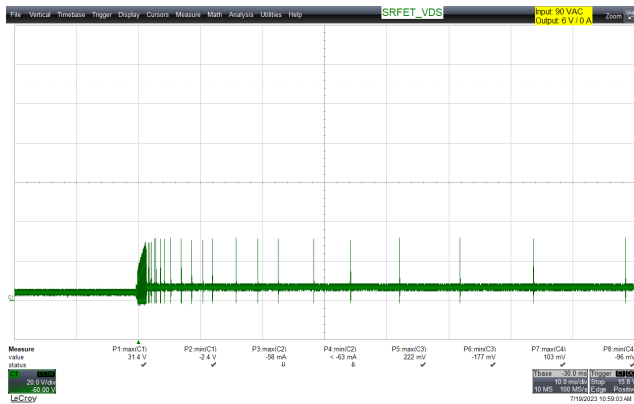
**Figure 131** – SRFET Voltage Waveforms.  
265 VAC Input, Full Load (78.6 V<sub>MAX</sub>).  
Upper: SRFET\_Vds. 20 V / div.  
10 ms / div.



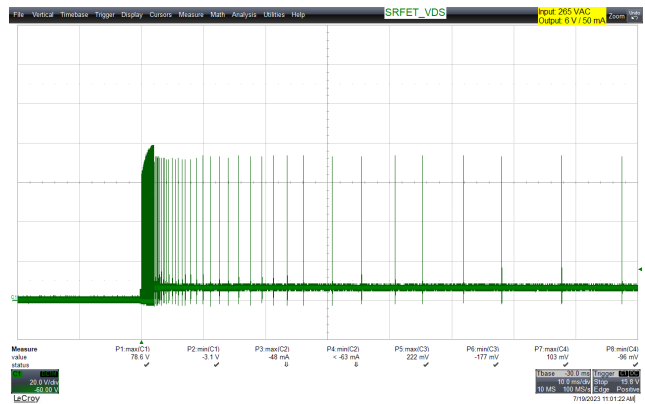
**Figure 132** – SRFET Voltage Waveforms.  
90 VAC Input, 50 mA Load.  
Upper: SRFET\_Vds. 20 V / div.  
10 ms / div.



**Figure 133** – SRFET Voltage Waveforms.  
265 VAC Input, 50 mA Load (77.9 V<sub>MAX</sub>).  
Upper: SRFET\_Vds. 20 V / div.  
10 ms / div.

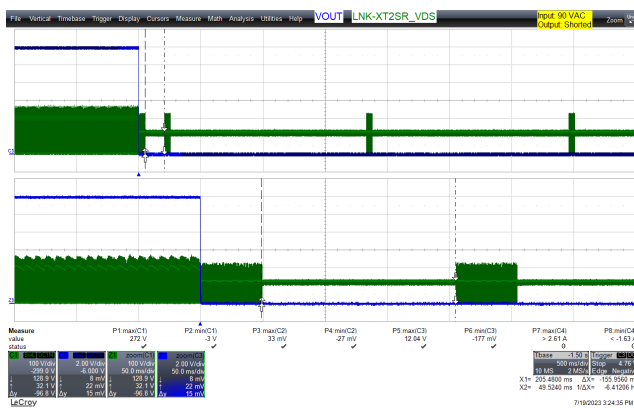


**Figure 134** – SRfet Voltage Waveforms. 90 VAC Input, No-Load.  
Upper: SRfet  $V_{DS}$ . 20 V / div.  
10 ms / div.

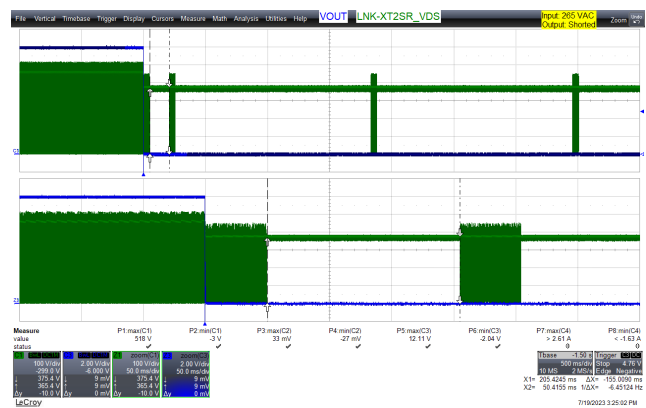


**Figure 135** – SRfet Voltage Waveforms. 265 VAC Input, No-Load (78.6  $V_{MAX}$ ).  
Upper: SRfet  $V_{DS}$ . 20 V / div.  
10 ms / div.

### 12.4.6 Output Voltage and Current Waveform with 12 V Output Shorted

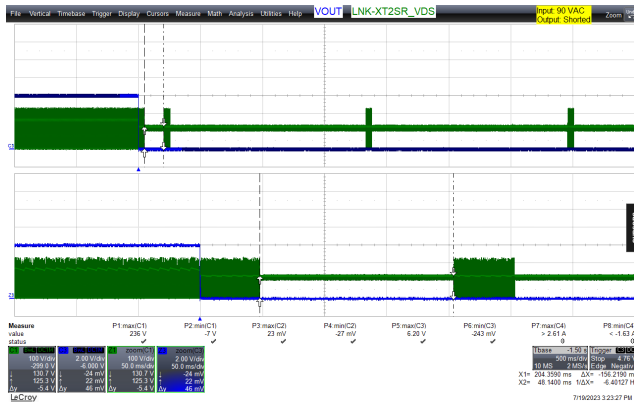


**Figure 136** – Output Voltage and Current Waveforms. 90 VAC Input. Output Shorted.  
Upper: 12  $V_{OUT}$ . 2 V / div.  
Lower: LNK-XT2SR  $V_{DS}$ , 100 V / div.  
500 ms / div.  
Zoom: 50 ms / div.

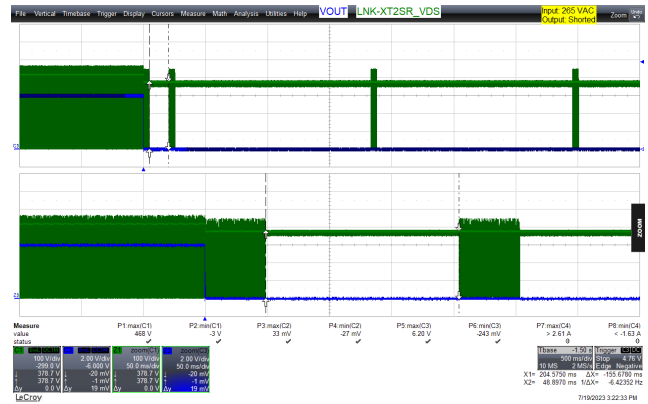


**Figure 137** – Output Voltage and Current Waveforms. 265 VAC Input. Output Shorted.  
Upper: 12  $V_{OUT}$ . 2 V / div.  
Lower: LNK-XT2SR  $V_{DS}$ , 100 V / div.  
500 ms / div.  
Zoom: 50 ms / div.

### 12.4.7 Output Voltage and Current Waveform with 6 V Output Shorted



**Figure 138** – Output Voltage and Current Waveforms. 90 VAC Input. Output Shorted.  
 Upper: 6 V<sub>OUT</sub>. 2 V / div.  
 Lower: LNK-XT2SR\_V<sub>DS</sub>, 100 V / div.  
 500 ms / div.  
 Zoom: 50 ms / div.



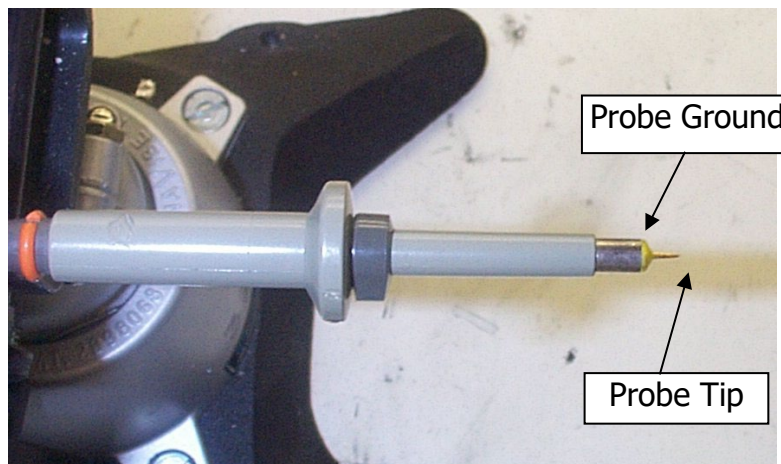
**Figure 139** – Output Voltage and Current Waveforms. 265 VAC Input. Output Shorted.  
 Upper: 6 V<sub>OUT</sub>. 2 V / div.  
 Lower: LNK-XT2SR\_V<sub>DS</sub>, 100 V / div.  
 500 ms / div.  
 Zoom: 50 ms / div.

## 12.5 Output Ripple Measurements

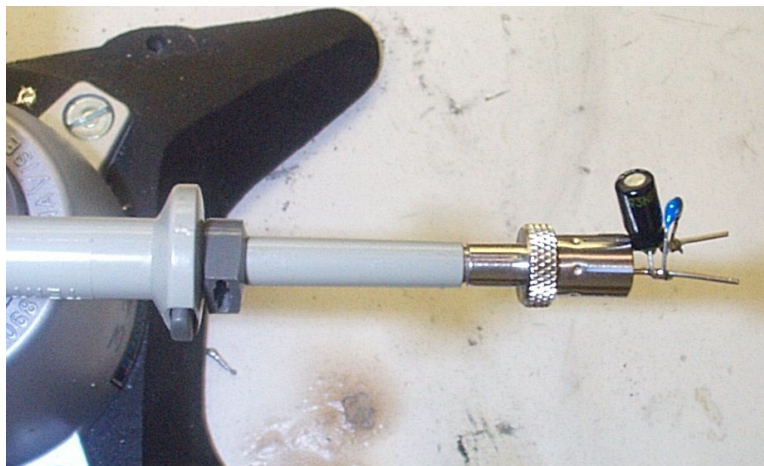
### 12.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1  $\mu\text{F}$ /50 V ceramic type and one (1) 47  $\mu\text{F}$  / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).



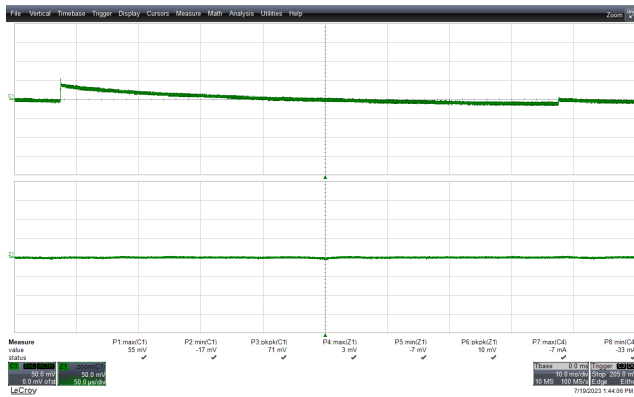
**Figure 140** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



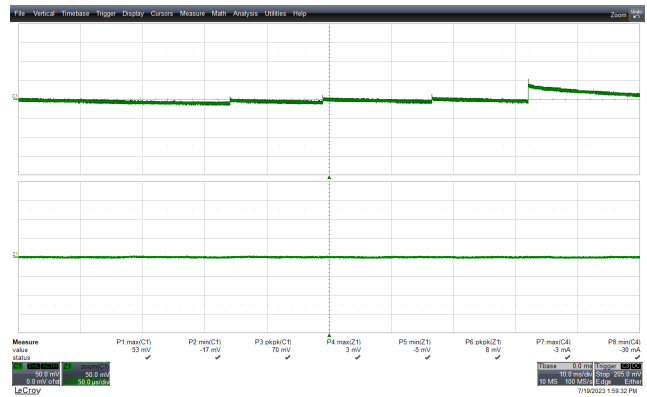
**Figure 141** – Oscilloscope Probe with Probe Master ([www.probemaster.com](http://www.probemaster.com)) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

## 12.5.2 12 V Output Ripple Voltage Waveforms ( $V_{CC} = 3.3 \text{ V} / 0 \text{ A}$ )

### 12.5.2.1 0% Load

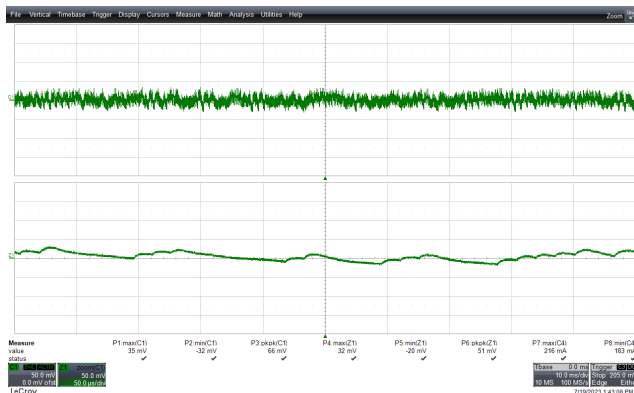


**Figure 142** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 71 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50  $\mu$ s / div.

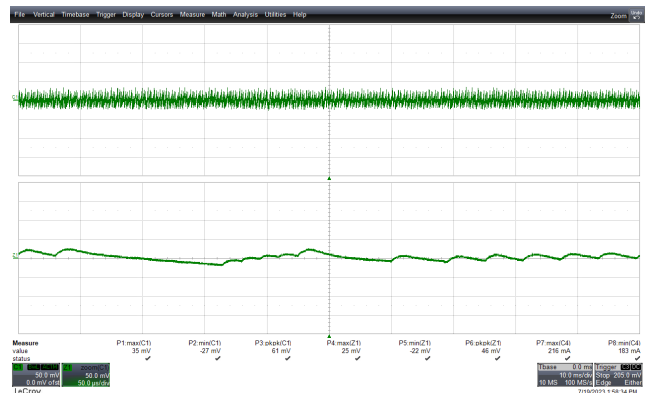


**Figure 143** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 70 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50  $\mu$ s / div.

### 12.5.2.2 25% Load



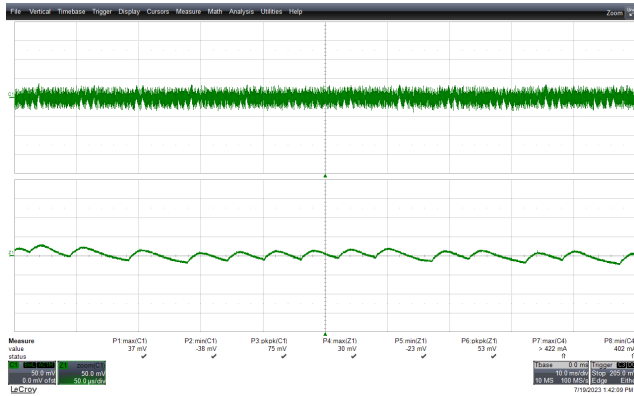
**Figure 144** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 66 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50  $\mu$ s / div.



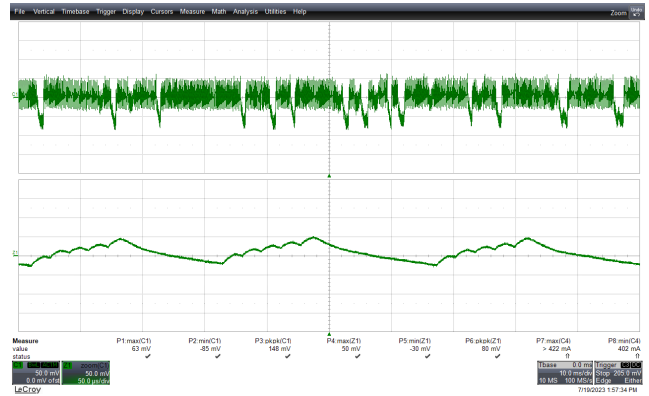
**Figure 145** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 61 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50  $\mu$ s / div.



12.5.2.3 50% Load

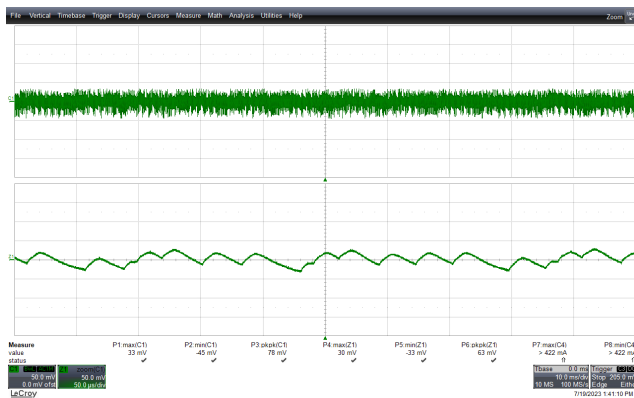


**Figure 146** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 75 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

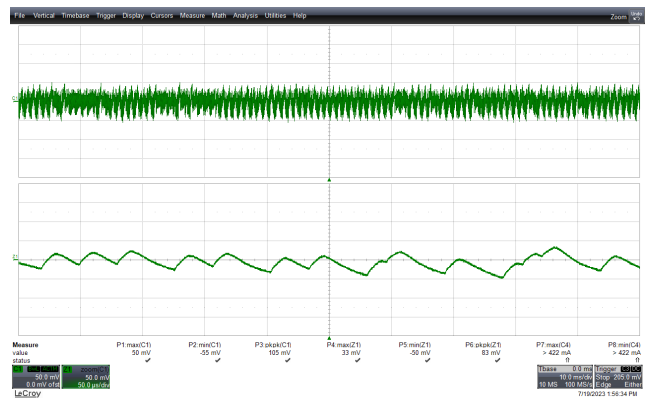


**Figure 147** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 148 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.2.4 75% Load

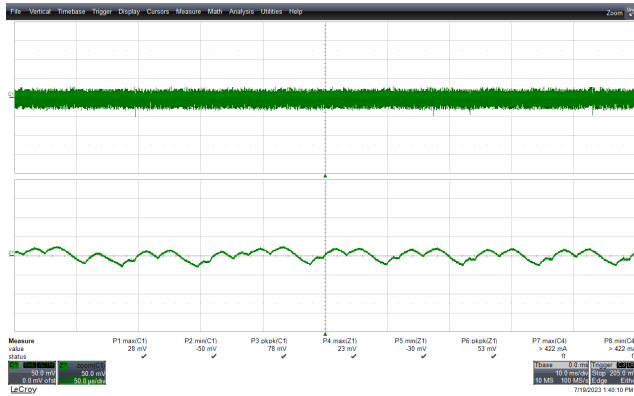


**Figure 148** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 78 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

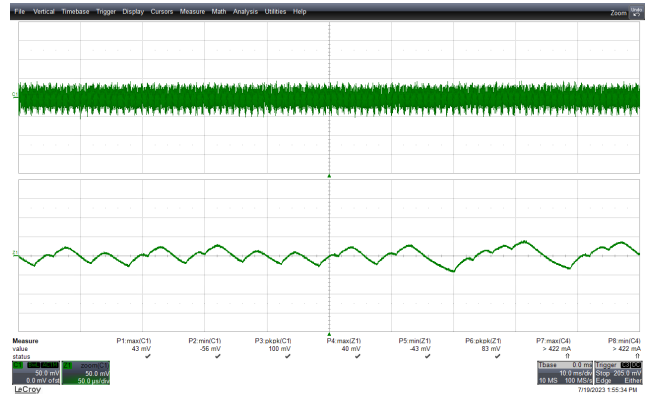


**Figure 149** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 105 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.2.5 100% Load



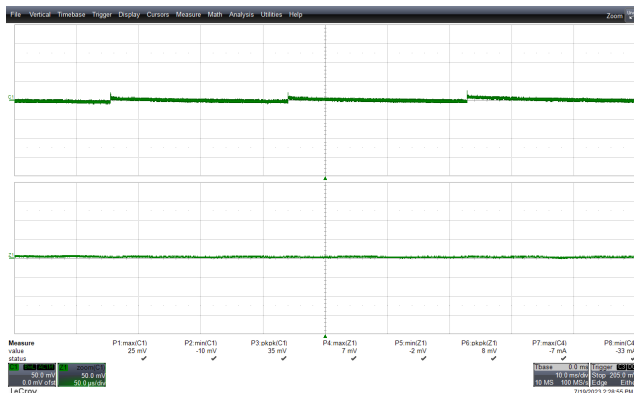
**Figure 150** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 78 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.



**Figure 151** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 100 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.3 6 V Output Ripple Voltage Waveforms (uVCC = 3.3 V / 0 A)

12.5.3.1 0% Load

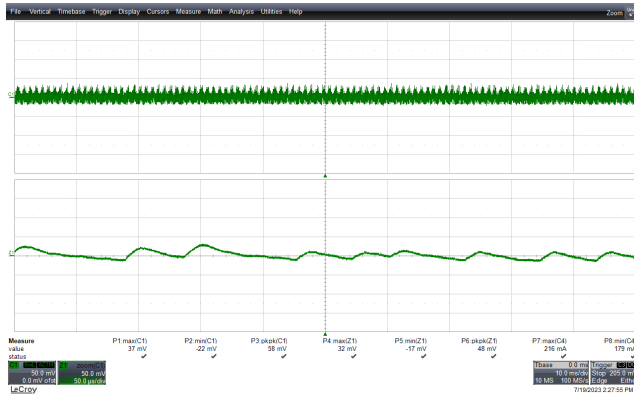


**Figure 152** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 35 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

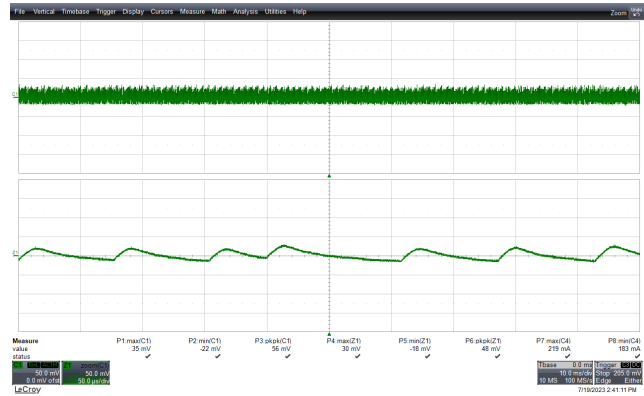


**Figure 153** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 43 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.3.2 25% Load

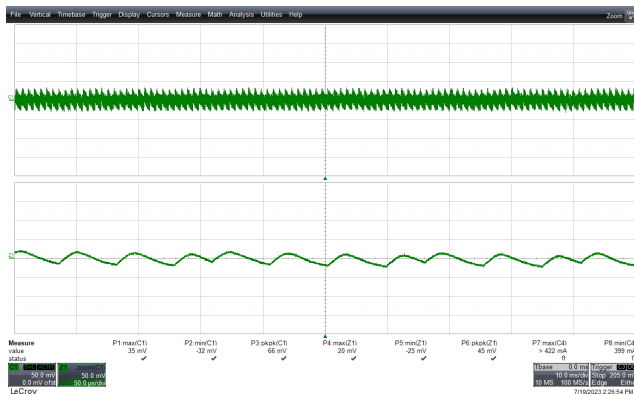


**Figure 154** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 58 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

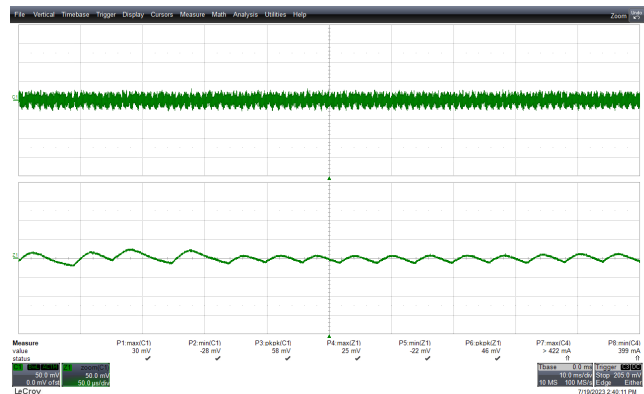


**Figure 155** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 56 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.3.3 50% Load

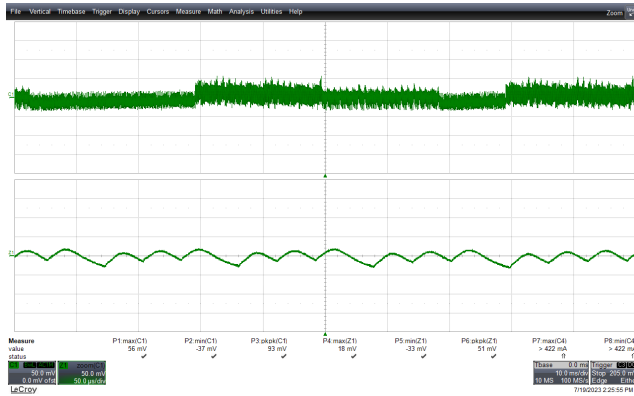


**Figure 156** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 66 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

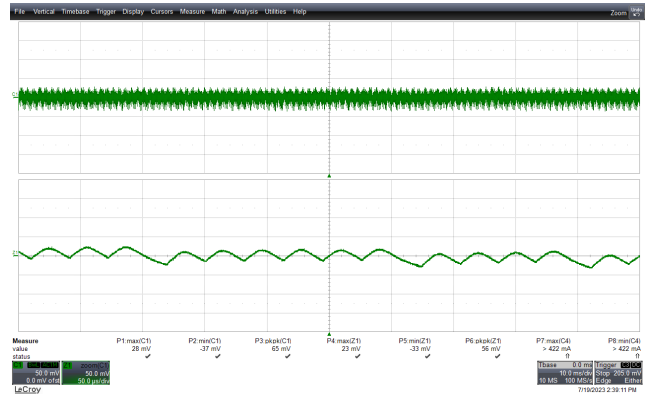


**Figure 157** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 58 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.3.4 75% Load

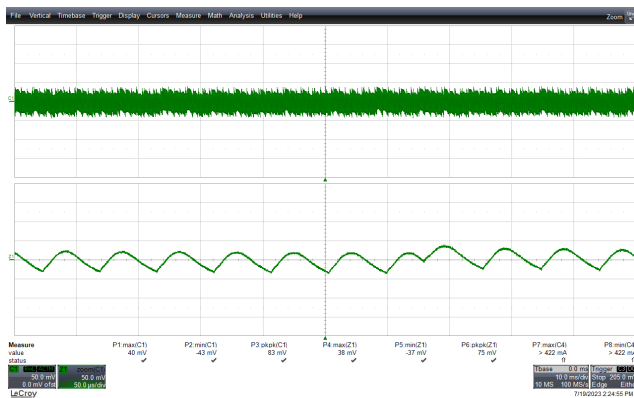


**Figure 158** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 93 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

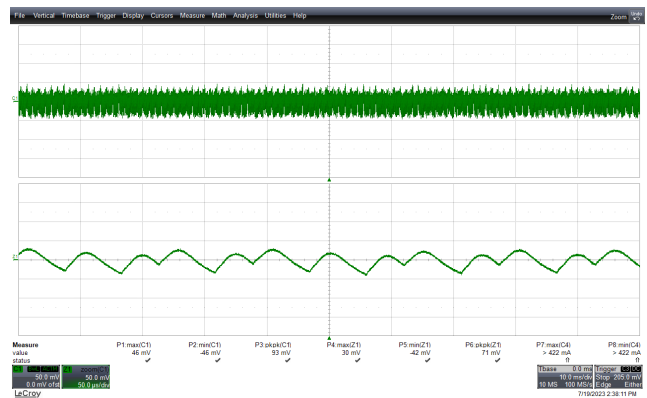


**Figure 159** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 65 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.3.5 100% Load



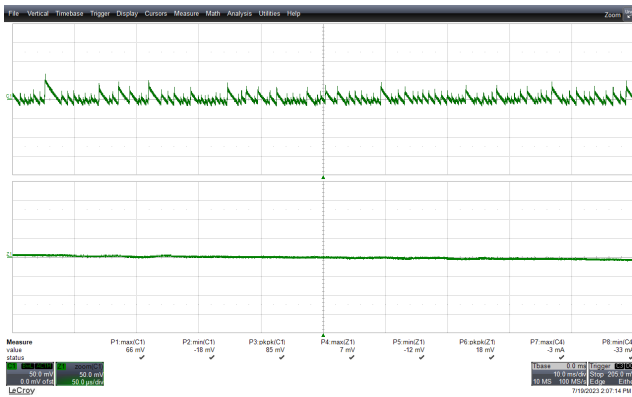
**Figure 160** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 83 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.



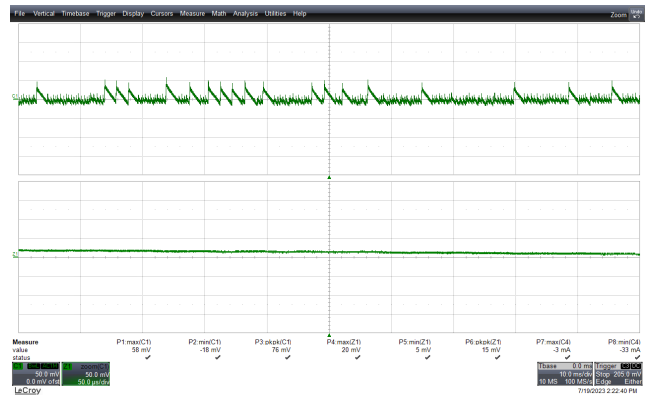
**Figure 161** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 93 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.5 12 V Output Ripple Voltage Waveforms ( $V_{CC} = 3.3 \text{ V} / 20 \text{ mA}$ )

12.5.5.1 0% Load

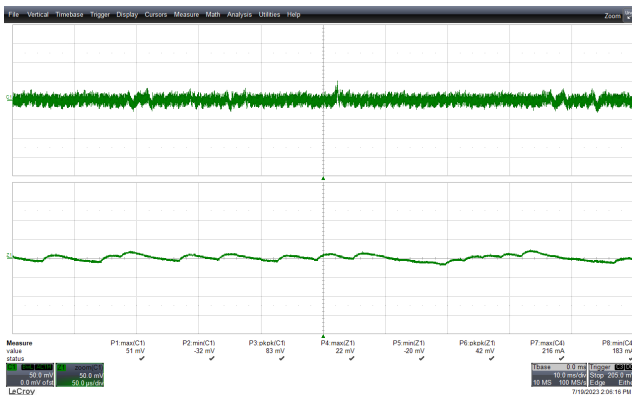


**Figure 162** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 85 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

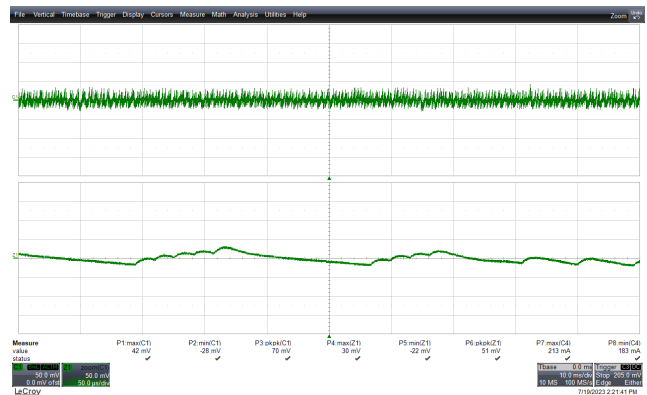


**Figure 163** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 76 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.5.2 25% Load

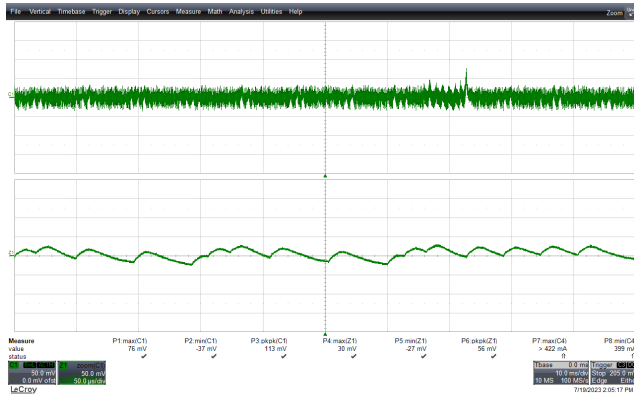


**Figure 164** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 83 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

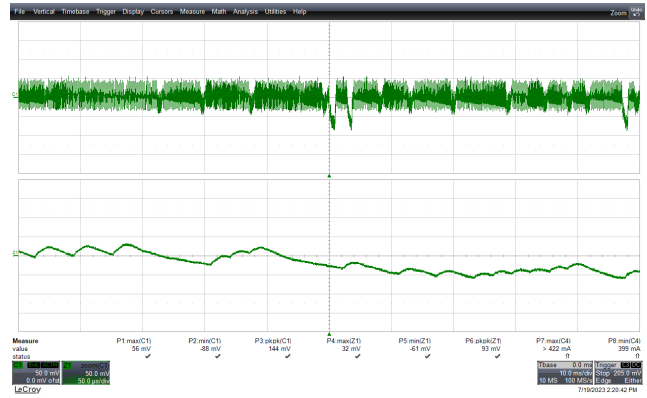


**Figure 165** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 70 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.5.3 50% Load

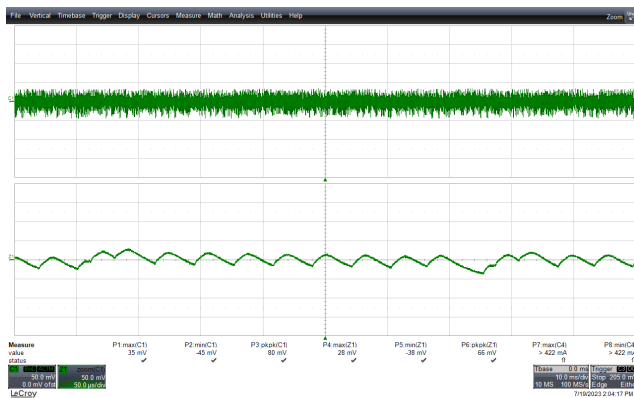


**Figure 166** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 113 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

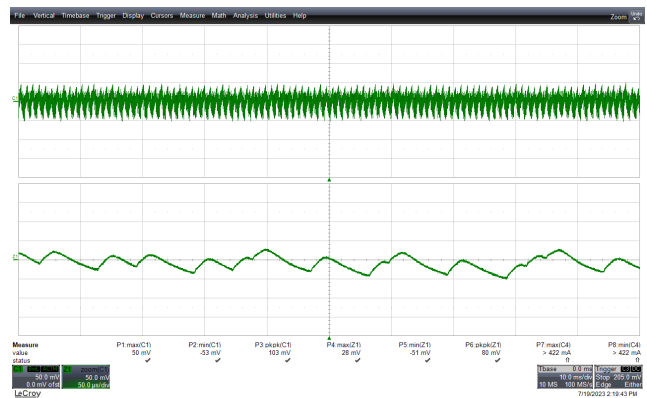


**Figure 167** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 144 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.5.4 75% Load

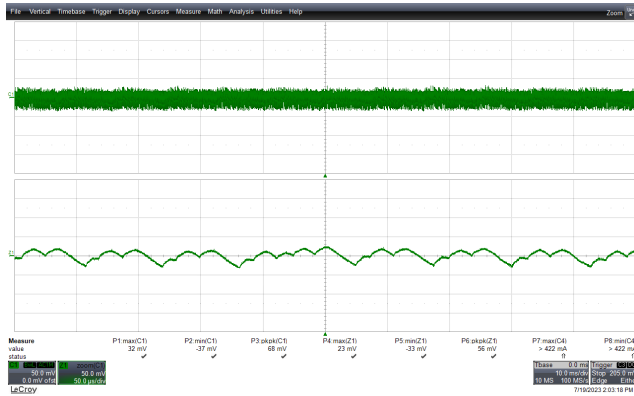


**Figure 168** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 80 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

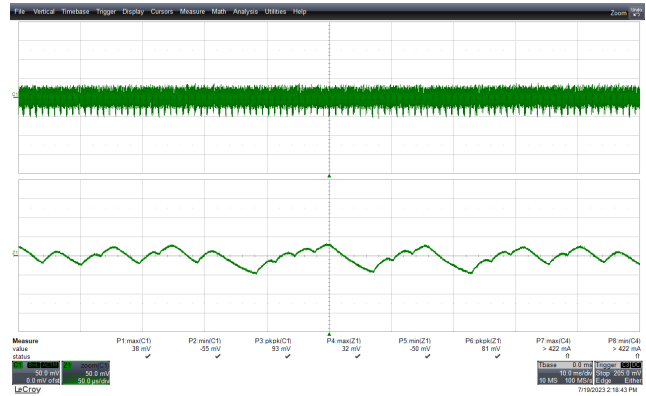


**Figure 169** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 103 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.5.5 100% Load



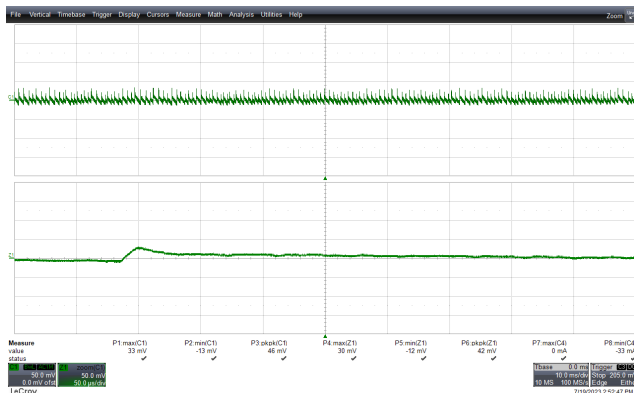
**Figure 170** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 12 V<sub>PK-PK</sub>: 68 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.



**Figure 171** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 12 V<sub>PK-PK</sub>: 93 mV.  
 Upper: 12 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.6 6 V Output Ripple Voltage Waveforms (uVCC = 3.3 V / 0 A)

12.5.6.1 0% Load

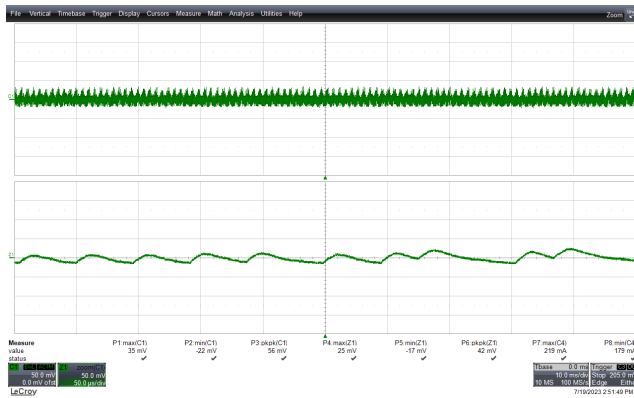


**Figure 172** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 46 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

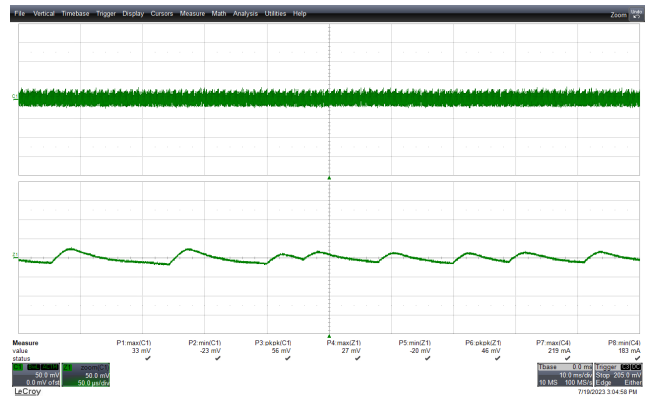


**Figure 173** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 55 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.6.2 25% Load

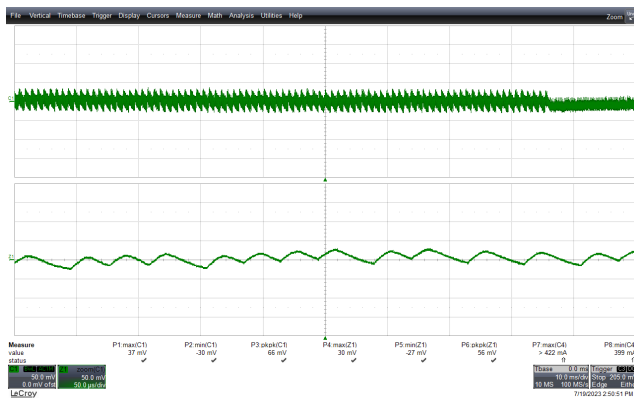


**Figure 174** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 56 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

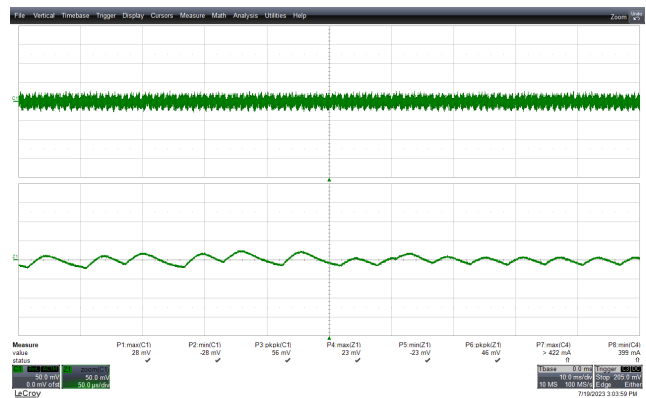


**Figure 175** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 56 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.6.3 50% Load



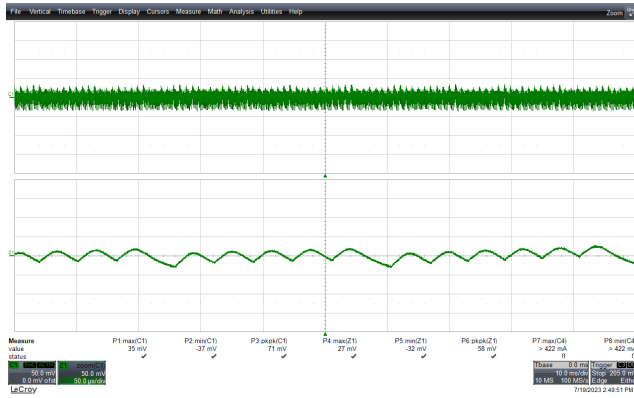
**Figure 176** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 66 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.



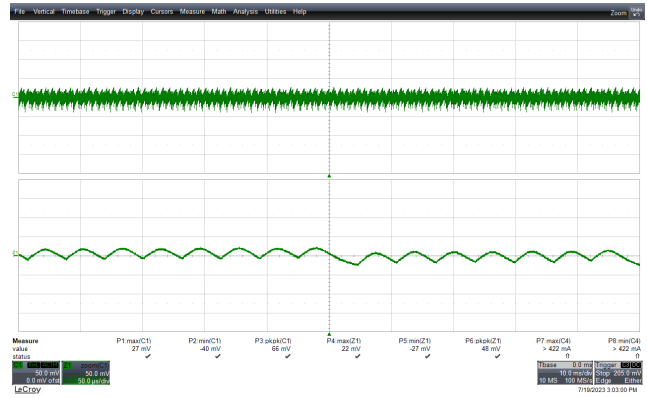
**Figure 177** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 56 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.



12.5.6.4 75% Load

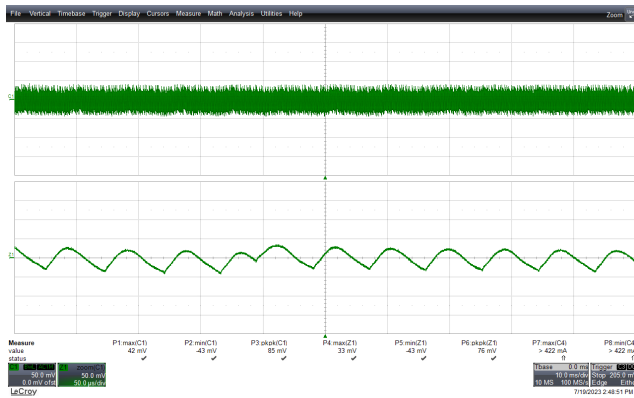


**Figure 178** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 71 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

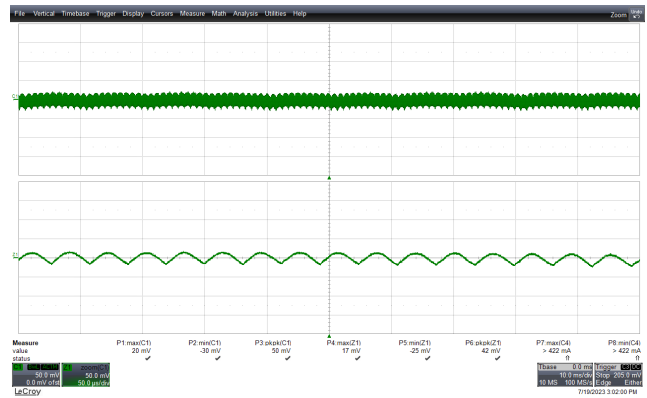


**Figure 179** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 66 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

12.5.6.5 100% Load



**Figure 180** – Output Ripple Voltage Waveforms.  
 90 VAC Input.  
 6 V<sub>PK-PK</sub>: 85 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

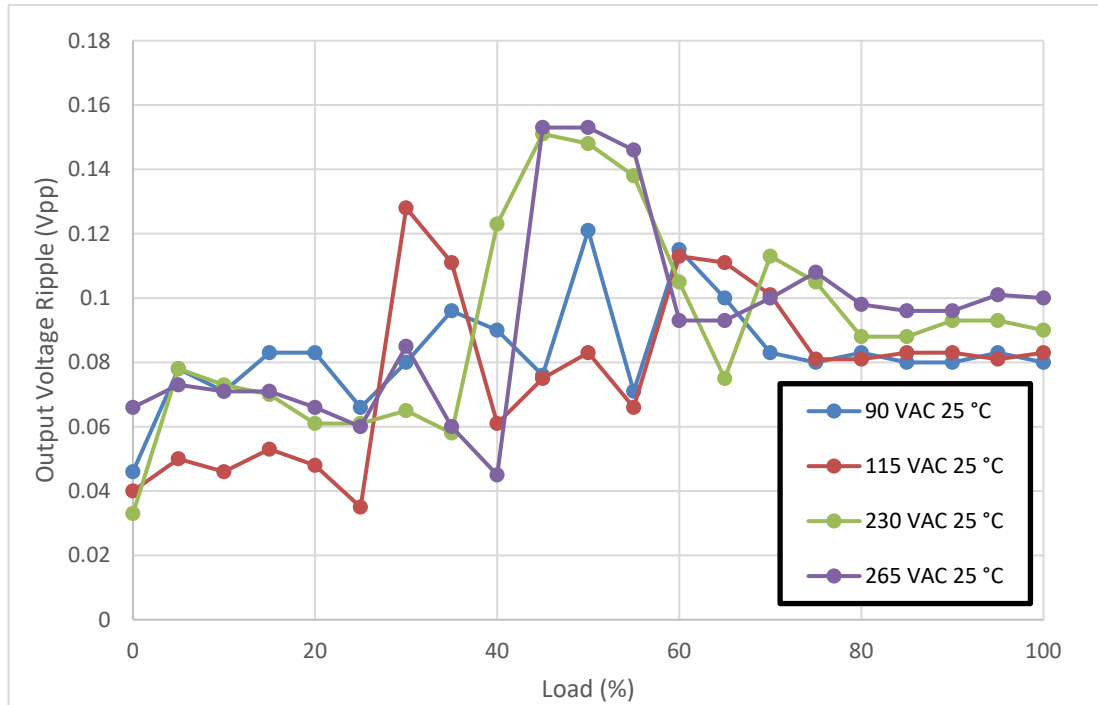


**Figure 181** – Output Ripple Voltage Waveforms.  
 265 VAC Input.  
 6 V<sub>PK-PK</sub>: 50 mV.  
 Upper: 6 V<sub>OUT</sub>, 50 mV / div, 10 ms / div.  
 Zoom: 50 μs / div.

### 12.5.8 Ripple (ATE Measurements)

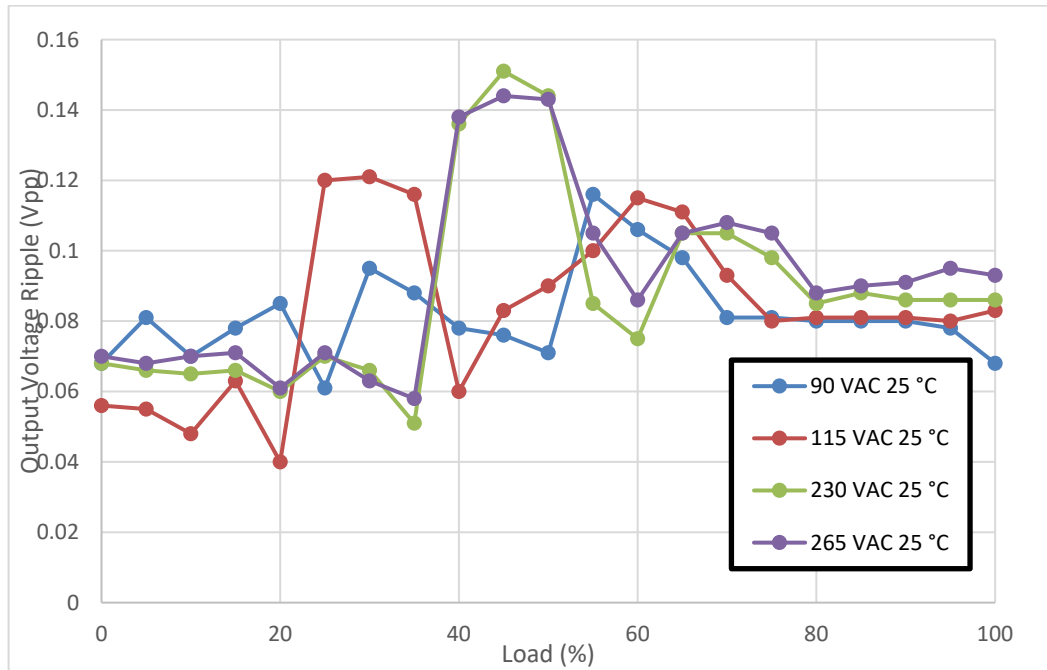
**Note:** Both 5 V and 12 V output are loaded with the same percentage.

#### 12.5.8.1 12 V Output Ripple ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )



**Figure 182** – 12 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 °C Temperature.

12.5.8.2 12 V Output Ripple ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )



**Figure 183** – 12 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 °C Temperature.

12.5.8.3 6 V Output Ripple ( $\mu\text{VCC} = 3.3 \text{ V} / 0 \text{ A}$ )

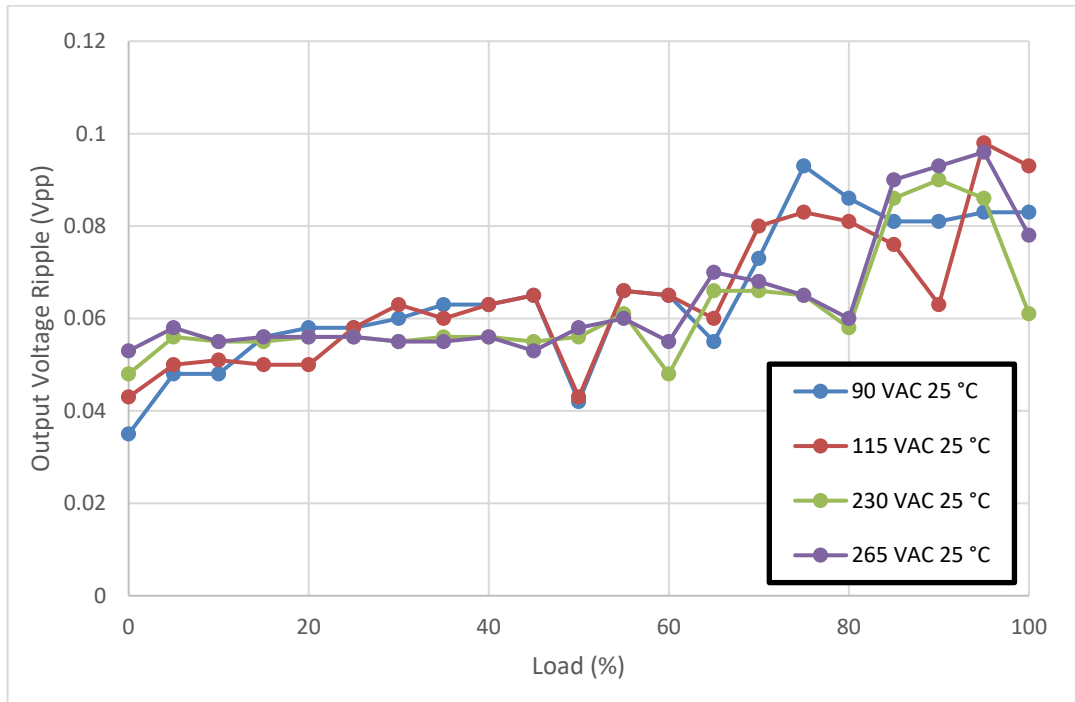
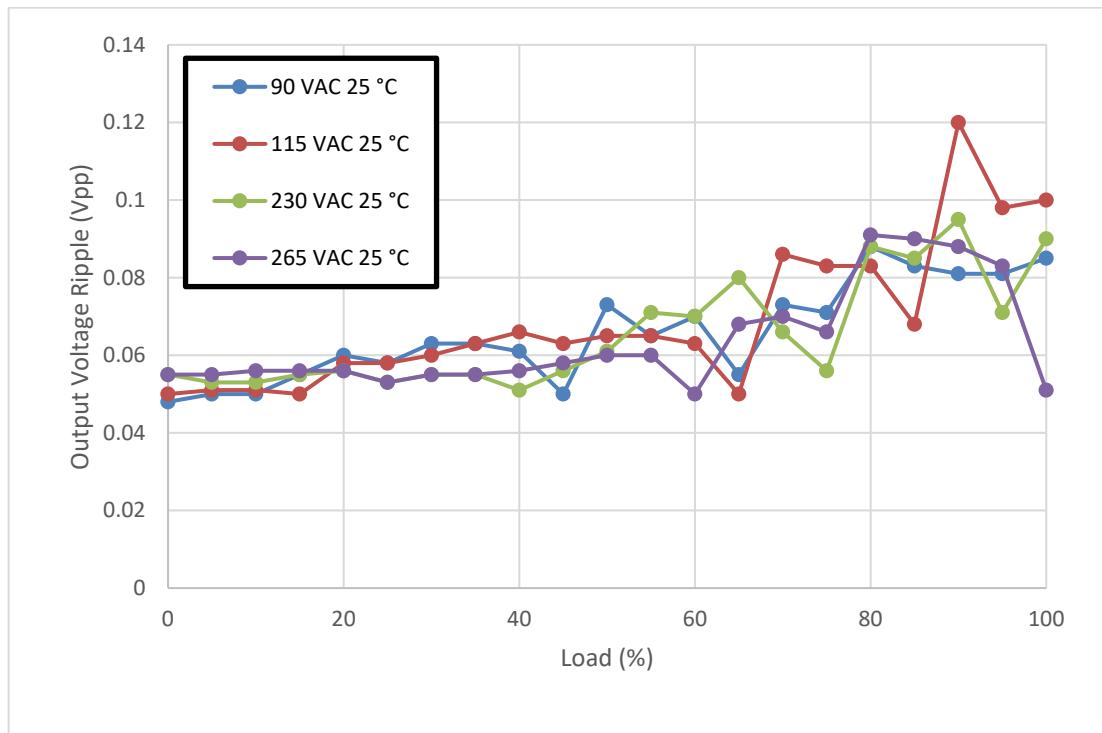


Figure 184 – 6 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 °C Temperature.

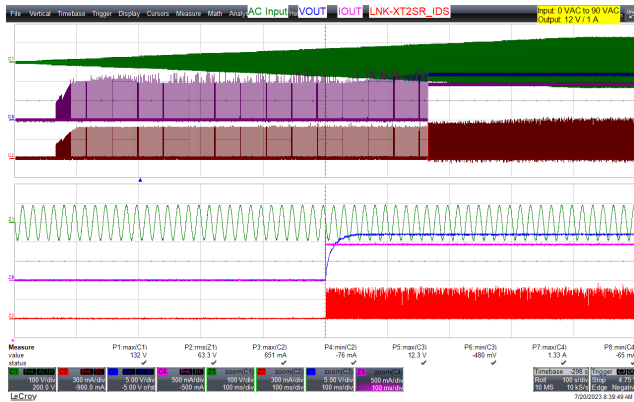
12.5.8.4 6 V Output Ripple ( $\mu\text{VCC} = 3.3 \text{ V} / 20 \text{ mA}$ )

**Figure 185** – 6 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 °C Temperature

## 12.6 Brown-In / Brown-Out Recovery Test

No abnormal overheating or voltage overshoot / undershoot was observed. The unit works normally after the brown-out test.

### 12.6.1 12 V / 1 A Output, $uVCC = 3.3\text{ V} / 0\text{ A}$



**Figure 186** – Brown-In Waveforms.

0 to 90 VAC Input, Full Load.

Upper: AC Input, 100 V / div.

Upper Middle: 12 V<sub>OUT</sub>, 5 V / div.

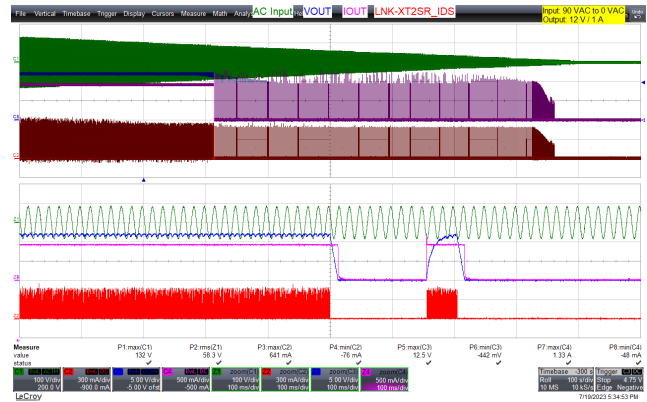
Lower Middle: 12 I<sub>OUT</sub>, 500 mA / div.

Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.

100 s / div.

Zoom: 100 ms / div.

Brown-In Voltage = 63.3 VAC



**Figure 187** – Brown-Out Waveforms.

90 to 0 VAC Input, Full Load.

Upper: AC Input, 100 V / div.

Upper Middle: 12 V<sub>OUT</sub>, 5 V / div.

Lower Middle: 12 I<sub>OUT</sub>, 500 mA / div.

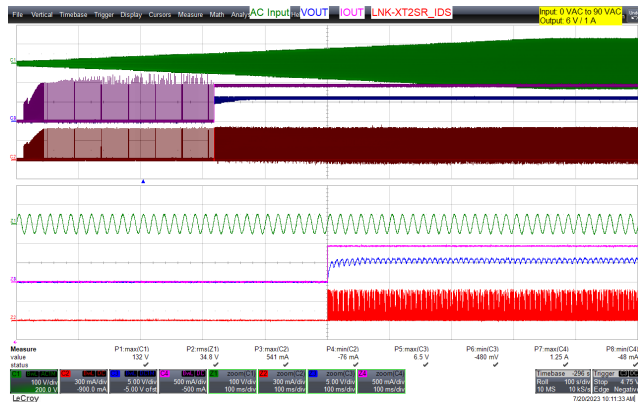
Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.

100 s / div.

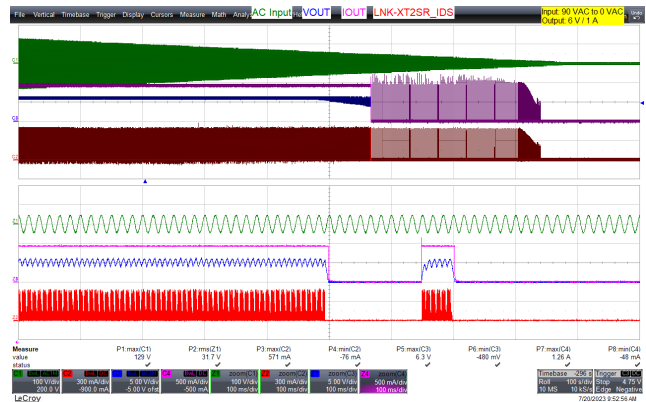
Zoom: 100 ms / div.

Brown-Out Voltage = 58.3 VAC

12.6.2 6 V / 1 A Output,  $uVCC = 3.3 V / 0 A$



**Figure 188** – Brown-In Waveforms.  
 0 to 90 VAC Input, Full Load.  
 Upper: AC Input, 100 V / div.  
 Upper Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower Middle: 6 I<sub>OUT</sub>, 500 mA / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 100 s / div.  
 Zoom: 100 ms / div.  
 Brown-In Voltage = 34.8 VAC

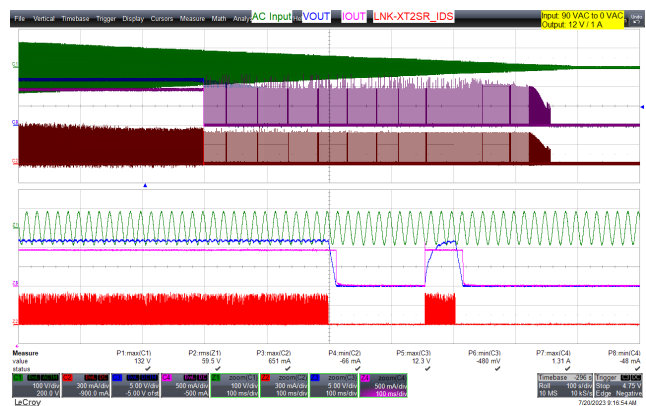


**Figure 189** – Brown-Out Waveforms.  
 90 to 0 VAC Input, Full Load.  
 Upper: AC Input, 100 V / div.  
 Upper Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower Middle: 6 I<sub>OUT</sub>, 500 mA / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 100 s / div.  
 Zoom: 100 ms / div.  
 Brown-Out Voltage = 31.7 VAC

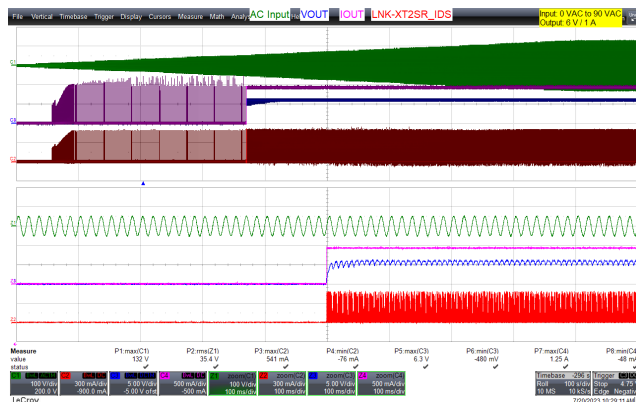
12.6.3 12 V / 1 A Output,  $uVCC = 3.3 V / 20 mA$



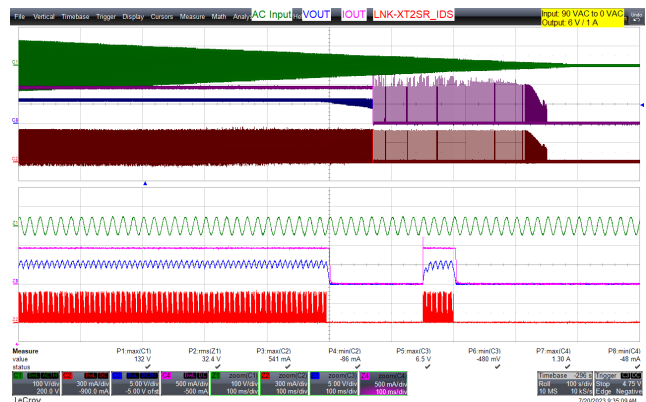
**Figure 190** – Brown-In Waveforms.  
 0 to 90 VAC Input, Full Load.  
 Upper: AC Input, 100 V / div.  
 Upper Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower Middle: 12 I<sub>OUT</sub>, 500 mA / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 100 s / div.  
 Zoom: 100 ms / div.  
 Brown-In Voltage = 65.8 VAC



**Figure 191** – Brown-Out Waveforms.  
 90 to 0 VAC Input, Full Load.  
 Upper: AC Input, 100 V / div.  
 Upper Middle: 12 V<sub>OUT</sub>, 5 V / div.  
 Lower Middle: 12 I<sub>OUT</sub>, 500 mA / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 100 s / div.  
 Zoom: 100 ms / div.  
 Brown-Out Voltage = 59.5 VAC

12.6.4 6 V / 1 A Output,  $uVCC = 3.3\text{ V} / 20\text{ mA}$ 

**Figure 192** – Brown-In Waveforms.  
 0 to 90 VAC Input, Full Load.  
 Upper: AC Input, 100 V / div.  
 Upper Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower Middle: 6 I<sub>OUT</sub>, 500 mA / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 100 s / div.  
 Zoom: 100 ms / div.  
 Brown-In Voltage = 35.4 VAC



**Figure 193** – Brown-Out Waveforms.  
 90 to 0 VAC Input, Full Load.  
 Upper: AC Input, 100 V / div.  
 Upper Middle: 6 V<sub>OUT</sub>, 5 V / div.  
 Lower Middle: 6 I<sub>OUT</sub>, 500 mA / div.  
 Lower: LNK-XT2SR\_I<sub>DS</sub>, 300 mA / div.  
 100 s / div.  
 Zoom: 100 ms / div.  
 Brown-Out Voltage = 32.4 VAC



## 13 EMI

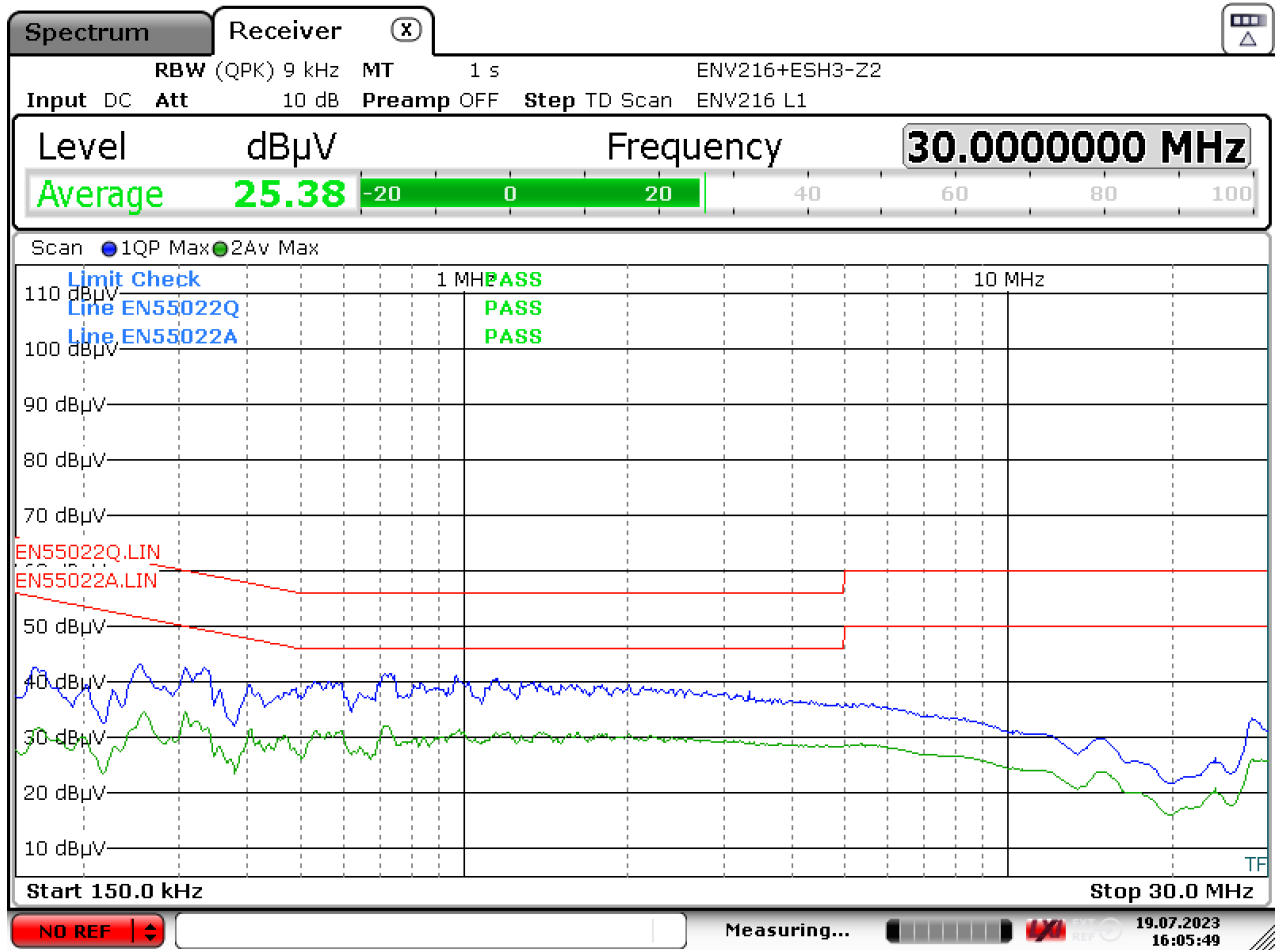
### 13.1 Conductive EMI



**Figure 194** - EMI Test Set-up.

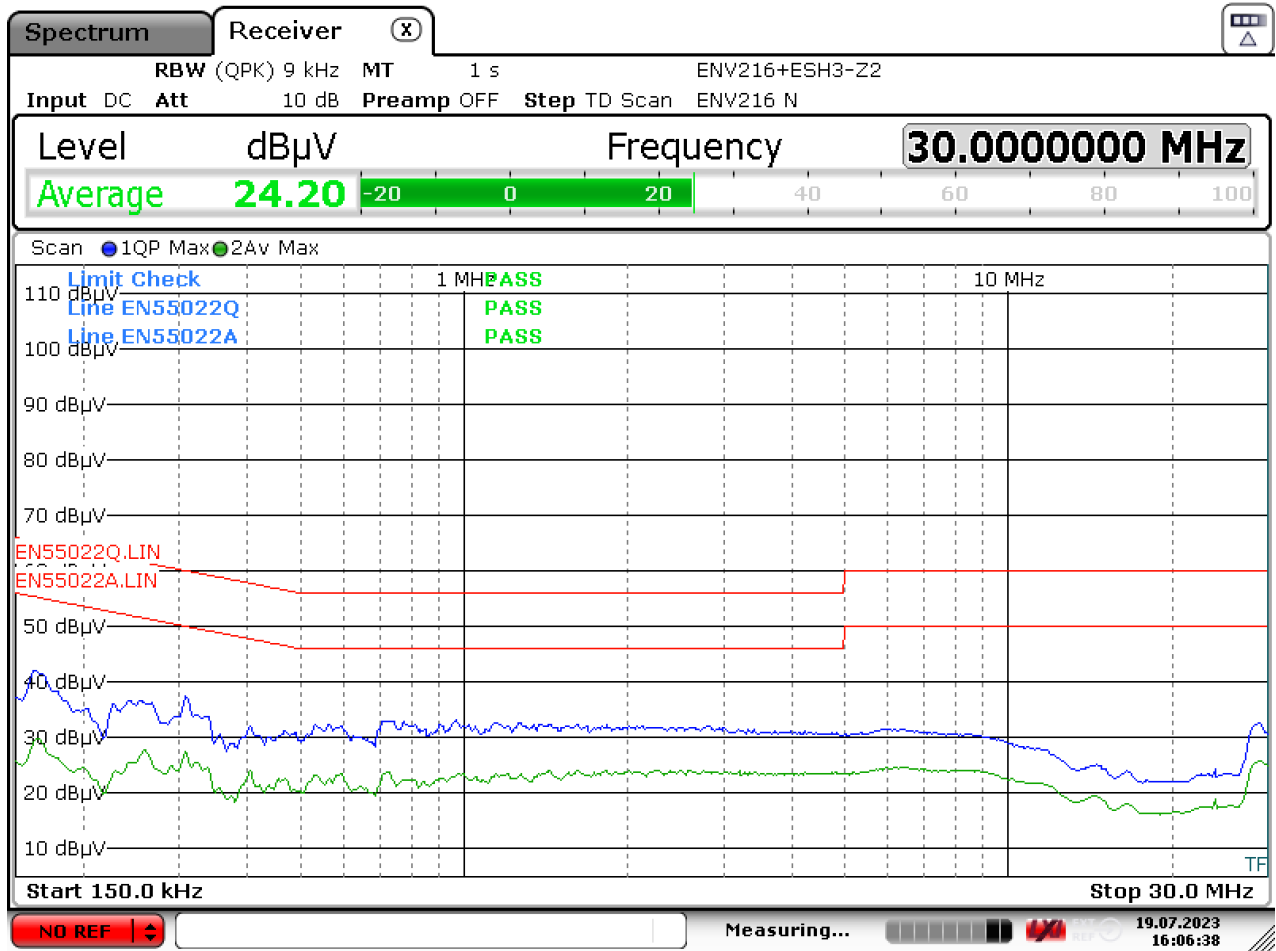
13.1.1 12 V Output - Floating Output (QP / AV)

13.1.1.1 115 VAC Input (uVCC = 3.3 V / 0 A)



Date: 19.JUL.2023 16:05:49

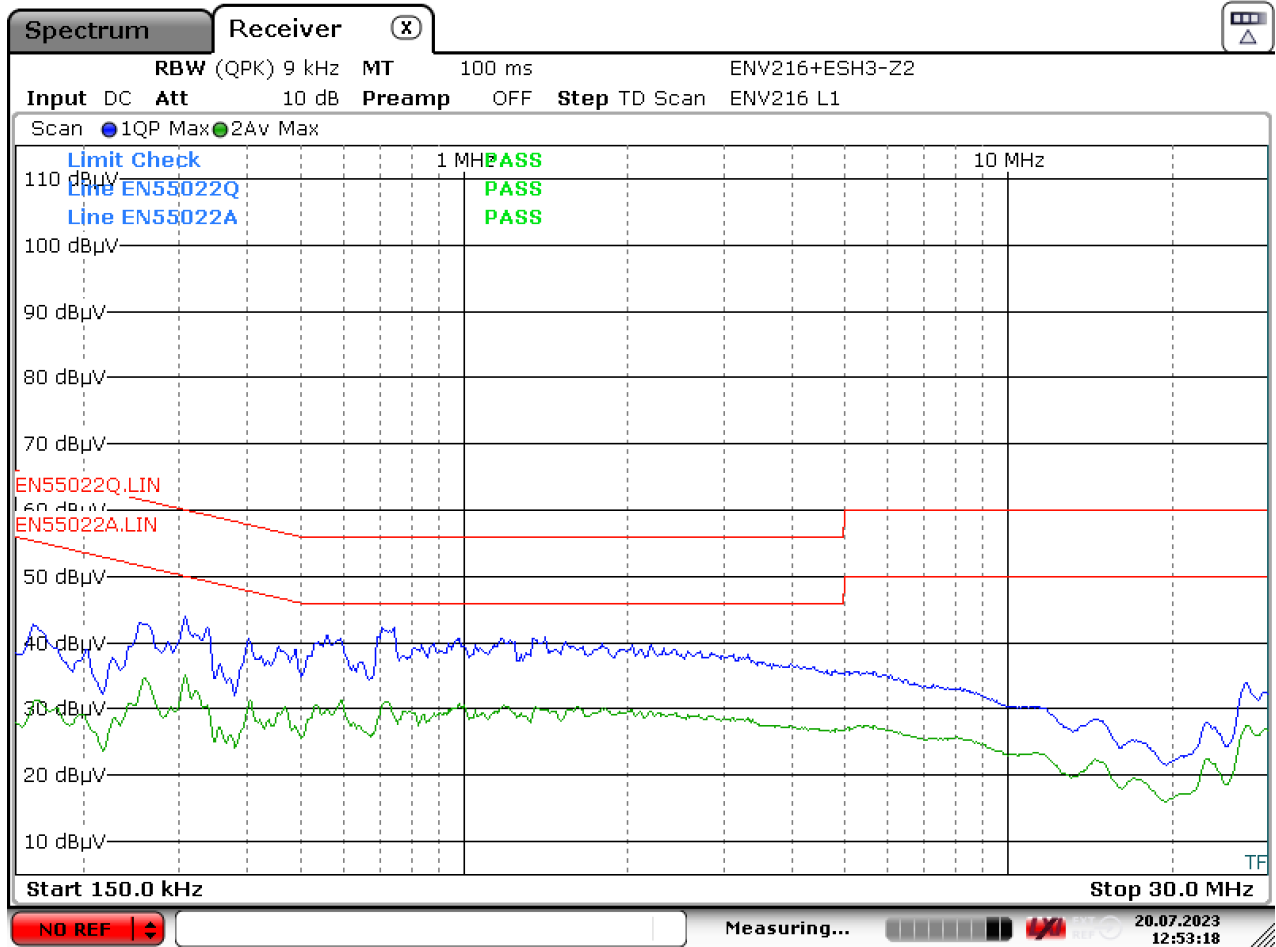
**Figure 195** – Floating Output - 115 VAC Line.



Date: 19.JUL.2023 16:06:39

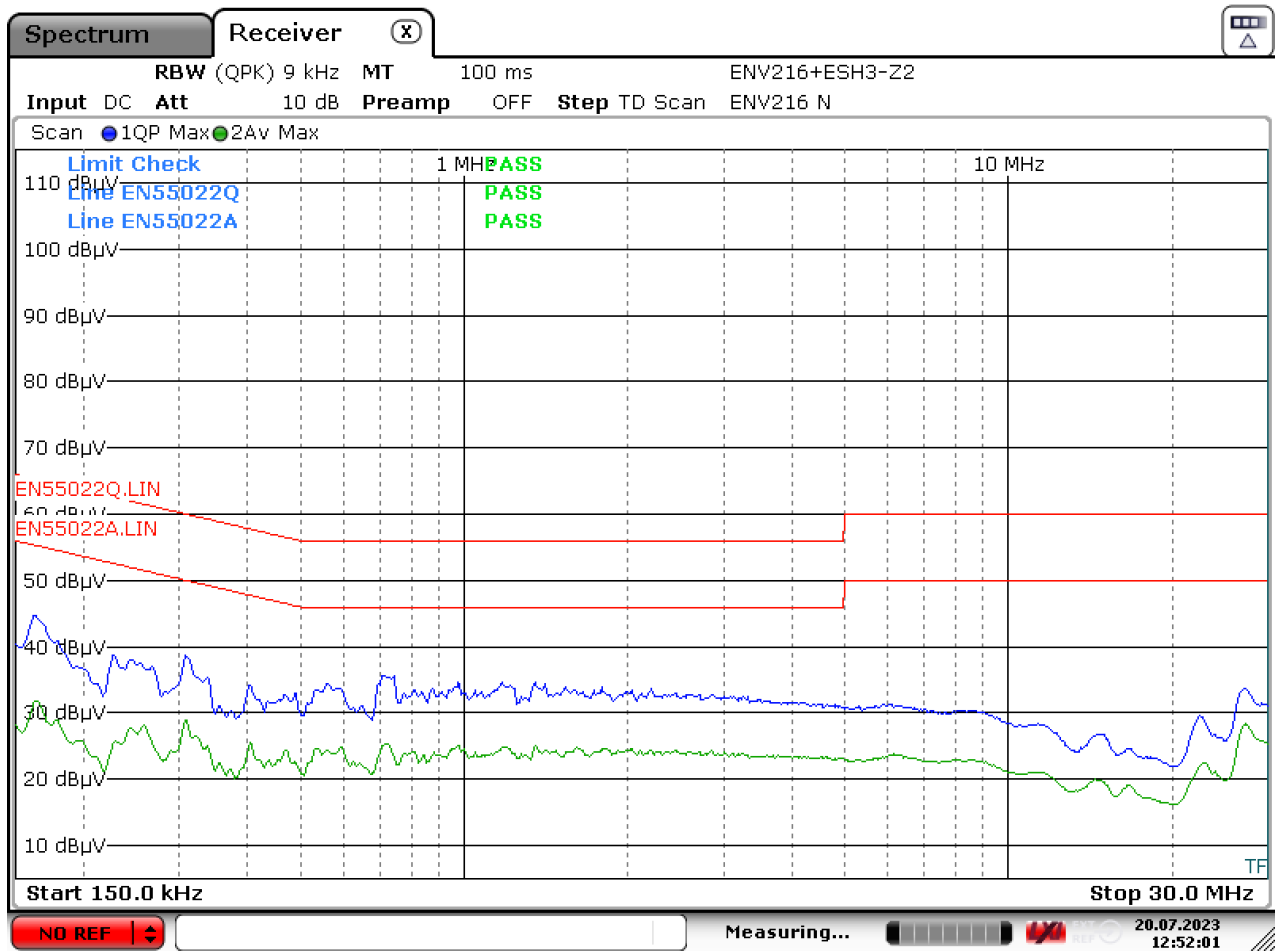
**Figure 196 – Floating Output - 115 VAC Neutral.**

13.1.1.2 115 VAC Input (uVCC = 3.3 V / 20 mA)



Date: 20.JUL.2023 12:53:18

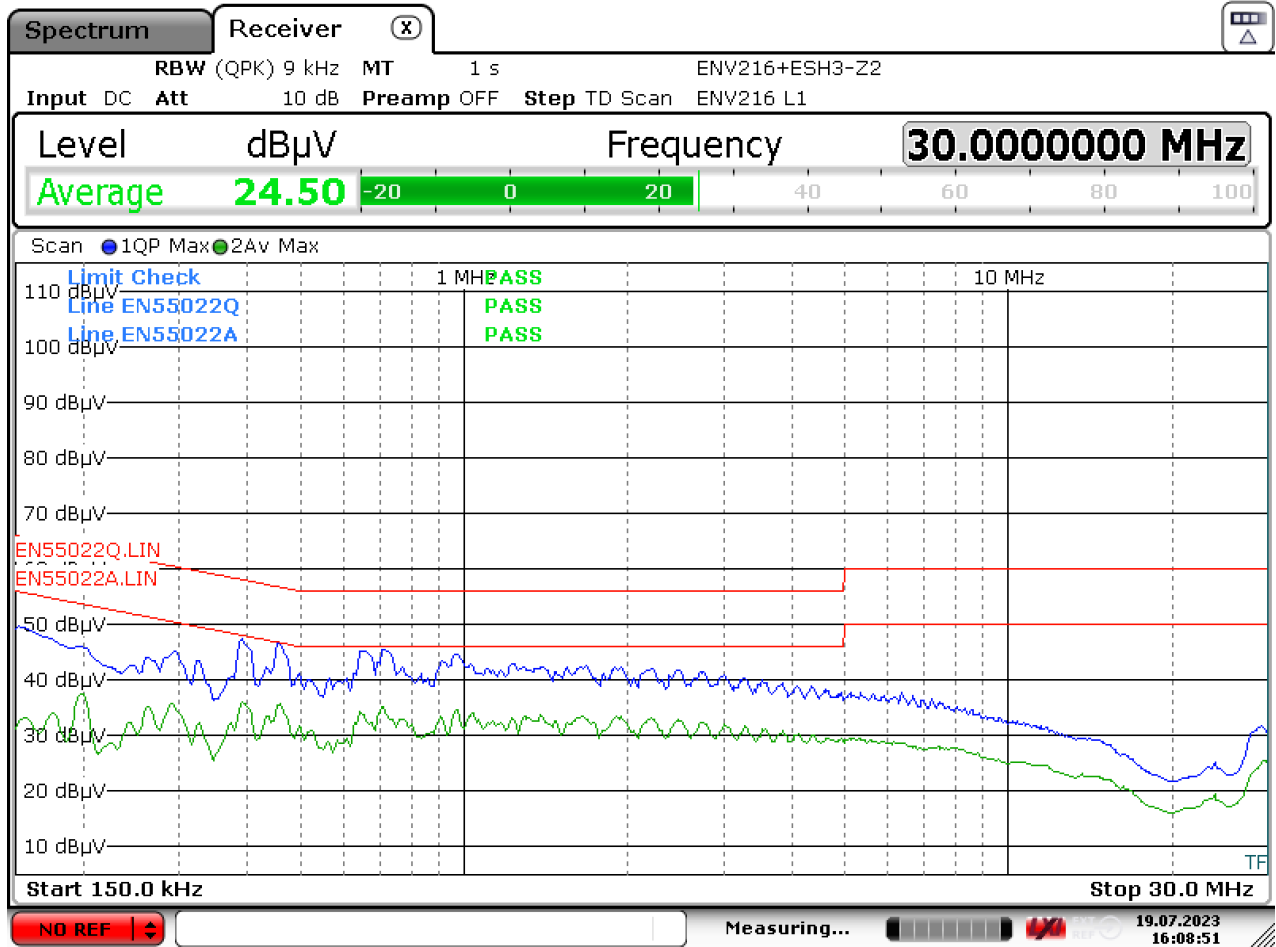
Figure 197 – Floating Output - 115 VAC Line.



Date: 20.JUL.2023 12:52:01

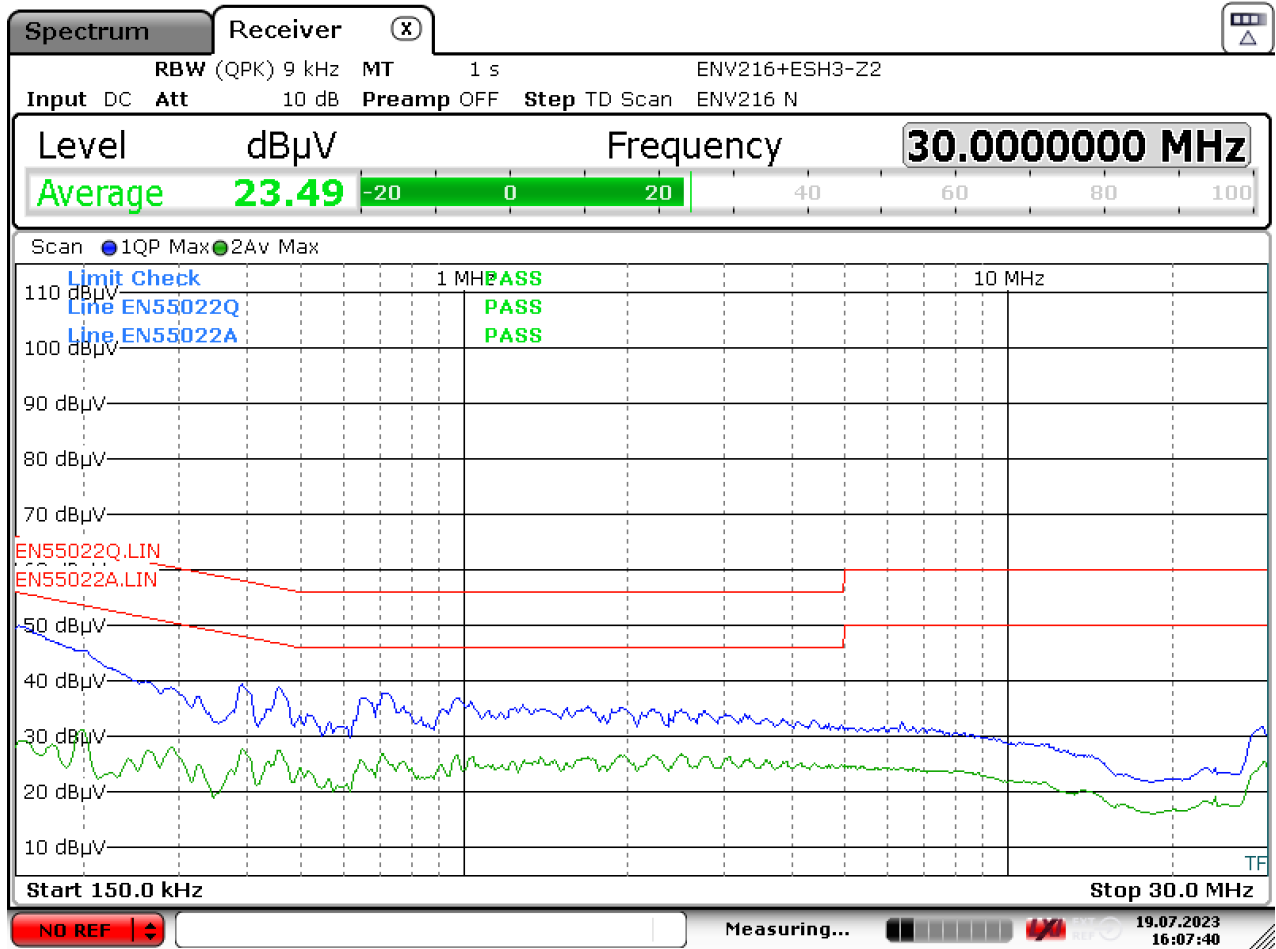
**Figure 198 – Floating Output - 115 VAC Neutral.**

13.1.1.3 230 VAC Input (uVCC = 3.3 V / 0 A)



Date: 19.JUL.2023 16:08:51

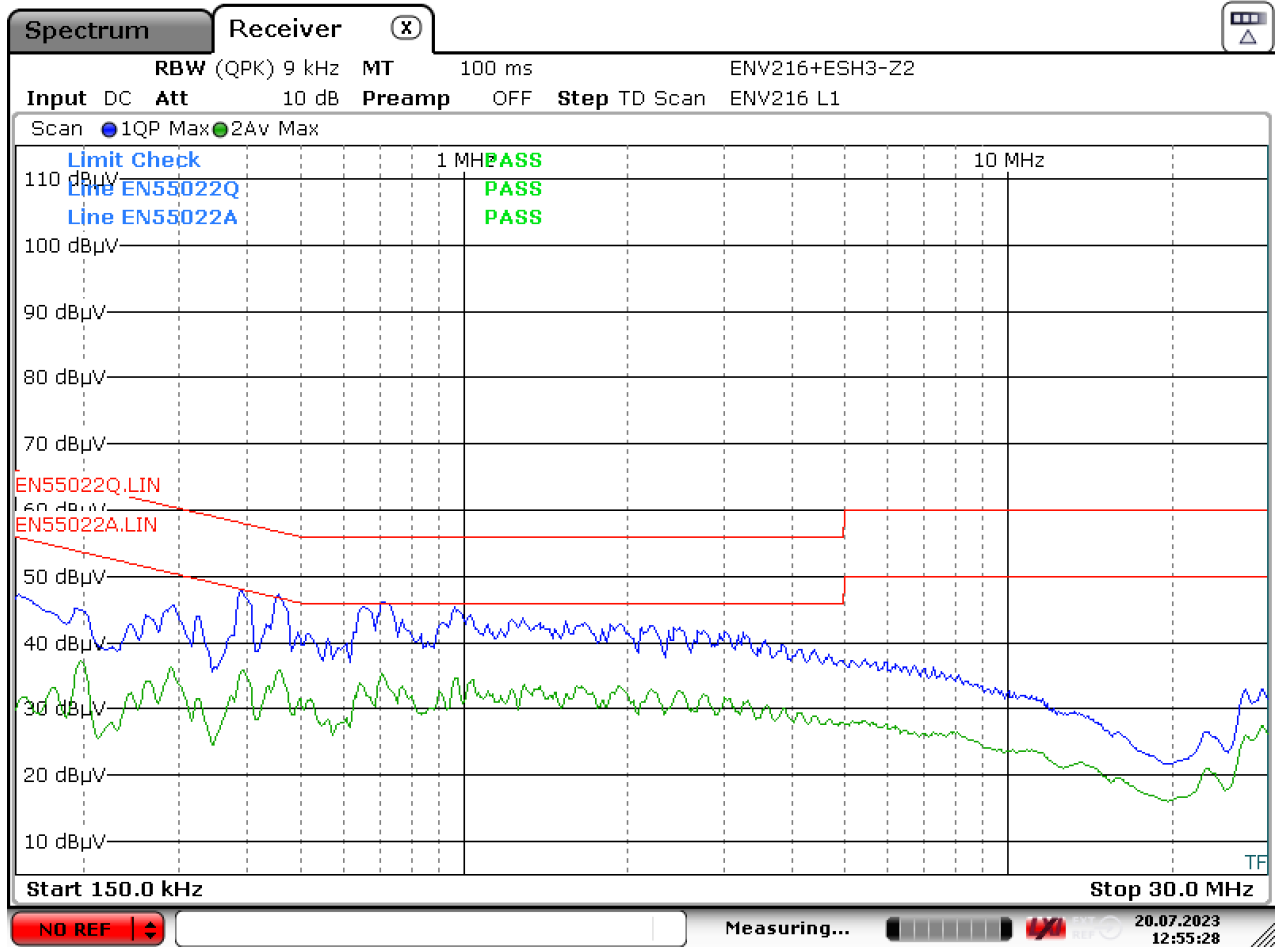
Figure 199 – Floating Output - 230 VAC Line.



Date: 19.JUL.2023 16:07:41

**Figure 200** – Floating Output - 230 VAC Neutral.

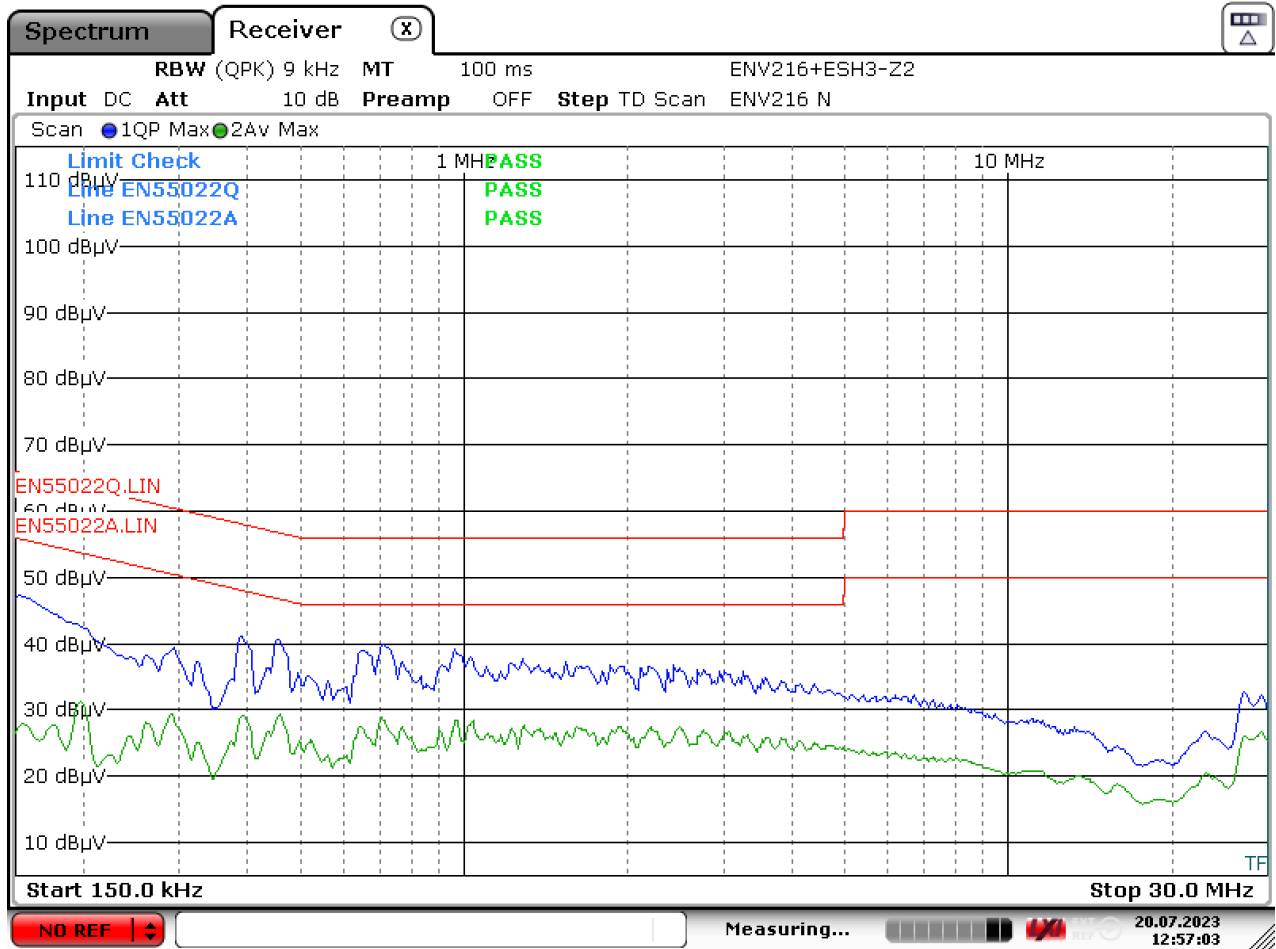
13.1.1.4 230 VAC Input (uVCC = 3.3 V / 20 mA)



Date: 20.JUL.2023 12:55:29

Figure 201 – Floating Output - 230 VAC Line.



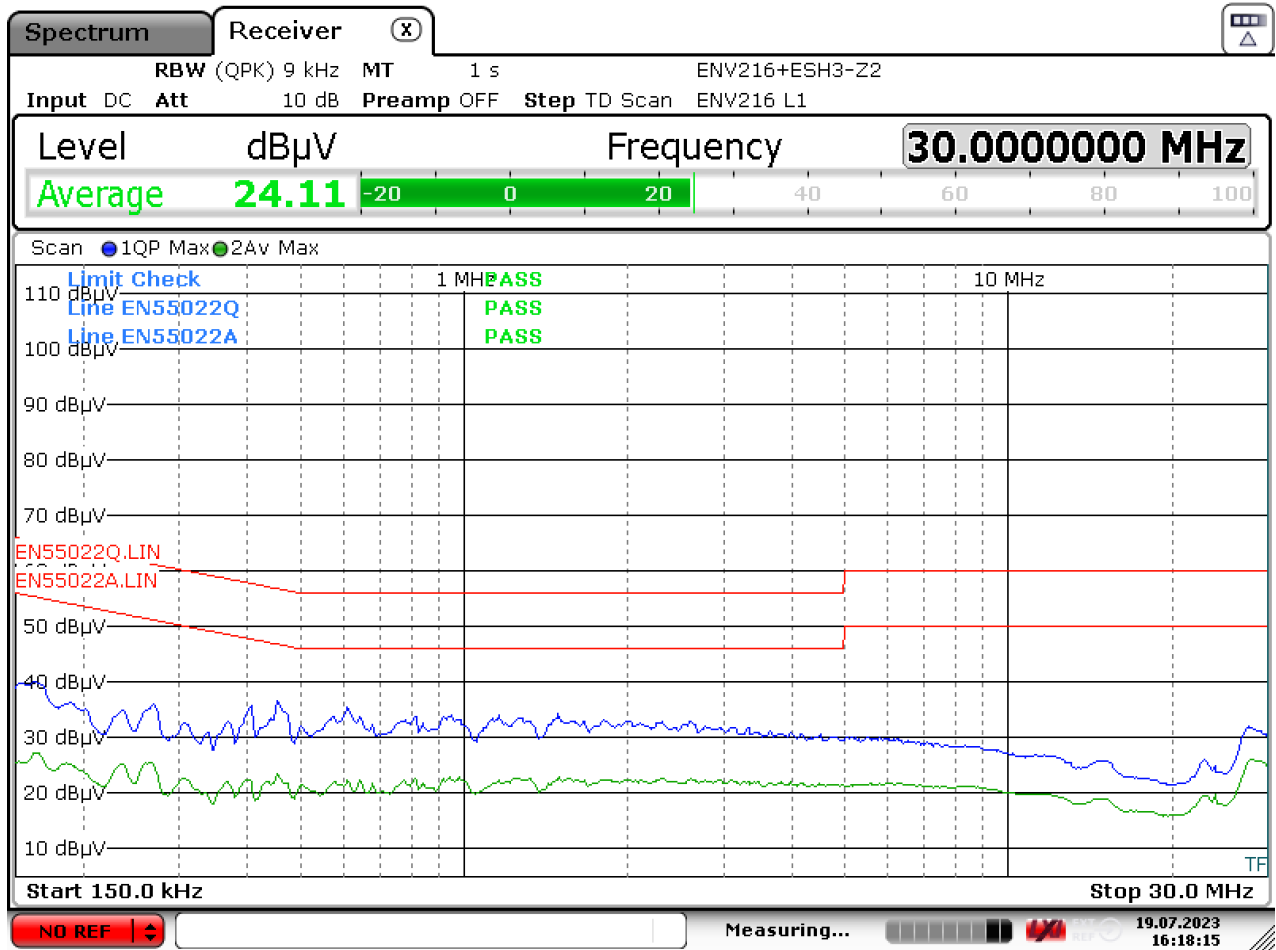


Date: 20.JUL.2023 12:57:03

Figure 202 – Floating Output - 230 VAC Neutral.

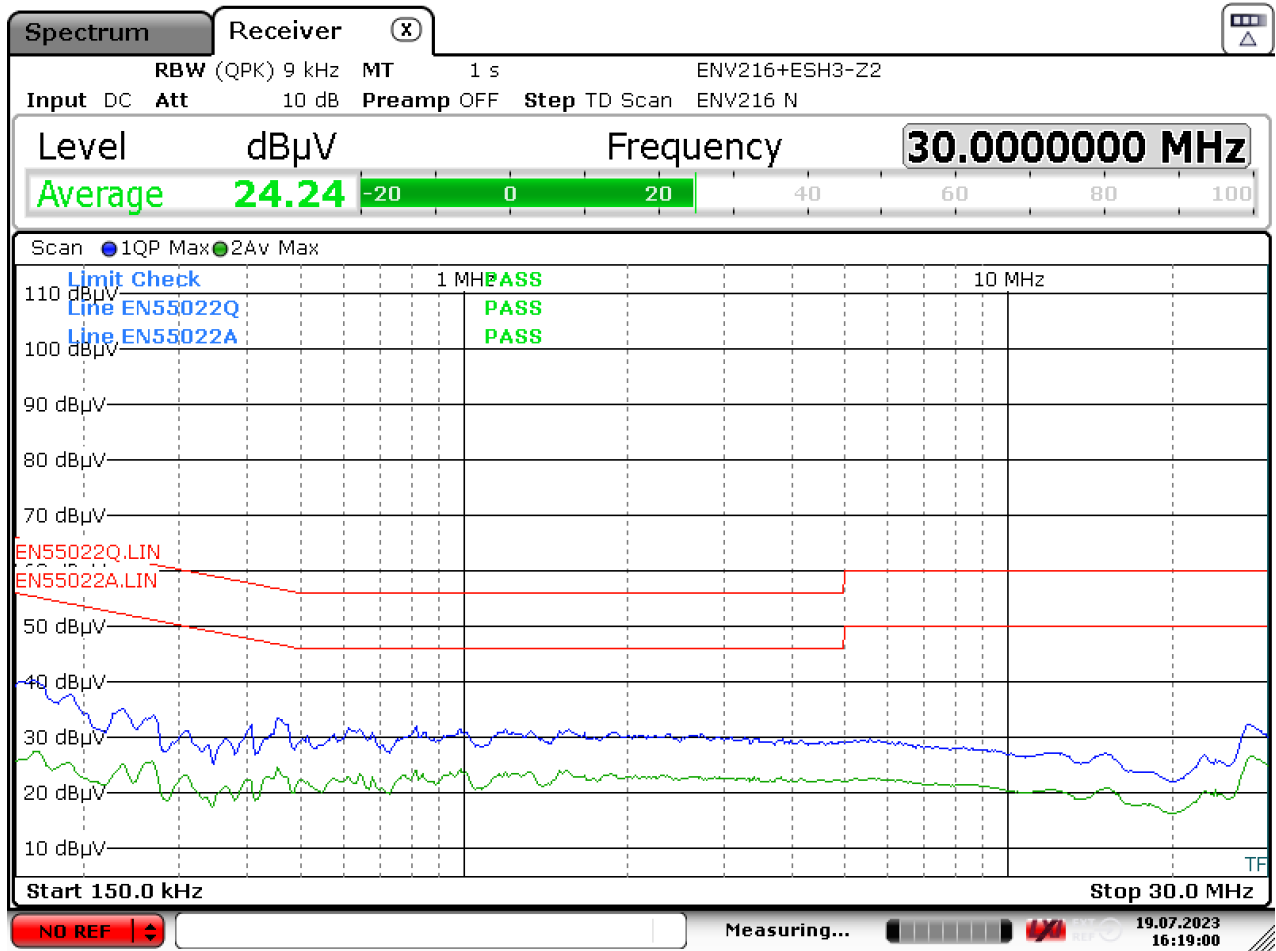
13.1.2 6 V Output - Floating Output (QP / AV)

13.1.2.1 115 VAC Input (uVCC = 3.3 V / 0 A)



Date: 19.JUL.2023 16:18:15

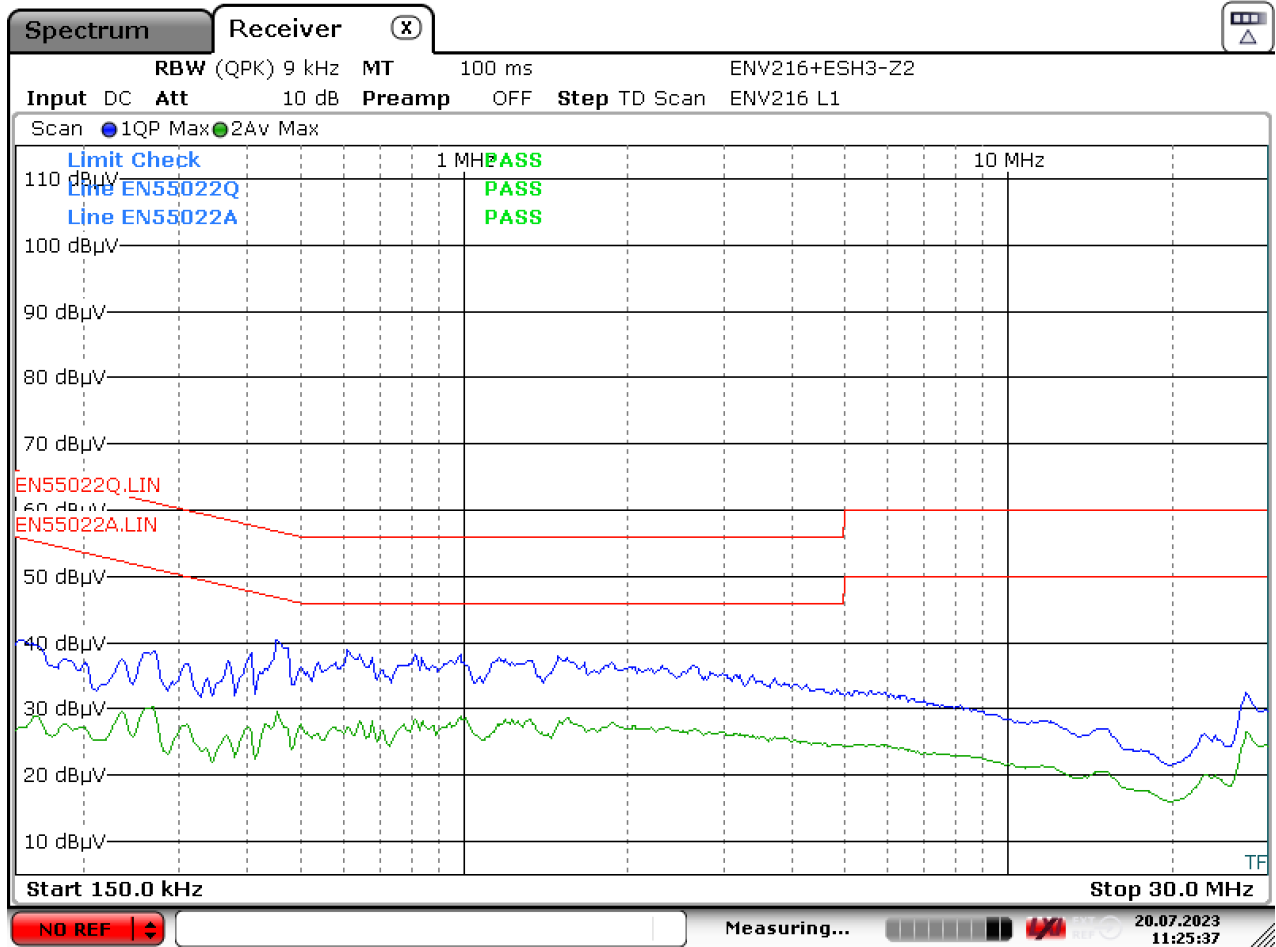
Figure 203 – Floating Output - 115 VAC Line.



Date: 19.JUL.2023 16:19:00

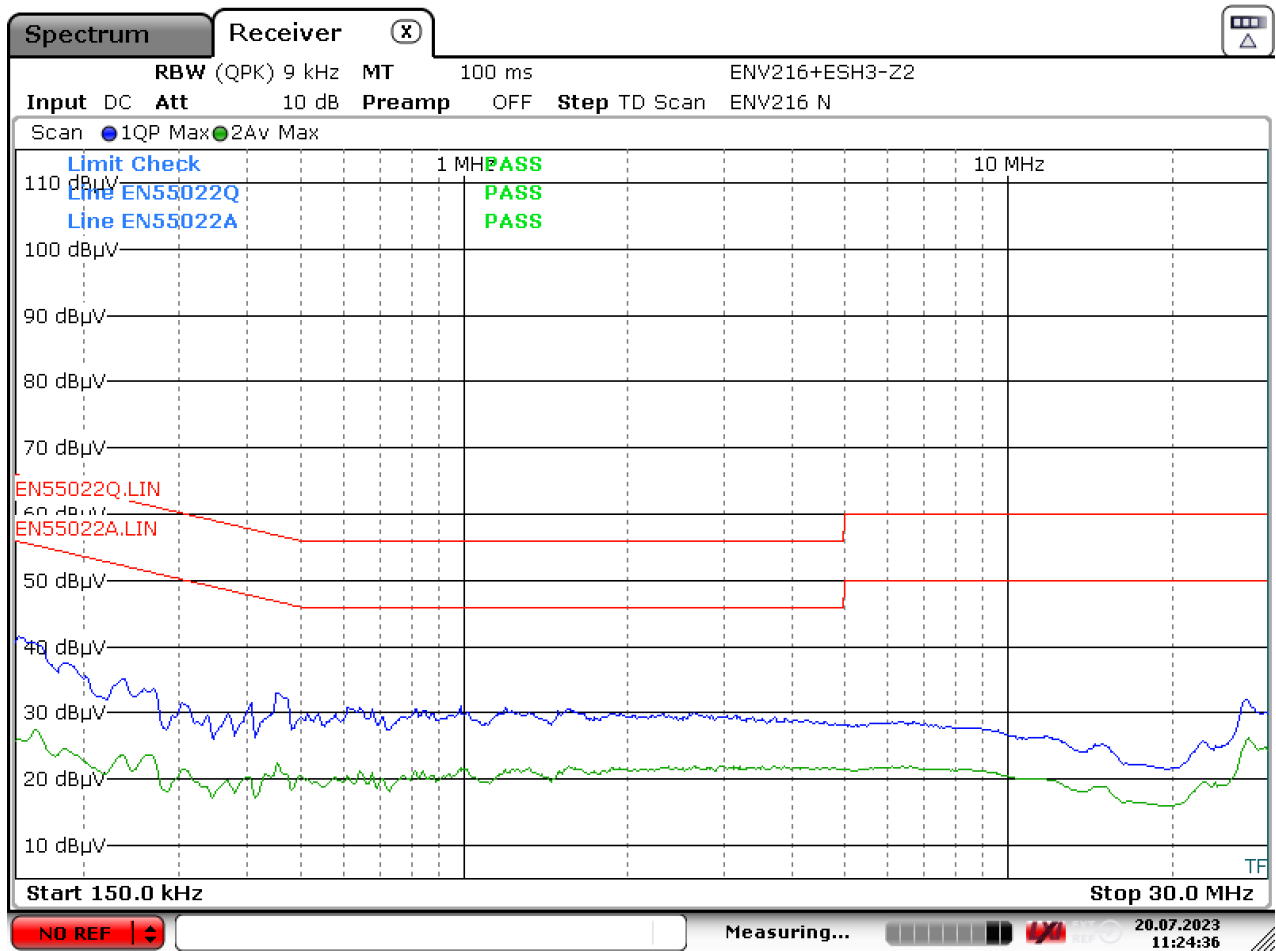
**Figure 204 – Floating Output - 115 VAC Neutral.**

13.1.2.2 115 VAC Input (uVCC = 3.3 V / 20 mA)



Date: 20.JUL.2023 11:25:38

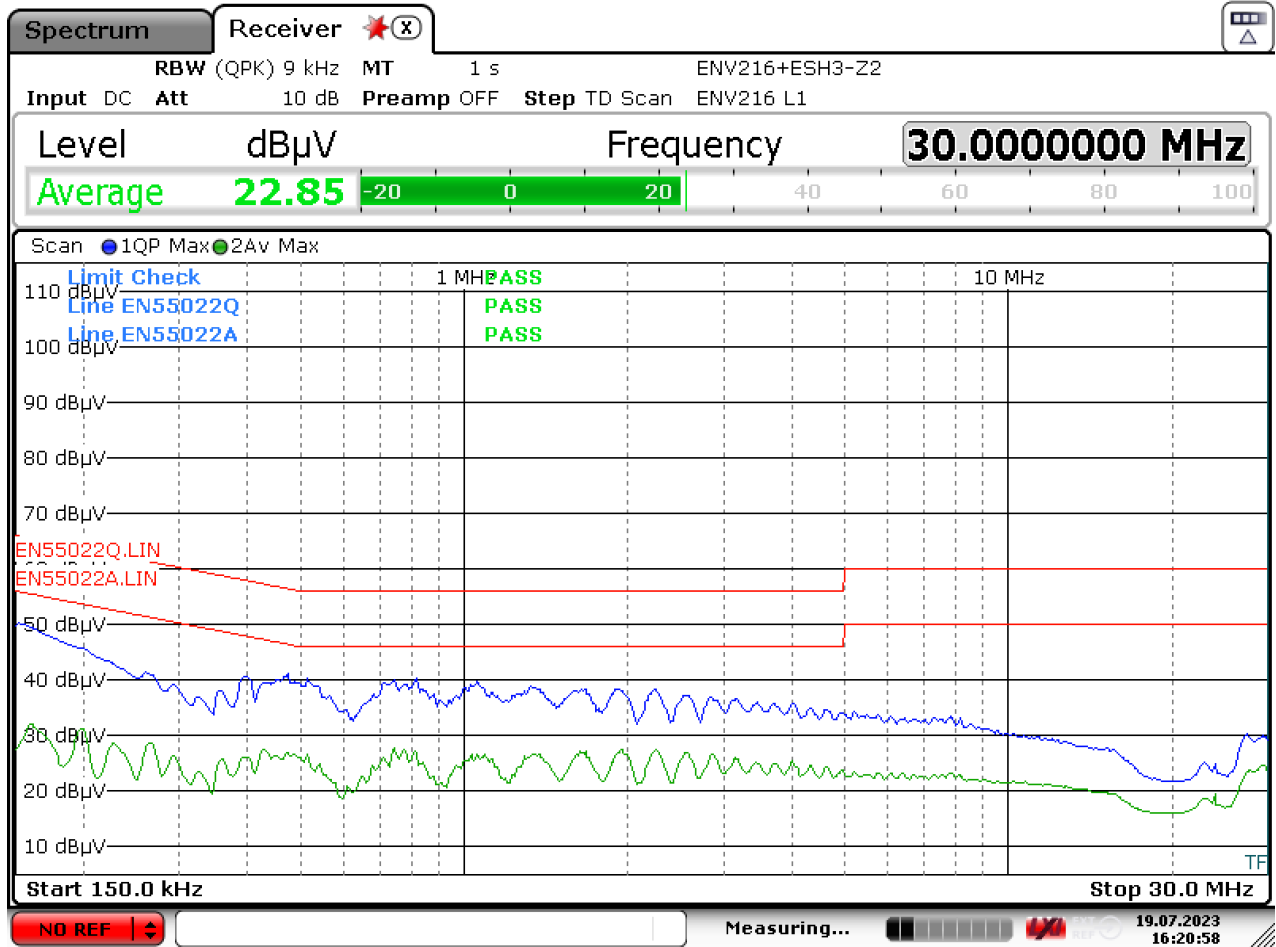
Figure 205 – Floating Output - 115 VAC Line.



Date: 20.JUL.2023 11:24:37

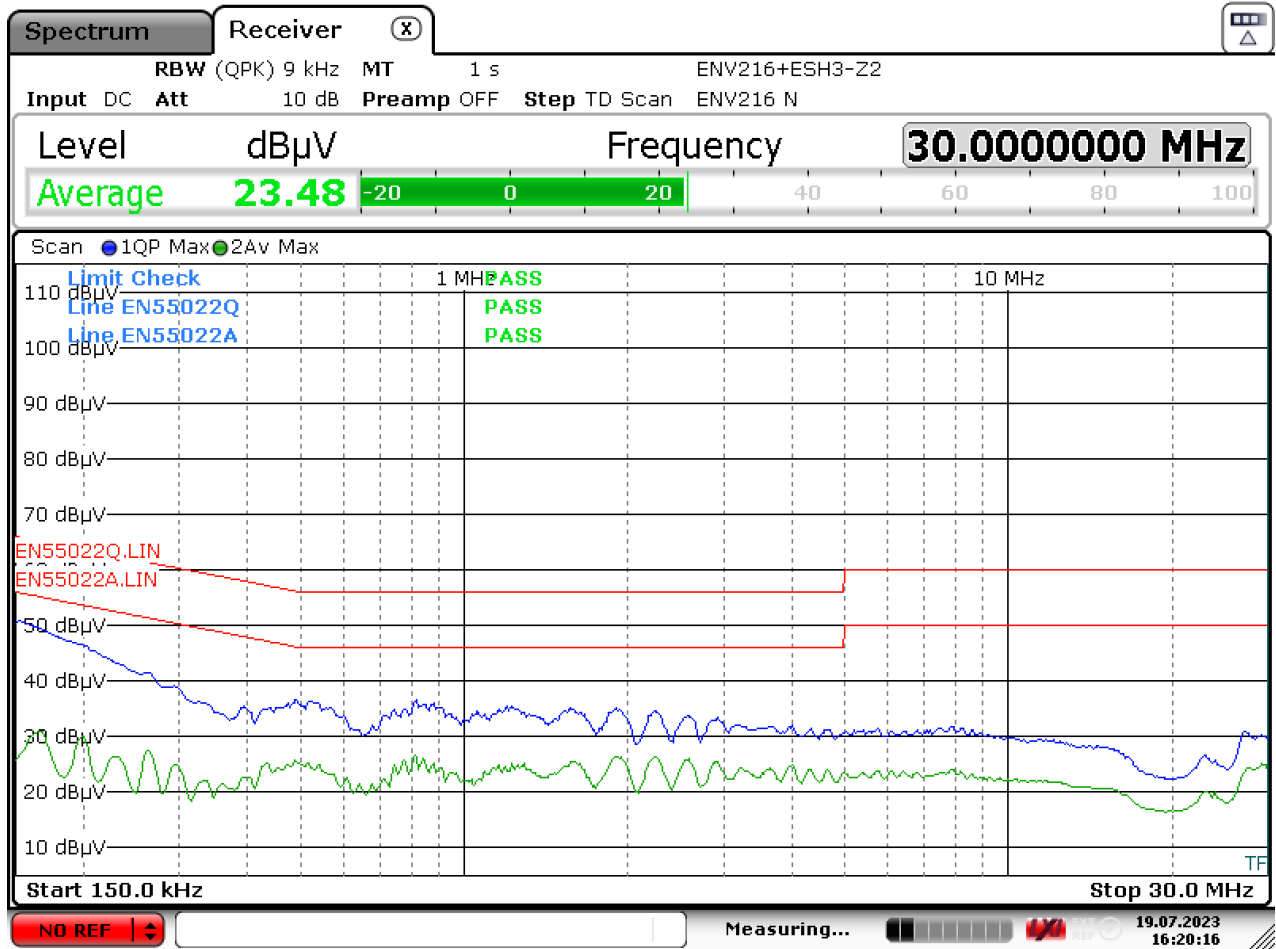
**Figure 206 – Floating Output - 115 VAC Neutral.**

13.1.2.3 230 VAC Input (uVCC = 3.3 V / 0 A)



Date: 19.JUL.2023 16:20:59

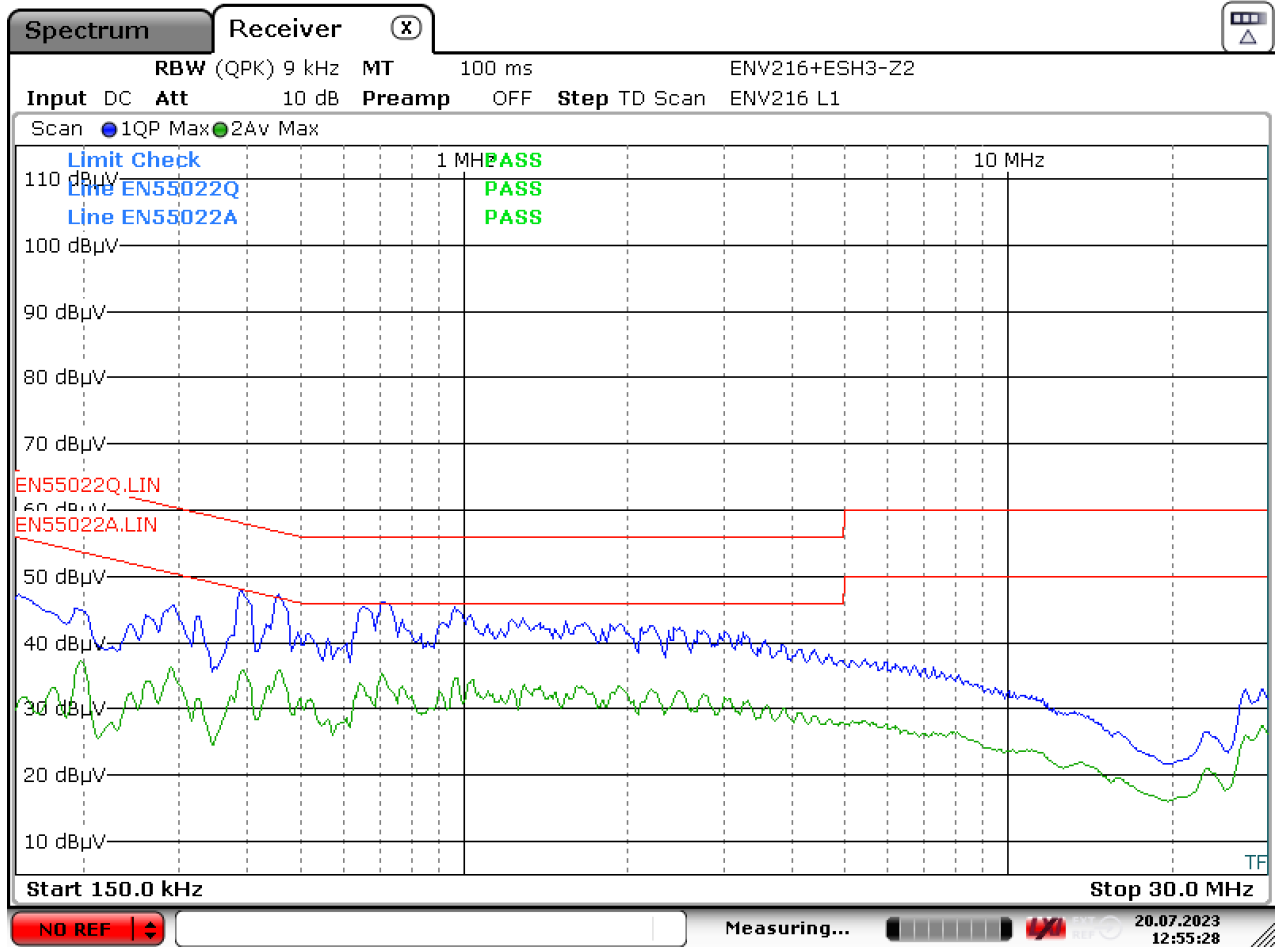
Figure 207 – Floating Output - 230 VAC Line.



Date: 19.JUL.2023 16:20:16

**Figure 208** – Floating Output - 230 VAC Neutral.

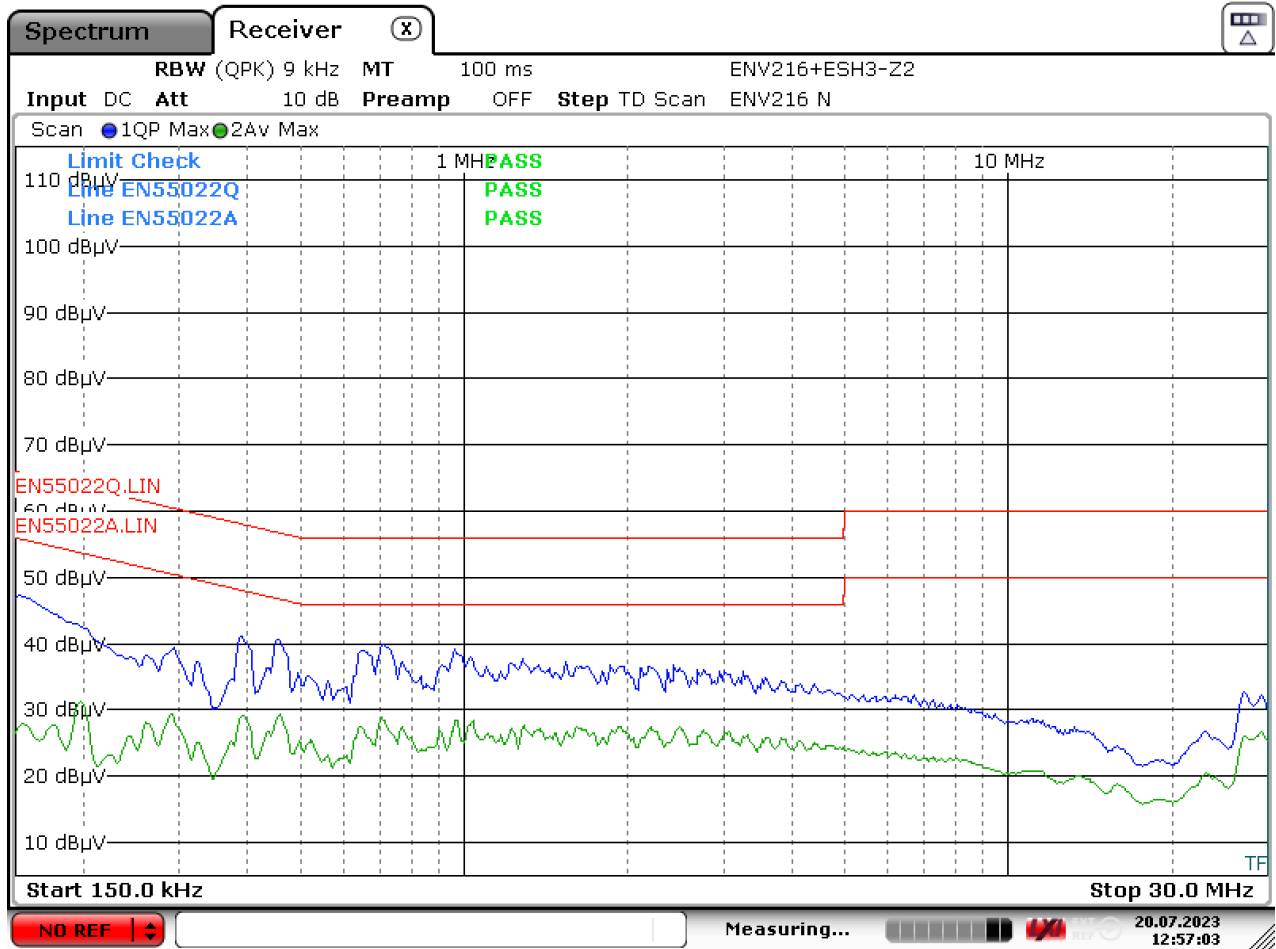
13.1.2.4 230 VAC Input (uVCC = 3.3 V / 20 mA)



Date: 20.JUL.2023 12:55:29

Figure 209 – Floating Output - 230 VAC Line.





Date: 20.JUL.2023 12:57:03

**Figure 210** – Floating Output - 230 VAC Neutral.

## 14 Line Immunity

Output Load set at maximum load (12 V / 1 A).

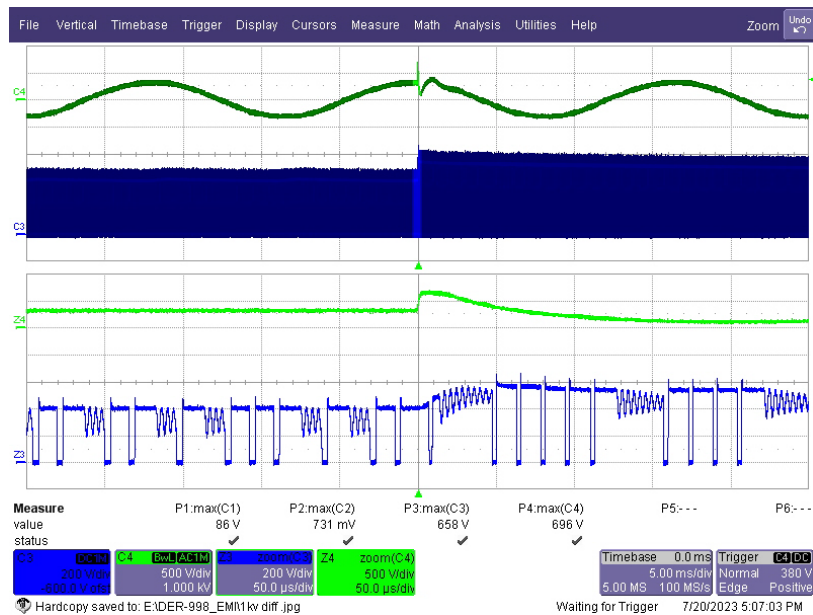
- using 12 Ω fixed resistor for 12 V output.

### 14.1 Differential Surge Test Results

Repetition rate: 1 strike / 30 seconds

Passed ±1 kV, 500 A surge test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
1	0	L, N	2	10	PASS
-1	0	L, N	2	10	PASS
1	90	L, N	2	10	PASS
-1	90	L, N	2	10	PASS
1	180	L, N	2	10	PASS
-1	180	L, N	2	10	PASS
1	270	L, N	2	10	PASS
-1	270	L, N	2	10	PASS



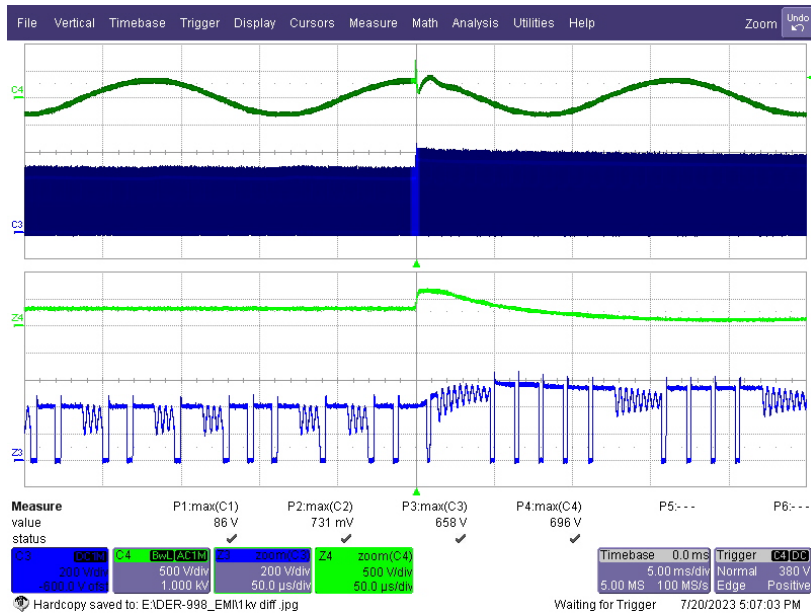
**Figure 211** – 230 VAC, +1 kV, Differential Surge L-N  
 Injection Phase: 90°.  
 Upper: AC Input, 500 V / div.  
 Lower: VDRAIN, 200 V / div. Max VDS = 658 V.  
 5 ms / div.  
 Zoom: 50 μs / div.

**14.2 Ring Wave Surge Test Results**

Repetition rate: 1 strike / 30 seconds

Passed  $\pm 6$  kV, ring wave test.

Ring Wave Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance ( $\Omega$ )	Number of Strikes	Test Result
2	0	L, N	12	10	PASS
-2	0	L, N	12	10	PASS
2	90	L, N	12	10	PASS
-2	90	L, N	12	10	PASS
2	180	L, N	12	10	PASS
-2	180	L, N	12	10	PASS
2	270	L, N	12	10	PASS
-2	270	L, N	12	10	PASS
4	0	L, N	12	10	PASS
-4	0	L, N	12	10	PASS
4	90	L, N	12	10	PASS
-4	90	L, N	12	10	PASS
4	180	L, N	12	10	PASS
-4	180	L, N	12	10	PASS
4	270	L, N	12	10	PASS
-4	270	L, N	12	10	PASS
6	0	L, N	12	10	PASS
-6	0	L, N	12	10	PASS
6	90	L, N	12	10	PASS
-6	90	L, N	12	10	PASS
6	180	L, N	12	10	PASS
-6	180	L, N	12	10	PASS
6	270	L, N	12	10	PASS
-6	270	L, N	12	10	PASS



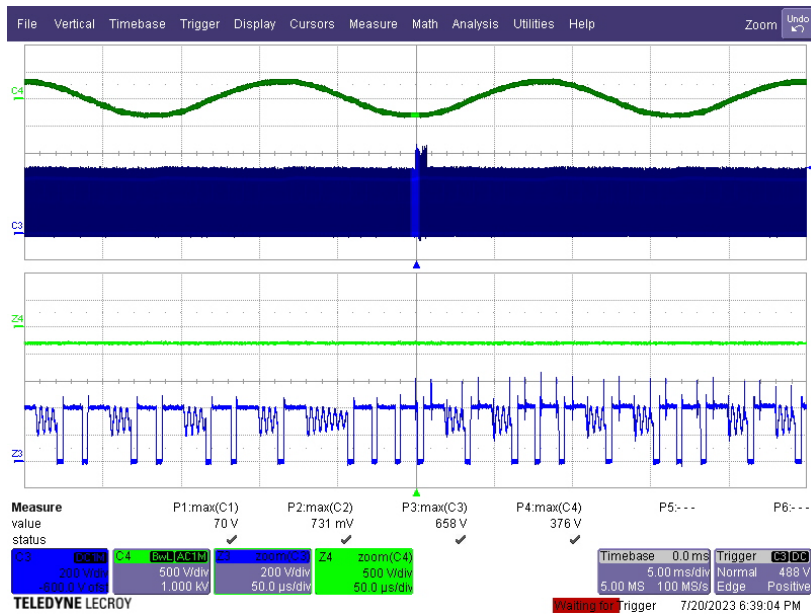
**Figure 212** – 230 VAC, +6 kV, Ring Wave L-N  
 Injection Phase: 90°.  
 Upper: AC Input, 500 V / div.  
 Lower:  $V_{DRAIN}$ , 200 V / div. Max  $V_{DS}$  = 658 V.  
 5 ms / div.  
 Zoom: 50  $\mu$ s / div.

### 14.3 EFT

Tested at 5 kHz and 100 kHz EFT burst frequency with test duration of 120 s. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

Passed  $\pm 2$  kV, EFT test.

EFT Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Frequency	T-Burst	T-Rep	Test Result
2	0	L, N	5 kHz	15 ms	300 ms	PASS
-2	0	L, N	5 kHz	15 ms	300 ms	PASS
2	90	L, N	5 kHz	15 ms	300 ms	PASS
-2	90	L, N	5 kHz	15 ms	300 ms	PASS
2	180	L, N	5 kHz	15 ms	300 ms	PASS
-2	180	L, N	5 kHz	15 ms	300 ms	PASS
2	270	L, N	5 kHz	15 ms	300 ms	PASS
-2	270	L, N	5 kHz	15 ms	300 ms	PASS
2	0	L, N	100 kHz	750 us	300 ms	PASS
-2	0	L, N	100 kHz	750 us	300 ms	PASS
2	90	L, N	100 kHz	750 us	300 ms	PASS
-2	90	L, N	100 kHz	750 us	300 ms	PASS
2	180	L, N	100 kHz	750 us	300 ms	PASS
-2	180	L, N	100 kHz	750 us	300 ms	PASS
2	270	L, N	100 kHz	750 us	300 ms	PASS
-2	270	L, N	100 kHz	750 us	300 ms	PASS



**Figure 213** – 230 VAC, +2 kV, EFT L-N  
 Injection Phase: 90°.  
 Upper: AC Input, 500 V / div.  
 Lower:  $V_{DRAIN}$ , 200 V / div. Max  $V_{DS}$  = 658 V.  
 5 ms / div.  
 Zoom: 50  $\mu$ s / div.

## 15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
12-Sep-23	MA	1.0	Initial Release.	Apps & Mktg
12-Oct-23	MA	1.1	Updated Schematic and Power Table.	Apps & Mktg



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