

# DESIGN EXAMPLE REPORT

Title	7 W (10 W peak) 3 Output Supply Using LNK626PG
Specification	85 – 265 VAC Input; 5 V / 1.7 A, 12 V / 0.1 A, and -22 V / 15 mA Outputs
Application	DVD Player
Author	Applications Engineering Department
Document Number	DER-198
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Revision	1.0

### **Summary and Features**

- Revolutionary control concept provides very low cost, low part-count solution
  - Primary-side control eliminates secondary-side control and optocoupler
  - Provides ±5% constant voltage (CV) accuracy
  - Over-temperature protection tight tolerance (±5%) with hysteretic recovery for safe PCB temperatures under all conditions
  - Auto-restart output short circuit and open-loop protection
  - Extended pin creepage distance for reliable operation in humid environments –
     >3.2 mm at package
- EcoSmart® Easily meets all current international energy efficiency standards China (CECP) / EISA / ENERGY STAR 2 / EU CoC
  - Ultra-low leakage current: <5 µA at 265 VAC input (no Y capacitor required)</li>
  - Design easily passes EN550022 and CISPR-22 Class B EMI testing with >10 dB margin
- Meets IEC 61000-4-5 Class 3 AC line surge
- Meets IEC 61000-4-2 ESD withstand (contact and air discharge to ±15 kV)

### PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <a href="http://www.powerint.com/ip.htm">http://www.powerint.com/ip.htm</a>.

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## **Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

# 1 Introduction

This document is an engineering report describing a DVD Player power supply utilizing a LNK626. This power supply is intended as a general purpose evaluation platform for LinkSwitch-CV.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.



Figure 1 - Populated Circuit Board Photograph.

# **Power Supply Specification**

Description	Symbol	Min	Тур	Max	Units	Comment
Input Voltage Frequency No-load Input Power (230 VAC)	V <sub>IN</sub> f <sub>LINE</sub>	85 47	50/60	265 64 0.14	VAC Hz W	2 Wire – no P.E.
Output Output Voltage 1 Output Ripple Voltage 1 Output Current 1 Output Voltage 2 Output Ripple Voltage 2 Output Ripple Voltage 2 Output Current 2 Output Voltage 3 Output Ripple Voltage 3 Output Ripple Voltage 3 Output Current 3 Total Output Power Continuous Output Power Peak Output Power	VOUT1 VRIPPLE1 IOUT1 VOUT2 VRIPPLE2 IOUT2 VOUT3 VRIPPLE3 IOUT3 POUT_PEAK	4.75 0.05 10.8 0.05 -19.8	5.0 12 -22	5.25 100 1.7 13.2 750 0.1 -24.2 200 15	V mV A V mV mA W W	± 5% 20 MHz bandwidth Peak ± 10% 20 MHz bandwidth  ± 10% 20 MHz bandwidth
Efficiency Full Load	η	68.0			%	Measured at P <sub>out</sub> 25 °C
Environmental Conducted EMI Safety Surge Differential (L1-L2) Common Mode (L1/L2-PE)	•		ts CISPR2 ed to mee Cla		-	Output Floating  1.2/50 μs surge (per IEC 1000-4-5) Series Impedance: 12 Ω Common Mode 2 Ω Differential Mode
100 kHz ring wave (L1/L2-PE)  Ambient Temperature	T <sub>AMB</sub>	6		40	kV °C	Free convection, sea level

# 3 Schematic

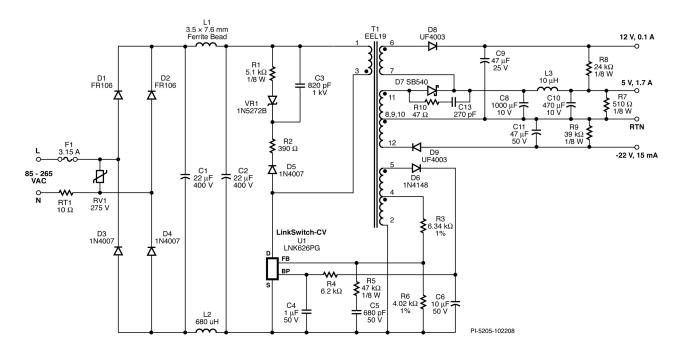


Figure 2 - Schematic.

## 4 Circuit Description

The LNK626PG was developed to be a cost effective solution in DVD Players, white goods, chargers or any application requiring a regulated constant voltage (CV) output. The LNK626PG has a monolithically integrated 700 V switching MOSFET and ON/OFF control function which together deliver high efficiency under all load conditions and low no-load energy consumption. Both the operating efficiency and no-load performance exceed all current international energy efficiency standards.

The LNK626PG controller consists of an oscillator, a feedback (sense and logic) circuit, a 5.8 V regulator, over-temperature protection, frequency jittering, a current-limit circuit, leading-edge blanking and an ON/OFF state machine for CV control.

The LNK626PG also provides a sophisticated range of protection features including autorestart for control loop component open/short circuit faults and output short circuit conditions. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

The IC package provides extended creepage distance between high and low voltage pins (both at the package and PCB), which is required in highly humid environments to prevent arcing and to further improve reliability.

The LNK626PG can be configured to either be self-biased from the high-voltage DRAIN pin, or to receive an optional external bias supply. When configured to be self-biased, the very low IC current consumption ensures a worst-case no-load power consumption of less than 200 mW at 230 VAC. With external bias, <70 mW is achievable.

This document contains the power supply specifications, schematic, bill of materials, transformer specifications, and typical performance characteristics for this reference design.

### 4.1 Input Section

Fuse F1 provides input current protection in case of a primary side component failure. Thermistor RT1 limits the inrush current when power is applied to the circuit. Metal oxide varistor RV1 provides differential line input surge protection, for surges greater than 2 kV. Below this level, RV1 may be omitted. Diodes D1 through D4 rectify the AC input, with D1 and D2 selected as a fast (500 ns) recovery to improve conducted EMI.

### 4.2 Input Filter

The AC input voltage is rectified by diodes D1 through D4 and filtered by C1 and C2. Capacitors C1 and C2 together with L1 and L2 form a pi  $(\pi)$  filter to attenuate conducted EMI.

### 4.3 Primary Clamp

The drain clamp network is formed by R1, R2, C3, D5 and VR1. This network limits the leakage inductance inducted drain voltage spike. However unlike secondary side feedback the drain clamp design also affects the output regulation and ripple performance.

Any ringing on the drain node also appears on the feedback winding and is therefore sampled by the FEEDBACK pin of U1. This can create an error between the output voltage and the sampled voltage seen by U1. This degrades regulation and output ripple. Sampling occurs between 2.1  $\mu$ s and 3.4  $\mu$ s after the primary switch turn off. Therefore ideally the drain voltage should settle to within ~1% of it's final value (equal to  $V_{OR}$ ) 2.1  $\mu$ s after turn off of the internal MOSFET.

The goal of the clamp design is to reduce drain node ringing while limiting the peak drain voltage and minimizing dissipation for high efficiency and low no-load input power consumption. To meet this set of goals a Zener bleed clamp configuration was used. This is a RCD clamp where the resistor is replaced by the series combination of a resistor (R1) and low power Zener (VR1). The addition of the Zener prevents the clamp capacitor (C3) from being discharged below the Zener voltage rating at light or no-load that would normally occur with a standard RCD clamp. This improves light load efficiency and reduces no-load input power. The instantaneous current through VR1 is limited by R1 allowing a standard low cost, low power Zener (versus a transient voltage suppressor type).

The value of VR1 is typically set 0%-20% above the value of  $V_{OR}$  (the output voltage reflected through the transformer turns ratio). Here it was chosen as 110 V the same as the  $V_{OR}$  to give the best possible output regulation. The value of R1 was selected to discharge C3 to the value of VR1 in 2.1  $\mu$ s.

In designs with higher transformer leakage inductance the value of R1 may need to be increased to keep the dissipation of VR1 acceptable. For designs with primary leakage inductance lower than ~100  $\mu$ H, VR1 may be replaced with a single resistor in the range of 100 k $\Omega$  to 470 k $\Omega$ .

To prevent high frequency ringing D5 was selected as a standard recovery diode versus a fast or ultra-fast type. Resistor R2 acts to dampen the drain ringing, the value being chosen to dampen the drain ring to an acceptable level while keeping the peak drain voltage to below the  $BV_{DSS}$  of the internal MOSFET.

### 4.4 Feedback

The ratio of R3 to R6 sets the output voltage level. The starting values are provided by the PI XIs design software. In some designs, C5 and R5 are required to eliminate excessive output ripple voltage caused by group pulsing. In LinkSwitch-CV applications, group pulsing is defined to be a group of five or more consecutive drain pulses followed

by four or more skipped pulses. The value of R5 should be greater than or equal to the value of 10xR6. The value of  $R5xC5 = 32 \mu s$  will provide optimum performance.

### 4.5 Optional Bias Circuit

Diodes D6, C6 and R4 along with a bias winding in the transformer provide an external bias supply. This circuit reduces the no load input power consumption to less than 150 mW (depending on the output preload resistor values) and increase efficiency. The components mentioned above may be removed if reduced no load input power and improved efficiency is not required.

### 4.6 LinkSwitch-CV Bypass Capacitor

LinkSwitch-CV requires a bypass capacitor of 1  $\mu$ F minimum to bias the internal circuitry. The voltage rating must be greater than 6.8 V. Electrolytic, tantalum or ceramic dielectric may be used.

## 4.7 Output Rectifiers and Filters

Diodes D7 rectifies and C8, C10 and L3 filter the 5 V output. A diode rated at 5 A was chosen for D7 to improve cross regulation. If the cross regulation specification was relaxed or for single output applications, a smaller diode could be used. Resistor R10 and C13 form a snubber to reduce conducted and radiated EMI.

Diode D8 and C9 rectify and filter the 12 V output. Diode D9 and C11 rectify and filter the -22 V output. Preload resistors R7, R8 and R9 limit the output voltages to safe levels in the event that the outputs become unloaded.

### 4.8 Output Y Capacitor

Capacitor C12 was not required to meet conducted EMI for a floating output test configuration. Other test configurations may require the use of a Y capacitor.

# 5 PCB Layout

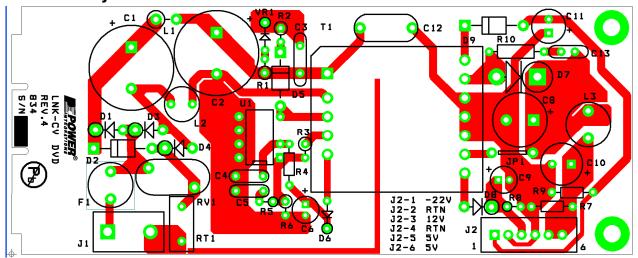


Figure 3 - Printed Circuit Layout.

# **Bill of Materials**

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C2	22 μF, 400 V, Electrolytic, Low ESR, 901 mOhm, (16 x 20)	EKMX401ELL220ML20S	Nippon Chemi-Con
2	1	C3	820 pF, 1 kV, Y5P, Disc Ceramic	ECK-A3A821KBP	Panasonic
3	1	C4	1.0 μF, 50 V, Ceramic, Z5U	B37988G5105M000	Epcos
4	1	C5	680 pF, 50 V, Ceramic, COG	B37979G5681J000	Epcos
5	1	C6	10 μF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL100ME11D	Nippon Chemi-Con
6	1	C8	1000 $\mu F,10$ V, Electrolytic, Very Low ESR, 38 m $\Omega,(10x16)$	EKZE100ELL102MJ16S	Nippon Chemi-Con
7	1	C9	47 $\mu F, 25$ V, Electrolytic, Low ESR, 500 m $\Omega, (5~x~11.5)$	ELXZ250ELL470MEB5D	Nippon Chemi-Con
8	1	C10	470 $\mu F,10$ V, Electrolytic, Very Low ESR, 72 m $\Omega,(8x11.5)$	EKZE100ELL471MHB5D	Nippon Chemi-Con
9	1	C11	47 $\mu\text{F}$ , 50 V, Electrolytic, Low ESR, 450 m $\Omega$ , (6.3 x 11.5)	ELXZ500ELL470MFB5D	Nippon Chemi-Con
10	1	C12	330 pF, Ceramic Y1	440LT33-R	Vishay
11	1	C13	270 pF, 50 V, Ceramic, COG	B37979N5271J000	Epcos
12	2	D1 D2	800 V, 1 A, Fast Recovery Diode, 500 ns, DO-41	FR106	Diodes Inc.
13	2	D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
14	1	D5	1000 V, 1 A, Rectifier, DO-41	1N4007	Vishay
15	1	D6	75 V, 300 mA, Fast Switching, DO-35	1N4148	Vishay
16	1	D7	40 V, 5 A, Schottky, DO-201AD	SB540	Vishay
17	2	D8 D9	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
18	1	F1	3.15A, 250V, TIME-LAG HI-BREAK TR5	38213150410	Wickman
19	1	J1	2 Position (1 x 2) header, 0.312 pitch, Vertical	26-50-3039	Molex
20	1	J2	6 Position (1 x 6) header, 2.5 mm pitch, Vertical	DF1B-6P-2.5DSA	Hirose Electric Co
21	1	JP1	Wire Jumper, Insulated, 22 AWG, 0.3 in	C2004-12-02	Gen Cable
22	1	L1	3.5 mm x 7.6 mm, 75 $\Omega$ at 25 MHz, 22 AWG hole, Ferrite Bead	2743004112	Fair-Rite
23	1	L2	680 uH, 0.21 A, 7 x 10.5 mm	SBC2-681-211	Tokin
24	1	L3	10 uH, 3.0 A	R622LY-100K	Toko
25	1	R1	5.1 k $\Omega$ , 5%, 1/4 W, Carbon Film	CFR-25JB-5K1	Yageo
26	1	R2	390 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-390R	Yageo
27	1	R3	$6.34$ k $\Omega$ , 1%, 1/4 W, Metal Film	MFR-25FBF-6K34	Yageo
28	1	R4	6.2 k Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-6K2	Yageo
29	1	R5	47 k Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-47K	Yageo
30	1	R6	4.02 k Ω, 1%, 1/4 W, Metal Film	MFR-25FBF-4K02	Yageo
31	1	R7	510 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-510R	Yageo
32	1	R8	24 k Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-24K	Yageo
33	1	R9	39 k Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-39K	Yageo
34	1	R10	47 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-47R	Yageo
35	1	RT1	NTC Thermistor, 10 Ohms, 1.7 A	CL-120	Thermometrics
36	1	RV1	275 V, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
37 38	1 1	T1 U1	Transformer, EEL19 Horizontal 12 pin (5/7). LinkSwitch-II, LNK626PG, CV/CC, DIP-8C	Santronics LNK626PG	SNX R1464 Power Integrations
39	1	VR1	110 V, 5%, 500 mW, DO-35	1N5272B	Microsemi
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# 7 Transformer Specification

## 7.1 Electrical Diagram

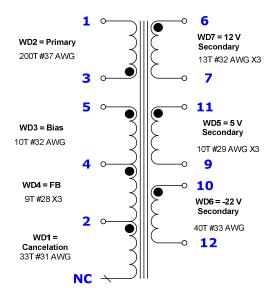


Figure 4 – Transformer Electrical Diagram.

# 7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1-5 to Pins 6-12	4250 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 VRMS	1.62 μH, ±10%
Resonant Frequency	Pins 1-3, all other windings open	375 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with Pins 9-11 shorted, measured at 100 kHz, 0.4 VRMS	210 μH (Max.)

# 7.3 Materials

Item	Description
[1]	Core: EEL19 PC40 or equivalent. Gapped to 40.5 nH/T <sup>2</sup>
[2]	Bobbin: EEL19 Horizontal 12 pin (5/7).

### Transformer Build Diagram 7.4

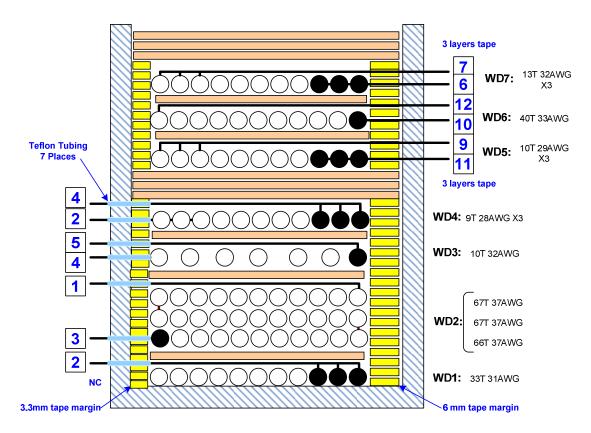


Figure 5 – Transformer Build Diagram.

# 8 Transformer Spreadsheets

7 Watt (10 W Peak) DVD Application	INPUT	INFO	OUTPUT	UNIT	ACDC_LNK-CV_080508_Rev0-5.xls; LinkSwitch-CV Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION V	/ARIABLES				Customer
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage
PO	10.00			Watts	Output Power
n	0.68				Efficiency Estimate
Z			0.5		Loss Allocation Factor
tC	3.50		3.5	mSecon	Bridge Rectifier Conduction Time Estimate
				ds	
CIN	44.00			uFarads	Input Filter Capacitor

ENTER LinkSwitch-CV LinkSwitch-CV	VARIABLES LNK626P			Univers al	115 Doubled/230V
Chosen Device		LNK626P	Power Out	10W	17W
ILIMITMIN			0.419	Amps	LinkSwitch-CV Minimum Current Limit
ILIMITMAX			0.482	Amps	LinkSwitch-CV Maximum Current Limit
fS			100000	Hertz	LinkSwitch-CV Switching Frequency
I2FMIN			18225	Hertz	LinkSwitch-CV Min I2F (power Co-efficienct)
I2FMAX			23693	Hertz	LinkSwitch-CV Max I2F (power Co-efficienct)
VOR	110.00		110	Volts	Reflected Output Voltage
VDS			10	Volts	LinkSwitch-CV on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
DCON			5.58	us	Output Diode conduction time
KP_TRANSIENT			0.70		Worst case ripple to peak current ratio. Maintain
					KP_TRANSIENT below 0.25
KP			0.73		Ripple to Peak Current Ratio (0.4 <krp<1.0:< td=""></krp<1.0:<>
					1.0 <kdp<6.0)< td=""></kdp<6.0)<>

ENTER TRANSFORM Core Type	ER CORE/CONSTR	RUCTION VARIABLES		
Core	ELLIO	EEL19	P/N:	PC40EE19/27/5-Z
Bobbin		EEL19_BOBBIN	P/N:	*
AE		0.2454	cm^2	Core Effective Cross Sectional Area
LE		6.185	cm	Core Effective Path Length
AL		720	nH/T^2	Ungapped Core Effective Inductance
BW		19.7	mm	Bobbin Physical Winding Width
M	4.50		mm	Safety Margin Width (Half the Primary to
				Secondary Creepage Distance)
L	3.00	3		Number of Primary Layers
NS	10.00	10		Number of Secondary Turns

DC INPUT VOLTAGE PA	RAMETERS				
VMIN		101	Volts	Minimum DC Input Voltage	
VMAX		375	Volts	Maximum DC Input Voltage	

Bias Winding Paramete	rs	
Add Bias winding NB	YES	Enter Yes if you want to add a Bias winding Number of Bias winding turns - AC stacked on Feedback winding

CURRENT WAVEFORM SHAPE PARAMETERS			
DMAX	0.55		Maximum Duty Cycle
IAVG	0.15	Amps	Average Primary Current
IP	0.42	Amps	Minimum Peak Primary Current
IR	0.30	Amps	Primary Ripple Current
IRMS	0.21	Amps	Primary RMS Current

TRANSFORMER PRIMARY DESIGN PARAME	TERS		
LPMIN	1465	uHenrie	Minimum Primary Inductance
		s	·
LP_TOL	10		
NP	200		Primary Winding Number of Turns
ALG	37	nH/T^2	Gapped Core Effective Inductance
BM	1438	Gauss	Maximum Flux Density, (BP<3100)
BAC	455	Gauss	AC Flux Density for Core Loss Curves (0.5 X
			Peak to Peak)
ur	1444		Relative Permeability of Ungapped Core
LG	0.80	mm	Gap Length (Lg > 0.1 mm)
BWE	32.1	mm	Effective Bobbin Width
OD	0.16	mm	Maximum Primary Wire Diameter including
			insulation
INS	0.04	mm	Estimated Total Insulation Thickness (= 2 * film
			thickness)
DIA	0.12	mm	Bare conductor diameter
AWG	37	AWG	Primary Wire Gauge (Rounded to next smaller
			standard AWG value)
CM	20	Cmils	Bare conductor effective area in circular mils
CMA Wa	arning 97	Cmils/A	!!! INCREASE CMA>200 (increase L(primary
		mp	layers),decrease NS,larger Core)

TRANSFORMER SECONDARY DESIGN PARAMETERS Lumped parameters			
ISP	8.38	Amps	Peak Secondary Current
ISRMS	3.77	Amps	Secondary RMS Current
10	2.00	Amps	Power Supply Output Current
IRIPPLE	3.20	Amps	Output Capacitor RMS Ripple Current
CMS	755	Cmils	Secondary Bare Conductor minimum circular mils
AWGS	21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS	0.73	mm	Secondary Minimum Bare Conductor Diameter
ODS	1.07	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS	0.17	mm	Maximum Secondary Insulation Wall Thickness

VOLTAGE STRESS PARAMETERS			
VDRAIN	626	Volts	Maximum Drain Voltage Estimate (Includes
			Effect of Leakage Inductance)
PIVS	24	Volts	Output Rectifier Maximum Peak Inverse Voltage

FEEDBACK VARIABL	.ES				
NFB		9.00		Feedback winding number of turns	
RUPPER		9.05	k-ohms	Upper resistor of feedback network	
RLOWER		6.13	k-ohms	Lower resistor of feedback network	

TRANSFORMER SEC	TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)						
1st output							
VO1	5.00	5	Volts	Output Voltage (if unused, defaults to single output design)			
IO1	1.70	1.700	Amps	Output DC Current			
PO1		8.50	Watts	Output Power			
VD1		0.5	Volts	Output Diode Forward Voltage Drop			
NS1		10.00		Output Winding Number of Turns			
ISRMS1		3.207	Amps	Output Winding RMS Current			
IRIPPLE1		2.72	Amps	Output Capacitor RMS Ripple Current			
PIVS1		24	Volts	Output Rectifier Maximum Peak Inverse Voltage			
CMS1		641	Cmils	Output Winding Bare Conductor minimum circular mils			
AWGS1		22	AWG	Wire Gauge (Rounded up to next larger standard AWG value)			
DIAS1		0.65	mm	Minimum Bare Conductor Diameter			

ODS1	1.07	mm	Maximum Outside Diameter for Triple Insulated Wire	
			vviie	

2nd output				
VO2	12.00		Volts	Output Voltage
IO2	0.10		Amps	Output DC Current
PO2		1.20	Watts	Output Power
VD2		0.7	Volts	Output Diode Forward Voltage Drop
NS2		23.09		Output Winding Number of Turns
ISRMS2		0.189	Amps	Output Winding RMS Current
IRIPPLE2		0.16	Amps	Output Capacitor RMS Ripple Current
PIVS2		55	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2		38	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2		34	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2		0.16	mm	Minimum Bare Conductor Diameter
ODS2		0.46	mm	Maximum Outside Diameter for Triple Insulated Wire

3rd output				
VO3	22.00		Volts	Output Voltage
IO3	0.02		Amps	Output DC Current
PO3		0.33	Watts	Output Power
VD3		0.7	Volts	Output Diode Forward Voltage Drop
NS3		41.27		Output Winding Number of Turns
ISRMS3		0.028	Amps	Output Winding RMS Current
IRIPPLE3		0.02	Amps	Output Capacitor RMS Ripple Current
PIVS3		99	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3		6	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3		42	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3		0.06	mm	Minimum Bare Conductor Diameter
ODS3		0.26	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power		10.03	Watts	Total Output Power
Negative Output	3	3		Output # 3 is negative output

### Notes:

- Primary winding CMA warning is allowed because this occurs during peak loading. CMA is higher under normal operation.
- Rupper and Rlower values may be different in the actual assembly due to tuning of output voltages.
- The -22 V winding turns was adjusted from 41 to 40 turns to center the output voltage.
- The transformer was designed with a flux density below 1500 Gauss (150 mT) to reduce audible noise generation from the transformer. A flux density around this level is recommended when using long cores (EEL vs EE). Higher flux densities are possible for EE cores or with EEL cores where higher levels of audible noise are acceptable.

# 9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

# 9.1 Efficiency

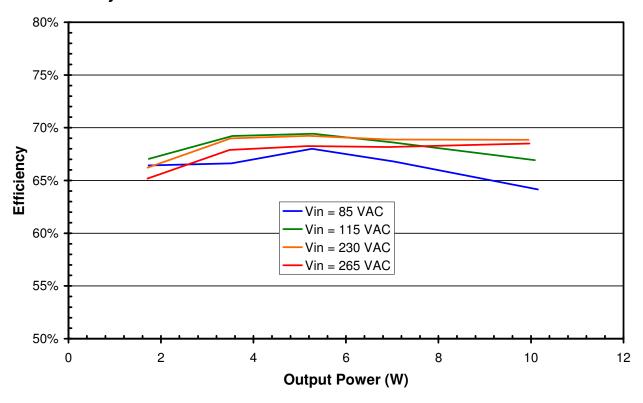


Figure 6 – Efficiency vs. Input Voltage, Room Temperature, 60 Hz.

# No-load Input Power

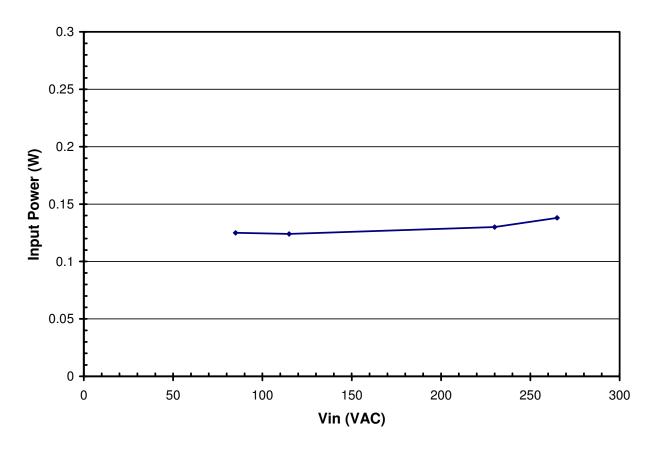


Figure 7 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

## 9.2 Available Standby Output Power

The chart below shows the available output power vs line voltage for an input power of 1 W, 0.5 W and 0.3 W.

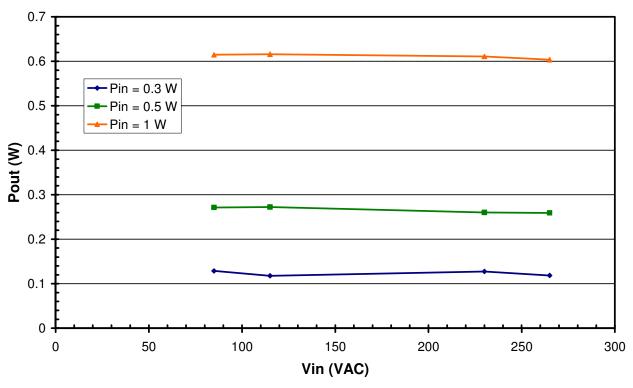
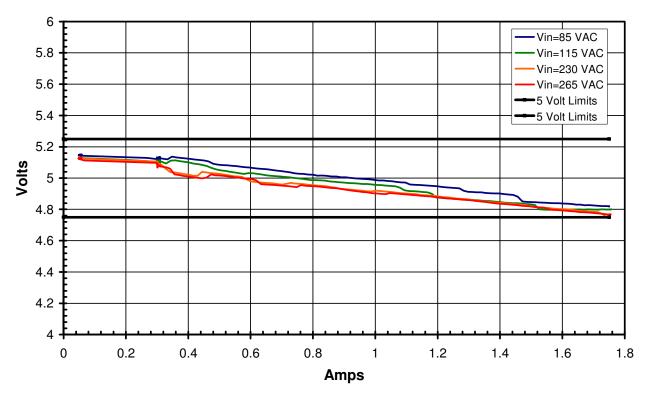


Figure 8 — Available Standby Power.

## 9.3 Regulation

## 9.3.1 Load Regulation

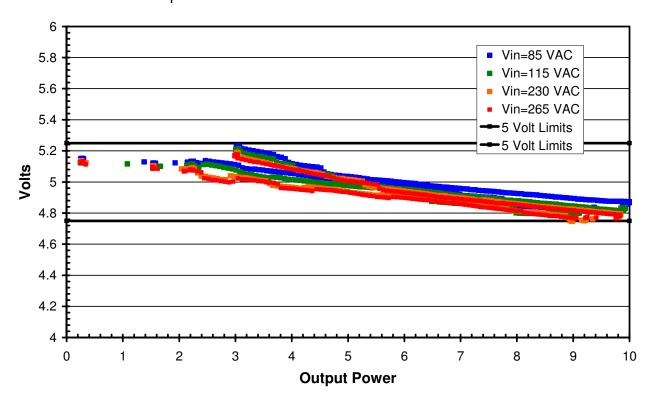
The 5 Volt output current was varied from 0.05 Amp to 1.75 Amps. The +12 V current was constant at 0.1 Amp and the -22 V current was constant at 15 mA.



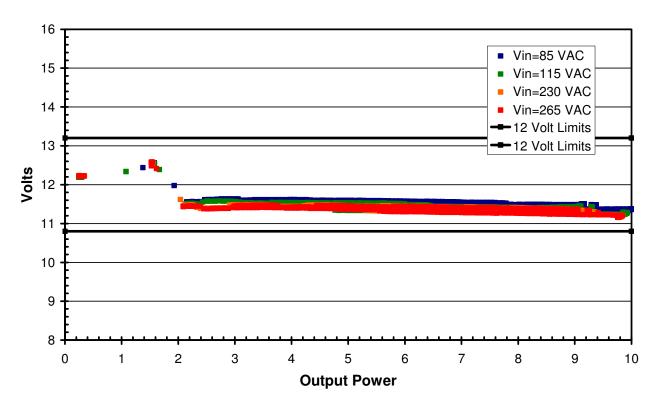
**Figure 9** – Load Regulation, Room Temperature.

### 9.3.2 Cross Regulation

The figures below show the output voltage vs. total output power. The charts show the voltage variations as the loads vary for all legal load combinations. The 5 V current varied from 50 mA to 1.75 Amps. The 12 V output current varied from 50 mA to 100 mA. The -22 V output current varied from 5 mA to 15 mA.



**Figure 10** – 5 V Cross Regulation, Room Temperature.



**Figure 11** – 12 V Cross Regulation, Room Temperature.

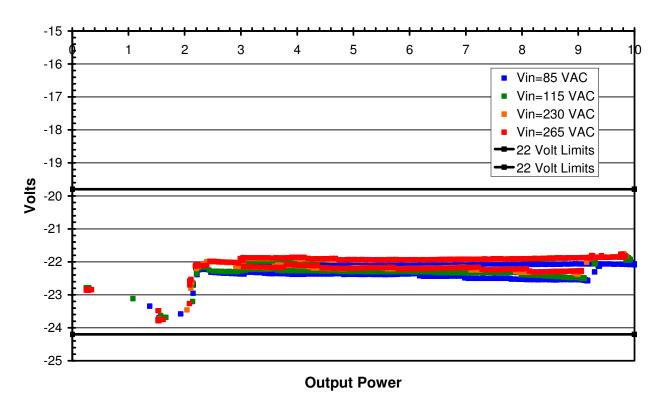


Figure 12 – 22 V Cross Regulation, Room Temperature.



The graphs below show the output Voltage and load currents required to power a DVD player. The graphs represent the current demand as the DVD player is exercised in all operating modes. The Model used was a Philips DVP 5990.

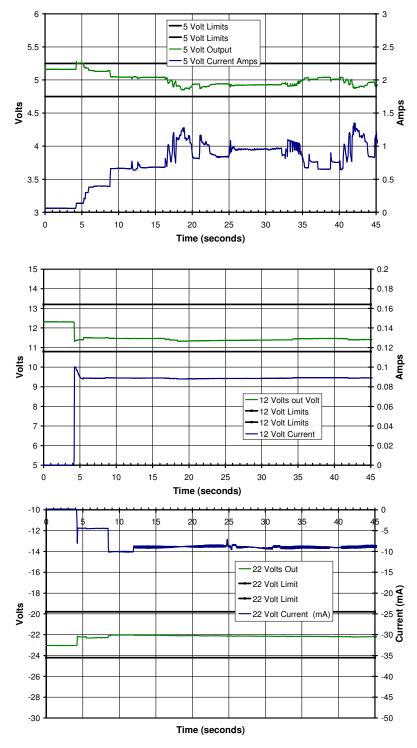


Figure 13 – Voltage Regulation and Current Demands in DVD Application.

# 10 Thermal Performance

The power supply was placed inside a cardboard box (no air flow) in the temperature chamber. The loads are as follows: 5 V at 1 Amp

12 V at 0.1 Amp -22 V at 15 mA

This load represents a typical DVD player Load during Play Mode. The ambient temperature was measured inside the cardboard box.

Item	Temperature Deg C						
Item	85 VAC	115 VAC	230 VAC	265 VAC			
Ambient	40	40	40	40			
Clamp Zener (VR1)	88.9	84.8	82.7	83.0			
LNK626 (U1)	68.0	65.1	66.4	65.0			



## 11 Waveforms

### 11.1 Drain Voltage and Current, Normal Operation

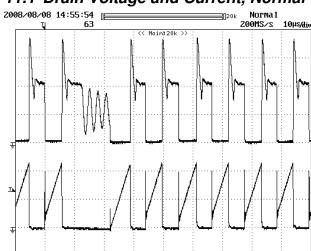


Figure 14 - 85 VAC, Full Load (10 W). Upper:  $V_{DRAIN}$ , 100 V, 10  $\mu s$  / div. Lower:  $I_{DRAIN}$ , 0.2 A / div.

# 

Figure 15 - 265 VAC, Full Load (10 W). Upper:  $V_{DRAIN}$ , 200 V, 10  $\mu s$  / div. Lower:  $I_{DRAIN}$ , 0.2 A / div.

## 11.2 Output Voltage Start-up Profile

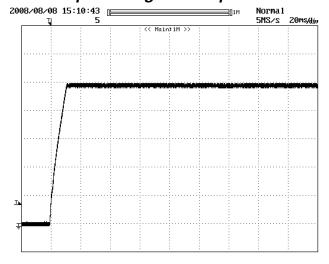


Figure 16 – 5 V Start-up Profile, 115 VAC 1 V, 20 ms / div.

Figure 17 – 5 V Start-up Profile, 230 VAC 1 V, 20 ms / div.

# 11.3 Drain Voltage and Current Start-up Profile

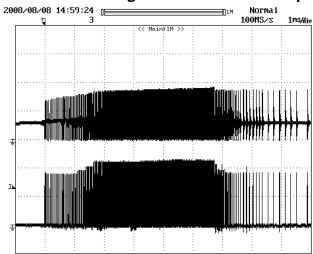


Figure 18 – 85 VAC Input and Maximum Load. Upper:  $V_{DRAIN}$ , 200 V, 1 ms / div. Lower:  $I_{DRAIN}$ , 0.2 A / div.

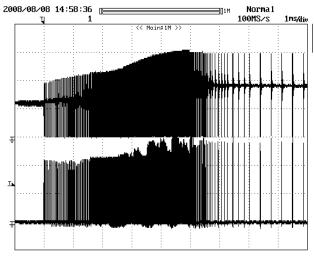
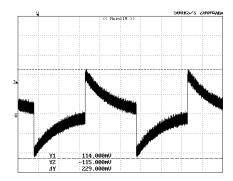


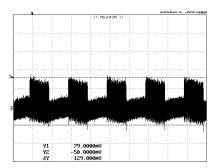
Figure 19 – 265 VAC Input and Maximum Load. Upper: V<sub>DRAIN</sub>, 200 V, 1 ms / div. Lower: I<sub>DRAIN</sub>, 0.2 A / div.

### 11.4 Load Transient Response (50% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

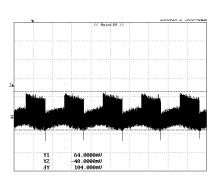


**Figure 20** – Transient Response, 115 VAC, 5 V Load Step: 0.55 A – 1.10 A -0.55 A 5 V Output 50 mV, 200 ms / div.

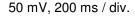


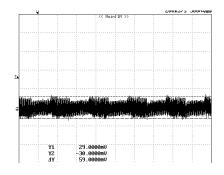
**Figure 21** – Transient Response, 115 VAC, 12 V Output Response During 5 V Transient.





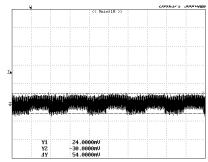
**Figure 24** – Transient Response, 230 VAC, 12 V Output Response During 5 V Transient.





**Figure 22** – Transient Response, 115 VAC, -22 V Output Response During 5 V Transient.

50 mV, 200 ms/div.



**Figure 25** – Transient Response, 230 VAC, -22 V Output Response During 5 V Transient.

50 mV, 200 ms / div.



Figure 23 – Transient Response,

230 VAC, 5 V Load Step: 0.55 A -

1.10 A -0.55 A

50 mV, 200 ms / div.

5 V Output

### 11.5 Output Ripple Measurements

### 11.5.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1  $\mu$ F/50 V ceramic capacitor and a 1.0  $\mu$ F/50 V aluminum-electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

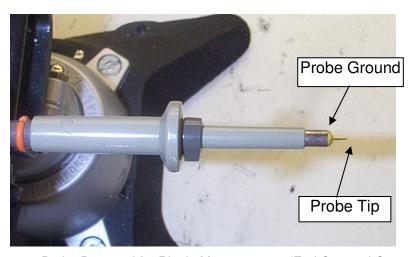


Figure 26 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 27 – Oscilloscope Probe with Probe Master (<u>www.probemaster.com</u>) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

### 11.5.2 Measurement Results

Unless otherwise specified, full load is: 5 Volts @ 1.10 A 12 Volts @ 0.10 A -22 Volts @ 0.015 A

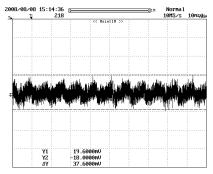


Figure 28 – 5 V Ripple, 85 VAC, Full Load (7W) 10 ms, 20 mV / div. Ripple: 38 mVp-p.

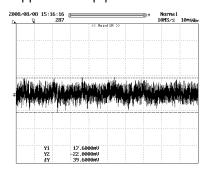
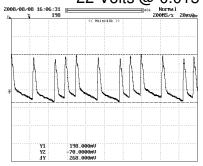


Figure 31 – 5 V Ripple, 115 VAC, Full Load (7 W). 10 ms, 20 mV / div. Ripple: 40 mVp-p.



**Figure 29** – 12 V Ripple, 85 VAC, Full Load. 10 μs, 100 mV / div. Ripple: 268 mVp-p.

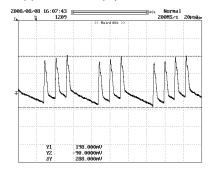
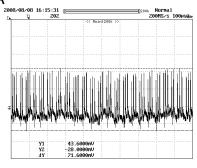
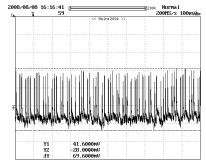


Figure 32 – 12 V Ripple, 115 VAC, Full Load. 20 μs, 100 mV / div. Ripple: 288 mVp-p.



**Figure 30** – -22 V Ripple, 85 VAC, Full Load. 100 μs, 20 mV / div. Ripple: 72 mVp-p.



**Figure 33** – -22 V Ripple, 115 VAC, Full Load. 100 μs, 20 mV / div. Ripple: 70 mVp-p.

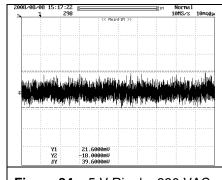
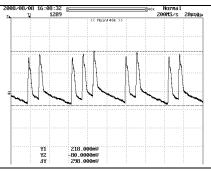
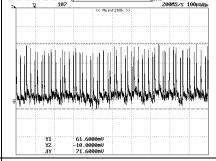


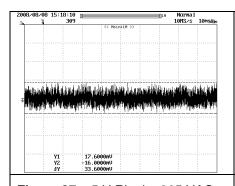
Figure 34 – 5 V Ripple, 230 VAC, Full Load (7W). 10 ms, 20 mV /div. Ripple: 40 mVp-p.

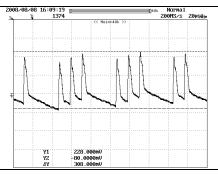


**Figure 35** – 12 V Ripple, 230 VAC, Full Load. 20 μs, 100 mV / div. Ripple: 258 mVp-p.



**Figure 36** – -22 V Ripple, 230 VAC,Full Load. 100 μs, 20 mV / div. Ripple: 72 mVp-p.





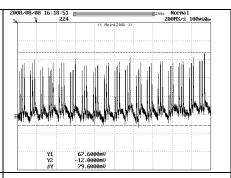


Figure 37 – 5 V Ripple, 265 VAC, Full Load (7 W). 10  $\mu$ s, 20 mV /div. Ripple: 33 mVp-p.

Figure 38 - 12 V Ripple, 265 VAC, Full Load. 20  $\mu$ s, 100 mV / div. Ripple: 308 mVp-p.

Figure 39 – -22 V Ripple, 265 VAC, Full Load. 100 µs, 20 mV / div. Ripple: 80 mVp-p.

# 12 Line Surge

Differential input line 1.2/50  $\mu s$  surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Generator Output Impedance (Ω)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2000	12	230	L to N	90	Pass
-2000	12	230	L to N	270	Pass
+2000	2	230	L to N	90	Pass
-2000	2	230	L to N	270	Pass
+6000 ring wave	12	230	L1/L2 - PE	90	Pass
-6000 ring wave	12	230	L1/L2 - PE	270	Pass
+6000	2	230	L1/L2 - PE	90	Pass
-6000	2	230	L,N to Output RTN	270	Pass

Unit passes under all test conditions.

### 13 Conducted EMI

Conducted EMI was measured with the power supply operating a DVD Player. Six plots show the conducted EMI for 115 VAC and 230 VAC and with the player in Standby Mode, On Mode (no disk in payer) and Play Mode. The DVD player chassis was not grounded for these measurements. Other testing configurations may require a Y capacitor to meet EMI requirements.

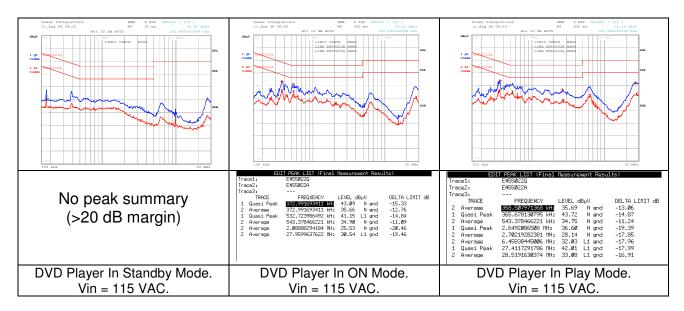


Figure 43 — Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits.

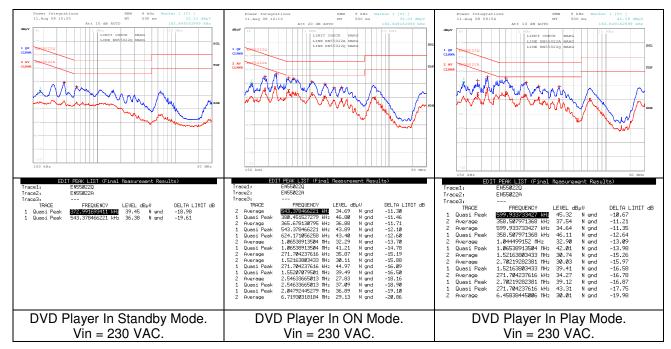
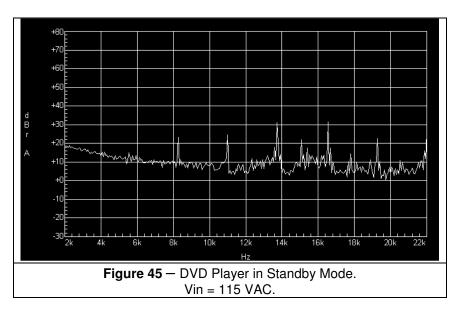
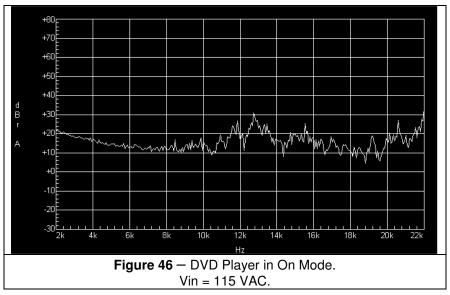


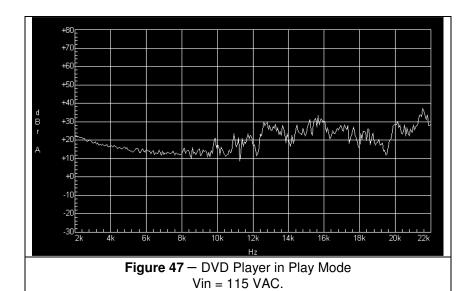
Figure 44 - Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits.

### 14 Audible Noise

The power supply's audible noise was measured while operating a DVD Player. With the case removed the microphone was placed 2 cm directly above the transformer. Measurements were made with a calibrated microphone and Audio Precision System II audio analyzer. Audio levels below 35 dBA measured in this way are considered inaudible when the case in fitted.







# **Revision History**

Date	<b>Author</b>	Revision	Description & changes	<b>Reviewed</b>
11-Nov-08	JAC	1.0	Initial Release	PV

# Notes

# **Notes**

# **Notes**

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5245 Hellyer Avenue San Jose, CA 95138, USA. Main: +1-408-414-9200 Customer Service: Phone: +1-408-414-9665 Fax: +1-408-414-9765 e-mail: usasales@powerint.com

### **GERMANY**

Rueckertstrasse 3

#1, 14<sup>th</sup> Main Road

D-80336, Munich Germany Phone: +49-89-5527-3911 Fax: +49-89-5527-3920 e-mail: eurosales@powerint.com

### **JAPAN**

Kosei Dai-3 Bldg., 2-12-11, Shin-Yokohama, Kohoku-ku, Yokohama-shi, Kanagawa 222-0033 Phone: +81-45-471-1021 Fax: +81-45-471-3717 e-mail: japansales@powerint.com

### **TAIWAN**

5F, No. 318, Nei Hu Rd., Sec. 1 Nei Hu Dist. Taipei, Taiwan 114, R.O.C. Phone: +886-2-2659-4570 Fax: +886-2-2659-4550 e-mail: taiwansales@powerint.com

### CHINA (SHANGHAI)

Rm 1601/1610, Tower 1, Kerry Everbright City No. 218 Tianmu Road West, Shanghai, P.R.C. 200070 Phone: +86-21-6354-6323 Fax: +86-21-6354-6325 e-mail: chinasales@powerint.com

### INDIA

Vasanthanagar Bangalore-560052 India Phone: +91-80-41138020 Fax: +91-80-41138023 e-mail: indiasales@powerint.com

### **KOREA**

RM 602, 6FL Korea City Air Terminal B/D, 159-6 Samsung-Dong, Kangnam-Gu, Seoul, 135-728, Korea Phone: +82-2-2016-6610 Fax: +82-2-2016-6630 e-mail: koreasales@powerint.com

### UNITED KINGDOM

1st Floor, St. James's House East Street, Farnham Surrey, GU9 7TJ United Kingdom Phone: +44 (0) 1252-730-141 Fax: +44 (0) 1252-727-689 e-mail: eurosales@powerint.com

### **CHINA (SHENZHEN)**

Rm A, B & C 4<sup>th</sup> Floor, Block C, Electronics Science and Technology Building, 2070 Shennan Zhong Rd, Shenzhen, Guangdong, China, 518031 Phone: +86-755-8379-3243 Fax: +86-755-8379-5828

chinasales@powerint.com

### ITALY

Via De Amicis 2 20091 Bresso MI – Italy Phone: +39-028-928-6000 Fax: +39-028-928-6009 e-mail: eurosales@powerint.com

### **SINGAPORE**

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### APPLICATIONS HOTLINE

World Wide +1-408-414-9660

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