



Design Example Report

Title	<i>22W 3 Output DC/DC Converter using DPA424R</i>
Specification	Input: -36 to -75VDC Output: 3.3V/3.5A, 5V/1A, -5V/-1A
Application	Telecom
Author	Power Integrations Applications Department
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Summary and Features

- 3 Output 22W DC/DC converter with minimal component count and cost.
- Full short circuit and thermal protection
- Very tight cross-regulation
- Over voltage and under voltage shutdown
- 89% Full Power Efficiency at 48V Input

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com.

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Important Notes:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.



1 Introduction

This document is an engineering report describing a 22W power supply utilizing DPA424R.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data taken from the prototype unit shown in Figure 1 below.

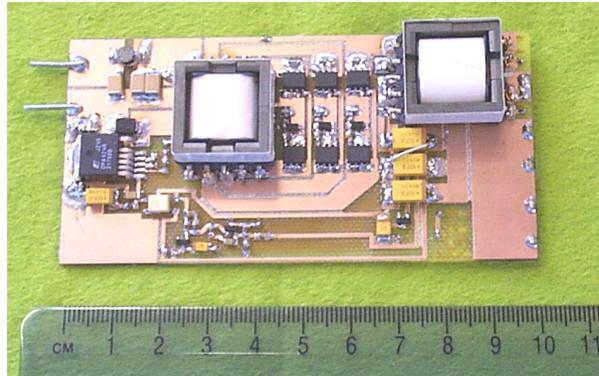


Figure 1 – Populated Circuit Board (Scale in cm)



2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input Voltage	V_{IN}	-36	-48	-75	VDC	
Output						
Output Voltage 1	V_{OUT1}	3.14	3.3	3.47	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			30	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}			3.5	A	
Output Voltage 2	V_{OUT2}	4.75	5	5.25	V	± 5%
Output Ripple Voltage 2	$V_{RIPPLE2}$			30	mV	20 MHz Bandwidth
Output Current 2	I_{OUT2}			1	A	
Output Voltage 3	V_{OUT3}	-5.25	-5	-4.75	V	± 5%
Output Ripple Voltage 3	$V_{RIPPLE3}$			30	mV	20 MHz Bandwidth
Output Current 3	I_{OUT3}			-1	A	
Total Output Power						
Continuous Output Power	P_{OUT}			22	W	
Efficiency	η	89			%	Measured at P_{OUT} (20 W), 25 °C, -48V Input
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

Table 1 - DC/DC Converter Specification



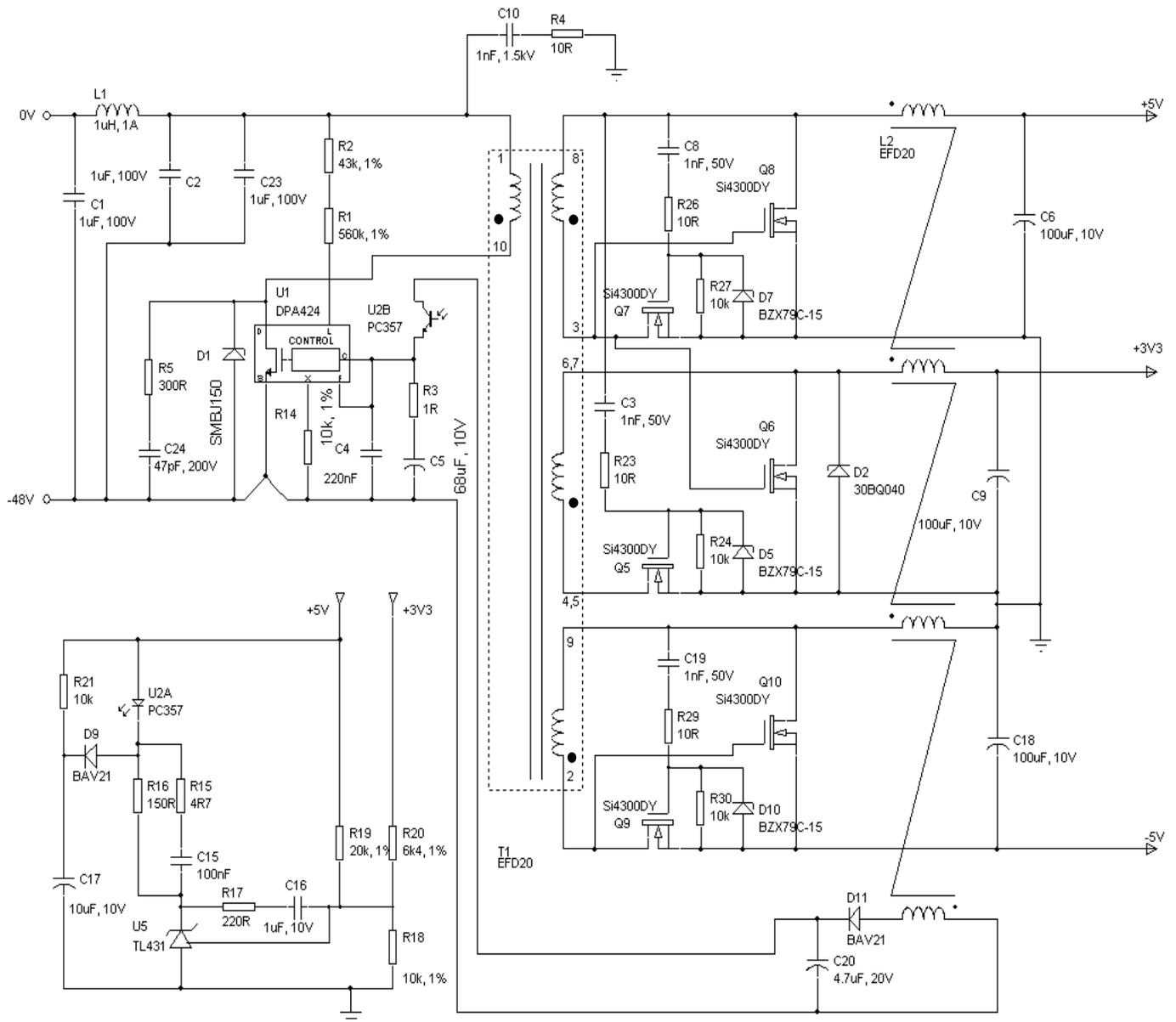


Figure 2 – Schematic



3.1 Circuit Description

The main power conversion stage uses a forward converter with coupled output inductor to give very good cross regulation. Also, the forward converter allows a low cost self-driven synchronous rectifier scheme to be used to boost conversion efficiency.

3.1.1 DPA-Switch Primary

A DPA-Switch is used on the primary side: in addition to the MOSFET and control circuitry, DPA-Switch also integrates:-

- High accuracy internal cycle by cycle current sensing which eliminates the need for external sense components
- Hysteretic short circuit and thermal protection to give high reliability
- Source connected to the device tab to minimize EMI
- Over voltage and undervoltage protection to ETSI standards
- Built in soft start to increase system reliability

Input filtering is provided by C1, L1, C2 and C23. These components filter the differential switching current. A common-mode choke and x-capacitor may be required to meet EMI requirements, depending upon system level considerations.

3.1.2 Output Rectification

Output rectification is achieved using self-driven synchronous MOSFETs on all the outputs. The Si4300DY MOSFETs chosen give low gate charge and also include a parallel Schottky diode which is required to freewheel current when the synchronous MOSFETs (Q8, Q6 and Q10) turn off. Q7, Q5 and Q9 don't require the parallel Schottky diode but should exhibit low gate charge if alternative devices are used. The gate charge on the Si4300DY is typically 8.7nC at $V_{DS}=15V$ and $V_{GS}=5V$.

Drive for the synchronous MOSFETs on the 3.3 winding has been taken from the 5V winding to ensure there was enough drive voltage to switch all the MOSFETs on properly.

3.1.3 Output Feedback

Feedback has been derived from the 3.3 and 5V rails with a 50:50 influence from each rail. A precision 2.5V TL431 reference has been used to give good regulation accuracy. In addition, a soft-finish network of D9, C17 and R21 has been used to give zero output over-shoot during start-up.



4 PCB Layout

The PCB was designed using 1oz copper PCB material.

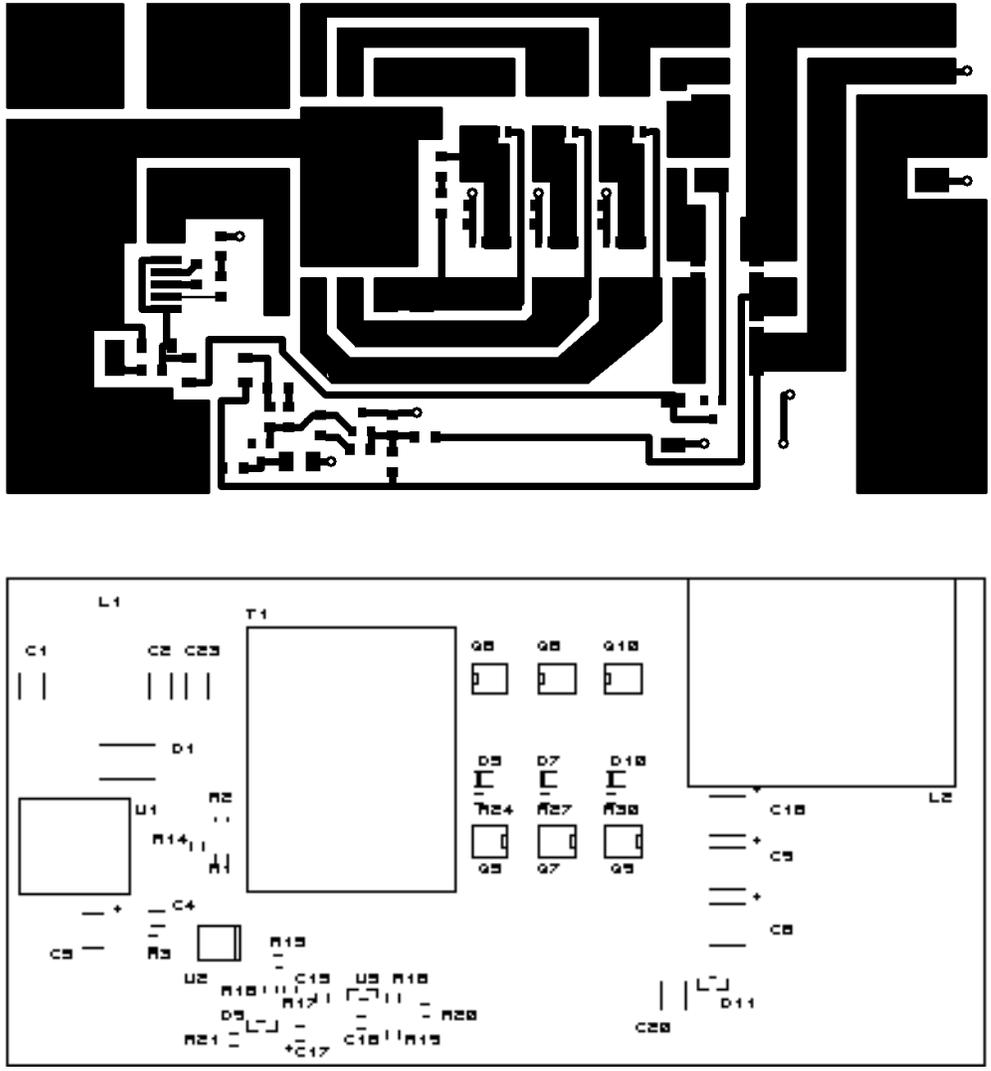


Figure 3 - Copper Top Side and Silk Screen (Scale not 1:1)



5 Bill Of Materials

Type	Reference	Quantity	Value / Description	Manufacturers Part Number	Manufacturer
RESISTORS	R1	1	560k, 1%	ERJ-3EKF5603V	Panasonic
	R2	1	43k, 1%	ERJ-3EKF4302V	Panasonic
	R3	1	1R, 5%, 0603	ERJ-3GEYJ1R0V	Panasonic
	R4,R23,R26,R29	4	10R, 5%, 0603	ERJ-3GEYJ100V	Panasonic
	R5	1	300R, 5%, 0603	ERJ-3GEYJ301V	Panasonic
	R21,R24,R27,R30	4	10k, 5%, 0603	ERJ-3GEYJ103V	Panasonic
	R14,R18	2	10k, 1%, 0603	ERJ-3EKF1002V	Panasonic
	R15	1	4R7, 5%, 0603	ERJ-3GEYJ4R7V	Panasonic
	R16	1	150R, 5%, 0603	ERJ-3GEYJ151V	Panasonic
	R17	1	220R, 5%, 0603	ERJ-3GEYJ221V	Panasonic
	R19	1	20k, 1%, 0603	ERJ-3EKF2002V	Panasonic
R20	1	6k4, 1%, 0603	ERJ-3EKF6401V	Panasonic	
CAPACITORS	C1,C2,C23	3	1uF, 100V, 1812	THCR50E2A105ZT	UCC
	C3,C8,C19	3	1nF, 50V		
	C4	1	220nF, 25V, 0805	ECJ-2VB1C224K	Panasonic
	C5	1	68uF, 10V, Tantalum C Size	T491C476K010	Kemet
	C6,C9,C18	3	100uF, 10V, Tantalum	TPSD10710R0100	AVX
	C10	1	1nF, 1.5kV, 1808	1808SC102KAT1A	AVX
	C15	1	100nF, 25V, 0805	ECJ-2YB1E104K	Panasonic
	C16	1	1uF, 10V, 0805	ECJ-2YB1A105K	Panasonic
	C17	1	10uF, 20V, Tantalum size B	ECS-T1DY106R	Panasonic
	C20	1	4.7uF, 20V, Tantalum size B	ECS-T1DY475R	Panasonic
C24	1	47pF, 200V, 0805	ECJ-2VC2D470J	Panasonic	
IC's	U1	1	DPA424		Power Integrations
	U2	1	PC357N1T		Sharp
	U5	1	TL431		National Semiconductor
MOSFETS	Q5,Q6,Q7,Q8,Q9,Q10	6	Si4300DY		Vishay Siliconix
DIODES	D1	1	SMBJ150		General Semiconductor
	D2	1	30BQ040		International Rectifier
	D5,D7,D10	3	BZX79C-15		General Semiconductor
	D9, D11	2	BAV21		General Semiconductor
MAGNETICS	L1	1	1uH, 2.5A	SCD-0403-1ROM	Chilisin
	L2	1	Custom EFD20		
	T1	1	Custom EFD20		

Total of 55 components



6 Magnetics Specification

6.1 Transformer Design

6.1.1 Electrical Diagram

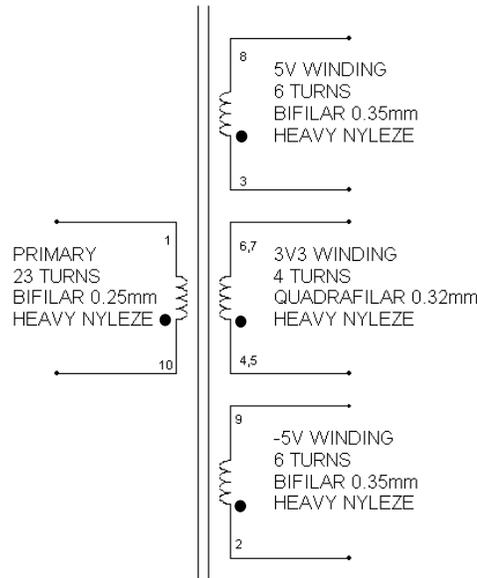


Figure 4 – Transformer Electrical Diagram

6.1.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1 and 10 to all other pins	500V
Primary Inductance	Pins 1-10, all other windings open, measured at 100 kHz, 0.4 VRMS	600 μ H, -0/+20%
Resonant Frequency	Pins 1-10, all other windings open	1 MHz (Min.)
Primary Leakage Inductance	Pins 1-10, with all other pins shorted, measured at 100 kHz, 0.4 VRMS	20 μ H (Max.)

6.1.3 Materials

Item	Description
[1]	Core: EFD20, 3F3 or equivalent material
[2]	Bobbin: 10 pin surface mount EFD20 bobbin
[3]	Magnet Wire: 0.25mm Heavy Nyleze
[4]	Magnet Wire: 0.35mm Heavy Nyleze
[5]	Tape: 3M 13mm wide insulation tape
[6]	Varnish



6.1.4 Transformer Build Diagram

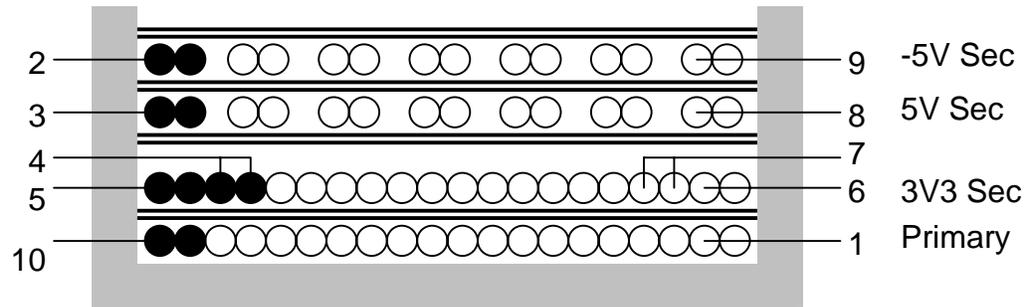


Figure 5 – Transformer Build Diagram

6.1.5 Transformer Construction

Bifilar Primary	Start at pin 10. Wind 23 bifilar turns of item [3] in approximately 1 layer. Terminate winding directly on pin 1.
Basic Insulation	Use two layers of item [5] for basic insulation.
3V3 Secondary	Start at pins 4 and 5. Wind 4 quadrifilar turns of item [4]. Spread turns evenly across bobbin. Finish on Pins 6 and 7.
Basic Insulation	Use two layers of item [5] for basic insulation.
5V Secondary	Start at pin 3. Wind 6 bifilar turns of item [4]. Spread turns evenly across bobbin. Finish on pin 8.
Basic Insulation	Use two layers of item [5] for basic insulation.
-5V Secondary	Start at pin 2. Wind 6 bifilar turns of item [4]. Spread turns evenly across bobbin. Finish on pin 9.
Final Assembly	Assemble and secure core halves. Varnish impregnate (item [6]).

6.2 Inductor Design

6.2.1 Electrical Diagram

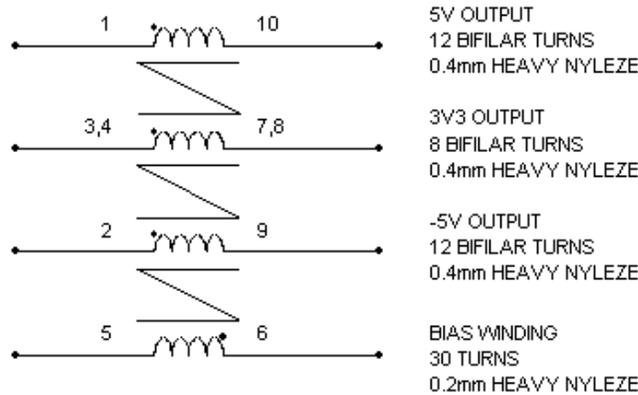


Figure 6 – Inductor Electrical Diagram

6.2.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 5 and 6 to all other pins	500V
3V3 Output Inductance	Pins 3,4 - 7,8, all other windings open, measured at 100 kHz, 0.4 VRMS	10uH

6.2.3 Materials

Item	Description
[1]	Core: EFD20, 3F3 or equivalent material gapped for 156nH/T ² (Approx 0.14mm)
[2]	Bobbin: 10 pin surface mount EFD20 bobbin
[3]	Magnet Wire: 0.2mm Heavy Nyleze
[4]	Magnet Wire: 0.4mm Heavy Nyleze
[5]	Tape: 3M 13mm wide insulation tape
[6]	Varnish



6.2.4 Inductor Build Diagram

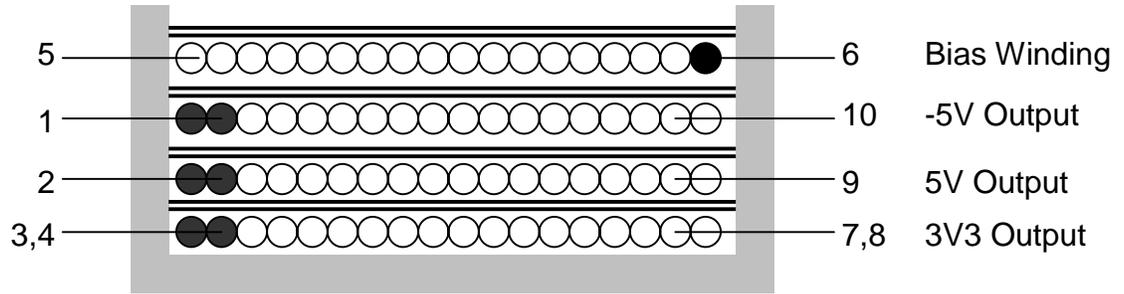


Figure 7 – Inductor Build Diagram

6.2.5 Inductor Construction

Bifilar 3V3 Winding	Start at pins 3,4. Wind 8 bifilar turns of item [4] in approximately 1 layer. Terminate winding directly on pins 7,8.
Basic Insulation	Use two layers of item [5] for basic insulation.
Bifilar 5V Winding	Start at pin 2. Wind 12 bifilar turns of item [4]. Spread turns evenly across bobbin. Finish on Pin 9.
Basic Insulation	Use two layers of item [5] for basic insulation.
Bifilar -5V Winding	Start at pin 1. Wind 12 bifilar turns of item [4]. Spread turns evenly across bobbin. Finish on pin 10.
Basic Insulation	Use two layers of item [5] for basic insulation.
Bias Winding	Start at pin 5. Wind 30 turns of item [3]. Spread turns evenly across bobbin. Finish on pin 6.
Final Assembly	Assemble and secure core halves. Varnish impregnate (item [6]).

7 Transformer Spreadsheets

	INPUT	INFO	OUTPUT	UNIT	
OUTPUT VOLTAGE AND CURRENT					
VMAIN	3.3			Volts	Main output voltage
IMAIN	3.5			Amps	Main output current
VOUT2	5			Volts	Output2 voltage
IOUT2	2			Amps	Output2 current
POUT			21.55	Watts	Total output power
VBIAS	12.0			Volts	DC bias voltage from output inductor winding
INPUT VOLTAGE AND UV/OV					
VMIN	36			DC volts	Minimum DC input voltage
VMAX	75			DC volts	Maximum DC input voltage
		min	max		
VUV OFF		29.3	32.4	DC volts	Minimum undervoltage On-Off threshold
VUV ON		31.5	33.9	DC volts	Maximum undervoltage Off-On threshold (turn-on)
VOV ON		73.1	-	DC volts	Minimum overvoltage Off-On threshold
VOV OFF		-	92.4	DC Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			603.1	kOhm	Line Sense resistor value (L-pin) - goal seek (VUV OFF) for std 1% resistor series
ENTER DPA-Switch VARIABLES					
DPA-Switch	dpa424				
Chosen Device			Power		
ILIMIT		2.68		Amps	From DPA-Switch datasheet
Frequency - (F)=400kHz, (L)=300kHz	I				Low (L) frequency option - 300kHz
fS		317000	300000	Hertz	From DPA-Switch datasheet
KI	0.66				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITTEXT			1.53	Amps	External current limit. Use 1% resistor to set current limit
RX			10.05	kOhm	Current Limit resistor value (X-pin) - assumes minimum datasheet curve (fig 32)
DUVON GOAL	0.65		0.65		Maximum allowed duty cycle at VUV ON MIN undervoltage threshold
KDI			0.15		Maximum current ripple factor
VDS			1.32	Volts	DPA-Switch average on-state Drain to Source Voltage
VDSOP			174.66	Volts	Required drain voltage for guaranteed transformer reset
DIODE Vf SELECTION					
VDMAIN	0.1		0.1	Volts	Main output diodes forward voltage drop
VDOUT2	0.1		0.1	Volts	Secondary output diodes forward voltage drop
VDB			0.7	Volts	Bias diode forward voltage drop
TRANSFORMER CORE SELECTION					



Core Type	efd20				
Core		EFD20		P/N:	EFD20-3F3-Exxx-xx
Bobbin		EFD20_Bobbin		P/N:	CPHS-EFD20-1S-10P-T
AE			0.31	cm^2	Core Effective Cross Sectional Area
LE			4.7	cm	Core Effective Path Length
AL			1200	NH/T^2	Ungapped Core Effective Inductance
BW			13.5	mm	Bobbin Physical Winding Width
LG MAX			0.002	mm	Maximum actual gap when zero gap specified
D FACTOR			1		Duty cycle factor
L	1.00				Transformer primary layers (split primary recommended)
NMAIN	4		4		Main rounded turns
NS2			2		Vout2 rounded secondary turns (AC stacked winding)
VOU2 ACTUAL			5	Volts	Approximate Output2 voltage of with NS2 = 2 turns (AC stacked secondary)
TRANSFORMER DESIGN PARAMETERS					
NP			23		Primary rounded turns
BM			972.32	Gauss	Max operating flux density at minimum switching frequency
BP			1931.49	Gauss	Max transient flux density at minimum switching frequency
LP MIN			0.60	mHenries	Minimum primary magnetizing inductance (assumes LG MAX=2um)
IMAG			0.11	Amps	Peak magnetizing current at minimum input voltage
OD_P			0.66	mm	Primary wire outer diameter
AWG_P		Warning	22	AWG	!!! Primary < 27AWG: decrease L, increase NP, consider multifilar winding
DUTY CYCLE VALUES					
DUVON MIN			0.65		Duty cycle at minimum undervoltage threshold
DVMIN			0.56		Duty cycle at minimum DC input voltage
DVMAX			0.27		Duty cycle at minimum DC input voltage
DOVOFF MAX			0.21		Duty cycle at maximum DC overvoltage threshold
CURRENT WAVESHAVE PARAMETERS					
IP			1.25	Amps	Maximum peak primary current at maximum DC input voltage
IPRMS			0.85	Amps	Maximum primary RMS current at minimum DC input voltage
COUPLED INDUCTOR OUTPUT PARAMETERS					
LMAIN	10		10	uHenries	Main / Output2 coupled output inductance (referred to Main winding)
WLMAIN			211	uJoules	Main / Output2 coupled output inductor full-load stored energy
KDIMAIN			0.13		Current ripple factor of combined Main and Output2 outputs
nOUT2			1.50		Approximate turns ratio for Output2 winding
nBIAS			3.7		Approximate turns ratio for Bias winding
SECONDARY OUTPUT PARAMETERS					
No derating					
ISMMAINRMSLL			4.13	Amps	Maximum transformer secondary RMS current (AC stacked secondary)
ISOUT2RMSLL			1.50	Amps	Maximum transformer secondary RMS current (AC stacked secondary)



IDAVMAIN			2.57	Amps	Maximum average current, Main rectifier (single device rating)
IDAVOUT2			1.47	Amps	Maximum average current, Main rectifier (single device rating)
IRMSMAIN			0.13	Amps	Maximum RMS current, Main output capacitor
IRMSOUT2			0.07	Amps	Maximum RMS current, Out2 output capacitor
VPIVMAIN			25.27	Volts	Main rectifiers peak-inverse voltage
VPIVOUT2			37.91	Volts	Output2 rectifiers peak-inverse voltage
VPIVB			59.43	Volts	Bias output rectifier peak-inverse voltage



8 Performance Data

All measurements performed at 25°C with the PCB mounted horizontally and natural convection cooling.

8.1 Efficiency

Efficiency was measured as a function of input voltage with each rail loaded to its full power as defined in Table 1.

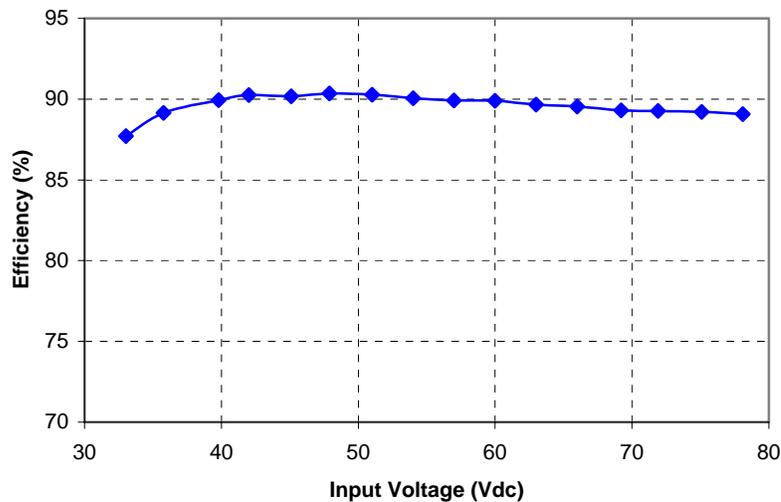


Figure 8 - Efficiency vs. Input Voltage at full power



8.2 Regulation

8.2.1 Line

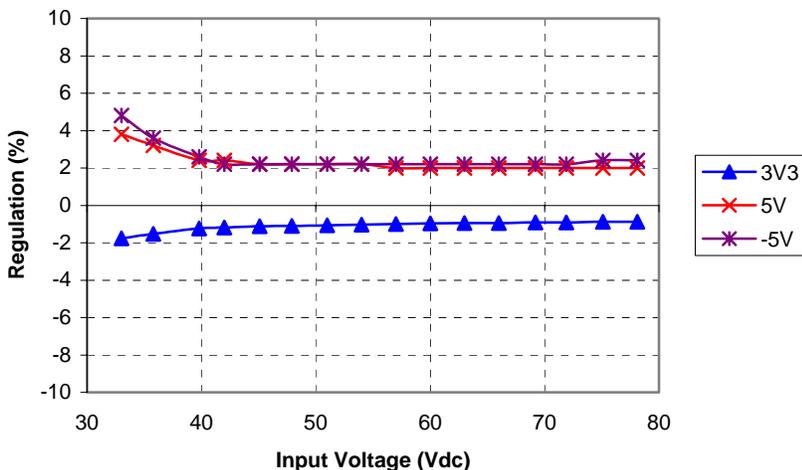


Figure 9 - Line Regulation at Full Load

8.2.2 Cross Regulation

X denotes minimum load current and M denotes maximum load current. Measurements taken with -48V input and minimum loads defined as 15% of maximum load on each rail.

Rail Voltage	3.3	5	-5
Min Current (X)	0.525	0.15	-0.15
Max Current (M)	3.5	1	1

Load Combination			
3V3 - 5V - '-5V'	3V3	5V	-5V
XXX	3.31	5.02	-5.02
XXM	3.31	5.03	-4.91
XXM	3.32	4.97	-5.05
XMM	3.32	4.97	-4.94
MXX	3.24	5.2	-5.23
MXM	3.24	5.2	-5.09
MMX	3.25	5.13	-5.25
MMM	3.25	5.14	-5.13
Minimum Voltage (V)	3.24	4.97	-4.91
Maximum Voltage (V)	3.32	5.2	-5.25
% below Nominal	-1.82	-0.60	-1.80
% Above Nominal	0.61	4.00	5.00

Figure 10 – Cross Regulation with -48V input



9 Thermal Performance

In 25°C local ambient, the temperature of several key power stage components was measured as a function of line voltage at full output power. Figure 11 shows the resulting temperature profile.

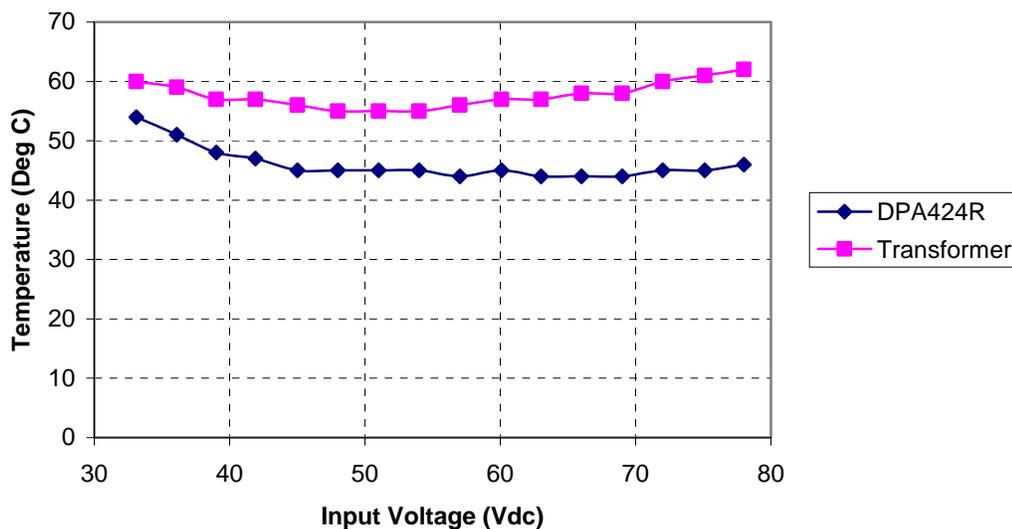


Figure 11 - Full Power Operating Temperatures in 25°C Ambient



10 Waveforms

10.1 Drain Voltage and Current, Normal Operation

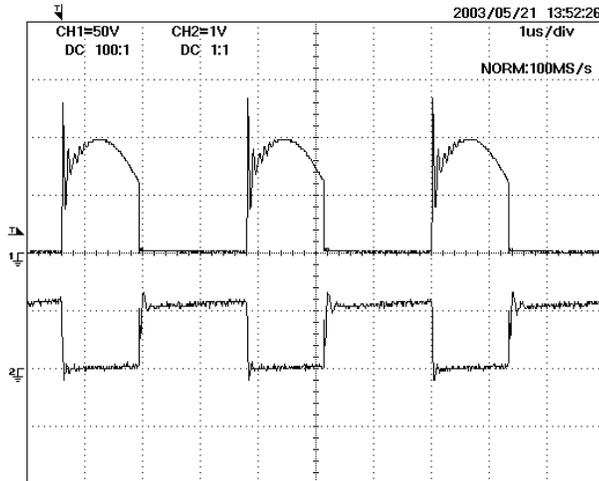


Figure 12 - 36 VDC, Full Load.
 Upper: V_{DS} , 50 V / div
 Lower: I_D , 1 A / div, 2 μ s / div

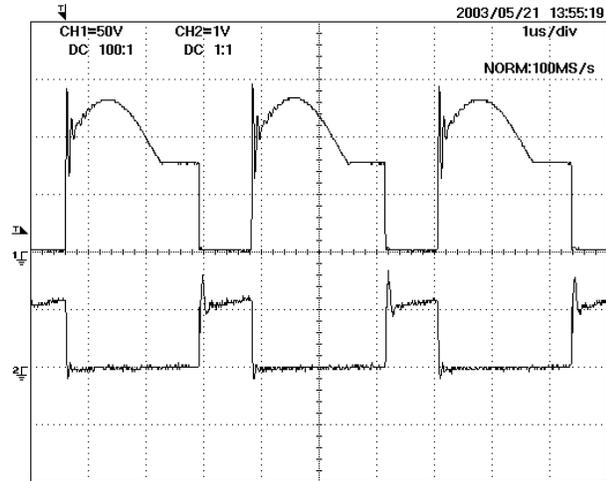


Figure 13 - 75 VDC, Full Load.
 Upper: V_{DS} , 50 V / div
 Lower: I_D , 1 A / div, 2 μ s / div

10.2 Drain Voltage and Current Start-up Profile

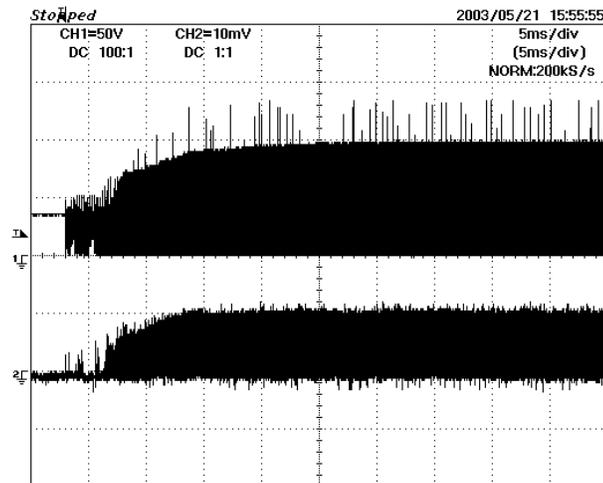


Figure 14 – 36V_{DC} Input and Maximum Load.
 Lower: I_{DRAIN} , 1 A / div.
 Upper: V_{DRAIN} , 50 V & 5 ms / div.

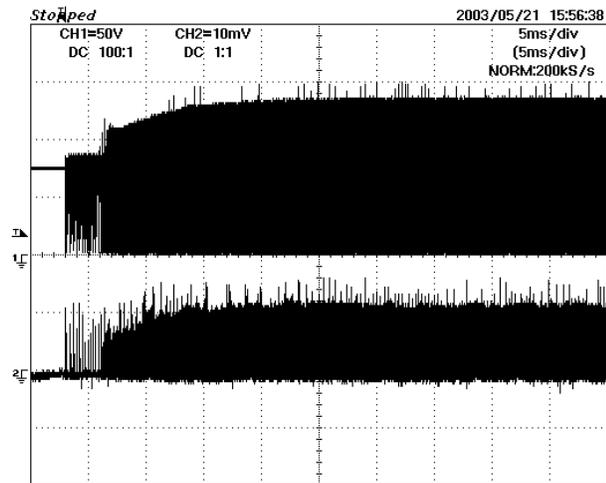


Figure 15 - 75V_{DC} Input and Maximum Load.
 Lower: I_{DRAIN} , 1 A / div.
 Upper: V_{DRAIN} , 50 V & 5 ms / div.



10.3 Output Voltage Start-up Profile

Output voltage start-up was measured using purely resistive loads.

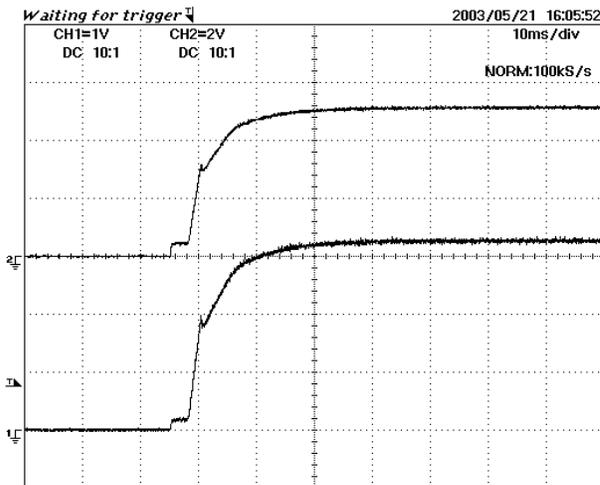


Figure 16 - 36 V_{DC}, Full Load.
Lower: 3V3 Rail 1V / div
Upper: 5V Rail 2V / div, 10ms / div

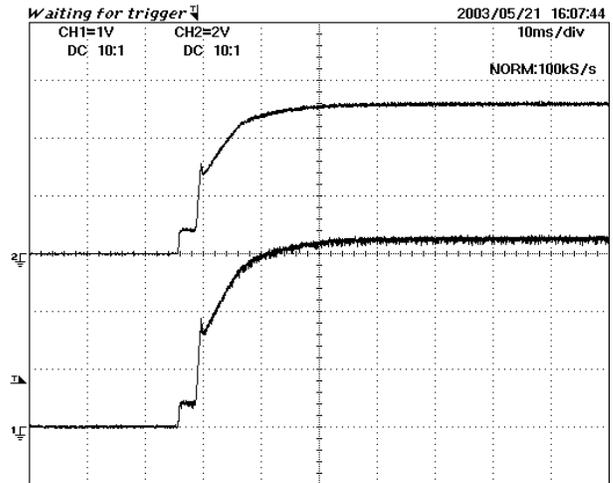


Figure 17 - 75 V_{DC}, Full Load.
Lower: 3V3 Rail 1V / div
Upper: 5V Rail 2V / div, 10ms / div

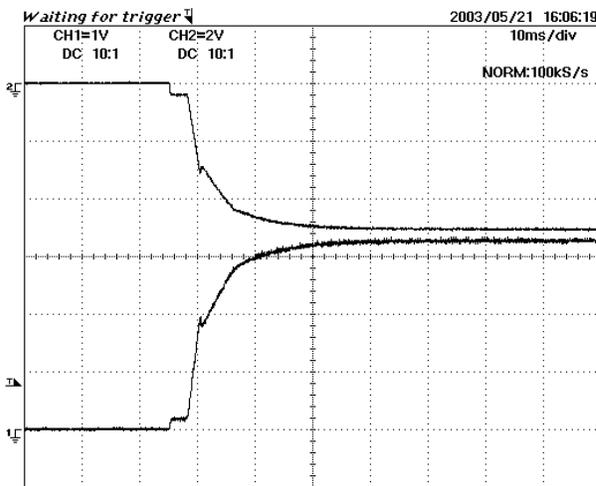


Figure 18 - 36 V_{DC}, Full Load.
Lower: 3V3 Rail 1V / div
Upper: -5 Rail 2V / div, 10ms / div

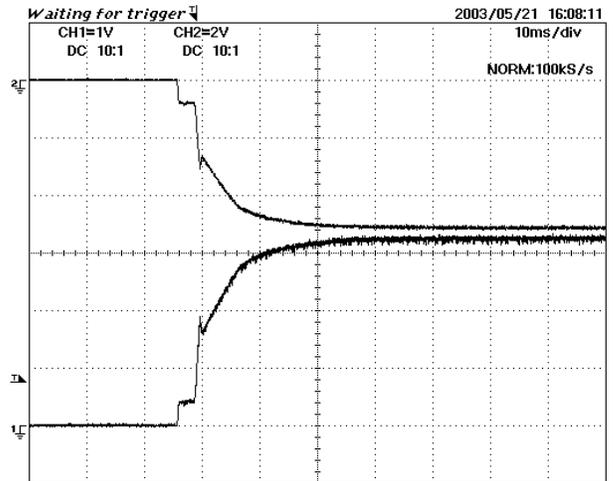


Figure 19 - 75 V_{DC}, Full Load.
Lower: 3V3 Rail 1V / div
Upper: -5 Rail 2V / div, 10ms / div



10.4 Load Transient Response

In order to assess loop stability, step load change was performed on the 3V3 rail. The current on this rail was stepped from 0.5A to 1.5A and back to 0.5A and the rail voltage (AC coupled) measured. The two figures below show an approximate 15mV deviation in output voltage when the rail is subject to this current change at a di/dt of 5kA/s.

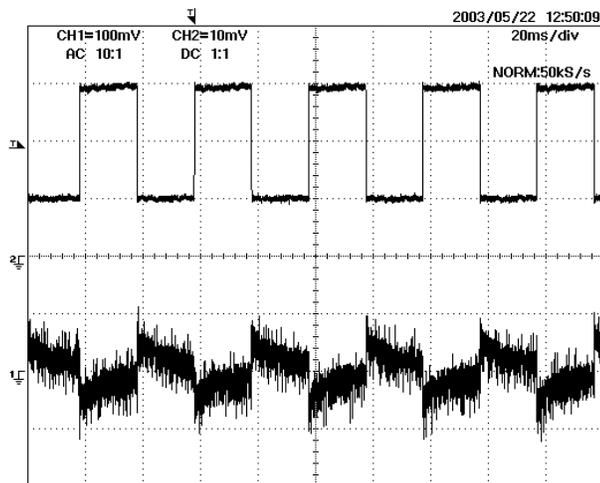


Figure 20 – 3V3 Rail Transient Response, 48 V_{DC}
0.5A – 1A – 0.5A Load Step.
Top: Load Current, 0.5 A/div.
Bottom: Output Voltage (AC coupled)
10 mV / div, 20 ms / div.

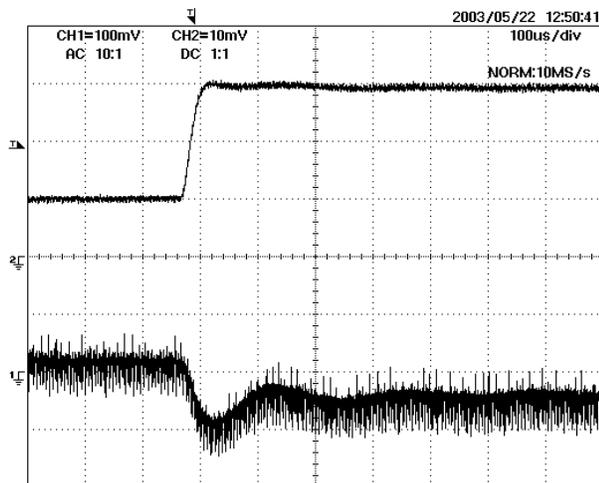


Figure 21 – 3V3 Rail Transient Response, 48 V_{DC}
0.5A – 1A – 0.5A Load Step.
Top: Load Current, 0.5 A/div.
Bottom: Output Voltage (AC coupled)
10 mV / div, 100 μ s / div.

The well damped recovery is a good indication of adequate phase margin in the control loop.



10.5 Output Ripple Measurements

10.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 22 and Figure 23.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu\text{F}/50\text{ V}$ ceramic type and one (1) 1.0 $\mu\text{F}/50\text{ V}$ aluminum electrolytic. **The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).**

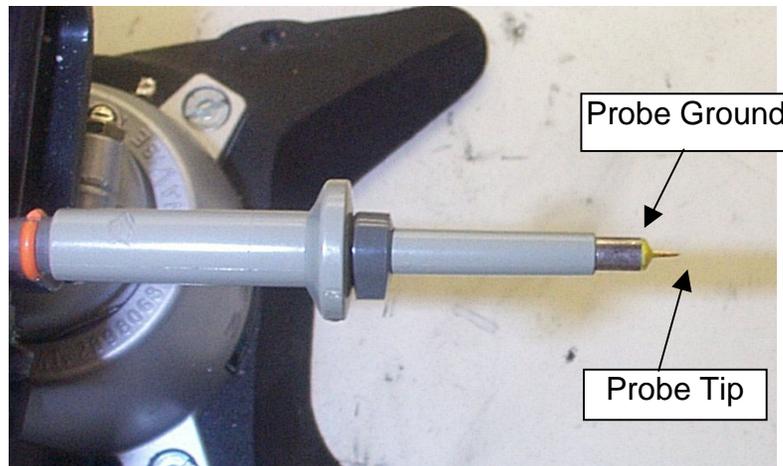


Figure 22 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

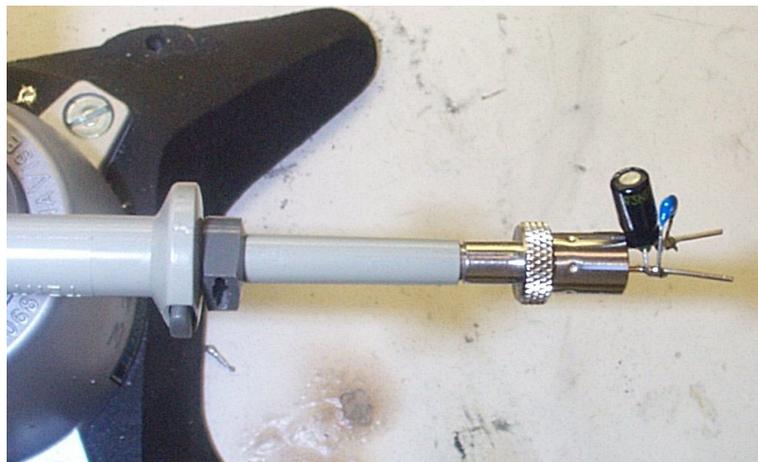


Figure 23 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

10.5.2 Measured Ripple

Ripple was measured using resistive loads.

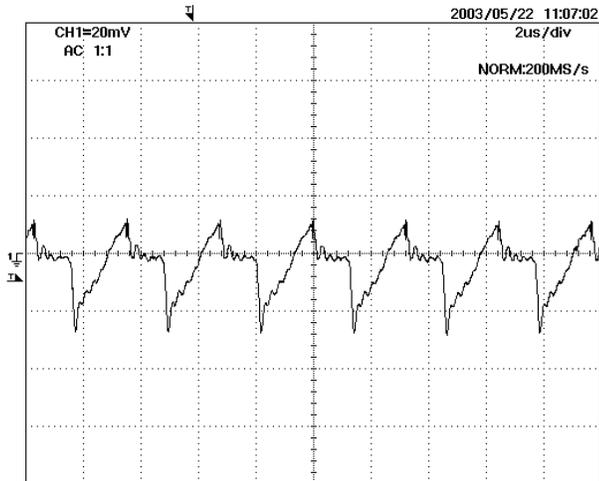


Figure 24 – 3V3 Rail Ripple, 36 V_{DC}, Full Load.
2 us / div, 20 mV / div

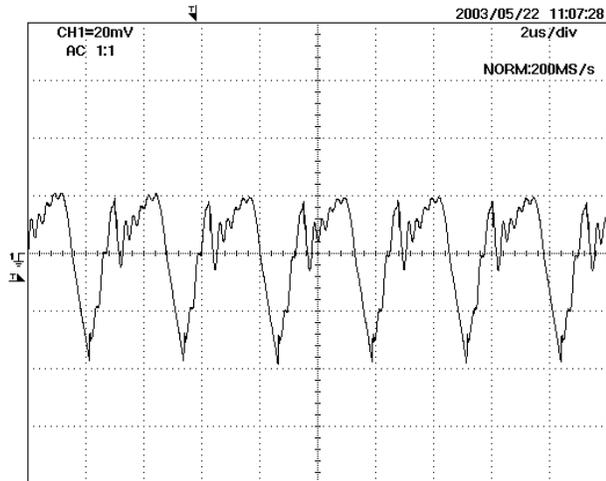


Figure 25 – 3V3 Rail Ripple, 75 V_{DC}, Full Load.
2 us / div, 20 mV / div

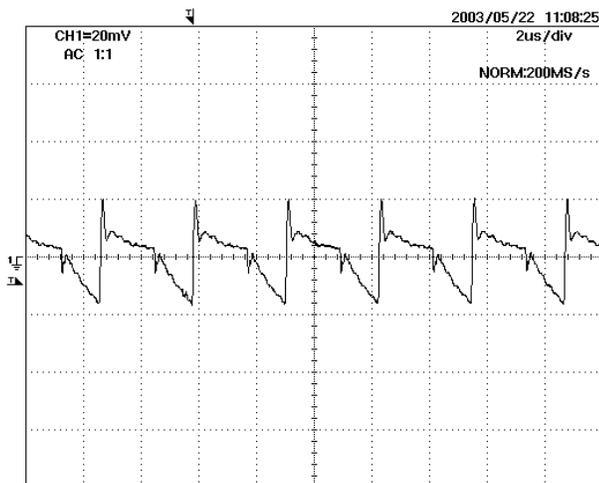


Figure 26 – 5V Rail Ripple, 36 V_{DC}, Full Load.
2 us / div, 20 mV / div

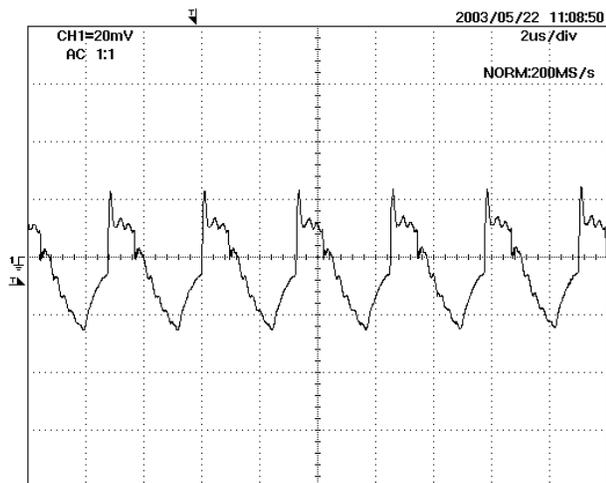


Figure 27 – 5V Rail Ripple, 75 V_{DC}, Full Load.
2 us / div, 20 mV / div



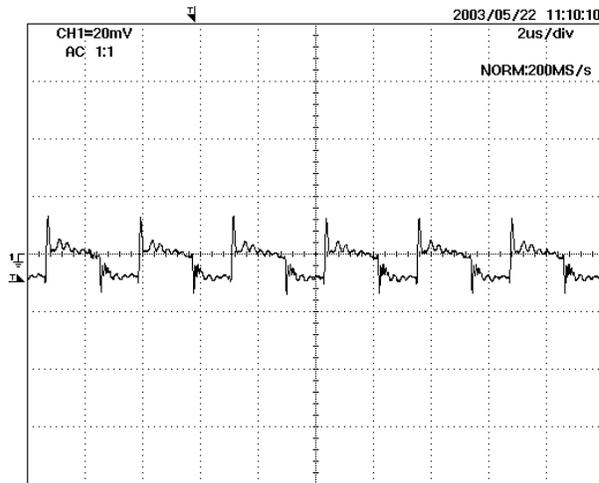


Figure 28 – -5V Rail Ripple, 36 V_{DC}, Full Load.
2 us / div, 20 mV / div

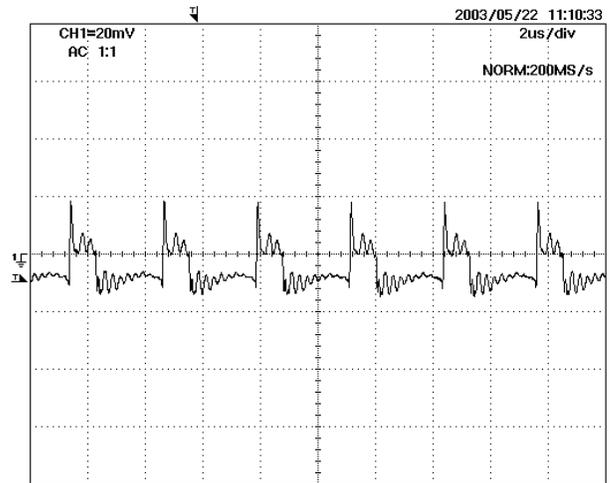


Figure 29 – -5V Rail Ripple, 75 V_{DC}, Full Load.
2 us / div, 20 mV / div



11 Revision History

Date	Author	Revision	Description & changes	Reviewed
March 30, 2004	IM	1.0	Initial release	VC /AM

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**WORLD HEADQUARTERS
NORTH AMERICA - WEST**
Power Integrations, Inc.
5245 Hellyer Avenue
San Jose, CA 95138 USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail:
usasales@powerint.com

CHINA
Power Integrations
International Holdings, Inc.
Rm# 1705, Bao Hua Bldg.
1016 Hua Qiang Bei Lu
Shenzhen Guangdong,
518031
Phone: +86-755-8367-5143
Fax: +86-755-8377-9610
e-mail:
chinasales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

EUROPE & AFRICA
Power Integrations (Europe) Ltd.
Centennial Court
Easthampstead Road
Bracknell
Berkshire RG12 1YQ,
United Kingdom
Phone: +44-1344-462-300
Fax: +44-1344-311-732
e-mail: eurosales@powerint.com

KOREA
Power Integrations
International Holdings, Inc.
Rm# 402, Handuk Building,
649-4 Yeoksam-Dong,
Kangnam-Gu,
Seoul, Korea
Phone: +82-2-568-7520
Fax: +82-2-568-7474
e-mail: koreasales@powerint.com

APPLICATIONS FAX
World Wide +1-408-414-9760

SINGAPORE
Power Integrations, Singapore
51 Goldhill Plaza #16-05
Republic of Singapore,
308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail:
singaporesales@powerint.com

JAPAN
Power Integrations, K.K.
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama
2-Chome,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail:
japansales@powerint.com

TAIWAN
Power Integrations
International Holdings, Inc.
17F-3, No. 510
Chung Hsiao E. Rd.,
Sec. 5,
Taipei, Taiwan 110, R.O.C.
Phone: +886-2-2727-1221
Fax: +886-2-2727-1223
e-mail:
taiwansales@powerint.com
INDIA (Technical Support)
Innovatech
#1, 8th Main Road
Vasanthnagar
Bangalore, India 560052
Phone: +91-80-226-6023
Fax: +91-80-228-9727
e-mail:
indiasales@powerint.com

