Reference Design Report

Title	**10.9 W Dual Output Flyback Power Supply Using INN3624C-H606 – An InnoSwitch™3-EP IC with a 1250 V PowiGaN™ Switch**
Specification	58 VAC – 480 VAC Input; 7 V, 0.3 A and 17.5 V, 0.5 A Outputs 40 VDC Start-up and Operation (8.4 W Output Power)
Application	Industrial Applications
Author	Applications Engineering Department
Document Number	RDR-1066
Date	August 20, 2025
Revision	B

Summary and Features

- Built in synchronous rectification for >85% efficiency at nominal AC input
- FluxLink™ barrier crossing technology means that no optocoupler is required
- Increased reliability and reduced part-count
- All the benefits of secondary side control with the simplicity of primary side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- Meets output cross regulation requirements without linear regulators
- Meets EN550022 and CISPR-22 Class B conducted EMI with ≥ 6db margin
- Very low component count: 57 components

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 7 V, 0.3 A and 17.5 V, 0.5 A dual output power supply using the InnoSwitch™3-EP 1250 V PowiGaN™ (INN3624C-H606) IC. This design demonstrates the efficiency and reduced component count that can be achieved due to the high level of integration of the InnoSwitch™3 IC. Excellent efficiency across load and line is provided by the control algorithm, synchronous rectification and the use of a PowiGaN switch.

This document contains the power supply specification, schematic, bill of materials (BOM), printed circuit board (PCB) layout, transformer specification, and performance data.

Figure 1 – Populated Circuit Board, Top View.

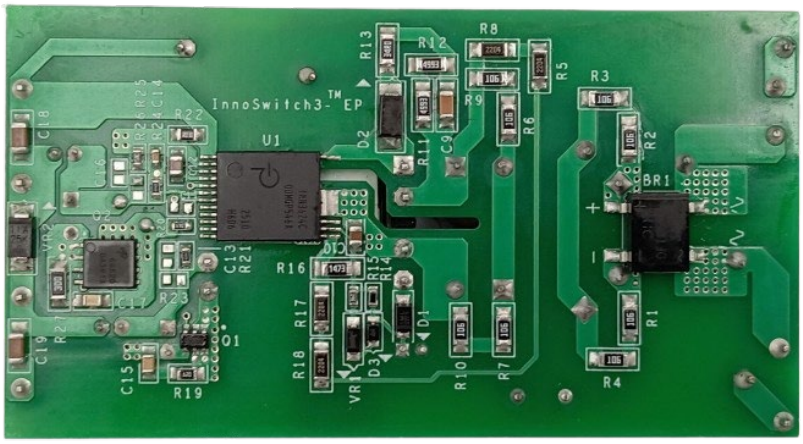


Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min	Nom	Max	Units	Comment
Input						
Voltage	$V_{IN(AC)}$ $V_{IN(DC)}$	58	115/230 40	480	VAC VDC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				<240	mW	Input: 58 VAC – 480 VAC
Output						
Output Voltage 1	V_{OUT1}	17.1	17.5	17.9	V	± 2% @ 58 VAC - 480 VAC ±4% @ 40 VDC input (± 5% with 10% min load on 17.5 V)
Output Ripple Voltage 1	$V_{RIPPLE1}$			171	mV	20 MHz Bandwidth, at 25 °C Ambient
Output Current 1	I_{OUT1}	0		0.5[1]	A	
Output Voltage 2	V_{OUT2}	6.65	7	7.35	V	± 5% @ 58 VAC - 480 VAC ±7% @ 40 VDC input (± 10% with 10% min load on 17.5 V)
Output Ripple Voltage 2	V_{RIPPLE}			79	mV	20 MHz Bandwidth, at 25 °C Ambient
Output Current 2	I_{OUT2}	0		0.3	A	
Total Output Power						
Continuous Output Power at:						
58 VAC – 480 VAC Input	P_{OUT}		10.9		W	
40 VDC Input			8.4			7 V, 0.3 A and 17.5 V, 0.36 A outputs
Efficiency	η		82			Average @ 58 VAC
			84			Average @ 90 VAC
			85			Average @ 115 VAC
			85			Average @ 230 VAC
			84			Average @ 265 VAC
			80			Average @ 480 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				2.5	kV	1.2/50 μs Surge, IEC 61000-4-5, Impedance: 2 Ω Class A
Combination Wave Surge Test				6	kV	
EFT				4	kV	IEC 61000-4-4
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

Table 1 – Power Supply Specifications.

[1] Output current rating for 17.5 V output is derated to 0.36 A at 40 VDC input.

3 Schematic

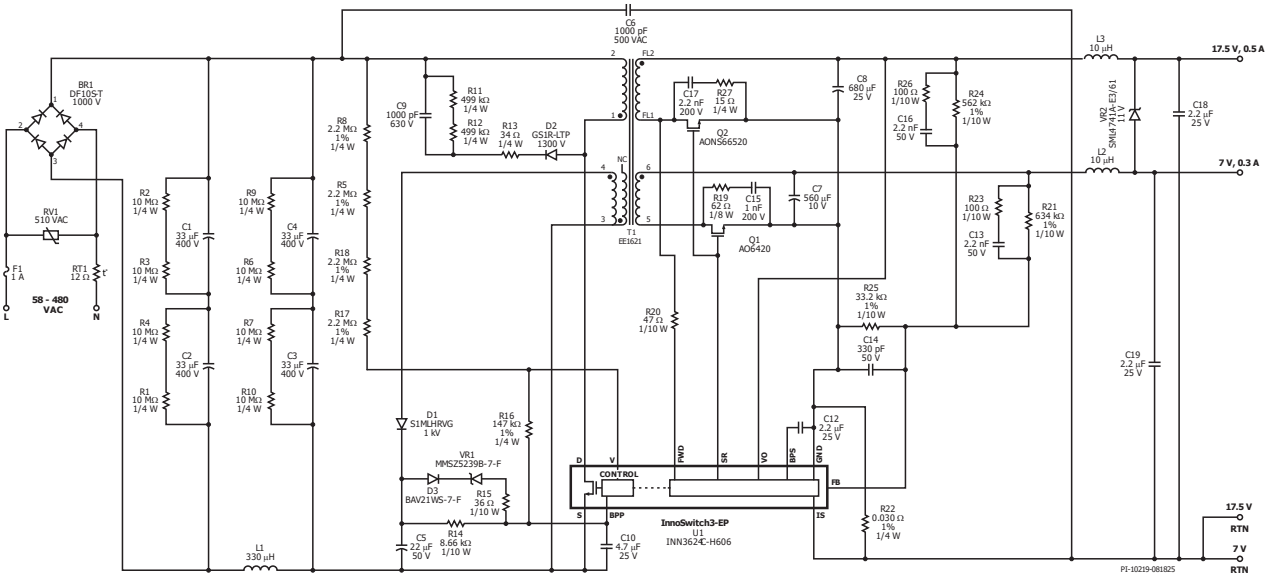


Figure 3 – Schematic.

4 Circuit Description

The InnoSwitch™3 combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates a 1250 V PowiGaN primary switch, primary-side controller, secondary-side controller for synchronous rectification and Fluxlink™ technology that eliminates the optocoupler typically needed for secondary-side control. InnoSwitch™3 also employs quasi-resonant switching to increase efficiency.

4.1 Input EMI Filtering and AC Rectifier Stage

Fuse F1 isolates the circuit and provides protection from component failure while thermistor RT1 reduces inrush current. Varistor RV1 clamps the input voltage to protect the circuit from line surge events. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC to the input filter capacitors C1, C2, C3, and C4. The differential inductance of L1 with capacitors C1, C2, C3, and C4 provide differential noise filtering. Capacitor C6 is used to reduce common mode electromagnetic interference (EMI). Resistors R1, R2, R3, R4, R6, R7, R9, and R10 are used to balance the voltage across the input filter capacitors.

4.2 InnoSwitch3-EP IC Primary

The primary winding for the power transformer is terminated on pins 1 and 2. Pin 2 of the transformer (T1) primary is connected to the rectified DC bus; pin 1 is connected to the drain terminal of the power switch inside the InnoSwitch3-EP IC (U1) via the DRAIN pin. Resistors R5, R8, R16, R17, and R18 provide input voltage sense information which is used to provide over- and undervoltage protection for the wide-range input.

A simple RCD clamp formed by diode D2, resistors R11, R12, R13, and capacitor C9 limits the peak drain voltage of U1 at turn-off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C10) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on transformer T1. Output of the auxiliary (bias) winding is rectified using diode D1 and filtered using capacitor C5. Resistor R14 limits the current being supplied to the BPP pin of the InnoSwitch3-EP IC (U1).

Zener diode VR1 in series with resistor R15 and diode D3 provides primary-sensed output overvoltage protection (OVP). In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage on the output of the converter, the auxiliary winding voltage increases and causes breakdown of Zener diode VR1 which then causes a current to flow into the BPP pin of InnoSwitch3-EP IC U1. If this current increases above the I_{SD} threshold, the InnoSwitch3-EP controller enters auto-restart to protect the power supply and the load from damage.

4.3 InnoSwitch3-EP IC Secondary

The secondary side of the InnoSwitch3-EP 1250 V IC (U1) provides output voltage and output current sensing, and controls the operation of the Synchronous Rectification Field-Effect Transistor (SR FET).

Total output current is sensed by R22 connected between the IS and GND pins via a voltage detection circuit with a low voltage drop (approximately 36 mV) to reduce losses. The current sense has a voltage threshold that is used to trigger short circuit protection. Once the current sense voltage threshold is exceeded for longer than a fixed time (t_{AR}), the device enters auto-restart (AR).

Output rectification for the 7 V output is provided by SR FET Q1. The very low ESR capacitor C7 provides filtering, and inductor L2 along with capacitor C19 form a second-stage filter that significantly attenuates the high frequency ripple and noise on the 7 V output. Output rectification for the 17.5 V output is provided by SR FET Q2. Very low ESR capacitor C8 provides filtering, and Inductor L3 plus capacitor C18 form a filter that significantly attenuates the high frequency ripple and noise on the 17.5 V output.

RC snubber networks comprising R19 and C15 for Q1, along with R27, and C17 for Q2, damp the high frequency ringing across the SR FETs, which results from the resonance between the leakage inductance of the transformer windings and secondary trace inductances interacting with parasitic circuit capacitances.

The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R20 and the FWD pin of the IC. In continuous conduction mode (CCM) operation, the power MOSFET is turned off just prior to the secondary side controller requesting a new switching cycle from the primary. In discontinuous conduction mode (DCM) the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary side ensures that it is never on at the same time as the synchronous rectification MOSFET. The SR-MOSFET drive signal is provided by the SR pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage (FWD) pin or the output voltage. When output voltage powers the device, current is fed into the VO pin and charges the decoupling capacitor C12 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V. The InnoSwitch3-EP IC has an internal reference of 1.265 V for the output voltage feedback signal. Capacitor C14 provides decoupling from high frequency noise to prevent it from affecting power supply operation. Resistor R21, R24, and R25 form a voltage divider network that senses the output voltage from both outputs to improve cross-regulation. Zener diode VR2 further improves the cross regulation when only the 7 V output is loaded, which causes the 17.5 V output operating at the higher end of its specified output voltage range.

5 PCB Layout

PCB copper thickness is 2.0 oz.
PCB Material Thickness is 1.6 mm.
PCB Material is FR4.

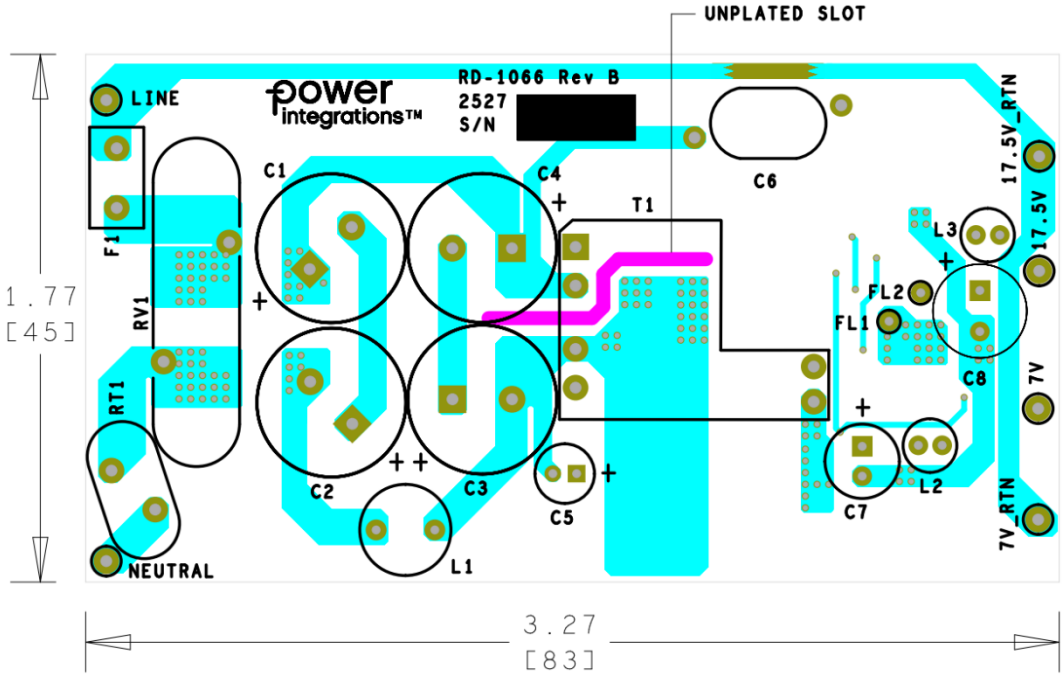


Figure 4 – Printed Circuit Layout, Top.

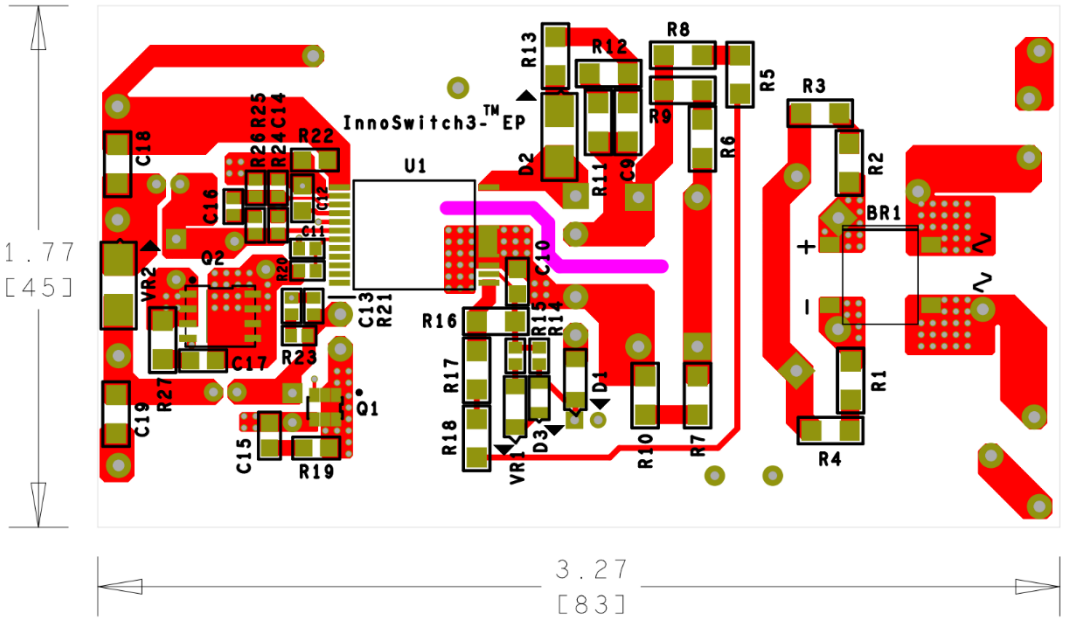


Figure 5 – Printed Circuit Layout, Bottom[2].

[2] C11 – Unused and should be unpopulated in the assembly

6 Bill of Materials

6.1 Bill of Material: Electrical Components

Item	Qty.	Ref Des.	Description	Mfr. Part Number	Manufacturer
1	1	BR1	Bridge Rectifier, Single Phase, Standard, 1 kV, Surface Mount, DF-S, 4-SMD, Gull Wing	DF10S-T	Diodes Incorporated
2	4	C1 C2 C3 C4	33 µF, 400 V, Electrolytic, (12.5 x 20)	KMG401ELL330MK20S	Nippon Chemi-Con
3	1	C5	22 µF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
4	1	C6	1 nF, 500 VAC, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay BC Components
5	1	C7	560 µF, 10 V, Aluminum - Polymer Capacitors, Radial, Can 12 mOhm 2000 Hrs @ 105 °C, (6.3 x 12)	A750EQ567M1AAAE012	KEMET
6	1	C8	680 µF, ±20%, 25 V, Aluminum - Polymer Capacitors Radial, Can 16 mOhm 2000 Hrs @ 105 °C (8 mm x 16 mm)	A750KW687M1EAAE016	KEMET
7	1	C9	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
8	1	C10	4.7 µF, ±10%, 25 V, Ceramic, X7R, -55 °C ~ 125 °C, 0805 (2012 Metric)	TMK212AB7475KG-T	Taiyo Yuden
9	1	C12	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M125AB	TDK Corp
10	2	C13 C16	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
11	1	C14	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
12	1	C15	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX Corp
13	1	C17	2200 pF, ±10%, 200 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	08052C222K4T2A	AVX Corp
14	2	C18 C19	2.2 µF, 25 V, Ceramic, X7R, 1206	TMK316B7225KL-T	Taiyo Yuden
15	1	D1	Diode, Standard, 1000 V, 1 A, Surface Mount, Sub SMA	S1MLHRVG	TAIWAN SEMICONDUCTOR
16	1	D2	Diode, Standard, 1300 V, 1 A, Surface Mount DO-214AC (SMA)	GS1R-LTP	Micro Commercial Co
17	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diode Inc.
18	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
19	2	FL1 FL2	Flying Lead, Hole size 30 mils	N/A	N/A
20	1	L1	330 µH, 0.55 A, 9 x 11.5 mm	SBC3-331-551	Tokin
21	2	L2 L3	Inductor, 10 µH, Unshielded, Wirewound, 950 mA, 140 mOhm Max, Radial	11R103C	Murata Power Solutions Inc
22	1	Q1	MOSFET, N-CH, 60 V, 4.2 A, 6TSOP	AO6420	Alpha & Omega Semiconductor Inc
23	1	Q2	MOSFET, N-Channel, 150 V 17 A (Ta), 100 A (Tc) 6.2 W (Ta), 215W (Tc) Surface Mount 8-DFN (5 x 6) N-Channel 150 V 17 A (Ta), 100A (Tc) 6.2 W (Ta), 215 W (Tc) Surface Mount 8-DFN (5 x 6)	AONS66520	Alpha & Omega Semiconductor
24	8	R1 R2 R3 R4 R6 R7 R9 R10	RES, 10 M, 5%, 1/4 W, Thick Film, 1206	RC1206FR-0710ML	YAGEO

25	4	R5 R8 R17 R18	RES, 2.2 M, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF2204	Rohm Semi
26	2	R11 R12	RES, 499 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4993V	Panasonic
27	1	R13	RES, 34 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF34R0V	Panasonic
28	1	R14	RES, 8.66 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF8661V	Panasonic
29	1	R15	RES, 36 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ360V	Panasonic
30	1	R16	RES, 147 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1473V	Panasonic
31	1	R19	RES, 62 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ620V	Panasonic
32	1	R20	RES, 47 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
33	1	R21	RES, 634 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF6343V	Panasonic
34	1	R22	RES, 30 mOhms, ±1%, ±200 ppm/°C, 0.25 W, 1/4W, Chip Resistor, 0805 (2012 Metric) Current Sense Thick Film	CSR0805FK30L0	Stackpole Electronics Inc
35	2	R23 R26	RES, 100 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
36	1	R24	RES, 562 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5623V	Panasonic
37	1	R25	RES, 33.2 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3322V	Panasonic
38	1	R27	RES, 15 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF15R0V	Panasonic
39	1	RT1	Inrush Current Limiter, 12 Ohms, ±20%, 3 A, 0.472" (12.00 mm)	ICL121D11MIB	Eaton - Electronics Division
40	1	RV1	510 VAC, 10 kA, 365 J, disc 20 mm, RADIAL	V20E510P	Littlefuse
41	1	T1	Bobbin, EE1621, Vertical, 8 pins, 4pri, 4sec	EE-1621	Shen Zhen Xin Yu Jia Tech
42	1	U1	INN3624C-H606, INNO3 Switch Integrated Circuit, InnoSwitch-3EP_1250V, InSOP24D	INN3624C-H606	Power Integrations
43	1	VR1	DIODE ZENER 9.1 V 500 MW SOD123	MMSZ5239B-7-F	Diodes, Inc
44	1	VR2	DIODE ZENER 11 V 1 W DO214AC	SML4741A-E3/61	Vishay General Semiconductor - Diodes Division

Table 2 – Electrical Bill of Materials.

6.2 Bill of Material: Mechanical Components

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	1	17.5 V	Test Point, Yellow, Miniature THRU-HOLE MOUNT	5004	Keystone
2	1	17.5 V_RTN	Test Point, Black, Miniature THRU-HOLE MOUNT	5001	Keystone
3	2	7 V, NEUTRAL	Test Point, Red, Miniature THRU-HOLE MOUNT	5000	Keystone
4	2	7 V_RTN, LINE	Test Point, White, Miniature THRU-HOLE MOUNT	5002	Keystone

Table 3 – Mechanical Bill of Materials.

7 Transformer (T1) Specification

7.1 Electrical Diagram

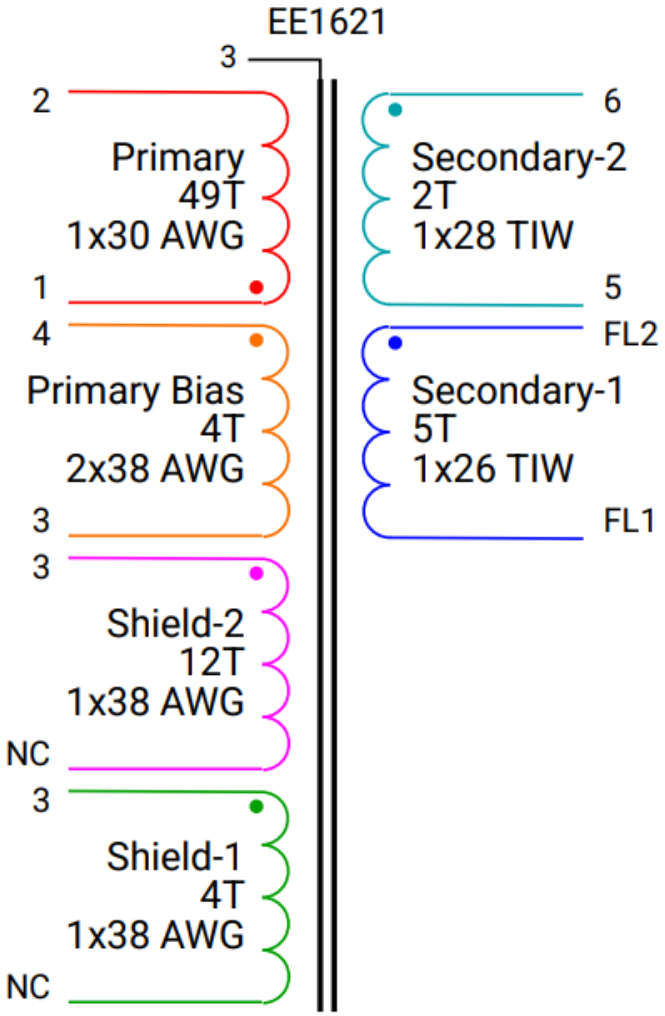


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, typical switching frequency, between pin 2 to pin 1, with all other windings open	553 µH ±5.0%
Electrical Strength	60 Hz 1 second, from pins 1, 2, 3, 4 to pins 5, 6, FL1, FL2	3000 VAC
Primary Leakage Inductance	Measured between pin 2 to pin 1, with all other windings shorted	22 µH (Max).

Table 4 – Transformer Electrical Specifications.

7.3 List of Materials

Item	Description
[1]	Core: EE1621, PC47, gapped for ALG of 239 nH/T^2.
[2]	Bobbin: EE1621.
[3]	Magnet Wire: #30 AWG, double coated.
[4]	Magnet Wire: #38 AWG, double coated.
[5]	Magnet Wire: #26 AWG, Triple Insulated Wire (TIW).
[6]	Magnet Wire: #28 AWG, Triple Insulated Wire (TIW).
[7]	Barrier Tape: 3M 1298 Polyester Film, 1 mil thickness, 5.6 mm width.
[8]	Copper Foil: 2 mil thick, 15 mm x 5 mm.
[9]	Bus wire: #28 AWG, Alpha wire, tinned copper.
[10]	Varnish: Dolph BC-359.

Table 5 – Transformer Materials List.

7.4 Transformer Build Diagram

Secondary-2: **2T** – 1 x #28 **TIW**
Secondary-1: **5T** – 1 x #26 **TIW**
Shield-2: **12T** – 1 x #38 **AWG**
Shield-1: **4T** – 1 x #38 **AWG**
Primary Bias: **4T** – 2 x #38 **AWG**
Primary: **49T** – 1 x #30 **AWG**

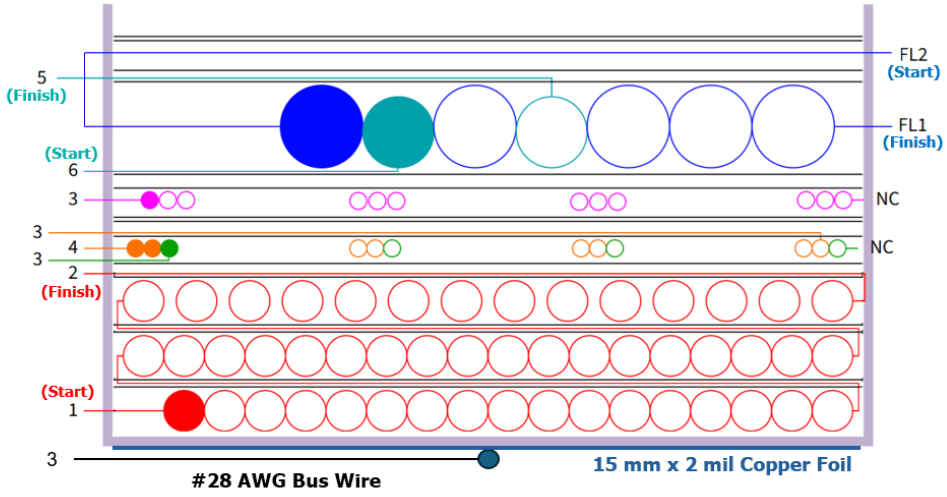
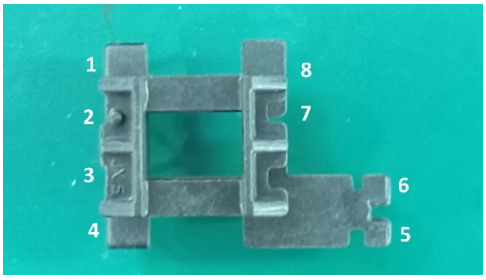


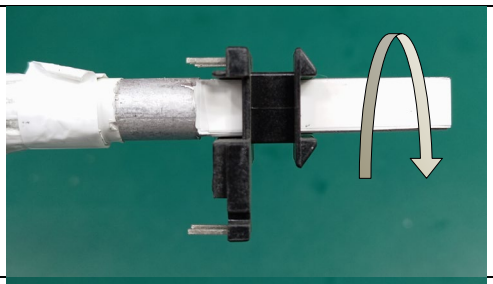
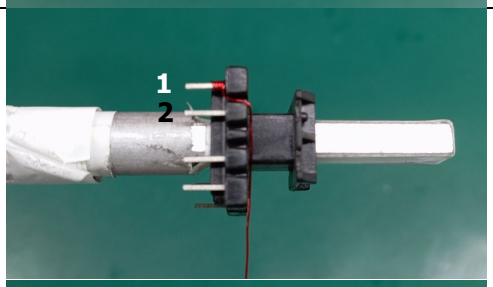
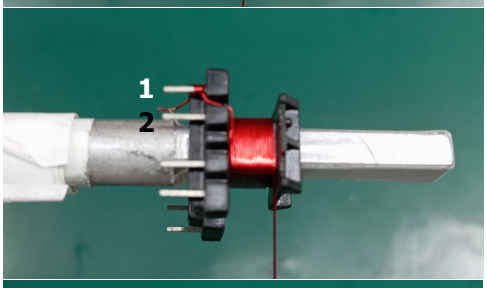
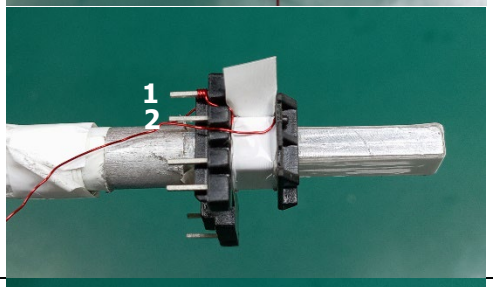
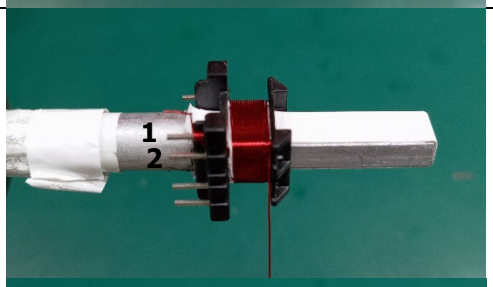
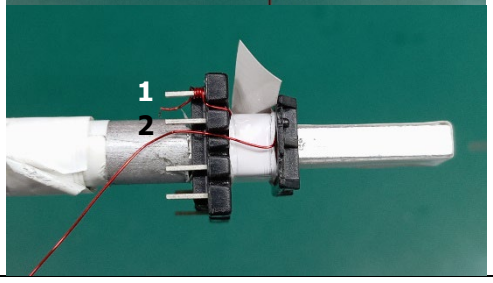
Figure 7 – Transformer Build Diagram.

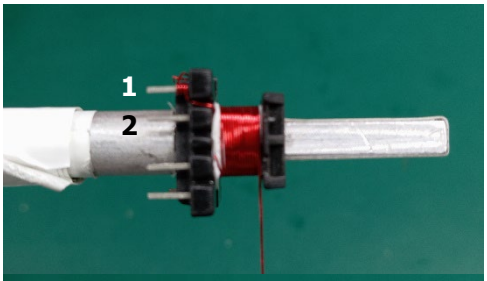
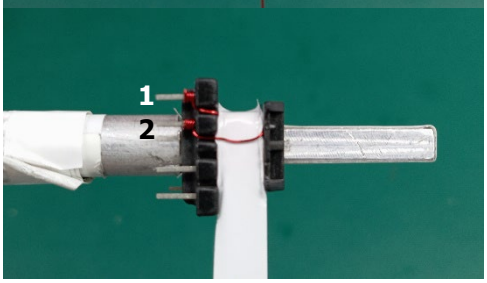
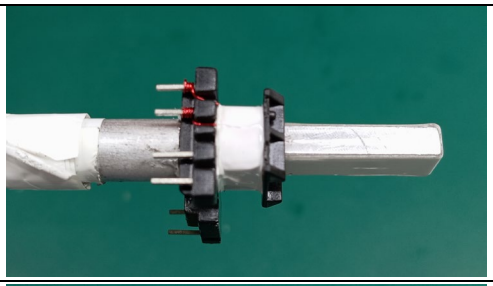
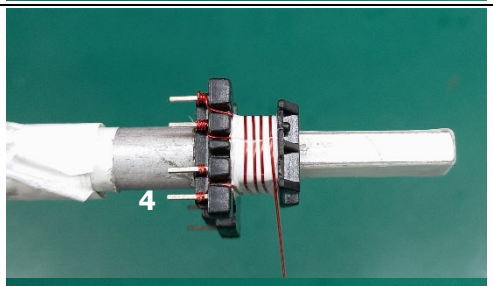
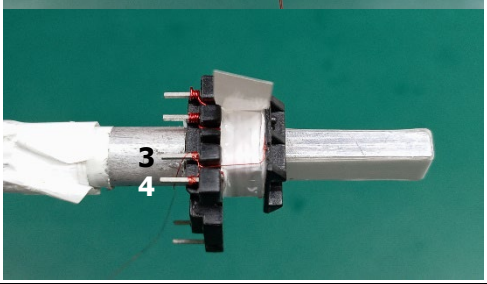
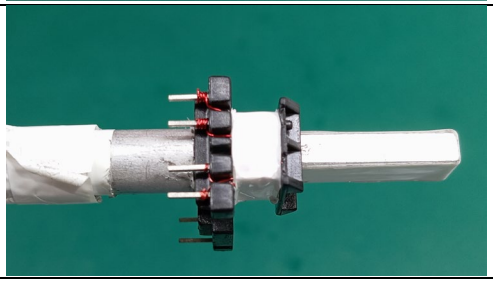
7.5 Winding Instructions

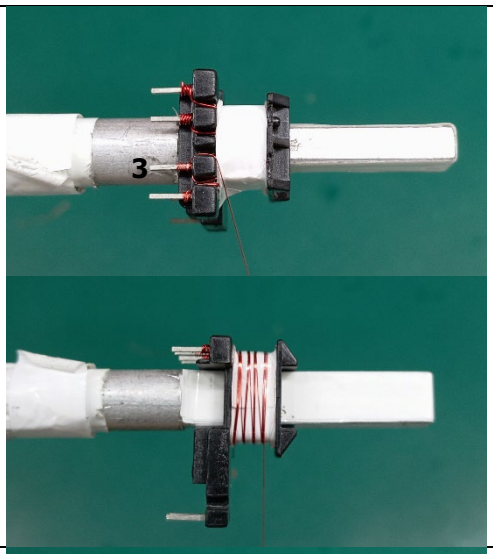
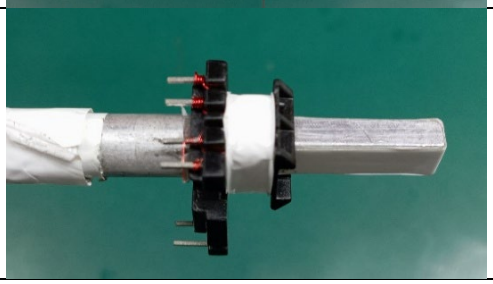
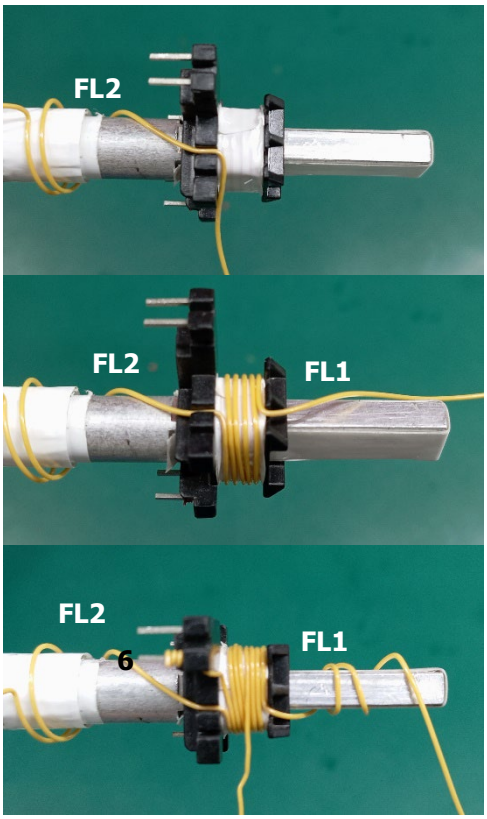
Primary	Start at pin 1, wind 17 turns of wire Item [3] from left to right and bring it back to the left and add 2 layers of tape Item [7] for insulation. Continue to wind 18 turns on the second layer using the same wire from left to right and bring it back to the left and add 2 layers of tape Item [7] for insulation. Continue to wind 14 turns on the third layer using the same wire from left to right, add 1 layer of tape, Item [7], and bring the wire back to the left and terminate the wire on pin 2.
Insulation	Add 1 layer of tape, Item [7], on the top.
Sheild-1, Primary Bias	Start with Shield-1 using Item [4] (x2 leads) from Pin 4, together with Primary Bias Item [4] (x1 lead) from Pin 3. Wind 4 turns from left to right. Spread the winding evenly across the entire bobbin. For Primary Bias, add 1 layer of tape, Item [7], between the exit lead and winding and finish this winding on Pin 3. For Shield-1, leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.
Insulation	Add 2 layers of tape, Item [7], on the top.
Shield-2	Start with 1 lead of Item [4] from Pin 3, and wind 12 turns in clockwise direction in total of 1 layer. Wind one layer from left to right. Wind the turns in groups of 3 and space the groups evenly. Leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.
Insulation	Add 2 layers of tape, Item [7], on the top.
Secondary-1, Secondary-2	Start with Secondary-1 winding, wind 5 turns using Item [5] for flying lead FL2 from left to right. For the Secondary-2 winding, wind 2 turns using Item [6] on pin 6 from the left to the right, interleaving with the first 2 turns of Secondary-1 winding. Before terminating the Secondary-1 and Secondary-2 winding, add 1 layer of tape, Item [7]. Terminate Secondary-2 winding on pin 5, and bend FL1 wire to terminate to the right (top of bobbin).
Insulation	Add 2 layers of tape, Item [7], on the top.
Finish	Cut short FL1 to ~22.0 mm and FL2 to ~19.0 mm. Gap the core halves to get 553 μH. Prepare copper foil Item [8], solder wire Item [9] at the middle to connect to pin 3, and then place on top core halves. Then secure 2 core halves with 2 layers of tape Item [7]. Remove pins: 7 and 8. Varnish with Item [10].

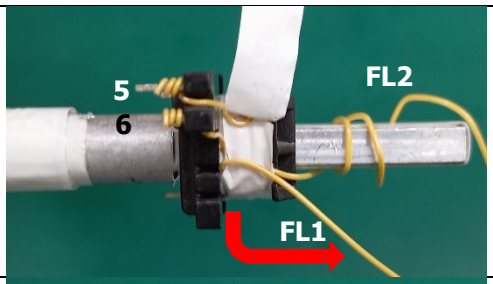
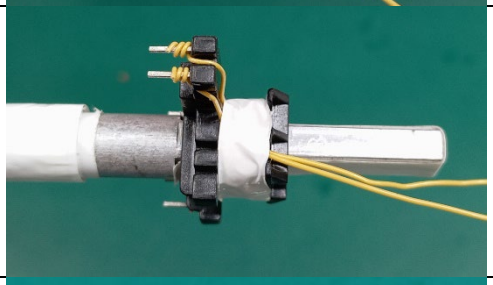
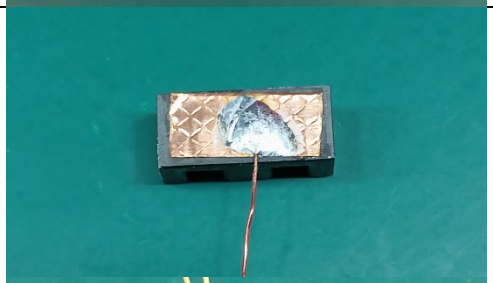
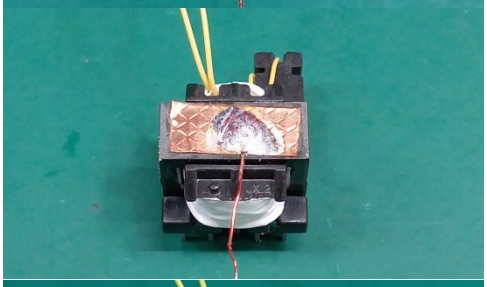
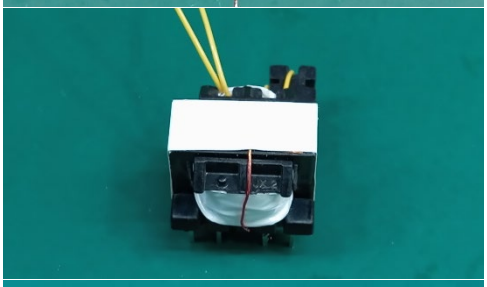
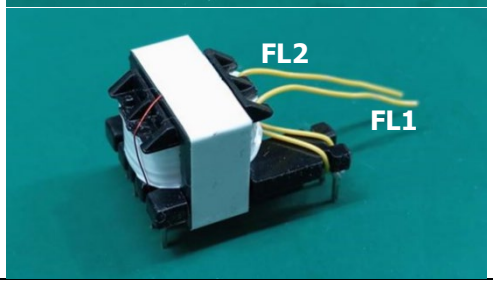
7.6 Winding Illustrations

Winding Preparation		Bobbin pin numbering is as shown in the image on the left.

		For the purpose of these instructions, bobbin Item [2] is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
Primary (1st Layer)	  	Start at pin 1, wind 17 turns of wire Item [3] from left to right and bring it back to the left and add 2 layers of tape Item [7] for insulation.
Primary (2nd Layer)	 	Continue to wind 18 turns on the second layer using the same wire from left to right and bring it back to the left and add 2 layers of tape Item [7] for insulation.

Primary (3rd Layer)	 	Continue to wind 14 turns on the third layer using the same wire from left to right, add 1 layer of tape, Item [7], and bring the wire back to the left and terminate the wire on pin 2.
Insulation		Add 1 layer of tape, Item [7], on the top.
Primary Bias & Shield-1	 	Start with Shield-1 using Item [4] (x2 leads) from Pin 4, together with Primary Bias Item [4] (x1 lead) from Pin 3. Wind 4 turns from left to right. Spread the winding evenly across the entire bobbin. For Primary Bias, add 1 layer of tape, Item [7], between the exit lead and winding and finish this winding on Pin 3. For Shield-1, leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.
Insulation		Add 2 layers of tape, Item [7], on the top.

Shield-2		Start with 1 lead of Item [4] from Pin 3, and wind 12 turns in clockwise direction in total of 1 layer. Wind one layer from left to right. Wind the turns in groups of 3 and space the groups evenly. Leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.
Insulation		Add 2 layers of tape, Item [7], on the top.
Secondary-1 and Secondary-2		Start with Secondary-1 winding, wind 5 turns using Item [5] for flying lead FL2 from left to right. For the Secondary-2 winding, wind 2 turns using Item [6] on pin 6 from the left to the right, interleaving with the first 2 turns of Secondary-1 winding.

		Before terminating the Secondary-1 and Secondary-2 winding, add 1 layer of tape, Item [7]. Terminate Secondary-2 winding on pin 5, and bend FL1 wire to terminate to the right (top of bobbin).
Insulation		Add 2 layers of tape, Item [7], on the top.
Finish	   	Cut short FL1 to ~22.0 mm, and FL2 to ~19.0 mm. Gap the core halves to get 553 µH. Prepare copper foil Item [8], solder wire Item [9] at the middle to connect to pin 3, and then place on top core halves. Then, secure 2 core halves with 2 layers of tape Item [7]. Remove pins: 7 and 8. Varnish with Item [10].

8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-EP1250V_Flyback_050625; Rev.1.2; Copyright Power Integrations 2025	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-EP 1250V Flyback Design Spreadsheet
2	APPLICATION VARIABLES					Design Title
3	VIN_MIN	58		58	V	Minimum AC input voltage
4	VIN_MAX	480		480	V	Maximum AC input voltage
5	VIN_RANGE			CUSTOM		Range of AC input voltage
6	LINEFREQ	60		60	Hz	AC Input voltage frequency
7	CAP_INPUT	33.0		33.0	µF	Input capacitor
8	VOUT	17.50		17.50	V	Output voltage at the board
9	PERCENT_CDC			0		Cable drop compensation desired at full load
10	IOUT	0.620		0.620	A	Output current
11	POUT			10.85	W	Output power
12	EFFICIENCY	0.83		0.85		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE			OPEN FRAME		Power supply enclosure
15						
18	PRIMARY CONTROLLER SELECTION					
19	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
20	DEVICE_GENERIC	INN3624C		INN3624C		Generic device code
21	DEVICE_CODE			INN3624C		Actual device code
22	POUT_MAX			20	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			4.50	Ω	Primary switch on time drain resistance at 100 °C
24	ILIMIT_MIN			0.884	A	Minimum current limit of the primary switch
25	ILIMIT_TYP			0.950	A	Typical current limit of the primary switch
26	ILIMIT_MAX			1.017	A	Maximum current limit of the primary switch
27	VDRAIN_BREAKDOWN			1250	V	Device breakdown voltage
28	VDRAIN_ON_PRSW			1.17	V	Primary switch on time drain voltage
29	VDRAIN_OFF_PRSW			872.4	V	Peak drain voltage on the primary switch during turn-off
30						
33	WORST CASE ELECTRICAL PARAMETERS					
34	FSWITCHING_MAX	65173		65173	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	170.0		170.0	V	Secondary voltage reflected to the primary when the primary switch turns off
36	VMIN			45.32	V	Valley of the minimum input AC voltage at full load
37	KP			1.99		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			DCM		Mode of operation
39	DUTYCYCLE			0.659		Primary switch duty cycle
40	TIME_ON_MIN			0.654	µs	Minimum primary switch on-time
41	TIME_ON			12.08	µs	Primary switch on-time
42	TIME_OFF			5.35	µs	Primary switch off-time

43	LPRIMARY_MIN			525.4	µH	Minimum primary inductance
44	LPRIMARY_TYP			553.0	µH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			580.7	µH	Maximum primary inductance
47						
48	PRIMARY CURRENT					
49	IPEAK_PRIMARY			0.930	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.273	A	Primary switch average current
52	IRIPPLE_PRIMARY			0.930	A	Primary switch ripple current
53	IRMS_PRIMARY			0.412	A	Primary switch RMS current
54						
55	SECONDARY CURRENT					
56	IPEAK_SECONDARY			9.118	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
58	IRMS_SECONDARY			2.054	A	Secondary winding RMS current
59						
62	TRANSFORMER CONSTRUCTION PARAMETERS					
63	CORE SELECTION					
64	CORE	EE16		EE16		Core selection
65	CORE CODE	EE1621	Info	EE1621		Either custom core code is not entered or a standard core code has been overwritten
66	AE	32.50		32.50	mm^2	Core cross sectional area
67	LE	39.30		39.30	mm	Core magnetic path length
68	AL	2800		2800	nH/turns^2	Ungapped core effective inductance
69	VE	980.0		980.0	mm^3	Core volume
70	BOBBIN	EE1621		EE1621		Bobbin
71	AW	12.33		12.33	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
72	BW	5.40		5.40	mm	Bobbin width
73	BH	2.28		2.28	mm	Bobbin height
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75						
76	PRIMARY WINDING					
77	NPRIMARY			49		Primary turns
78	BPEAK			3794	Gauss	Peak flux density
79	BMAX			3344	Gauss	Maximum flux density
80	BAC			1672	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			230	nH/turns^2	Typical gapped core effective inductance
82	LG			0.163	mm	Core gap length
88						
89	SECONDARY WINDING					
90	NSECONDARY			5		Secondary turns
95						
96	BIAS WINDING					
97	NBIAS			4		Bias turns
98						
101	PRIMARY COMPONENTS SELECTION					
102	LINE UNDERVOLTAGE					
103	BROWN-IN REQURED			28.0	V	Required AC RMS line voltage brown-in threshold

104	RLS			8.43	MΩ	Connect two 4.02 MΩ resistors to the V-pin for the required UV/OV threshold
105	BROWN-IN ACTUAL			1.0 - 27.1	V	Actual AC RMS brown-in range
106	BROWN-OUT ACTUAL			1.0 - 10.9	V	Actual AC RMS brown-out range
107						
108	LINE OVERVOLTAGE					
109	OV_TARGET			482.4	V	AC RMS line voltage at which overvoltage will trigger. For High Line designs, brown-in threshold might need to be lowered to get the required overvoltage
110	RV_BIAS_ENABLED	AUTO		YES		Resistor between BPP and V pins to increase Line OV threshold without increasing Line UV
111	RV_BIAS			158	kΩ	Biasing resistor between BPP and V pins of the device
112	OVERVOLTAGE_LINE		Warning	490 - 594	V	The device voltage stress will be 1004 V when overvoltage is triggered. It is recommended to keep the stress below 1000 V
113						
114	BIAS DIODE					
115	VBIAS			12.0	V	Rectified bias voltage
116	VF_BIAS			0.70	V	Bias winding diode forward drop
117	VREVERSE_BIASDIODE			75.02	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
118	CBIAS			22	µF	Bias winding rectification capacitor
119	CBPP			4.70	µF	BPP pin capacitor
120						
123	SECONDARY COMPONENTS					
124	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
125	RFB_LOWER			7.87	kΩ	Lower feedback resistor
126	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
127						
130	MULTIPLE OUTPUT PARAMETERS					
131	OUTPUT 1					
132	VOUT1			17.50	V	Output 1 voltage
133	IOUT1	0.50		0.50	A	Output 1 current
134	POUT1			8.75	W	Output 1 power
135	IRMS_SECONDARY1			1.657	A	Root mean squared value of the secondary current for output 1
136	IRIPPLE_CAP_OUTPUT1			1.579	A	Current ripple on the secondary waveform for output 1
141	NSECONDARY1			5		Number of turns for output 1
142	VREVERSE_RECTIFIER1			86.62	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
143	SRFET1	AUTO		AON7254		Secondary rectifier (Logic MOSFET) for output 1
144	VF_SRFET1			0.033	V	SRFET on-time drain voltage for output 1
145	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
146	RDSON_SRFET1			66.0	mΩ	SRFET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1
147						
148	OUTPUT 2					
149	VOUT2	7.00		7.00	V	Output 2 voltage
150	IOUT2	0.300		0.300	A	Output 2 current

151	POUT2			2.10	W	Output 2 power
152	IRMS_SECONDARY2			0.994	A	Root mean squared value of the secondary current for output 2
153	IRIPPLE_CAP_OUTPUT2			0.948	A	Current ripple on the secondary waveform for output 2
158	NSECONDARY2			2		Number of turns for output 2
159	VREVERSE_RECTIFIER2			34.65	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
160	SRFET2	AUTO		Si4436DY		Secondary rectifier (Logic MOSFET) for output 2
161	VF_SRFET2			0.013	V	SRFET on-time drain voltage for output 2
162	VBREAKDOWN_SRFET2			60	V	SRFET breakdown voltage for output 2
163	RDSON_SRFET2			43.0	mΩ	SRFET on-time drain resistance at 25 °C and VGS = 4.4 V for output 2
182	PO_TOTAL			10.85	W	Total power of all outputs
183	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Table 6 – Transformer Design Spreadsheet.[3]

[3] The warnings on the spreadsheet have been verified to not be an issue for this design.
For line 112 (OVERVOLTAGE_LINE), the InnoSwitch3-EP INN3624C employs a 1250 V rated primary switch.

9 Performance Data

All the performance data was measured on the board unless otherwise noted.

9.1 Full-load Efficiency vs. Line

Input Voltage (VDC)	Derated Output Load	Efficiency (%)
40	7 V/0.3 A, 17.5 V/0.36 A	79.9

Table 7 – Derated Load Efficiency vs. Input Line Voltage (40 VDC).

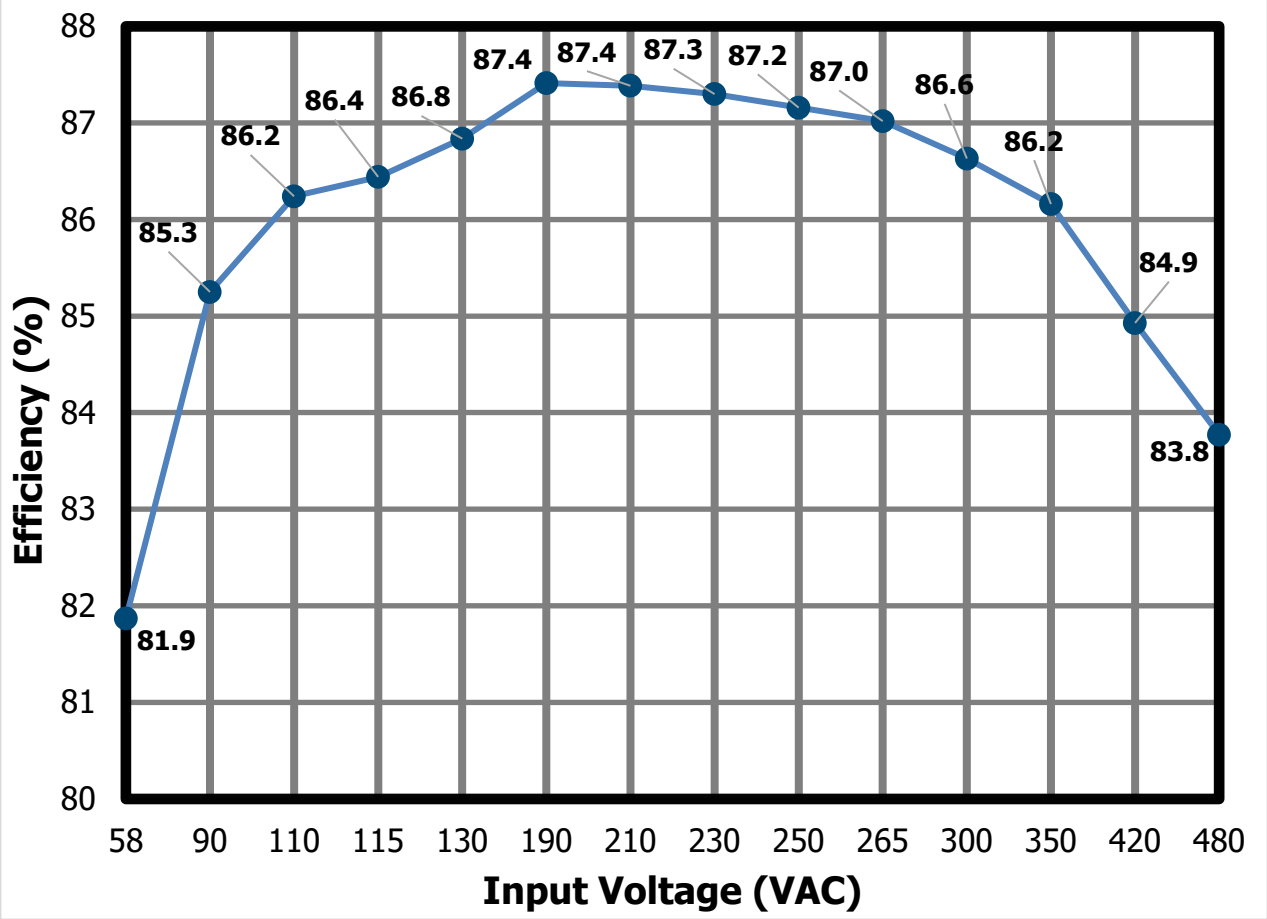


Figure 8 – Full-load Efficiency vs. Line, Room Ambient.

9.2 Efficiency vs. Load

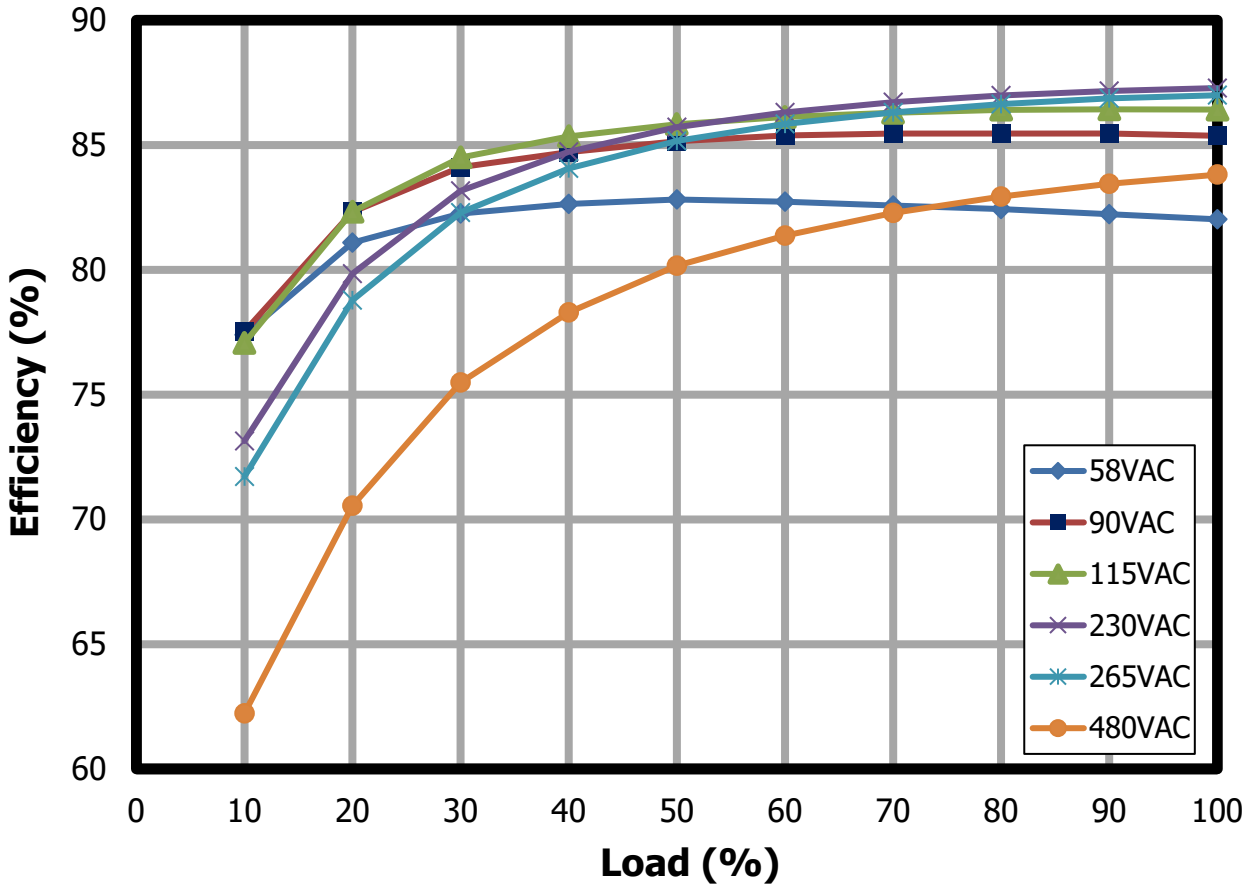


Figure 9 – Efficiency vs. Load, at 25 °C Room Ambient.

9.3 Average Efficiency

	Test	Average	Average	10% Load
Output Voltage (V)	**Power [W]**	**DOE6 Limit (%)**	**CoC v5 Tier 2 (%)**	**CoC v5 Tier 2 (%)**
7, 17.5	10.9	82.4	82.7	72.7

Table 8 – Average Efficiency.

9.3.1 Average and 10% Efficiency at 58 VAC Input

% Load	Efficiency (%)	Average Efficiency (%)
100	82.0	82.2
75	82.3	
50	82.8	
25	81.6	
10	77.4	

Table 9 – Average and 10% Efficiency Test data at 58 VAC.

9.3.2 Average and 10% Efficiency at 90 VAC Input

% Load	Efficiency (%)	Average Efficiency (%)
100	85.4	84.8
75	85.3	
50	85.2	
25	83.2	
10	77.5	

Table 10 – Average and 10% Efficiency Test data at 90 VAC.

9.3.3 Average and 10% Efficiency at 115 VAC Input

% Load	Efficiency (%)	Average Efficiency (%)
100	86.4	85.5
75	86.2	
50	85.8	
25	83.4	
10	77.1	

Table 11 – Average and 10% Efficiency Test data at 115 VAC.

9.3.4 Average and 10% Efficiency at 230 VAC Input

% Load	Efficiency (%)	Average Efficiency (%)
100	87.3	85.3
75	86.7	
50	85.7	
25	81.6	
10	73.1	

Table 12 – Average and 10% Efficiency Test data at 230 VAC.

9.3.5 Average and 10% Efficiency at 265 VAC Input

% Load	Efficiency (%)	Average Efficiency (%)
100	86.9	84.8
75	86.4	
50	85.2	
25	80.6	
10	71.7	

Table 13 – Average and 10% Efficiency Test data at 265 VAC.

9.3.6 Average and 10% Efficiency at 480 VAC Input

% Load	Efficiency (%)	Average Efficiency (%)
100	83.8	79.9
75	82.6	
50	80.2	
25	73.2	
10	62.2	

Table 14 – Average and 10% Efficiency Test data at 480 VAC.

9.4 No-Load Input Power

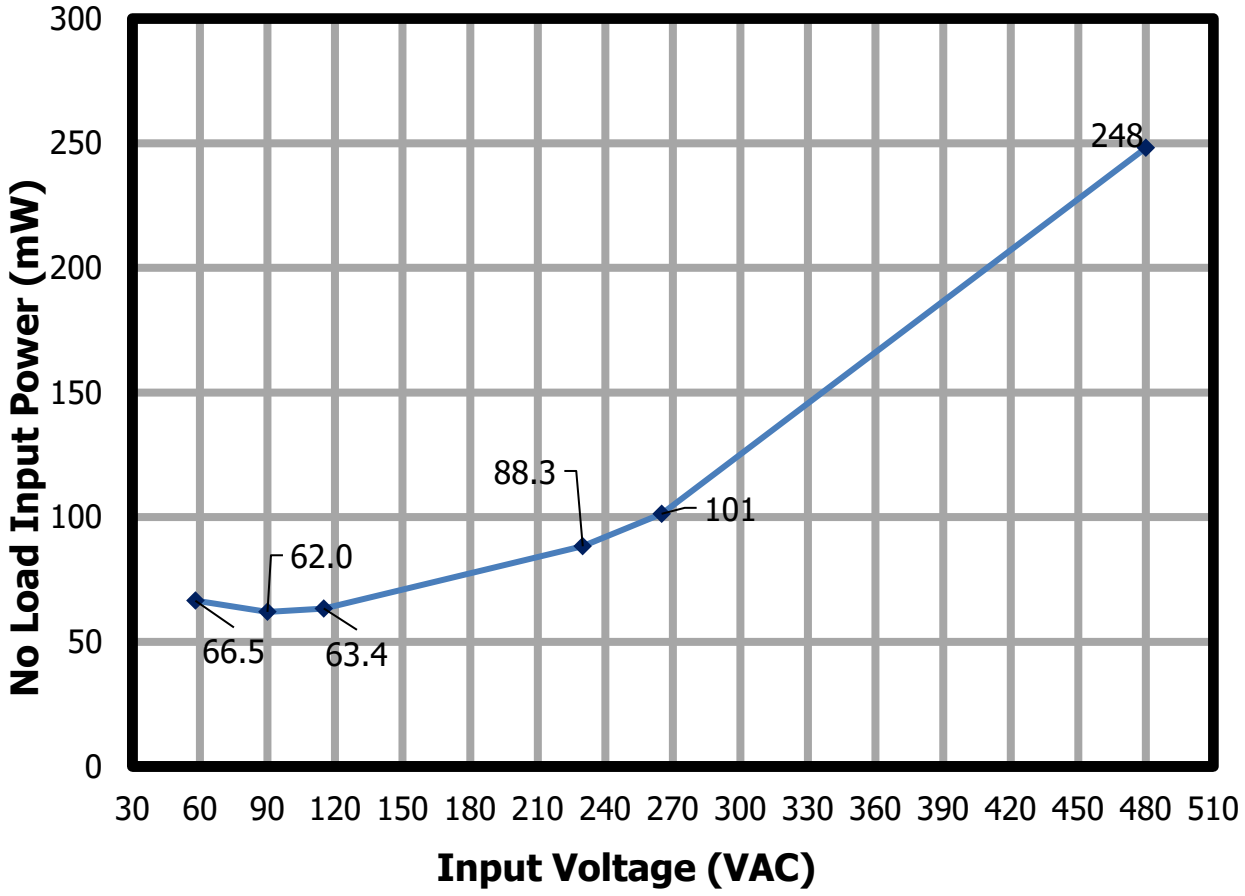


Figure 10 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

9.5 Full Load Line Regulation

Input Voltage (VDC)	Derated Output Load	17.5 V Output Voltage (V)	7 V Output Voltage (V)
40	7 V/0.3 A, 17.5 V/0.36 A	17.3	6.51

Table 15 – Output Voltage vs. Input Voltage at Derated Load (40 VDC).

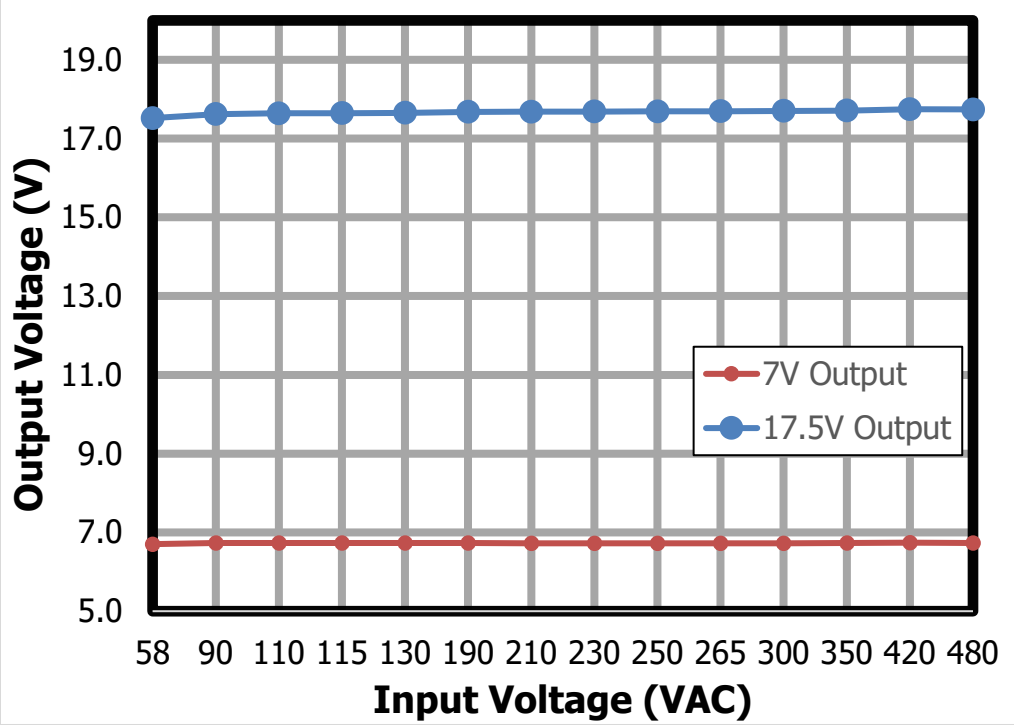


Figure 11 – Full Load Line Regulation.

	17.5 V	7 V
Min	17.5	6.70
Max	17.8	6.74

9.6 Cross Load Regulation

9.6.1 17.5 V Voltage Change with Full Load on 7 V

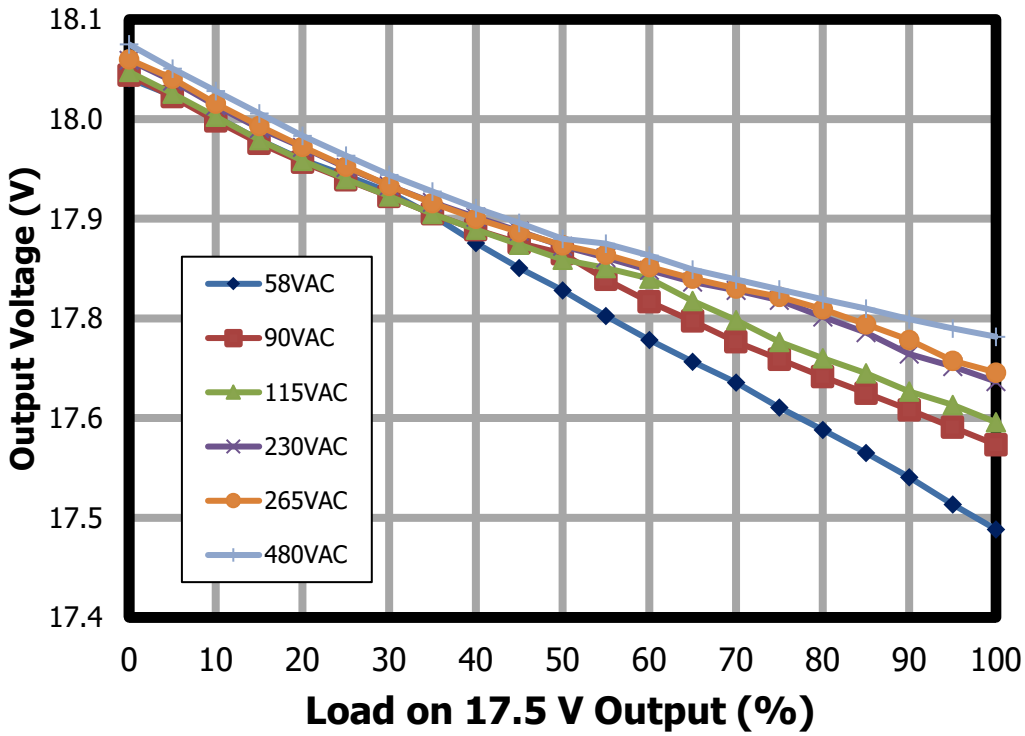


Figure 12 – Cross Regulation (PCB Output Terminal), Room Temperature.

	17.5 V	7 V
Min	17.5	5.60
Max	18.1	6.35

9.6.2 17.5 V Voltage Change with 10% Load on 7 V

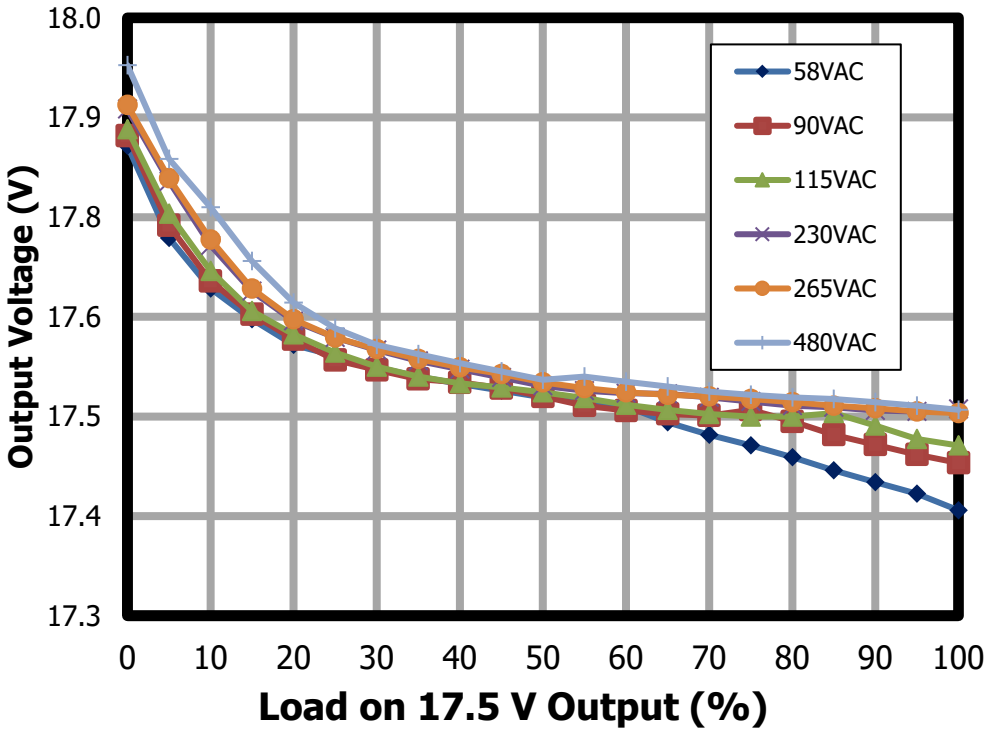


Figure 13 – Cross Regulation (PCB Output Terminal), Room Temperature.

	17.5 V	7 V
Min	17.4	6.69
Max	17.9	6.99

9.6.3 7 V Voltage Change with Full Load on 17.5 V

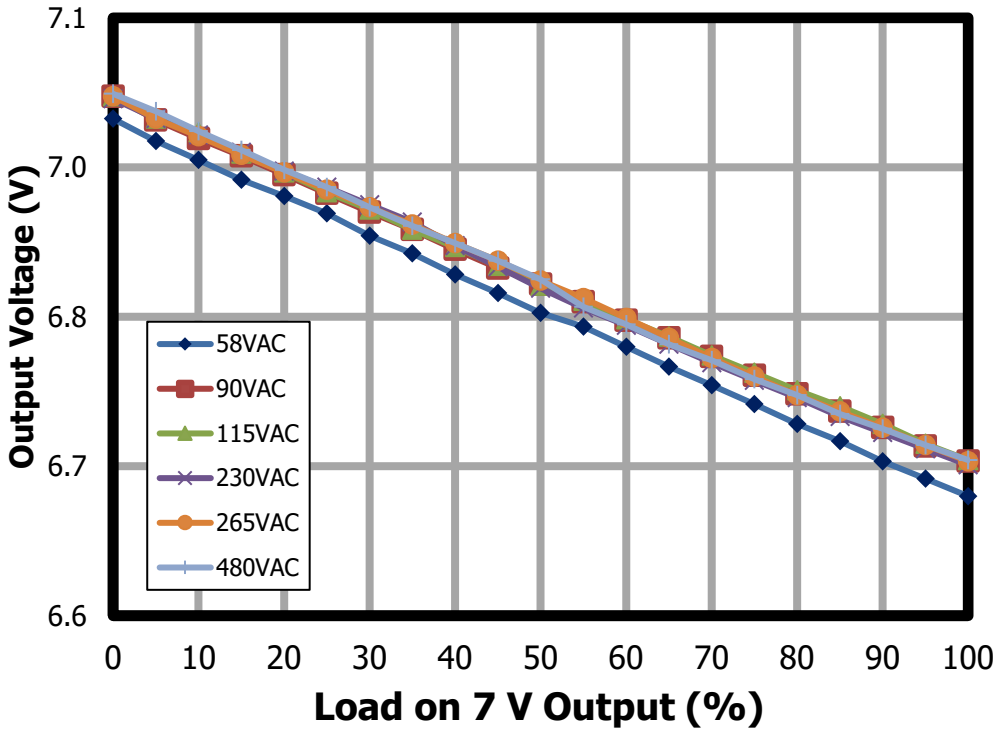


Figure 14 – Cross Regulation (PCB Output Terminal), Room Temperature.

	17.5 V	7 V
Min	17.4	6.70
Max	17.7	7.02

9.6.4 7 V Voltage Change with 10% Load on 17.5 V

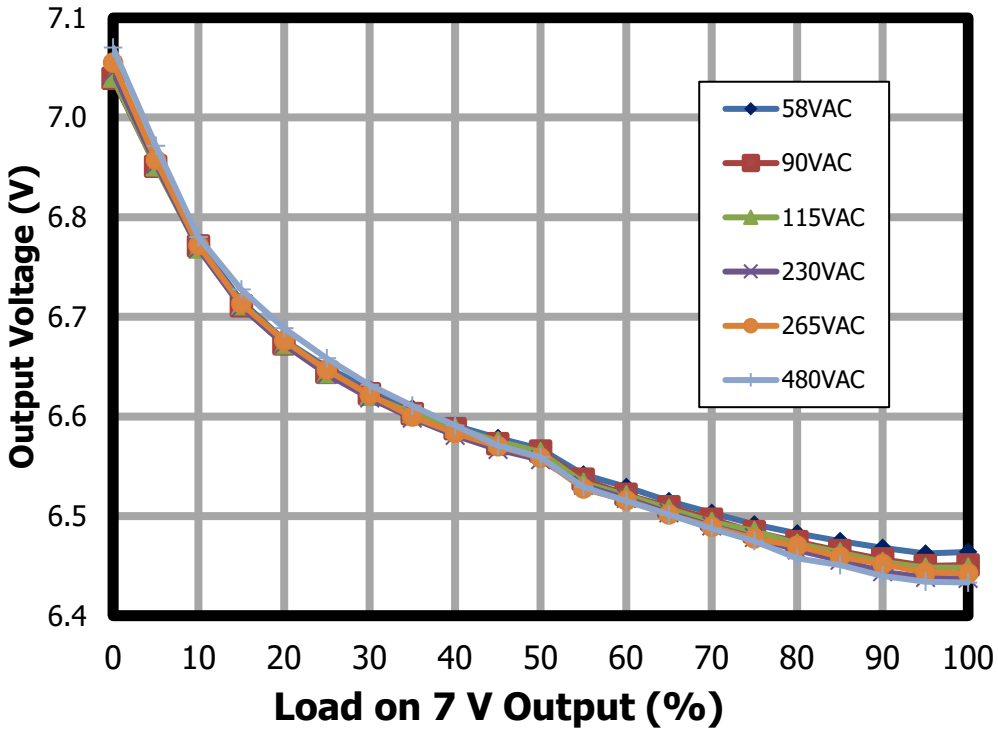


Figure 15 – Cross Regulation (PCB Output Terminal), Room Temperature.

	17.5 V	7 V
Min	17.3	6.40
Max	17.5	7.04

10 Thermal Performance

Thermal performance is measured in room temperature at ambient temperature of 25 °C using a thermal camera.

10.1 40 VDC, 8.4 W[4] at 25 °C Ambient

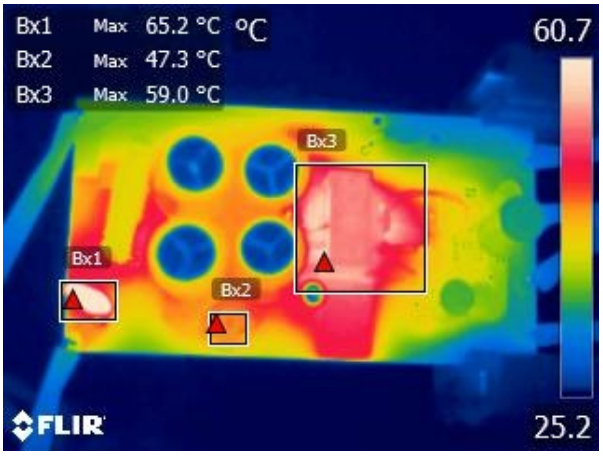


Figure 16 – Top Thermal Image at 40 VDC.

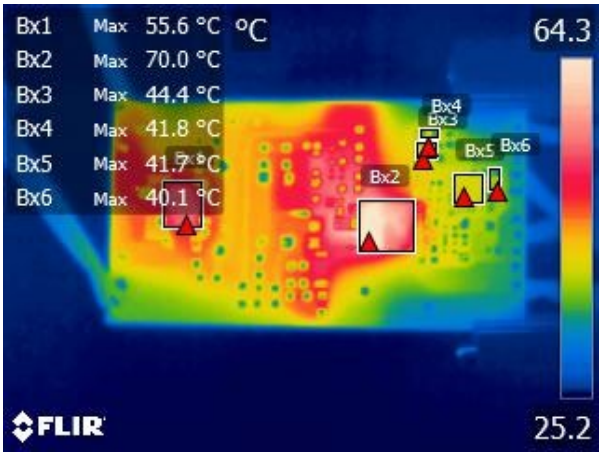


Figure 17 – Bottom Thermal Image at 40 VDC.

Component	Temperature (°C)
Bridge Diode (BR1)	55.6
InnoSwitch (U1)	70.0
SRFET (Q1)	44.4
Snubber Resistor (R19)	41.8
SRFET (Q2)	41.7
Snubber Resistor (R27)	40.1
Thermistor (RT1)	65.2
Differential Mode Choke (L1)	47.3
Transformer (T1)	59.0
Ambient	25.8

Table 16 – Temperature Measurement of Critical Components at 40 VDC Input.

[4] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

10.2 58 VAC, 10.9 W at 25 °C Ambient

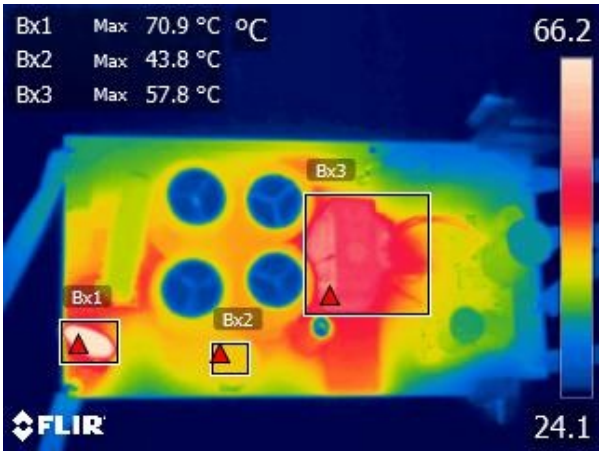


Figure 18 – Top Thermal Image at 58 VAC.

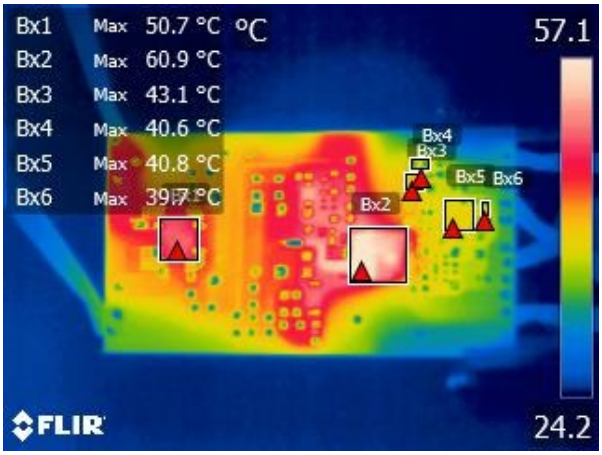


Figure 19 – Bottom Thermal Image at 58 VAC.

Component	Temperature (°C)
Bridge Diode (BR1)	50.7
InnoSwitch (U1)	60.9
SRFET (Q1)	43.1
Snubber Resistor (R19)	40.6
SRFET (Q2)	40.8
Snubber Resistor (R27)	39.7
Thermistor (RT1)	70.9
Differential Mode Choke (L1)	43.8
Transformer (T1)	57.8
Ambient	25.0

Table 17 – Temperature Measurement of Critical Components at 58 VAC Input.

10.3 90 VAC, 10.9 W at 25 °C Ambient

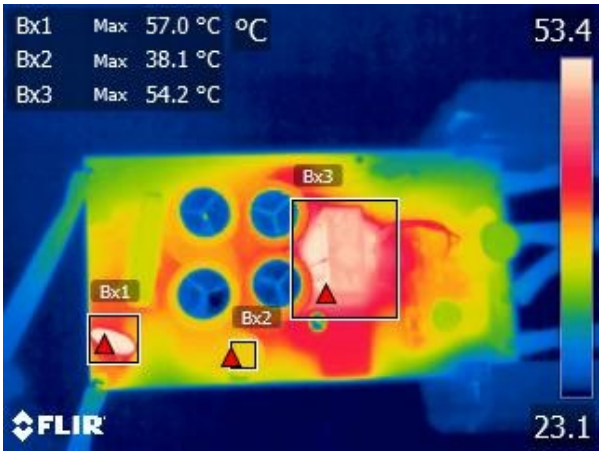


Figure 20 – Top Thermal Image at 90 VAC.

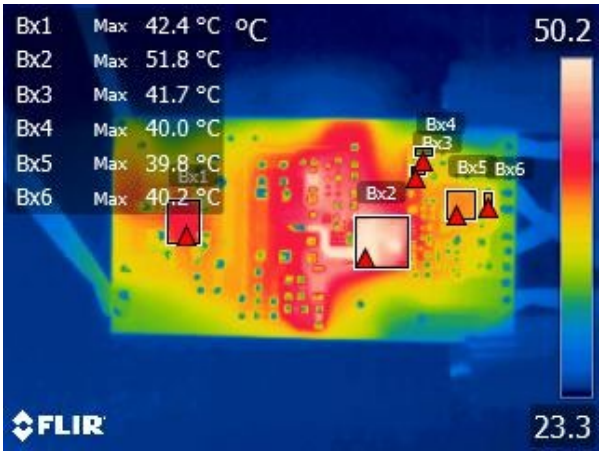


Figure 21 – Bottom Thermal Image at 90 VAC.

Component	Temperature (°C)
Bridge Diode (BR1)	42.4
InnoSwitch (U1)	51.8
SRFET (Q1)	41.7
Snubber Resistor (R19)	40.0
SRFET (Q2)	39.8
Snubber Resistor (R27)	40.2
Thermistor (RT1)	57.0
Differential Mode Choke (L1)	38.1
Transformer (T1)	54.2
Ambient	24.0

Table 18 – Temperature Measurement of Critical Components at 90 VAC Input.

10.4 265 VAC Input, 10.9 W at 25 °C Ambient

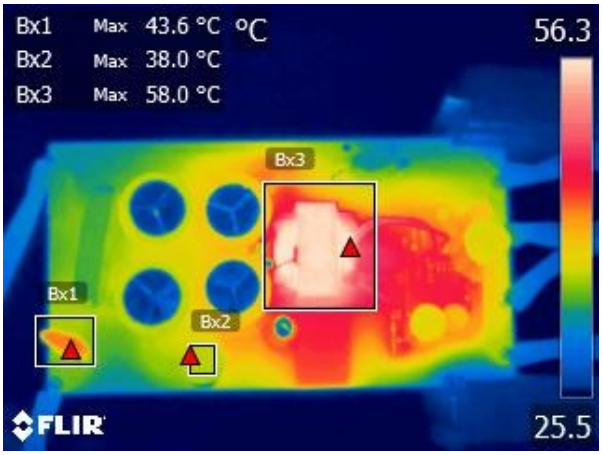


Figure 22 – Top Thermal Image at 265 VAC.

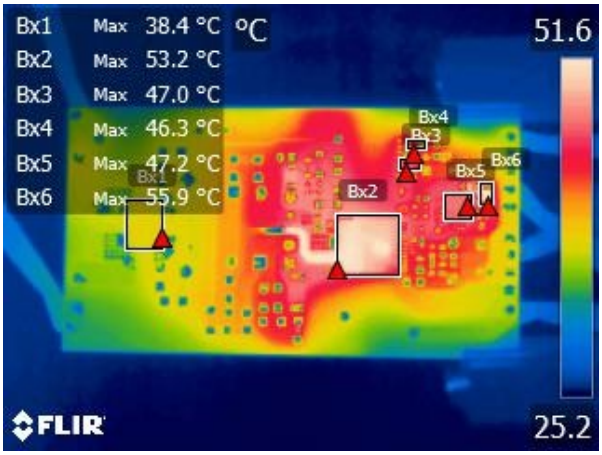


Figure 23 – Bottom Thermal Image at 265 VAC.

Component	Temperature (°C)
Bridge Diode (BR1)	38.4
InnoSwitch (U1)	53.2
SRFET (Q1)	47.0
Snubber Resistor (R19)	46.3
SRFET (Q2)	47.2
Snubber Resistor (R27)	55.9
Thermistor (RT1)	43.6
Differential Mode Choke (L1)	38.0
Transformer (T1)	58.0
Ambient	26.0

Table 19 – Temperature Measurement of Critical Components at 265 VAC Input.

10.5 480 VAC Input, 10.9 W at 25 °C Ambient

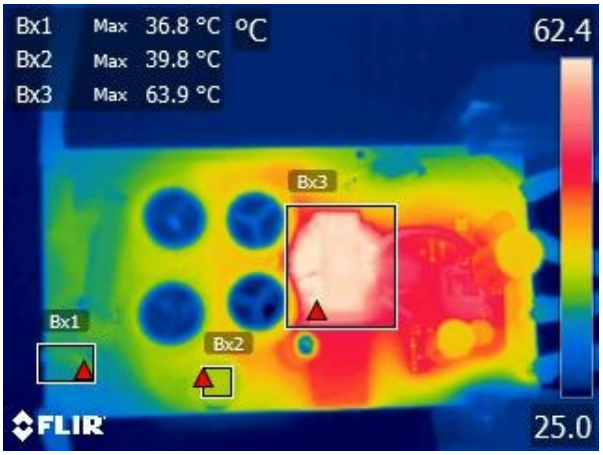


Figure 24 – Top Thermal Image at 480 VAC.

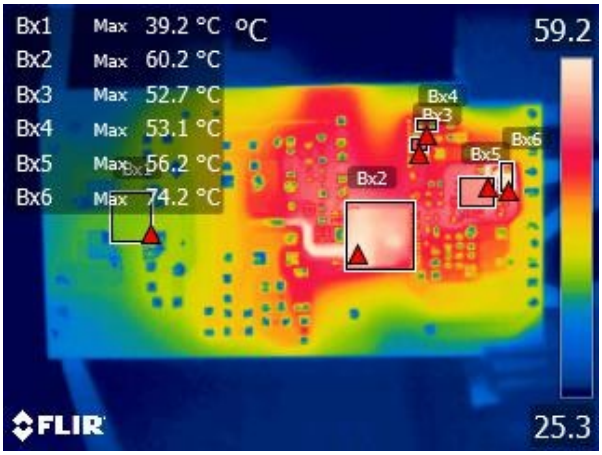


Figure 25 – Bottom Thermal Image at 480 VAC.

Component	Temperature (°C)
Bridge Diode (BR1)	39.2
InnoSwitch (U1)	60.2
SRFET (Q1)	52.7
Snubber Resistor (R19)	53.1
SRFET (Q2)	56.2
Snubber Resistor (R27)	74.2
Thermistor (RT1)	36.8
Differential Mode Choke (L1)	39.8
Transformer (T1)	63.9
Ambient	25.8

Table 20 – Temperature Measurement of Critical Components at 480 VAC Input.

11 Waveforms

11.1 Output Voltage Start-up Waveforms at Room Temperature

11.1.1 100% Load

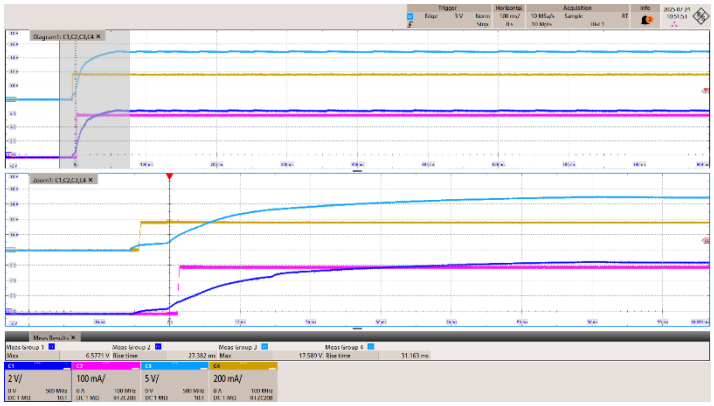


Figure 26 – 40 VDC[5]
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 31 ms
7 V Output Voltage, Rise Time = 27 ms

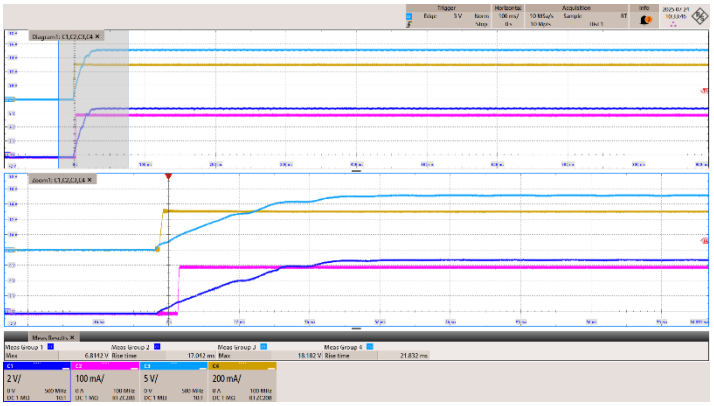


Figure 27 – 58 VAC, 60 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 22 ms
7 V Output Voltage, Rise Time = 17 ms

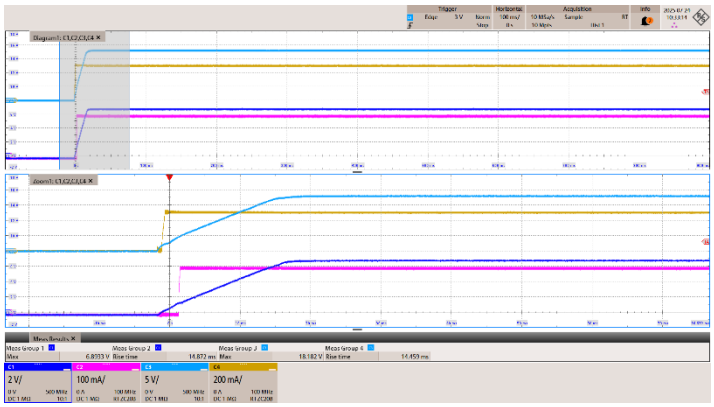


Figure 28 – 90 VAC, 60 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 14 ms
7 V Output Voltage, Rise Time = 15 ms

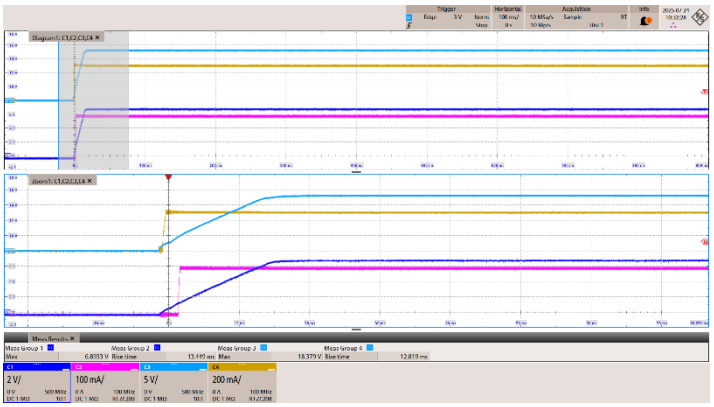


Figure 29 – 265 VAC, 50 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 13 ms
7 V Output Voltage, Rise Time = 13 ms

[5] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

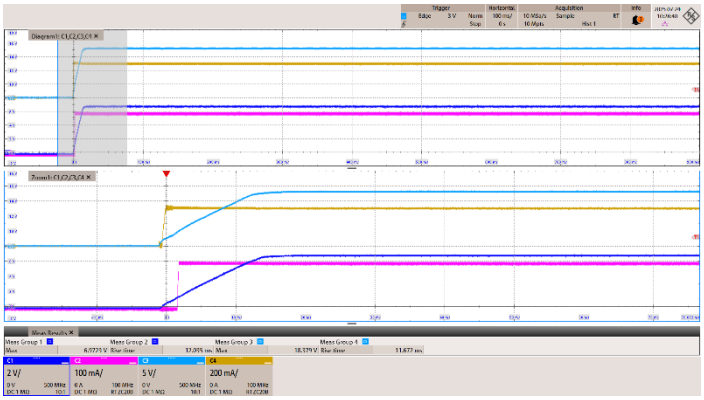


Figure 30 – 480 VAC, 50 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 12 ms
7 V Output Voltage, Rise Time = 12 ms

11.1.2 0% Load

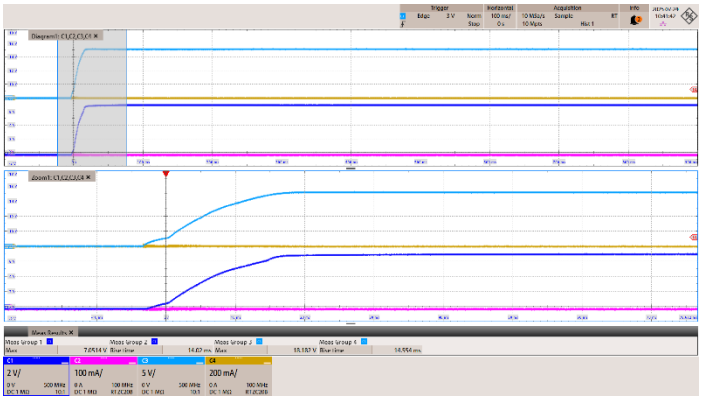


Figure 31 – 40 VDC
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 15 ms
7 V Output Voltage, Rise Time = 14 ms

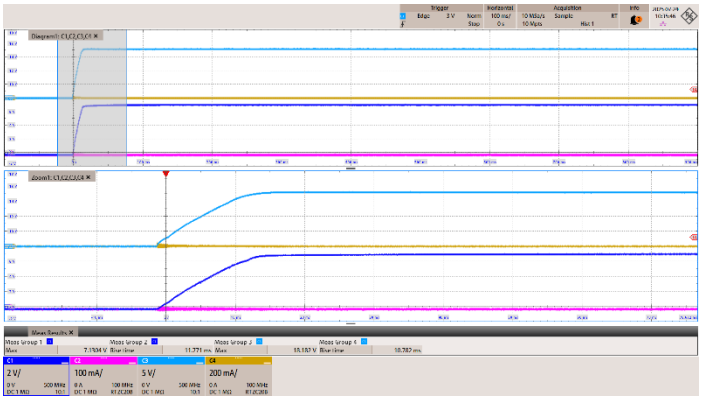


Figure 32 – 58 VAC, 60 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 11 ms
7 V Output Voltage, Rise Time = 12 ms

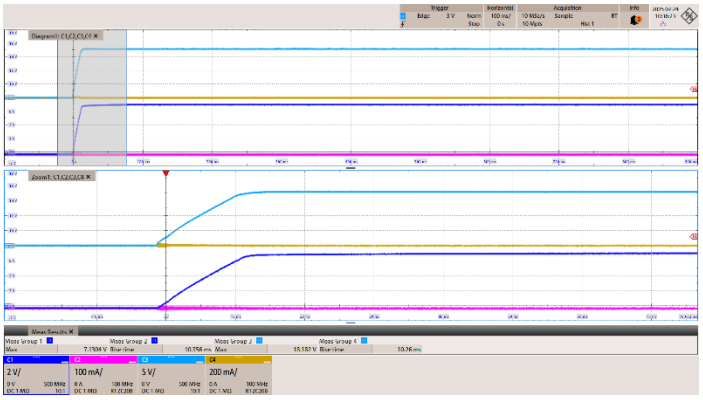


Figure 33 – 90 VAC, 60 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 10 ms
7 V Output Voltage, Rise Time = 10 ms

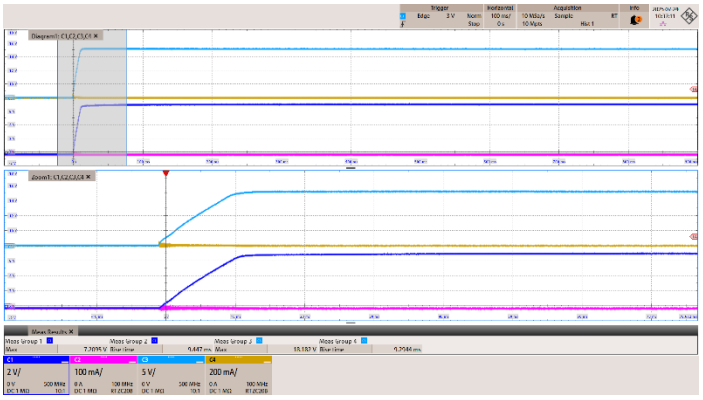


Figure 34 – 265 VAC, 50 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 9 ms
7 V Output Voltage, Rise Time = 9 ms

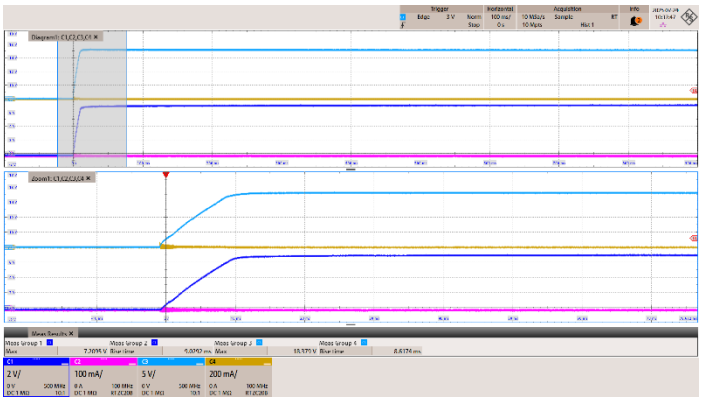


Figure 35 – 480 VAC, 50 Hz
CH1: 7 V_{OUT}, 2 V / div., 100 ms / div
CH2: 7 V I_{OUT}, 100 mA / div., 100 ms / div
CH3: 17.5 V_{OUT}, 5 V / div., 100 ms / div
CH4: 17.5 V I_{OUT}, 200 mA / div., 100 ms / div
Zoom: 10 ms/div
17.5 V Output Voltage, Rise Time = 9 ms
7 V Output Voltage, Rise Time = 9 ms

11.2 Load Transient Response (On Board)

11.2.1 17.5 V Output: 0 – 100% (0 – 0.5 A), 7 V Output: Full Load (0.3 A)

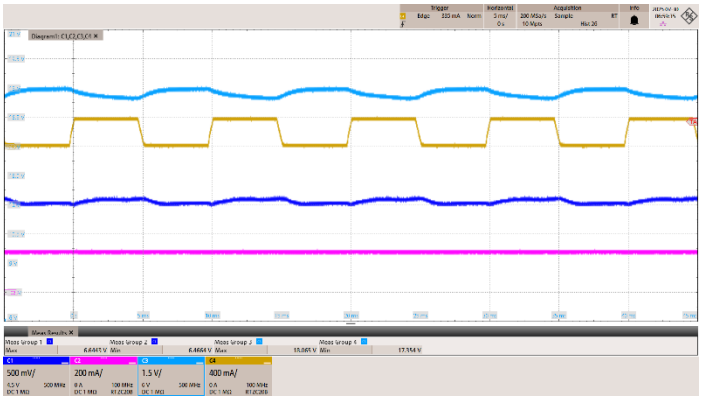


Figure 36 – 40 VDC[6]
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 18.1 V
17.5 V_{MIN}: 17.4 V

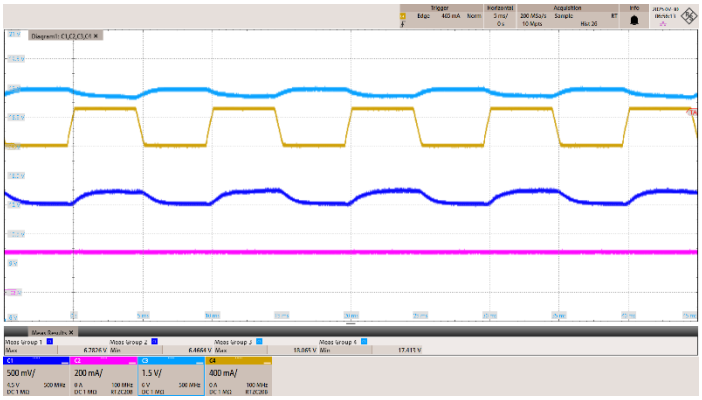


Figure 37 – 58 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 18.1 V
17.5 V_{MIN}: 17.4 V

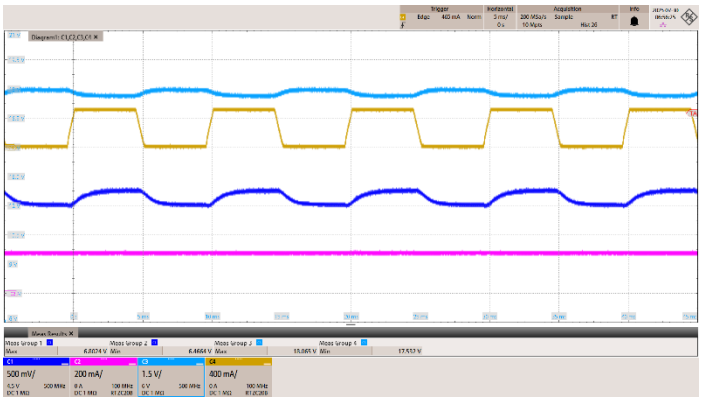


Figure 38 – 90 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 18.1 V
17.5 V_{MIN}: 17.5 V

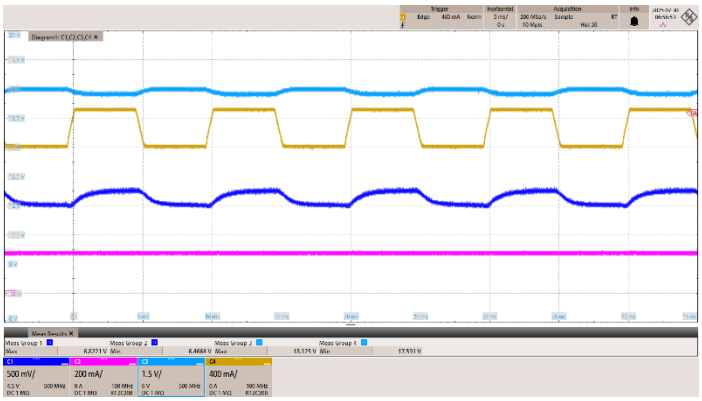


Figure 39 – 265 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 18.1 V
17.5 V_{MIN}: 17.6 V

[6] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

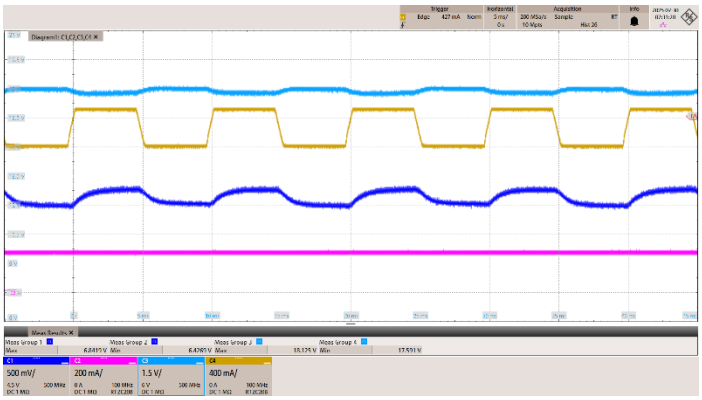


Figure 40 – 480 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 18.1 V
17.5 V_{MIN}: 17.6 V

11.2.2 17.5 V Output: 50 – 100% (0.25 – 0.5 A), 7 V Output: Full Load (0.3 A)

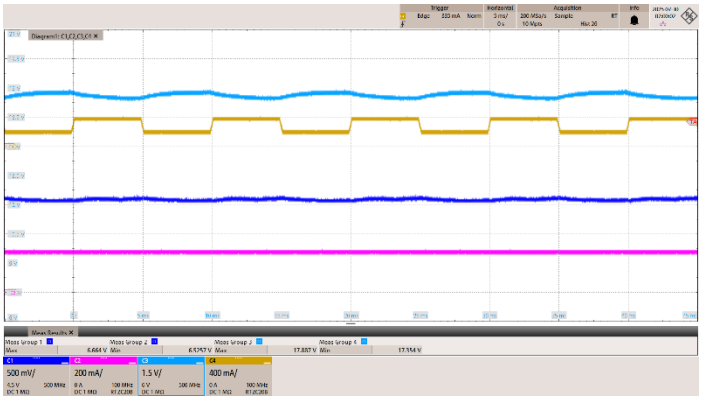


Figure 41 – 40 VDC[7]
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 17.9 V
17.5 V_{MIN}: 17.4 V

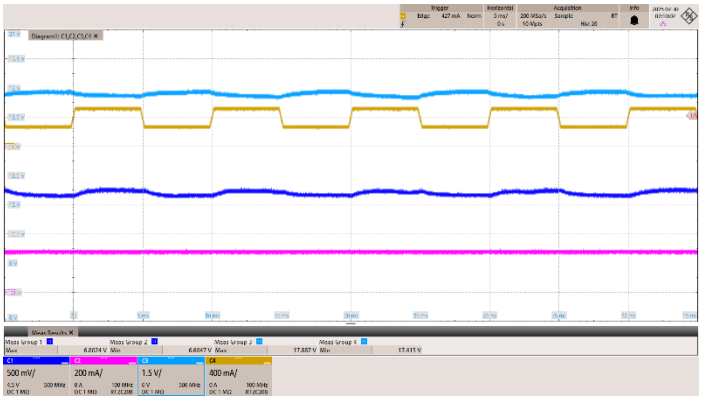


Figure 42 – 58 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 17.9 V
17.5 V_{MIN}: 17.4 V

[7] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

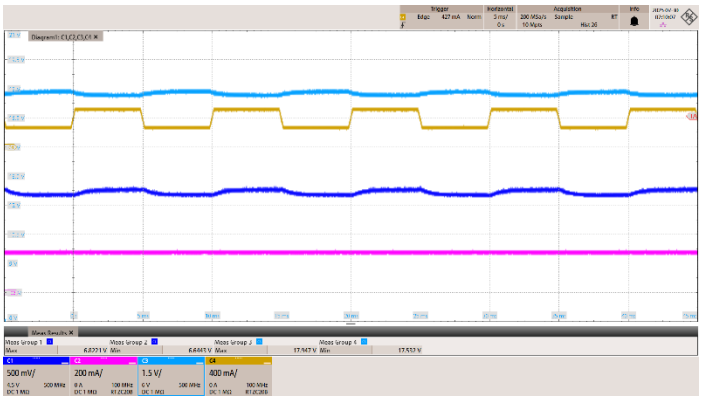


Figure 43 – 90 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 17.9 V
17.5 V_{MIN}: 17.5 V

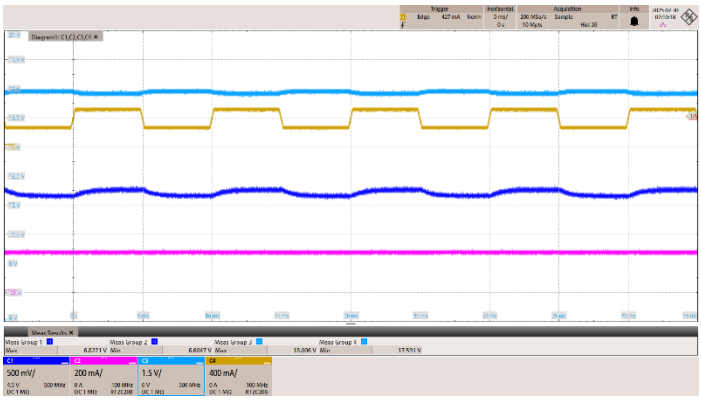


Figure 44 – 265 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 18.0 V
17.5 V_{MIN}: 17.6 V

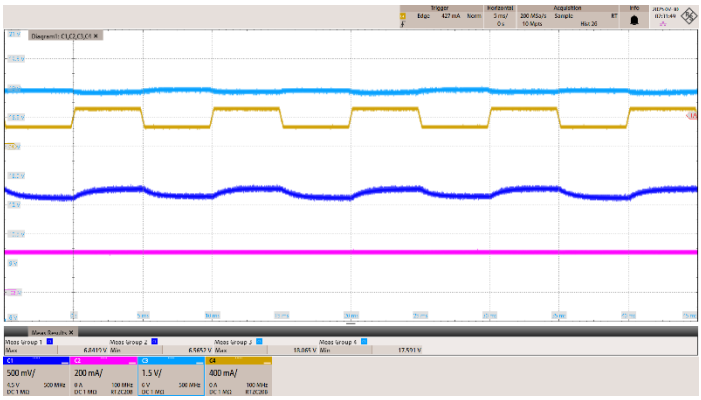


Figure 45 – 480 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
17.5 V_{MAX}: 18.1 V
17.5 V_{MIN}: 17.6 V

11.2.3 7 V Output: 0 – 100% (0 – 0.3 A), 17.5 V Output: Full Load (0.5 A)

Figure 46 – 40 VDC[8]
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 7.06 V
7 V_{MIN}: 6.57 V

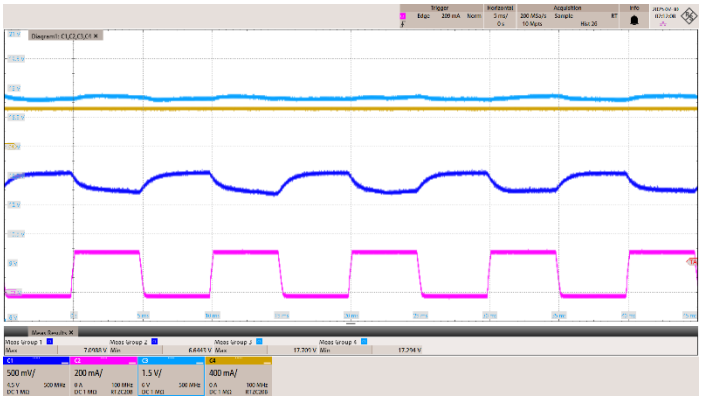


Figure 47 – 58 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 7.10 V
7 V_{MIN}: 6.64 V

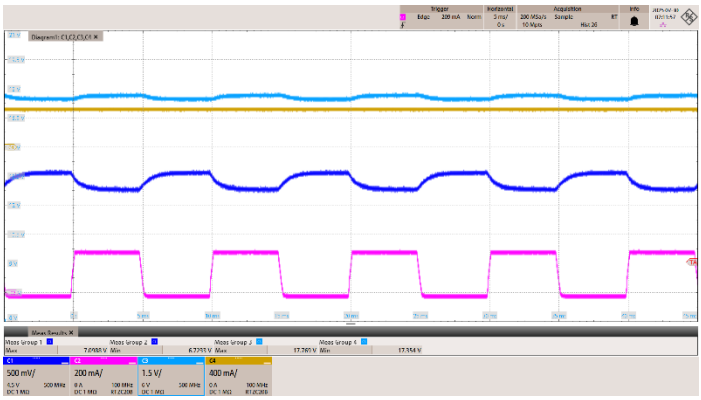


Figure 48 – 90 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 7.10 V
7 V_{MIN}: 6.72 V

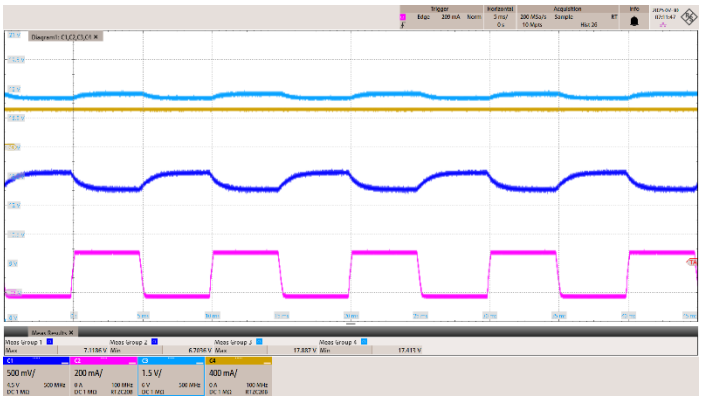


Figure 49 – 265 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 7.12 V
7 V_{MIN}: 6.70 V

[8] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

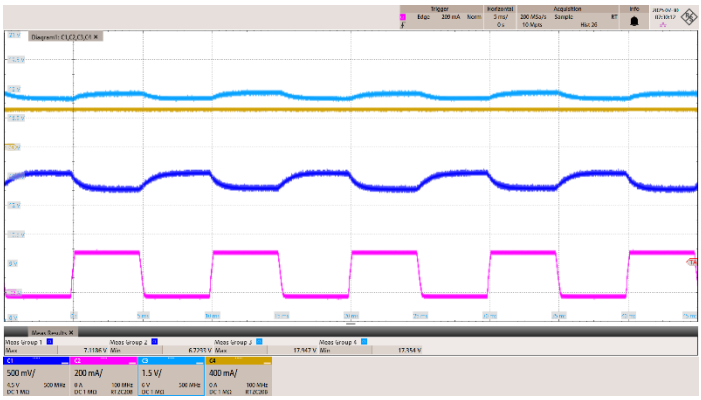


Figure 50 – 480 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 7.12 V
7 V_{MIN}: 6.72 V

11.2.4 7 V Output: 50 – 100% (0.15 – 0.3 A), 17.5 V Output: Full Load (0.5 A)

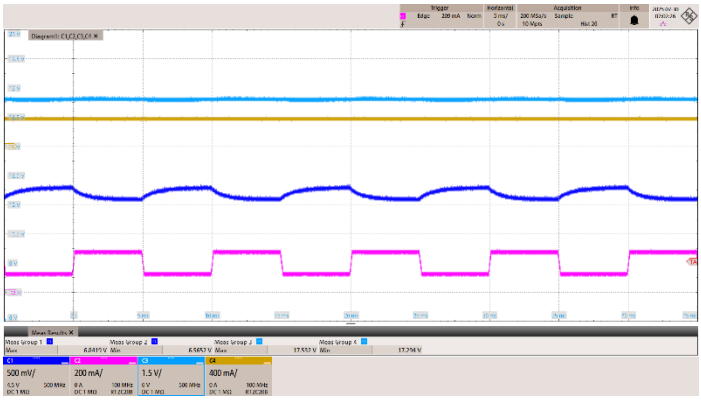


Figure 51 – 40 VDC[9]
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 6.84 V
7 V_{MIN}: 6.57 V

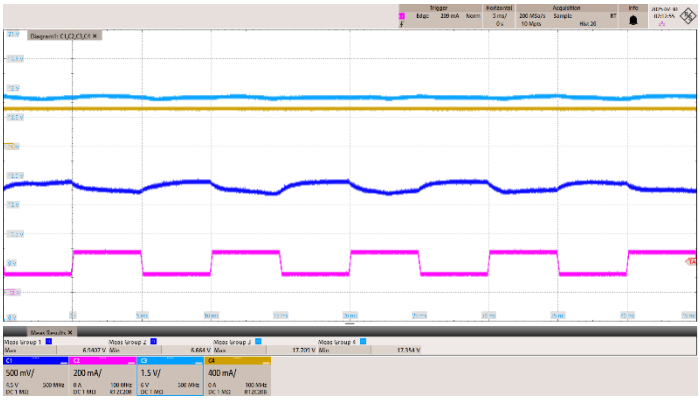


Figure 52 – 58 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 6.94 V
7 V_{MIN}: 6.64 V

[9] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

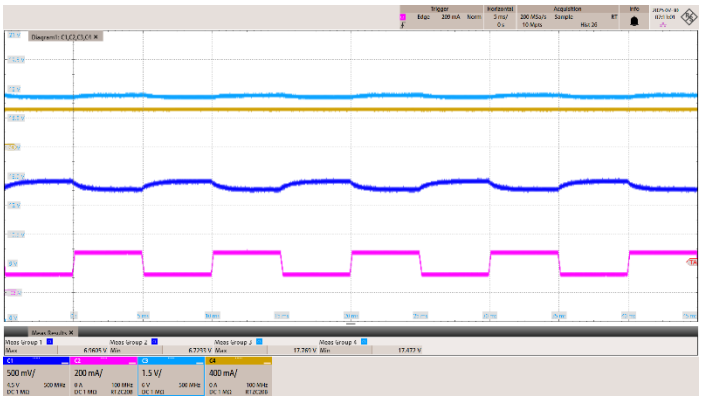


Figure 53 – 90 VAC, 60 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 6.96 V
7 V_{MIN}: 6.72 V

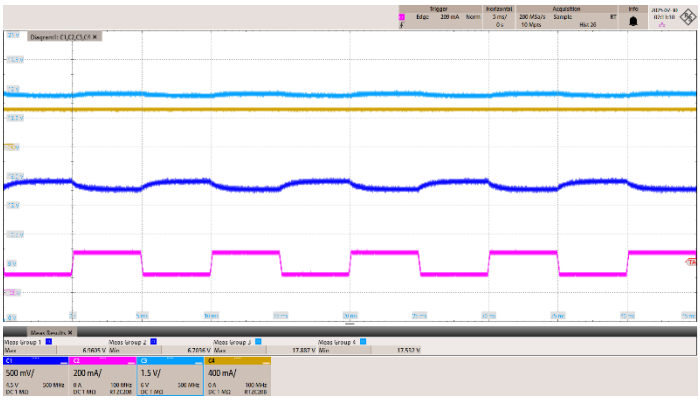


Figure 54 – 265 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 6.96 V
7 V_{MIN}: 6.70 V

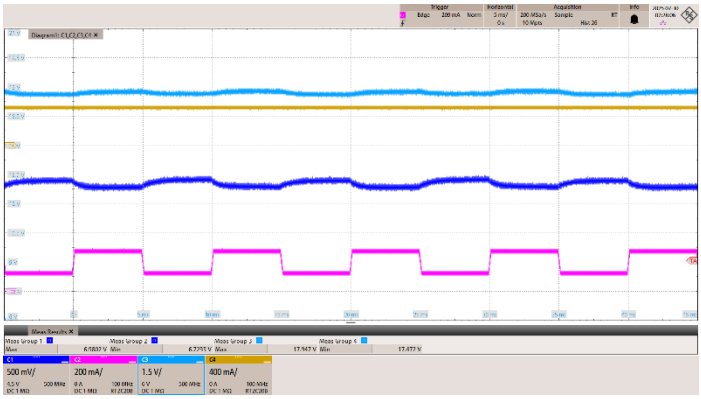


Figure 55 – 480 VAC, 50 Hz
CH1: 7 V_{OUT}: 500 mV / div, 5 ms / div
CH2: 7 V I_{OUT}: 200 mA / div, 5 ms / div
CH3: 17.5 V_{OUT}: 1.5 V / div, 5 ms / div
CH4: 17.5 V I_{OUT}: 400 mA / div, 5 ms / div
7 V_{MAX}: 6.98 V
7 V_{MIN}: 6.72 V

11.3 InnoSwitch Switching Waveforms

11.3.1 Drain Voltage and Current at Start up

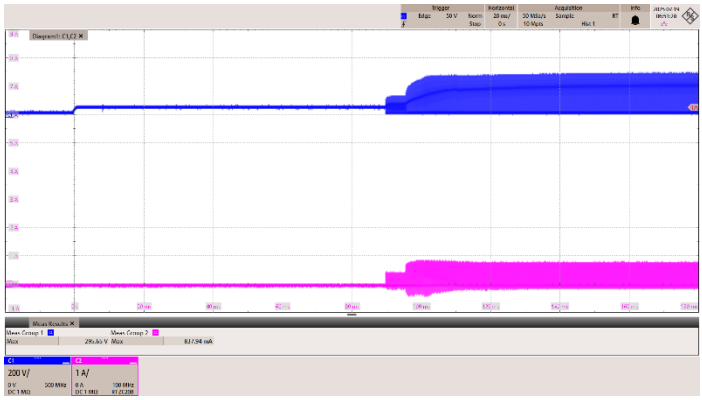


Figure 56 – 40 VDC, Po = 8.4 W[10]
CH1: Drain Voltage: 200 V / div, 20 ms / div
CH2: Drain Current: 1 A / div, 20 ms / div
Drain Voltage, Max = 296 V
Drain Current, Max = 0.838 A

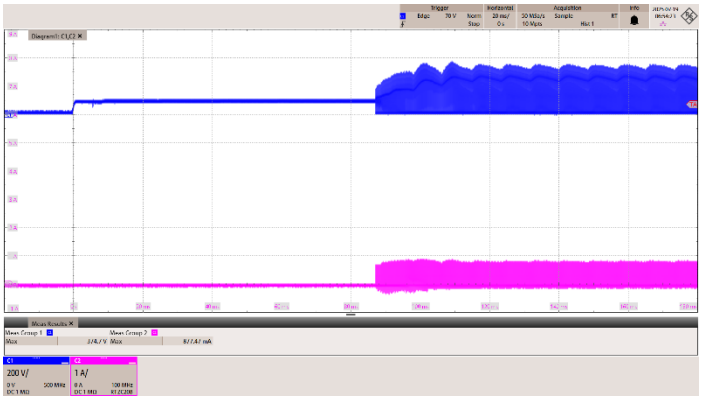


Figure 57 – 58 VAC, 60 Hz, Po = 10.9 W
CH1: Drain Voltage: 200 V / div, 20 ms / div
CH2: Drain Current: 1 A / div, 20 ms / div
Drain Voltage, Max = 375 V
Drain Current, Max = 0.878 A

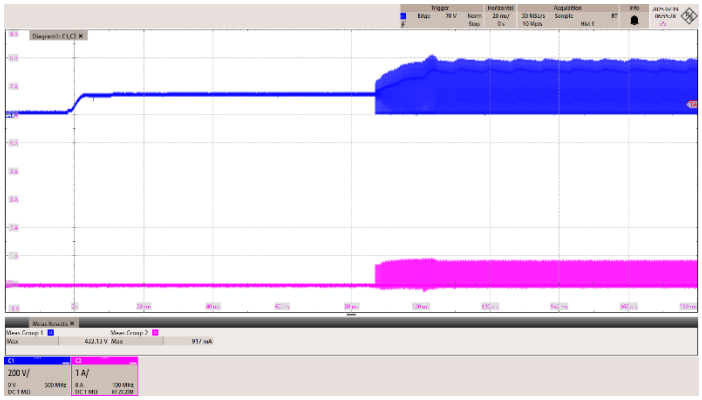


Figure 58 – 90 VAC, 60 Hz, Po = 10.9 W
CH1: Drain Voltage: 200 V / div, 20 ms / div
CH2: Drain Current: 1 A / div, 20 ms / div
Drain Voltage, Max = 422 V
Drain Current, Max = 0.917 A

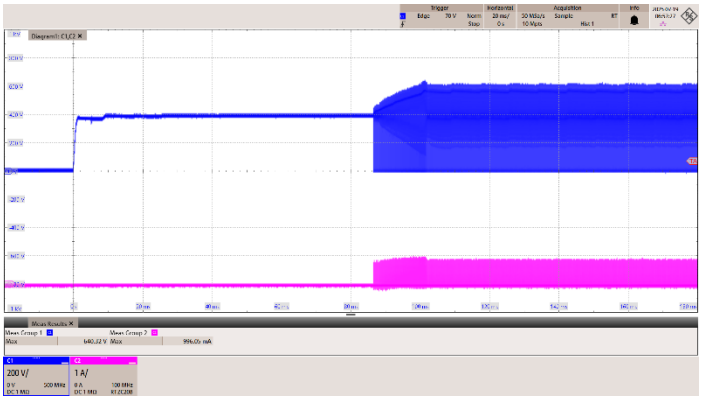


Figure 59 – 265 VAC, 50 Hz, Po = 10.9 W
CH1: Drain Voltage: 200 V / div, 20 ms / div
CH2: Drain Current: 1 A / div, 20 ms / div
Drain Voltage, Max = 640 V
Drain Current, Max = 0.996 A

[10] Full load at 40 VDC input is derated to 8.4 W (7 V0.3 A, 17.5 V/0.36 A).

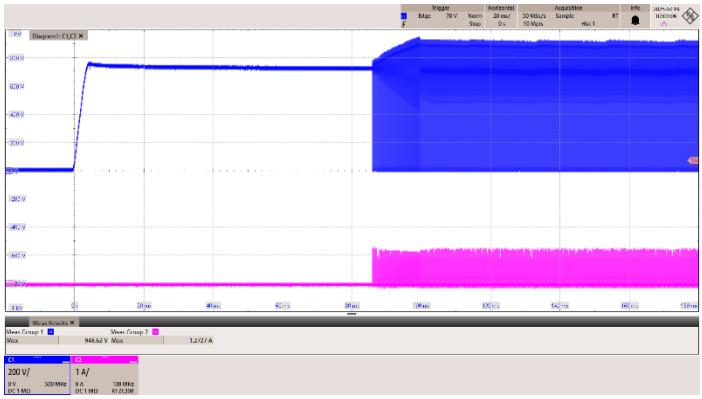


Figure 60 – 480 VAC, 50 Hz, Po = 10.9 W
CH1: Drain Voltage: 200 V / div, 20 ms / div
CH2: Drain Current: 1 A / div, 20 ms / div
Drain Voltage, Max = 949 V
Drain current, Max = 1.27 A

11.3.2 Drain Voltage and Current in Normal Operation

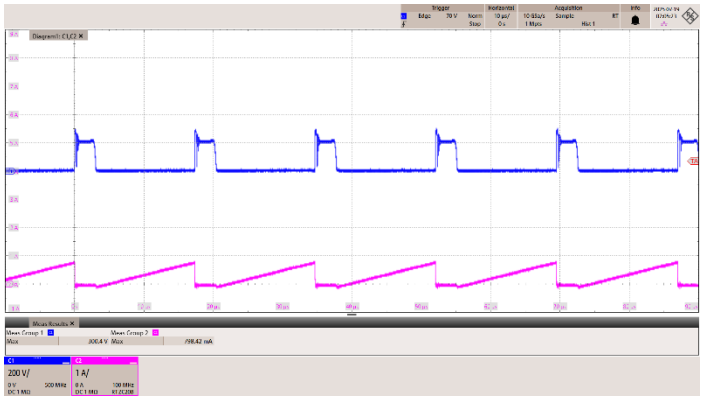


Figure 61 – 40 VDC, Po = 8.4 W[11]

CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 1 A / div, 10 µs / div
Drain voltage, Max = 300 V
Drain current, Max = 0.798 A

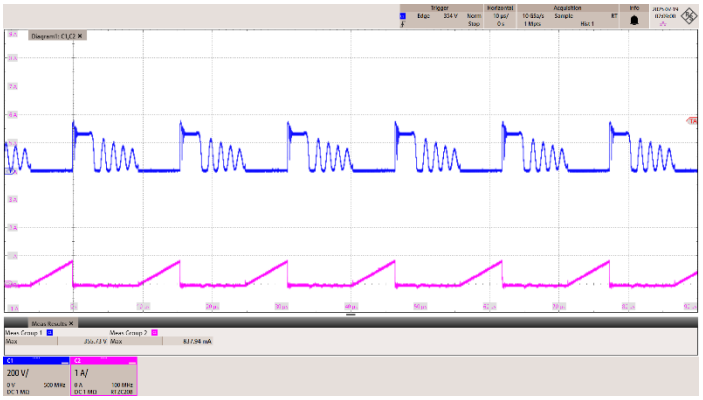


Figure 62 – 58 VAC, 60 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 1 A / div, 10 µs / div
Drain voltage, Max = 356 V
Drain current, Max = 0.834 A

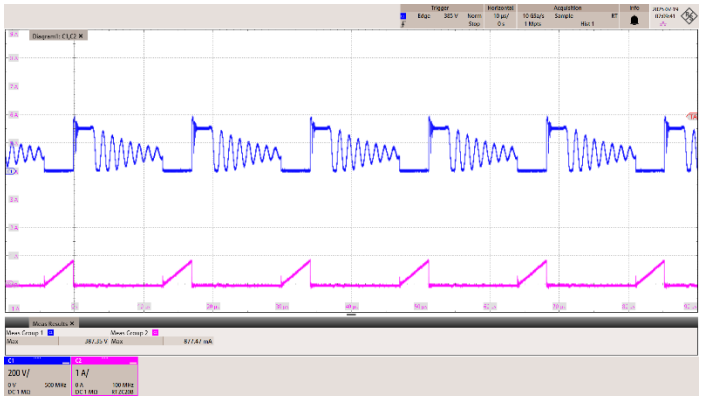


Figure 63 – 90 VAC, 60 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 1 A / div, 10 µs / div
Drain voltage, Max = 387 V
Drain current, Max = 0.878 A

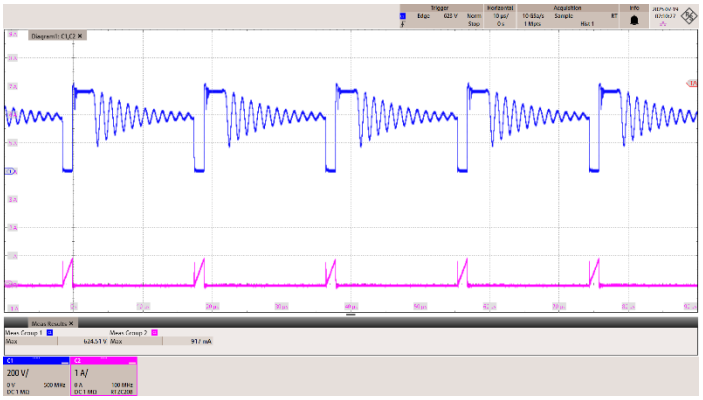


Figure 64 – 265 VAC, 50 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 1 A / div, 10 µs / div
Drain voltage, Max = 625 V
Drain current, Max = 0.917 A

[11] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

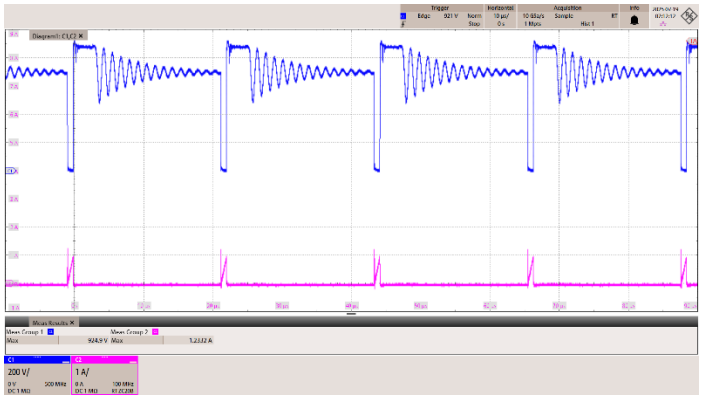


Figure 65 – 480 VAC, 50 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 1 A / div, 10 µs / div
Drain voltage, Max = 925 V
Drain current, Max = 1.23 A

11.3.3 Drain Voltage and Current with Output Shorted

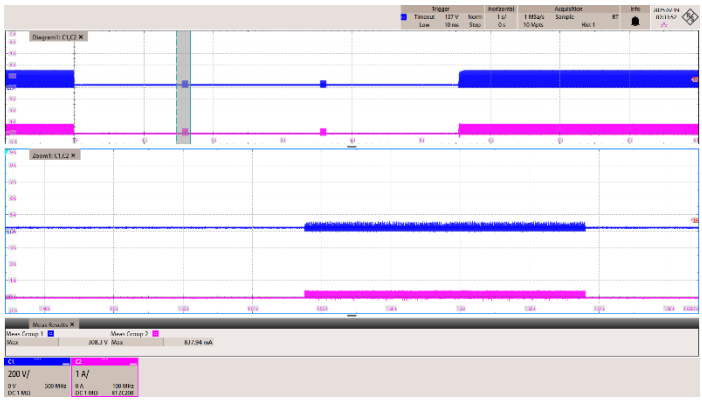


Figure 66 – 40 VDC, Po = 8.4 W[12]

CH 1: Drain Voltage: 200 V / div, 2 s / div
CH 2: Drain Current: 1 A / div, 2 s / div
Zoom: 20 ms / div
Drain voltage, Max = 308 V
Drain current, Max = 0.838 A

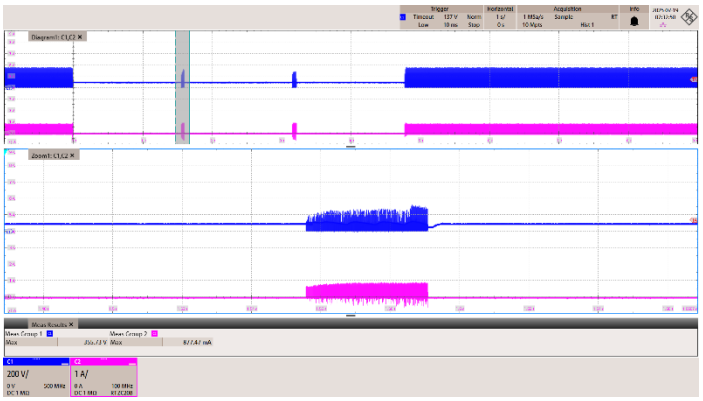


Figure 67 – 58 VAC, 60 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 2 s / div
CH 2: Drain Current: 1 A / div, 2 s / div
Zoom: 20 ms / div
Drain voltage, Max = 356 V
Drain current, Max = 0.878 A

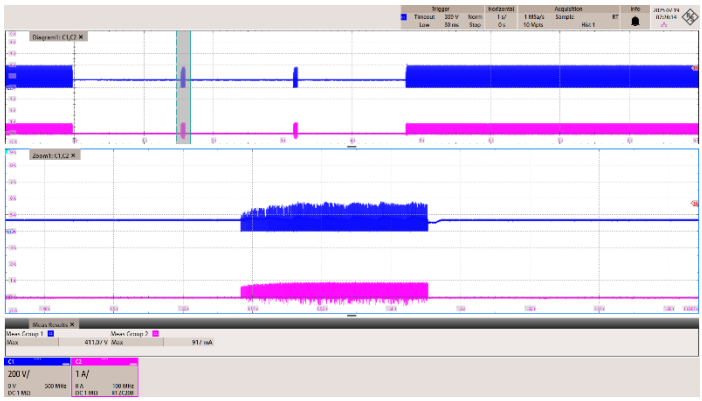


Figure 68 – 90 VAC, 60 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 2 s / div
CH 2: Drain Current: 1 A / div, 2 s / div
Zoom: 20 ms / div
Drain voltage, Max = 411 V
Drain current, Max = 0.917 A

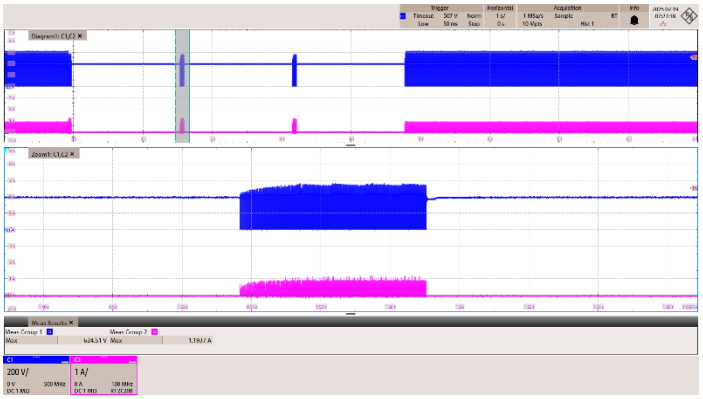


Figure 69 – 265 VAC, 50 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 2 s / div
CH 2: Drain Current: 1 A / div, 2 s / div
Zoom: 20 ms / div
Drain voltage, Max = 625 V
Drain current, Max = 1.19 A

[12] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

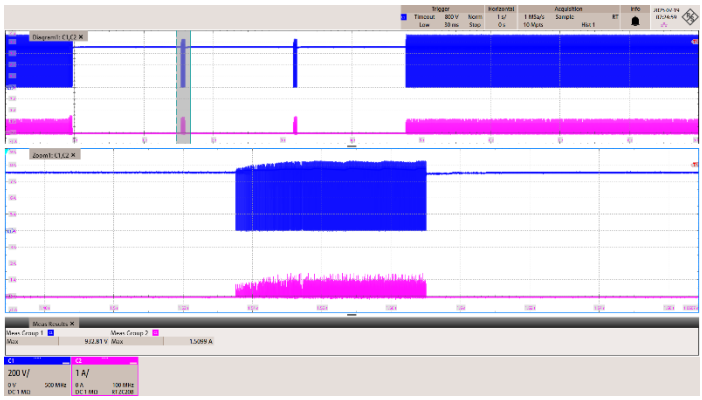


Figure 70 – 480 VAC, 50 Hz, Po = 10.9 W

CH 1: Drain Voltage: 200 V / div, 2 s / div
CH 2: Drain Current: 1 A / div, 2 s / div
Zoom: 20 ms / div
Drain voltage, Max = 933 V
Drain current, Max = 1.51 A

11.4 SRFET Switching Waveforms

11.4.1 17.5 V SR FET Waveforms

11.4.1.1 Start-up Operation (100% Load)

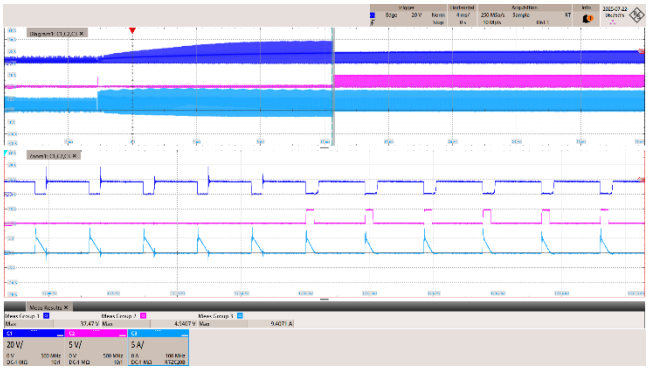


Figure 71 – 40 VDC, Po = 8.4 W[13]

Ch1: SR V_{DS}, 20 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 5 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 37.5 V
SRFET Drain Current, Max. = 9.41 A

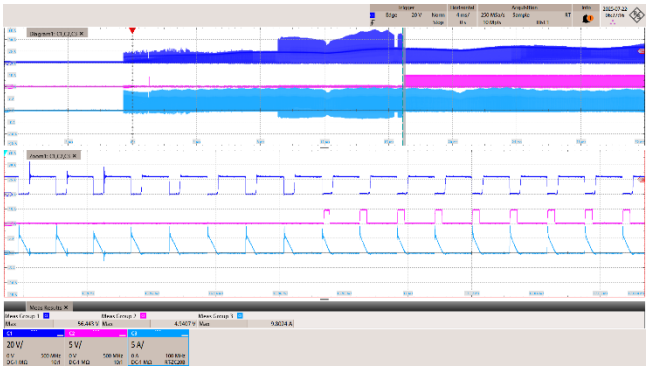


Figure 72 – 58 VAC, 60 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 20 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 5 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 56.4 V
SRFET Drain Current, Max. = 9.80 A

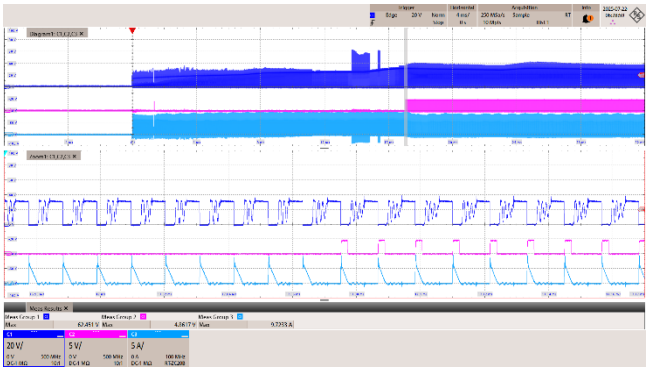


Figure 73 – 90 VAC, 60 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 20 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 5 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 62.4 V
SRFET Drain Current, Max. = 9.72 A

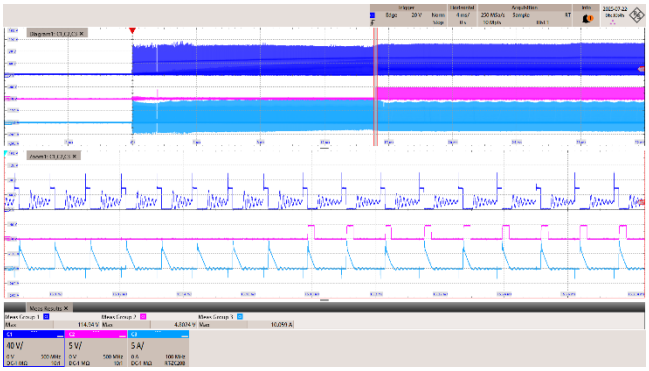


Figure 74 – 265 VAC, 50 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 40 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 5 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 115 V
SRFET Drain Current, Max. = 10.1 A

[13] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

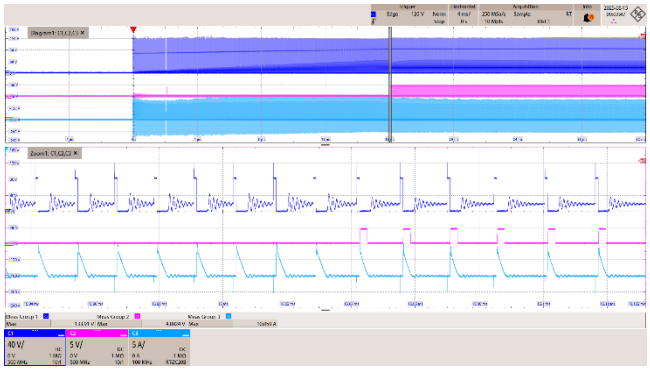


Figure 75 – 450 VAC, 50 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 40 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 5 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 134 V
SRFET Drain Current, Max. = 10.1 A

11.4.1.2 Normal Operation (100% Load)

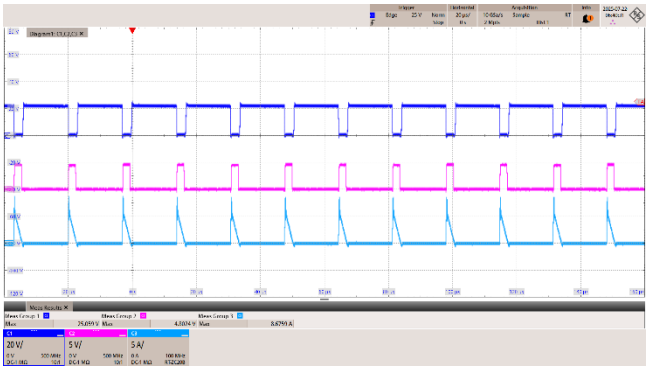


Figure 76 – 40 VDC, Po = 8.4 W[14]

Ch1: SR V_{DS}, 20 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 5 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 25.1 V
SRFET Drain Current, Max. = 8.68 A

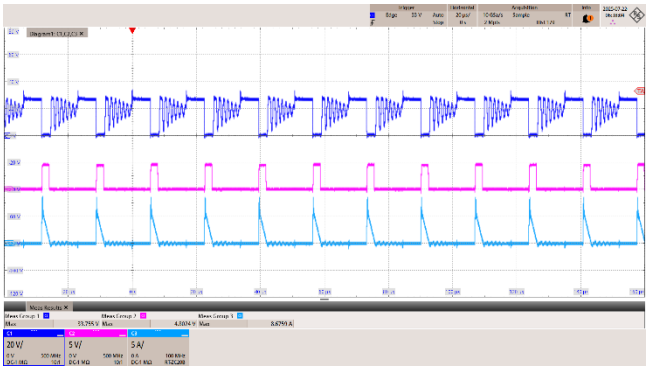


Figure 77 – 58 VAC, 60 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 20 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 5 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 33.8 V
SRFET Drain Current, Max. = 8.68 A

[14] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

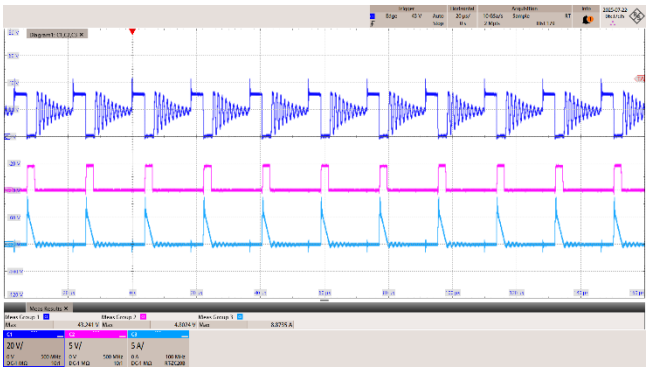


Figure 78 – 90 VAC, 60 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 20 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 5 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 43.2 V
SRFET Drain Current, Max. = 8.87 A

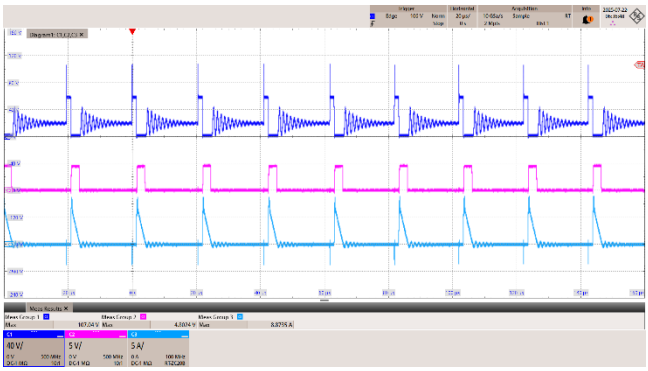


Figure 79 – 265 VAC, 50 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 40 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 5 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 107 V
SRFET Drain Current, Max. = 8.87 A

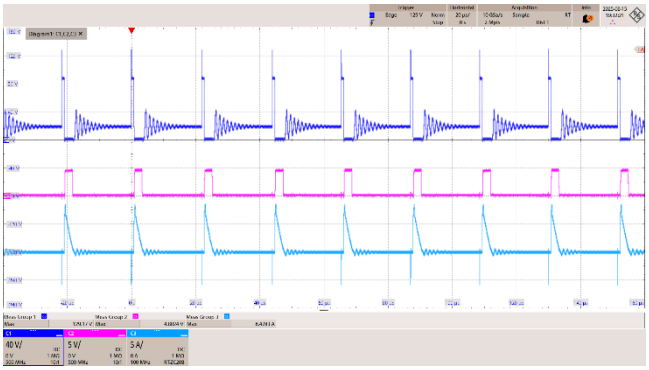


Figure 80 – 480 VAC, 50 Hz, Po = 10.9 W

Ch1: SR V_{DS}, 40 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 5 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 129 V
SRFET Drain Current, Max. = 8.48 A

11.4.2 7 V SR FET Waveforms

11.4.2.1 Start-up Operation (100% Load)

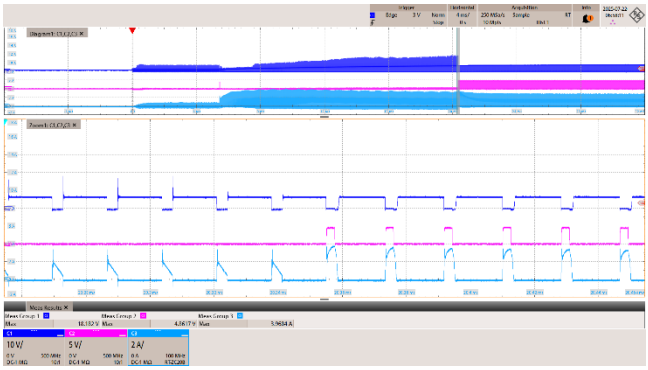


Figure 81 – 40 VDC, Po = 8.4 W[15]
Ch1: SR V_{DS}, 10 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 2 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 18.2 V
SRFET Drain Current, Max. = 3.97 A

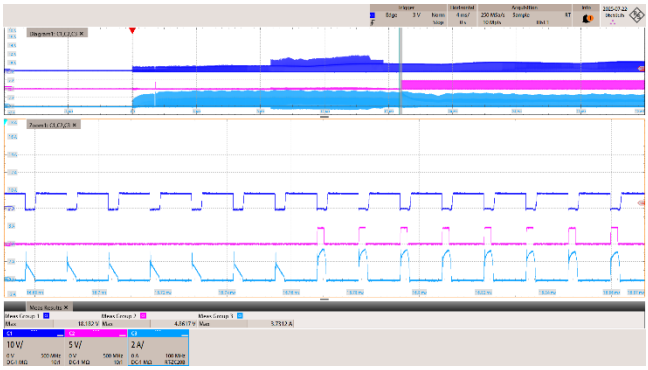


Figure 82 – 58 VAC, 60 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 10 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 2 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 18.2 V
SRFET Drain Current, Max. = 3.73 A

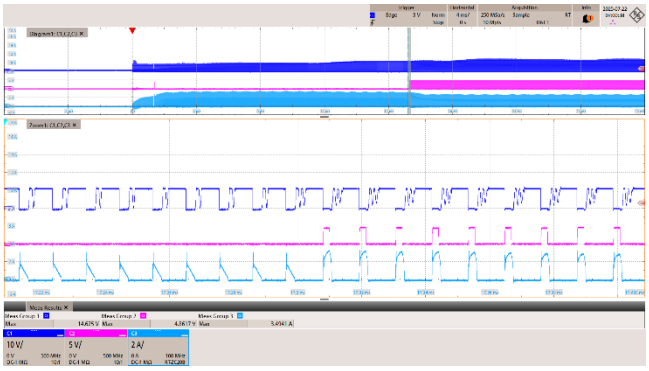


Figure 83 – 90 VAC, 60 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 10 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 2 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 14.6 V
SRFET Drain Current, Max. = 3.49 A

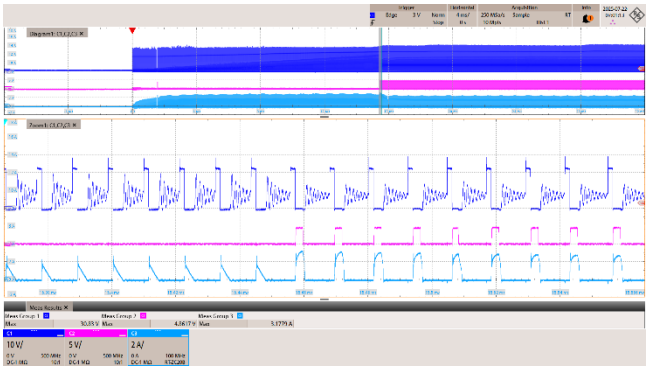


Figure 84 – 265 VAC, 50 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 10 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 2 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 30.8 V
SRFET Drain Current, Max. = 3.18 A

[15] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

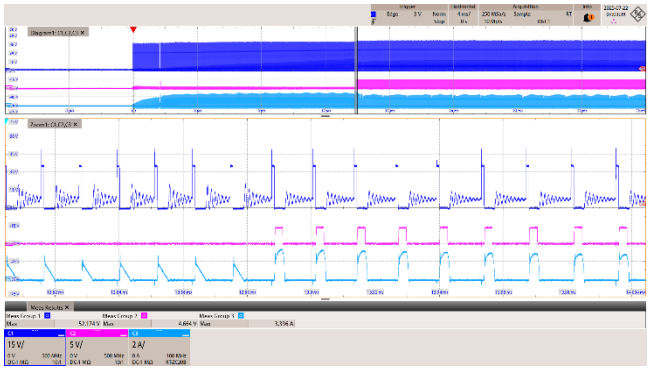


Figure 85 – 480 VAC, 50 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 15 V / div., 4 ms / div.
Ch2: SR V_{GS}, 5 V / div., 4 ms / div.
Ch3: SR I_{DS}, 2 A / div., 4 ms / div.
Zoom: 20 µs/div.
SRFET Drain Voltage, Max. = 52.2 V
SRFET Drain Current, Max. = 3.34 A

11.4.2.2 Normal Operation (100% Load)

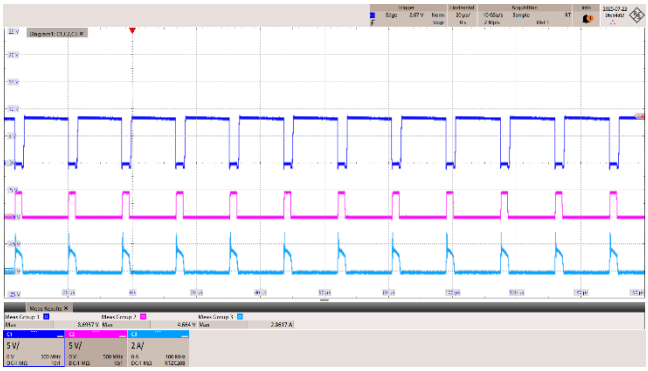


Figure 86 – 40 VDC, Po = 8.4 W[16]
Ch1: SR V_{DS}, 5 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 2 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 8.69 V
SRFET Drain Current, Max. = 2.86 A

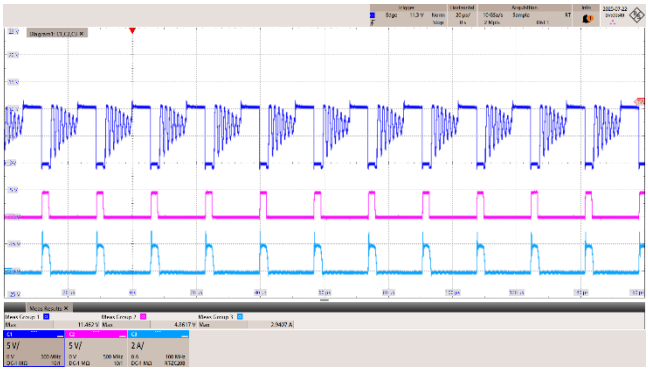


Figure 87 – 58 VAC, 60 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 5 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 2 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 11.5 V
SRFET Drain Current, Max. = 2.94 A

[16] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

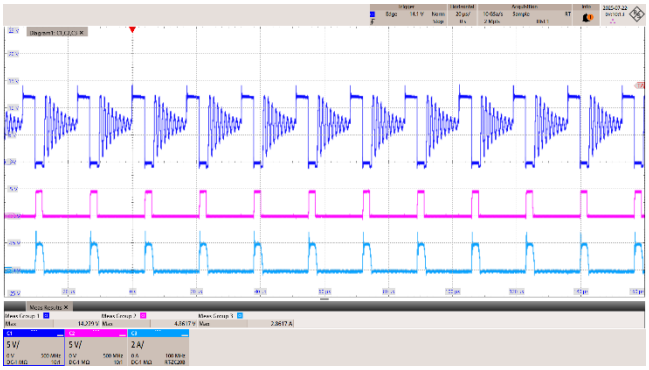


Figure 88 – 90 VAC, 60 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 5 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 2 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 14.2 V
SRFET Drain Current, Max. = 2.86 A

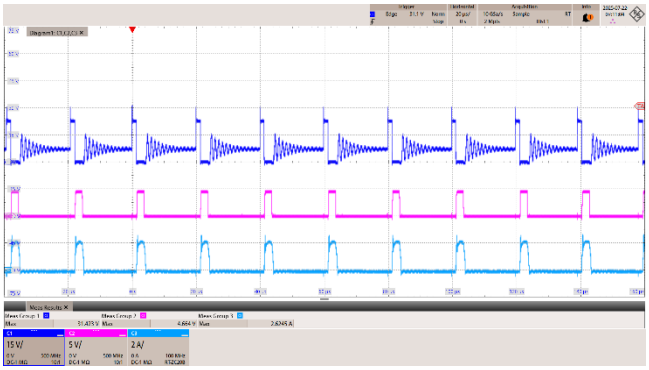


Figure 89 – 265 VAC, 50 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 15 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 2 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 31.4 V
SRFET Drain Current, Max. = 2.62 A

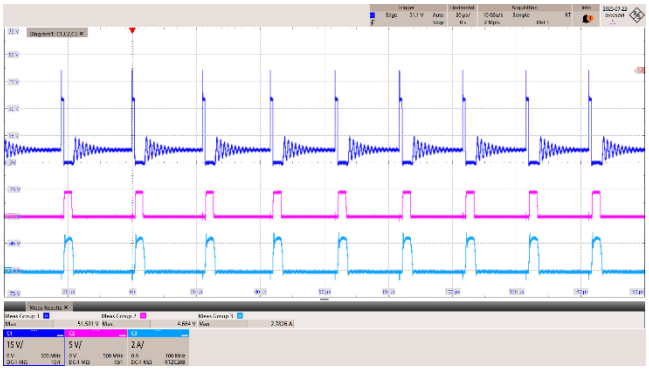


Figure 90 – 480 VAC, 50 Hz, Po = 10.9 W
Ch1: SR V_{DS}, 15 V / div., 20 µs / div.
Ch2: SR V_{GS}, 5 V / div., 20 µs / div.
Ch3: SR I_{DS}, 2 A / div., 20 µs / div.
SRFET Drain Voltage, Max. = 51.6 V
SRFET Drain Current, Max. = 2.78 A

11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4905-1 probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors are one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

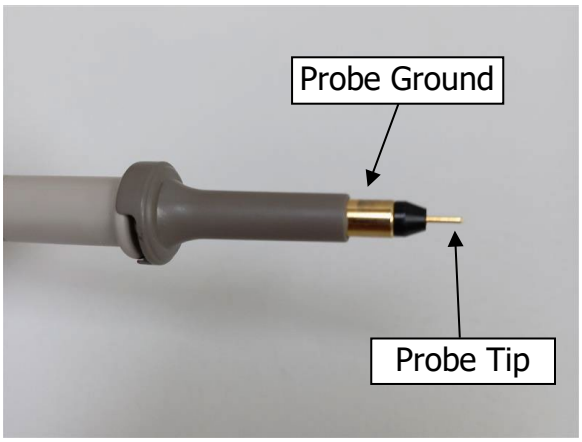


Figure 91 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

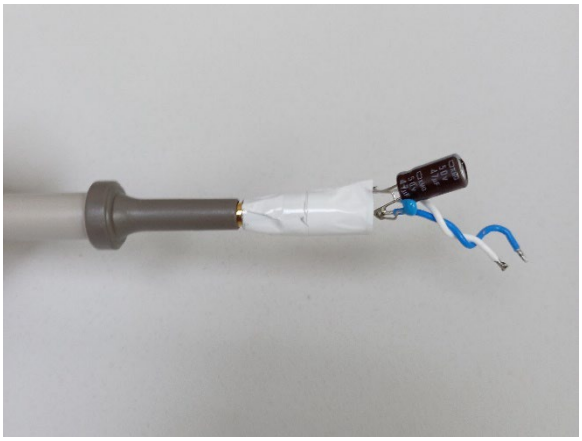


Figure 92 – Oscilloscope Probe with BNC Adapter.

(https://probemaster.com/4900-oscilloscope-probe-basic-kit-150-300-mhz/)

11.5.2 Ripple Waveforms (Measured on Board)

11.5.2.1 100% Load

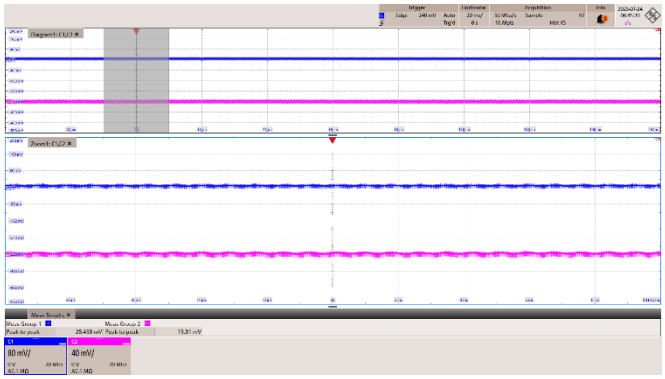


Figure 93 – 40 VDC, 100% Load.[17]
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 28.5 mV_{PK-PK}.
Measured 7V Ripple = 15.8 mV_{PK-PK}.

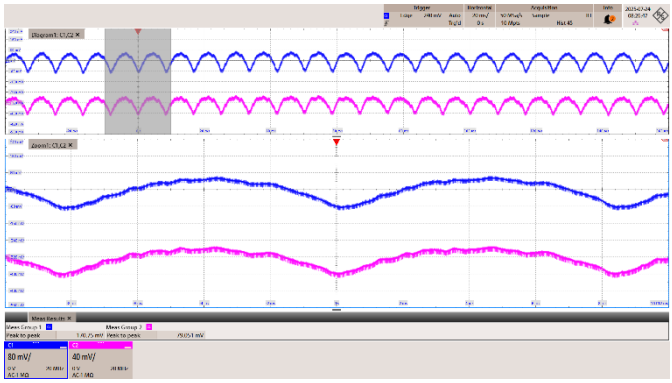


Figure 94 – 58 VAC, 60 Hz, 100% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 170 mV_{PK-PK}.
Measured 7V Ripple = 79.1 mV_{PK-PK}.

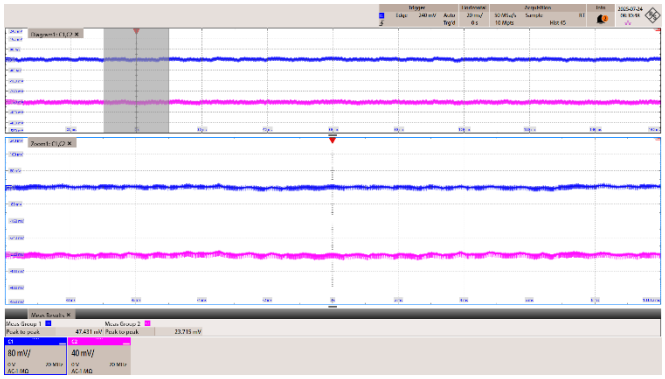


Figure 95 – 90 VAC, 60 Hz, 100% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 47.4 mV_{PK-PK}.
Measured 7V Ripple = 23.7 mV_{PK-PK}.

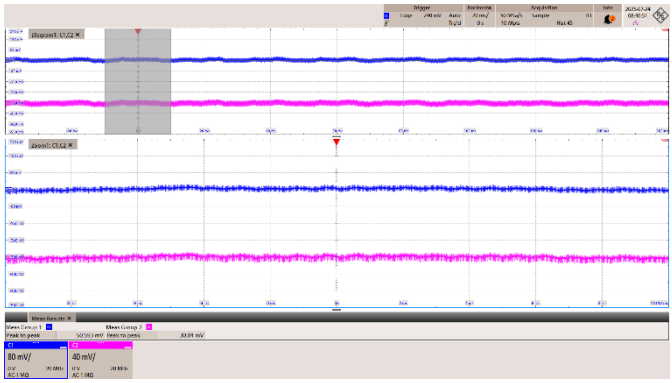


Figure 96 – 265 VAC, 50 Hz, 100% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 50.6 mV_{PK-PK}.
Measured 7V Ripple = 30.0 mV_{PK-PK}.

[17] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

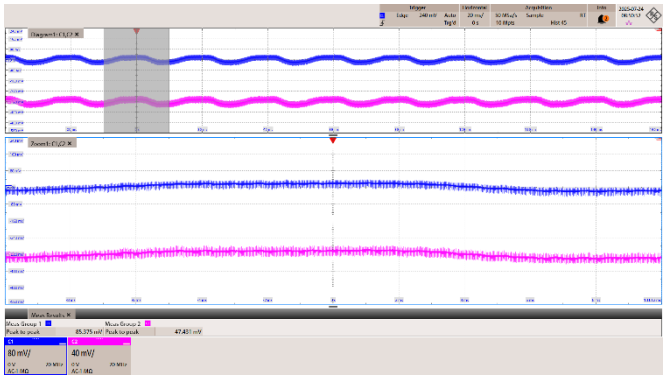


Figure 97 – 480 VAC, 50 Hz, 100% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 85.4 mV_{PK-PK}.
Measured 7V Ripple = 47.4 mV_{PK-PK}.

11.5.2.2 50% Load

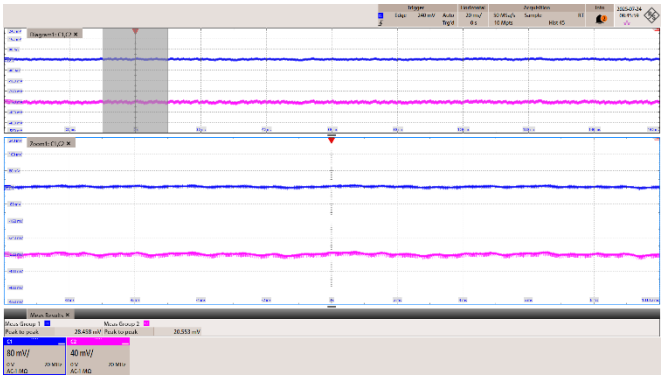


Figure 98 – 40 VDC, 50% Load.[18]
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 28.5 mV_{PK-PK}.
Measured 7V Ripple = 20.6 mV_{PK-PK}.

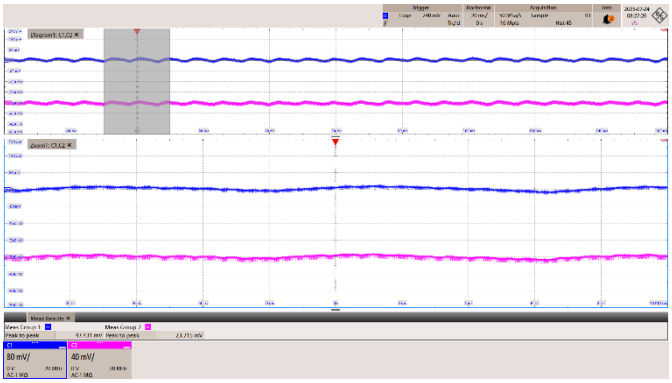


Figure 99 – 58 VAC, 60 Hz, 50% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 47.4 mV_{PK-PK}.
Measured 7V Ripple = 23.7 mV_{PK-PK}.

[18] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

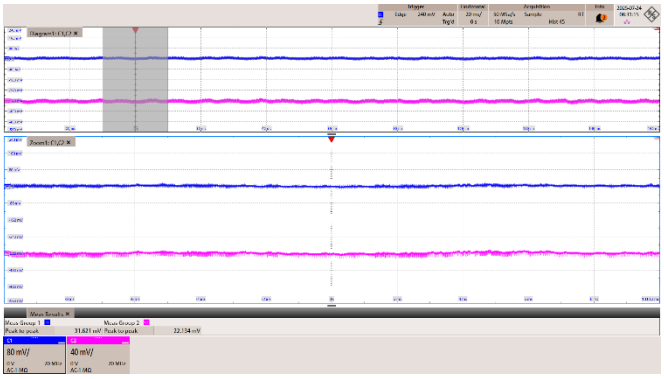


Figure 100 – 90 VAC, 60 Hz, 50% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 31.6 mV_{PK-PK}.
Measured 7V Ripple = 22.1 mV_{PK-PK}.

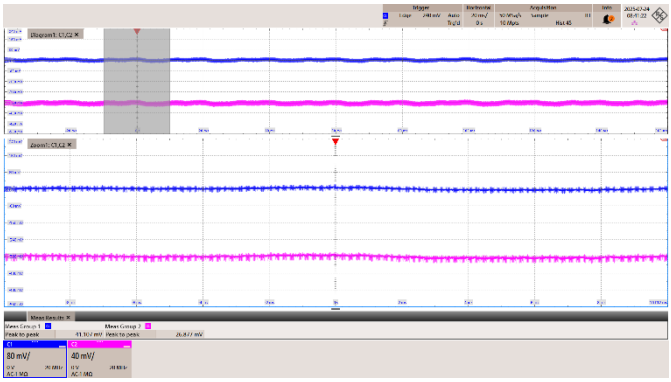


Figure 101 – 265 VAC, 50 Hz, 50% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 41.1 mV_{PK-PK}.
Measured 7V Ripple = 26.9 mV_{PK-PK}.

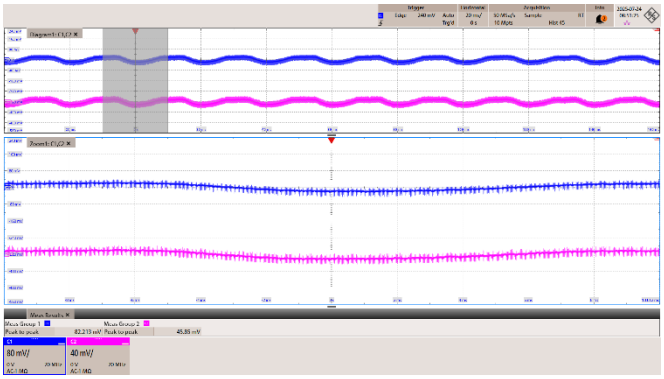


Figure 102 – 480 VAC, 50 Hz, 50% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 82.2 mV_{PK-PK}.
Measured 7V Ripple = 45.9 mV_{PK-PK}.

11.5.2.3 10% Load

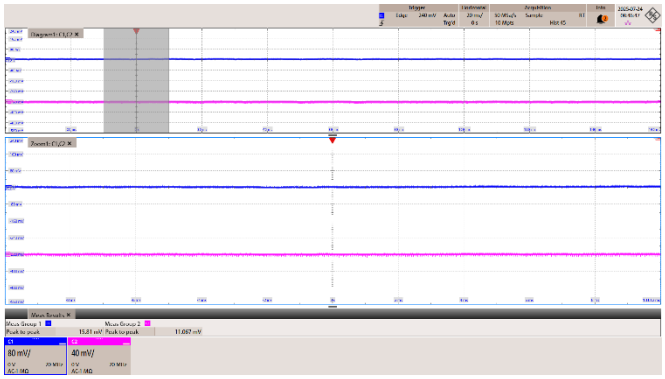


Figure 103 – 40 VDC, 10% Load.[19]
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 15.8 mV_{PK-PK}.
Measured 7V Ripple = 11.1 mV_{PK-PK}.

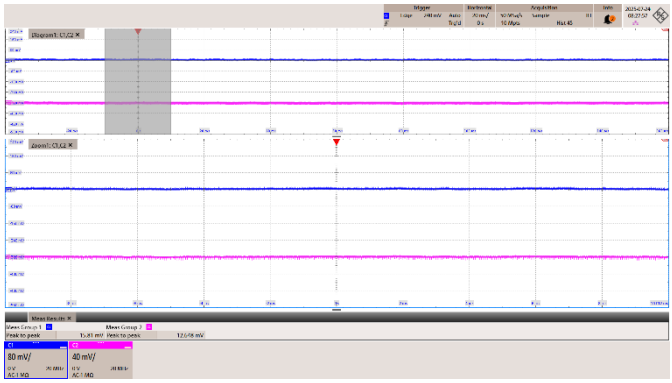


Figure 104 – 58 VAC, 60 Hz, 10% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 15.8 mV_{PK-PK}.
Measured 7V Ripple = 12.6 mV_{PK-PK}.

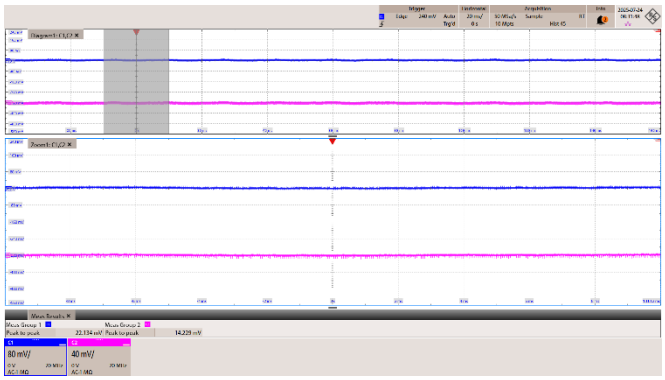


Figure 105 – 90 VAC, 60 Hz, 10% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 22.1 mV_{PK-PK}.
Measured 7V Ripple = 14.2 mV_{PK-PK}.

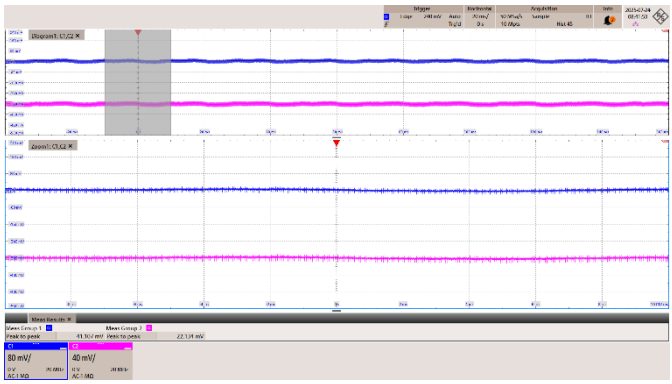


Figure 106 – 265 VAC, 50 Hz, 10% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 41.1 mV_{PK-PK}.
Measured 7V Ripple = 22.1 mV_{PK-PK}.

[19] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

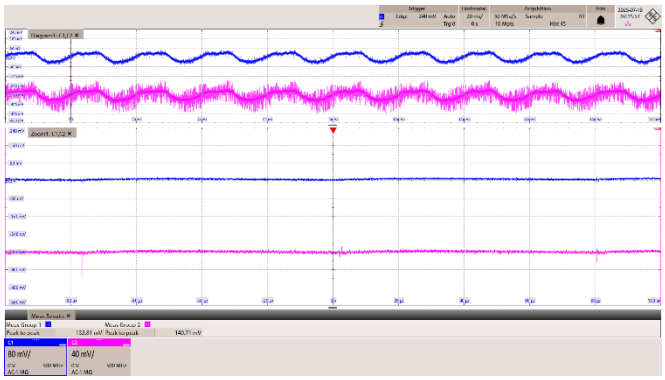


Figure 107 – 480 VAC, 50 Hz, 10% Load.
Ch1: 17.5 $V_{OUTRIPPLE}$, 80 mV / div., 20 ms / div.
Ch2: 7 $V_{OUTRIPPLE}$, 40 mV / div., 20 ms / div.
Zoom: 20 µs/div.
Measured 17.5 V Ripple = 91.7 mV_{PK-PK}.
Measured 7V Ripple = 49.0 mV_{PK-PK}.

11.5.3 Output Voltage Ripple

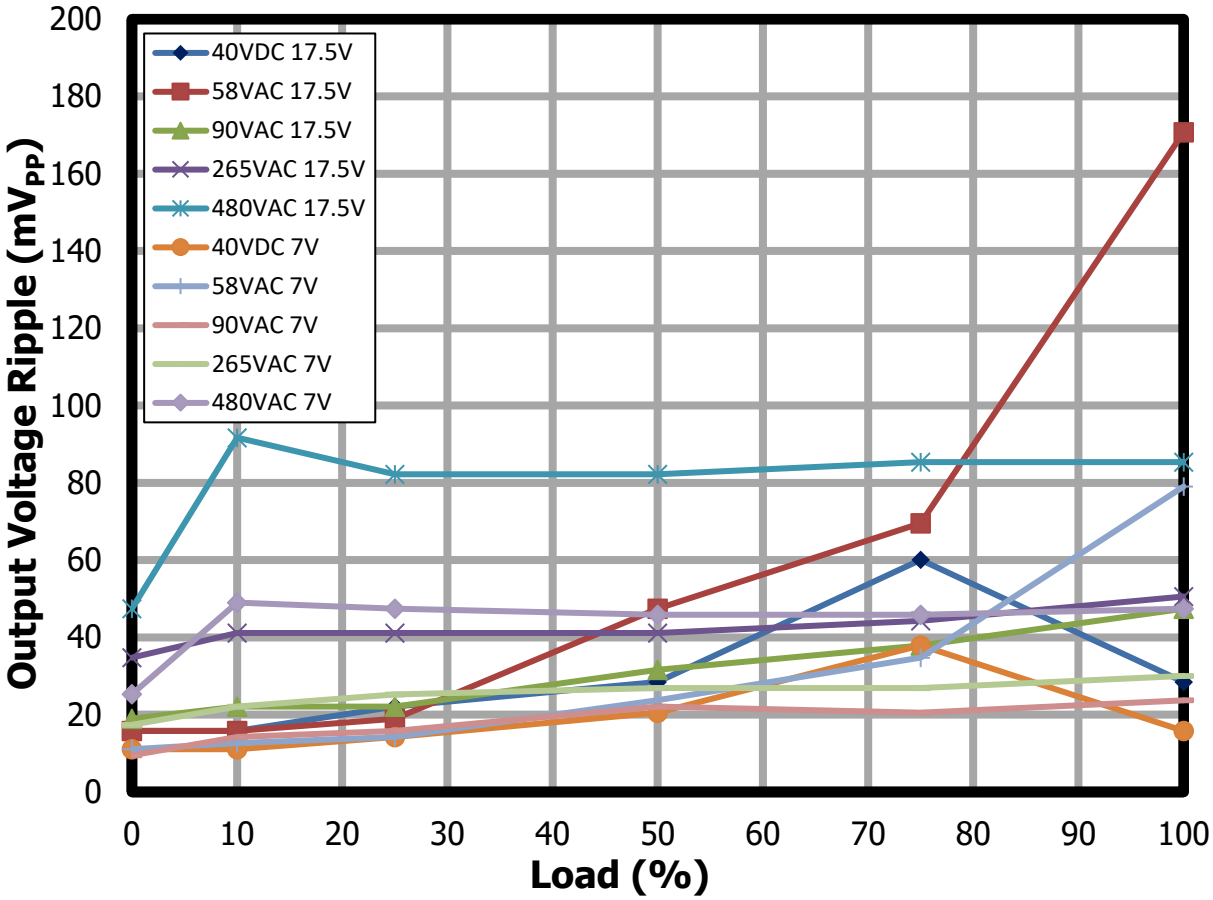


Figure 108 – Output Voltage Ripple.[20]

[20] Full load at 40 VDC input is derated to 8.4 W (7 V/0.3 A, 17.5 V/0.36 A).

12 Conductive EMI

12.1 Neutral

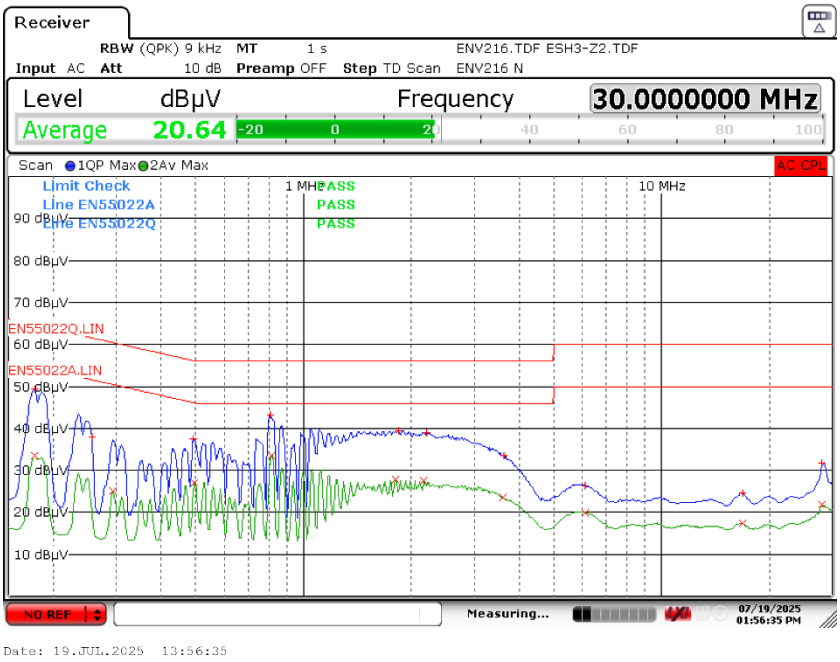


Figure 109 – Floating Ground EMI at 115 VAC, Neutral.

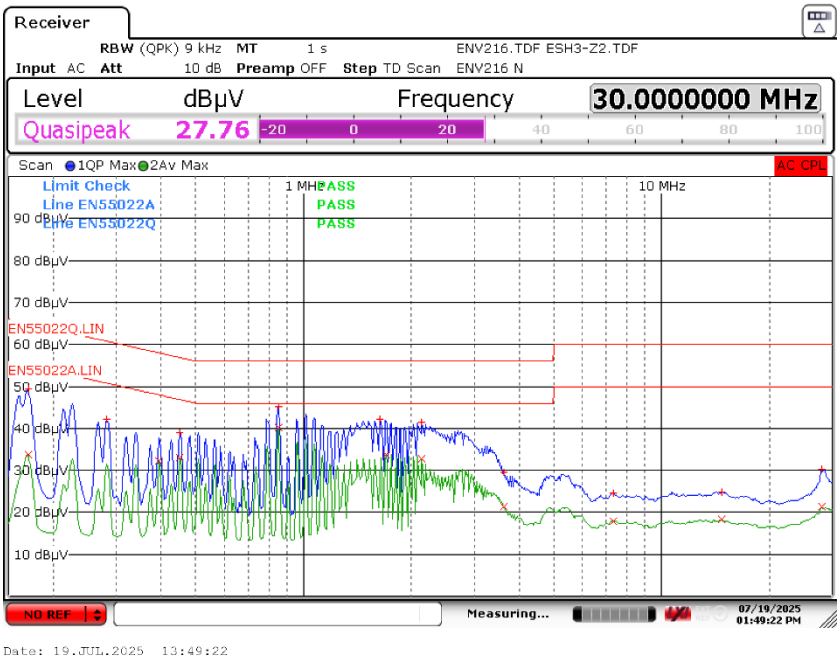


Figure 110 – Floating Ground EMI at 230 VAC, Neutral.

12.2 Line

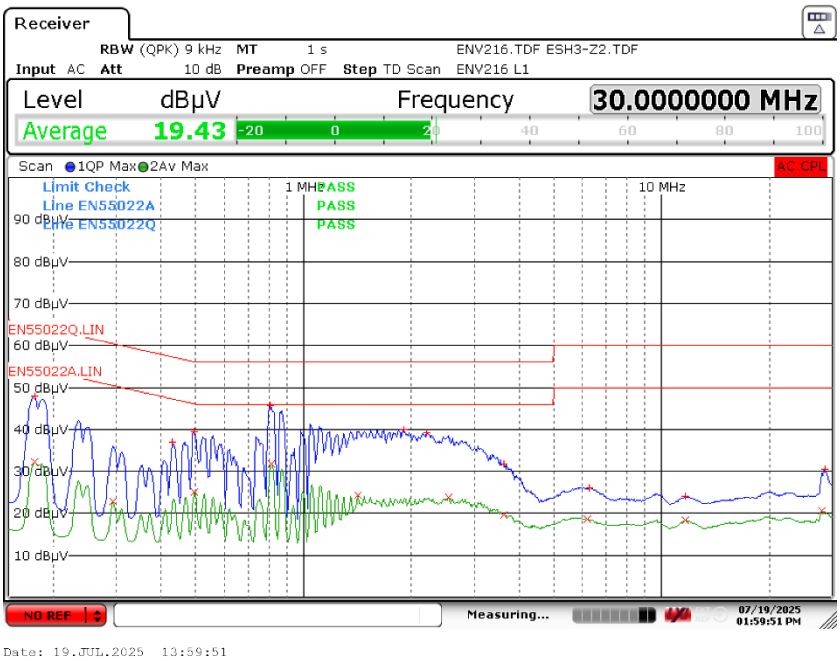


Figure 111 – Floating Ground EMI at 115 VAC, Line.

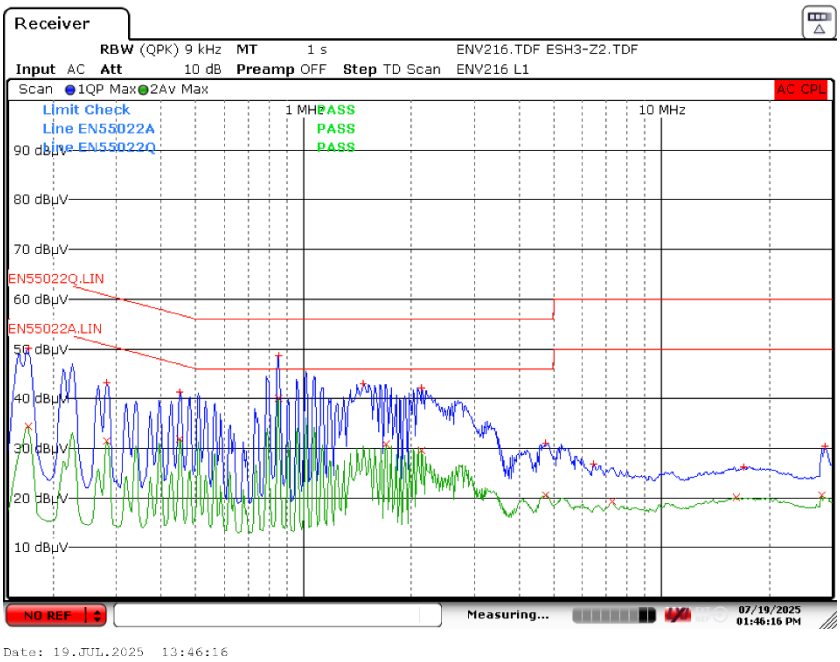


Figure 112 – Floating Ground EMI at 230 VAC, Line.

13 Line Surge

13.1 Differential Mode Test

Surge Voltage (V)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+2500	90	L, N	2	10	PASS
–2500	90	L, N	2	10	PASS
+2500	180	L, N	2	10	PASS
–2500	180	L, N	2	10	PASS
+2500	270	L, N	2	10	PASS
–2500	270	L, N	2	10	PASS

Table 21 – Test Data at 2.5 kV Differential Surge.

13.2 Ring Wave Surge

Surge Voltage (V)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	90	L, N → PE	12	10	PASS
–6000	90	L, N → PE	12	10	PASS
+6000	180	L, N → PE	12	10	PASS
–6000	180	L, N → PE	12	10	PASS
+6000	270	L, N → PE	12	10	PASS
–6000	270	L, N → PE	12	10	PASS

Table 22 – Test Data at 6 kV Ring Wave Surge.

14 EFT

Surge Voltage (V)	Phase Angle (°)	IEC Coupling	Frequency (kHz)	Burst Time	Reception Time (ms)	Step Duration (s)	Result
+4000	90	L, N - PE	5	15 ms	300	120	PASS
–4000	90	L, N - PE	5	15 ms	300	120	PASS
+4000	180	L, N - PE	5	15 ms	300	120	PASS
–4000	180	L, N - PE	5	15 ms	300	120	PASS
+4000	270	L, N - PE	5	15 ms	300	120	PASS
–4000	270	L, N - PE	5	15 ms	300	120	PASS
+4000	90	L, N - PE	100	750 µs	300	120	PASS
–4000	90	L, N - PE	100	750 µs	300	120	PASS
+4000	180	L, N - PE	100	750 µs	300	120	PASS
–4000	180	L, N - PE	100	750 µs	300	120	PASS
+4000	270	L, N - PE	100	750 µs	300	120	PASS
–4000	270	L, N - PE	100	750 µs	300	120	PASS

Table 23 – Test Data at 4 kV EFT.

15 Electrostatic Discharge (ESD)

Passed ±16.5 kV air discharge and ±8.8 kV contact discharge at both output positive and negative terminals, under full load condition for both 115 VAC and 230 VAC.

15.1 Contact Discharge at 115 VAC and 230 VAC

Contact Discharge (kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+2	V_{OUT} (+17.5 V)	10	0/10	PASS
-2		10	0/10	PASS
+2	V_{OUT} (+7 V)	10	0/10	PASS
-2		10	0/10	PASS
+2	V_{OUT} (-)	10	0/10	PASS
-2		10	0/10	PASS
+4	V_{OUT} (+17.5 V)	10	0/10	PASS
-4		10	0/10	PASS
+4	V_{OUT} (+7 V)	10	0/10	PASS
-4		10	0/10	PASS
+4	V_{OUT} (-)	10	0/10	PASS
-4		10	0/10	PASS
+6	V_{OUT} (+17.5 V)	10	0/10	PASS
-6		10	0/10	PASS
+6	V_{OUT} (+7 V)	10	0/10	PASS
-6		10	0/10	PASS
+6	V_{OUT} (-)	10	0/10	PASS
-6		10	0/10	PASS
+8	V_{OUT} (+17.5 V)	10	0/10	PASS
-8		10	0/10	PASS
+8	V_{OUT} (+7 V)	10	0/10	PASS
-8		10	0/10	PASS
+8	V_{OUT} (-)	10	0/10	PASS
-8		10	0/10	PASS
+8.8	V_{OUT} (+17.5 V)	10	0/10	PASS
-8.8		10	0/10	PASS
+8.8	V_{OUT} (+7 V)	10	0/10	PASS
-8.8		10	0/10	PASS
+8.8	V_{OUT} (-)	10	0/10	PASS
-8.8		10	0/10	PASS

Table 24 – Test Data at 115 VAC and 230 VAC.

15.2 Air Discharge at 115 VAC and 230 VAC

Air Discharge (kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+8	V_{OUT} (+17.5 V)	10	0/10	PASS
-8		10	0/10	PASS
+8	V_{OUT} (+7 V)	10	0/10	PASS
-8		10	0/10	PASS
+8	V_{OUT} (-)	10	0/10	PASS
-8		10	0/10	PASS
+10	V_{OUT} (+17.5 V)	10	0/10	PASS
-10		10	0/10	PASS
+10	V_{OUT} (+7 V)	10	0/10	PASS
-10		10	0/10	PASS
+10	V_{OUT} (-)	10	0/10	PASS
-10		10	0/10	PASS
+12	V_{OUT} (+17.5 V)	10	0/10	PASS
-12		10	0/10	PASS
+12	V_{OUT} (+7 V)	10	0/10	PASS
-12		10	0/10	PASS
+12	V_{OUT} (-)	10	0/10	PASS
-12		10	0/10	PASS
+14	V_{OUT} (+17.5 V)	10	0/10	PASS
-14		10	0/10	PASS
+14	V_{OUT} (+7 V)	10	0/10	PASS
-14		10	0/10	PASS
+14	V_{OUT} (-)	10	0/10	PASS
-14		10	0/10	PASS
+15	V_{OUT} (+17.5 V)	10	0/10	PASS
-15		10	0/10	PASS
+15	V_{OUT} (+7 V)	10	0/10	PASS
-15		10	0/10	PASS
+15	V_{OUT} (-)	10	0/10	PASS
-15		10	0/10	PASS
+16.5	V_{OUT} (+17.5 V)	10	0/10	PASS
-16.5		10	0/10	PASS
+16.5	V_{OUT} (+7 V)	10	0/10	PASS
-16.5		10	0/10	PASS
+16.5	V_{OUT} (-)	10	0/10	PASS
-16.5		10	0/10	PASS

Table 25 – Test Data at 115 and 230 VAC.

16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
31-Jul-2025	SNZ	A	First Release	PI Expert & Mktg
20-Aug-2025	SNZ	B	Updated components in Schematic and BOM and updated Figures 58, 75 and 80	PI Expert & Mktg

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